An Implantable Stimulator for Selective Stimulation of Nerves

By

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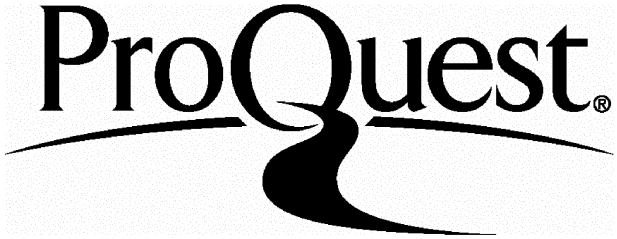

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ABSTRACT

Acute experimentation performed at many centres over the last twenty years has shown techniques which allow small neurones to be stimulated without large, the reverse of the normal recruitment order usually encountered during electrical stimulation; one-way excitation of neurones; and excitation of only a region of a nerve. These techniques should improve neural prosthesis by, for example: avoiding pain during stimulation and requiring electrode sites and therefore fewer incisions.

To enable chronic clinical experiments of these advanced methods, there is a need for a specialised chronically-implantable stimulator, which can control either dipolar, tripolar or pentapolar nerve cuff electrodes. This thesis is concerned with the design and development of such a stimulator and, in particular, a fully customised analogue integrated circuit that converts incoming digital words into corresponding stimulation currents.

A binary word is transmitted to the implant, which defines the current waveform parameters for the electrodes. This word is loaded into a shift register at the input. Part of the word is presented to a digital to analogue converter, to specify stimulation amplitude, and a pulse generator, which generates either a quasi-trapezoidal, or a square shaped stimulation waveforms. Four novel low offset linear transconductors provide the stimulation currents that are switched to the desired outputs. The charge balancing of the stimulation waveform is realised by a very long time-constant switched capacitor integrator.

The major difficulties in the design of the analogue full custom IC proved to be the linear transconductor stages and the integrator. Results for the test ICs are presented and the design of a complete stimulator system is described.

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Chapter 1. Introduction

1.1 History of Implanted Stimulators for FES

The following gives a brief history of the major developments affecting neuroprostheses. A more detailed history can be found in "Neural Prosthesis" by Agnew and McCreery [3].

In the eighteenth century, investigators such as Benjamin Franklin [59] and others demonstrated that the output of frictional electricity machines could cause the contractions of muscles. However, no long-term recovery effects were observed and the experiments were not utilised for functional stimulation. Galvani [60] suggested in 1791 that, nerves and muscles utilised electricity to function. In the early nineteenth century, Volta [152] developed the battery and demonstrated that the electricity it produced could cause muscular contractions.

Electrical developments in the nineteenth century allowed the development of the faradaic stimulator (or induction coil stimulator), which consisted of a battery connected to a primary coil via a mechanically timed switch and a secondary coil with many more turns than the primary. This device allowed tetanic (i.e. continuos) muscle contractions rather than single twitches as generated previously. In 1867, Duchenne described a development of these techniques in which moistened surface electrodes were used to study the functional anatomy of individual muscles [53].

The development of electronic devices, such as the diode and triode, from the beginning of the twentieth century allowed the development of improved electrical oscillators, pulsed circuits and amplifiers for neuro-physiological studies. The invention of the much smaller transistor in 1947, and its later incorporation in integrated circuits, allowed the realisation of implantable stimulator systems. During the early 1930s, the use of a secondary induction coil, placed beneath the skin was published [32,86]: this method removed the danger of infection associated with percutaneous wires. Using radio frequency carriers and rectification increased the efficiency of these systems. These advances allowed the development of a totally implantable heart pacemaker [62], as reported in 1959. Heart pacemakers have since developed into battery powered devices with highly integrated electronics to allow advanced functions such as adaptive pacing so the heart can beat at different rates depending on conditions.

Phrenic nerve [63,79,145] and bladder stimulators [14,15], for breathing and bladder emptying respectively, based on radio-frequency magnetic induction, as used in the early pacemaker [4,74], appeared during the 1960s and 1970s and the commercial devices in use today are very little changed, in concept, from the initial devices and contain only a few discrete components. These devices all suffer from the problem that the pulse amplitude is not well controlled as the stimulation amplitude varies with the coupling between the coils. A second problem with these devices is that each stimulation channel requires separate coils and components, physically limiting the maximum number of stimulation channels.

An implantable single channel cochlea stimulator was first reported in 1957 [42]. In the past thirty years cochlea stimulators have undergone major developments and commercialisation, and are probably the most developed and clinically accepted [36,42] implanted stimulator after the pacemaker.

In 1961 Liberson introduced restoration of function to paralysed muscles using functional neuromuscular stimulation (FNS), with the development of a non-implanted peroneal nerve stimulator for the treatment of foot drop in hemiplegic patients [84]. This device was the first stimulator system to include closed-loop feedback control in the form of a heel switch placed inside the shoe. Long *et al* [85] reported an electrophysiological splint for the hand in 1963. However, although both of these applications demonstrated the potential for FNS they were not widely accepted by patients [129]. The development of hermetic packages suitable for implanted devices allowed the implantation of the complex semiconductor devices such as multi-channel stimulators. These have addressed the problem of size, complexity and accurate control, allowing devices for the restoration of hand-grasp in tetraplegics [104,129,130] to start to gain clinical acceptance [102]. Multi-channel stimulators have also allowed the investigation of the restoration of standing and walking in paraplegics [47]. One such multi-channel device for standing (and limited stepping) is the LARSI (Lumber Anterior Root Stimulator) system developed in the Implanted Devices Group at University College London (formerly at the MRC Neurological Prosthesis Unit) and is described in 1.3.

To summarise: Implanted FES systems for the restoration of muscle functions have been used since 1961. They are established in clinical practice for phrenic pacing [7,8,64], bladder emptying [18,24,119], standing [47,50] and hand grasp [80,102-104].

These devices typically use approximately square shaped stimulation pulses and electrodes of various designs (epimysial electrodes placed directly on muscle motor points [80], nerve cuffs either closed or helical shaped [92] and root cuff (or book) electrodes placed directly on nerve roots inside the dura [92]. These conventional FNS systems suffer from several shortcomings described below.

1.2 Shortcomings of existing stimulators

1.2.1 Electrode Siting

Peripheral Motor nerve fibres (neurones) emerge from the spinal cord at nerve roots within the spinal canal, pass through spine, and join to form nerve trunks, some passing through plexi. The nerve trunks, which are of various sizes, are routed towards groups of muscles and branch out near the muscles. The peripheral nervous system is aptly described like a tree with roots, trunks, branches and twigs. Close to a muscle, the nerve will finally branch to just the fibres innervating that particular muscle. This means that to individually stimulate just one muscle, the electrodes must be placed in close proximity to this branch. For example in the Freehand System [96] which requires fine control of individual muscles to restore hand grasp in tetraplegic SCI patients, epimysial electrodes are located on individual muscles to obtain fine control. In paraplegic, paralysed muscles should be stimulated in the lower back, buttocks, thighs and calves, so very extensive surgery is required using epimysial or nerve twig electrodes. This is a major disadvantage. A method of placing the electrodes more centrally while retaining control over individual muscles or small groups of muscles is therefore desirable.

Stimulating regions of a nerve trunk should allow the selective activation of the muscles innervated by a nerve [88,133] (as inside a nerve the fibres innervating an individual muscle are grouped functionally in fascicles [133]). By using multipolar nerve cuffs this selective recruitment may be possible [88], allowing this selective stimulation of individual muscles innervated by a nerve. If practicable, this would mean that fewer electrodes would have to be implanted during surgery and the electrodes could be placed more centrally to the body, reducing the amount of associated cabling.

1.2.2 Inverse Recruitment of Nerve Fibres

During 'normal' voluntary muscle contraction, motor units are recruited with a specific recruitment order in which the first units to be recruited are slow, low-force, fatigue-resistant units, innervated by small nerve fibres, followed by fast, high-force,

fast-fatigable units. This is thought to be due to the need for fine control of movement at low force levels and less fine control for high-force fast movements. It also gives greater endurance for continuous (postural) tasks while allowing rapid response and larger forces for dynamic activities. This orderly recruitment of neurones by diameter is known as the 'Size Principle' [34,35,87].

However, this normal pattern of recruitment does not occur during electrical stimulation due to the inverse relationship that exists between the excitability of an axon and its diameter. Blair and Erlanger [13] established that during electrical stimulation larger nerve fibres have lower excitation thresholds than smaller nerve fibres, this is known as 'Inverse Recruitment' [34]. It follows that FES produces fast-fatiguing muscle contractions, which is undesirable. Related to this, in some applications such as the stimulation of bladder (and bowel), it is desirable to selectively activate the small (parasympathetic) fibres (e.g. innervating the smooth muscle of the bladder wall) whilst avoiding activation of the larger (somatic) fibres (e.g. innervating the external sphincter). Using conventional implantable nerve stimulators, this is not possible due to the inverse recruitment characteristic and consequently supra-normal bladder pressures are observed during stimulation.

The phenomenon of anodal blocking allows a 'normal' recruitment pattern during stimulation using specially shaped stimulation waveforms and close fitting nerve cuffs. With anodal blocking the conduction of action potentials in the larger nerve fibres can be blocked at a lower threshold than the smaller fibres, so that action potentials only propagate in the smaller nerve fibres during stimulation.

1.2.3 Pain and Unwanted Reflex Activity

Peripheral nerves carry both sensory and motor nerve fibres. During conventional stimulation both types of fibres are excited. This has two disadvantages; the first is that in people with intact central sensory pathways, pain may be felt during stimulation (and has been reported in some cases with the use of bladder stimulators [17,18]. The second problem is the generation of unwanted reflexes generated in the spinal cord due to excitation of sensory fibre stimulation.

Anodal blocking also makes possible the generation of unidirectional propagating action potentials (UPAPs) using asymmetrical nerve cuffs. The ability to generate UPAPs in the relevant neurones would mean that unwanted reflexes and pain should be

avoidable. Also sensation during stimulation can be prevented, allowing the implantation of stimulators in people with intact sensory innervation.

1.3 The LARSI Stimulator

The LARSI (Lumbar Anterior Root Stimulator Implant) stimulator system [44] was developed to allow stimulation of spinal roots to restore standing function in paraplegics (and some limited stepping). This device can control up to 32 pseudo-tripolar (dipolar) book electrodes[1]. A simplified overview of the LARSI system is shown in Figure 1.

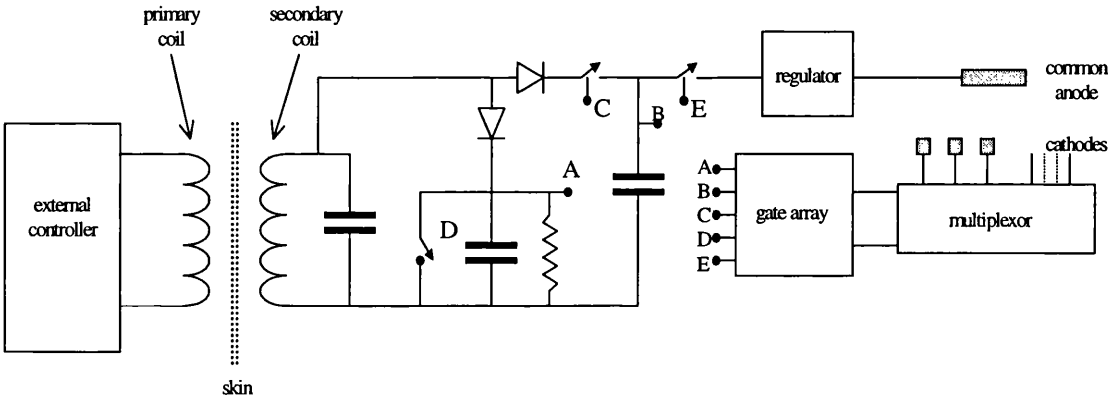

Figure 1. Overview of the LARSI stimulator

As the new stimulator device is being developed in the Implanted Devices Group, several of the key concepts are being carried over to the selective stimulator design.

The LARSI implant consists of passive components, a voltage regulator to control the stimulator current to the electrodes, a gate array performing digital control functions and a multiplexor to switch stimulation channels. Power is transmitted to the implant using RF tuned coils. The carrier is 100% amplitude modulated, using a non-linear pulse-interval modulation, in which each interval determines the length of the corresponding stimulation pulse. The demodulated signal in the implant at point A (Figure 1) is fed to the gate array, which generates the stimulus pulse widths as a series of pulses. Energy is stored by a capacitor at point B and this voltage is regulated to supply a common anode for all the electrodes. The stimulation pulses are switched by a multiplexor to the

[1] Book electrodes are multiple trough shaped nerve cuffs. The spinal roots are laid between the 'pages'

individual cathodes. Each cathode has a blocking capacitor attached to it for safety reasons (to prevent electrochemical damage).

This device has several characteristics that will be discussed in the following sections that will be used in the new device.

1.3.1 Handshaking

To prevent 'small pulses' due to insufficient stored energy in the storage capacitor (caused by a smaller than expected output load or a low storage capacitor voltage), handshaking is used in the LARSI device. The voltage on the storage capacitor inside the implant is monitored by the gate array (at point B) and stimulation pulses are only begun when this voltage is sufficiently high. If this voltage is already high at the beginning of the charging period, a signal is sent immediately from the implant to the external controller to allow stimulation to begin. This handshaking is performed by briefly shorting the receiving coil using switch D. This creates a glitch in the transmitter current, which can be detected by the controller. If no acknowledgement signal is sent, the internal storage capacitor voltage is taken to be too low and the transmitter continues to transmit energy until this acknowledgement is received. The effect of this handshaking is that the train of pulses modulating the transmitter is stretched, so the stored charge is sufficient to supply all of the stimulation pulses.

1.3.2 Use of Blocking Capacitors to avoid Electrolysis

Figure 2 shows the output stage of the LARSI stimulator with the blocking capacitor. During the stimulation phase, the transistor is turned on and most of the potential AB is applied between the anode and the cathode. The reasons for having these capacitors is Maximal charge can be injected through an electrode without causing irreversible electrochemical reactions [49,52] and direct current cannot flow in the event of a fault occurring in the implant.

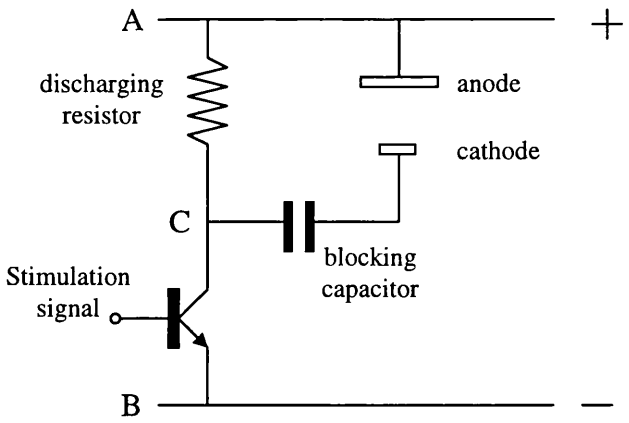

Figure 2. Output stage of the LARSI stimulator

The presence of a blocking capacitor limits the injectable charge to $V_{AB}C_{blocking}$. The capacitor itself may fail (e.g. dendrites shorting out the capacitor if moisture penetrates the package) however this would not make the system unsafe for a single fault condition.

1.3.3 Coupling Measurement/Compensation

The series regulator in the device is needed to smooth small ripple on the storage capacitor voltage. It is not meant to accommodate the gross changes that occur due to changes in the coupling coefficient. The LARSI device uses coupling compensation to keep the voltage on the storage capacitor close to the desired value. The coupling can be calculated, by measuring the total resistance in the transmitter circuit, if the load resistance on the secondary coil is known. However for the stimulator, this is generally not the case as the apparent load resistance depends on the rate of change of storage capacitor voltage. This problem is overcome by using switch C (Figure 1) to temporarily disconnect the storage capacitor from the secondary coil. In that case, the only load connected to the secondary coil is now the demodulator components, which behave as a linear load. This new circuit settles to a steady state in less than 500μs, after which time, the current in the transmitter is used to calculate the coupling. This measurement is used to vary the transmitter voltage and so control the voltage on the storage capacitor inside the implant, a form of feedback described as coupling compensation.

This measurement is also used to decide when the coils have moved too far out of alignment and to cut off the stimulator. It also allows the controller to inform the user how well the coils are aligned (so they can minimise the power used by the transmitter)

and warn the user if the coupling is approaching the cut-off point (allowing the user to realign the coils before the stimulation fails) [43].

1.3.4 Minimised Power Losses

The stimulator only has to be active during stimulation, this typically can be of the order of 15% if the total time [45]. During the remaining 85%, the stimulator is simply waiting for the next stimulation train. During this period, it is desirable that the storage capacitor does not discharge, as this energy will have to be restored before stimulation, and the power supply for the gate array must also maintains its voltage. The Mark IV LARSI minimised the load on the capacitor by using switch E to disconnect the series regulator from the storage capacitor. The device also disables that main oscillator, used by the gate array for all timing functions, to reduce the loading when the stimulator is passive.

1.4 New stimulators for FES

Clearly there is considerable potential for improved FES systems, if the stimulators are made more versatile in selectivity and recruitment. An ideal system would allow the recruitment of nerve fibres according to their size, allowing a 'natural' pattern of recruitment or the reverse, generate action potential that propagate in only one direction to prevent unwanted reflexes and allow the selective activation of regions of a nerve trunk. All three of these characteristics may not be possible together but the implantable stimulator system need not limit what can be achieved in clinical application.

Strangely, methods for overcoming all of these three shortcomings have been described (Chapter 2). However, none have been used clinically because implantable stimulators for these methods are not available. This lack of availability may be due to the relatively complex electronic design required for these stimulators.

1.5 This Thesis

The work described in this thesis is concerned with the design and development of an implantable selective nerve stimulator. This device should be capable of selective stimulating either by fibre position, fibre size or to launch action potentials in one direction only, whilst using nerve cuff electrodes. This thesis describes:

i) A literature review of Selective Stimulation

ii) Specification for a selective Stimulator

iii) Design and testing of Integrated Circuits

iv) Proposed applications for the system and a description of a complete stimulator system.

v) Conclusions

Chapter 2. Selective Stimulation

2.5 Introduction

2.5.1 Neurophysiology

The nervous system is a network of cells designed for the rapid transfer and integration of information. It consists of two main parts; i) the Central Nervous System (CNS), the brain and spinal cord, and ii) the Peripheral Nervous System, that transmits information to and from the CNS. This is shown in the flow diagram of Figure 3.

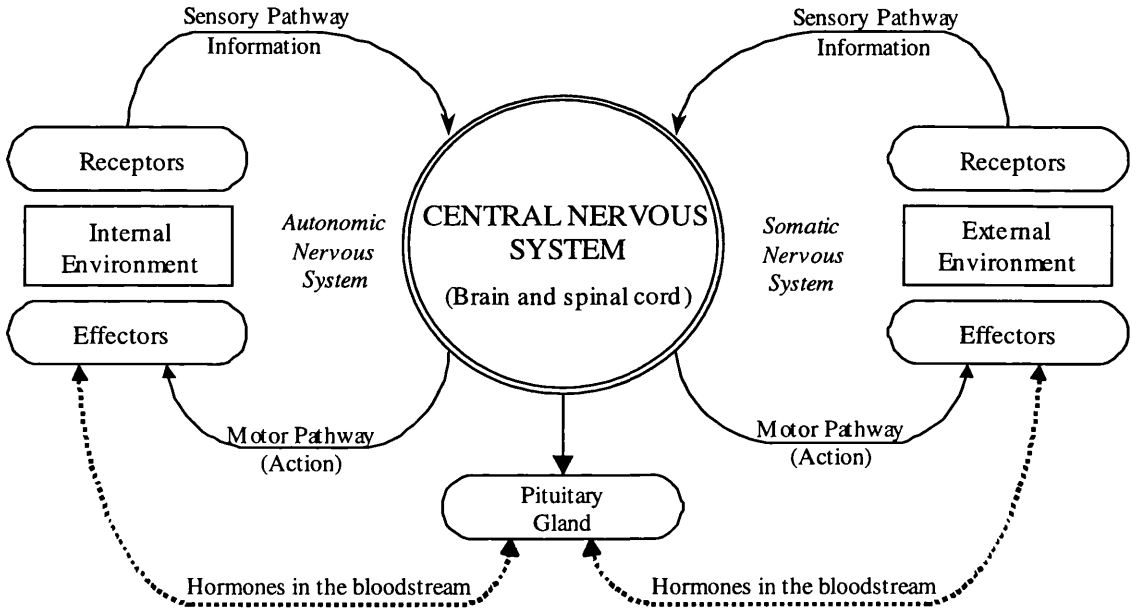

Figure 3. The nervous system

2.5.2 Peripheral Nerves

The signals carried in the four 'pathways' of Figure 3, are transmitted by neurones (nerve cells) in nerves. Peripheral neurones can be classified into two types, *motor* and *sensory*. Motor neurones have their cell bodies in the CNS. The motor axons (the elongated part of the cell) emerge from the spinal cord in the ventral roots as shown in Figure 4 and run along nerve trunks to terminate in muscles. The muscle is activated by action potentials from the nerve reaching the motor end plate[2], and propagating through the muscle. Sensory neurones have their cell body in the dorsal root ganglion ('spinal

[2] Motor end plate is the interface between the neuron and the muscle.

ganglion' in Figure 4), and carry information from receptors to the CNS, via the dorsal roots. The spinal cord is surrounded by cerebro-spinal fluid contained inside a membrane called the dura. The space inside the dura is the spinal canal, in which the sensory and motor roots are separate. However, outside the dura, the roots coalesce into peripheral nerves, which are transmitting information in both peripheral and cordal directions.

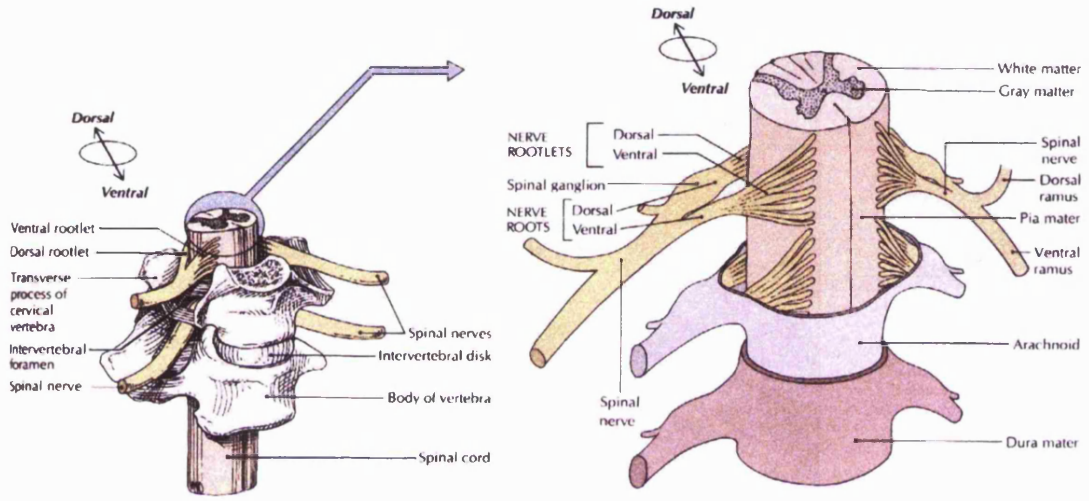

Figure 4. Cross section spinal showing dorsal and ventral root locations (modified from[31]).

2.5.3 The Cell

Every cell is surrounded by a plasma membrane that separates it from the extra-cellular region. The plasma membrane acts as a selectively permeable barrier, which allows the cell to maintain a cytoplasmic composition very different from the extra-cellular fluid. The plasma membrane contains enzymes, receptors and antigens that allow the cell to interact with other cells [11,97]. In the cell membranes, the most abundant constituents are phospholipids and proteins. A phospholipid molecule consists of a polar head group and two non-polar, hydrophobic fatty acyl chains. In water, phospholipids form structures that prevent the fatty acyl chains having contact with water. In cells, the lipids are arranged as a bilayer structure that keeps the fatty acyl chains away from contact with water. This is shown Figure 5.

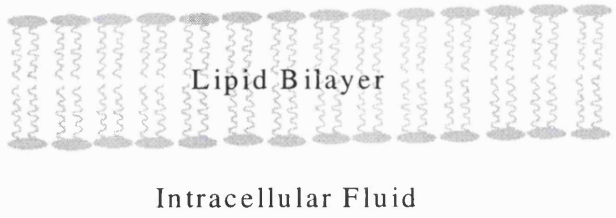

Figure 5. Cell membrane: Structure of the lipid bilayer

Cell membranes contain active and passive channels that allow ions to cross the cell membrane, and are usually specific to certain ions. The passive channels, also known as pores, allow ions to diffuse across the cell membrane. The active channels transport one or more ions across the cell membrane against chemical or electrical gradients. The active channels are called ion pumps.

2.5.4 Action Potential Generation

2.5.4.1 The Resting Membrane Potential

The following is a description of the behaviour many neurons (e.g. the frog nerve of classical experiments), the human nerve is similar but not identical. At rest, neurones typically maintain a voltage across their cell membrane of between 60mV and 70mV, the inside being a more negative potential. Inside neurones, the most common cation is Potassium (K^+), and outside, Sodium (Na^+). The most common anion outside is Chloride (Cl^-), while inside organic ions (A^-) predominate. Ions can pass through the cell membrane via the water filled ion channels, which are ion specific. The permeability of the membrane to each ion depends on which of the corresponding types of ion channel are open. At rest, the membranes of nerves and muscles are much more permeable to K^+ than Na^+ (by about 30 times). Each K^+ ion that passes across the membrane moves a small charge out of the cell, which leads to a resting potential close to the equilibrium potential for K^+. Active exchange pumps in the cell membrane maintain the ion concentration inside the cell. Ion transport across a resting cell membrane is shown in Figure 6.

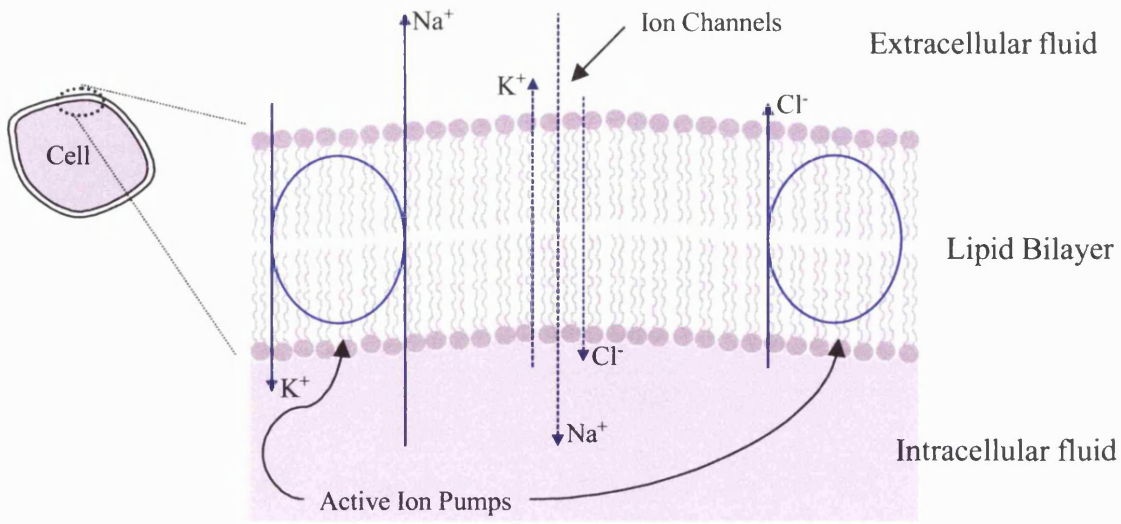

Figure 6. Ion transport across a resting cell membrane.

2.5.4.2 The Action Potential

If an axon's membrane is depolarised temporarily by a small stimulus current the localised change in the membrane potential decreases exponentially with the distance from the stimulus. This is called a sub-threshold response and is shown in Figure 7 and Figure 9.

However, if the change in membrane potential exceeds approximately 15 mV, there is a sudden increase in the number of voltage-gated Na^+ channels that are open. This increase in the number of open Na^+ channels causes the membrane potential to increase and opens more voltage-gated Na^+ channels. This produces a rapid depolarisation of the membrane to +30 to +50mV within 1ms. The voltage-gated Na^+ ion channels that have been opened start to deactivate after 500µs-1ms, causing the membranes permeability to Na^+ to decrease towards the rest potential value again. However, voltage gated K^+ channels are also opened by the depolarisation. These K^+ channels cause the membrane potential to fall rapidly back towards the resting potential. In fact, as more K^+ channels are open than at rest, the membrane becomes hyper-polarised for 1-2ms. This rapid depolarisation and hyper-polarisation is called the *action potential*. The voltage gated Na^+ channels that have opened become inactivated for a couple of ms after the initiation of the action potential. This causes a *refractory period* where no action potential can be generated by depolarising of the membrane.

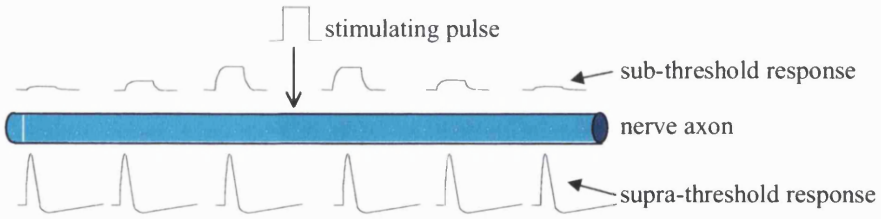

Figure 7. Propagation of sub-threshold and supra-threshold stimulation along an axon.

The action potential and the membranes relative permeability to the ions Na^+ and K^+ are shown in Figure 8.

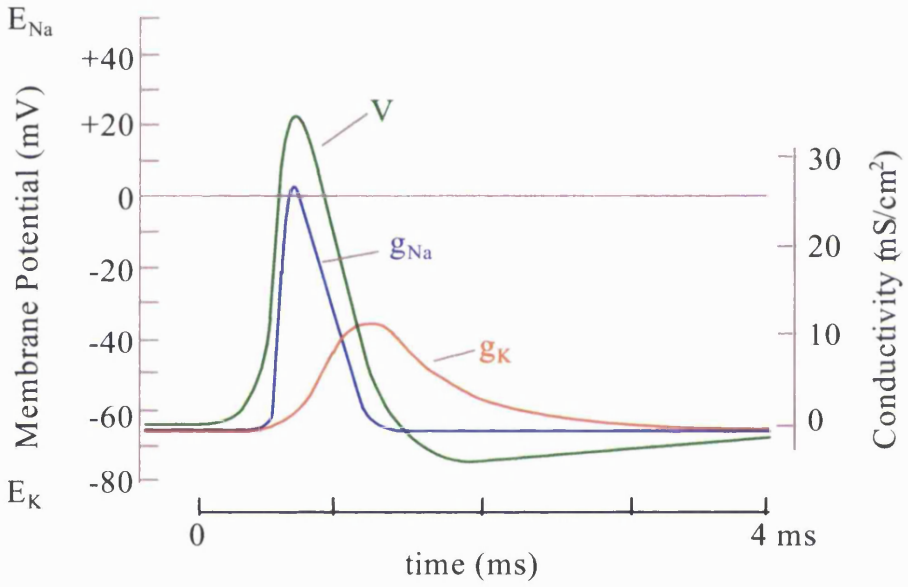

Figure 8. Comparison of the effect of a sub-threshold stimulus (non-propagating) and a supra-threshold stimulus (propagating)

2.5.5 Action Potential Propagation

Generation of an action potential in one region of an axonal membrane causes regenerative action in adjacent regions of the membrane, as local current flow causes more Na^+ voltage gated ion channels to open. The refractory period after an action potential means that the action potential will propagate away from its point of origin because previously activated regions cannot be immediately reactivated. The speed of conduction is proportional to the diameter of the axon for an unmyelinated axon.

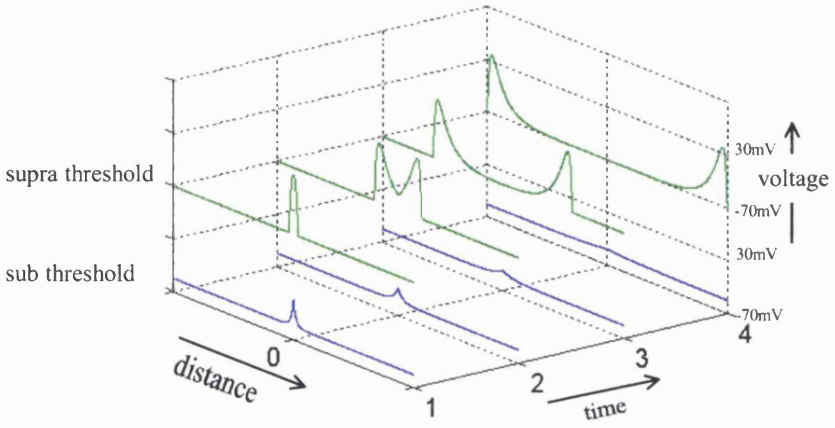

Figure 9. Supra and sub threshold stimulus propagation at various times after stimulation.

2.5.5.1 Myelination

In the peripheral nervous system of vertebrates the larger nerve fibres are myelinated by Schwann cells that wrap themselves tightly around the nerve axons. The axon can be surrounded by up to 150 layers, although this only causes an increase in the total diameter of between 20% and 40%. This wrapping causes the effective membrane resistance around the nerve fibre to increase greatly. The myelin sheath is interrupted periodically by exposed patches of axonal membrane called *Nodes of Ranvier* as shown in Figure 7.

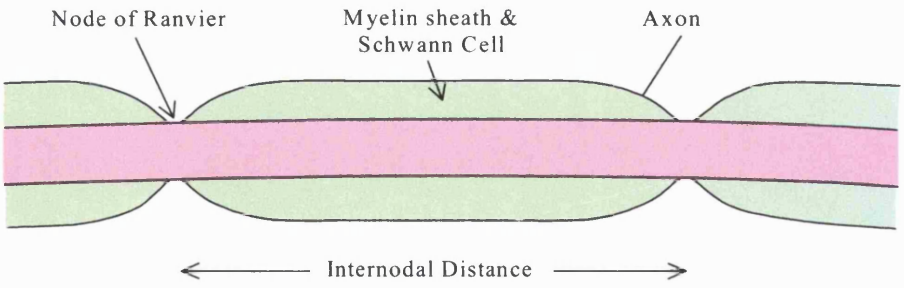

Figure 10. Myelinated nerve fibre

Typically, the inter-nodal distance is about 100 times the axonal diameter [97]. Ions can only enter or leave the axon at the Nodes of Ranvier; as a result the action potential jumps from node to node down the axon. This 'saltatory conduction' greatly increases the propagation speed [11]. Another result of myelination is that fewer ions

leave/enter the axon during an action potential and so less energy is used to restore the resting ion concentrations in the axons.

2.5.6 Stimulation of Nerve

2.5.6.1 Electrode Cuff Designs

Cuff electrodes usually consist of a cylinder or a box of insulating material with ring electrodes embedded on its inner surface. The cuff is then placed around the nerve for stimulation. A few examples of nerve cuff designs used for FNS[3] are shown Figure 11. Cuff electrodes have shown long term reliability [18,19,24,154,155] with reports of cuff electrodes still functioning after more than ten years [18,24,155].

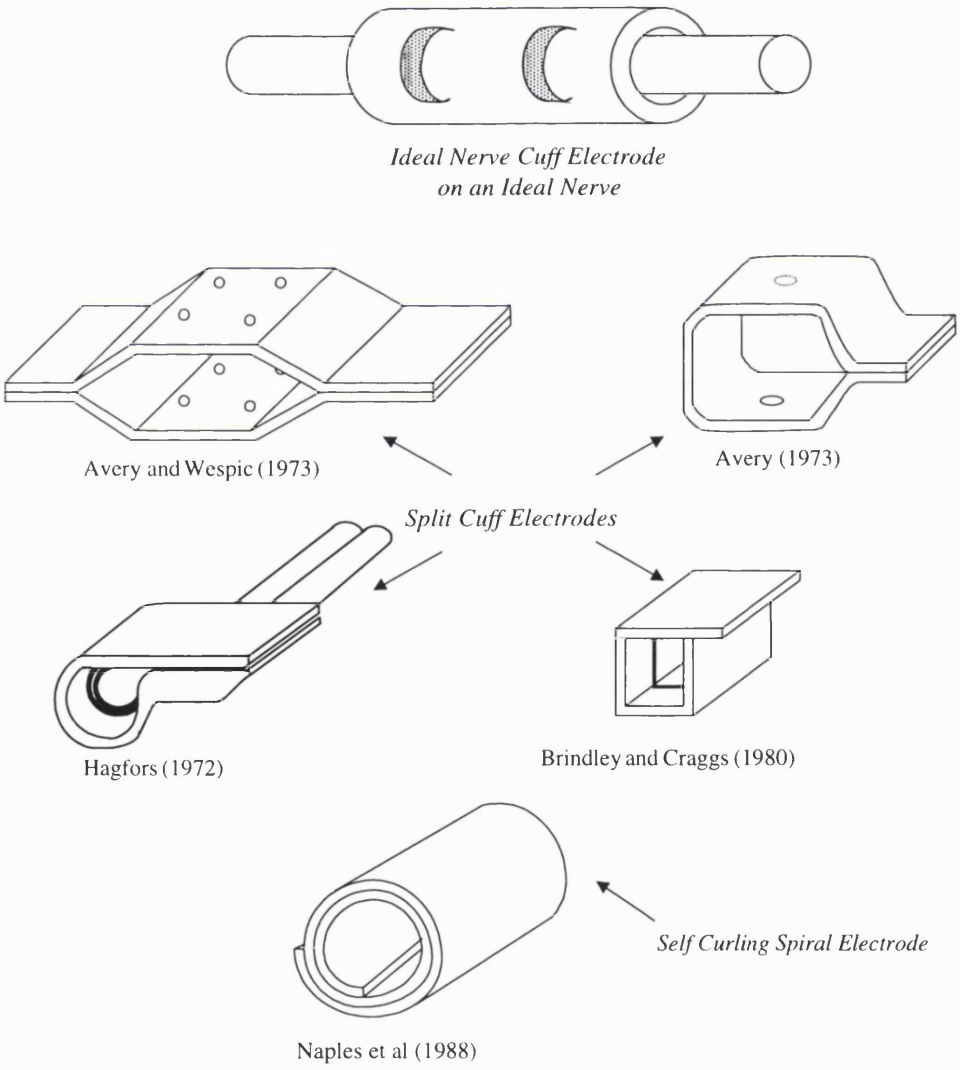

Figure 11. Historical electrode cuff designs

[3] Functional Neural Stimulation

2.5.6.2 *How Electrodes Cause Action Potentials*

Action potentials can be initiated by subjecting a nerve fibre to a rapidly changing electric field generated by two opposing electrodes. If the electrodes are in a nerve cuff, the cathode current flow results in a local depolarisation of the cell membrane. If the membrane is depolarised beyond its threshold an action potential will be generated. The anode current flow during stimulation results in the membrane being locally hyper-polarised.

Placing electrodes along the direction of a nerve fibre allows a longitudinal current to flow. Placing electrodes, either side of a nerve fibre allows a transverse current, as shown in Figure 12. It has been shown that a given longitudinal current results in the stimulation of greater number of nerve fibres than an equal transverse current; also the threshold for stimulation is lower using a longitudinal current.

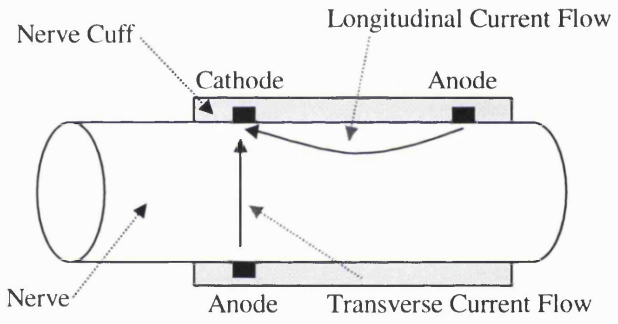

Figure 12. Longitudinal and transverse current flow inside a nerve cuff

2.5.7 Electrical Stimulation of Nerve

The "threshold" for activation most commonly describes the minimum stimulus amplitude (or duration at a fixed amplitude) to initiate action potentials [3], usually manifested by a muscle contraction

2.5.7.1 *Monophasic and Biphasic Stimulation*

Monophasic stimulation is the simplest type current waveforms, where only one cathodic (depolarising) pulse is applied to the stimulating electrode. However to prevent electrochemical damage to the nerve it is desirable to apply a biphasic stimulating pulse where the net charge injected in the two phases is close to zero. Looking at the biphasic

case most simply, the electrochemical reactions in one phase are neutralised by the electrochemical reactions in the opposing phase.

The most common stimulation method is to apply the cathodic stimulating pulse first and the anodic charge balancing pulse second. However the second charge balancing pulse tends to oppose the generation of the action potential and will increase the threshold for stimulation. For this reason, a time delay between the two phases of >100μs is often used. Alternatively, by using a lower amplitude hyperpolarising (anodic) phase before the cathodic phase, this effect can be reduced [3].

2.5.7.2 Anode Break Response During Stimulation.

Stimulation can occur at both the beginning and end of a stimulation pulse, this effect is known as 'Anode Break Excitation'. When a hyperpolarising current is applied to a neuron, the membrane conductances to both Na^+ and K^+ are altered. If the stimulus duration is fairly long (several ms), the membrane conductance to both Na^+ and K^+ will have returned to a level close to the conductance's at the resting potential. When the stimulus current is removed, a depolarising potential difference appears across the membrane and if the amplitude is larger than the activation potential then an action potential will be initiated. During normal biphasic stimulation this effect does not occur as both the magnitude and duration of the stimulus are too small. However, in stimulation where large high amplitude anodal currents are applied this phenomenon may occur. This effect can be avoided by terminating the stimulus with an exponentially decaying edge [3,22,142]. The slow removal of the pulse allows the membrane conductance to change fast enough so that anode break excitation is avoided.

2.6 Selective Stimulation Methods

2.6.1 Selective Stimulation by Fibre Size

During the 1850s it was discovered that when a steady direct current is passed through a nerve, excitability is raised near the cathode and lowered near the anode [12]. From this and related observations, the belief arose that when a brief pulse of current is passed through a nerve, action potentials arise near the cathode and may be blocked near the anode ("anodal blocking") [21,142]. The threshold for anodal blocking is always higher than the threshold for stimulation [22,23,55-58,70,71,110-114,116,118,133-135,142-144]. The thresholds for both excitation and blocking are inversely related to the size of the nerve fibre [22,58,114], so that during neural stimulation larger nerve fibres are stimulated before smaller nerve fibres. This is referred to as the Inverse Recruitment because it is the reverse of the order of normal physiological recruitment in which the small fibres are active before the large. During 1953, Kuffler and Vaughan-Williams [83] used anodal blocking to successfully block large fibre stimulation in one direction in the spinal root. Their technique was to pass rectangular current pulses between two electrodes. The Action Potentials in the larger fibres were blocked at the anode end of the nerve cuff. This method worked for the spinal roots but failed to work with peripheral nerve due to the nerve fibres being stimulated at the anode at the end of each pulse, due to anode break excitation. Burke and Ginsburg [28] showed that it was possible to avoid anodal break excitation with direct current anodal blocking by removing the voltage slowly. They used an exponential decay with a time constant of around 30ms. DC Anodal blocking however is not suitable for clinical applications as it causes electrochemical tissue damage and asynchronous neural discharge prior to block unless the electrical current is applied very slowly.

Accornero *et al* [1] showed in 1977 that by using triangularly shaped pulses with an exponential decay, it was possible to selectively stimulate the smaller nerve fibres inside a nerve trunk by blocking the action potential conduction at the anode for only the larger fibres. They proposed that launching action potentials unidirectionally away from a muscle could be used to alleviate spasticity, as the generated action potentials would annihilate the natural signals progressing in the nerve due to the collision of the two action potentials. This is referred to as "collision blocking": one would expect the

minimum frequency for collision block to be v/2d Hz where v is the conduction velocity of the nerve and d is the separation between the stimulus site and the spinal cord.

van den Honert and Mortimer [142] used an asymmetric tripolar cuff (tripolar nerve cuff definitions shown in Figure 13) to show that anodal blocking in peripheral nerve could be achieved using a pulse with a 350μs plateau and a 350μs exponential decay (anodal blocking waveform defined in Figure 14). They showed that it was possible to generate unidirectionally propagating action potentials in peripheral nerve by using an asymmetric nerve cuff and ratioing the pulsatile current to the two anodes, so that the potential difference between the two anodes was small. This means that the flow of current outside to the nerve cuff remains small and so unwanted stimulation to adjacent nerves is prevented.

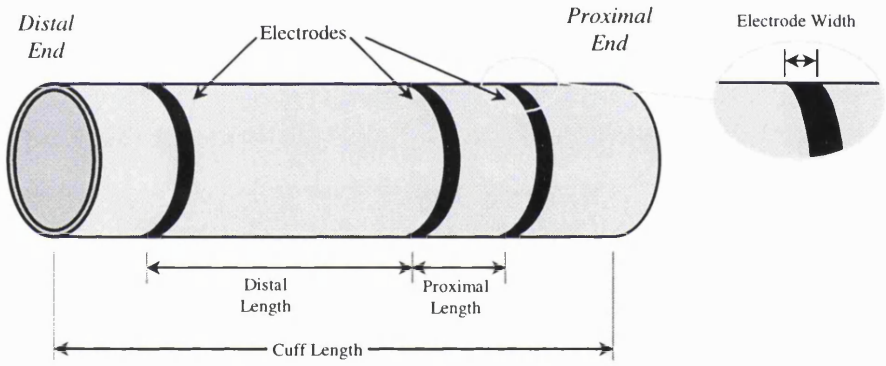

Figure 13. Ideal tripolar cuff electrode definitions

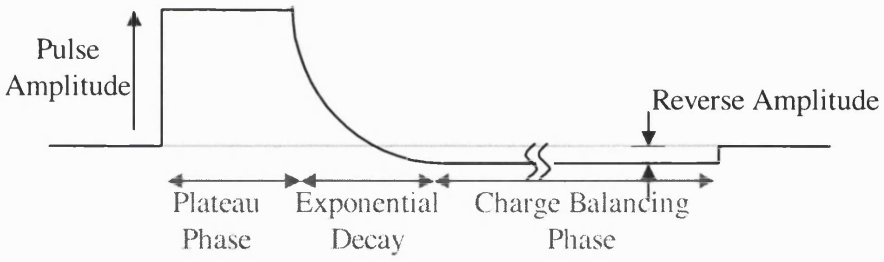

Figure 14. "Quasi-Trapezoidal" blocking waveform definitions.

Brindley and Craggs [22] showed in 1980 that anodal break excitation could be avoided by using a decay time constant greater that 200μs - 500μs. They found that the current threshold for blocking decreases as the pulse duration increases, and that successful anodal blocking will not occur for short pulses with plateau durations of less

than 200μs. The ability to generate unidirectionally-propagating action potentials using an asymmetric nerve cuff was also demonstrated. However, Brindley and Craggs used loose-fitting trough-shaped electrode cuffs and the currents found for partial and total block were high (around 5.5mA and 10mA respectively). This compares with the results from van den Honert and Mortimer [142] who found total block occurring above 5.5mA in their experiments although the closeness of the fit of the electrodes in this case was not reported.

van den Honert and Mortimer [143,144] reported the production of unidirectional action potentials in peripheral nerve in cats using both monopolar and bipolar "quasi-trapezoidal pulses" with a fast rising edge and an exponential decay. The authors used a multipolar cuff in which three ring electrodes were selected to form a tripole. It was shown again that in peripheral nerve the use of square shaped pulses could not produce anodal blocking due to anodal break excitation. The authors investigated the effect of changing the spacing of the electrodes on the threshold for anodal block. It was found that the threshold for block was related to the ratio between the distance of the proximal blocking anode to the cathode and the distance of the distal anode to the cathode. The total cathodal current needed for blocking was lowest when the ratio was highest.

Fang and Mortimer [55,57] showed that anodal blocking could selectively activate only the smaller nerve fibres in a mixed population nerve. The first paper [57] presented single fibre recordings of the action potentials elicited during anodal blocking. The paper conclusively demonstrated that the larger faster nerve fibres were blocked at a lower threshold than the smaller slower nerve fibres. The second paper [55] showed that, by using anodal blocking, fatigue of muscle could be significantly reduced during stimulation as the fast fatiguing motor units, innervated by the larger nerve fibres, are selectively blocked.

Sweeney and Mortimer [134,135] proposed using an asymmetric two-electrode cuff (ATEC) to generate unidirectionally-propagating action potentials (UPAPs). The 'ATEC' (Figure 15) works by having the diameter of the anode electrode greater than the cathode: this increases the threshold for stimulation at the virtual anode, generated outside of the cuff (by external current flow), to a level above the threshold for successful anodal blocking. This type of cuff reduces the number of wires to each cuff and removes the need to have co-ordinated control of a two-current-output stimulator. The waveforms used were quasi-trapezoidal mono-phasic pulses. The range of currents

for blocking was shown to be dependent on the ratio of the cuff to the nerve trunk diameter.

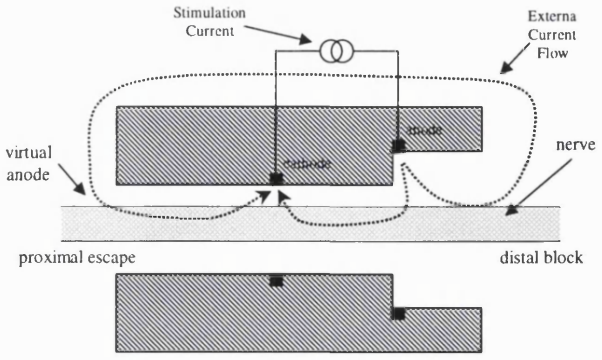

Figure 15. Sweeney and Mortimer ATEC

Rijkhoff *et al* [114] presented a very complete computer modelling paper on anodal blocking. The nerve cuffs modelled were asymmetric tripolar nerve cuffs placed around ventral spinal roots innervating the bladder. The cuffs were modelled and complete block occurred at the proximal end of the cuff while selective block occurring at the distal end. The threshold for anodal blocking increases as the electrode separation decreases; however, above 3mm separation, the change in threshold is small. The paper also showed that, for a population of fibres sized 4µm - 12µm, if the electrode separation is too small, then the small fibres close to the nerve periphery will be blocked before the large fibres on the axis of the nerve trunk are blocked. This minimum electrode separation for successful anodal blocking was found to be 2.2mm. As the electrode separation increases, the *window* for selective stimulation of only the smaller fibres at the distal end of the cuff increases, but above 4mm separation, the increase in the window of blocking currents is small, this is shown in Figure 16. The paper shows that as the diameter of the cuff increases so does the threshold for anodal blocking. The effect of pulse duration for successful anodal blocking is also shown. If the blocking pulse is too short, the action potential may reach the proximal anode too late to be blocked. This means that nerve cuffs where the electrode separation is large need longer stimulation pulses to obtain anodal blocking. This minimum duration time is related to the conduction velocity of the nerve fibre. For a 4µm fibre a typical minimum pulse width for a 6mm electrode separation is about 350µs. Increasing electrode width is also shown to increase the blocking threshold, however for an increase from 0.6mm to 1.2mm the threshold only increases 6%. Later Rijkhoff *et al* [111] reported anodal blocking during chronic experiments performed on non-spinalised female dogs. The spinal roots

innervating the bladder (sacral roots S2R and S2L) were placed in multipolar nerve cuffs configured to act as symmetrical tripoles. The experiments showed complete block of the large nerve fibres innervating the urethral sphincter in the range 1.2-2.5mA, whilst stimulating the fibres innervating the detrusor muscle of the bladder.

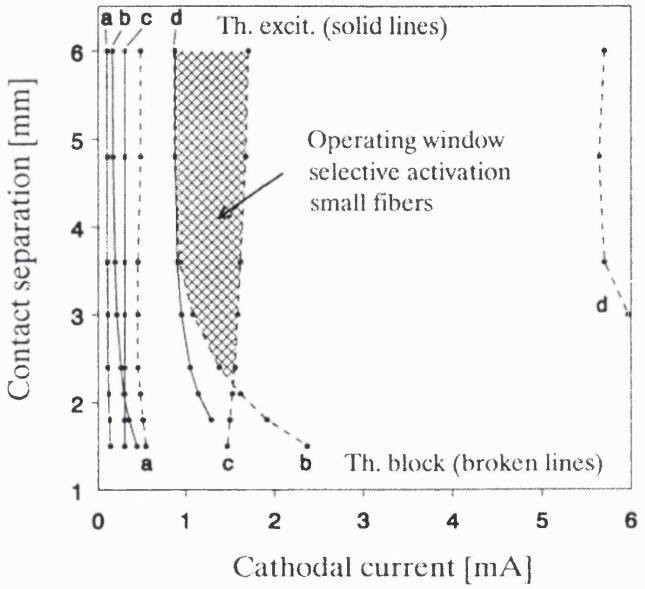

Figure 16. Excitation and blocking thresholds for a) 4um nerve fibre located on border of nerve, b) 4um fibre on axis, c) 12um fibre on border, d) 12um fibre on axis, reproduced from [114]

Fitzpatrick *et al* [58] presented the results of computer modelling of anodal blocking as well as animal experimentation. The paper showed good agreement with the results of Rijkhoff *et al* [110-114,116,118], the paper investigated in detail the ability to generate unidirectionally propagating action potentials in small fibres only using an asymmetric tripolar cuff electrode (TCE) or an ATEC. The paper shows that the current threshold for blocking is decreased as the pulse width is increased. For the animal experiments, the range of currents over which successful anodal blocking could be obtained was found to be between 240μA and 4000μA when using a TCE.

During 1989-1990, Sweeney *et al* [135,136] reported successful anodal blocking in chronic experiments in cats and dogs using an ATEC. The papers demonstrated selective stimulation by fibre size. The range of currents for which anodal blocking was successful was between 500μA and 1400μA using a 350μs-500μs plateau phase, and in the cat, a decay time constant (90%-10%) of 100μs to 500μs.

Recently Rijkhoff *et al* [112] [116,118]have reported successful anodal blocking in acute experiments on humans. The experiments took place during operations to

implant the Finetech-Brindley sacral root bladder stimulator [18]. The papers showed that successful anodal blocking was possible in humans. Typically, the onset of anodal blocking was observed at around 2mA with maximal block occurring at 5mA-6mA. The stimulation waveforms required a plateau period of at least 500μs-700μs. The electrode design used in these experiments was similar to the design used by Brindley and Craggs [22]. The large physical geometry of these cuffs may well explain why fairly long high amplitude current pulses were required. The authors also noted that anodal break excitation appeared not to occur inside the dura, allowing the use of square shaped blocking waveforms in some cases.

2.6.1.1 Summary

Although the anodal block has been known about in one form or another for over 100 years, it was not until for 1977 that a method for using this phenomenon was developed that was suitable for clinical applications. Initially there was serious concern that anodal blocking was not suitable for long term clinical use because the waveforms needed for successful anodal blocking have to be very accurately defined meaning the associated electronics for an implant have to be complex when compared with other types of stimulators. Now, with the advances in full custom integrated-circuit, this is not a significant problem. Another concern was that for anodal blocking, tight fitting nerve cuffs have to be used. With rigid cuffs and the trough types of electrodes, this is a problem, but the newer self curling spiral cuffs have been shown to not to damage the nerve even when they fit the nerve very snugly (10-30% larger than the nerve). Recent animal experiments and computer models have shown that for a reasonably snug cuff (30% larger than the diameter of the nerve), the threshold for anodal blocking is much lower than initially found by van den Honert *et al* [142] and Brindley *et al.* [22]. From the literature available in 1995 it was apparent that a maximal current of about 4-5mA should be sufficient to show the onset of total block although this would probably not be sufficient to allow detailed investigation of the failure of anodal blocking at higher current levels. In the computer modelling papers of Rijkhoff *et al* [114] and Fitzpatrick *et al* [58] the onset of block typically occurred below 1mA and, in the animal experiment by these two authors, this was shown to be roughly correct, although variation between animals was quite high. The waveforms suggested by van den Honert *et al* [142,144] and Brindley *et al* [22] have been shown to be suitable for anodal blocking. The duration of the exponential tail needed for successful blocking has been shown to be as low as 200μs

in peripheral nerve and in spinal roots anodal no exponential tail is necessary. A value of 350μs - 500μs has been found suitable by most investigators. However, anodal blocking for specific fibre sizes at specific positions inside the nerve trunk only occurs over a small 'window' of pulse amplitudes and pulse currents. Very fine control over either of these parameters should however allow successful anodal blocking. It would be better to have control over both pulse amplitude and plateau duration to allow the maximum possible 'window of operation'. With control over both variables, selective anodal blocking should be achievable for a reasonably large window. Another factor that needs to be taken into account when considering anodal blocking is the fact that current flow inside the nerve trunk will be higher in the peripheral regions of the nerve and lower in the centre of the nerve [41,149]. This means that while using anodal blocking, when the larger nerve fibres in the periphery are blocked, those in the centre of the nerve trunk fibres of the same size may still be activated. This means that uniform selective control of fibre size is not possible (i.e.: trying to block all fibres larger than 10μm). However unidirectional propagation of action potentials is feasible and so is the selective stimulation of only the smaller fibres (although with some variation with respect to position).

Table 1 shows a summary of the literature for anodal blocking.

			Selective Stimulation		Electrode Configuration			Experimaentation Type		
Authors	*Journal(s)*	*Date*	*Unidi-rectional*	*Fibre Size*	*Tripolar Electrode Cuff*	*ATEC*	*Other (type)*	*Computer Stimulation*	*Animal Experiments*	*Comparison of modelling and experimentation*
Accornero	J. Physiol.	1977					Tripolar Hooks		✓	
van den Honert & Mortimer	Science	1979	✓						✓	
Brindley & Craggs	J. Neurol. Neurosurg.	1980	✓	✓					✓	
Sweeney *et al*	IEEE BME	1986	✓			✓			✓	
Sweeney *et al*	Neurol. & Neurodyn.	1989	✓			✓			✓	
Fang & Mortimer	IEEE BME	1991		✓	✓				✓	
Fang & Mortimer	IEEE BME	1991		✓	✓				✓	
van Den Honert, Mortimer	IEEE. BME	1991	✓	✓	✓				✓	
Rozman *et al*	J. Biomed. Eng.	1993		✓			15 trip dots	✓	✓	
Rijkhoff	IEEE BME	1994		✓	✓				✓	
Tai & Jiaag	IEEE BME	1994		✓			mono	✓		
Rijkhoff	IEEE BME	1994	✓	✓	✓			✓		
Creasey *et al*	IMSP, 1995, abstract	1995		✓	✓				✓	
Fitzpatrick	PhD, Univ. Strath.	1995	✓	✓	✓	✓		✓	✓	✓
Rijkhoff	Med. Biol. Eng. & Comp	1995		✓			mono	✓		
Rijkhoff	J. Urol. (2)	1996		✓					✓	
Rijkhoff	J. Urol. , Neurol. Uro. W.J.Urol,	1997 -8		✓	✓				✓ Human	

Table 1. Summary of previous works in selective stimulation by fibre size

2.6.2 Selective Stimulation by Fibre Position

The efficacy of using multiple-electrode cuffs to selective stimulate specific regions of nerve trunks has been reported in several papers [30,68,72,88,105,121,122,148-150].

Caldwell [30] placed up to eight electrodes (0.25mm diameter, 1mm long Pt wire) around the sciatic nerve of rabbits and recorded the EMG (Electromyogram) activity of the gastrocnemius and anterior tibialis muscles during stimulation. He found that combinations of electrodes could be found that produced contraction of only one muscle without any activation of the other. The electrode positions and stimulus amplitudes were not presented.

Petrofsky [105] used a six-electrode array in a cylindrical cuff, with 3 stimulating and 3 ground electrodes placed radially as shown in Figure 17, to selectively stimulate three distinct regions inside the nerve trunk (shown by dotted lines). Measurements of the electric field inside the nerve cuff suggested that three pie-shaped segments would be stimulated inside the nerve. Recording EMG from many single fibres of the medial gastrocnemius showed that each stimulating electrode activated approximately one third of the muscle with very little overlap between the regions. This result would not expected if the motor neurones innervating the medial gastrocnemius were evenly distributed inside the nerve. However, in the sciatic nerve, the fibres innervating the medial gastrocnemius are contained in only one or two fascicles grouping the nerve fibres are together in one position. The author did not attempt to explain this incongruity.

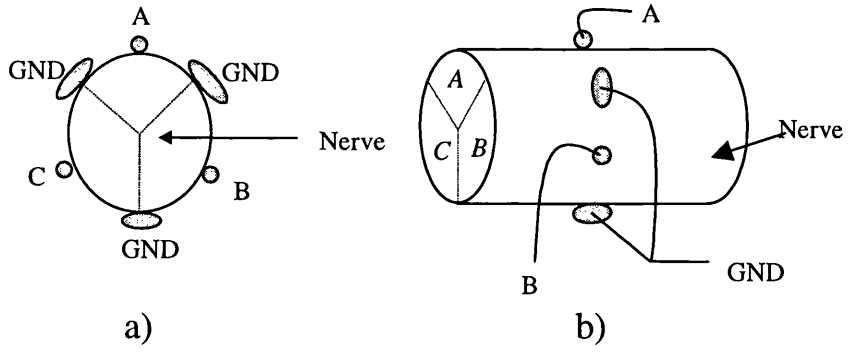

Figure 17. Multipolar nerve cuff used by Petrofsky. a) cross section b) side view showing electrode connections

McNeal and Bowman [88] used seven-electrode split-cylinder nerve cuffs (as shown in Figure 18.) implanted chronically around the sciatic nerves of three dogs. Stimulation by electrode pairs located on the same side of the nerve cuff was

investigated. The cuff was rotated around the nerve to obtain a maximally selective response. The paper showed that, after choosing the best pairs of electrodes in the cuff, selective stimulation of either the extensors or flexors muscles in the ankle was possible. An important influence on the selectivity was the closeness of the fit of the nerve cuff around the nerve. Excellent results were obtained for one dog, where the cuff was closest fitting (diameter of the cuff approximately 50% larger than the nerve trunk) and poor results for a dog where the cuff had the loosest fit. The paper also showed that stimulation outside of the nerve cuff only occurred at intensities several times the stimulation level needed for a maximal response inside the cuff.

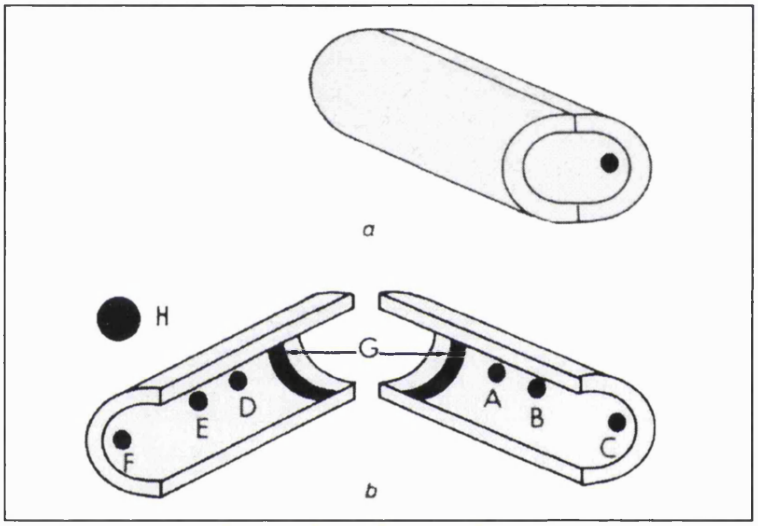

Figure 18. McNeal and Bowman split cuff electrode, (a).closed cuff, (b).view inside of the split cuff

Sweeney *et al* [133] modelled the regions of a nerve trunk within a snug-fitting self-curling nerve cuff. The authors investigated three different electrode configurations. The configurations; monopolar dot[†] electrode; a tripole of three longitudinally arranged dots; or the same tripole with an extra steering dot anode placed on the opposite side of the cuff (The anode acts to restrict the region of activation). The paper showed that tripolar stimulation restricts excitation to superficial nerve trunk regions more successfully than monopolar dot electrode configurations. Also that the use of a steering electrode restricted the stimulating current to a smaller region closer to the stimulating cathode. Chronic implantation on the sciatic nerve in dogs showed the improved

[†]dot refers to a small electrode made from a small elliptical or oblong piece of conductor.

selectivity of tripolar stimulation over monopolar stimulation and that the use of a steering anode placed opposite to the stimulating cathode increases the selectivity [4].

Veraart [150] and Sweeney [132] investigated the selective stimulation of nerve fascicles, using a snug-fitting, self-curling, 12-dot nerve cuffs as shown in . The dots were arranged as four longitudinal tripoles, placed at 90° intervals around the nerve. Both papers showed that by using longitudinal tripoles, selective stimulation of nerve fascicles is possible and that using a steering anode[5], at 180° to the stimulating cathode also increases the selectivity. However, the difference in selectivity between using and not using a steering electrode is much smaller than the difference between tripolar and monopolar stimulation. Veraart showed that connecting the anodes together only produced a small decrease in the selectivity: this is important as it decreases the number of conductors connected to the nerve cuff from 12 to 5 or 6.

Veraart also showed that using two longitudinal tripoles at 90° together allowed effective selective stimulation of regions of the nerve trunk between the two stimulating regions of the cathodes used separately. Steering anodes again increased the selectivity. The improvement from using monopolar stimulation to tripolar stimulation is great, however the increase in selectivity using steering currents is fairly small and requires anodal currents in the range of 50% to 90% of the stimulating current to have any significant effect.

[4] Where selectivity is defined as the ability to recruit specific muscle groups with out activating other muscle groups innervated by the same nerve

[5] The steering anode opposite the stimulating cathode acts to confine the region of activation closer to the stimulating cathode.

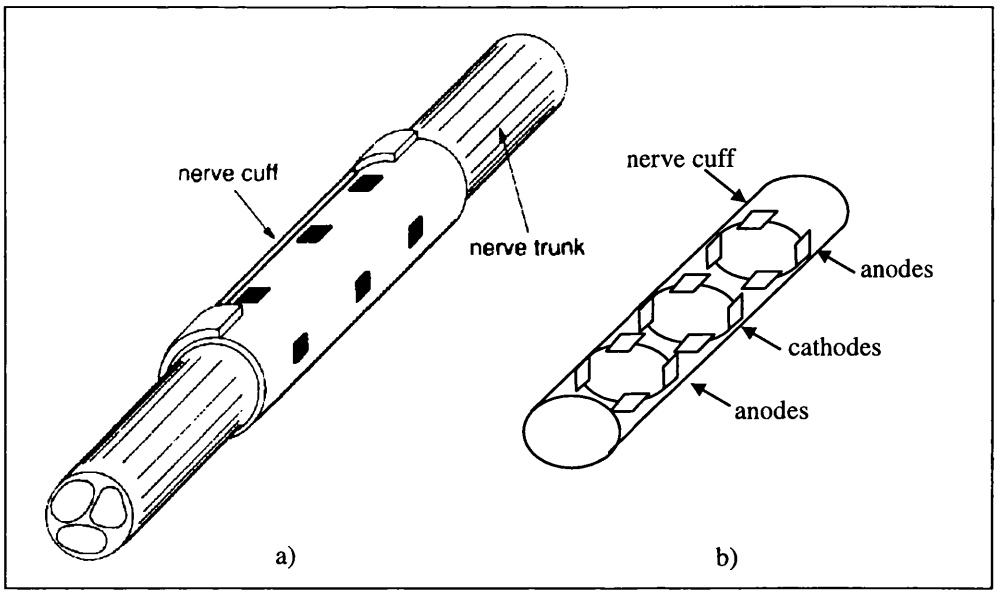

Figure 19. Veraart 12 electrode nerve cuff

Veltink *et al* [149] presented a paper describing computer modelling of selective stimulation of nerve fascicles using extra-neural and intra-fascicle electrodes. The authors found that the positions of the electrodes and fascicles were the main factors in determining the recruitment characteristics. The results showed that the region closest to the cathode had the lowest stimulation threshold. The theoretical results were stated to agree with the experimental results presented by McNeal and Bowman [88].

Rozman and Trlep [122] presented a paper showing computer modelling of geometrical-selective stimulation using a self-curling electrode cuff containing 14 stimulating cathodes and one ring anode. The modelling results showed that during single-cathode stimulation, the region closest to the cathode had the lowest threshold and that the region above the stimulation threshold is confined fairly close to the stimulation cathode. Such a nerve cuff was implanted on the sciatic nerve in two dogs; the experiments took place eight weeks post operation. The experiments showed that it was possible to select the gastrocnemius or tibialis anterior muscle by choice of electrode. However, some overflow to the gastrocnemius muscle was seen when attempting to stimulate only the tibialis anterior muscle. A second paper that described a 45-electrode nerve cuff followed [121]. The electrodes were arranged as longitudinal tripoles. The computer modelling agreed with the previous paper and again showed that the stimulating current is lowest close to the stimulating cathode. However, in this paper the animal experiments investigated the problem of obtaining fibre size selective stimulation as well as geometrical selective stimulation. The results are presented as two recruitment

curves for only one experiment and in my opinion are inconclusive. Trying to get selective stimulation in the regions closest to the tripoles means that the regions away from the stimulating electrodes will not have reverse recruitment due to current flow inside the nerve, and will be recruited normally unless a very large stimulation current is used. It would be better to use ring electrodes for the anodes to produce anodal blocking.

Grill and Mortimer [72] attempted to quantify the recruitment properties of 12-electrode self-curling nerve cuffs implanted on the sciatic nerve of cats. No effort was made to align the nerve cuff to any fascicles during implantation. The results showed that using a steering current restricted activation to a smaller region of the nerve trunk. They also presented a second reason for using steering current: the steering anode will hyper-polarise the region around the steering anode increasing the threshold for stimulation in this region of the nerve. The authors also showed that, as expected, increasing distance from the stimulating cathode to the fascicle increases the threshold for stimulation. The increase appears from the results to be approximately a first order inverse relationship. However using a steering current increases the total cathodal current and this extra charge must be removed in a reverse phase.

Goodall *et al* [68] presented an experimental paper on stimulation using a 12-dot electrode electrode, with longitudinal tripoles. There was an overlap in recruitment between the dot electrodes that starts at a fairly low stimulation level. When using a steering current this overlap is reduced, the authors also stated that when not using a steering current, fibres on the periphery of the nerve tend to be recruited first due to current flowing around the nerve cuff - nerve border. This effect is reduced when using a steering current. They concluded that the effect of the steering current is greatest when the steering current is a large proportion of the total anodal current (steering current 3 times larger than the other anodal currents). This sort of stimulation precludes the use of anodal blocking for site-selective stimulation, as the total cathodal current needed for successful blocking may be outside of the safe region for reversible electrochemical reactions using Platinum electrodes as discussed in detail by Donaldson [46,48,51].

Deurloo and Holsheimer [41] presented a computer modelling paper showing the current distribution for multiple contact nerve cuff electrodes. Some example distributions are shown in Figure 20.

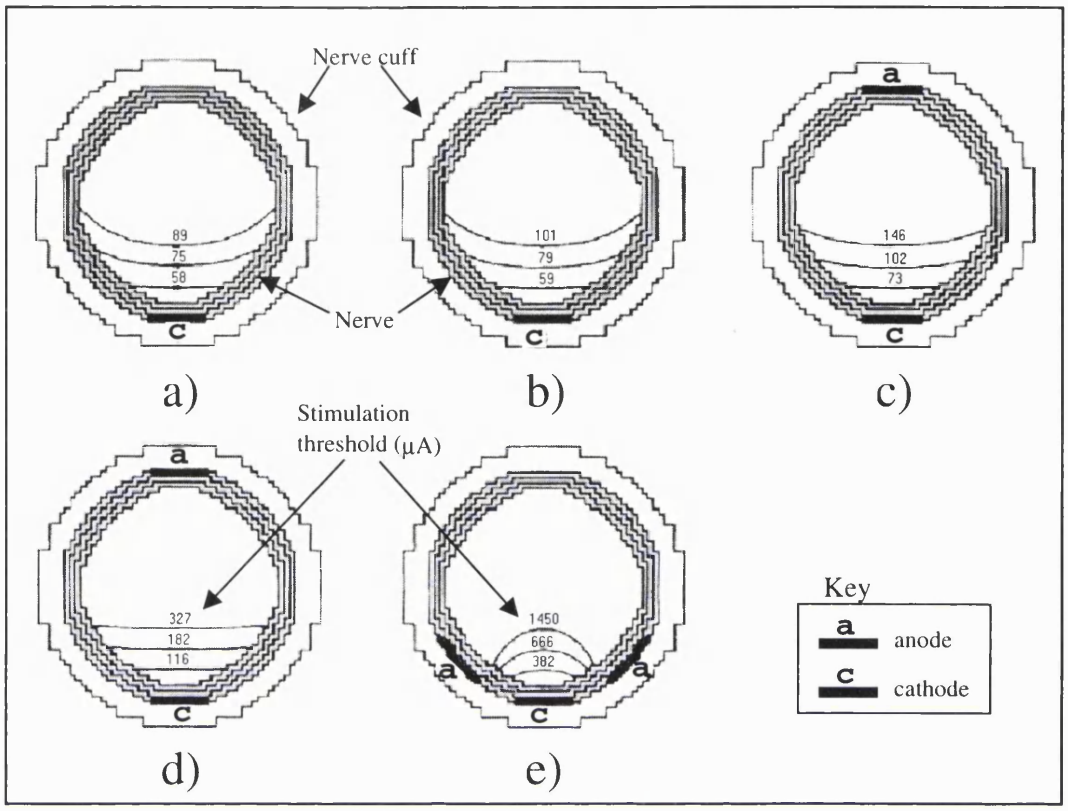

Figure 20. Recruitment regions inside a nerve cuff for 15μm fibres [41]. a) monopolar, b) longitudinal tripolar, c) longitudinal tripolar with 40% steering, d) transverse bipolar e) transverse tripolar.

As can be seen in Figure 20a, a single dot electrode produces a crescent-shaped activation region at one side of the nerve trunk. However using a low-level steering current has only a slight effect on the shape of the activation region. Larger steering current changes the shape of the activation regions to roughly horizontally demarked shapes (Figure 20d.). The use of a steering current increases the stimulation threshold by a factor of approximately 3 in the larger steering current case. However by placing two dot anodes close to the stimulating cathode reduces the stimulation region to a very small spherical shaped region desired, but the stimulation threshold has been increased by a factor of approximately 14 (Figure 20e).

2.6.2.1 Summary

Selective stimulation by fibre position has been shown in computer models [41,121,122,149] and experimentally [30,41,68,72,88,105,120-122,132,133,150,151]. However, great selectivity is not possible and, with 4 longitudinal tripoles, it is unlikely that the fibres in only one fascicle will be activated. A steering current increases the selectivity at a cost of increasing the overall cathodal current significantly. This has been experimentally verified. The work by Deurlwoo *et al* showed that the use of transverse tripoles allow very small regions of a nerve trunk to be selectively stimulated, however the increase in the total cathodal current compared with monopolar stimulation was shown to be around 14 times.

In many applications however the need to activate only one fascicle is not needed, what is required more often is the ability to stimulate one muscle (or group) more than another antagonistic muscle (or group). As in the case of dorsiflexion of the foot where an adjustment to 'balance' inversion and eversion is needed. This is achievable using dipolar and tripolar stimulation as shown by McNeal and Bowman.

The fit of the nerve cuff to the nerve has been shown to affect greatly the selectivity [72,133,150]. The development of self-curling nerve cuffs that can be implanted safely, with a diameter very close to the diameter of the nerve trunk, means that it is now feasible to implant systems that use tight fitting cuffs to increase selectivity.

Table 2 Shows a summary of the literature for selective stimulation by fibre size.

Table 2. Summary of previous works in selective stimulation by fibre position

Authors	*Journal(s)*	*Date*	*Number of Electrodes*	Electrode Configuration				*Experimaentation Type*	
				Monopolar	*Dipolar*	*Tripolar*	Tripolar & Steering	*Animal Experiments*	*Computer Stimulation*
Caldwell	*Internal Report Uni. Ljubljana*	*1975*	8	✓	✓				
Petrofsky et al	Med. Biol. Eng. Comp.	*1979*	6		✓				✓
Mc Neal & Bowman	Med. Biol. Eng. Comp.	1985	7	✓	✓				✓
Veltinck *et al*	IEEE BME	1989	2	✓	✓			✓	
Sweeney *et al*	IEEE BME	1990	12			✓	✓		✓
Veraart *et al*	IEEE BME	1993	12			✓	✓	✓	
Rozman & Trlep	J. Biomed . Eng.	1993	15			✓		✓	
Rozman & Trlep	Med. Biol. Eng. Tech.	1995	45			✓		✓	✓
Grill & Mortimer	IEEE BME	1996	12			✓	✓		✓
Goodall *et al*	IEEE BME	1996	12			✓	✓	✓	
Deurlwoo & Holshiemer	IEEE BME	1998	3			✓	✓		
Veraart	Brain Res.	1998	4	✓				✓ Human	

Chapter 3. Selective Stimulator Specification

This chapter outlines the specification of an implantable selective nerve stimulator suitable for selective stimulation either by fibre position or by fibre size.

3.1 General Requirements of an Implanted Selective Stimulator

The general requirements are similar to those for any implantable stimulator. It must be small enough to be implanted without causing any problems for the patient (perceived or otherwise). The device should be powered by induction so that all the energy used by the implant is supplied by an external power source. This source will be a battery, to allow mobility, so low power operation is required to give a reasonable operation lifetime. A second reason for having the device low powered is that the device and transmitter will generate heat due to power consumed, and this must be small enough to prevent possible thermal damage to the patient.

Many of the methods described in 1.4 for the LARSI system can be used for the selective stimulator system. However, because many parameters must be defined for each stimulating pulse (amplitude, duration, trailing edge type, number of electrode, etc), the analogue timing coding used in LARSI, cannot be used and must be replaced with a digital encoding system.

3.2 Nerve Cuff Types for the Selective Stimulator

From the literature review in chapter 2, we can see that there are three selective stimulation techniques, which we would like to implement in a new system (selective stimulation by fibre size, fibre position and generation of unidirectionally propagating action potentials). The stimulator must be capable of controlling more than one type of nerve cuff to allow selective stimulation by fibre size and/or selective stimulation by fibre position. The types of nerve cuff the stimulator can utilise are discussed in the following section.

3.2.1 Nerve Cuffs for Selective Stimulation by Position

The stimulator was originally specified to be capable of controlling a nerve cuff with separate stimulating cathodes, to allow the investigation of selective stimulation by fibre position. We have called the final cuff design a *Pentapolar Electrode Cuff* (PEC). The design is related to the 12-dot electrode cuffs, shown to be effective for geometrical

selective stimulation by Veraart *et at* [150]. A diagram of the cuff is shown in Figure 21. The problem with Veraart's cuff is the number of wires needed for the connection of each cuff to the stimulator. Using the Cooper Cable we wish to use with the stimulator, each cuff would require 3 cables (each containing 4 wires). This is not a satisfactory solution, because multiple cables, connected to the nerve cuff, raises the chance of damage during implantation as the cuff is difficult to place, and after implantation the mechanical forces exerted on the nerve trunk due to the nerve cuff will be higher. Therefore, it was decided to use a simplified version of this configuration. Veraart reported that the selectivity decreased only slightly if all the dot anodes at each end were connected together, but this also decreased the number of wires connected to each cuff to six. Our design is a further reduction with 4 centrally placed stimulating cathodes and two inter-connected anode rings, arranged, as shown in Figure 21. The anode rings could if desired be replaced with an indifferent electrode placed external to the nerve cuff (to reduce cuff length). A photograph of an actual pentapolar nerve cuff is shown in Figure 22[6].

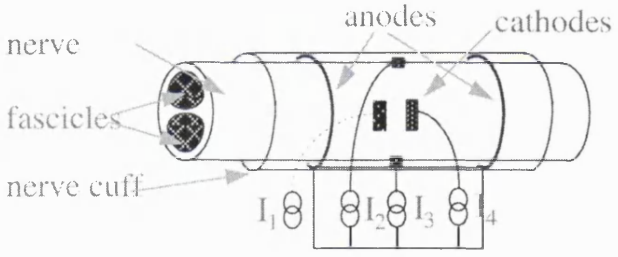

Figure 21. Pentapolar electrode cuff

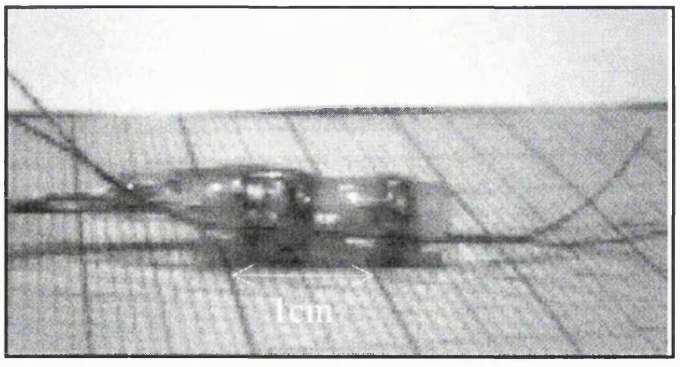

Figure 22. Photograph of an asymmetric pentapolar electrode cuff

The cathodes each have an exposed area of approximately $2mm^2$, the impedance of each cathode (at 1kHz) relative to the anodes was found to be $1k\Omega$ – $1.3k\Omega$ for a

[6] Manufactured by Morten Haugland, SMI, Aalborg, Denmark.

3.5mm diameter cuff immersed in 0.3%[7] NaCl to simulate the conditions after implantation [38].

3.2.2 Nerve cuffs for Selective Stimulation by Fibre Size

For selective stimulation by fibre size four types of cuff have been used successfully:

1. Pseudo-Tripolar electrode cuff (really a Dipolar Electrode Cuff (DEC))
2. Tripolar Electrode Cuff (TEC)
3. Asymmetric Tripolar Electrode Cuff
4. Asymmetric Dipolar Electrode Cuff (ADEC, also know as an ATEC in some papers)

Because of the disadvantages discussed in 2.2.1, the ADEC was not included in this specification. However the DEC (pseudo-tripole), TEC and ATEC are all expected to be used with the stimulator. The latter used to generate unidirectionally propagating action potentials)

A possible elaboration of the PEC is the asymmetric PEC (APEC), which may make it possible to combine selective stimulation by fibre size and selective stimulation by fibre position. This is speculative and has not being investigated theoretically or experimentally.

Figure 23 shows all of the types of nerve cuffs to be used with the stimulator and their configurations.

[7] 0.3% saline has three times the restistivity of 0.9% normal saline and simulates the expected tissue restistivity inside the nerve cuff after implantation.

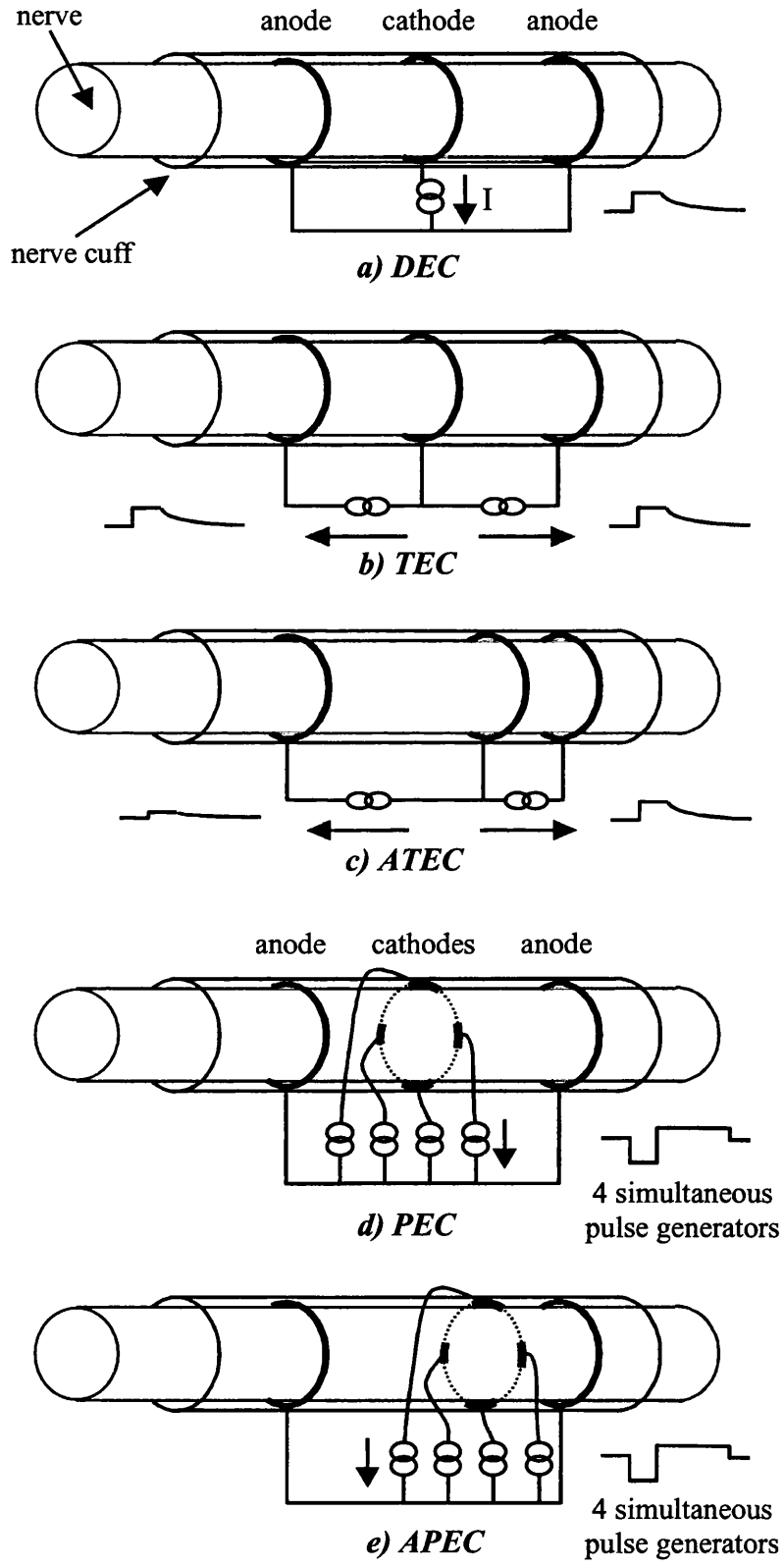

Figure 23. Nerve cuffs for use with the selective stimulator

The expected uses and the suitability of these nerve cuffs are shown in Table 3 (As discussed in the literature and proposed previously in this chapter)

Table 3. Expected uses with cuff types for the selective stimulator

Recruitment Type (Fibre Size)	Cuff Type				
	DEC (Quasi-TEC)	TEC	ATEC	PEC	APEC
Normal L→S	✓✓	✓	✓	✓	✓
Reverse S→L	✓	✓✓	✓	✓	?
Unidirectional	×	×	✓✓	×	?
Unidirectional & L→S	×	×	?	×	?
Selection by Fascicle L→S	×	×	×	✓✓	✓
Selection by Fascicle S→L	×	×	×	?	?

Key:

×	?	✓	✓✓
Not possible	Feasibility unknown	Possible use	Expected use

From Table 3 it can be seen that each type of nerve cuff has an expected application, however the suitability of some cuff types for producing some types of selective stimulation requires further investigation as the basic experiments to show their efficacy have not yet been undertaken. This is especially true of the APEC proposed in this chapter.

3.3 Number of Nerve Cuffs

The number of cuffs that need to be controlled in a practical device will depend on the application. One proposed application is the stimulation of bladder and bowel where control over the extra-dural roots S2, S3 & S4 is necessary; this requires six tripolar cuffs for selective stimulation in each root. However, for development purposes and to reduce the overall cost, this number of cuff controllable for the prototype devices was reduced to two tripolar cuffs, with the system expandable later to some multiple of this initial figure. A system that is capable of controlling two tripolar nerve cuffs can alternatively control

three dipolar cuffs or one pentapolar cuff, by virtue of having six outputs. Table 4 shows the number of nerve cuffs specified for the development system.

Table 4. Number of nerve cuffs for the initial test devices

Cuff Type	Anodes / Cuff (Separate[8])	Cathodes / Cuff	Number of Wires / Cuff	Number of Cuffs
Pentapole	1	4	5	1
Tripole	2	1	3	2
Dipole	1	1	2	3

Another significant factor, in determining the number of nerve cuffs that a stimulator system can control, is the maximum frequency of operation. To obtain tetanic contraction of muscle typically stimulation must be performed at a minimum of 15 – 20Hz. This may create a problem for devices developed to implement anodal blocking, as the pulses used for anodal blocking are longer than stimulation pulses used for conventional stimulation. If four tripolar cuffs are used during stimulation and each plateau is 500μs long with a 350μs tail and 5% reverse amplitude then each stimulation pulse will take approximately 17ms. When stimulating only one cuff the maximum frequency of stimulation is approximately 60Hz. With four nerve cuffs with the same parameters, the maximum frequency becomes 15Hz on each cuff. This problem limits the number of cuffs that can be simultaneously used for stimulation. However, although a practical system may have up to six-tripolar nerve cuffs attached, not all of the cuffs could be used at the same time at higher frequencies. This problem has not been mentioned in the literature but would appear to place an upper limit on the number of nerve cuffs any selective stimulator system can realistically control unless there is isolation between the outputs to prevent currents flowing between the cuffs during stimulation.

[8] Connected anodes are counted as one anode

3.4 Stimulation Waveform Specification

This section discusses the waveform parameter specifications for the simulator. The anodal blocking waveforms are shown in Figure 24 with the definitions used in the following section.

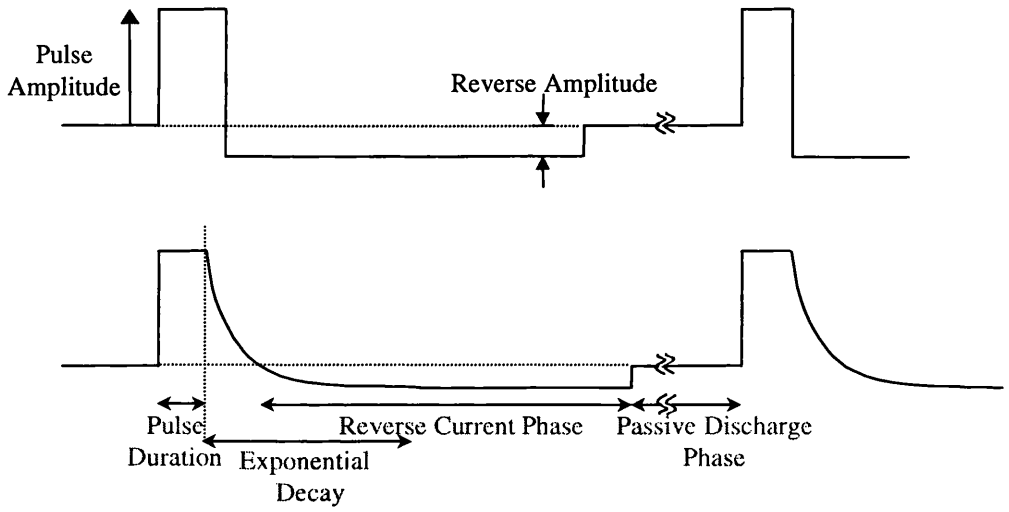

Figure 24. Anodal blocking waveform definitions (Anodal current waveforms shown)

3.4.1 Pulse Amplitudes

The currents required for conventional stimulation are always lower than for anodal blocking so the maximum stimulation current is based on the requirement for anodal blocking. Unfortunately, this current has shown great variance in the literature (see section 2.2.1). The current required to achieve anodal blocking is dependent on the type of nerve cuff used. The two main types of nerve cuff used for anodal blocking are the Tripolar Electrode Cuff (TEC) and the Asymmetric Dipolar Electrode Cuff (ADEC).

3.4.1.1 Asymmetric Dipolar Electrode Cuff (ADEC)

In the literature ADECs have been used for the generation of unidirectionally propagating action potentials. Sweeney and Mortimer [134] found that total block at one end of an ADEC could occur at current amplitudes around 0.5mA; whilst at the other end of the cuff the threshold for blocking was around 1.4mA. A later chronic experimentation paper by Sweeney *et al* [135] showed that several weeks after implantation the upper blocking threshold was found to be 5-8.5mA in one animal. The results were found to be highly dependant on the ratio of the cuff diameter to the nerve diameter and all the cuffs used in this experiment were relatively loosely fitting (as

described by the authors, with cuff diameters 144% to 173% of the nerve diameter). As more literature is available for the Tripolar Electrode Cuff (TEC), the threshold is generally lower [[58,82,111,134,135]], it was decided the specification would be based around the parameters required to achieve anodal blocking using a TEC.

3.4.1.2 Tripolar Electrode Cuff (TEC)

The threshold for anodal blocking has shown variation from 0.24mA [58] to 9mA [22]. However, it is noted in the literature that the earlier papers on anodal blocking generally had a larger threshold than the more recent papers. This may be due to the relatively large dimensions of nerve cuffs used in the earlier papers (both in electrode spacing and cuff diameter). The range of thresholds for anodal blocking found in the literature is shown in Table 5. Most of the literature on anodal blocking shows that blocking is typically feasible in the amplitude range of 0.24mA to 5mA (cathodal current). It was decided that 5mA per anode (or 10mA cathodal, as usually quoted in the literature) was a reasonable upper limit that would allow anodal blocking to be investigated. However, this upper value may not be high enough to investigate the failure of blocking at higher current levels in some applications.

Table 5. Examples of the thresholds found for anodal blocking using TECs

Author	*Date*	*Location*	*Cathodal Current (mA)*			
			Onset of block	*Complete block* † *(fibre size)*		*Limit of block*
van den Honert *et al*	1979	Peripheral Nerve	5	5.75		
Brindley & Craggs	1980	Spinal Roots Peripheral Nerve	5.5	9 2.2 ‡		29 5.2
van den Honert *et al*	1981	Sciatic nerve	1.5	1.95		3.25
Fang & Mortimer	1991	Theoretical		0.2 0.3 0.6	20µm 10µm 4µm	
		Sciatic (branch)		1.5-3 1-1.35	Fast Slow	
Fang & Mortimer	1991		1.5	2.5		
Rijkhoff *et al*	1993	Theoretical		.5-.9 1.75-5.2	12µm 4µm	
Rijkhoff et al	1994	Spinal roots	0.7-1.1			1.6-3
Fitzpatrick	1995	Theoretical		<.410 .428 .598 .849 >1.276	12µm 10µm 8µm 6µm 4µm	
Fitzpatrick	1995	Spinal roots	0.24 - 4			
Rijkhoff	1998	Dog Spinal roots	0.3 - 0.7	0.7 – 1.1		1.9 – 10.24
Rijkhoff	1999	Human Spinal Roots	1 – 2	6 – 7		

† *In the case of asymmetric tripoles the threshold for anodal blocking at the escape end*

‡ *Complete block was not observed, most complete block occurred at 2.2mA*

3.4.2 Output Current Ratios

The stimulator needs to be capable of defining the ratio between the output currents for each separate cathode in the pentapolar and either anode in the tripolar electrode cuffs. It should also be possible to set any output current to zero so that, as in the case of the pentapolar electrode cuff, full control over the stimulating cathodes is feasible.

For the tripolar electrode cuff, the ability to fix the ratio of the anode currents is important to keep the potential difference between the anodes small when the used cuff is asymmetric to produce unidirectional Action Potential propagation. Any potential difference between the anodes will cause a current to flow outside of the cuff between the two anodes: this external current can cause undesired stimulation of nerve outside of

the nerve cuff. 10% steps have being used in experiments in which pulse widths were also modulated (see below) [58]. For the stimulator it was decided to use 4 bits per output channel to define the output current ratios, equating to steps of 6.7% (1/15).

3.4.3 Pulse Durations

It has been shown in the literature [21,22,58,111,116,118,135] that there is a minimum pulse width required for successful anodal blocking. This minimum is dependent on the separation of the blocking anodes from the central cathode, as the action potential is initiated at the cathode and propagates towards the anodes. The nerve must still be hyperpolarized in the region of the anodes when the action potential arrives at the anodes to allow anodal blocking.

The minimum pulse width can be estimated for a nerve cuff [113] and is shown in Figure 25. The propagation speeds are assumed as 66m/s and 27m/s respectively for 12μm and 4μm myelinated nerve fibres.

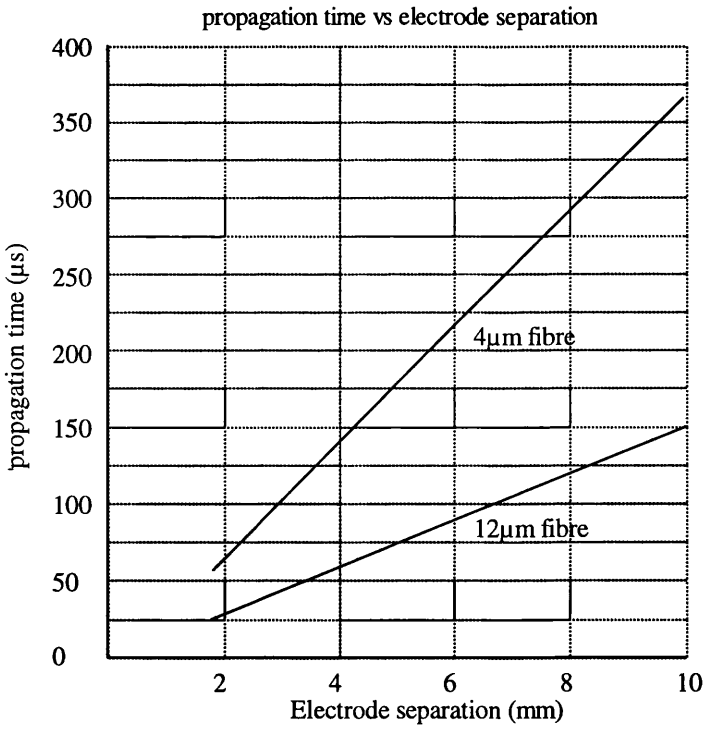

Figure 25. Separation of the cathode from the blocking anode vs propagation for 4μm and 12μm fibres

This means that to successfully block fibres above 12μm inside a cuff with an anode-cathode electrode spacing of 5mm the pulse duration must be a minimum of 145μs. However, this is not the whole story, as the pulse must also be applied for slightly longer than calculated since the action potential has a finite period during which it can regenerate [113].

Experimentally the minimum plateau period has been found to be in the order of 200μs [22] to 600μs [58,118] (although some authors have used much longer pulse durations of up to 20ms [22,111] to demonstrate anodal blocking). Rijkhoff [114] found theoretically that the onset of block was visible at 200μs and complete at 350μs (2mm contact separation, 4μm fibre). He also showed theoretically that the minimum electrode separation for low current anodal blocking is in the order of about 2mm. This is due to the electric fields of the anodes and cathode starting to overlap decreasing the potential beneath each electrode.

In the literature the sensitivity of anodal blocking to the duration of the pulse width has been investigated [58,113,114], the computer modelling investigations by Fitzpatrick [58] and Rijkhoff [114] both showed that for a particular nerve fibre diameter successful anodal blocking could only be obtained if the pulse duration was sufficiently long. Fitzpatrick investigated the sensitivity of Anodal Blocking to pulse duration for several fibre diameters. The investigation showed that the difference in pulse duration to block selectively 8μm fibres and not 4μm fibres could be as low as 50μs (or 30μs between 12μm and 10μm fibres). From this it was decided that steps of smaller than 10μs would be a more than adequate to allow successful Anodal Blocking. Finally, 4μs was decided upon as 1ms divided by an 8bit number (256 divisions) is approximately 4μs.

The final specification allows for the range of plateau durations was 20μs to 1ms in 4μs steps; this should be sufficient to allow successful anodal blocking of the nerve fibres, as well as conventional stimulation.

3.4.4 Reverse Current Phase

The reverse current phase is used to balance the charge delivered in the stimulation pulse. The reverse current has to be kept sufficiently small to prevent unwanted stimulation occurring when the reverse current finishes (due to the positive going edge at the end of the stimulation). Fang and Mortimer [55,57] stated that this should be less than 100μA for successful anodal blocking, however the absolute maximum current step will depend on the actual stimulation conditions (pulse duration, cuff and nerve geometry, nerve fibre population)

For a 5mA pulse and a reverse phase of 100μA, the current ratio is 50:1; for a 1mA pulse the ratio is 10:1. For the development system, it was decided that it was

desirable to have a few programmable reverse current ratios, of the order of 10:1, 20:1 and 50:1. However, during the design it was found that it was just as easy to generate 7 ratios in the range 6.7:1 to 46:1. It should be noted that for a 1ms square pulse and a reverse phase of 10:1, the total time for one stimulation pulse is 11ms, the reverse phase will determines the upper stimulation frequency limit while using Anodal Blocking waveforms. For very long duration pulse width with small reverse currents phases, the maximum frequency obtainable will be fairly low.

3.4.5 Passive Discharging

Any error in the magnitude or duration of the two stimulation phases will cause a charge imbalance at the electrodes. This would lead to electrochemical damage if no blocking capacitors were present, or cause the blocking capacitors to saturate if they were present. By connecting a resistive load between the cathode and anode after the stimulation phases, this charge can be passively removed. Figure 26 shows how passive discharge resistors should be connected for the DEC, TEC and PEC. The value of these resistors has to be low enough so that the residual charge can be removed before the next pulse is delivered to the same nerve cuff.

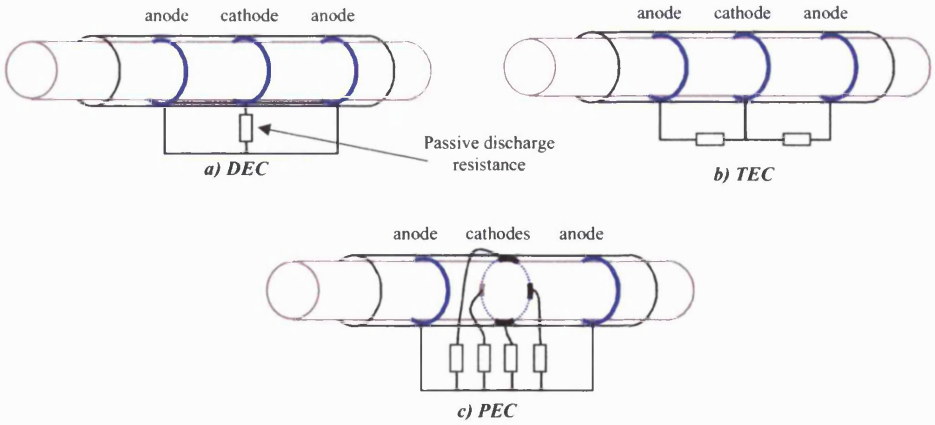

Figure 26. Configuration of passive discharging resistors for the DEC, TEC and PEC

Producing switched resistances (using CMOS transistors) of less than 250Ω on an IC is difficult due to the physical area occupied by the transistors, the following calculation uses 250Ω resistors, which are feasible to implement in a reasonable silicon area. If a 1% charge error occurs for a 1ms, 5mA square pulse with a reverse current ratio of 6.7:1 and the blocking capacitors are 4.7μF, then the residual charge would be

0.05μC. The time to remove 95% of this charge (leaving 5nC error or 0.25mV on the blocking capacitor) with a 250ohm resistor is approximately 3.5ms.

The time taken to transmit the data for each stimulation pulse is expected to be approximately 750μs[9]. Therefore, with four cuffs there will be approximately 3ms available for passive discharging with the stimulator operating at maximum frequency (i.e. minimum spacing between stimulation pulses). Figure 21 shows the simulated current waveform for a 1mA, 1ms stimulating pulse with a 7.5% reverse current phase when a 2% charge error is present and a 3ms passive discharge (250Ω) is used after the stimulation pulse has finished.

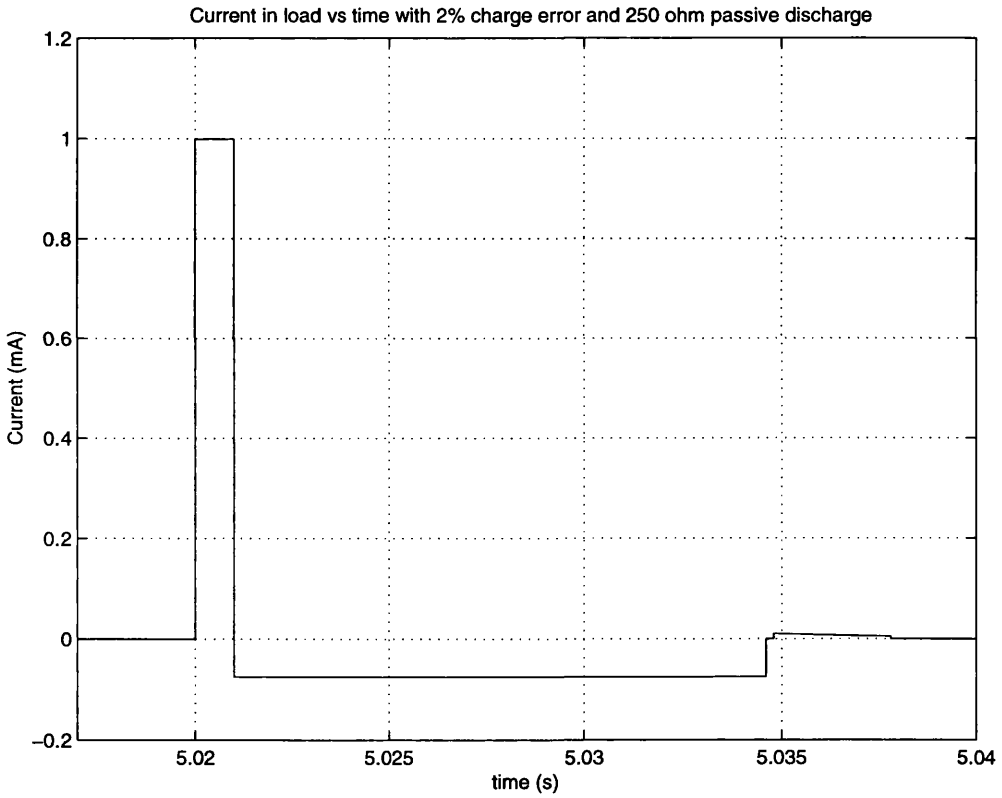

Figure 27. Current in 1kohm resistive load vs. time after 5 seconds stimulation.

Figure 27 shows that after several seconds constant stimulation the current spike due to the passive discharge settles at approximately 9μA. For a 4mA stimulation pulse the current spike due to the passive discharging settles to approximately 35μA. If the current spike is positive (as shown) then erroneous stimulation could be caused due to the passive discharging if the current spikes approach stimulation thresholds (which can

[9] Assuming 44 data bits, 16 parity modulated at 83.3kHz

be as low as 40uA). With a charge balancing error of 1.5% and a 250Ω passive discharge resistance, the current spikes due to the passive discharging are simulated as 25μA for worst-case stimulation pulses (5mA, 1ms). This should be small enough to prevent unwanted stimulation with large stimulation pulse. Although by allowing longer discharging periods the current spike due to passive discharging can be reduced.

Figure 28 shows the voltage waveforms observed on the blocking capacitor and load when stimulating with the same parameters of Figure 27. The figure shows that the average offset voltage on the blocking capacitor due to a 2% charge error settles to approximately 6mV.

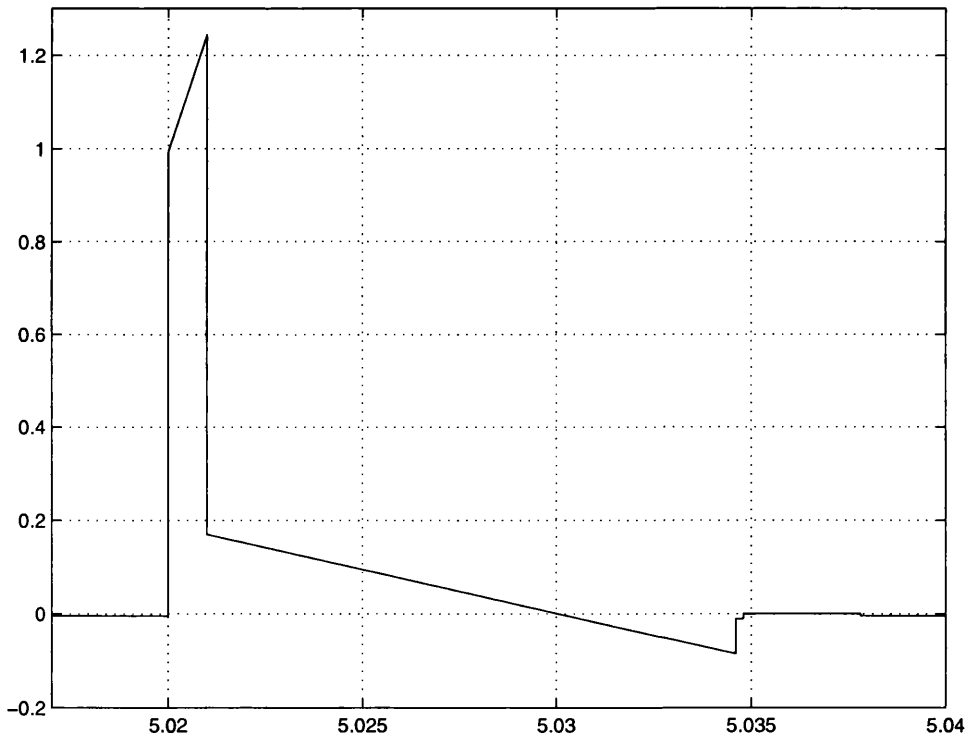

Figure 28. Voltage across blocking capacitor and 1kohm load vs. time after 5 seconds stimulation.

These results suggest that a value close to 250ohms is a sensible value for the passive discharge resistance when considering both the maximum current during discharge and the offset voltage.

3.4.6 Exponential Decay Time Constant

The exponential tail that has been used in the literature for prevention of anode break excitation in peripheral nerve has been found to be effective only if the time constant is greater than 200μs - 350μs [22,58]. For this reason the time constant for the

tail has been arbitrarily set at 350μs for this stimulator, determined by the value of an external capacitor which may be altered if necessary. The design should also allow the tail to be enabled to disabled, to allow square-shaped pulses or quasi-trapezoidal pulses. It should also be possible to change the time constant at the time of implant construction to allow a different exponential decay to be used if it is required for a particular application.

A summary of the waveform specification is shown in Table 6.

Table 6. Output waveforms specification

Output Waveforms	
Pulse Amplitudes (A_f)	19μA – 5mA in 19μA steps
Plateau Duration	20μs – 1ms in 4μs steps
Reverse Current Phase (A_R)	1/47 to 7/47 of the Pulse Amplitude where: $A_R = \frac{A_f}{6.7n}$ where n = 1 to 7

3.4.7 Output Current Resolution (in Tripolar Operation)

Having defined the provisional specification for the stimulation waveform parameters in the previous sections, we decided that the most satisfactory system to generate the output waveforms would be that shown in Figure 29. The circuit consists of a pulse generation stage to produce the shaped waveforms, four attenuators to produce the four-ratiod waveforms and a voltage to current conversion stage to produce the output currents.

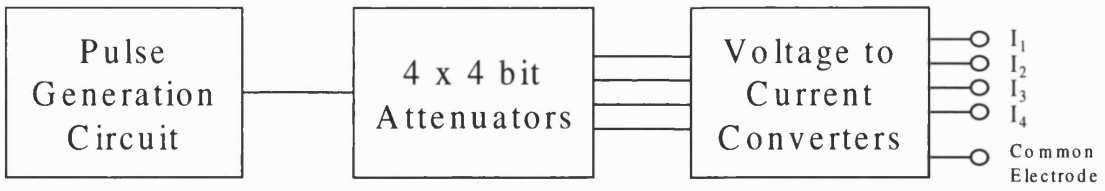

Figure 29. System to generate multiple output waveforms

This implementation actually allows higher current resolution than the step size defined by the reference amplitude (steps of 19.2μA) in tripolar operation (and Pentapolar operation to a smaller degree). Using the ability to control the attenuation on each output to set the output current ratios allows this higher resolution. For some output ratios (e.g. 1.5:1) there is more than one combination of output attenuator ratios that can

be used (e.g. 15:10, 12:8, 9:6, 4:3) to obtain the same output current ratio. This ability allows a finer control of the output currents to be obtained. Table 7 shows the number of output levels available for different output current ratios in tripolar mode along with the average cathodal current steps size obtainable (using only one attenuator ratio the cathodal step size is 38.4μA). The table shows that for some output current ratios very fine control of the output currents can be realised using this implementation.

Table 7. Control of output currents in tripolar operation

Ratio (I1:I2)	*Number of Steps*[10]	*Imax (Cathodal)*	*Step Size (Cathodal)*
		μA	*μA*
5	516	5875	11.3
4	385	3264	8.47
3	765	6528	8.53
2.5	516	6854	13.3
2	930	6202	6.67
1.67	511	7834	15.3
1.5	769	8160	10.6
1.33	516	6854	13.3
1.25	512	8813	17.2
1	1842[11]	9754	5.30

Figure 30 shows graphically the cathodal output currents vs the input step number (steps sorted into increasing output current order) using this implementation for a 3:1 current ratio. Figure 30 shows that the finest control is possible at the lowest currents with courser control available at larger amplitudes.

[10] Reproduced values removed

[11] Using only attenuator ratios above 7:7

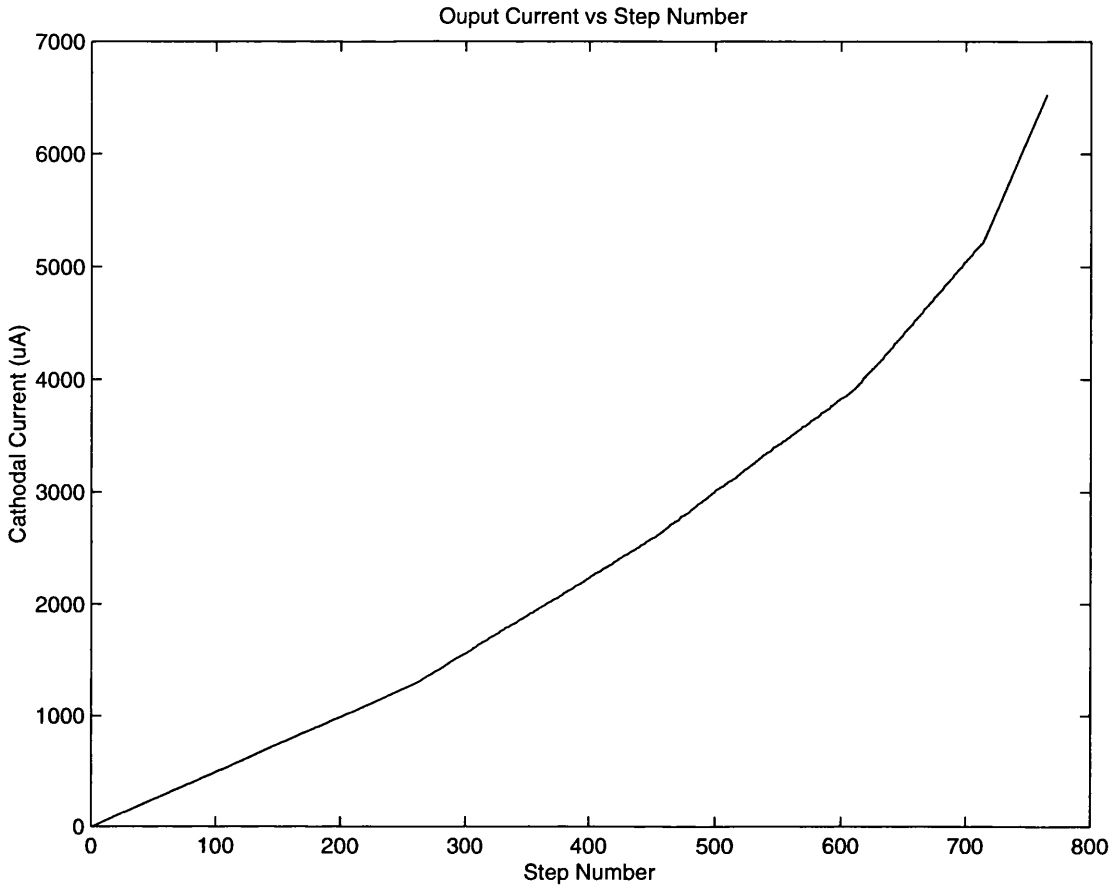

Figure 30. Output current curve in tripolar operation at 3:1 current ratio

3.4.8 Stimulation with Multiple Cuffs (The need for a Switching Array)

For correct operation of a stimulator, each cuffs has to be electrically isolated from every other cuff to prevent unwanted current flowing between cuffs during stimulation. This section discusses the methods that can be used to achieve this. A simple RF coupled stimulator with one isolated output channel is shown in Figure 31.

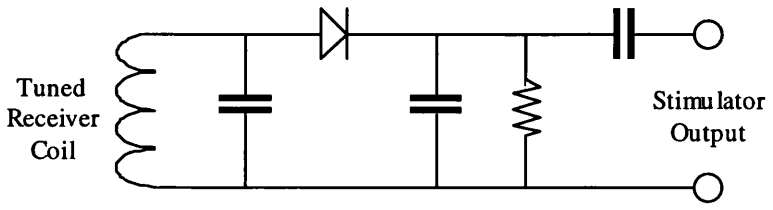

Figure 31. Simple isolated stimulator

One method for controlling multiple cuffs using this system would be to have a separate coil for each current source, each has it's own tuned receiver circuit. This is the method used for the Finetech - Brindley stimulator [15] that utilises three tuned receiver

coils tuned to 7, 9 and 11MHz. However, as each coil is quite physically large (diameter = 15mm) and this limits the number of coils that can feasibly be implanted whilst keeping the implant a reasonable size. This method is also sensitive to the transmitter / receiver coils relative positions, each separate receiver coil must lie in close proximity to its relevant transmitter coil, this gets progressively more difficult to obtain as the number of coils increases. Above three to four coils, this simple method becomes undesirable due to the size and positional constrains.

To produce a larger number of current sources, a different method must be utilised. One method is to use a single tuned coil for each group of channels that will be in simultaneous use (e.g. for tripolar stimulation two channels are required) and a multiplexer to select the relevant nerve cuff. Figure 32 shows a simplistic realisation of this type of system (dipolar stimulation). This is the method used in the LARSI stimulator (along with duration control)

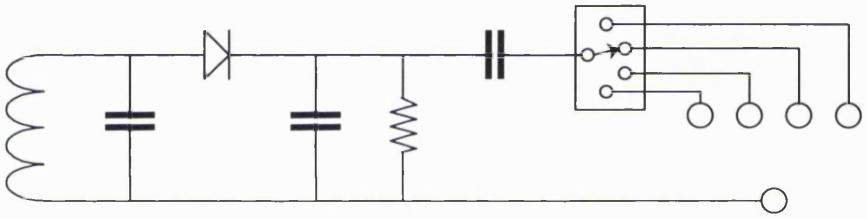

Figure 32. Four channel isolated stimulator

This method reduces the number of coils required for a six-channel tripolar stimulator from 12 to 2 (additionally some method of controlling the multiplexer is required, possibly another tuned coil for the digital data). A simple stimulator controlling two tripoles using this method is shown in Figure 33.

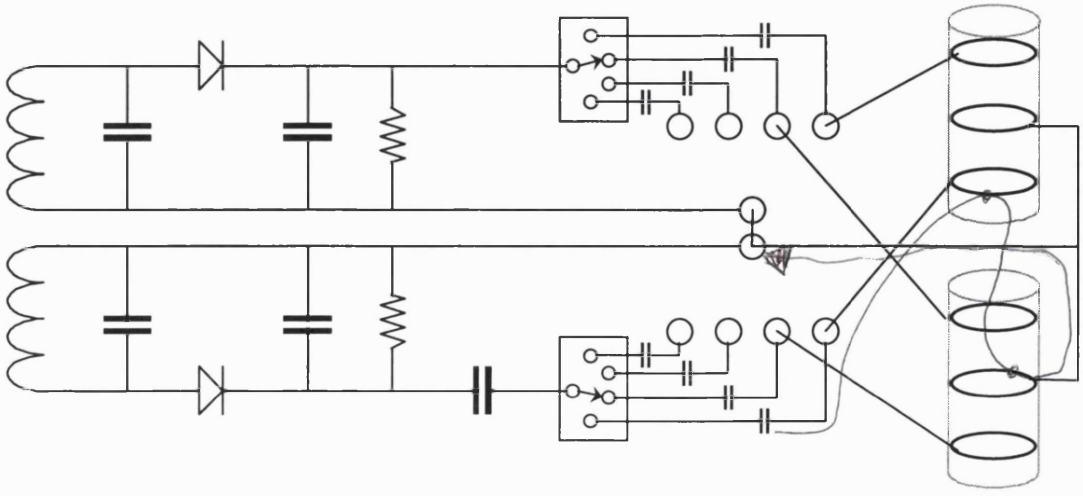

Figure 33. Four channel isolated tripolar stimulator

Using this method four coils are required to control a pentapolar cuff (plus a data channel). Realistically no more than two coils are desirable in a stimulator and ideally, only one coil would be used. The very simple devices described so far have very poor amplitude and waveform shape control and therefore are not directly suitable for a selective stimulator. The next stage in refinement is a system that has only one receiver coil and multiple current source outputs. The multiple current sources can be multiplexed to allow the control of several cuffs using one set of current sources. This implementation can be realised on a single integrated circuit allowing the number of components required for the stimulator to be minimised, simplifying implant construction and possibly allowing the implants size and complexity to be reduced.

For a small number of cuffs separate isolated outputs appears to be a suitable option as long as the outputs can be guaranteed to be isolated, to prevent crosstalk (i.e. when one cuff is being stimulated there must be no current flowing to/from the other cuffs). However, as the number of nerve cuffs increases an output stage for every separate nerve cuff must be added. For multiple cuffs the multiplexer option appears more desirable as only one output stage is required for all of the cuffs, however the multiplexer will add a series resistance between the output and the electrode. One advantage for the multiplexer option is i) the channel isolation (which can typically be $10^{12}\Omega$ using CMOS switches and a leakage current of pA, which is several orders of magnitude below the typical stimulation threshold of nerve using cuff electrodes) and ii) the reduced silicon area required for output stages (set against the increased area required for the multiplexer itself). Ideally the multiplexer should add as little series resistance as possible to maximise the output impedance that can be driven for any given power supply voltage.

The multiplexer also makes the control of several types of nerve cuff possible because it can be designed to route the currents to the desired electrode without the need for external routing connections. shows a stimulator system using a multiplexed output and one coil.

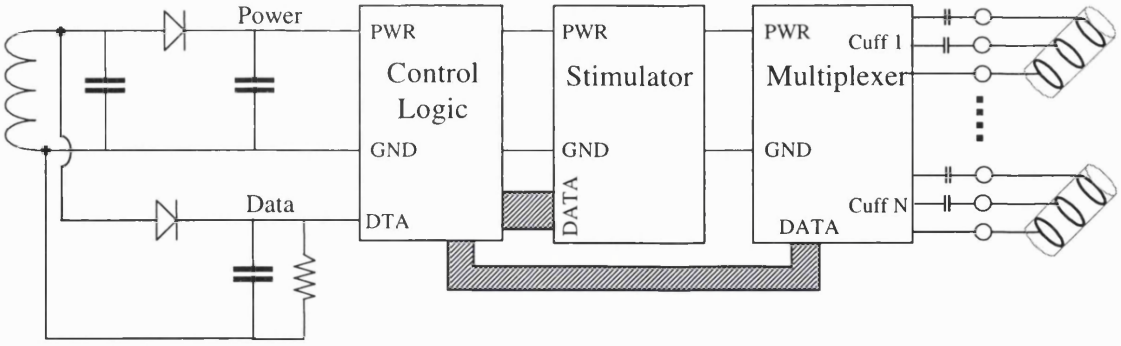

Figure 34. Figure 34. Multiple channel multiplexed tripolar stimulator

One disadvantage of the multiplexed output stimulator is that only one cuff can be stimulated at any time, therefore for a given stimulation waveform, there is an upper maximum stimulation rate that can be achieved, as discussed in section 3.3.

The problem with stimulating more than one cuff at any time could be avoided using power transformers for each cuff. This implementation is shown in Figure 35. A separate isolated data channel would also be required to control the stimulator circuits. The transformers electrically isolate each separate cuff and allow stimulation of several cuffs at the same time removing the frequency limit introduced by using one set of outputs and a multiplexer. This implementation however suffers from the need to incorporate transformer coils (using a toroidal transformer only one core with several windings would be required for power and data) in the stimulator. A second disadvantage is that separate circuits are required for each output. However, this solution may provide the answer to using Anodal Blocking in a large number of cuffs with a single stimulator device. A further development would be to have several stimulator IC's with multiplexed outputs powered via a transformer, reducing the number of windings required for a stimulator system.

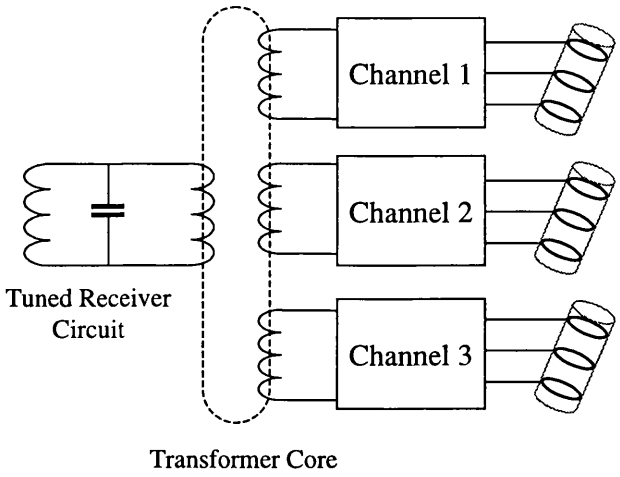

Figure 35. Multiple channel tripolar stimulator using transformers

As will be described (4.5), a differential output stage was used for the current sources and this allows the multiplexer to make the connection of the common anode / cathode connections without external connections are required to connect the common electrode. For this design, the single stimulator with one set of current sources and a multiplexer was chosen for this design rather than using separate isolated output channels for each cuff to be stimulated. The multiplexer option was chosen as a single IC can be used to control a number of nerve cuffs and implanted transformers using this implementation are not required.

3.5 Power Consumption

In a stimulator system, based around an implant powered and controlled by inductive coupling a major system limitation will be the life of the external power source. Rechargeable batteries must not be too heavy or cumbersome and yet must be able to supply power for operation all day. If this time is set at 15 hours then some simple calculations can be used to calculate the maximum implant power consumption acceptable during operation.

To keep the size of the external power source acceptable for use the maximum number of batteries is set at four 1.5V size C NiCad batteries, supplying 2550mAh [123] (6V total), supplying a 5V regulator driving the transmitter. The batteries will occupy approximately 10cm by 5cm by 5cm and weigh approximately 230g). Of course the use of modern LiH rechargeable batteries would decrease both the size and weight of the power supply for the same available power, however this increase in capacity should be used to decrease the dimensions and weight of the external system.

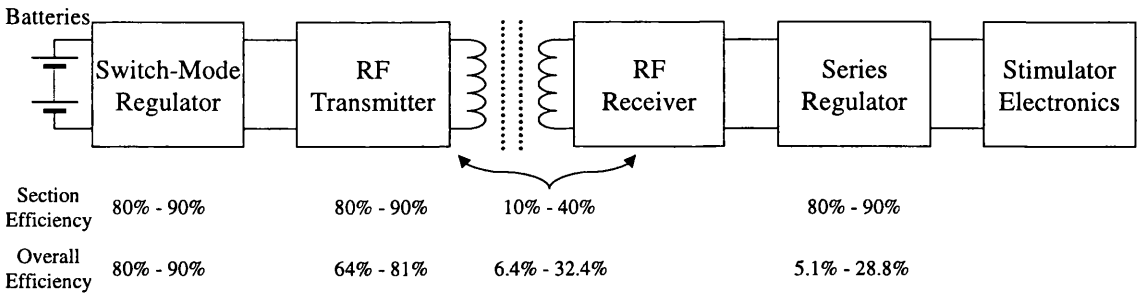

Figure 36. Estimated inductively couple stimulator efficiency

Figure 36 shows an example transmitter – receiver link for an implanted stimulator and some estimated operating efficiencies for each part of the link. The overall efficiency will depend significantly on the coupling between the transmitter and receiver tuned circuits (quoted as 10% to 40% in Figure 36), the overall efficiency of the system can be defined as:

$$System\ Efficiency = Eff_{Switched\ Regulator} \times Eff_{Transmitter} \times Eff_{RF\ Link} \times Eff_{Ser\ Regulator} \quad (3.1)$$

If the link was operated at critical coupling (K_{CRIT}), the system efficiency could be as high as 29%, however as some patients will be overweight and the coil position will move during operation this may be impossible to achieve. The minimum estimated system efficiency using these values is only 5%.

Assuming the transmitter – receiver is operating at 5% efficiency, then 127mAh are available inside of the implant. For 16 hours of operation, this gives us an average available current of 8mA. Assuming the device is used for only 33% of the day (a rather high estimate) and turned off for the rest of the time then the available current becomes 24mA. This defines the absolute maximum current available inside the implant. To allow for ageing of the batteries, incomplete charging, longer than expected usage a value 50% lower than this limit was decided upon (12mA).

Allowing the Stimulation Unit 30% of the quiescent current in the implant and defining a maximum current during stimulation of 20mA (four output channels stimulating at 5mA for 1ms). The following specification meets the power requirement:

Quiescent Current: 5mA

Current During Stimulation: 25mA

3.6 Choice of Blocking Capacitor Value

Although the absolute value of blocking capacitor does not have to be defined, the expected range of values has to be considered for the stimulator design. The choice of blocking capacitor value is affected by two parameters: i) The maximum voltage produced on the capacitor during stimulation and ii) The physical size of the blocking capacitor. The voltage the capacitor drops during a stimulation pulse will limit the maximum current the stimulator can produce using any given power supply. The physical size of the capacitor will affect the overall size of the implant. Figure 37 shows the maximum capacitance available for a given case size (as of November 1999) and the voltage dropped against the case size of the capacitor. The capacitors shown in Figure 37 are available from a number of manufacturers (namely AXV [5], TDK [138] and Murata [93]) in one or more of the values shown and are all specified for use up to 16V.

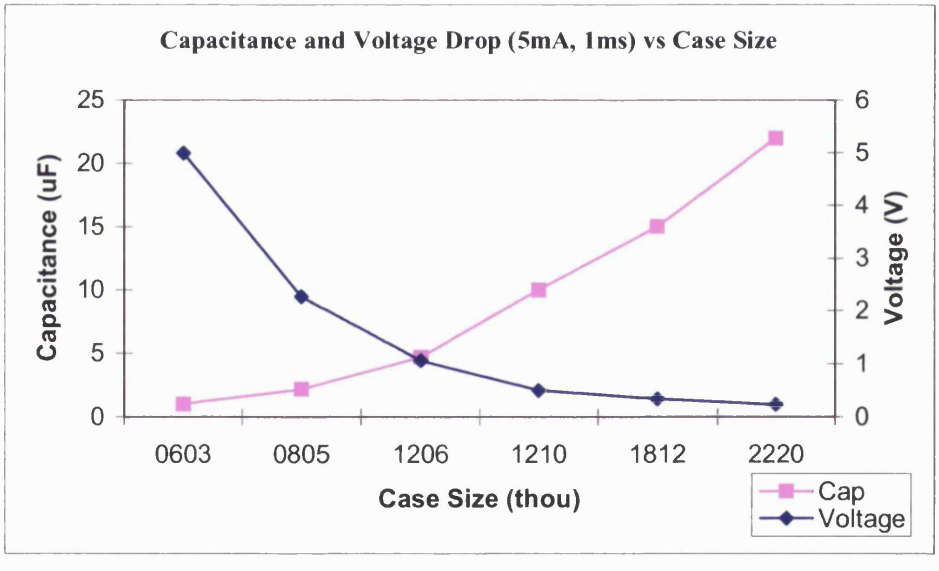

Figure 37. Capacitance and voltage vs case size for blocking capacitors.

Figure 37 shows that for a required 500mV maximum voltage drop (with a 5mA, 1ms stimulation pulse) a 1206 10uF capacitor could be used. Table 8 shows the physical area occupied by a blocking capacitor for each case size and the voltage dropped during maximal stimulation.

Table 8. Blocking capacitor parameters

Case Size (Thou)	Capacitance (μF)	Area occupied (mm^2)	Voltage Dropped (V) (5mA, 1ms stimulation)
0603	1	1.28	5
0805	2.2	2.84	2.3
1206	4.7	5.12	1.1
1210	10	8.53	0.5
1812	15	15.36	0.3
2220	22	31.28	0.2

As Table 8 and Figure 37 show the final choice of capacitor will be a compromise between physical size and the voltage dropped, however the availability of 4.7μF - 10μF in reasonably sized cases would suggest a value of at least 4.7μF is a realistic value for use as a blocking capacitor.

3.7 Choice of Manufacturing Process

The specification states that the system should be capable of delivering 5mA pulses into load impedances of 1kΩ, so that a 5V potential difference may exist across the load during stimulation. However taking into account voltage drops due to the internal on-chip switches and the off-chip blocking capacitors, the supply voltage must be greater. Ideally, a process that has ± 15V supplies could be used allowing the use of small external blocking capacitors and allowing larger load impedances to be driven. It was felt that the feasibility of the design should be checked using a low cost ±5V, process although this will reduce the maximum current * maximum load resistance produce, limiting the achievable output current at a particular load impedance.

The Mietec 2.4μ process was chosen for this stimulator. This is a 12V CMOS, dual-layer metal, and dual-layer poly-silicon process. The reason for choosing it was primarily cost, it is relatively cheap (80ECU[12] per mm^2). Another point of view in its favour is that it is quite old and therefore well characterised. Smaller feature sized processes are typically lower voltage (5V and below) making them even less suitable. However, some processes recently available have both small feature sizes and high

[12] ECU: European Currency Unit, replaced by the Euro (€) in Jan 99.

voltage devices (up to 50V for the AMS High Voltage 1.2µ process). When this project was started, the latter processes were not available for projects or were unacceptably costly for a student project (in 1997 (after the initial designs were completed) the Mietec 0.7µ 50V-process costs 375ECU/mm^2). However, the possible migration to a higher voltage process later was kept in mind during the design.

3.8 System Design

The specification for the stimulator was developed to give as much flexibility in application as possible. The prototype devices will only be able to stimulate a small number of cuffs, however the design should allow this number to be easily expanded. The complete stimulator system can be divided into three main sections as shown in Figure 38.

1. The Control Box
2. The Transmitter
3. The Implanted Stimulator

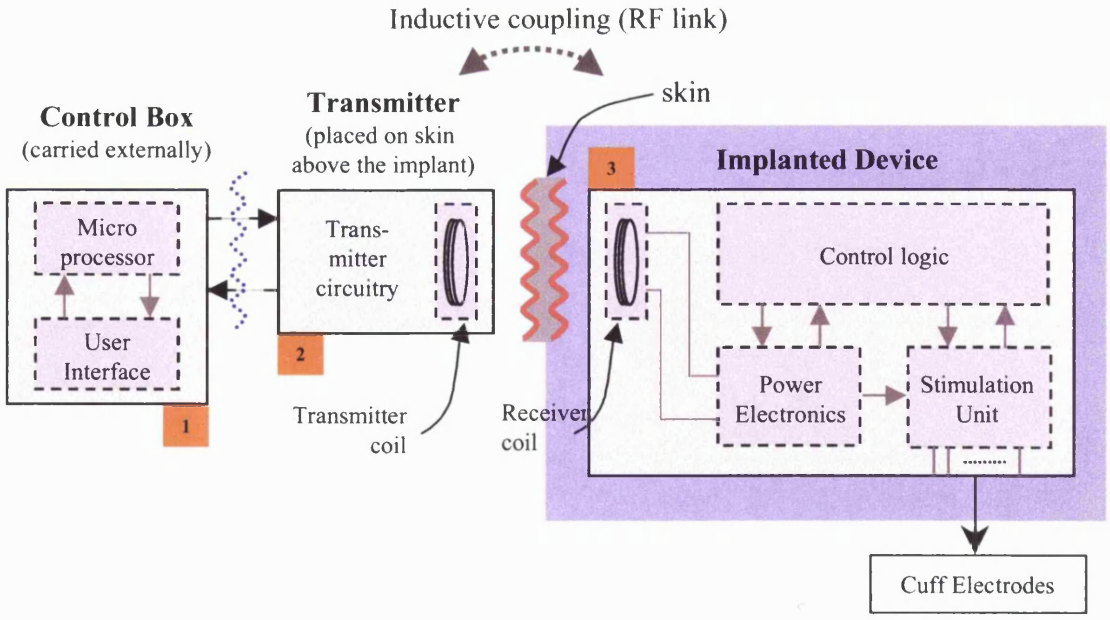

Figure 38. Selective stimulator system overview

The Control Box is an externally worn system that deals with the generation of stimulation patterns, communication with the implanted device and provides the user interface. The purpose of the tuned RF transmitter is to provide power and data for the

in this thesis as they share many characteristics of the LARSI device counterparts and were not developed during the course of this PhD study.

The implanted stimulator can be divided into three main sections

1. Power Electronics
2. Control Logic
3. Stimulation Unit

1. The Power Electronics for the implantable stimulator are to be based around LARSI design, as discussed in 1.3. It consists of discrete components that generate the power supplies for the internal electronics and demodulate the transmitted data.
2. The Control Logic decodes the received data, generates all the digital timing signals required by the stimulation unit, and provide the signals used by the Power Electronics to communicate with the Control Box.
3. The Stimulation Unit produces the quasitrapezoidal or square charge balanced current outputs using the signals provided by the Control Logic. The SU has to communicate to the Control Logic when the stimulation has finished.

Due to the expected complexity of the Control Logic and Stimulation Unit, both have to be integrated circuits. Ideally all of this electronics should be included on a single IC, however during the design of this implant it was decided that the logic and stimulation electronics would be realised separately. The control logic has been realised using a MPGA (Mask Programmable Gate Array) and is purely digital. An overview this device is discussed in Chapter 5.

This thesis concentrates on the development of the electronics for the Stimulation Unit.

3.9 Implant Specification

From the points discussed previously in this chapter, a complete specification for the proposed selective stimulator prototype was defined:

Number of Nerve Cuffs:		3 Dipolar Electrode Cuff
	or	2 Tripolar Electrode Cuff
	or	1 Pentapolar Electrode Cuff
Plateau Amplitude:		20μA to 5mA in 20μA steps
Plateau Duration:		20μs to 1016μs in 4μs steps
Reverse Amplitude:		1/6.7 to 1/46 in multiples of 1/6.7
Ratio of output currents:		0:1 to 1:1 in steps of 1/15
Power Consumption (@10V):		< 25mA during stimulation[13] pulse
		< 5mA quiescent

This specification should allow the use of this stimulator to investigate selective stimulation by fibre-size and selective stimulation by fibre-position. From this specification, the requirements for each of the blocks inside the Stimulation Unit were derived and are detailed in Chapter 4.

3.10 Design of the Stimulator Core

From the Specification given in 3.9 the structure of each data word required for each stimulation pulse was developed. The relationship between the stimulation pulse and the digital data word is shown in Figure 39.

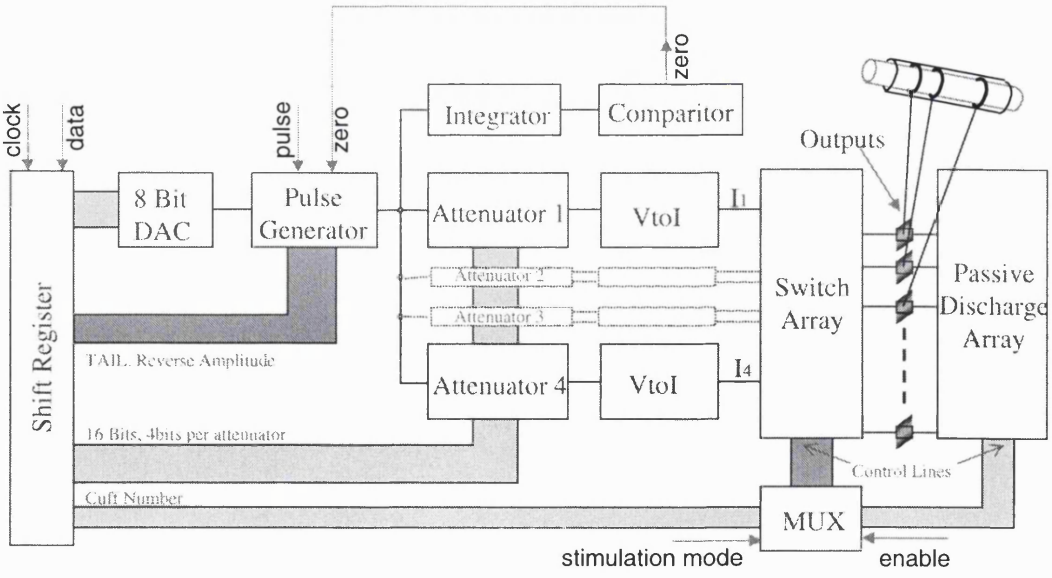

Figure 39. Proposed organisation of the stimulation unit

In addition, from the specification given in 3.9, the modular system shown in Figure 38 was developed. The system was broken down into defined modules; each module has a specific task in the generation of the stimulation waveform. This design method allowed individual specifications for each block to be defined (given in chapter 4 for each module) before the design process on that section was started. During the development, IC's had to have sufficient testability to allow for the detection / correction of problems in the individual modules.

A single shift register is loaded with a word that defines the stimulation pulse. An eight-bit DAC is used to produce a variable reference voltage; this reference voltage is used by the pulse generator to define the amplitude of either a square or quasi-trapezoidal shaped voltage waveform. The pulse generator is also set up, using four bits from the shift register, to i) enable / disable the exponential tail (1bit) and ii) define the reverse amplitude (3 bits). The duration of the plateau is controlled by an external signal 'pulse' generated by the control logic and the stimulation ended by the signal 'zero'. The output of the pulse generator is integrated to determine the end of the reverse current phase and generate the 'zero' signal via a comparator. The voltage waveform is then attenuated by attenuators 1-4 to produce four variable-amplitude versions of the waveform generated by the pulse generator. The outputs of the attenuators are converted from a voltage to a current using four transconductor stages (VtoI) to produce four stimulation output currents. These outputs are then switched depending on the operating mode to the correct output using the switching array. The discharge array consists of resistors and switches attached to the outputs to allow the removal of and remaining charge imbalance after stimulation.

This system allows the proposed specification to be met. This design also allows the number of cuffs controlled by the stimulator to be increased simply by adding extra switches to the switching and discharge arrays.

For the prototype IC's the number of bits required for the shift register is given below and compared to the number of bits required for a stimulator capable of controlling six tripolar or three pentapolar nerve cuffs. The table shows that only one extra bit is required for a complete stimulator system.

---

[13] Including Stimulation Currents, excluding stimulation currents <5mA

Table 9. Number of bits required for the stimulator modules

Configuration	DAC	Pulse Generator	Attenuators	Switching Array[14]	Total
Prototype Stimulator	8	4	16	2	30
6 Tripolar / 3 Pentapolar	8	4	16	3	31

In addition to the bits shown in Table 9, 8 bits are required to define the pulse duration, these bits are used by the control logic. The total number of required bits for each stimulation pulse is therefore 39 (31 + 8) plus any other control information sent (such as a coupling measurement request).

The individual blocks for the stimulation unit were developed using Cadence Analogue Artist to simulate and layout the designs.

[14] Number of bits required to define the cuff number (not total number of bits required for the switching array control).

3.11 Summary

The complete specification for the proposed prototype of the selective stimulator are given below:

Number of Nerve Cuffs:		3 Dipolar Electrode Cuff
	or	2 Tripolar Electrode Cuff
	or	1 Pentapolar Electrode Cuff
Plateau Amplitude:		20μA to 5mA in 20μA steps
Plateau Duration:		20μs to 1016μs in 4μs steps
Reverse Amplitude:		$\frac{1}{46}, \frac{2}{46}, \ldots, \frac{7}{46}:1$ (i.e. Approximately 2% to 15% of the plateau amplitude)
Ratio of output currents:		0:1 to 1:1 in steps of 1/15
Power Consumption (@10V):		< 25mA during stimulation[15] pulse < 5mA quiescent

From this general specification, individual specifications were developed for each module inside of the stimulation unit. These specifications are included in Chapter 4.

This specification should allow the use of this stimulator to investigate selective stimulation by fibre-size and selective stimulation by fibre-position.

[15] Including Stimulation Currents, excluding stimulation currents <5mA

Chapter 4. Development of Analogue Blocks for the Stimulator Core

4.1 Introduction

This chapter gives the detailed design, implementation and testing of integrated circuits for the selective stimulator described in Chapter 3. The circuits discussed in the following chapter are:

4.2.Digital to Analogue Converter (DAC)
4.3.Pulse Generator
4.4.Attenuators
4.5.Transconductors
4.6.Switching and discharge arrays
4.7.Long time constant Integrator

Deviations from expected results are discussed and suggestions are presented that will overcome them in future designs.

Simulation results from a complete stimulation unit are presented in 4.8. Experimental results obtained from the circuits connected as a complete stimulator are presented in 4.9.

The transistor equations used to describe the behaviour of circuits in this chapter are given in Appendix 2.

The partitioning of the stimulation modules onto three integrated circuits (SSTIM1, SSTIM2 and SSTIM3) and the testing circuits used to obtain the results presented in this chapter are discussed in Appendix 1.

Finally, a summary of this chapter is given in 4.11.

4.2 Digital to Analogue Converter (DAC)

4.2.1 Specification

From the specification given in 3.9, the specification for the DAC was derived. The primary consideration was the ability to generate 256 monatomic voltage divisions. The 1% settling time was defined as 3μs, to allow the DAC to have settled to 1/3 LSB (0.1%) within half a data clock cycle. Half a data clock cycle is 12μs assuming a 83.3kHz data rate.

Table 10. DAC specification

Parameter	Value
Number of divisions	256 (8-bits)
Offset	< 1/3 LSB (least significant bits)
Linearity (maximum deviation)	< 1/3 LSB, Monatomic
Settling time (1%)	< 3μs
Digital data control	Serial data input

4.2.2 Implementation

The Mietec 2.4μm process contains an 8-bit monatomic DAC as a standard cell and this has characteristics that fit this specification. The characteristics of the standard cell are given below [91]:

Table 11. Mietec standard cell DAC

Parameter	Value
Number of divisions	256 (8-bits)
Offset	< 1/4 LSB
Linearity	< 1/4 LSB, Monatomic
Settling time (1%)	$\approx 4*R_{out}*C_{load}$
Digital data control	Parallel data Input
Output Impedance (Rout)	≈ 100kΩ

The high output impedance of the DAC is >100kΩ, meaning that the loading on the output of the DAC means that the loading on the DAC must be high impedance (i.e. capacitive), and therefore a voltage follower amplifier was designed to act as a buffer at the output of the DAC. The input data for the DAC is loaded through a shift register and

digital buffers, allowing the DAC to be controlled serially. An overview of the DAC stage implementation is shown in Figure 40.

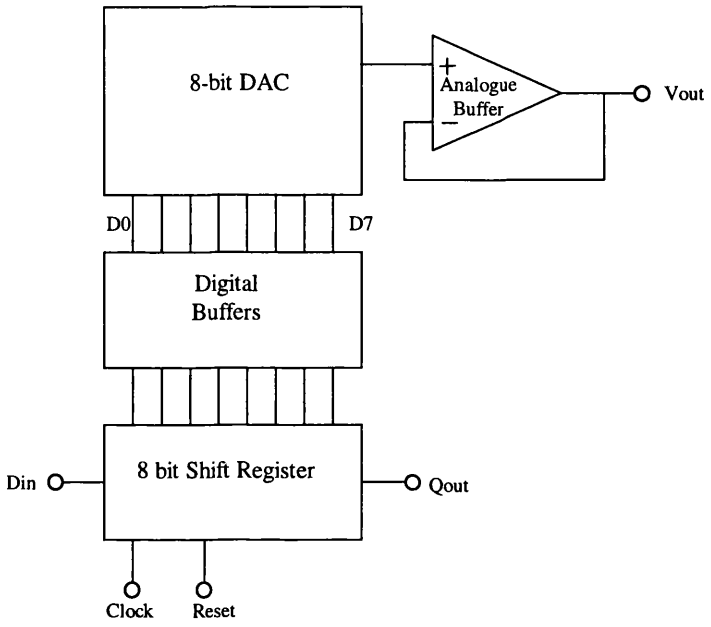

Figure 40. Overview of the DAC

The digital standard cells for the Mietec process operate using -5V to 0V supplies, so that the output of the DAC is in the range -5V to 0V, and the voltage follower should have at least this output range.

The specification for the DAC amplifier is given in Table 12. The offset specification comes from the fact that the DAC standard cell has a maximum error of 1/4 LSB and the main specification defines the maximum permitted error as 1/3 LSB requiring the amplifier offset to be a maximum of 1/12LSB (or 1.7mV). The DC gain specification comes from the linearity requirement of 1/3LSB, the DAC standard cell has a maximum non-linearity of 1/4 LSB, and so the non-linearity due to the amplifier gain error must be kept below 1/12LSB. The amplification error due to the open loop DC gain is given by:

$$\text{Gain Error} = \frac{A_d}{1 + A_d / k} - k \qquad 4.1$$

Where A_d = open loop DC gain and k = designed closed loop gain

With a closed loop gain of 1, the open loop DC gain must be greater than 72dB.

Table 12. DAC amplifier specification

Parameter	Value
Open-Loop DC Gain	> 72dB
Offset	< 1.7mV (< 1/12 LSB)
Settling Time (1%)	< 3μs (C_{Load} = 12pF)
Slew Rate	> 2.5V /μS
Output Swing	+0V -4.9V

The amplifier is shown in Figure 41.

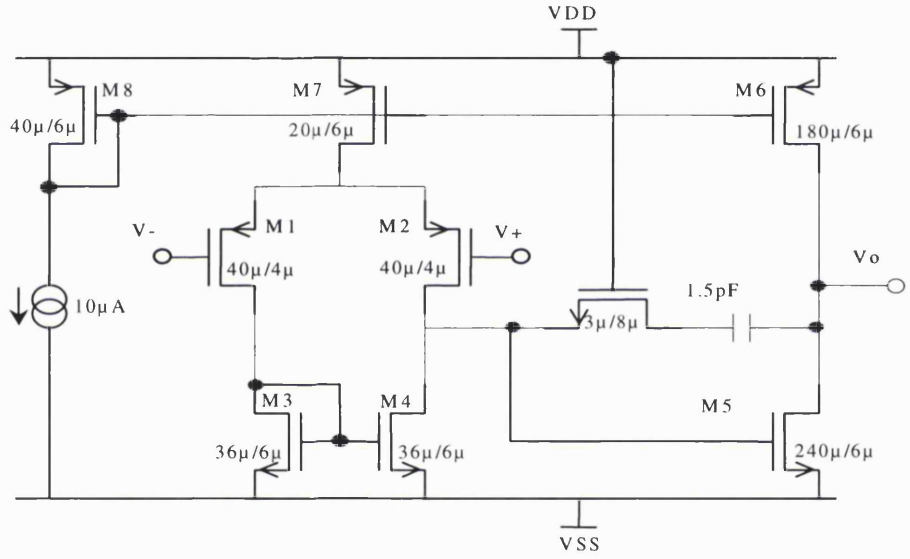

Figure 41. Two-stage DAC op-amp (transistor sizes shown)

It is a simple two-stage operational amplifier with p-channel input FETs (Field Effect Transistors), and uses +5V (VDD) and -5V (VSS) power supplies. The amplifier is not suitable for driving small resistive loads as the current drive for voltages >0 is limited to the bias current supplied by M6 (45μA), however, as the pulse generator [4.3] has an input impedance >500kΩ this limitation is not significant.

4.2.3 Results

The simulated and experimental characteristics of the amplifier are compared in Table 13. The results show that the experimental values lie within the simulated

tolerances[16]. The simulated parameter ranges all meet the specification given in Table 12.

Table 13 . Characteristics of the DAC op-amp

Parameter	Simulated Range		Experimental Value[17]
DC Gain	85.2dB	96.4dB	89.8dB
Input offset voltage	0.5mV	1mV	0.6mV ± 0.5mV
Slew Rate	3.2V/µs	3.5 V/µs	3.3V/µs ± 0.2V/µs
Settling Time (1%)	2.4µs	2.9µs	2.7µs ± 0.2µs
Output Swing Range	-4.95V +4.1V	-4.97V +4.4V	-4.95V +4.2V
Unity gain bandwidth	3MHz	3.8MHz	3.3MHz ± 0.2MHz

The testing results for the DAC are given in Table 14. The largest absolute deviation from linearity found for the DAC was 0.14LSB this compares with the quoted worst-case accuracy of 0.5LSB [91] for only the standard cell of the DAC.

Table 14. DAC testing results

Parameter	Value
Offset	-0.4mV to 1.0mV (<1/20 LSB)
Linearity[18]	< 1/7 LSB, Monatomic
Settling time (1%)	2.7µs ± 0.3µs

4.2.4 Summary

The DAC design meets the developed specification. The testing of the DAC and DAC amplifier showed that this implementation was suitable for the stimulator system, producing an accurate reference voltage for the pulse generator circuit.

[16] Simulated tolerances based on expected process variations supplied by foundry [90]

[17] Measured in Five Integrated Circuits

[18] Maximum Absolute Deviation

4.3 Pulse Generator

4.3.1 Introduction

The pulse generator is needed to generate either square or quasi-trapezoidal voltage waveforms with a controlled amplitude, duration, tail and reverse phase amplitude ratio. The implementation is discussed in the following section.

4.3.2 Specification

The specification is based around the general specification given in 3.9. The specification for the pulse generator is in Table 15. The Plateau Amplitude (Ar) range comes from voltage-input range required for the transconductors (voltage to current converters) discussed in 4.5. The rise time specification is due primarily to the need to generate short pulses (for use with conventional stimulation) of duration down to 16μs and secondly by the fact that the threshold for stimulation increases as the pulse rise time increases [71]. The other requirements come from the general specification given in 3.9.

Table 15. Pulse generator specification

Parameter	Value
Plateau Duration	16μs to 1ms in 4μs increments
Plateau Amplitude (Af)	6mV to 1.5V in 6mV increments
Reverse Phase (A_R)	1/6.7 to 1/47 (2% to 15%) of the pulse amplitude (Af) where: $A_R = \frac{A_f}{6.7n}$ where n = 1 to 7
Pulse Rise Time (90%)	< 8μs
Pulse Tail	i) Exponential with time constant of 350μs (Variable after Integrated Circuit manufacture) ii) Fast decay with time constant <10μs

4.3.3 Implementation

The specification states that it is required to allow the exponential decay variable to be modified after manufacture, to allow different time constants to be implemented for different stimulation applications. The stimulation pulses must be produced with the minimum of required controlling signals (ideally one signal to generate the pulse plateau and another to end the stimulation pulse) and use the output of the DAC to define the plateau voltage (Vplat).

Figure 42 shows a circuit that will produce simple quasi-trapezoidal waveforms. Initially S1 is open and V2 = Ar, when S1 closes, C1 will be charged to Af, then when S1 opens V2 will decay exponentially to Ar with a time constant given by:

$$\tau = R_p C_p \tag{4.2}$$

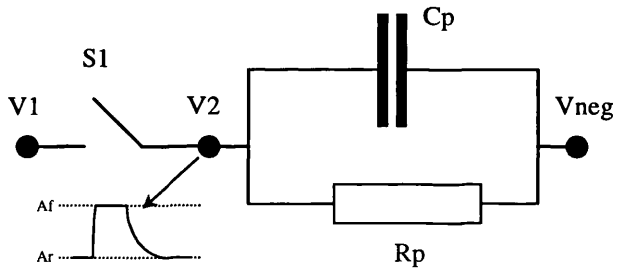

Figure 42. Simple RC circuit to produce a quasi-trapezoidal waveform

For a reasonable integrated capacitance value such as Cp=5pF, Rp must be 70MΩ. Such a large value of resistance is unrealisable in an integrated circuit as a passive component. Using a FET to replace this resistance is undesirable due to the large voltage changes occurring across the FET and the relatively high resistance required. At this point it was decided that it was reasonable for both the capacitor and the resistor to be external components. This has the advantage that it makes changing the value of the RC time constant relatively simple after manufacture, which is required in the specification. By taking the capacitor external to the Integrated Circuit the need for an extremely high resistance is removed. This solution introduces the need for two external components, but provides the means to change the exponential decay time constant over a wide range.

The circuit in Figure 42 has the problem that the resistance of the switch S1 will cause the voltage V2 to be lower than Af due to the potential divider caused by R_{switch} and Rp. For a 2kΩ switch resistance and Rp=175kΩ (Cp = 2nF) the voltage drop across

the switch will be 1.1%Vplat. Simply placing a switch in series with Rp can remove this problem, by disconnecting the resistive load during the plateau period of the stimulation pulse, as shown in Figure 43.

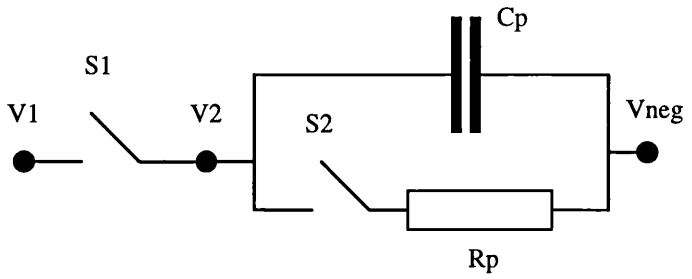

Figure 43. RC circuit to remove inaccuracies in plateau voltage

This circuit will introduce an error in the time constant, due to the resistance of S2, however using the same values as previously the error introduced using a 2kΩ switch is 0.57% of the time constant (i.e. τ=352μs). This error is not significant, as the absolute value of the decay constant is not critical for anodal blocking and small compared with the expected component tolerances (typically 1%-5%)

To allow the pulse generator to produce pulses that do not have the exponential tail the only modification required to the circuit is to add another switch in parallel with Rp (shown in Figure 44 as S3). A switch with a resistance of 5kΩ will reduce the time constant to approximately 5μs, allowing the specification to be met. A smaller switch resistance will decrease the time constant further.

One limitation of this circuit has is that Vplat has to charge Cp within a time period not exceeding about 5μs, in order to produce a pulse with a sharply rising edge required in the specification. This circuit also only produces pulses that transition between Ar and Af, and do not return to zero. Both of these limitations can be removed by adding a sampling stage that holds the output at zero until the capacitor Cp is fully charged. This also has the benefit of allowing the output to be set to true zero at the end of the stimulation pulse.

This implementation is shown in Figure 44 (sampling stage switches S4 and S5) along with associated voltage waveforms and required data lines. Included in Figure 44 are the amplifiers required to: i) buffer the output of the DAC (Af) so the large capacitive load can be driven and ii) generate the reverse amplitude Ar from Af.

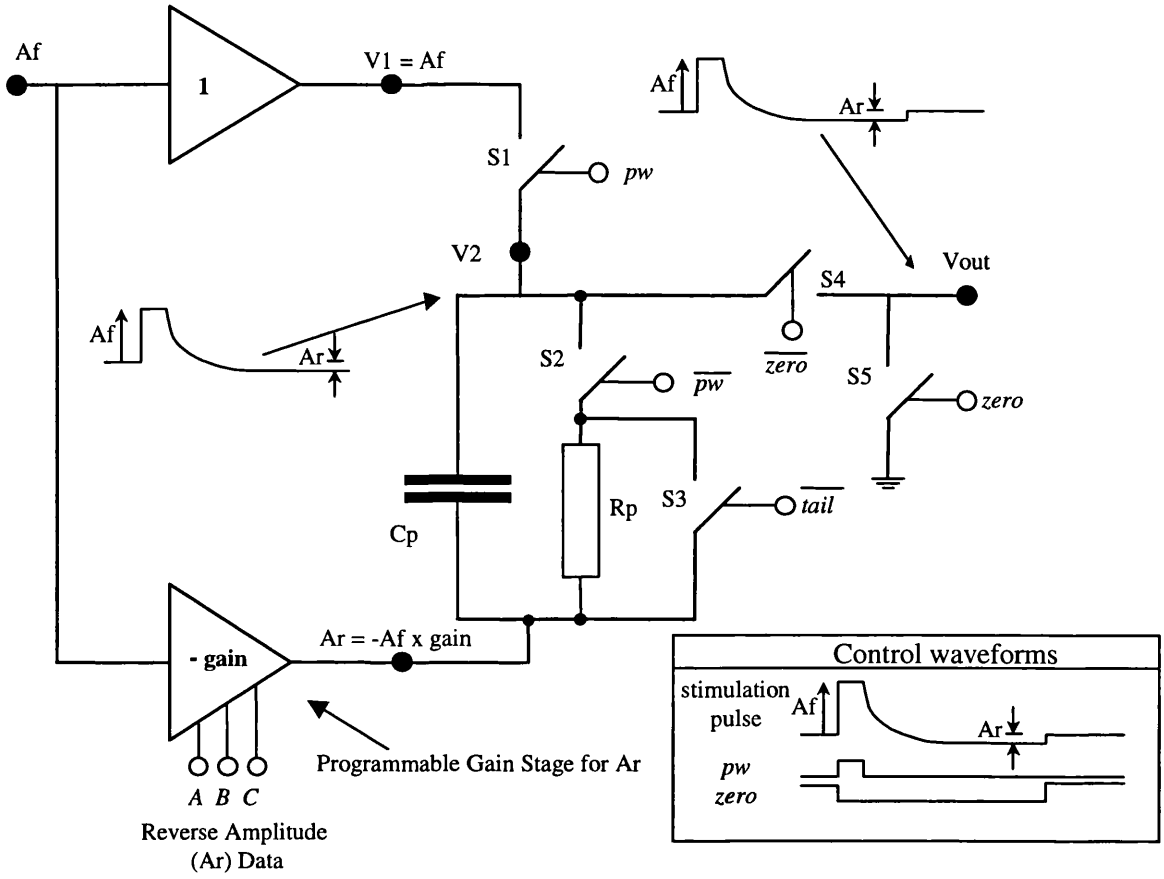

Figure 44. Pulse generator implemention

All of the switches in this module have been implemented using single n-channel or p-channel FETs. The sizing of the transistors around the capacitor was influenced by two factors, i) the error they are expected to introduce over a range of RC values, ii) minimisation of switching transients (due to charge injection and differences in switching times).

The variable gain of the amplifier for the reverse phase has been implemented using switched complementary pairs of FETs for the feedback resistances and a T-Cell voltage divider of FETs (T-Cell discussed in 4.7) at the input, allowing various amplifier gains to be set.

The only remaining problem with this implementation is due to the impedance of the output switches (2-4kΩ) implying that the driving of resistive loads needs to be carefully considered. As the input of the attenuators is resistive (Rin ≈ 16kΩ), the output of the pulse generator should be buffered in a complete stimulator device.

4.3.3.1 Amplifier Implementation

The amplifiers which precede the pulse generator must be capable of driving a large external capacitive load of 1-2nF. Their design is shown in Figure 45. It is a two-stage amplifier with a class AB output stage. The output stage has a limited output voltage swing, however this is not significant (the gain of the DAC can be modified simply by changing the gain of the DAC amplifier). Moreover, as will be seen in 4.5, the transconductors require a similarly reduced input range.

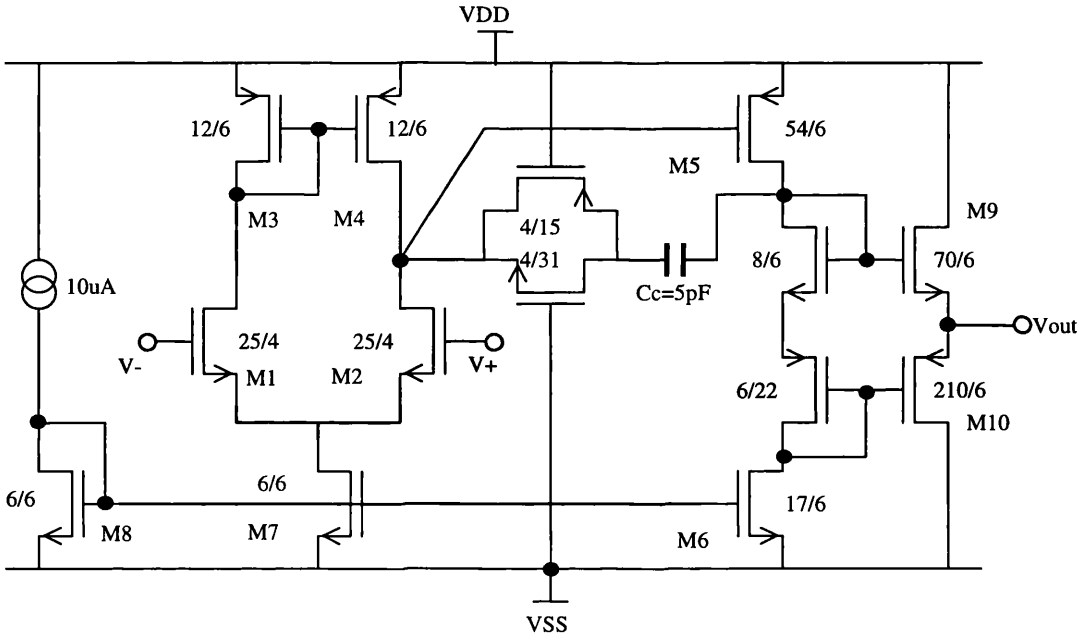

Figure 45. Amplifier for the pulse generator

The specifications for the amplifier are shown Table 16. The DC gain specification was set to a minimum of 4000 although, in this application, the actual value is not critical. The slew rate was defined to allow the amplifiers to produce the fast edges on the pulses. The output swing range is set 25% higher than the specification for the pulse generator (4.3.2), allowing a reasonable operating overhead. The offset is important as it affect the accuracy of Ar (and to a far less extent Af): 1.5mV was chosen to keep the errors for a minimum amplitude pulse below 20% (using 1/47 reverse phase). The effect of offset on Af is far smaller as when the worst-case error occurs in Ar the percentage change in Af due to a similar offset will be 47 times smaller (0.5%). As this waveform drives the attenuators and transconductors and is integrated to detect when the injected charge is zero, the absolute offset values are not critical.

Table 16. Specifications of the pulse generator opamp

Parameter	Parameter
DC Gain	72dB
Unity gain bandwidth (C_{load}=100pF)	1.0MHz
Input offset voltage	1.3mV
Slew Rate	2.0V/μS
Output Swing Range	+2.0V -2.0V

4.3.4 Simulation Results

The simulated characteristics of the pulse generator amplifier are shown in Table 17: these meet the specification. The only characteristic that does not exceed the specification is the input offset voltage that has an upper limit that only just meets the criterion.

Table 17. Pulse generator amplifier simulated characteristics

Parameter	Specification	Simulated Range	
DC Gain	72dB	75dB	89.9dB
Unity gain bandwidth (C_{load}=100pF)	1.0MHz	1.5MHz	2MHz
Input offset voltage	1.3mV	0.2mV	1.3mV
Slew Rate	2.0V/μS	+1.9V/μS -3.8V/μS	+3.6V/μS -4.6V/μS
Output Swing Range	+2.0V -2.0V	+2.1V -2.6V	+3.2V -3.6V

The behaviour of the pulse generator was extensively simulated; Figure 46 shows an example of a waveform with an exponential falling edge and a negative second phase of equal area to the positive phase. Table 18 shows the simulated characteristics of the pulse generator. Their range lies within the range required by the specification for all of the parameters. However to meet the specification, the pulse generator timing determined by external components Rp and Cp must be sufficiently accurate. For the pulse generator

it has been assumed that all of the external reference signals (Ar, zero and pw) are of nominally defined amplitude and duration.

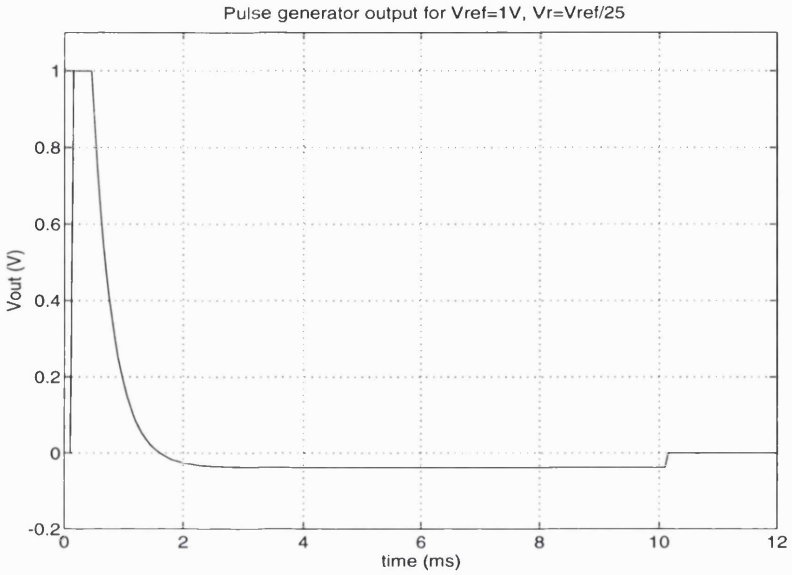

Figure 46. Simulated response of the pulse generator for a 1V pulse plateau and a reverse phase of 1/26

Table 18. Pulse generator simulated characteristics

Parameter	Specification	Simulated Range
Plateau Duration	16µs to 1ms in 4µs increments	Greater than 5µs, step size defined by control signals
Plateau Amplitude (Af)	6mV to 1.5V in 6mV steps	5.54mV – 6.79mV to 1.523V– 1.546mV in 5.95-6.04mV steps
Reverse Phase (A_R)	1/6.7 to 1/47 (2% to 15%)of (Af) where: $A_R = \frac{A_f}{6.7n}$ where n = 1 to 7	1/6.7 –1/6.6, 1/13.2 – 1/13.4, 1/ 19.7 – 1/20.3, 1/26.3 – 1/26.8, 1/32.6 – 1/33.2, 1/39.1 – 1/40.2, 1/44.1 – 1/46.1
Pulse Rise Time (90%)	< 8µs,	5µs - 7.5µs.
Exponential Tail	Exponential with time constant of 350µs (Variable) Fast decay of time constant <10µs	Time constant defined by external components 6.2µs – 9.3µs

4.3.5 Experimental Results

4.3.5.1 Pulse Amplitude and Duration

Both the pulse amplitude and duration depend on external signals for their definition, namely *Af* for the amplitude; *pw* and *zero* for the pulse duration. The output of the pulse generator for various amplitudes, defined by Af and generated by the DAC, is shown in Figure 47, and pulses of various durations are shown in Figure 48.

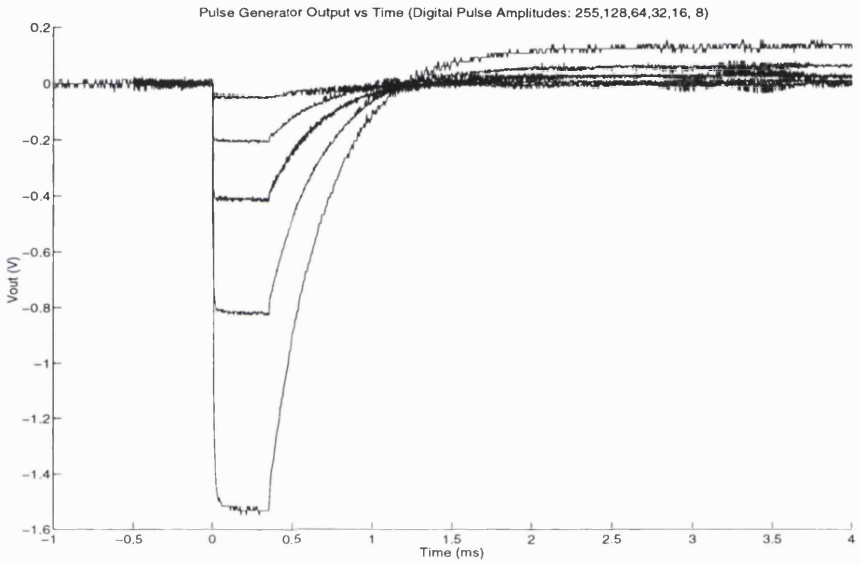

Figure 47. Pulse generator output for various pulse amplitudes

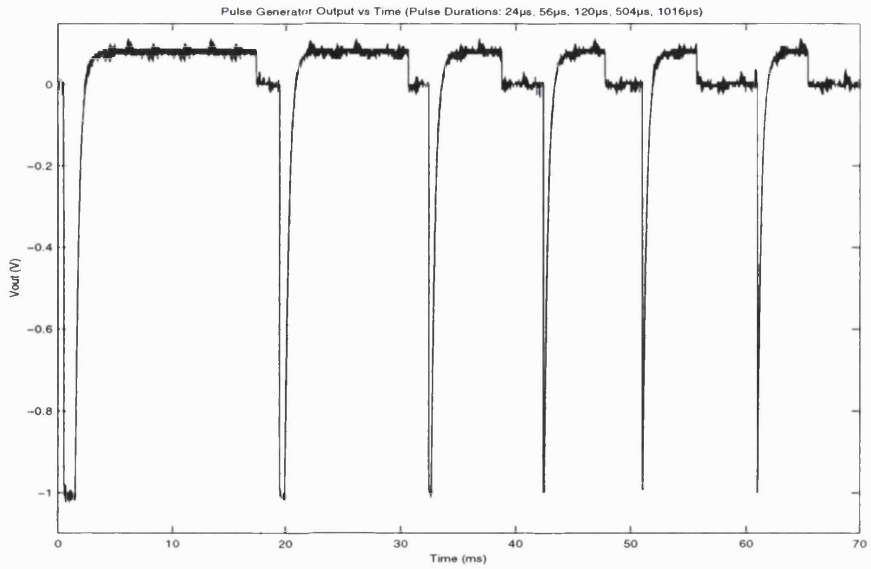

Figure 48. Pulse generator output for various pulse durations

Figure 47 and Figure 48 demonstrate that the pulse generator, when implemented in silicon, is capable of generating quasi-trapezoidally shaped pulses of controllable amplitude and duration whose absolute definition depends on external control signals. Tests show that the amplitudes and durations meet the specification.

4.3.5.2 Exponential Tail

Figure 49 shows the output of the pulse generator with various nominal tail time constants (200µs, 300µs, 400µs, 500µs, 600µs). The load capacitance for the time constant was kept constant at 680pF and the tail resistance set to the closest available resistor value. The figure shows that the time constant of the pulse generator is adjustable after Integrated Circuit manufacture over a range of 200µs - 600µs, which is in excess of the range required for anodal blocking. The actual range examined was 100µs – 3ms, obtained by varying both the time constant resistance and capacitance, however this range is not required for anodal blocking.

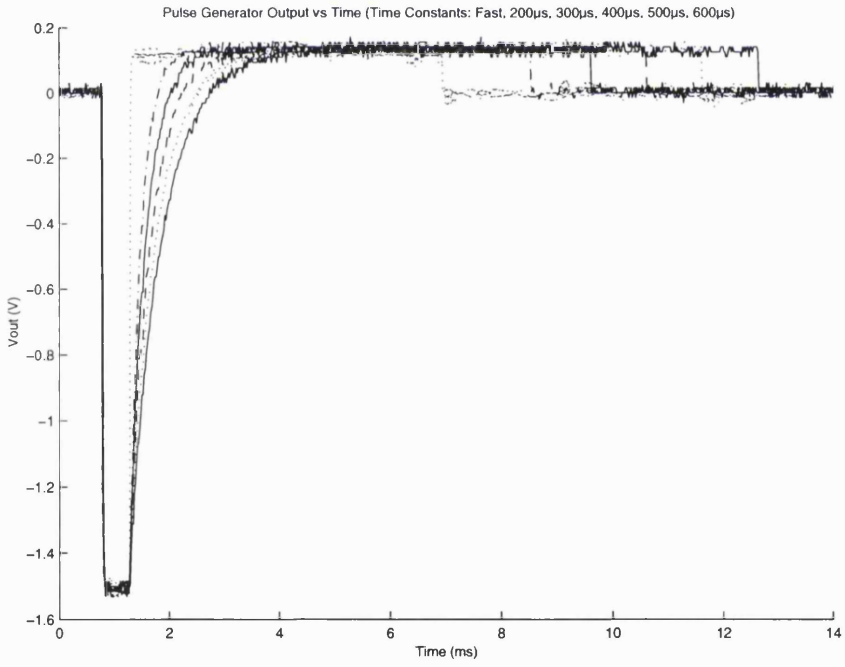

Figure 49. Pulse generator output showing various time constants

For time constants greater than 1ms, however, the output of the pulse generator circuit falls outside the specification due to either i) the rise time of the pulse becoming too large due to an excessively large capacitance having to be used, or ii) the amplitude of the reverse phase becoming smaller due to a very large tail resistance (several MΩ) which is necessary.

4.3.5.3 Rise Time

The 90% rise time for the pulse generator is shown in Table 19, the measurements show that for when using a tail capacitor of 680pF and below the rise time for the pulse generator meets the specified rise time. However, these measurements were taken by attaching a probe with a capacitance of 12pF-15pF to the output of the pulse generator (which itself is connected to an output pad increasing the capacitive load). In reality, the rise time observed when this node is connected internally to the attenuators inside an integrated circuit will be lower than the values shown in Table 19. Meaning a 1000pF tail capacitor could be used as long as the capacitive loading on the pulse generator output inside the IC is minimised (e.g. not connecting the output to a pad).

Table 19. Pulse generator experimental rise time with a RpCp set to 350µs[19]

Tail Capacitor (Cp)	Rise Time (90%)
100pF	2µs
220pF	3µs
470pF	5µs
680pF	7µs
1nF	9µs

4.3.5.4 Reverse Phase

The experimental value of the reverse voltage Ar is compared with the expected value in Table 20 (Af = 1V).

[19] Measured in 4 Integrated circuits

Table 20. Reverse voltage (Vneg) measurements for Af = 1V

Ar Theoretical Value (Af/X)		Ar Experimental Range, mean[20]	
1/6.66	(0.150Af)	1/6.7 –1/6.6	1/6.7
1/13.33	(0.075 Af)	1/13.3 – 1/13.4	1/13.4
1/20	(0.050 Af)	1/20 – 1/20.3	1/20.2
1/26.66	(0.0375 Af)	1/26.4 – 1/26.6	1/26.5
1/33.33	(0.03 Af)	1/32.8-1/33.1	1/32.9
1/40	(0.025 Af)	1/39.4- 1/39.8	1/39.6
1/46.66	(0.021 Af)	1/44.1 – 1/44.9	1/44.8

The results for the reverse phase Ar show that the reverse phase of the stimulation pulse can be set between 1/6.7 and 1/45, this agrees with the specification given for the pulse generator. The inaccuracy at higher attenuation levels is mainly due to the offset of the amplifiers, as this waveform is integrated to detect when the pulse is charge balanced, this is not significant. With the experimental results the reverse current to a 5mA pulse and smallest reverse phase would be 111µA, however at 4.5mA the reverse current is at the 100µA limit suggested as suitable by Fang and Mortimer [144]. However, this is not an absolute limit, but simply a recommended value, whether a 111µA reverse current is too large is not known from the published literature.

4.3.5.5 Pulse Generator Amplifier

The characteristics of the pulse generator amplifier (used as a buffer and a variable gain amplifier in Figure 44) are shown in Table 21, the experimental results indicate that all of the characteristics fell within of the simulated range. The offset voltages of the amplifier however showed a little experimental variation between devices. This may in part have been due to the fact that for this amplifier dummy transistors[21] were not used in the layout, this modification is recommended for future designs to keep the amplifier offset at low as possible.

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[20] Measured in 6 Integrated Circuits

[21] Dummy transistors are unused transistor that are placed next to active transistor edges to help remove variations that occur during processing [78].

Table 21. Characteristics of the pulse generator opamp

Parameter	Specification	Simulated Range		Experimental Range
DC Gain	72dB	75dB	89.9dB	83.1dB ± 0.7dB
Unity gain bandwidth (C_{load}=100pF)	1.0MHz	1.5MHz	2MHz	1.7MHz ± 0.2MHz
Input offset voltage	1.3mV	0.2mV	1.5mV	-1.3mV to +1.1mV
Slew Rate	2.0V/μs	+2.0V/μs -3.8V/μs	+3.6V/μs -4.6V/μs	+2.36 V/μs ± 0.26V/μs -4.55 V/μs ± 0.14V/μs
Output Swing Range	+2.0V -2.0V	+2.1V -2.6V	+3.2V -3.6V	+2.36V± 0.13V -3.02V± 0.21V

4.3.6 Discussion

The theoretical and experimental results for the pulse generator show that the developed circuit can produce waveforms of the shapes required for both anodal blocking and conventional stimulation. The reverse phase amplitude (Ar) can be defined accurately and although the voltage is more accurate for larger values of Ar the maximum deviation found at 1/47 of the plateau voltage (Af) was 5%. The stimulator requires 3-bits to define the reverse amplitude ratio (*A, B, C* shown in Figure 44) and one bit for the type of tail (*tail*). To generate the stimulation pulses two signals are required *pw* to define the plateau duration and *zero* to define when the stimulation pulse is to terminate. The specification for the pulse generator has been satisfied as shown in Table 22, which compares the specification and experimental results.

Table 22. Pulse generator specification and experimental results

Parameter	Specification	Experimental Result
Plateau Duration	16μs to 1ms in 4μs increments	> 5μs, externally defined by control signal *pw*
Plateau Amplitude (Af)	6mV to 1.5V in 6mV increments	Step Defined by DAC, Maximum Af is 3.0V
Reverse Phase (A_R)	1/6.7 to 1/47 (2% to 15%)of the pulse amplitude (Af) where: $A_R = \frac{A_f}{6.7n}$ where n = 1 to 7	1/6.6 to 1/44.8 (2.2% to 15%) of Af
Pulse Rise Time (90%)	< 8μs	< 8μs when Cp < 900pF
Pulse Tail	i) Exponential with time constant of 350μs (Variable after Integrated Circuit manufacture) ii) Fast decay of time constant <10μs	i) Tail defined by external resistor and capacitor, variable between 100μs and 1ms. ii) Fast decay of time constant <10μs

4.4 Attenuators

4.4.1 Introduction

The attenuator stages are required to take the output of the pulse generator and produce four attenuated versions to be used by the Voltage to Current Converters (Transconductors), which generate the stimulation currents. The easiest way to do this would have been to simply use four variable-gain amplifiers. However, after the design of the transconductor stage with a differential input, the attenuator stage had to be changed to include a differential output, this modification to the original specification is included in the specification given in 4.4.2.

4.4.2 Specification

Table 23. Attenuator specification

Parameter	Value
Variable Gain	0:1 – 1:1, 4-Bit precision
Output Voltage Swing	-2V to +2V
Output Polarity	Differential
DC Offset	< 1mV
Differential Offset	< 1mV

The specification for the attenuators is fairly simple with only four parameters; the variable gain specification comes from the main specification given in 3.9. The output swing range is defined by the specification for the pulse generator output. The Offset specification is to keep the DC offset in the transconductors minimised, the specified value of 1mV offset translates to a 3μA offset current after the transconductors. However, if the DC offset in each of the amplifiers is the same the actual current offset will be zero as the transconductors have a differential input. The maximum differential offset is defined as the same as the maximum DC offset (i.e. 1mV). The effect of offset matching is shown graphically in Figure 50.

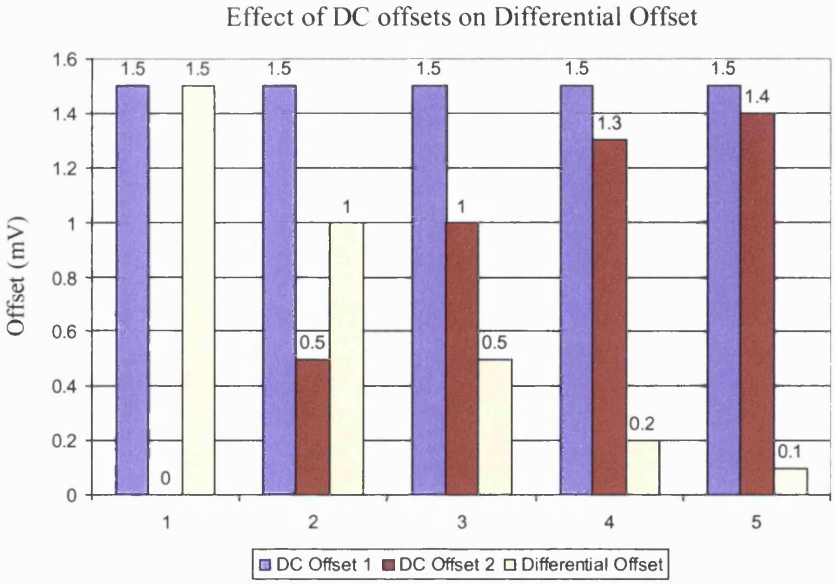

Figure 50. Effect of offset matching on the differential offset (5 examples shown)

4.4.3 Implementation

There are two standard methods to produce a differential output for the attenuator stage, one is to design a fully differential amplifier that takes the single sided output of the pulse generator and converts this to differential output. The second is to simply have two stages after the amplifier, one with variable a gain to attenuate the signal and a second stage to invert the attenuated signal.

The first method initially seems the best solution as only one stage is needed and the phase shift between the two output signals will be negligible. The problem with this method however turns out to be converting the signal from single-ended to differential and having a variable gain in the same stage. An example of a fully differential amplifier is shown in Figure 51 [6,9].

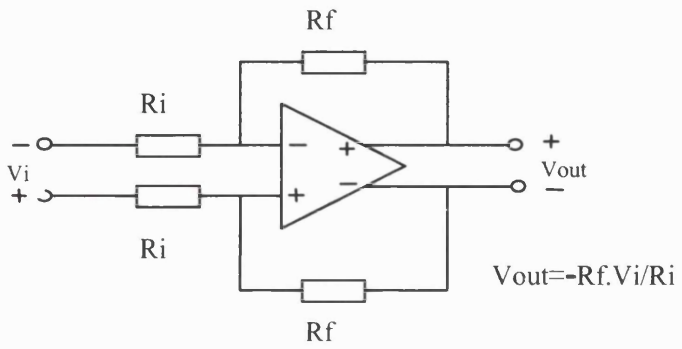

Figure 51. Fully differential attenuator

To convert from single-sided to differential, one of the inputs can be connected to ground. To implement a variable gain both Ri's or both Rf's have to be made variable, this has a number of disadvantages over a single sided implementation, and these are.

i) The number of resistors and switches is doubled.

ii) Matching of the components has to be accurate to avoid errors in the differential output voltage.

The complexity of an attenuator based on a single sided amplifier is much less than a fully differential implementation. The attenuator can be made having a structure identical to a voltage scaling DAC, attached to the output of the pulse generator stage. This produces a positive attenuated version of the signal. An inverting amplifier at the output of the variable gain stage will produce the negative version. A 2-bit example of this implementation is shown in Figure 52.

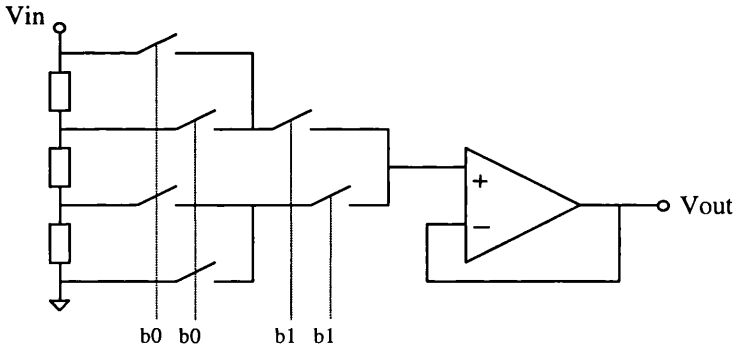

Figure 52. 2-bit voltage scaling DAC acting as an attenuator

For our design, we need a 4-bit attenuator based on the scheme of Figure 52. However, we need only one chain of resistors for all four of our attenuators, as we can have multiple sets of switches. This is useful because accurately matched resistors take up large areas of silicon. The second advantage of this method is that when two channels are set to the same attenuation setting they should have identical outputs.

Each switch was made using an n-channel FET (W/L = 6μm/6μm), the on resistance of each switch is approximately 4.5kΩ. Each 4-bit switching array requires 30 n-channel transistors.

The whole attenuator is shown in Figure 53.

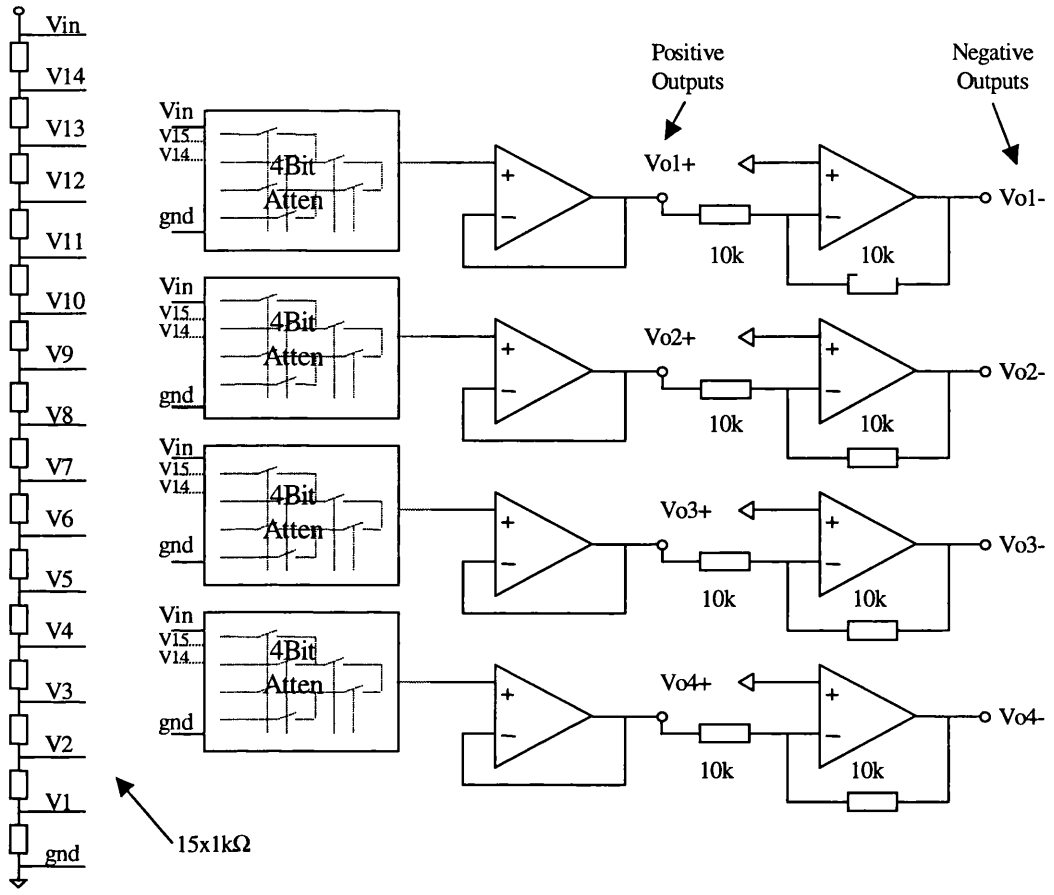

Figure 53. 4-channel, 4-bit single- sided to fully-differential attenuator

For the attenuator design, the value of each resistor in the chain was set at approximately 1kΩ, and the feedback resistors in the inverting amplifier were specified arbitrarily as 10kΩ. For the first implementation, it was decided to use an amplifier similar to the amplifier used in the pulse generator. The advantage of this amplifier is that it is capable of driving resistive loads for the feedback on the negative channel, and can be connected to output pads for driving off chip loads during testing. In a final stimulator device, this may not be ideal (lower power, larger output swing and lower offset amplifiers may be preferred), however the design of the attenuator stage allows the simple replacement of the amplifiers with no other modifications to the stage. The amplifier used is shown in Figure 54 and has the same characteristics as discussed for the pulse generator amplifier in 4.2.3.1. As both the amplifiers need approximately the same characteristics (except the attenuator amplifier is not required to drive capacitive loads of 1nF), the specification given in 4.2.3.1 was used.

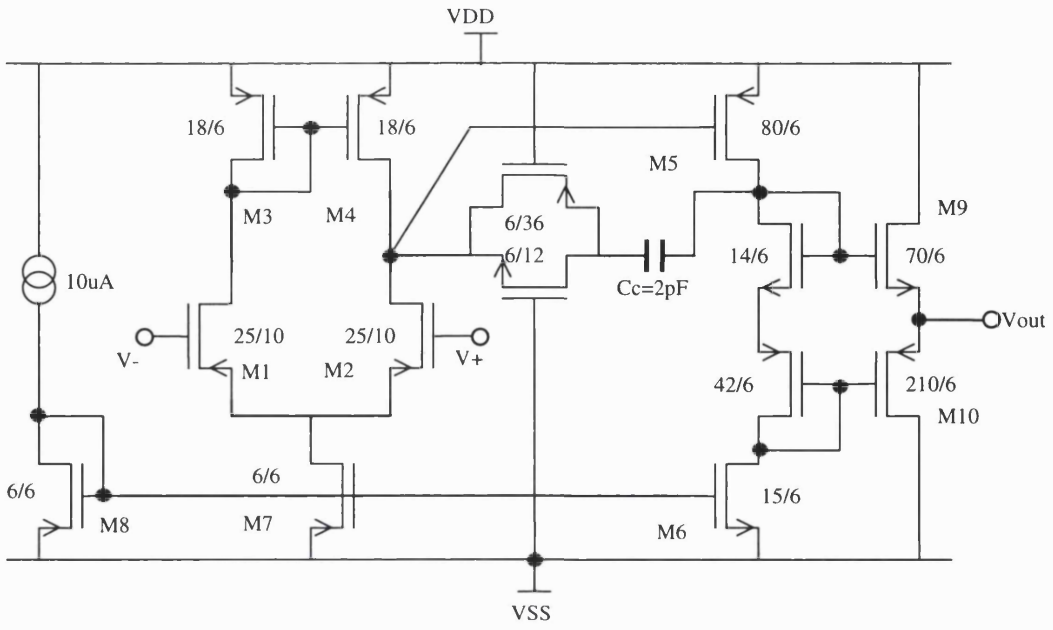

Figure 54. Attenuator amplifier

The attenuators requires 120 6µm/6µm n-channel switching FETs, 16 1kΩ resistors (matched), 8 op-amps and 8 10kΩ resistors. This was felt to be a reasonable number of components to integrate and is far fewer than would be required by the fully differential method discussed.

Table 24. Attenuator: Components and areas occupied

Device	Number required	No of transistors per device	Area per device (mm^2)
Amplifier	8	14	0.065
4-bit attenuator	4	30	0.026
1kΩ resistor	16[22,23]	0	0.024
10kΩ resistor	8	0	0.014
Total	28	232	1.664

Using the same areas per device as shown in Table 24, the fully differential implementation would require 4 amplifiers, 8 4-bit attenuators, 32 switching resistors

[22] Including area occupied by dummy resistors.

[23] Dummy resistors are placed at the boundary edges of polysilicon resistors to remove the effect of boundary dependant over etching. In effect every resistor sees the same boundary conditions improving the matching of the resistors[78].

(1kΩ) and 8 feedback resistors (10kΩ), occupying a minimum physical area of 1.816mm^2. Allowing 0.5mm^2 for interconnection (approximately the same as for the implemented attenuators) gives a total estimated area of 2.316mm^2 for the fully differential implementation (40% larger than the implemented attenuator stage).

4.4.4 Simulation Results

Table 25 shows a comparison between the specification and the simulated behaviour of the attenuator. The simulated characteristics all fall within the specification given in 4.4.2.

Table 25. Simulated characteristics compared to specification

Parameter	Specification	Simulated Range
Output Voltage Swing	-2V to +2V	-2.66V to -3.61V +2.05V to +3.17V
DC Offset	< 1mV	0.3mV – 1.0mV
Differential Offset	< 1mV	0.0mV – 0.6mV

4.4.5 Experimental Results

Figure 55 shows the experimental behaviour of the attenuators using a reference signal produced by the pulse generator and variable defined gains for each output channel. The testing showed that the attenuators behaved as expected producing positive and negative attenuated versions of the input signal. The maximum absolute deviation from linearity for the attenuator was found to be 0.15% (0.024LSB), meaning that the error introduced by the attenuators is small.

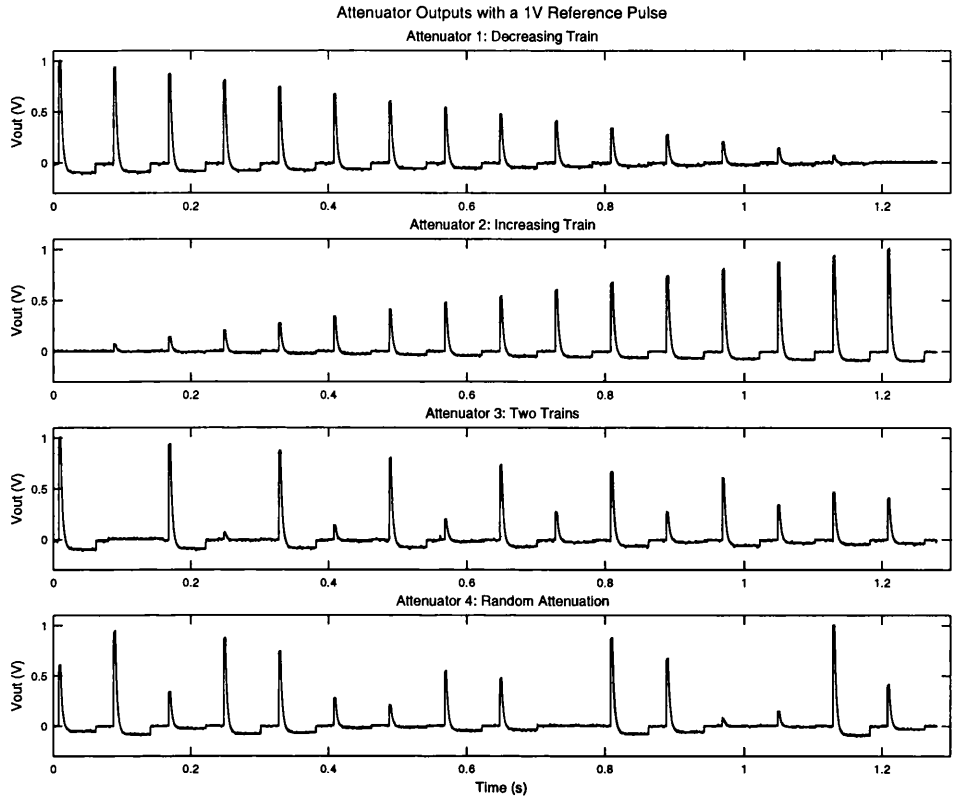

Figure 55. Attenuator negative outputs for a fixed reference signal from the pulse generator (various gains)

Figure 56 shows differential error voltage observed at the attenuator outputs for a 1V DC reference voltage over the attenuation range.

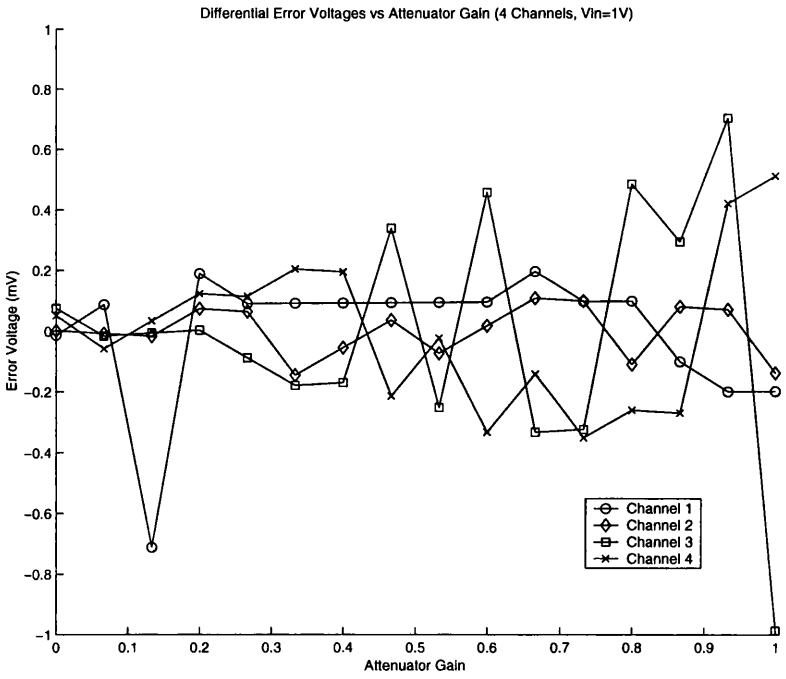

Figure 56. Differential offset error voltage vs attenuator gain (4 channels, Vin = 1V, IC 4)

Figure 56 shows the maximum differential offset error in output voltages on this IC is just below 1mV. However, across all ten Integrated Circuits tested the maximum differential offset error was found to be 1.3mV, which exceeds the maximum offset allowed in the specification.

Table 26. Attenuator simulated and experimental characteristics compared to specification

Parameter	Specification	Simulated Range	Experimental Range
Output Voltage Swing	-2V to +2V	-2.66V to -3.61V +2.05V to +3.17V	+2.28V ± 0.2V -3.06V ± 0.3V
DC Offset	< 1mV	0.3mV – 1.0mV	1mV ± 4mV
Differential Offset	< 1mV	0.0mV – 0.6mV	0.1mV – 1.3mV

The experimental and simulated characteristics of the attenuator amplifier are compared in Table 27. The offset for the amplifier was found to be greater than the simulated range as discussed previously. The other amplifier characteristics all lie within the simulated range.

Table 27. Attenuator amplifiersimulated and experimental characteristics

Parameter	Simulated Range	Experimental Range
DC Gain	81.6dB – 91.0dB	84.2dB
Input offset voltage	0.4mV – 1.0mV	1mV ± 4mV
Slew Rate	+2V/µs to +3.4V/µs -3.4V/µs to -4.25V/µs	+3.8V/µs -4.9V/µs
Output Swing Range	-2.66V to -3.61V +2.05V to +3.17V	+2.28V -3.06V
Unity gain bandwidth	2MHz -2.7MHz	2.2MHz

4.4.6 Discussion

The simulated and experimental results show that the proposed design almost meets the specification given in 4.4.2, with the notable exception of the output offsets, which showed a greater variation than expected. This offset variation was probable due to poor layout of the input stage of the amplifiers without dummy transistors[24].

[24] For the same reasons as described for dummy resistors, dummy transistors improve device matching.

The main source of error in the attenuators was the offset introduced by the amplifiers. This was the only amplifier layout in the stimulator not to use dummy transistors and the amplifier input offset observed was the highest of all the amplifiers. This leads to the conclusion that all of the amplifiers should use dummy transistors on the amplifier input transistors to reduce offset. The use of dummy transistors should allow the specification to be met fully, which the current implementation does not due to the amplifier offsets. The DC offset in the amplifiers showed a fairly large variation, however the differential offset for pairs of amplifiers was lower than the DC offset meaning the actual offset observed in the output current is lower than suggested looking at the DC offset for each amplifier individually.

The other simulated and experimental characteristics demonstrated that the attenuators perform the required function of generating four differential attenuated versions of the output of the pulse generator.

4.5 Linear Transconductor (Voltage to Current Converter)

4.5.1 Introduction

Voltages to current devices are known as Transconductors (VCT).

Many linear transconductors suitable for integration have been described in the literature [76,77,94,95,99,100,109,124,128,139]. Most VCT circuits are not suitable for this application because they are not capable of functioning over the range of current amplitude and load impedance required (up to 5mA into 1kΩ), due to the power supply limitation of ≤12V while maintaining adequate linearity. Most VCTs in the literature are proposed for transconductance-C filters, where the output current is typically much lower (typically below 100μA [139]) and therefore the voltage limitation problem is not present. The 5mA is a problem because of the technology used in this design has a maximum supply rail of 12V and as 5mA into 1kΩ will drop 5V, +/- 5mA will drop 10V leaving only 2V for the output transistors. Technologies are now available capable of functioning up to 50V [IMEC web site[25]], however the cost using these technologies was prohibitive during this project. From the general specification for the stimulator in chapter 3 the specification for the transconductor was developed:

4.5.2 Specification

Table 28.Linear transconductor specification

Parameter	Range
Output Current	-5mA to 5mA
Load Impedance	300Ω to 3kΩ
Maximum Absolute Deviation (Iout=4mA)	≤ 5%
DC Output Offset	≤ 3μA
Quiescent Current	≤ 1mA
Power Supply	±5V (set by process limits)

The range of the Load impedances comes from the maximum expected range of impedances expected for nerve cuffs while using this stimulator, this has being

[25]http://www.imec.be

determined experimentally and is detailed in Appendix 3. The maximum absolute deviation in output current comes from the maximum error the switching array is expected to remove at the end of the stimulation pulse (discussed in 3.4.5).

4.5.3 Background

Single sided transconductors typically have an inherent offset; one method for cancelling offset is to use a differential output stage where the offsets of each output side cancel each other out. Most papers that describe this type of transconductor have a bias current equal to double the maximum output current [76,139], this is clearly not feasible when the required output current is so high (for four 5mA output channels a bias current of 40mA would be required!). This section describes some previously reported single sided and differential transconductors. Figure 57 shows several possible transconductor implementations that could be adapted for use with this stimulator. Figure 57a shows a Common-source differential pair [78], the differential output current (Iout) is defined by:

$$Iout = I1 - I2 = \frac{k_p W_p}{2L_p}(V_1 - V_2)(V_1 + V_2 - 2V_C - 2V_{tn}) \tag{4.3}$$

This circuit and Figure 57b [78] and Figure 57c [128] require a active loads to provide a current pathway to the power supply, this can be implemented using a current mirror or similar circuit. Equation 4.3 shows that the Common Source differential pair output current has a non-linear term proportional to V_1^2 and V_2^2, which, coupled with a bias current of Iout(maximum), make this circuit unsuitable as a linear transconductor. Figure 57c and Figure 57d implement linear transconductors based on differential pair implementations. The circuits both linearise the output currents removing the Vin^2 terms, however the bias current required for both circuits is of the same order of magnitude as the maximum output current, making the circuits unsuitable in this application. The quoted distortions of Figure 57c and Figure 57d are both below 1% (in fact the error in Figure 57c is typically below 0.5%, depending on the bias conditions). A single sided transconductor based on an inverter is shown in Figure 57b [94], the output current for the inverter is given by[26]:

$$I_{OUT} = I\alpha - I\beta = K_p\left(V_{DD} - V_{IN} - |V_{tp}|\right)^2 - K_n(V_{IN} - V_{SS} - V_{tn})^2 \tag{4.4}$$

[26] Where K_p, K_n are defined on the next page

Where $K_p = \frac{k_p W_p}{2L_p}$ and $K_n = \frac{k_n W_n}{2L_n}$ (definition used for the rest of this section)

Equation 4.4 has a non-linear term is equal to $(K_p\text{-}K_n)Vin^2$, the inverter also contains an offset term dependant on mismatches between the threshold voltages, K_p / K_n and the power supply voltages [99]. The input range of the inverter can be increased using a DC voltage (V_G) placed between Vin and the gates of the transistors [61]. This has the same effect as increasing the threshold voltages in equation 4.4 by V_G, expanding the input voltage range of the transconductor.

Park and Schumann [99,100] proposed a scheme to remove the offset from the simple inverter transconductor described, by using the circuit shown in Figure 57e. This circuit works by using V_{G4} to zero the offset and V_{G1} to vary the transconductance (to a degree). This circuit also increases the PSRR (Power Supply Rejection Ratio) of the transconductor. The residual problem with this circuit is the limited output swing caused by the need to keep M1 and M4 in saturation. The body effect of transistors M1 and M4[27] increases the minimum V_{DS}, allowed for both devices to remain in saturation, and so reduces the available output voltage swing, making this implementation unsuitable for this application. This circuit demonstrates a non-linearity error of approximately 1% for a Vin of 1V. The output current of this transconductor is given by:

$$I_{OUT} = -2K_{eff}(V_{G1} + V_{G4} - \Sigma V_T) + K_{eff}(V_{G1} + V_{G4} - \Sigma V_T)\Sigma V_T \qquad (4.5)$$

Where $K_{eff} = K_n K_p / (\sqrt{K_n} + \sqrt{K_p})^2$, $\Sigma V_T = Vtn1 + Vtn3 + |Vtp2| + |Vtp4|$ and

$\Delta V_T = (Vtn1 - Vtn3) + (|Vtp2| - |Vtp4|)$

Another way to remove the inverter offset is to employ two identical versions of the simple inverter circuit connected differentially. This doubles the effective output voltage swing. A common-mode feedback path must be added to the circuit to bias the circuit correctly in operation. One implementation of this is shown in Figure 57f [94]. The feedback is implemented using simple inverter circuits to define the common mode output voltage. This circuit also has the problem that that channel length modulation[28] effects cause non-linearity of the output current. A transconductor based on this

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[27] The threshold voltage (Vt) is somewhat dependent on the bulk-source voltage (V_{BS}). The bulk-channel voltage affects the carriers in the depletion region under the gate (by forming a virtual gate). This in turn affects the voltage needed to form an inversion layer [61] and is known as the body effect.

[28] The drain current in the saturation region increases in an approximately linear manner with V_{DS}. This is due to a slight shortening of the effective length of the channel, as V_{DS} is increased [61]. λ is defined as the coefficient linking I_{DS} with V_{DS}.

implementation was chosen for this application, due to the possibility of keeping the quiescent bias currents reasonable.

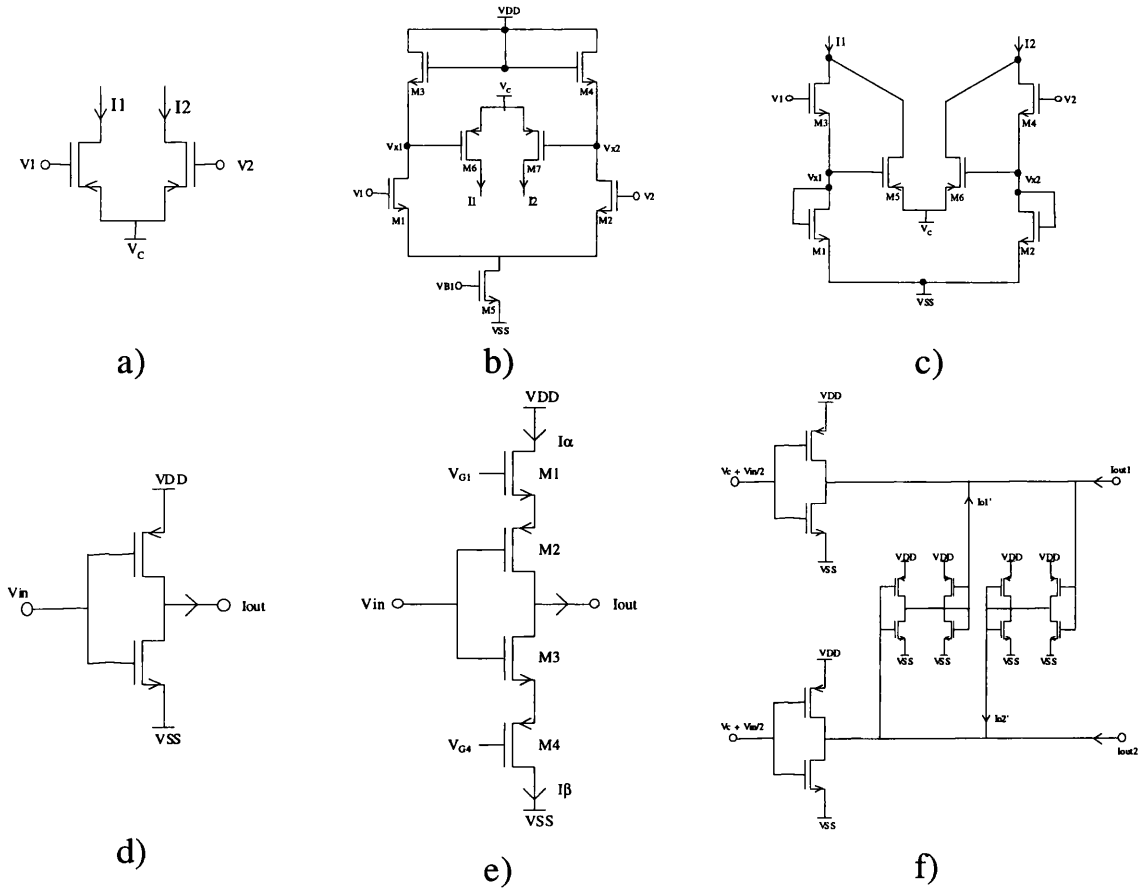


Figure 57. Transconductor circuits

4.5.4 Implementation: Single Sided Transconductor

From the circuit discussed the inverter / differential inverter has the characteristics best suited to meet the specification. A circuit is presented in the following section that uses a development of the simple inverter circuit to implement a linear transconductor with adjustable transconductance, low offset and low bias currents.

As stated in 4.5.3, the input range of the simple inverter transconductor can be increased by placing a DC voltage between Vin and the gates of the two transistors as shown in Figure 57d. The circuit however suffers from channel-length modulation effects causing non-linearity. This effect can be reduced by either cascoding the output transistors [61], or increasing the length of the transistors, however the substantial increase in transistor size makes the option of increasing the channel lengths unfeasible. An inverting transconductor with cascoded output transistors is shown in Figure 58

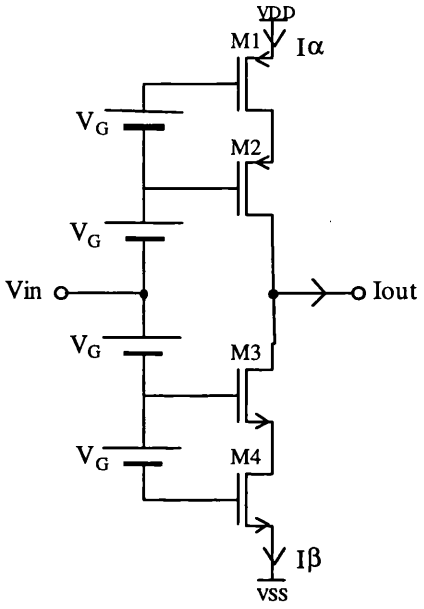


Figure 58. Proposed linear transconductor

This circuit suffers from a reduced output swing range due to the effect of having two transistors in series. However, the reduction in output swing is much lower than in the Park and Schumann circuit as the body effect is not as significant. By using this circuit in a differential configuration, as shown in Figure 57f, the effective output range can be doubled and the offset removed. The single-sided linear output range of this transconductor is approximately:

$$V_{DD} - |V_{tp1}| - |V_{tp2}| \geq V_{OUT} \geq V_{SS} + |V_{tn3}| + |V_{tn4}| \tag{4.6}$$

Where $V_{tp1\text{-}2}$ and $V_{tn1\text{-}2}$ are the threshold voltages for transistors M1 to M4 respectively.

Including the body effect the output range becomes +2.9V to -2.7V (for the Mietec 2.4µm process). Differentially this becomes approximately ± 5.4V. Meeting the specification for 5mA into a 1KΩ load, although this will depend on the actual threshold voltages for the processed devices.

The single-sided proposed transconductor circuit is shown in Figure 59a and the equivalent circuit is shown in Figure 59b.

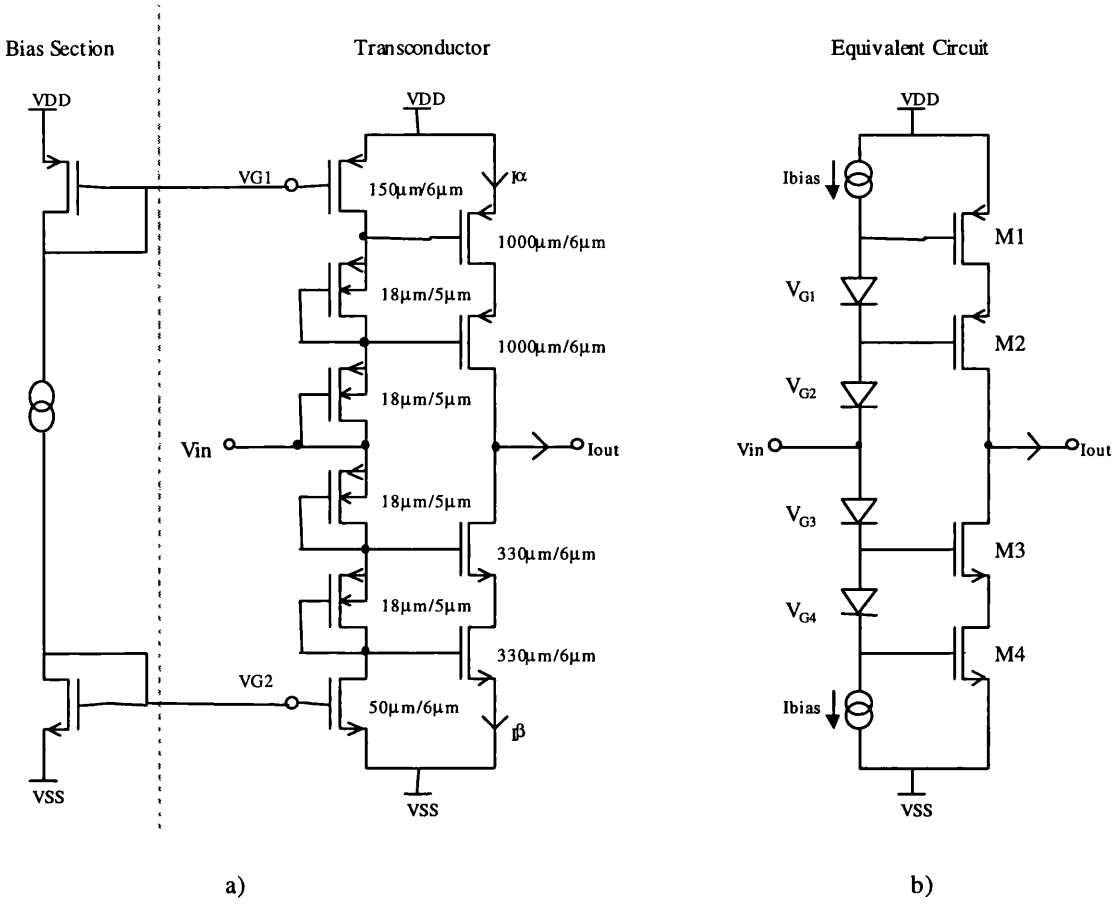


Figure 59. a) Proposed linear transconductor b) Equivalent circuit

The transconductor realises the floating voltage sources (V_G) using diode connected p channel FETs (each with their body tied to their sources to avoid the body effect). The actual value of V_G is controllable by changing the bias current, this allow the transconductance to be varied using the bias voltages VG1 and VG2. M1-M2 and M3-M4 are ratioed to keep equation 4.6 valid (ie: $K_n = K_p$) and the sizes of the output FETs were chosen to give a transconductance of approximately 3.5mA/V in simulation, setting the required maximum input voltage to 1.4V (for 5mA).

4.5.5 Analysis of Single Sided Transconductor

In this section, all of the results presented assume the device sizes and bias conditions the same described in 4.5.6 for the realised transconductor, assuming a transconductance of 3.5mA/V and a bias current of 15µA.

The output current (I_{OUT}) of the transconductor shown in Figure 58 is:

$$I_{OUT} = I\alpha - I\beta \tag{4.7}$$

Using the FET equations defined in Appendix 3.

$$I\alpha = \frac{k_p W_p}{2L_p}\left(V_{DD} - V_{IN} - |V_{tp}|\right)^2 \tag{4.8}$$

$$I\beta = \frac{k_n W_n}{2L_n}\left(V_{IN} - V_{SS} - V_{tn}\right)^2 \tag{4.9}$$

Substituting (4.8) and (4.9) in (4.7) and substituting $K_p = \frac{k_p W_p}{2L_p}$ and $K_n = \frac{k_n W_n}{2L_n}$

$$I_{OUT} = I\alpha - I\beta = K_p\left(V_{DD} - V_{IN} - |V_{tp}| - 2V_G\right)^2 - K_n\left(V_{IN} - V_{SS} - V_{tn} - 2V_G\right)^2 \tag{4.10}$$

Assuming that $K_n = K_p = K$ and $V_{DD} = -V_{SS}$

$$I_{OUT} = -2KV_{IN}(2V_{DD} - V_{tn} - |V_{tp}| - 4V_G) + K[V_{tp}^2 - V_{tn}^2 + 4|V_{tp}|V_G - 4V_{tn}V_G + 2V_{DD}(V_{tn} - |V_{tp}|)] \tag{4.11}$$

Therefore, we can see from 4.11 that the circuit behaves as a linear transconductor. When the parameters K_n, K_p, and supply voltages V_{SS}, V_{DD} are matched, we can say:

$$I_{OUT} \propto V_{IN} + offset \tag{4.12}$$

If $V_{tn} = |V_{tp}|$ then the offset of the transconductor will be zero and an ideal transconductor is realised. If the parameters are not matched then 4.6 can be rewritten as:

$$\begin{aligned} I_{OUT} = (K_p - K_n)V_{IN}^2 - 2V_{IN}(K_p(V_{DD} - |V_{tp}| - 2V_G) - K_n(V_{SS} + V_{tn} + 2V_G)) \\ + (K_p(V_{DD} - |V_{tp}| - 2V_G)^2 - K_n(-V_{SS} - V_{tn} - 2V_G)^2) \end{aligned} \tag{4.13}$$

Equation 4.13 shows that this transconductor has a non-linear term relating to mismatch in K_p and K_n.

4.5.5.1 Offset

From equation 4.13 the offset of the transconductor is given by:

$$I_{OFFSET} = K_p(V_{DD} - |V_{tp}| - 2V_G)^2 - K_n(-V_{ss} - V_{tn} - 2V_G)^2 \tag{4.14}$$

The offset depends on the parameters V_{tp}, V_{tn}, K_p and K_n and power supplies V_{SS} and V_{DD}, the effect of each is considered in turn in this section.

4.5.5.1.1 Effect of V_{tn} / V_{tp} mismatch on offset

By substituting $V_{tn}= V_t$ and $|V_{tp}| = (1+\alpha)V_t$ in 4.14 the effect of mismatches in V_{tn} and $|V_{tp}|$ can be shown. The offset of the transconductor is:

$$I_{OFFSET} = K_p V_t^2 \alpha^2 - 2K_p V_t (V_{DD} - V_t - 2V_G)\alpha + K_p (V_{DD} - V_t - 2V_G)^2 - K_n (-V_{ss} - V_t - 2V_G)^2 \quad (4.15)$$

Assuming $V_{SS} = -V_{DD}$ and $K_p = K_n = K$ then 4.15 simplifies to:

$$I_{OFFSET} = KV_{tn}^2 \alpha^2 - 2KV_t (V_{DD} - V_t - 2V_G)\alpha \quad (4.16)$$

The effect of mismatches in V_{tn}/V_{tp} is shown in Figure 60. The results show that a 10% variation in V_{tn} to $|V_{tp}|$ causes almost 400μA offset.

4.5.5.1.2 Effect of Kn / Kp mismatch on offset

By substituting $K_n= K$ and $K_p = (1+\alpha)K$ in 4.14 the effect of mismatches in K_n and K_p is given by:

$$I_{OFFSET} = K(V_{DD} - V_{tp} - 2V_G)^2 \alpha + K((V_{DD} - V_{tp} - 2V_G)^2 - (-V_{SS} - V_{tn} - 2V_G)^2) \quad (4.17)$$

Assuming $V_{SS} = -V_{DD}$ and $K_p = K_n = K$ and $V_{tn}= |V_{tp}| = V_t$ then 4.17 simplifies to:

$$I_{OFFSET} = KV_{DD}(V_{DD} - V_t - 2V_G)^2 \alpha \quad (4.18)$$

The effect of Kn/Kp on the offset is linear. The effect of mismatches in K_n/K_p is shown in Figure 60. The figure shows that a 10% variation in K_n to K_p causes almost 200μA offset.

4.5.5.1.3 Effect of V_{DD} / V_{SS} mismatch on offset

By substituting $V_{SS} = -(1+\alpha)V_{DD}$ in 4.14 and assuming $V_{tn} = |V_{tp}| = V_t$, $K_n = K_p = K$ the effect of mismatches in V_{DD} and V_{SS} is given by:

$$I_{OFFSET} = KV_{DD}^2 \alpha^2 - 2KV_{DD}(V_{DD} - V_t - 2V_G)\alpha \quad (4.19)$$

The effect of mismatches in V_{DD} / V_{SS} is shown in Figure 60 (a 20% change in V_{DD} is equivalent to a 1V change). The figure shows that a 0.5V (10%) power supply mismatch causes almost 400 μA offset. This equation is a quadratic, so the effect of power supply variation on the offset contains a second order term.

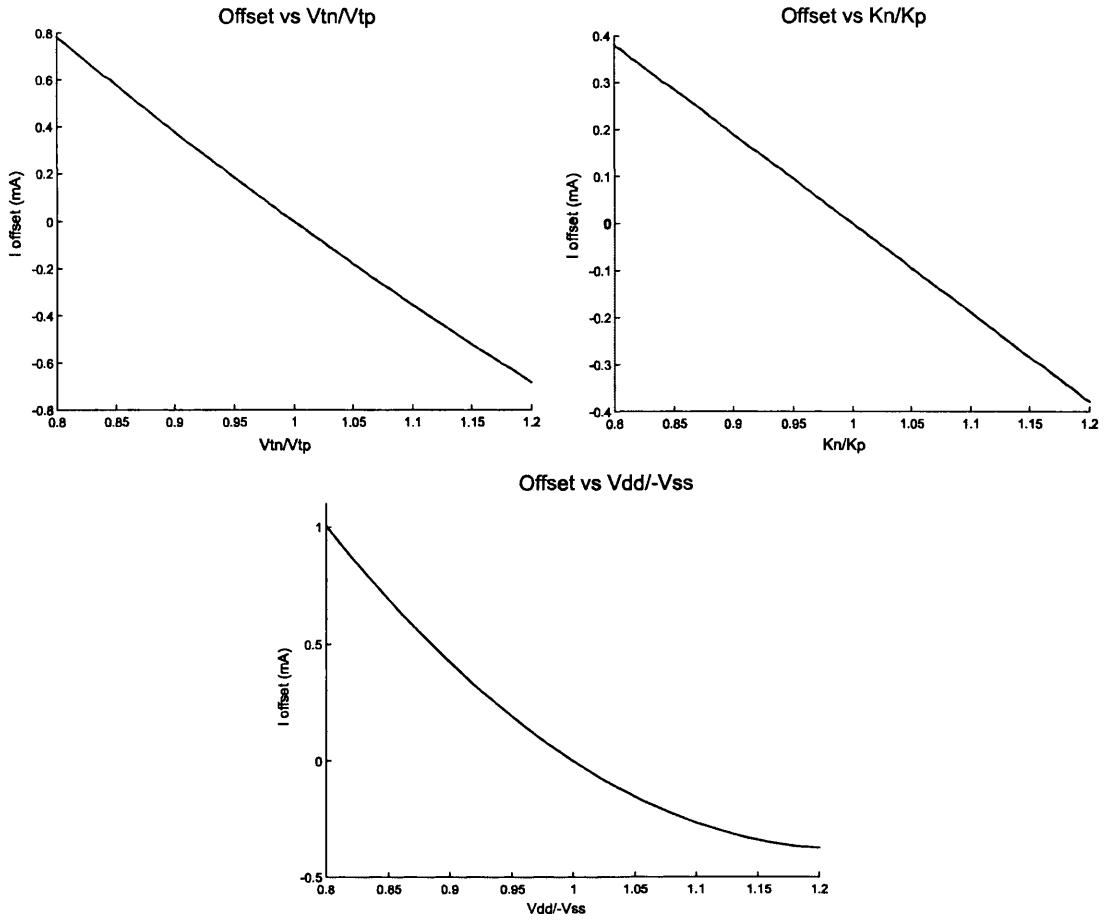


Figure 60. Effect of mismatches on transconductor DC offset

From this analysis, we can see that this circuit requires some method of removing the DC offset from the transconductor, using the circuit differentially with common-mode feedback will perform this function.

4.5.5.2 Linearity

The only non-linear term with respect to V_{IN} (in 4.13) is $((K_p - K_n))V_{IN}^2$. The non-linearity error can be expressed in terms of the output current as:

$$Error\ (\%) = 100 \times (I_{OUT} - I_{Linear}) / I_{Linear} \tag{4.20}$$

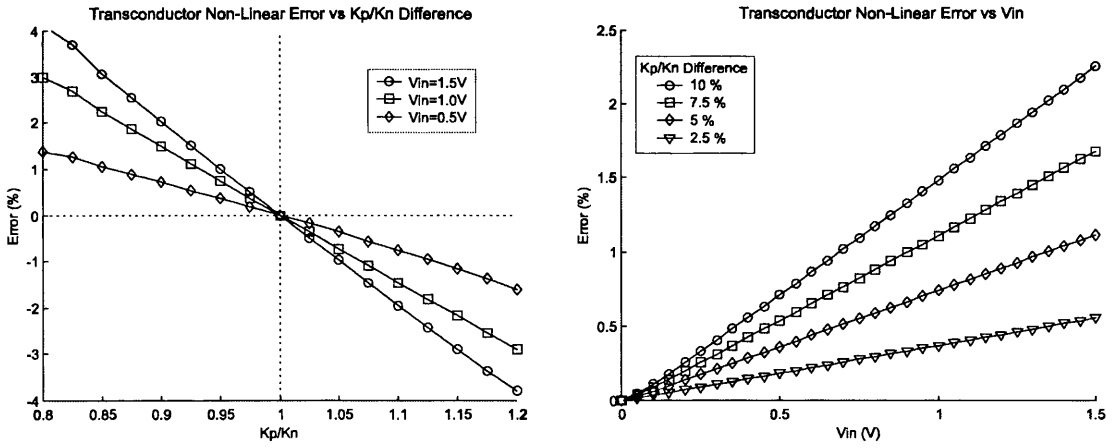
Where I_{OUT} is defined in 4.12 and I_{Linear} is the V_{IN} and offset terms of 4.13. Substituting the relevant terms in 4.20 gives the error as:

$$Error\ (\%) = 100 \times \frac{(K_p - K_n)^2 V_{IN}^2}{\left(\begin{array}{l} -2V_{IN}(K_p(V_{DD} - |V_{tp}| - 2V_G) - K_n(V_{SS} + V_{tn} + 2V_G)) \\ +(K_p(V_{DD} - |V_{tp}| - 2V_G)^2 - K_n(-V_{SS} - V_{tn} - 2V_G)^2) \end{array} \right)} \tag{4.21}$$

Assuming V_{DD}=-V_{SS} and V_t=V_{tn}=|V_{tp}| equation 4.20 simplifies to:

$$Error\ (\%) = 100 \times \frac{(K_p - K_n)^2 V_{IN}^{\ 2}}{\left(\begin{array}{r} -2V_{IN}(K_p(V_{DD} - |V_{tp}| - 2V_G) - K_n(-V_{DD} + V_t + 2V_G)) \\ +(K_p - K_n)(V_{DD} - V_t - 2V_G)^2 \end{array}\right)} \qquad (4.21)$$

Figure 61 shows the calculated non-linearity for the transconductor for various Kn/Kp ratios and the effect of Vin on the non-linearity. The graphs show that for a 10% process variation in Kp relative to Kn a 1.5% error is present in the output current. From the Mietec process parameters, this is likely to be close to the worst-case situation (The worst case variation according to the process parameters is approximately a 11-12% variation). Using this data, the realised transconductor will have a maximum non-linearity error of approximately 2% for a 5mA stimulation pulse. This is within the specification given in 4.5.2.



a) b)

Figure 61. Transconductor non-linearity vs a) Kp/Kn, b) Vin

4.5.6 Implementation: Differential Transconductor

4.5.6.1 Connection of Outputs to Electrodes

An overview of how the realised transconductor is connected is shown in Figure 62 for the stimulator operating in pentapolar mode. The circuit has four differential inputs ±A, ±B, ±C, ±D each connected to one transconductor stage and eight outputs. On one side all the outputs have been connected together, to define the common anodal current (for the pentapole) and the opposing transconductors supply the current for each separate cathode.

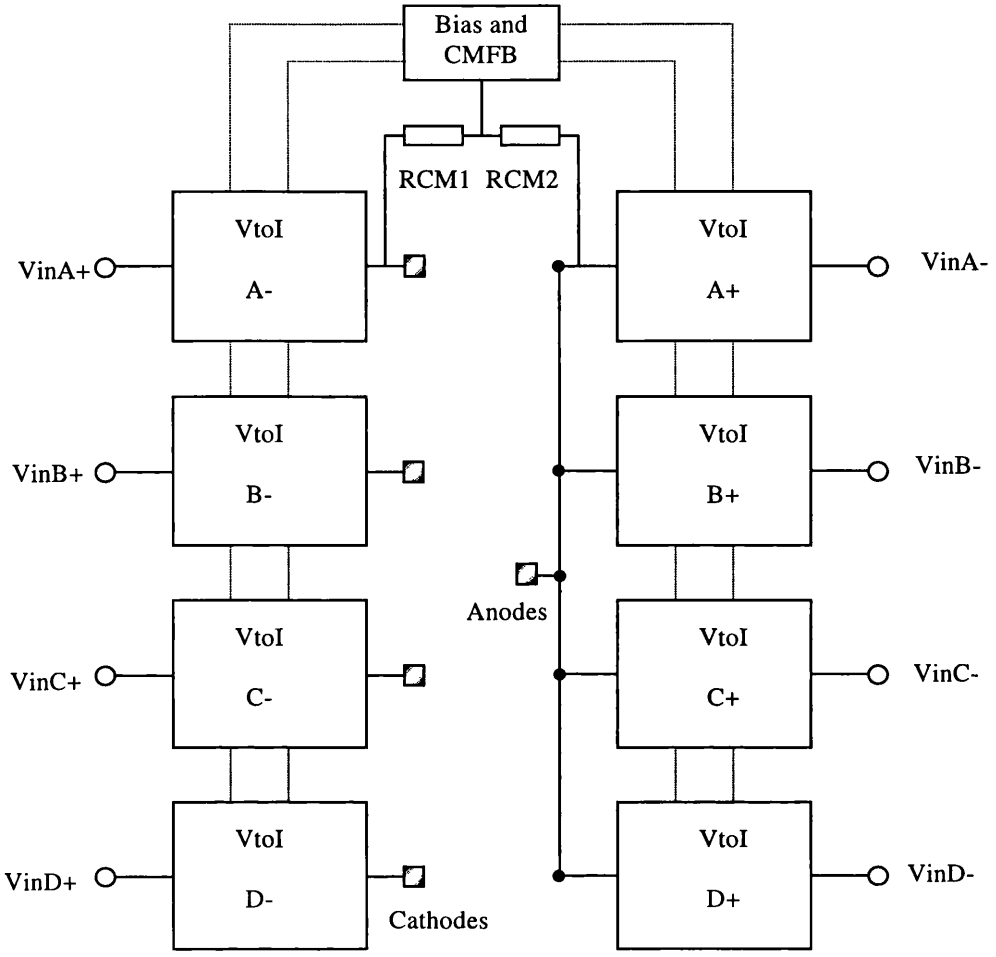


Figure 62. Connection of the transconductors and common mode feedback to the pentapolar electrode

4.5.6.2 Common-Mode Feedback

As mentioned, differential transconductors require common mode feedback to operate in the desired region. The approach chosen was the simplest method shown in Figure 63. Later this could be replaced by a more complex system that does not require an extra resistive load (R_{CM1}, R_{CM2}) to be connected to one pair of the outputs [54,156], such as the implementation shown in Figure 57f. This feedback is applied to the biasing mirrors for the diode-connected FETs in the circuit that act as floating voltage sources. The simulated results showed that this feedback system is suitable for all the expected modes of operation (dipolar, tripolar and pentapolar). The operation of the circuit is as follows. If the common mode voltage is not in the range V1 + Vtp > Vcm > -V1 + Vtn then either M1 or M2 will start to turn on and resulting drain current will cause the voltages in the bias chain to move the common mode voltage towards this condition.

V1 is chosen to keep Vcm close to zero, this is accomplished by setting V1 close to Vtn (or Vtp).

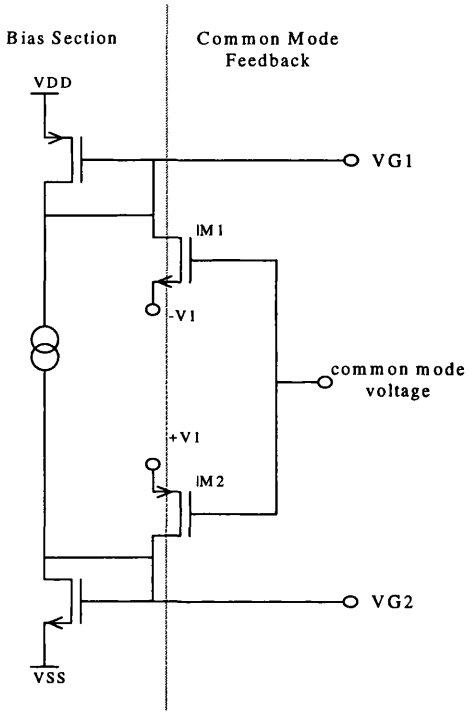


Figure 63. Common mode feedback for the differential transconductor

4.5.7 Simulation Results

The test configuration for the simulated transconductor, operating differentially (in dipolar mode), is shown in Figure 64: the response of the transconductor shown in Figure 65. The behaviour of the output voltage on the positive output for dipolar operation is shown in Figure 66. The quiescent current[29] for the transconductors was 580μA with a bias current of 15μA.

[29] As measured for Vin1=Vin2=0V

These figures show the operation of the transconductor and its linear region. Table 29 shows the simulated output range for several Maximum Absolute Deviations.

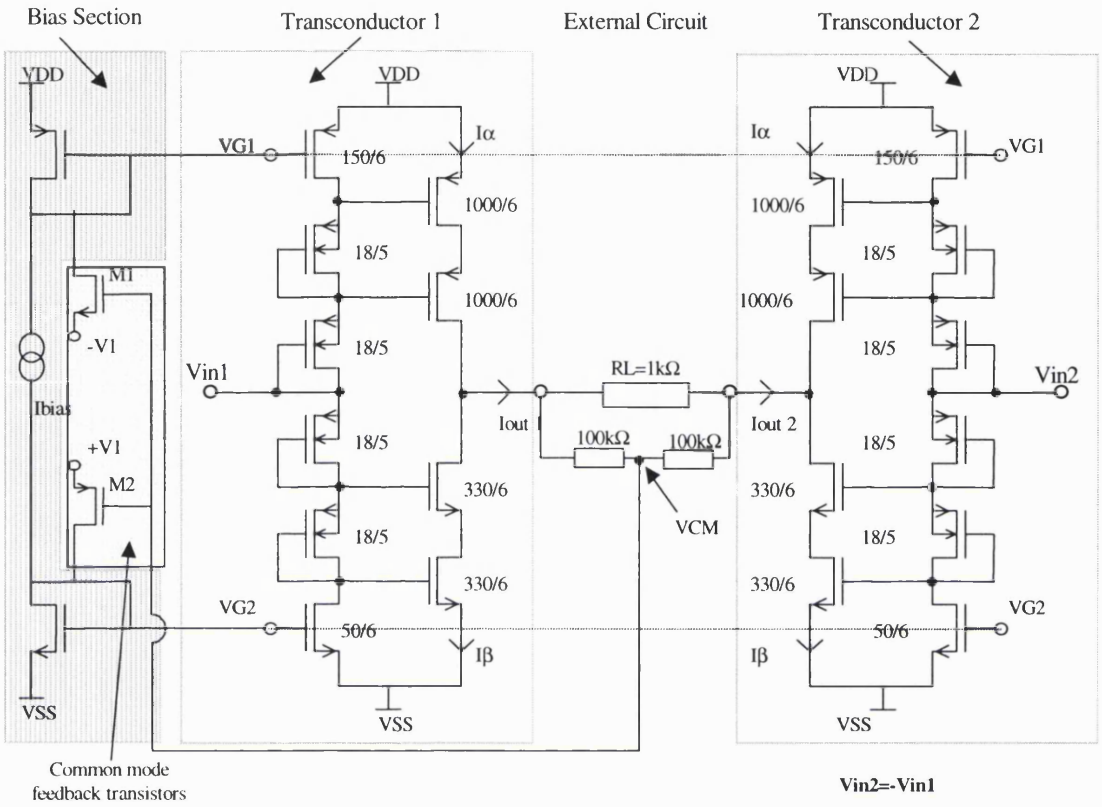


Figure 64. Differentially connected transconductor

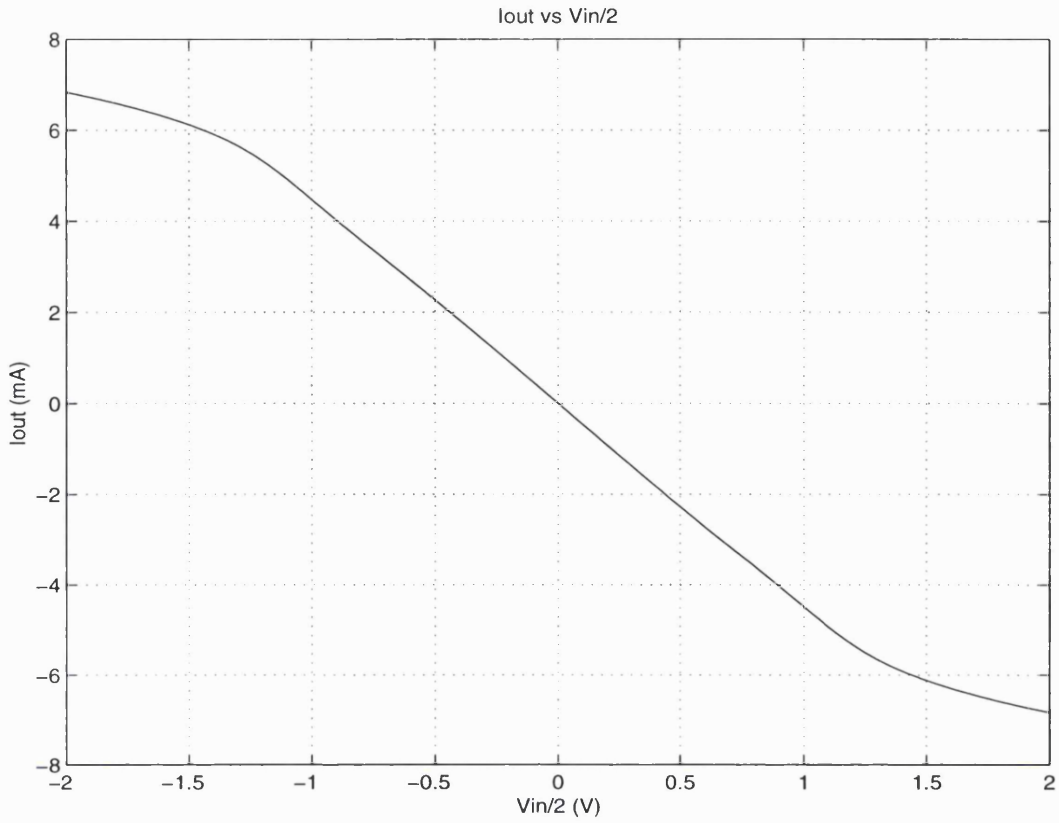


Figure 65. Simulated transconductor output current in dipolar operation (Rload=1kΩ)

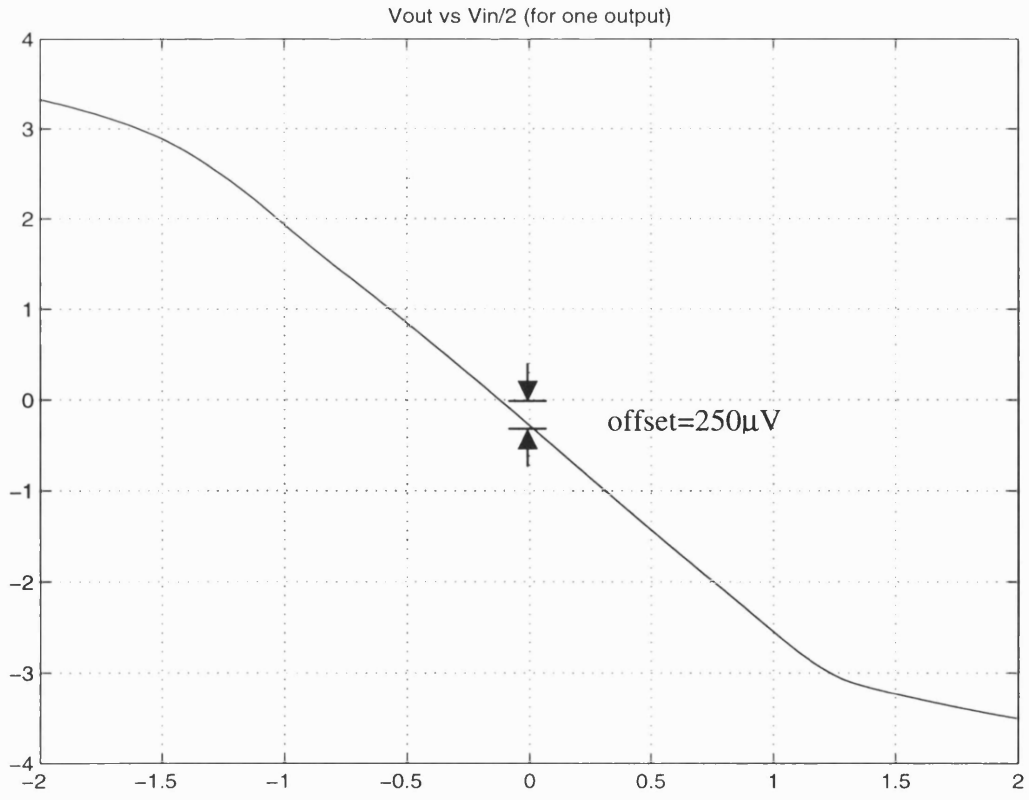


Figure 66. Simulated transconductor output voltage in dipolar operation

Table 29. Linear range (simulation)

Maximum Absolute Deviation	Output Current Range (mA)
≤ 10%	-6.02 to 6.08
≤ 7.5%	-5.89 to 5.94
≤ 5%	-5.63 to 5.65
≤ 2%	-4.39 to 4.40

A small offset voltage can be seen in Figure 66, due to the difference between the reference voltage V1 and Vth of the common-mode feedback transistors. This offset voltage can be reduced by increasing V1, making the common mode voltage smaller.

As ≤ 5% error limit in the output current allows a maximum swing of -5.63mA to 5.65mA (for a 1kΩ load) the transconductor meets the specification for the output current range and load. The fact that the ≤ 2% error range is -4.39mA to 4.40mA means that for most of the operating range the transconductor exceed the linearity specification by at least a factor of 2. In a complete stimulator, it may be desirable to change the specification from +/- 5mA to +/- 4mA to increase the accuracy of the injected charge. As the quiescent current specification is also exceeded for this transconductor, the proposed design was adopted.

With perfectly balanced input voltages the offset of the transconductor is <0.1μA, meaning that the previous stages will actually define the offset current observed at the transconductors outputs.

4.5.8 Initial Experimental Results

4.5.8.1 Single Sided Operation

The transconductor was initially connected single sided with a load impedance of 1kΩ and a bias current of 15μA. Figure 67 shows the experimental relationship between output current and input voltage with a load resistance of 1kΩ, the simulated tolerances are also shown[30].

[30] The bias current for the expected deviation result is varied to maintain a constant V_G.

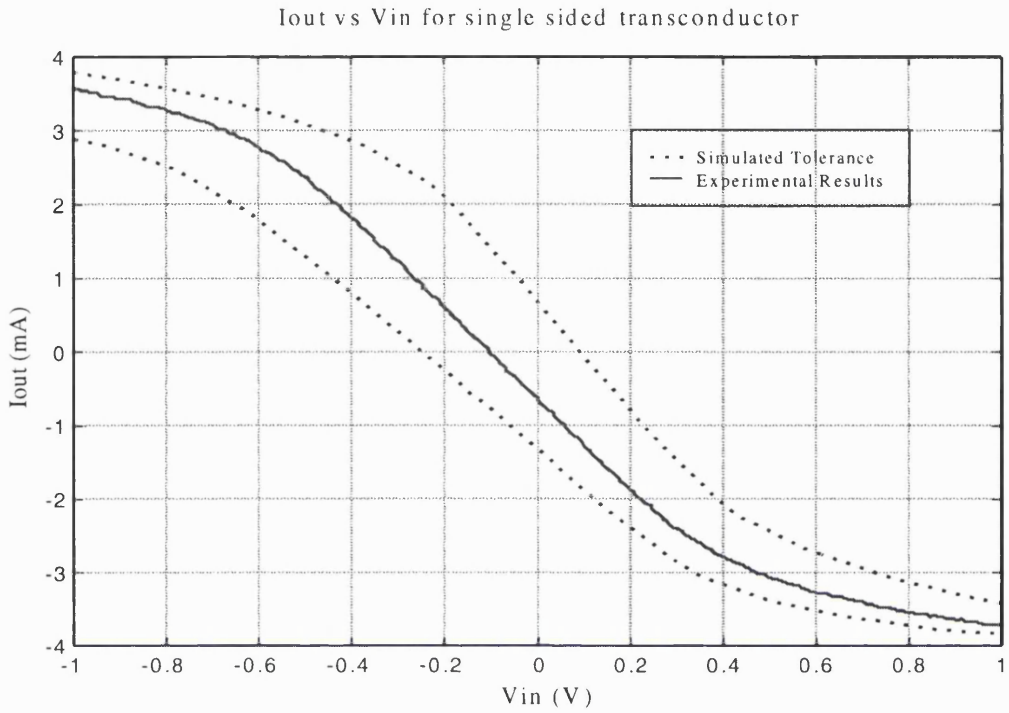


Figure 67. Iout vs Vin transconductor in single sided mode

From the experimental transfer response, the Maximum Absolute Deviation was calculated, the results are shown in Table 30.

Table 30 . Experimental linear range (single sided)

Maximum Absolute Deviation	Output Current Range (mA)
≤ 20%	-3.09 to 3.13
≤ 10%	-2.68 to 2.71
≤ 5%	-2.47 to 2.39
≤ 2%	-1.85 to 1.68

The transconductor shows linear behaviour as expected with a ≤ 5% error range of +2.39mA to –2.47mA. The error is approximately double the theoretical errors shown in Table 29 (error is actually larger due to the voltage offset at the output), this is due to the output swing being approximately halved in single sided operation. Simply doubling these values means that the differential range was expected to be of the order of +/-5mA which just meets the specification.

Varying the bias current allows the transconductance to be varied (by changing V_G); this change in transconductance vs. bias current is shown in Figure 68.

The single sided experimental results show that the transconductor has a linear operation region and the transconductance can be varied in the range 0.2mA/V to 1.4mA/V.

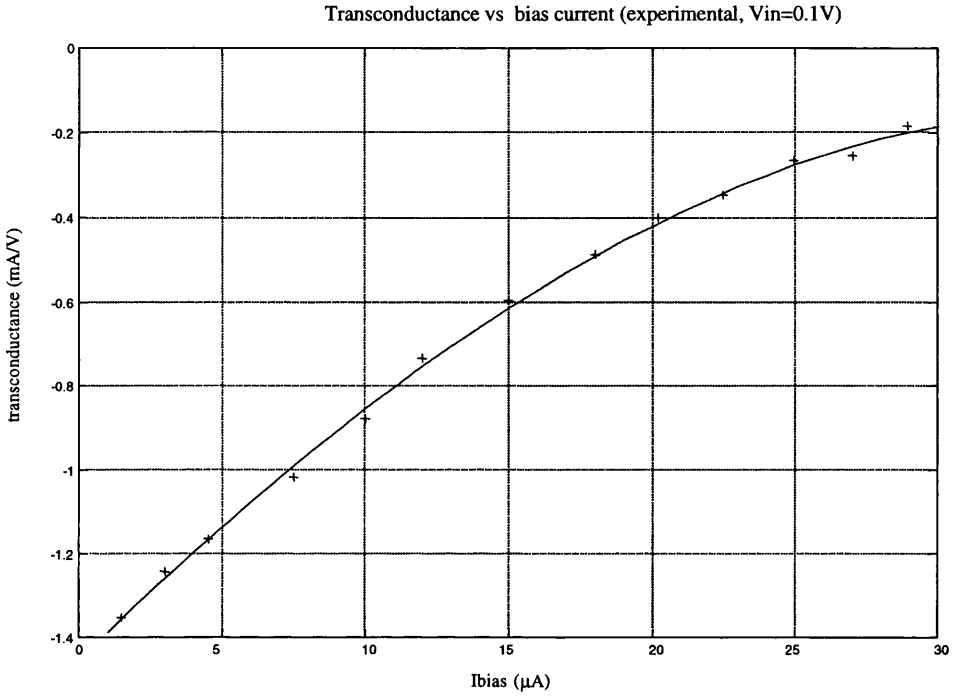


Figure 68. Change in transconductance vs bias current

4.5.8.2 Differential Operation

Unfortunately, a major problem was found with the transconductor in differential operation. With no common mode feedback and with the circuit connected as shown in Figure 64 the circuit functioned as shown in Figure 69, this was exactly the response expected with no common mode feedback and agrees with the simulated results. However, when the transconductors were connected to the common-mode feedback they oscillated sinusoidally with a frequency of approximately 3MHz (with a 1kΩ load). The frequency of oscillation was found to decrease with the load capacitance. Stable operation could not be obtained.

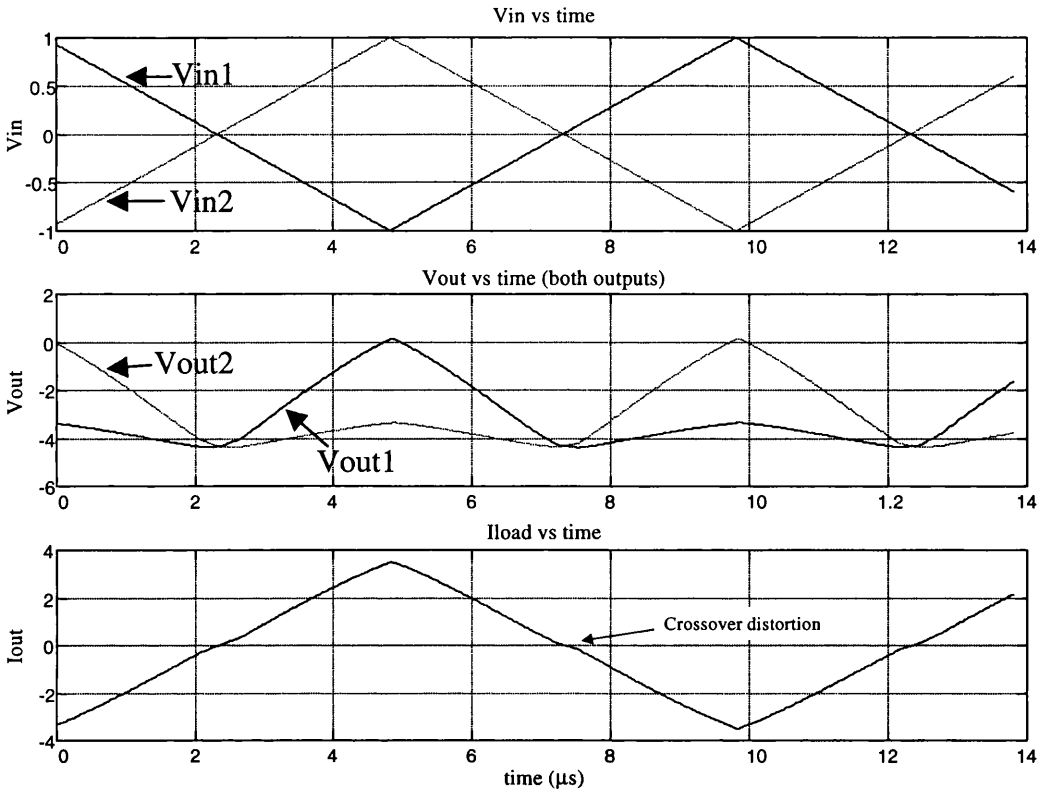


Figure 69 . Differentially connected transconductor with no cmfb

This instability prevented further experimental results using this implementation.

4.5.9 Analysis of Transconductor Instability

This problem had not been observed during transient or ac simulation analysis using HSPICE [89] even when the layout parasitic capacitances were added to the circuit (extracted from the layout using Cadence [29]). The ac response of the transconductor showed no unexpected gain or phase changes in the MHz region so the reasons for the instability did not appear to be simple.

The reason why this problem was not initially observed was found to be two fold:

i) AC analysis was only performed on the circuit with a zero DC offset between the two inputs.

ii) With the extracted parasitic capacitances the circuit simulates as stable during transient analysis, however this turned out to be pure luck, as by changing the loading and parasitic capacitances the circuit can be made to oscillate.

When loading the output with a small capacitance (1pF-1μF) and applying a square wave input, the circuit appears stable initially. However, the circuit starts to oscillate after several cycles. The reason that this oscillation was not observed in simulation before manufacture appeared to be that with the extracted capacitances the circuit appeared to be close to a stable region of operation and long periods of simulation we not run (0.1 seconds). Changing the parasitic capacitances by 50% moves the circuit into a far less stable state and the oscillation starts far more quickly.

The ac response of the transconductor and common mode feedback did not appear to indicate this behaviour; however applying a DC offset to the inputs gives the ac responses shown in Figure 70 and Figure 71. A phase shift and magnitude peak can be seen in the 1MHz - 10MHz range (shown for 1pF - 100pF load capacitance). These changes are not present when a DC offset (of a few hundred mV) is not present. The transconductor is unstable because the transconductor still has gain when the phase shift is close to zero degrees destroying the phase and gain margin of the transconductor and making the circuit unstable.

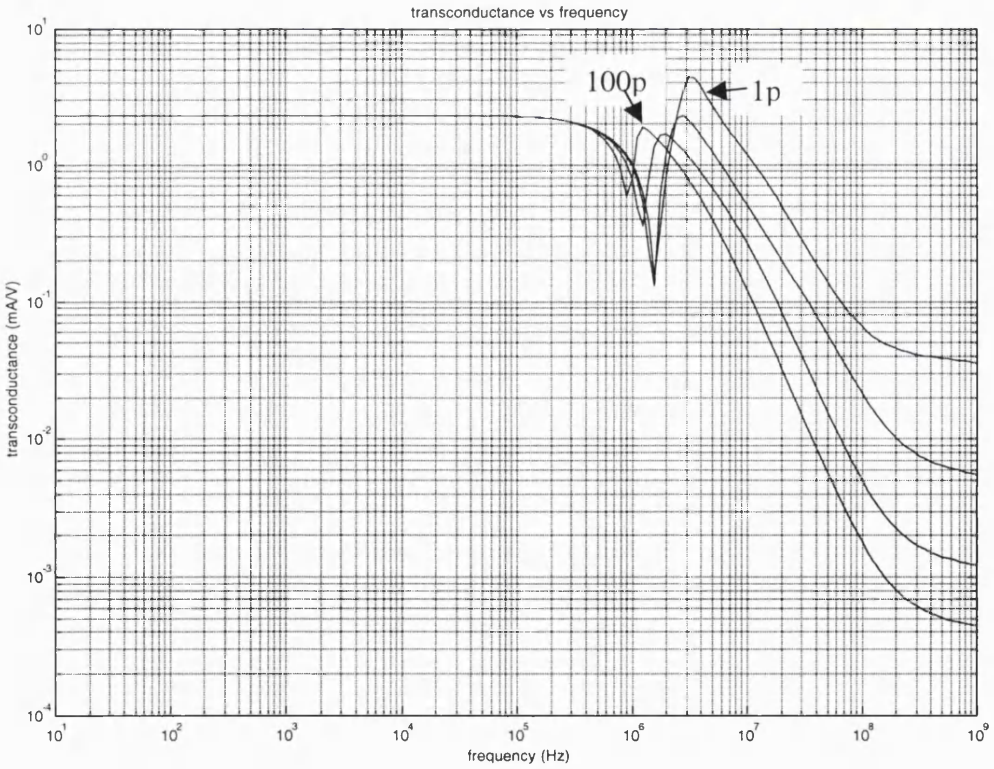


Figure 70. Transconductance vs frequency with a DC input voltage of 300mV

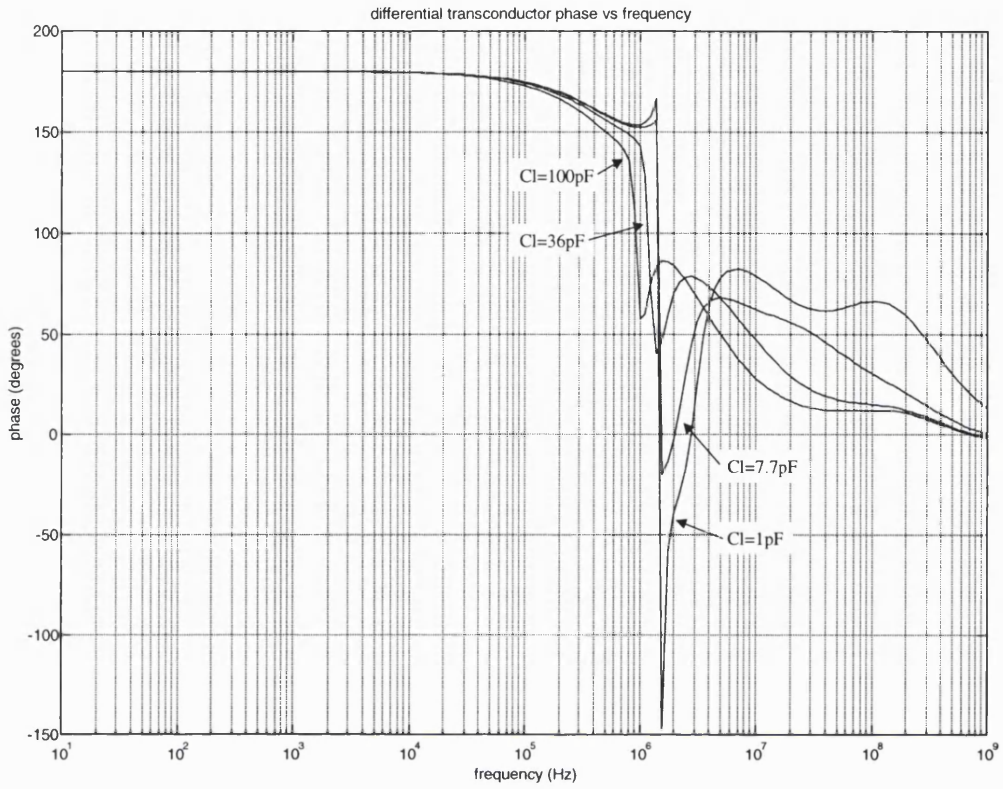


Figure 71. Phase vs frequency with a DC input voltage of 300mV (input to output phase shift)

The reason for these gain peaks appeared to be directly related to the common-mode feedback, which made the open-loop gain too high. This was verified by reducing the gain of the common mode feedback (by decreasing the W/L of the feedback transistors) until stable operation was observed. Stable operation was shown in simulation for a W/L of the p-channel feedback transistor set to < 1. This is a factor of 150 smaller than the original transistor size. When the circuit was incorporated into a complete stimulator IC, as discussed in Chapter 5, the W/L for the n-channel feedback transistor was set to 6/100 and 6/33 for the p-channel transistor. Reducing the common-mode feedback gain has the effect of increasing the common-mode voltage, however this can be corrected for by increasing V1 (the common mode reference voltage).

4.5.10 Experimental Results (using Modified Common-Mode Feedback)

The transient response of the transconductor with modified common-mode feedback is shown in Figure 72. These results were obtained from a complete stimulator device discussed in Chapter 5 (although most test results for this device are not presented in this thesis).

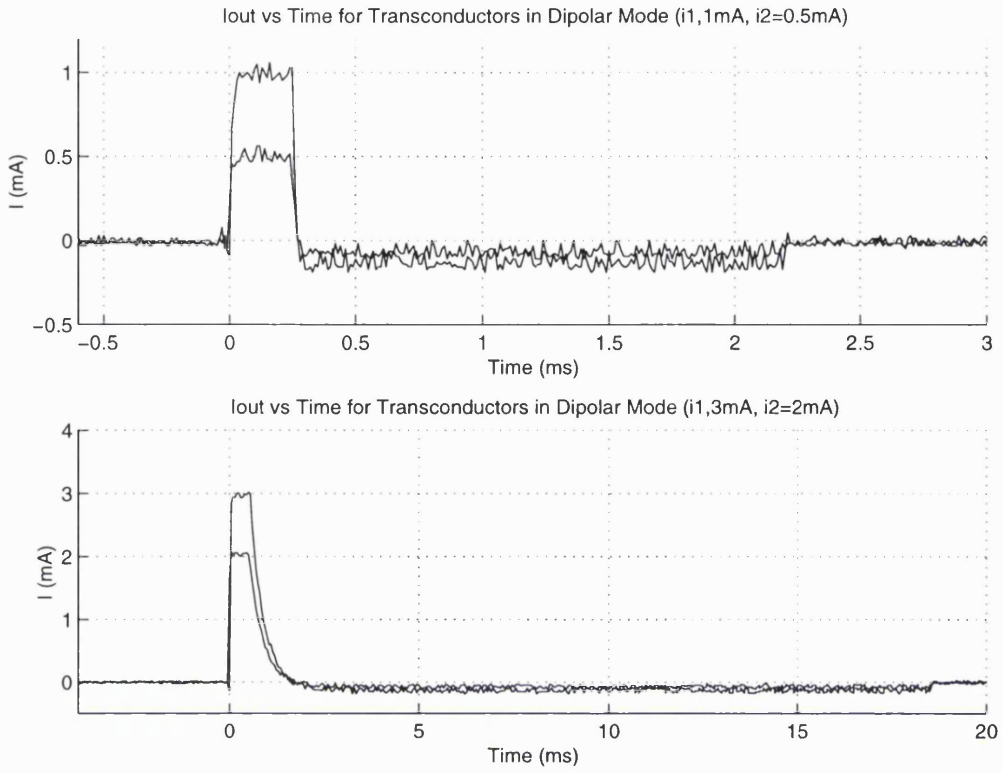


Figure 72. Transient response of the transconductor operating in dipolar mode (two active currents), for 0.5mA, 1mA, 2mA, 3mA stimulation pulses with two differing waveform shapes generated using the pulse generator circuit (R_{load}=1kohm).

The experimental results obtained using the modified common-mode feedback configuration showed stable behaviour when driving both resistive and nerve cuff loads. The Maximum Absolute Deviation was obtained again for while using the modified feedback circuit and the results are shown in Table 31. However, it should be noted that the dimensions of the output and bias transistors were modified in this implementation.

Table 31 . Experimental linear range (differential operation)

Maximum Absolute Deviation	Output Current Range (mA)	
	Simulated	Experimental
≤ 20%	-6.02 to 6.08	-6.4 to 6.1
≤ 10%	-5.89 to 5.94	-5.89 to 5.8
≤ 5%	-5.63 to 5.65	-5.1 to 5.4
≤ 2%	-4.39 to 4.40	-4.1 to 4.0

The quiescent current for this transconductor was found to be 500μA-680μA, measured for four transconductors simultaneously in five Integrated Circuits. This range is slightly larger than the simulated range of 500μA-620μA, however this may have been due to the biasing conditions been different for the simulated and experimental circuits. However, even the highest bias current observed of 680μA is well under the 750μA limit imposed by the specification.

The DC offset current was found to be 0.2μA-1μA when operating in dipolar mode.

4.5.11 Conclusions

The linear transconductor developed meets the specification and functions as expected when used in single sided mode. However due to problems with the common-mode feedback, the realised transconductor was unstable when used differentially with the initial feedback scheme. Without the feedback the circuit functioned as expected, exhibiting crossover distortion close to 0mA. Decreasing the W/L for the feedback transistors has solved the instability problem with no other change to the circuits expected behaviour. The experimental results show the circuit functions as a linear transconductor.

The linearity analysis and experimental results show that the linearity of the transconductor is approximately half that of the transconductor proposed by Park and Schumann, however the output voltage swing is over double that of their implementation. The realised transconductor has a far greater non-linearity than what could be achieved using a differential pair but large bias currents and the need for active loads make the differential pair unsuitable for this device.

Table 32 compares the Specification with the simulated and experimental results.

Table 32. Comparison of specification with simulated and experimental results for the linear transconductor.

Table 32. Comparison of specification with simulated and experimental results for the linear transconductor.

Parameter	Specification	Simulated Results	Experimental Results[31]
Output Current (5% non-linearity)	-5mA to 5mA	-5mA to 5mA	-5.1mA to 5.4mA
Maximum Absolute Deviation (Iout=4mA)	≤ 5%	2.6%	4.3%
DC Output Offset	≤ 3μA	<0.1μA	0.2μA-1.0μA
Quiescent Current (Not Stimulating)	≤ 750μA	500μA-620μA	500μA-680μA

With the discussed modification to the feedback scheme the transconductor is suitable for use in a selective stimulator.

Each differential transconductor occupied 0.25mm^2 when laid out, with a total area occupied area of 1.28mm^2 for 4 differential transconductors, and their associated connections.

[31] Measured in 5 Integrated Circuits, I bias = 15μA

4.6 Switching and discharge arrays

4.6.1 Switching Array

The switching array is required to switch the currents generated by the transconductors to the relevant electrodes during stimulation of dipolar, tripolar and pentapolar nerve cuffs. The switching array also disconnects the transconductors from the electrodes in periods between the stimulation of a particular nerve cuff. The discharge array is required to remove any charge imbalance occurring during stimulation. A detailed description of the need for the switching array is discussed in 3.4.8.

4.6.1.1 Specification

The outputs of the transconductor stages need to be switched to the output pads connected to the individual electrodes (for the reasons discussed in 3.4.8). The switch should introduce as small a voltage drop as feasible.

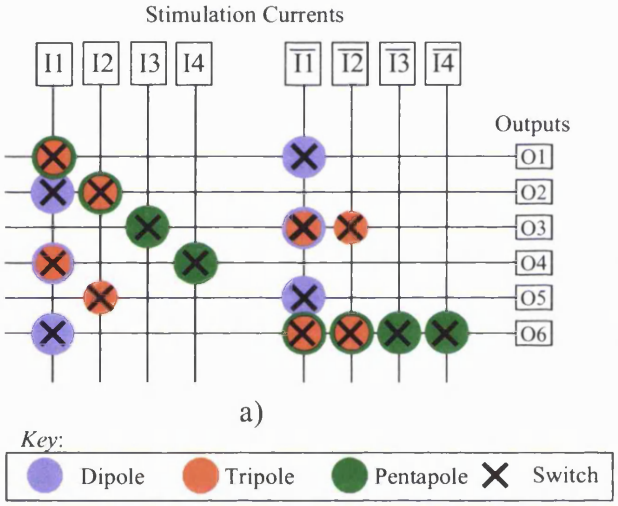
The resistance of the switches was designed to be nominally 50Ω this value is low enough to have only a small voltage drop at 5mA (0.25V), the largest stimulation current, and high enough to produce reasonable sized switches.

Table 33. Switching array Specification

Parameter	Value
On Resistance (nominal designed value)	50Ω
Switching Array Area	$< 2mm^2$
Nerve Cuffs	1 pentapole or 2 tripoles or 3 dipoles

4.6.1.2 Implementation

Figure 73 shows an overview of the organisation of the switches in the switching array in relation to the transconductor current sources and the output pads. The figure shows that several switches are used for more than one cuff. This is also true of the data lines used to control the switching array; the organisation of the data lines in the switching array is shown in Figure 76. In Figure 73 I_1-I_4 represent one side of the differential outputs of the transconductors 1-4 and $\overline{I}_1$-$\overline{I}_4$ represent the other outputs of the transconductors. The switching array is capable of switching currents to three dipoles, two tripoles or one pentapole.

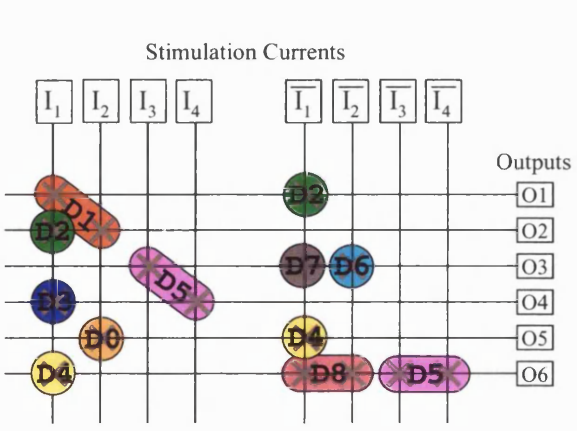


Outputs vs Cuff Type and Connections

Output	Cuff Number, Cathode(C) or Anode(A)					
	Dipole		Tripole		Pentapole	
O1	1C		2A		1C	
O2		1A	2A		1C	
O3	2C			1C	1C	
O4		2A	2A		1C	
O5	3C		2A			
O6		3A		2C		1A

b)

Figure 73. Switch-array organisation showing output switch connections for a) current sources and cuff types and b) electrode connections and cuff types



Data vs Cuff Connections

Data	Dipole			Tripole		Pent
	1	2	3	1	2	1
D0				X		
D1				X		X
D2	X					
D3		X			X	
D4			X			
D5						X
D6					X	
D7		X		X		
D8					X	X

b)

Figure 74. Switch-array data organisation showing output switch connections for a) current sources and cuff types and b) data connections and cuff types

As much compaction as possible of the number of switches needed to control the dipolar, tripolar and pentapolar cuffs was attempted in this design, leading to several switches being used for more than one type of cuff as shown in Figure 73 and Table 34. For example, switch 1 is used to switch current to both tripole 1 and pentapole 1. A simplification of the data lines was performed, so that switches that are used for switching the same cuffs share data lines. The reason for these simplifications was to try and reduce the area occupied by the switching array, which, due to the size of the FETs, is quite large. Figure 74 shows the connection of the cuffs to the outputs and the digital control lines required for each cuff. The table shows that multiple cuffs share both switches and control lines.

Table 34. Switching array connections

Cuff	Cathodes(s)	Anodes(s)	Switches	Data Lines
Pentapole	O1, O2, O3, O4	O6	1, 5, 6, 7, 12, 14, 15, 16	D1, D5, D8
Tripole 1	03	01, 02	1, 5, 10, 13	D1, D7, D0
Tripole 2	06	04, 05	3, 8, 12, 14	D3, D6, D8
Dipole 1	01	02	2, 9	D2
Dipole 2	03	04	3, 10	D3, D7
Dipole 3	05	06	4, 11	D4

The only disadvantage of the merging performed on the data lines is that to control a specific cuff, several data lines have to be used (e.g. for Tripole 1 data lines D1, D7 and D0 are required), this is performed using the digital control logic and is thus not a major problem. The switches were implemented as complementary pairs of CMOS FETs

The resistance of a FET switch operating in its ohmic region is given by:

$$R_{ON} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{(K'W/L)(V_{GS} - V_T - V_{DS})} \tag{4.23}$$

If $R_{ON} << R_{load}$ it can be assumed that V_{DS} is negligible.

To produce a nominal 50Ω switch, the resistance of both FETs was set as 100ohms. Taking into account the body effect, this gives us an n-channel FET with a W/L ≈ 60 and a p-channel FET with a W/L ≈ 175. The final switch design is shown in

Figure 42, each switch has a build in inverter to reduce the number of data lines needed for the switch array. The simulated range of resistances[32] for the CMOS switches was 40Ω to 63Ω, depending on the process parameters described in [90].

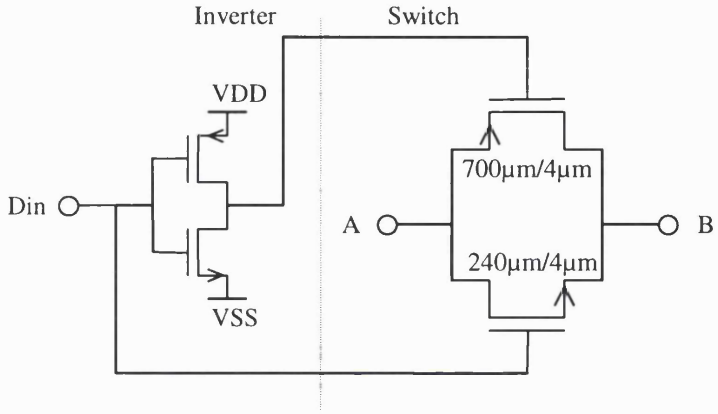


Figure 75. CMOS switch with inverter

4.6.1.3 Results

Table 35 shows the experimental characteristics found for the switching array.

Table 35 Switching array characteristics

Parameter	Experimental Value
Ron (experimental)	57Ω ± 5Ω[33]
Number of Switches	16
Number of Switching Transistors	32
Single Switch Area	0.076 mm^2
Switching Array Area (six outputs)	1.971 mm^2

The experimental value of Ron was found to be close the expected nominally designed value of 50Ω and lies within the simulated range of 40Ω to 63Ω.

[32] Obtained from the process model parameters provided by IMEC.

[33] Number of sample: 7

4.6.2 Discharge Array

The discharge array is required to remove any charge error from the blocking capacitors and electrodes after the two active stimulation phases. A switched resistance is connected in place of every current source as described in 3.4.5.

The value of the resistance was chosen so that any remaining charge would be removed quickly, the nominal value of resistance chosen for the discharge array was 250Ω, the choice of the 250Ω resistance used for the switching array is discussed in detail in 3.4.5 and is not discussed here.

Table 36. Switching array Specification

Parameter	Value
On Resistance (nominal designed value)	250Ω
Switching Array Area	$< 0.75mm^2$

4.6.2.1 Implementation

The circuit is the same as the switching array circuit, with different transistor sizes. Taking into account the body effect, we require an n-channel FET with a W/L ≈ 12 and a p-channel FET with a W/L ≈ 35. Due to the smaller transistor sizes required separate switches were used for tripolar dipolar and pentapolar discharging, allowing simplification of the data lines required to one data line for each mode of operation (dipolar, tripolar and pentapolar). Figure 76 shows how the implemented switching array is connected to the outputs of the IC (and switching array).

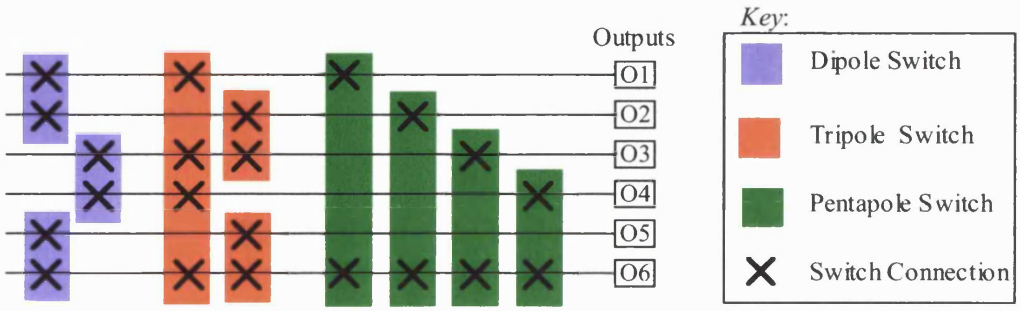


Figure 76. Discharge-array organisation showing switch connections to outputs

The simulated range of resistances for the CMOS discharge switches was 205Ω to 310Ω, depending on the process parameters described in [90].

4.6.2.2 Experimental Results

The experimental characteristics of the discharge array are shown in Table 37.

Table 37. Characteristics of the discharge array

Parameter	Value
Ron (experimental)	220Ω ±11Ω
Number of Switches	11
Number of Discharge Transistors	22
Discharge Switch Area	0.038mm^2
Discharge Array Area	0.64945mm^2

The experimental discharge resistance showed good agreement with the designed value and lies within the simulated range of resistances.

4.6.3 Summary

A discharge and switching array for the stimulator were designed that meet the requirements of the specification given in 3.9.

The switching arrays characteristics were a compromise between the realised resistance and the switch area, the final design occupied less than 2mm^2 and the experimental switching resistance of 57Ω means a voltage drop across the switch of 0.285V when using a 5mA stimulating current. The switching array implementation reduced the number of required switches by using each switch for as many modes of operation as possible, and so only 16 switches are required to control six cuff combinations (one pentapole, two tripoles and three dipoles).

The discharge array having a higher on-resistance (220Ω) and fewer switches occupied only 0.6mm^2 in the final realisation, the experimentally found resistance showed good agreement with the simulated range.

4.7 Long Time Constant Integrator

4.7.1 Introduction

The stimulator needs to be capable of delivering charge balanced current pulses [2.2.1]. The method chosen to do this was to place an integrator at the output of the pulse generator as shown in Figure 39. Inaccuracy in the integrator will cause an error in the charge balancing of phase 1 and phase 2, although the passive discharge should remove any residual charge. The reason for deciding to place the integrator after the pulse generator was for simplicity, since before the attenuator stage the system is single sided, whereas after the attenuator stages the waveforms become differential and have each passed through a gain stage. It would be possible to place the integrator either after the attenuator (integrating voltage), or at the outputs (integrating current). However, in the latter case the integrator would have to operate differentially. A secondary problem of placing only one integrator after the attenuators occurs if the channel to which the integrator is connected is set to zero during stimulation while the other channels are active. Then the integration will not be valid. From the general specification for the stimulator presented in chapter 3, a specification for the integrator was developed.

4.7.2 Specification

The primary concern in the design was the need to produce an integrator with a time constant long enough to keep the output out of saturation during the two stimulation phases. Using a maximum duration, maximum amplitude pulse with a 500μs exponential tail and assuming the amplifier reaches saturation at 2.5V, a time constant of approximately 800μs is required. In this specification, the time constant was specified as 1ms or greater. The reason for the Maximum Operating Frequency is due to the short duration of some stimulation pulses (of pulse width 20μs). The maximum charge balancing error comes from the discussion of active and passive charge balancing in Chapter 3. The DC output offset voltage is important as this leads to errors in the detecting of when charge is balanced. Finally, due to the fact that some external components were required for the pulse generator (to allow the time constant to be adjusted after integrated circuit manufacture), and the desire to integrate as much of the stimulator as possible the specification defines a totally integrated solution.

Table 38. Long time-constant integrator specification

Parameter	Value
Time Constant (τ)	≥ 1ms
Maximum Operating Frequency	≥ 100kHz
Maximum Charge Balancing Error (worst case)	≤ 5%
DC Output Offset	< 15mV
External Components	None

The Maximum deviation is defined as the error at the end of stimulation from ideal and is assumed worst for a low-amplitude short-duration stimulation pulse.

4.7.3 Implementation

4.7.3.1 Background

A classical RC Miller inverting integrator is shown in Figure 77.

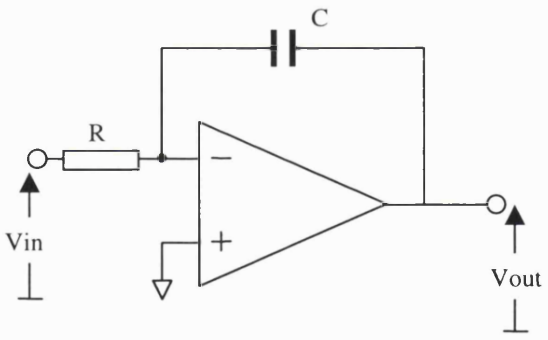


Figure 77. Classical miller integrator

The time constant of the Miller integrator is given by:

$$\tau = RC \tag{4.24}$$

The output voltage is given by:

$$V_{out}(t) = \frac{1}{\tau}\int_0^t V_{in}(t)dt \tag{4.25}$$

It is not feasible to realise large value capacitors on integrated circuits, the dimensions required for a 30pF capacitor being approximately 300µm by 300µm ($0.09mm^2$) for the Mietec 2.4µm process. For a time constant of 1ms and a capacitor of 10pF ($0.27mm^2$), the resistor value would have to be 100MΩ, which is not a practicable value on an integrated circuit using any form of passive resistor.

One solution is to use a FET, biased in its ohmic region, to simulate a resistor. The resistance of a FET in its ohmic region is given by:

$$R_{on} = \frac{1}{k'(W/L)(v_{gs} - v_t - v_{ds})} \tag{4.26}$$

To realise a 100MΩ resistor using a typical n-channel FET (assuming Vds=0V, Vgs=5V) a W/L[34] of 20,000 is required. Using a pair of complementary FETs to reduce the voltage dependant nature of the active resistor, the sizes are doubled to approximately W/L = 40,000 for the n-channel FET and W/L = 120,000 for the p-channel FET[35]. Using minimum transistor dimensions would require a 120mm/3µm n-channel FET and 360mm/3µm p-channel FET, these transistors are unfeasible to integrate due to the large areas required[36]. The resistor could be replaced with a T-Cell of resistors as shown in Figure 78.

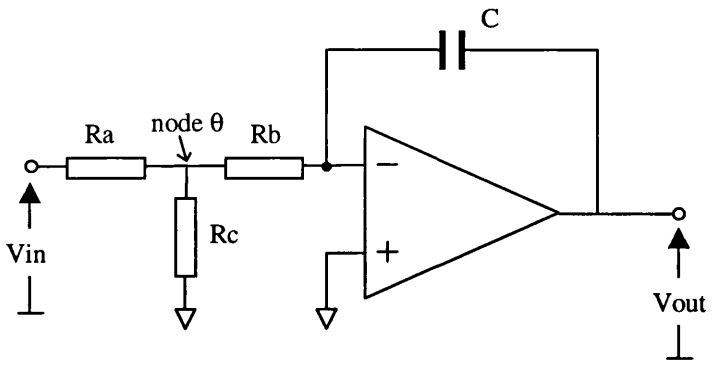


Figure 78. Integrator with a T-Cell resistive input

[34] W = Width, L = Length

[35] Using the Mietec 2.4µ process.

[36] The area would be approximately 1.125mm² for the n-channel and 3.375mm² for the p-channel.

The effective resistance of the T-Cell of resistors is given by:

$$Reff = \frac{RaRb}{Rc} + Ra + Rb \tag{4.27}$$

Assuming $Ra = Rb = R1$ then:

$$Reff = \frac{R1^2}{Rc} + 2R1 \tag{4.28}$$

For an effective resistance of 100MΩ then R1=316kΩ and Rc=1kΩ: t would be feasible to implement these values as active resistors. However, the actual value of the Reff would be very inaccurate, as small changes in R1 (or Rc) produce large changes in the effective resistance. This circuit also suffers from the amplifiers input offset, due to the very small input voltage actually presented at node θ in Figure 78. This offset voltage is the effective input voltage to the integrator. Using the values just calculated the voltage at node θ is 1.5mV for a 1V input, which is the same order of magnitude as the input offset voltage of CMOS op-amps.

Another method to produce a long time constant is to employ a transconductance stage to charge a small capacitor. However, the current would have to be set to 10pA for time constant of 1ms using a 10pF capacitor. This, again, is not really suitable for integration.

At this point in the design process, it was decided to investigate the possibility of using a switched-capacitor circuit to implement the integrator, although a switched current circuit implementation was also a possibility. For switched capacitor circuits the time constant is defined by a ratio of two (or more) capacitances giving an accurate time constant [61,78] as will be shown in 4.7.3.2. For simple switched current integrator's the time constant of the integrator depends on both transistor ratios (which can be accurately defined) and the ratio of transistor transconductance to a capacitance, which may vary widely with random and systematic variations [78,157]. For these reasons the switched capacitor implementation was investigated fully.

4.7.3.2 Switched Capacitor Integrator's

In a conventional Switched Capacitor (SC) circuit, the resistors are replaced by switches and capacitors. Transferring packets of charge from one node to another

simulates the effect of a resistance. Figure 79 shows a simple SC integrator that is insensitive to parasitic capacitance [140].

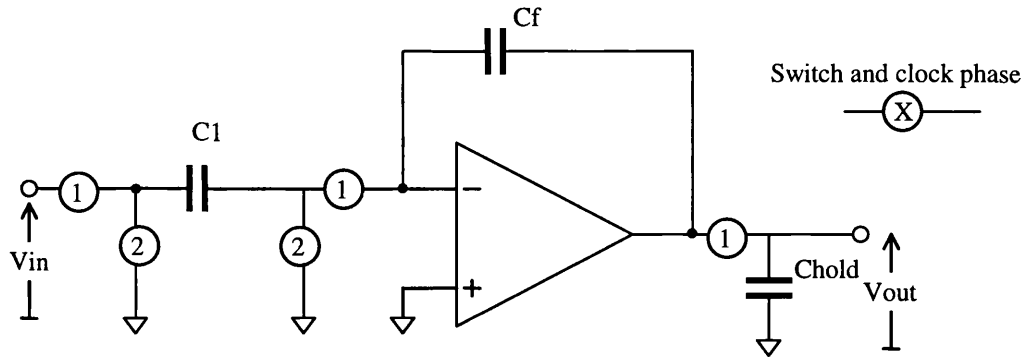


Figure 79. Simple switced-capacitor integrator with a sample and hold circuit

The value of the equivalent resistance for a capacitor switched at frequency f_s is:

$$R_{eq} \approx \frac{1}{C_1 f_s} \tag{4.29}$$

The time constant of the integrator is:

$$\tau \approx \frac{C_f}{f_s C_1} \tag{4.30}$$

A capacitor ratio and the switching frequency now define the time constant. Typically, the capacitor ratio can be set to 0.1% accuracy or better using CMOS technology [33,107]. The main limitations of SC filters are [69,126]:

i) Charge injection in the switches [98]
ii) Signal to noise limitation [67]
iii) Charge transfer error (due to limited amplifier gain) [69]

Careful layout methods can minimise these effects: the precautions taken during the layout of the integrator are discussed in Appendix 2.

For the simple integrator shown in Figure 79, the capacitance ratio can be calculated. Firstly assuming the clocking frequency is 200kHz (allowing four samples during a minimal plateau duration of 20μs), and by defining C_1 as 400fF[37], then from

[37] For the Mietec 2.4μ m process, this is approximately the smallest capacitor value suitable for realising accurate switched capacitor circuits [126].

(4.18) C_f is 80pF. The value of 80pF is too large to realistically integrate because of its large area (0.67mm^2) and the required ratio of 200 would be difficult to produce accurately. However, it is possible to design a switched capacitor version of the T-Cell integrator.

4.7.3.3 Integrator Development

Sansen and van Peteghem [125,147] produced a circuit based on the T-Cell idea that functioned as a very long time constant unity gain low pass filter, the experimental results presented showed that very long time constant switched capacitor filters were realisable using switched capacitor circuits. No simulation results were presented, as this circuit was too complex to simulate at the time (the authors claimed). Other methods for increasing the time constant of switched capacitor filters do exist (either dividing the integrated charge or lowering the clocking frequency in parts of the circuit). However, they all have the problems of being very sensitive to input offset voltages [73,107,125] or of having reduced frequency responses [73,107,153], making them unsuitable for this specific application. For these reasons the T-Cell Switched Capacitor Integrator was chosen for this application. The proposed circuit, shown in Figure 80, this circuit is the same as the circuit developed by Sansen & van Peteghem [125,147] except the feedback capacitors and switches for the unity gain have being removed. The feedback capacitor (not shown) was the same value as the smallest capacitor and does not provide a suitable feedback scheme for this implementation because for a reasonable DC gain the feedback capacitor would have to be at least an order of magnitude smaller than the smallest switched capacitor. The removal of this capacitor causes the circuit in Figure 80 to have a high DC gain (effectively the DC gain of the amplifier), exagerating the effect of the amplifier offset. A modified DC feedback path was essential to make the circuit functionally stable.

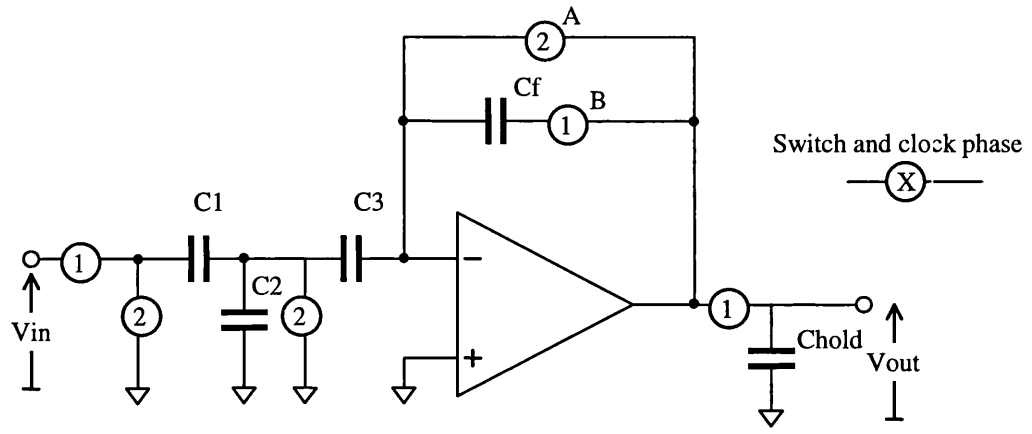


Figure 80. T-cell switched capacitor integrator

The voltage transfer function of the T-Cell integrator, shown in Figure 80, is given by:

$$\frac{Vo(z)^1}{Vi(z)^1} = -\frac{C_\alpha z^{-1/2}}{C_f(1-z^{-1})} \tag{4.31}$$

Where: $C_\alpha = \frac{C_1 C_3}{(C_1 + C_2 + C_3)}$

The time constant of the T-Cell switched capacitor integrator is given by:

$$\tau = \frac{C_f(C_1 + C_2 + C_3)}{f_s.C_1C_3} = \frac{C_f}{f_s.C_\alpha} \tag{4.32}$$

Setting $C_1 = C_3 = 400$fF, $C_2=C_f$, and fs = 200kHz, the value of C_2 and C_f needed for a 1ms time constant becomes 5.27pF. This new capacitor ratio of 1:13 is realisable and obviously consumes much less area than the capacitor ratio of 1:200 needed for the simple switched capacitor integrator. This was the design selected for the integrator. The capacitor ratio was actually set to 1:15 (C_1:C_2) to give a divisible number of unit capacitors (C_1=400fF, C_2=6pF), and making the time constant of the integrator 1.275ms (fs=200kHz) or 1.02ms (fs=250kHz).

Figure 80 shows two extra switches (A and B) in the feedback loop, the function of these extra switches is to implement correlated double sampling of the integrator. This is a method to reduce the effect of amplifier offset and provides a way of resetting the amplifier (by turning on all of the switches at the same time). The reduction of offset is important, due to the smallness of the effective input voltage, referred to above, and the high DC gain of the integrator.

4.7.3.3.1 DC Stability Feedback for the T-Cell Integrator

From equation 4.20 it can be seen that the integrator of Figure 80 is not DC stable, as when z=1 (DC), Vo/Vi→-∞. This means that the integrator requires feedback to define the DC gain. A method to provide DC stability is shown in Figure 81. The new voltage transfer function becomes:

$$\frac{Vo(z)^1}{Vi(z)^1} = -\frac{C_\alpha z^{-1/2}}{C_f(1-z^{-1})+C_x z^{-1}} \tag{4.33}$$

Where $C_\alpha = \frac{C_1 C_3}{(C_1 + C_2 + C_3)}$

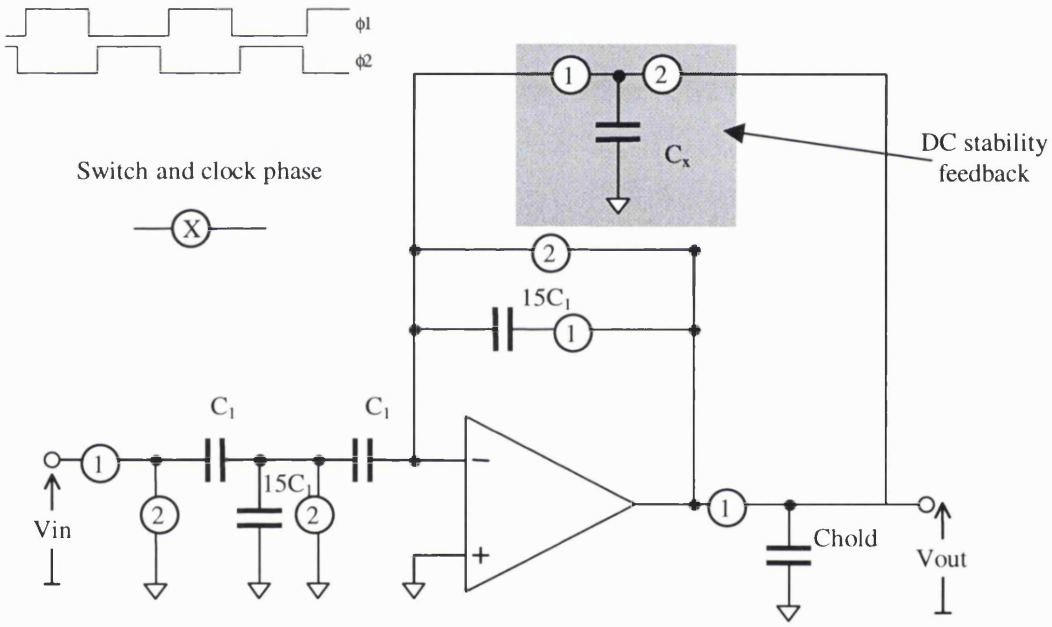


Figure 81. T-Cell integrator with DC stability feedback of Figure 81

The pole for the integrator has now being moved from z=1 to z=1-Cx/Cf, as shown in Figure 82, making the integrator DC stable and defining the DC gain.

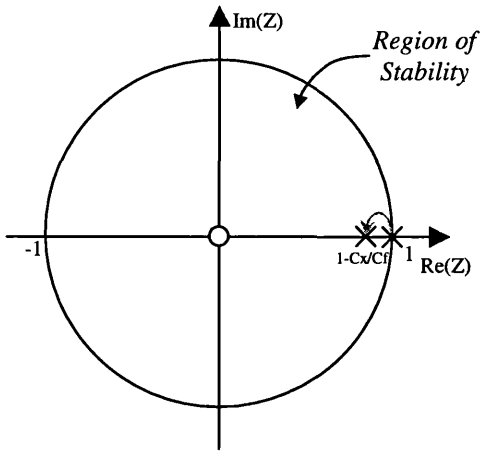


Figure 82. z-plane pole-zero diagram for the t-cell integrator

The DC gain for integrator becomes:

$$\frac{Vo(z=1)^1}{Vi(z=1)^1} = -\frac{C_\alpha}{C_x} \tag{4.34}$$

Figure 83 shows the integrator's theoretical frequency response with different amounts of DC feedback. With a DC gain of 30dB the magnitude error at 20Hz is below 1%[38]. A gain of 30dB requires that $C_x = C_\alpha/31.6$. As C_α is the equivalent capacitance of the T-Cell and is already small ($C_1/17$), C_x has to be approximately $C_1/500$. To keep the capacitance spread small (and so reduce the total capacitance) this can be realised by moving the DC feedback connection from the amplifiers negative input, back to share the input T-Cell of capacitors and switches. The circuit also utilises a T-Cell in the DC feedback to obtain an effective overall feedback capacitance of $C_1/500$. If the DC feedback connection were not moved two cascaded T-Cells of capacitors would be required to obtain the same effect. The developed integrator is shown in Figure 84.

[38] Assuming that the longest stimulation pulse used is 50ms, then the lowest frequency of interest is 20Hz

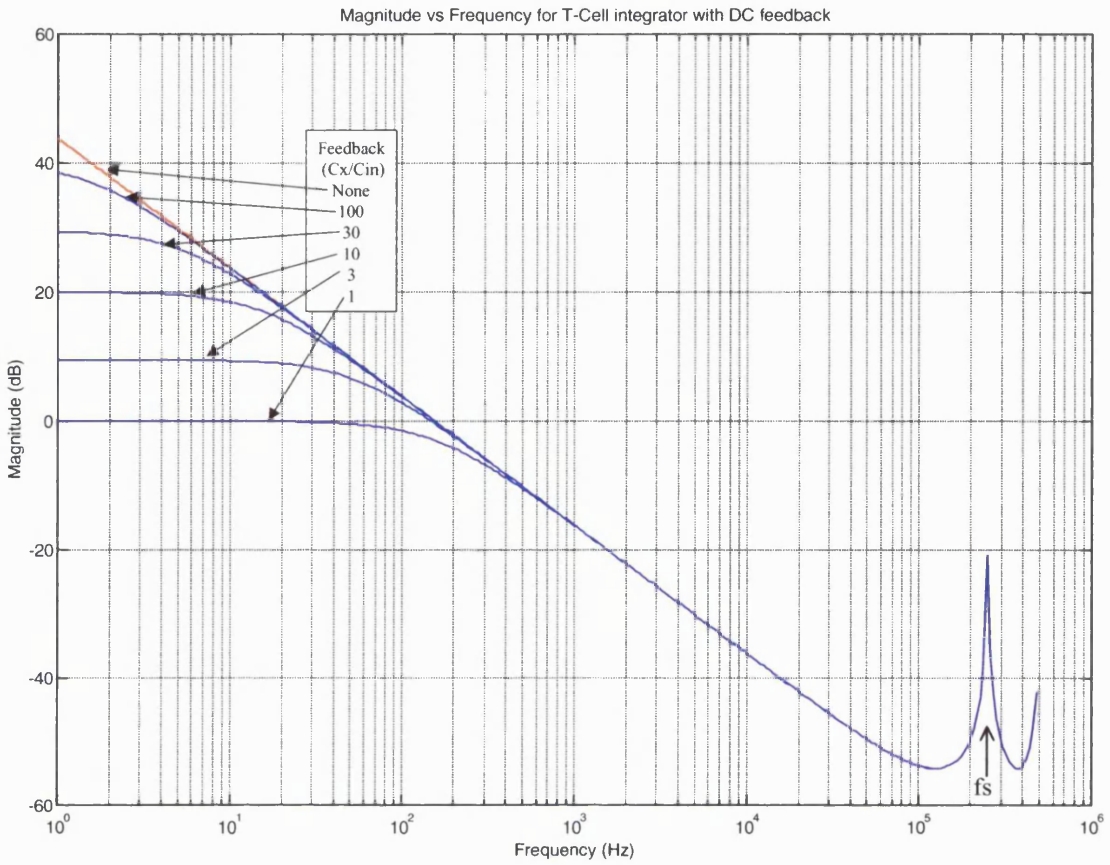


Figure 83. T-Cell integrator AC magnitude response with DC feedback, fs=250kHz. Circuit shown in Figure 81

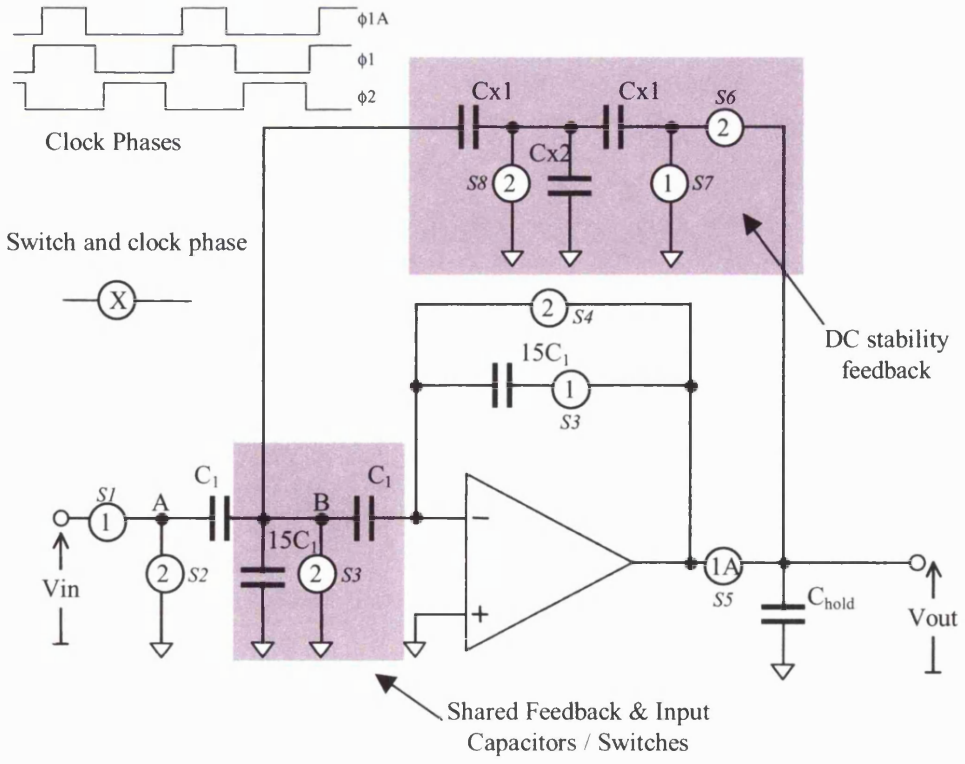


Figure 84. Final T-Cell integrator with DC stability feedback

The effective capacitance in the DC feedback pathway, shown in Figure 84 is given by:

$$C_x = \frac{C_{x1}^2 C_1}{C_{x1}^2 + 32C_1C_{x1} + 16C_1C_{x2}} \tag{4.35}$$

For Cx = C_1/500, Cx1 = C_1 then Cx2 = 29.75C_1. However, as the absolute value of the DC gain is not critical Cx1 can be reduced to C_1/2 without adversely affecting the behaviour of the circuit, reducing the required Cx2 to 7C_1. With this feedback scheme the total capacitance required for the integrator increases from 32C_1 (12.8pF) to 40C_1 (or 16pF).

4.7.3.4 Improvement in Observed Switching Transients

The circuit shown in Figure 84 has three switching clocks ϕ1, ϕ1A, ϕ2. Effectively ϕ1 and ϕ1A are in phase except ϕ1A turns on after ϕ1 starts and off before ϕ1 finishes. This is to reduce the observed switching transients at the output, due to the transients that occur inside the integrator in the period between ϕ1 and ϕ2. By having ϕ1A start only when ϕ1 is fully established, the switching transients as the amplifier settles can be eliminated producing an output with less transient noise. ϕ1A is fully generated from ϕ1 inside the integrated circuit.

4.7.3.5 Integrator Layout

Appendix 2 discusses the layout precautions and methodology used for the construction of the T-Cell Integrator.

The complete integrator layout occupied 0.38mm^2. This compares with the area required for an 80pF capacitor of 0.67mm^2 (as needed by a simple switched capacitor integrator). This smaller area, and the reduced capacitance spread, are the main advantages of the T-Cell Integrator.

4.7.3.6 T-Cell Integrator Amplifier

Amplifiers are one of the essential parts of switched capacitor filters; their major effect on performance is errors introduced when charge is transferred between capacitors and the introduction of noise [33]. DC gain, offset, common mode and power supply rejection are also important [40,73].

In SC circuits operational transconductance amplifiers (OTAs) are normally used in preference to operational amplifiers (OAs) as only capacitive loads are present. OTAs can provide a wider bandwidth than OAs leading to a faster settling time, although due to

the slow clocking frequency in this application this is not important. Adding a second gain stage can increase the gain of both OTAs and OAs, however this method requires that an internal compensation capacitor is used to compensate the amplifier for stable operation. In SC filters the load capacitance changes during clock phases, requiring that a large compensation capacitor be used to reduce the effect of the variation [33]. Therefore, single stage amplifiers are normally used and cascoding techniques are used to increase the DC gain [126]. One of the main problems of single stage amplifiers is that the changing load capacitance changes the amplifier slew-rate [40]. The effective load capacitance can be given in terms of its input (C_i), feedback (C_f) and load (C_L) capacitances by [126]:

$$C_{eff} = C_L + C_i + \frac{C_L Ci}{Cf} \tag{4.36}$$

The key specifications for the amplifier are given in Table 39:

Table 39. Integrator amplifier specification

Parameter	Value
DC Gain (A)	> 74dB
Unity Gain Bandwidth	> 4MHz
Slew rate	> 2.5V/μs
Input offset voltage	< 1mV
Output Voltage Swing	-2.5 to 2.5V

The required DC gain is higher than would be expected on first inspection. This is due to the charge injection error of the integrator not being 1/A, as would be expected for a simple switched capacitor circuit, but C_α/AC_1 [125] due to the charge division occurring in the T-Cell.

The amplifier circuit designed is shown in Figure 85 and is based on a folded cascode amplifier [61]. In the past, dynamic biasing techniques have been used to decrease the quiescent current, however these circuits add additional complexity to the design. It was decided to simply use a large output stage to drive the load. As only one of these amplifiers is present on the circuit this extra power consumption is not a major concern on the test devices, and, if necessary, dynamic biasing techniques can be introduced in later designs.

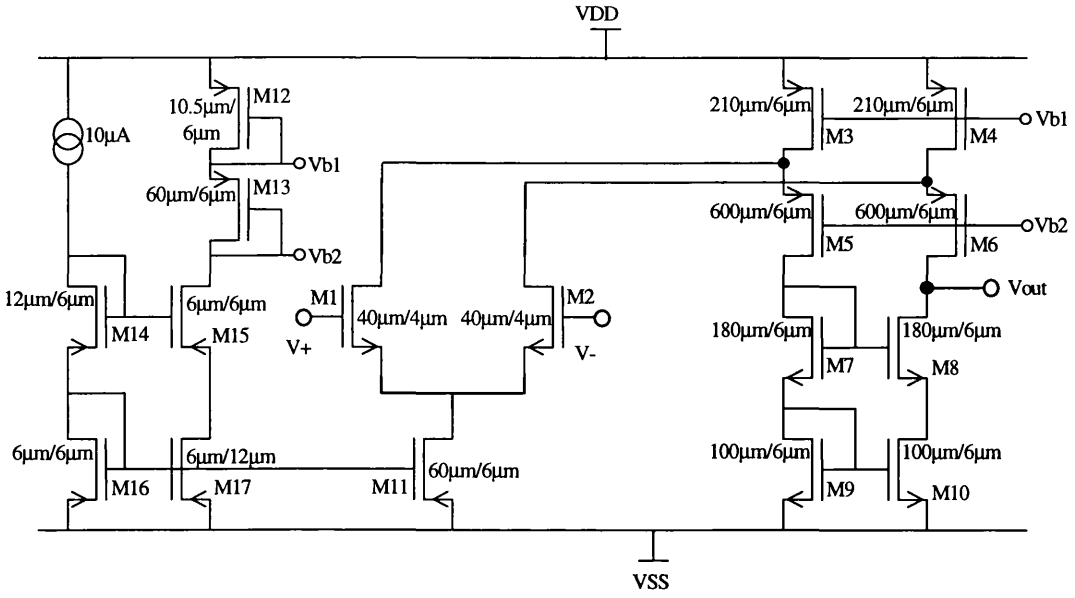


Figure 85. Folded cascode amplifer for the integrator

4.7.4 Simulation Results

4.7.4.1 Simulation of the Integrator Circuit

The circuit was simulated with both HSPICE [89] and SWITCAP2[39] [131]. Due to inherent software limitations, only transient analysis could be performed in HSPICE, SWITCAP2 was used for frequency analysis. Figure 86 shows the simulated transient response (Low pass filtered at 250kHz to remove fast switching transients (see 4.7.5.3) of the inverting T-Cell integrator with DC stability feedback. Figure 87 shows the integrator's transient deviation from an ideal real time integrator of identical gain. The error at the end of the stimulation pulse is approximately 0.3%[40] in the example shown, however the simulated worst-case error is 4.4% when using the shortest stimulation pulse of 20µs (fs=200kHz, no exponential tail). The worst case simulated error for a maximal amplitude, maximal duration stimulation pulse was 0.25% (this equates to a charge injection error during stimulation of approximately 12pC). This maximum simulated error of 4.4% meets the specification given in 4.7.1.

[39] Switcap2 is a simulation program for analysing switched capacitor circuits in both time and frequency domains

[40] Error defined by Vout(max)/Vout(end of stimulation)

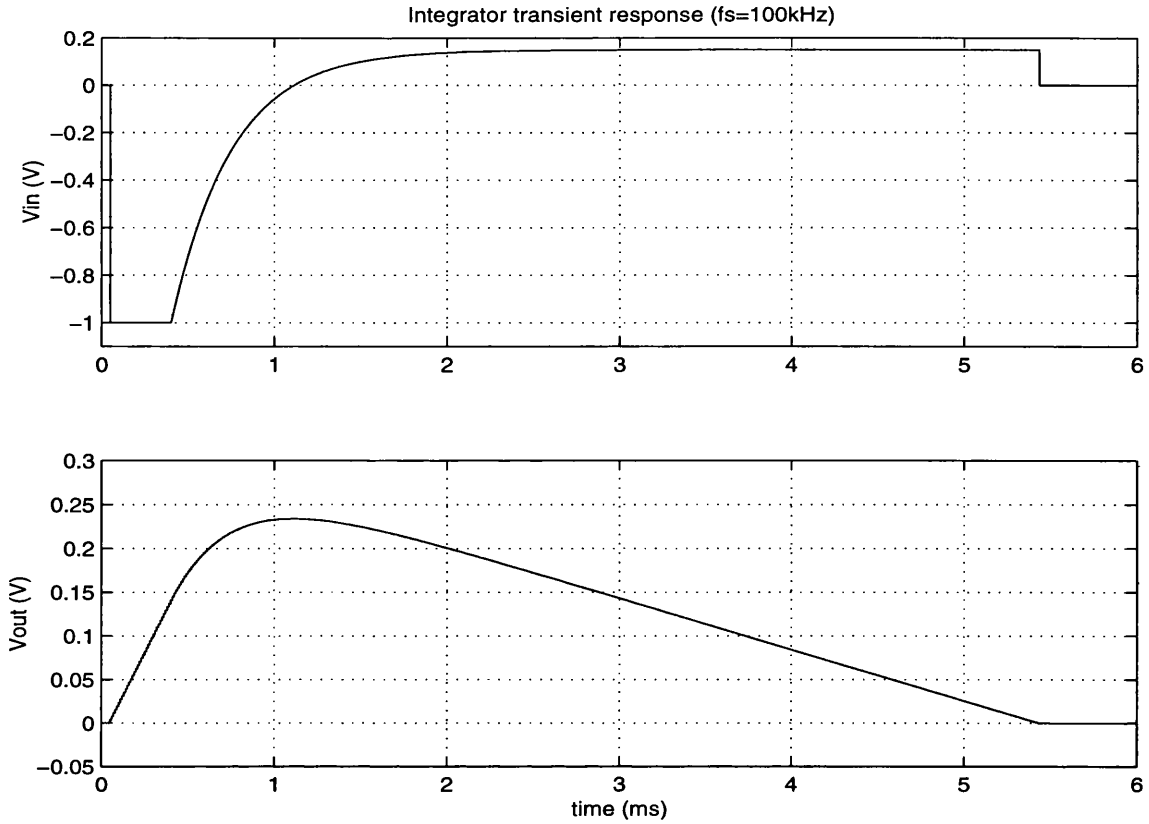


Figure 86. Simulation results for the inverting T-Cell SC integrator, fs=100kHz, top signal Vin, bottom signal Vout

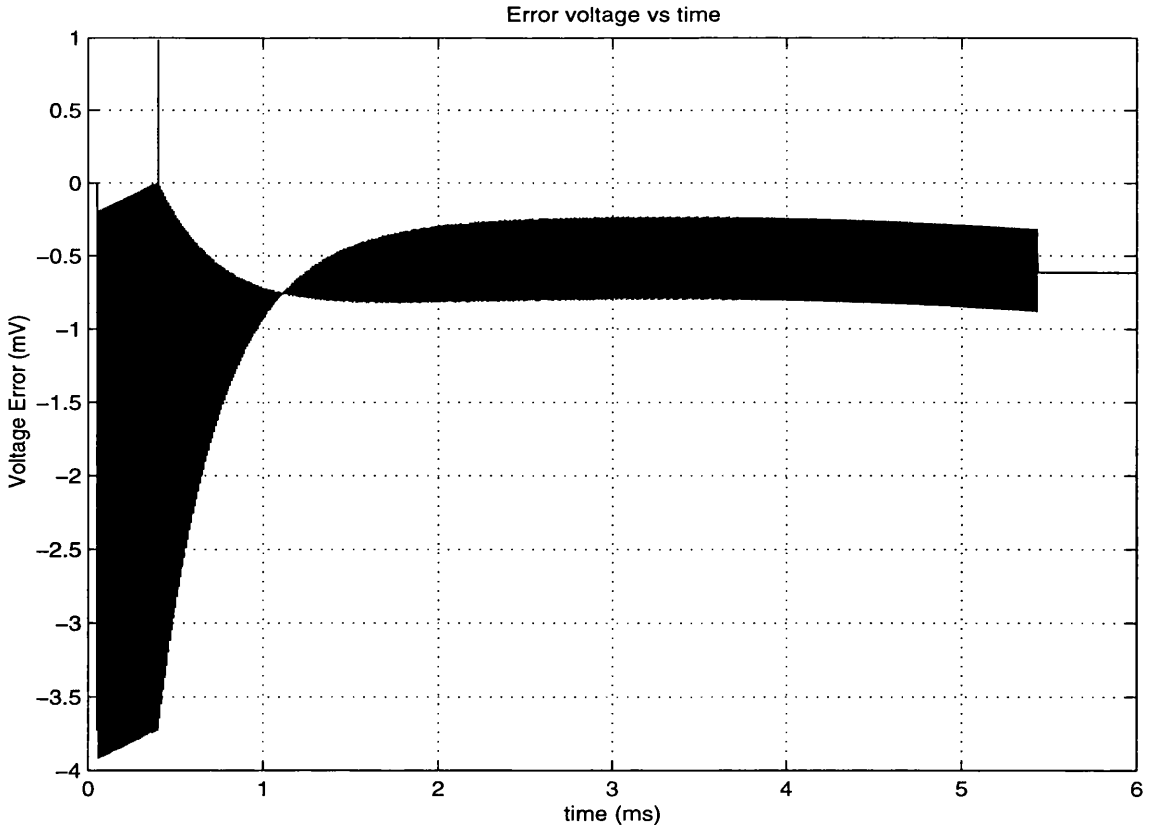


Figure 87. Transient integrator error (fs=100kHz)

4.7.4.2 Simulation of DC Output Offset Voltage

Even though correlated double sampling[41] of this switched capacitor has being implemented, the offset observed at the output has to be carefully considered due to the high low frequency gain of this circuit. In simulation it was found that certain switches in the input T-Cell contributed to a DC output offset voltage due to charge injection from the switches. Table 40 shows the output-offset voltages simulated in HSPICE (this offset is far larger than found when using SWITCAP2), for the circuit shown in Figure 81 with and without dummy switching transistors[42] to reduce charge injection. Table 40 shows that only switches in the input T-Cell (S1-S3) contribute significantly to the DC output offset voltage. From these simulation results, it is clear that dummy switches are required for switches S1-S4 to reduce the offset of the integrator to a level that meets the specification. However the initial layout of the integrator did not have these dummy transistors (the offset was difficult to reproduce during simulation, and not fully appreciated until after manufacture) and so a larger DC offset than expected was present for the experimental results obtained for the T-Cell Integrator.

Table 40 . Simulated offset of the T-Cell integrator using dummy transistors

Switches with Dummy Transistors	Simulated DC Output Offset
None	235mV
All	7.5mV
S1	71mV
S1-S3	11mV
S1-S4	7mV
S1-S5	7mV
S1-S6	7.5mV

The simulation results for the integrator amplifier are discussed following the experimental results.

[41] Correlated Double Sampling works by sampling the integrator offset during $\phi 2$ back to the input and is implemented using S4 in Figure 84

[42] Dummy switches are explained in Appendix 2.

4.7.5 Experimental results

All experimental measurements on the integrator output were taken using the buffer, described in Appendix 2, connected inside the integrated circuit. All of the results presented have the buffer offset voltage subtracted[43].

For testing the integrator was set up as shown in Figure 88.

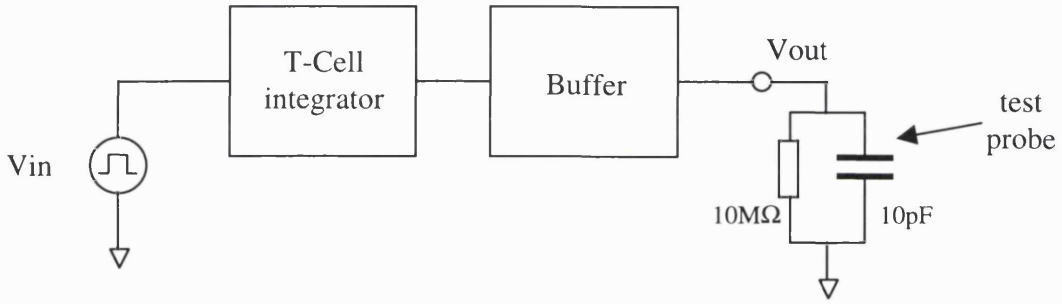


Figure 88. Test configuration for the T-Cell integrator

4.7.5.1 Integrator Time Constant

The time constant was measured using a 1V pk-pk square wave (1kHz) (Table 41)[44].

Table 41. T-Cell integrator characteristics

Clocking Frequency	Time Constant[45]	
fs	Theoretical Value	Experimental Value
fs=100kHz	2.56ms	2.52ms ± 0.12ms
fs=200kHz	1.28ms	1.25ms ± 0.07ms
fs=250kHz	1.02ms	1.01ms ± 0.07ms
fs=500kHz	0.51ms	0.49ms ± 0.06ms

The theoretical time constant for the integrator agrees well with the experimental results. By clocking the integrator at 250kHz the specification of a time constant of greater than 1ms is met.

[43] Offset Voltage measured using test structure on SSTIM3.

[44] For 4 devices

[45] ±1V square wave input at 500Hz

4.7.5.2 Integrator Transient Behavior

Figure 89 shows the output of the T-Cell Integrator (after the buffer stage) while having a 1V rectangular stimulation waveform applied at the input (fs=250kHz).

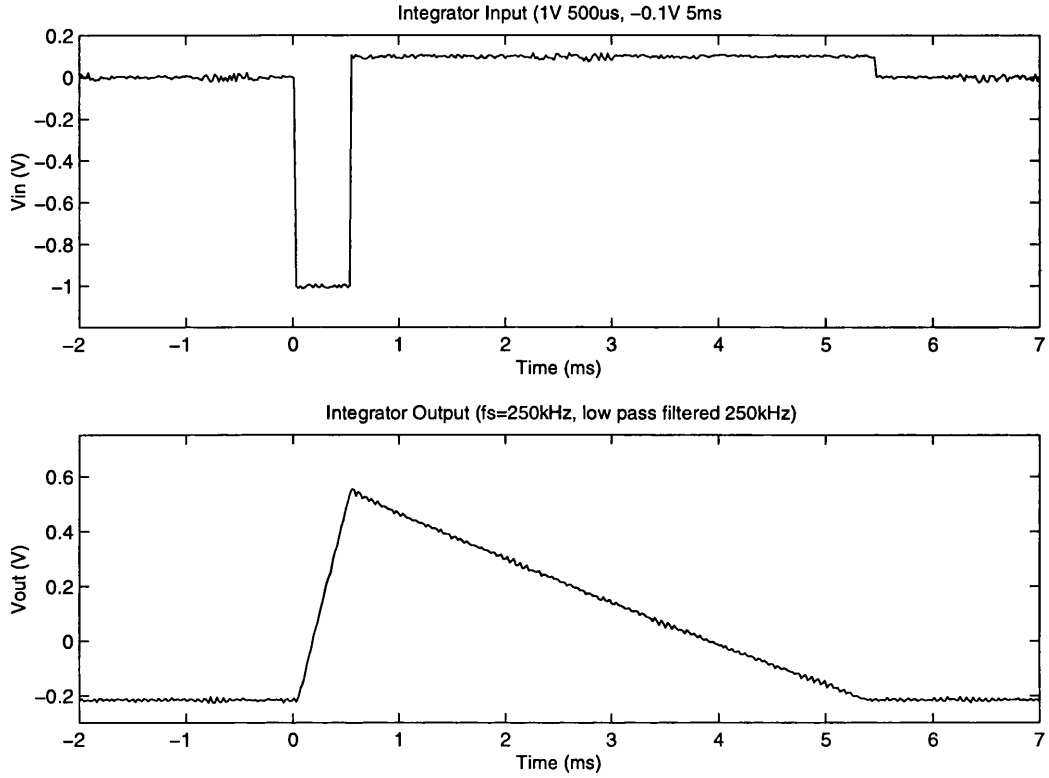


Figure 89. Integrator output for a 1V quasitrapezoidal input (fs=250kHz, filtered at 250kHz)

4.7.5.3 Integrator Switching Transients

Figure 90 shows the switching transients observed at the output of the integrator (fs=200kHz) for a 0V DC input. The observed transients are approximately 100mV peak to peak and of duration 100ns. These transients could cause false triggering of the comparator connected to the output of the integrator, either i) the comparator response is slower than ~ 200ns for a 100mV input or ii) the output of the integrator is low pass filtered to remove these spikes. The option of using a slower comparator is desirable as it is simpler to implement and requires less additional circuitry.

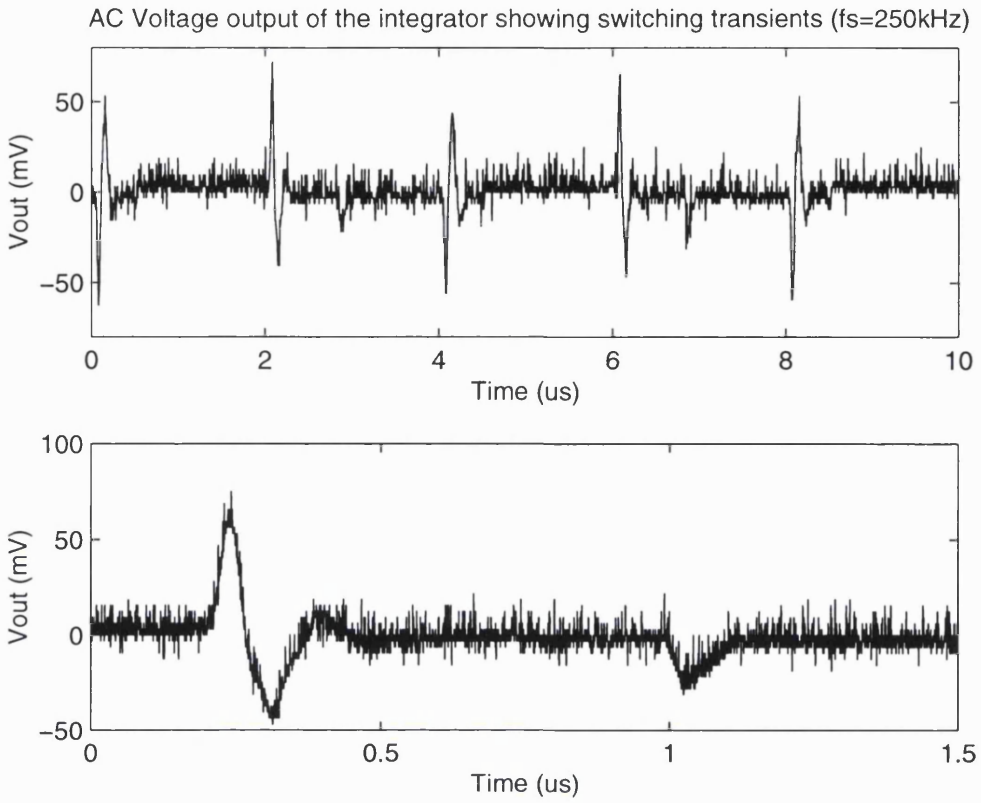


Figure 90. Integrator switching transients (AC coupled, fs=200kHz)

4.7.5.4 Integrator Output Offset Voltage

As described in 4.7.4.2, the output offset of the integrator was larger than initially expected. This was due to the sensitivity of some nodes inside the integrator to charge injection. Table 42 compares the theoretical and experimental output offset voltage of the integrator. As the table shows, the offset of the integrator is too high to meet the specification, however, with the additional dummy switches (for S1-S4) the specification can be met.

Table 42. Experimental DC output offset voltage

Simulated Offset Voltage	Experimental Offset Voltage[46]	
	Range	Mean
235mV	210mV to 250mV	227mV

[46] Measured in 6 Integrated Circuits, fs=250kHz

4.7.5.5 Experimental Results from the Integrator Amplifier

The integrator amplifier was tested using the test arrangements shown in Appendix 1. Table 43 shows the simulated and experimental results for five amplifiers.

Table 43 . Characteristics of the folded cascode integrator amplifier

Measurement	Simulated Range	Experimental Value
DC Gain	82.7dB to 87.5dB	83.7dB ± 0.3dB
Input offset voltage	0.32mV to 0.62mV	0.3mV± 0.4mV
Slew Rate[47]	4.6V/μs to 7V/μs	5.6 V/μS ± 0.4V/μs
Power Consumption (±5V)	2.0mW to 2.3mW	2.2mW
Common mode rejection ratio (CMRR)	-67.8dB to -74.1dB	-75dB ± -0.8dB
Unity gain bandwidth	4.81MHz to 9.44MHz	6.1MHz ± 0.3MHz
Output Voltage Range	-2.7V to –3.1V +3.7V to +4.2V	-2.9V ± 0.2V +4.0V ± 0.2V

All of the measurements fall inside the expected range of simulated results except for the CMRR, which is slightly better than the simulated range. The input offset voltage of the amplifier is particularly good considering the large variation in input offset voltage exhibited by the amplifier used for the attenuators, this is probable due to the use of dummy transistors and common centroid layout arrangement used for the input transistors of this amplifier.

The experimental results for the amplifier all lie within the specification given in 4.7.3.6.

[47] CL=7pF

4.7.6 Conclusions

A comparison of the integrator specification and experimental results is given in Table 44. The integrator on the integrated circuits meets the specification given in 4.7.2, with the exception of the DC output offset.

Table 44. Long time-constant integrator specification

Parameter	Specification	Experiment Value	
		(fs= 200kHz)	(fs= 250kHz)
Time Constant (τ)	$\geq$ 1ms	1.25ms ± 0.07ms	1.01ms ± 0.07ms
Maximum Operating Frequency	$\geq$ 100kHz	100kHz	125kHz
Maximum Charge Balancing Error[48]	$\leq$ 5%	4.4%	4.1%
DC Output Offset	< 20mV	227mV ± 23mV	
DC Output Offset with dummy switches	< 20mV	7mV (simulated)	
External Components	None	None	

A long time constant integrator has being developed based on a design proposed by Sansen and van Petegham that is very area efficient compared to the other types of integrated integrator considered. The Sansen and van Petegham design has been modified to produce an integrator with a high (30dB) DC gain and low output offset voltage. The larger than expected experimental offset in the integrator was due to the lack of dummy switches on some charge sensitive nodes inside the integrator. The cause of this large offset was found to be due to charge injection, this can be corrected by the use of dummy switches. The simulated response with dummy transistors shows the offset can be reduced significantly to make the circuit meet the specification.

The area occupied by the capacitors in the T-Cell integrator is only 30% of the estimated required area for a classical switched capacitor integrator with the same time constant. Using the T-Cell, the capacitance spread is reduced from 200:1 to 15:1. The DC feedback method discussed defines the DC gain of the integrator, making the circuit stable.

The factors that limit the accuracy of this integrator are i) offset and ii) number of samples per stimulation pulse. The effect of the offset is reduced using correlated double sampling. As the integrator realised did not have dummy switches the offset of the integrator was too large, the simulation results show that this offset voltage can be significantly reduced using dummy switches so the specification can be met. The number of samples per stimulation pulse means that for longer stimulation pulses the integrator will be more accurate. This is exactly what is required as the net charge injected during a short stimulation pulse is small and so a larger percentage error is not as important as the passive discharge array will remove any charge imbalance. The worst-case charge error has been simulated as 0.25% for a maximal amplitude and duration stimulation pulse.

[48] Maximum deviation at the end of a stimulation pulse from ideal

4.8 Power Consumption of the Implant Circuits

The current consumption for the individual integrated circuits was simulated and the total current consumed for the different circuits on each integrated circuit was measured experimentally, the power consumption for each circuit is shown in Table 45 .

Table 45. Simulated and experimental power consumption for an implant

Circuit	Simulated Range	Experimental Range[49]
Pulse Generator	310μA-365μA	320μA-340μA
Attenuators (4)	995μA-1230μA	1025μA-1160μA
DAC	55μA-70μA	60μA-65μA
Switching and Discharge Arrays	0μA	0μA
Transconductors (4)	2000μA-2480μA	2000μA-2720μA
Integrator	190μA-235μA	200μA-220μA
Total	3550μA-4380μA	3660μA-4505μA

From Table 45 it can be shown that the total theoretical current for an implant based on these circuits is 3550μA-4380μA and 3660μA-4505μA experimentally, both the simulated and experimental total current consumptions meet the specification given in 3.9.

4.9 Simulation Results for a Complete Stimulator

The behaviour of the complete stimulator constructed from the circuits described was performed.

Figure 49 shows an annotated simulation run of a complete stimulation unit. The output currents are shown for a pentapole and three different stimulation pulse amplitudes. The total charge injected is also shown at the base of the figure.

[49] Measured in 5 integrated circuits

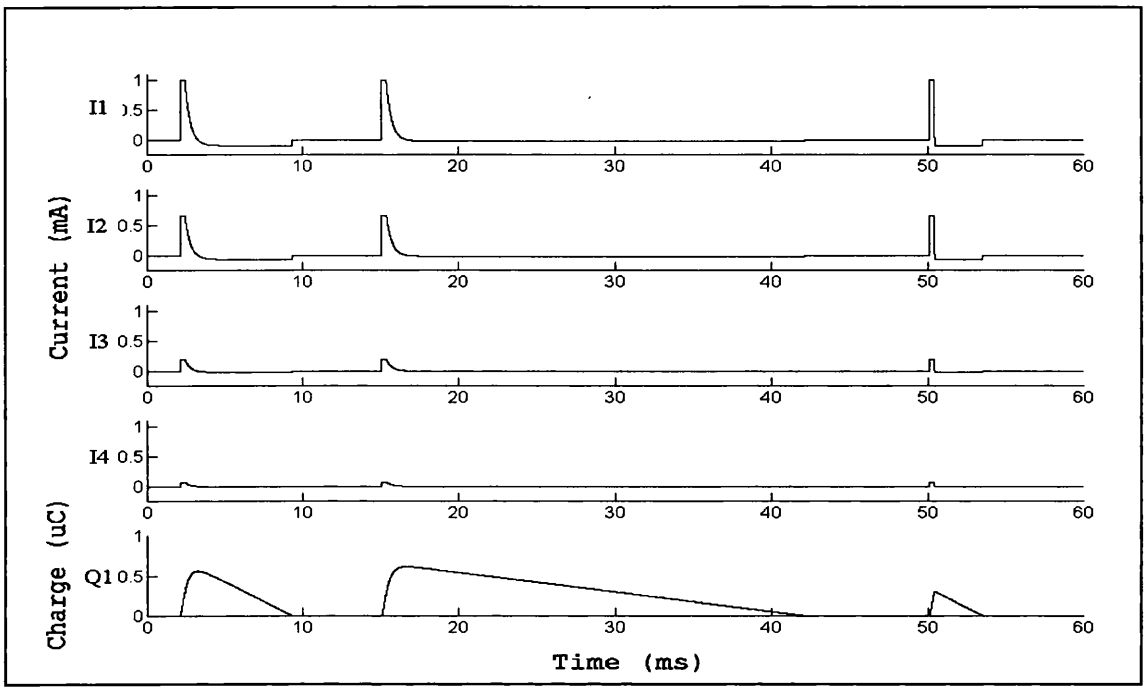


Figure 91. Output of the stimulator in pentapolar mode, I1=1mA, I2=2/3mA I1, I3=1/3mA I1, I4=1/15mA I1, (two quasitrapezoidal pulses of differing reverese amplitude and a square pulse shown)

The simulated results for the complete simulation unit (with the modifications discussed) showed that the device performed to the initial specification described in chapter 3 as was expected from the specifications drawn up for each individual circuit. The total offset current at the transconductor output was shown always be less than 5μA in simulation, a level that is unlikely to cause problems when the charge balancing of the discharge array is taken into account. Taking into account that every circuit meets it specification (after some modifications) this means a complete device should perform

4.10 Experimental Results for the Stimulator

Due to the stability problem of the transconductor it was not possible to evaluate the complete stimulator with these circuits, however using a later stimulator device (not discussed in this thesis it was possible to demonstrate the blocks functioning together to form a complete stimualtor device. The waveforms inside the stimulator are shown in Figure 92.

The timing signal *pw* shown in Figure 92 defines the platuea duration of the stimulation and is generated externally, the signal *zero* should be generated by the integrator, however due to the offset problem the signal shown was generated by an external integrator circuit. The bias conditions of this device are slightly different to the conditions discussed in the rest of this chapter, the quiecent current of all the amplifiers

is lower and the characteristics of the attenuator amplifier have beign improved (offset, gain, quiecent current), due to their relatively large proportion of the total power consumption (4.8). The DC offset current of channel one was found experimentally to be 1μA to 3μA.

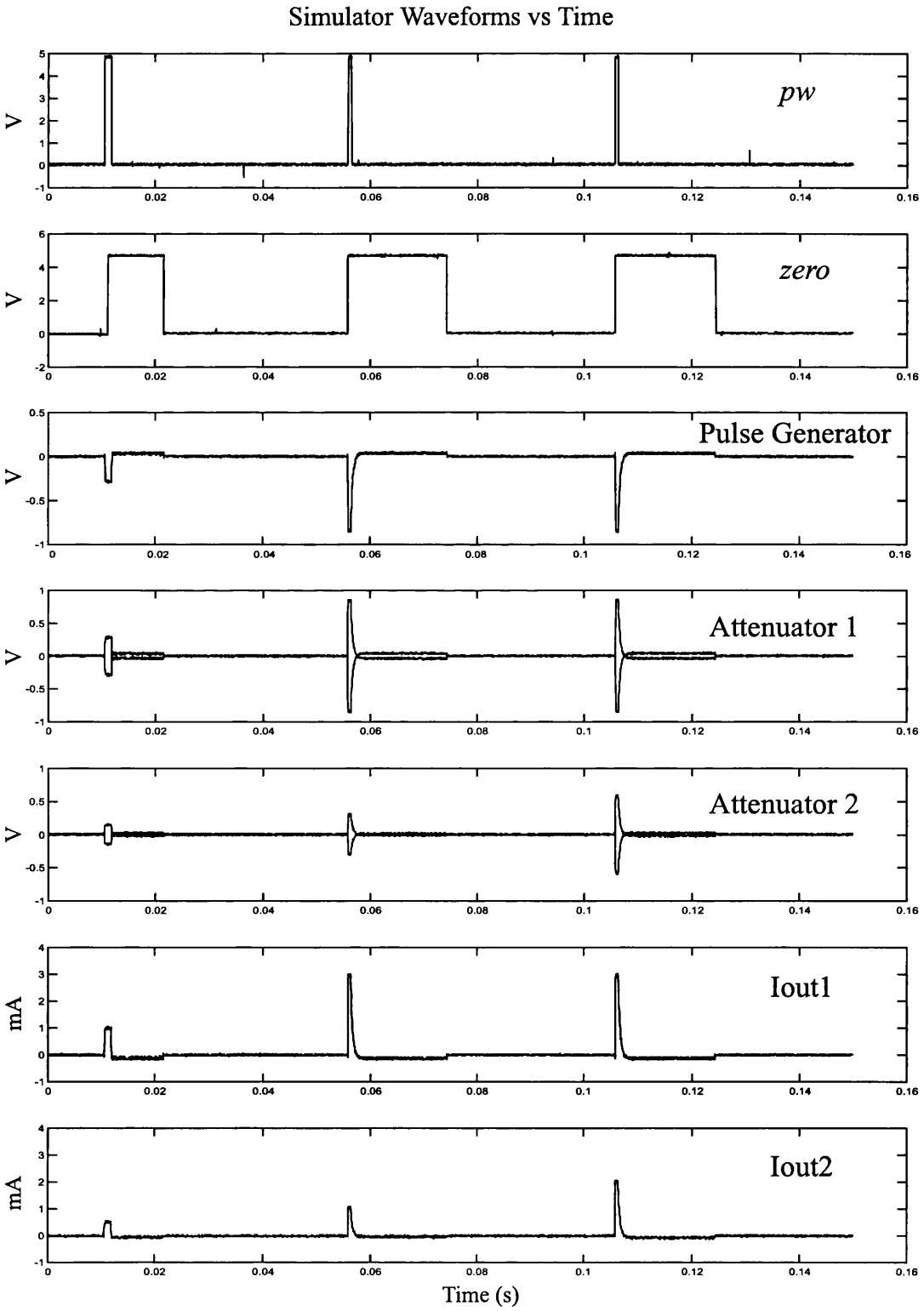


Figure 92.Experimental stimulator waveforms (tripolar) from top to bottom showing: pw, zero, pulse generator output, attenuators 1 and 2 (positive and negative outputs) and finally output currents from the transconductor

4.11 Effect of Offset

The effect of an offset current on the stimulators performance requires some consideration. The charge offset for the stimulator can simply be defined at the offset current multiplied by the stimulation duration. For a maximal stimulation pulse of 5mA, 1ms with a reverse phase of 1/47 (2%) the charge error will be approximately 4% (220nC). This excess charge has to be removed by the switching array. If a 0.5mA, 1ms, 1/47 stimulation pulse were generated the charge error would be 45%. This is obviously too large, however, a more sensible reverse phase amplitude would be 1/6.7 (Ar<100μA), where the error would be reduced to 30nC or 6%.

This consideration of error means that the reverse amplitude should be kept as large as possible (whilst avoiding erroneous stimulation) too keep the effect of offset minimised and maintain reasonable charge balancing.

4.11 Summary

The modules discussed in this chapter demonstrated that the development of a CMOS based integrated circuit for selective stimulation of nerves is feasible. The modules were fabricated on three ICs, altogether occupying more than 35mm^2 of silicon.

A novel transconductance circuit has being developed that allows ±5mA current pulses to be generated with loads approaching 1kΩ impedance using ±5V power supplies. The experimental results for the transconductor highlighted a problem with the common-mode feedback causing instability. However, it was demonstrated that by modifying the common-mode feedback arrangement that this problem could be solved. The modified transconductor demonstrated that a high transconductance linear transconductor could be realised with a non-linearity at higher currents (4mA) of below 1.5%, even when the process parameters vary by 10%. The transconductors simulated and experimental characteristics allow the stimulator specification given in section 3.9 to be met.

A long time constant integrator (τ=1ms, fs=250kHz) has being developed that is very area-efficient compared to other types of integrator investigated; requiring only 30% of the area required by a classical switched capacitor integrator with the same time constant. This circuit was a development of a low gain integrator proposed by Sansen and van Peteghem [125,147]. Using this implementation, the capacitance spread is

reduced from 200:1 to 15:1, making the circuit realisation and capacitor matching easier. The DC feedback method discussed defines the DC gain of the integrator, making the circuit stable and allows the low frequency gain of the integrator to be simply defined. The analysis shown for this circuit developed simple equations for both the time constant and the gain of this integrator. The experimental results from this circuit highlighted a problem with charge injection sensitivity in some of the input nodes of the circuit. The solution to this problem was shown to be to use dummy switches to cancel the charge injection in the critical nodes. With the proposed modifications the DC offset voltage of the integrator was reduced from an experimental (and later simulated) offset of 227mV to a simulated offset of around 7mV.

The pulse generator produces waveforms either quasi-trapezoidal shaped or square shaped. The time constant for the quasi-trapezoidal waveforms is defined by two external components. The experimental results agreed well with the simulated results, but highlighted that amplifier offset limits the accuracy of the reverse phase, leading to a minimum reverse current of 111μA when using a 5mA stimulation pulse. Whether this 10% increase over the 100μA limit suggested as suitable by Fang and Mortimer [144] is still acceptable is not known as most authors have used either monophasic stimulation pulses [21,22,39,110-118,135,136,141,142] (or not discussed the amplitude of this reverse current). The developed pulse generator allows the specification for the stimulator to be met.

The DAC, Switching Array, Discharge Array and the Attenuators exhibited good agreement between the experimental and theoretical results. All of these circuits allow the stimulator specification to be achieved.

The total power consumed by all of the circuits was smaller than the limit imposed by the specification, however in a real implant this situation can be significantly improved by reducing the biasing currents to the amplifiers and transconductors when the implant in not actively stimulating.

A discussion of how the offsets of the individual circuits affect the overall performance of the system is given in the summary in Chapter 6.

Overall, the design presented was suitable for integrated circuit techniques, except for the external capacitor and resistor required by the pulse generation circuit.

Chapter 5. Applications and Future Work

This chapter firstly proposes some specific applications for a selective stimulator and secondly details the developments needed to turn the previously discussed integrated circuits into a complete selective stimulator system.

5.1 Proposed Applications

5.1.1 Improved Implantable Bladder and Bowel Stimulator

Persons who sustain spinal cord injury (SCI) are frequently left paralysed and wheelchair bound. What is less immediately obvious is that they invariably lose voluntary control over their bladder and bowel functions as well. Persistent urinary tract infections, often requiring hospital treatment, are common among this group who most-often use catheters for bladder emptying [18,20].

It is possible to electrically stimulate the nerves which normally control the bladder and bowel to restore effective micturation and in some cases defecation. Over 1500 of the Finetech – Brindley stimulators for this purpose were implanted by the end of 1997 [2][50]. The surgical procedure involves cutting the sacral posterior nerve roots (*rhizotomy*) to prevent unwanted reflex bladder contractions (*hyper-reflexia*) and attaching electrodes to the sacral anterior roots S2-S4 (trapped in pairs) to allow simulation of the muscles [14,16,23]. The device itself consists of three RF tuned receivers and is constructed with simple discrete components. However, due to the simplicity of the circuitry, the control of amplitude is fairly crude and there is no direct control over the level of the stimulation *current* and only poor control of the *waveform shape.*

A drawback of conventional sacral anterior root stimulation is the simultaneous contraction of the urethral sphincter muscle that closes the urethra and the detrusor muscle of the bladder wall. Figure 93 shows the innervation of the bladder and bowel from the spinal roots in man, this figure shows that both the bladder and bowel are innervated by the same spinal sacral roots (S2-S4), theoretically allowing one implanted stimulator to activate both organs.

[50] A second device from Medtronic Inc is now also available

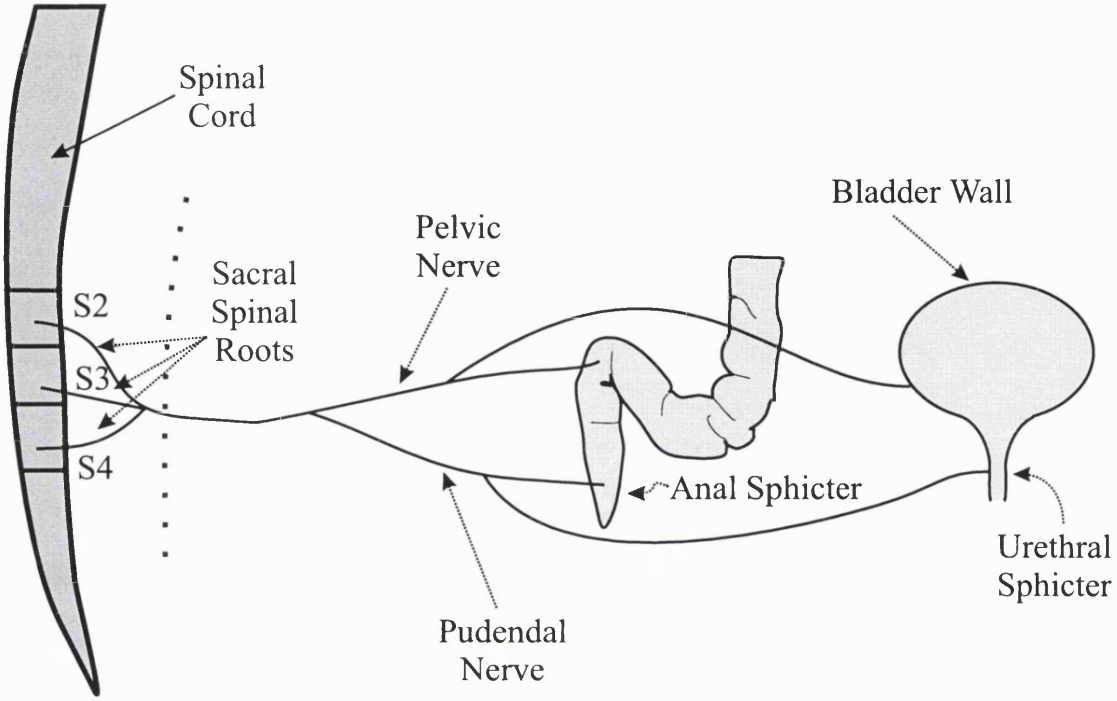


Figure 93. Innervation of the bladder and bowel from the sacral roots

In the bladder the sphincter muscle is innervated by large-diameter fibres and the detrusor muscle is innervated by small diameter nerve fibres in the same roots [114,117]. Hence, during conventional stimulation with rectangular pulses, the sphincter contracts at a lower threshold than the bladder wall which, if the stimulation is continuous, leads to supra-normal bladder pressures and incomplete emptying. *Post stimulus voiding* is the technique normally used to get around this problem [10,16,23,24,117,119,146]. It relies on the fact that the urethral sphincter muscle relaxes faster than the detrusor muscle, so that, if bursts of stimulation are applied, bladder emptying occurs during the periods of urethral sphincter relaxation between stimulation bursts.

Although the Finetech-Brindley stimulator has proved to be highly effective for bladder control and reliable, the use of the methods described in this thesis would allow several improvements. These improvements are listed below.

5.1.1.1 Selectivity

Only 50% of subjects with a Brindley implant defecate more easily using the stimulator alone [16,39]. The problem is analogous to bladder emptying: stimulation of the nerve roots produces contraction of the external anal sphincter and contraction of the distal colon and rectum, which does not easily tend to empty bowels. For the bowel, even

with the best stimulation adjustments, post-stimulus voiding is less effective than for bladder emptying. The ability to stimulate small nerve fibres within a nerve root, without stimulating the large ones (which would normally have a lower threshold), should allow stimulation of the rectum without closing the anal sphincter; and this should significantly improve bowel emptying. Also decreased bladder pressures during voiding may also be possible by selectively stimulating only the detrusor muscle of the bladder wall [112,116-118].

5.1.1.2 Uni-directional stimulation

As both the fibres innervating the detrusor and the pain fibres are small diameter, the ability to stimulate fibres in one direction only would be highly advantageous. This would greatly increase the potential market size because the device would become suitable for patients with *incomplete* SCI who retain pain sensitivity.

5.1.1.3 Neuromodulation

Neuromodulation may remove the need to perform the rhizotomy. A rhizotomy is inappropriate for patients with *incomplete* SCI, due to the associated loss of sensation, and even for patients with complete SCI, it is unacceptable to some clinicians and patients as it results in the loss of reflex erection for men, and is a destructive procedure. Neuromodulation may be used if it can suppress spontaneous bladder contractions by applying continuous low-level stimulation to the sensory nerves [37].

A stimulator device for improved bladder and bowel control would have six tripolar electrode cuffs, to allow selective stimulation of the S2-S4 roots, preferably with the electrodes placed extra-dural, to avoid the associated risks and costs of spinal cord surgery.

5.1.2 Implantable Foot Drop Stimulator

Hemiplegic stroke patients often suffer with a condition known as 'foot drop'. This is where, during the swing phase of gait, the ankle does not dorsiflex, causing the foot to impede locomotion. If not corrected by an orthosis, the problem is sometimes addressed with an external FNS system that stimulates the common peroneal nerve to lift the foot during the swing phase. A pair of electrodes are attached to the skin below and slightly lateral to the patella. Peroneal stimulators are usually arranged with an external heel pressure switch, which detects when the heel is lifted from the floor, and turns on

the stimulator for a fixed period to dorsiflex the ankle [84]. However, while these systems often are useful and sometimes seem to cause a recovery of the natural dorsiflexion, they are sometimes rejected by the patients or found difficult to use because the placement of the electrodes is too difficult. A significant number of users also suffer some allergic reaction to the electrodes on the skin [137].

Implanted common peroneal stimulators have being used to simplify the set-up time and donning of the stimulators, however one problem encountered is excessive inversion or eversion of the foot during stimulation [154,155]. Normally four muscles innervated by the peroneal nerve act synergistically to dorsiflex the foot. However during stimulation of the peroneal nerve, with a single nerve electrode, no adjustment is possible and there may be excessive eversion or inversion. Several authors have shown that balanced dorsiflexion can be obtained using multipolar nerve cuffs [72,88,150] placed acutely on the peroneal nerve to stimulate the fascicles innervating the individual muscles. Using our pentapolar nerve cuff it should be possible to obtain balanced dorsiflexion by balanced stimulation of fascicles inside the peroneal nerve which innervates inverters and everters.

During 1992 Kljajic [81] reported on the follow-up of 35 patients with peroneal stimulators. Of those who had stopped using the implant, four patients reported that unpleasant sensation during stimulation was the primary cause. If it was possible to combine selective stimulation by geometrical position with unidirectional propagation using quasi-trapezoidal pulses, this problem could be addressed. No studies to date have investigated this possibility.

5.2 A Complete Selective Stimulator System

The testing and simulation results from the ICs SSTIM1-SSTIM3 presented in Chapter 4, showed that, with the modifications discussed, the developed circuits are suitable for use in a selective stimulator system. An overview of the proposed stimulator system, based around the developed circuits, is discussed in this section. This system shares many of the characteristics of the LARSI device [44], however several modifications and improvements have been introduced. Figure 94 shows a block diagram of the complete system, which comprises three main sections.

1. Implanted Device (internal)
2. Control Box (external)
3. Radio-frequency transmitter (external)

The implanted device can be separated into three sections:

4. Stimulation Unit
5. Digital Control Unit
6. Discrete Circuitry

5.2.1 Overview of a Complete Stimulator

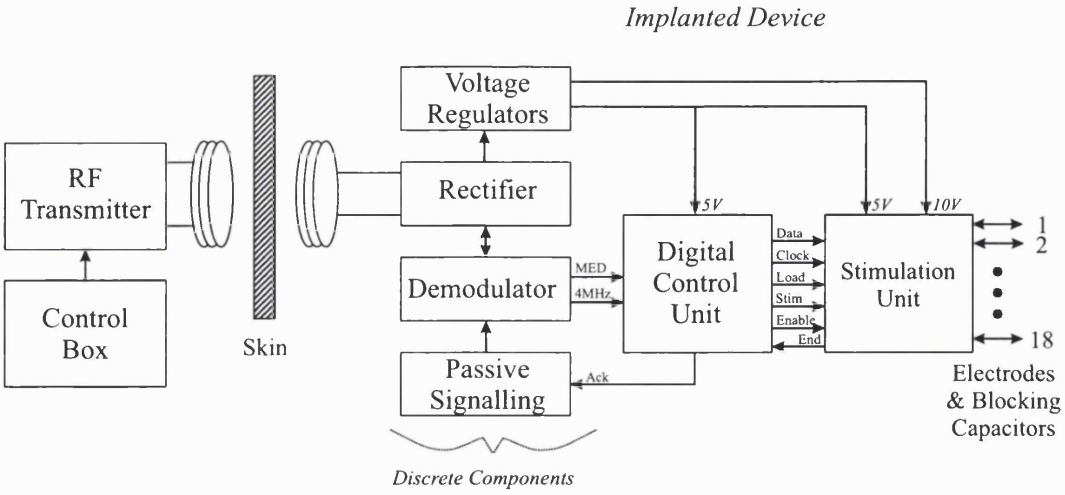


Figure 94. Overview of a selective stimulator system

The implanted system shown in Figure 94 consists of the devices discussed in the previous section. Inside the implant, the Stimulation Unit (SU) generates the stimulation waveforms and applies them to the electrodes. The Digital Control Unit (DCU) provides all the timing and control signals to the SU and generates the handshaking signals for the external controller. The discrete components are used for the high voltage sections of the implant (power generation, demodulation and passive signalling), and also for the blocking capacitors.

The system operates as follows: The external control box generates the binary word that describes the stimulation parameters and modulates the carrier in a tuned radio frequency transmitter circuit. A second tuned circuit in the implant receives this amplitude modulated carrier. The carrier is rectified to supply implant power. The carrier is also demodulated to recover the binary word, the DCU then checks that the received data is not corrupted. The DCU then generates all of the control and timing signals required by the Stimulation Unit (SU), which contains the circuits discussed in Chapter 3. The SU generates the stimulation pulses and multiplexes the signals to the attached nerve cuff electrodes via blocking capacitors. The SU informs the DCU when the stimulation pulse has finished; the DCU then signals the external control box via passive signalling components that the next stimulation pulse is ready to be received.

5.2.2 Implant Data

For every stimulation pulse, the DCU has to receive a valid words from the external controller. Every data set consists of 44 data bits and 16 parity bits (Hamming Encoded) for error detection. Four bits have been set aside for future applications. This brings the total number of required bits to 60 for every stimulation pulse. Table 46 shows the bit meanings for the data word.

Table 46. Implant Data

Data	Parameter	Description
D0-D7	Pulse Amplitude	8-bit word that defines the Pulse Amplitude (Af)
D8-D11	Cuff Number	Defines which cuff the switching array selects
D12	Tail	Turns the exponential tail ON/OFF
D13-D15	Reverse Amplitude	Defines the ratio of the Reverse Amplitude (Ar) to the Pulse Amplitude (Af)
D16	Reserved	
D17-D32	Attenuators Gain	Sets the attenuation of attenuators 1-4
D33	Coupling	Disconnects the stimulator from the power coil to allow a coupling measurement
D34-D36	Reserved	
D37-D43	Pulse Duration	Defines the pulse duration from 8μs to 1016μs

Figure 95 shows the timing of signals inside the implant during normal operation. RF represents the transmitted RF carrier signal, *clock* is the data clock recovered from the received data by the DCU. C_{up} is the internal signal generated by the DCU when the voltage on the storage capacitor is high enough to begin stimulation. *POWER* is the signal used to power up the SU. *LOAD* tells the SU that the data from the DCU should be loaded. *PW* is the duration of stimulation generated by the DCU and ZERO is the signal the SU generates when the stimulation pulse is charge balanced. There are two types of handshake signal, α and β: these signals are of different durations to allow the external controller to detect the meaning of the signal.

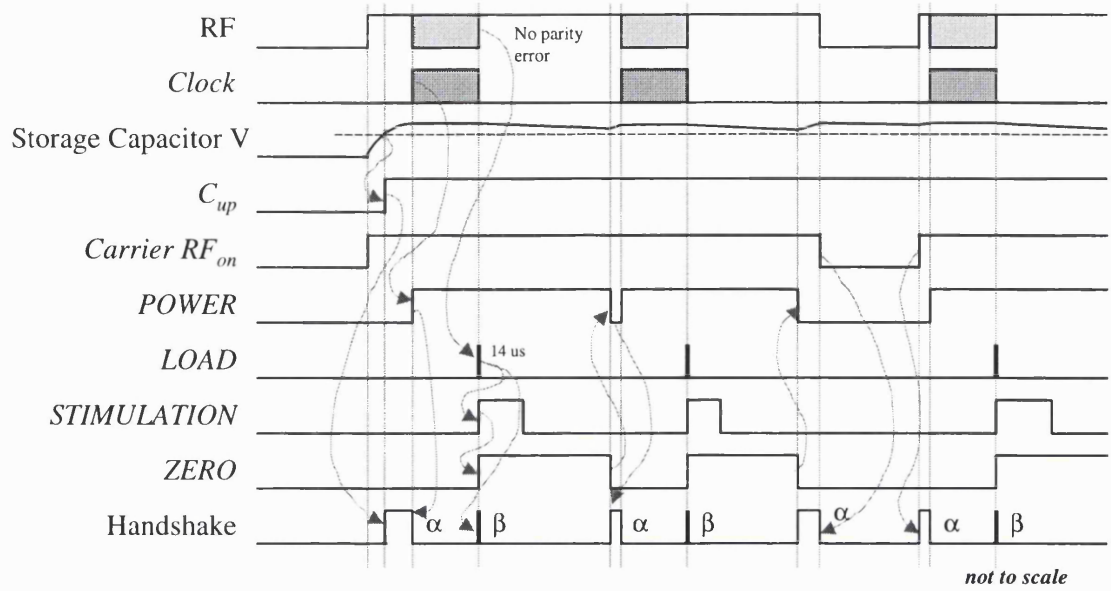


Figure 95. Control signals and handshaking timing diagram

During normal operation, the implant will power up when the RF starts and signals the external controller it is ready to start stimulation with an α handshake when the storage capacitor voltage is sufficiently high. Then the external controller will send the binary word to the implant. If the binary word is valid, a β handshake is sent from the implant to the controller.

The handshaking signals are transmitted to the external controller using passive signalling [43,48]. Passive signalling works by changing the loading on the receiver coil for a short duration, this change in load is detected as a change in current in the transmitter coil.

This data transmission scheme allows the implant to be turned off to save power when not stimulating, simply by turning off the RF carrier (as shown in Figure 95)

5.2.3 Stimulation Unit

The specification for the complete SU is the same as the specification given in Chapter 3 with one modification: the number of cuffs the device can control should be increased, so that six tripoles can be controlled (5.1.1), this also allows the device to control three pentapoles or nine dipoles. A flow diagram of the new stimulation unit is given in Figure 96.

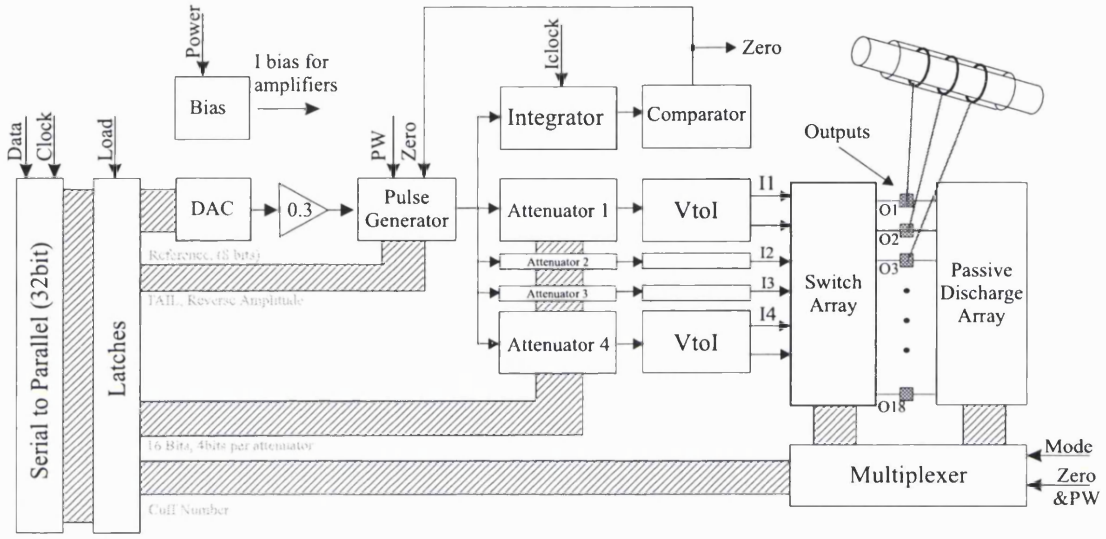


Figure 96. Complete stimulation unit

The new device allows the internal amplifiers to be powered down to 1/4 of their nominal bias current to conserve power when the stimulator is not stimulating. The digital control unit takes the decision to power the stimulation unit down using the power signal.

The digital section of the device contains a shift register to hold the binary word and control logic to control the data lines attached to the switching and discharge arrays. The device requires five signals from the digital control unit: *data, clock, integrator clock, power and pw (pulse duration)* and provides one return signal: *zero* to indicate when the stimulation is completed.

5.2.4 DCU

The DCU has four main functions:

1. Decoding of the received data and error detection
2. Generation of timing waveforms and data for the SU

3. Communication with the external controller (via passive signalling)
4. Monitoring of the implants power supplies.

Figure 97 shows a flow diagram of the DCU.

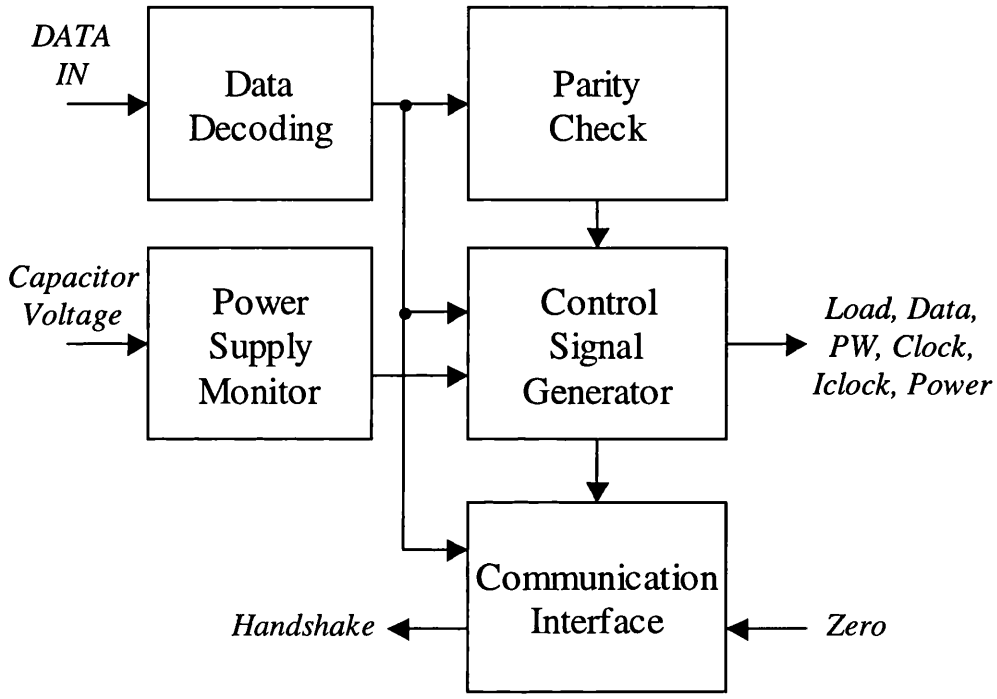


Figure 97. Flow diagram of the Digital Control Unit

The behaviour of each section is discussed in 5.2.4.1- 5.2.4.4.

5.2.4.1 Data Decoding

Data is Hamming and Manchester encoded before being transmitted to the implant. This requires a decoding of the received data in two steps.

The implant operates without a local oscillator (e.g. crystal): an internal clock signal of 83 kHz is generated during Manchester decoding by the decoding logic. This clock is automatically synchronised to the leading falling edge of the data stream. The data is then Hamming decoded, where the parity bits are calculated from the received data and compared to the received parity bits. The SU receives the decoded data, but only initiates the stimulation if the DCU signals an error-free transmission.

5.2.4.2 Control Signals

The DCU generates all of the signals required by the SU, these being, pulse duration (*PW*), data, data clock (*Clock*), data load (*Load*) and the integrator clock (Iclock, fs=250kHz).

The DCU powers up the SU whenever data is received using the 'power' line. Under normal condition, this control line remains HIGH until the SU completes the stimulation. When the stimulation pulse is completed, the SU signals this by sending a 'zero' signal to the DCU, and the DCU powers the SU down. The SU is powered immediately down when a transmission error is detected to conserve internal power.

5.2.4.3 Handshaking

Apart from the communication with the SU, the DCU also produces the handshaking signals discussed in 5.2.2.

5.2.4.4 Power Supply Monitoring

The DCU monitors the internal power supply voltage on the storage capacitor. If this voltage falls the DCU signals the external controller that an error has occurred and a coupling measurement should be performed. The external controller will then increase the power being transmitted to the implant

5.2.5 Implant Schematic

Figure 98 shows a schematic for a stimulator with four tripoles, based around the devices discussed in this chapter, along with the passive components required for both power and data communication.

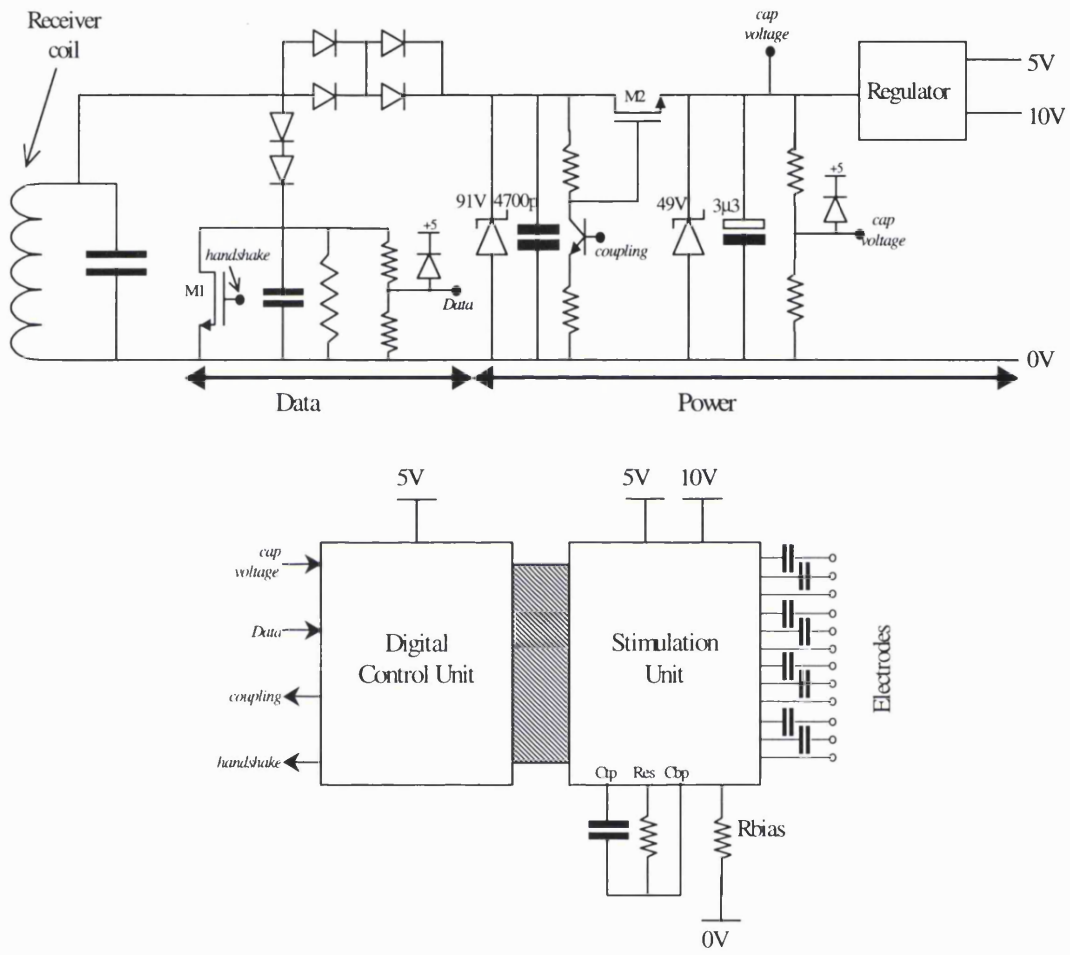


Figure 98. A complete four-channel tripolar selective stimulator

This system will require approximately 30 discrete components (1-coil, 5-capacitors, 3-transistors, 9-resistors, 10 diodes and 2-voltage regulators), plus blocking capacitors (in this example 8).

5.3 Summary

The two specific applications proposed for the selective stimulator system at the beginning of this chapter highlighted the potential benefits of such a system, compared to a conventional implanted stimulator, and show the specific need for such a device.

The work proposed in the rest of the chapter should allow the development of a stimulator suitable for selective stimulation by fibre size and/or selective stimulation by fibre position using implanted nerve electrode cuffs. Some of this proposed development shares characteristics with the LARSI system, reducing the amount of actual development work.

The device should be physically smaller than the LARSI stimulator due to the integration of many of the discrete components used in the LARSI system. This is important as it allows the device to be placed closer to the stimulation site in the case of peripheral nerve stimulation (e.g. An implanted foot drop stimulator).

The future work required to develop a complete selective stimulator system is given below.

1. Production and testing the complete stimulation unit
2. Production and testing of the digital control unit
3. Development of the external controller hardware and software
4. Bench lash-up of the complete implant system
5. Manufacture and population of hybrid circuits
6. Testing of hybrid implant
7. Encapsulation
8. Animal Experimentation
9. Human Trials

Although progress on items 1-5 and 8 has being made[51] [25-27], there still remains a large amount of work to create a system suitable for chronic human investigation of selective stimulation.

[51] As of September 1998

Chapter 6. Summary

The aim of this thesis was to demonstrate the feasibility of producing a selective stimulator using VLSI techniques. Although stimulators have been realised using integrated circuits in the past they have tended to rely on digital electronics to produce the stimulation waveforms. Due to the quasi-trapezoidal stimulation waveforms required for selective stimulation, analogue circuit techniques were deemed more appropriate in this stimulator design. In this study, the modules for a selective stimulator unit were implemented using Mietec 2.4μm CMOS technology. The principle results of the work presented in this thesis will now be summarised and discussed.

Following the general introduction given in Chapter 1, Chapter 2 reviews the history of selective stimulation, discussing the types of waveform and nerve cuffs that have being used for selection by fibre size and selection by fibre position. Conclusions are drawn from the literature and each section ends with a table showing the different methods used for obtaining selective stimulation. This review of selective stimulation methods has not being reported in the literature previously.

Chapter 3 presents the development of the specification for a selective stimulator system. The summaries developed for selective stimulation by fibre size and fibre position were invaluable in the development of the specification for a selective stimulator system. The specification allows the new device to control three different types of nerve electrode cuffs (dipoles, tripoles and pentapoles). The tripoles (and dipoles) are to be used for selection by fibre size. The specification introduces a new cuff design, the pentapole that consists of four central 'dot' electrodes and two anode rings. It is hoped that this cuff design, used with the new stimulator device, will, in practice, allow chronic investigation of selective stimulation by fibre position. The pentapolar electrode cuff may also allow the investigation of selective stimulation by fibre position in conjunction with selective stimulation by fibre size, a technique that has not yet being investigated. However, as the blocking of the nerve fibres occurs at the anodes the design of the nerve cuff may have to be modified to contain a central stimulating cathode and multiple anodes. This possibility will require acute and chronic investigations.

The output currents of the stimulator to each cuff are set as ratios, either of cathode currents in the pentapole or anode currents in the tripole. The specification proposes that the stimulator produce charge-balanced stimulation currents of variable duration,

amplitude, and reverse amplitude with and without an exponential tail. This greatly exceeds the number of parameters controlled by most existing stimulators.

In Chapter 4 the design, fabrication and testing results of the circuits required for a selective stimulator are discussed. The modules were first fabricated on three test ICs, altogether occupying more than $35mm^2$ of silicon.

A novel transconductance circuit is presented that allows ±5mA current pulses to be generated with loads approaching 1kΩ impedance. The simulation results showed that the circuit behaves as a linear transconductor with a variable transconductance defined by a single bias current. The nominal transconductance for the stimulator was 3.5mA/V. The transconductor demonstrated, in simulation, a 1.5% maximal non-linearity (at 4mA) with a 10% mismatch in transistor parameters. This is approximately double the non-linearity demonstrated by the Park and Schumman transconductor [99,100], however the output voltage swing of the developed transconductor is over double that achievable with their circuit. The experimental results highlighted a problem with the common-mode feedback that caused the circuit to behave unstably. This problem was analysed in simulation and a modified feedback scheme was proposed. The modified feedback scheme was implemented in a later integrated circuit and allowed the transconductor to operate stably. The offset of the developed differential transconductor was shown in simulation to be close to zero. The effective differential offset of this device is defined by the differential offset presented at its inputs (ref to section).

A long time constant integrator (τ=1ms, fs=250kHz) has been developed that is very area-efficient compared to other types of integrator investigated; requiring only 30% of the area required by a classical switched capacitor integrator with the same time constant. This circuit was a development of a low gain integrator proposed by Sansen and van Peteghem [125,147]. The capacitance spread is reduced from 200:1 to 15:1, making the circuit realisation and capacitor matching easier. The DC feedback method presented allows the low frequency gain of the integrator to be simply defined. The analysis shown for this circuit developed simple equations for both the time constant and the gain of this integrator. The experimental results from this circuit highlighted a problem with charge injection sensitivity in some of the input nodes of the circuit. The solution to this problem is to use dummy switches to cancel the charge injection in the critical nodes. With the proposed modifications, the DC offset voltage of the integrator was reduced

from an experimental (and later simulated) offset of 227mV to a simulated offset of around 7mV.

A pulse-generator circuit, capable of generating the waveform shapes required for selective stimulation of definable amplitude, duration, reverse amplitude and tail shape was developed. The circuits performance was shown to meet the specification developed for the circuit with the exception that the reverse amplitude ratio was slightly too low at the smallest ratios (2%). This should be corrected in future devices.

The other circuits for the stimulator unit all functioned within the expected tolerances when tested. Overall, the design presented was suitable for integrated circuit techniques, except for the external capacitor and resistor required by the pulse generation circuit. Two external components for the whole stimulation unit is acceptable when compared with the fact that every stimulating electrode requires a blocking capacitor of several μF, each of which will be of a volume comparable to the IC.

The overall offset needs careful consideration in a complete stimulator system. Because negligible offset is due to the transconductors (see above), the effective offset at the output is the transconductance multiplied by differential offset voltage *presented to* the transconductors. This offset voltage is effectively (V_{offset} (DAC) + V_{offset} (Pulse-Generator). + $V_{offset(differential)}$ (Attenuators)). The *experimental* results presented in 4.10 showed that this offset voltage will be below 5μA when the proposed improvements to reduce the offset of the attenuator amplifiers have been implemented. This equates to a maximal charge error[52] of 4% (0.2μC) of the maximal pulse charge. This charge has to be removed by the discharge array. Future designs may consider the addition of offset correction at the transconductor outputs to improve the overall accuracy of the charge balancing.

Chapter 5 firstly proposes applications for the stimulator; these applications include an improved stimulator for bladder and bowel and a foot-drop stimulator. The ability to generate unidirectionally-propagating action potentials should allow the device to be used with a larger group of patients. Secondly, Chapter 5 discusses the work required to turn the test devices, discussed in Chapter 4, into a complete selective stimulator system. This system has a minimal number of internal components: voltage regulators, handshaking transistors, an RF filter (to extract the transmitted data and power), a digital control IC, a stimulation unit, blocking capacitors plus a few other discrete components.

This minimal number of components means that the stimulator can be physically small, allowing the device to be placed closer to the stimulation site.

In conclusion this thesis presents the development of a stimulation IC, which, when incorporated into a complete stimulator system, will allow selective stimulation techniques to be investigate in chronic human clinical trials.

The claims of this thesis are as follows.

1. A detailed literature review of selective stimulation using implanted nerve cuff electrodes was presented and summaries of both stimulation methods were presented. This detailed review has not appeared in the literature before.
2. A specification for a selective stimulator was developed from the information generated by the literature review. The specification allows control of pulse amplitude, duration, reverse current amplitude and tail time-constant.
3. Circuits suitable for a selective stimulator were developed, simulated, and tested experimentally. Where necessary improvements to the realised designs have been proposed. The circuits developed for the stimulator are listed in 4-9.
4. An 8-bit DAC based mostly on standard cells.
5. A pulse-generator circuit, capable of generating the waveform shapes required for selective stimulation of definable amplitude, duration, reverse amplitude and tail shape.
6. A four-channel, single-sided to differential attenuator.
7. A novel linear differential transconductor capable of delivering ± 5mA into a 1 kohm load with a low offset current and using only ± 5V power supplies. The offset of the transconductor is effective defined by differential offset voltages presented at the input of the transconductor.
8. Area efficient switching and discharge switching arrays.
9. A long time-constant integrator with increased DC gain has beenn developed from a design proposed by Sansen and van Petegham. The circuit has being simulated, analysed and further improvements suggested.
10. The overall performance of the circuits (with some modifications) will allow a complete stimulator system to be developed using these designs.

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[52] Maximal error occurs for a 5mA, 1ms pulse with a 2% reverse amplitude

11. Applications for the stimulator have being proposed.
12. The developments required to produce a complete stimulator system have being discussed.

Appendix 1. Testing of the Integrated Circuits

This appendix is organised into three sections

1. Partitioning of the Integrated Circuits
2. Amplifier testing configurations
3. Test PCBs and schematics

A1.1. Partitioning of the Integrated Circuits

This section describes the partitioning of the circuits described in chapter 4 onto three integrated circuits for testing. Table 47 shows the partitioning of the circuits on the Integrated Circuits SSTIM1, SSTIM2 and SSTIM3 along with the various test amplifiers.

Table 47. Partitioning of the integrated circuits SSTIM1, SSTIM2, SSTIM3

Integrated Circuit	Circuits
SSTIM1	Attenuators Pulse Generator
SSTIM2	Switching Array Discharge Array DAC DAC test amplifier
SSTIM3	Transconductors Common mode feedback Integrator Integrator test buffer Attenuator test amplifier Pulse Generator test amplifier Integrator test amplifier

It was decided to place the modules on three separate IC's. The reasoning for this was two fold, i) A single failure (due to a layout error or design mistake) of one module

could prevent the testing of all of the other modules, ii) More pads per mm2 of silicon allowing more internal nodes to be examined.

SSTIM1 and SSTIM2 contained the circuits whose simulated and theoretical behaviour was expected to be similar to the experimental behaviour. SSTIM3 contained both of the circuits whose behaviour was in the most doubt (the Integrator and Transconductors), as well as most of the test amplifiers used in other circuits. This was to allow simpler resubmission of the circuits if required.

Figure 99 to Figure 104 give the pin-outs, floor-plans, and the chip photographs of the fabricated ICs SSTIM1-SSTIM3.

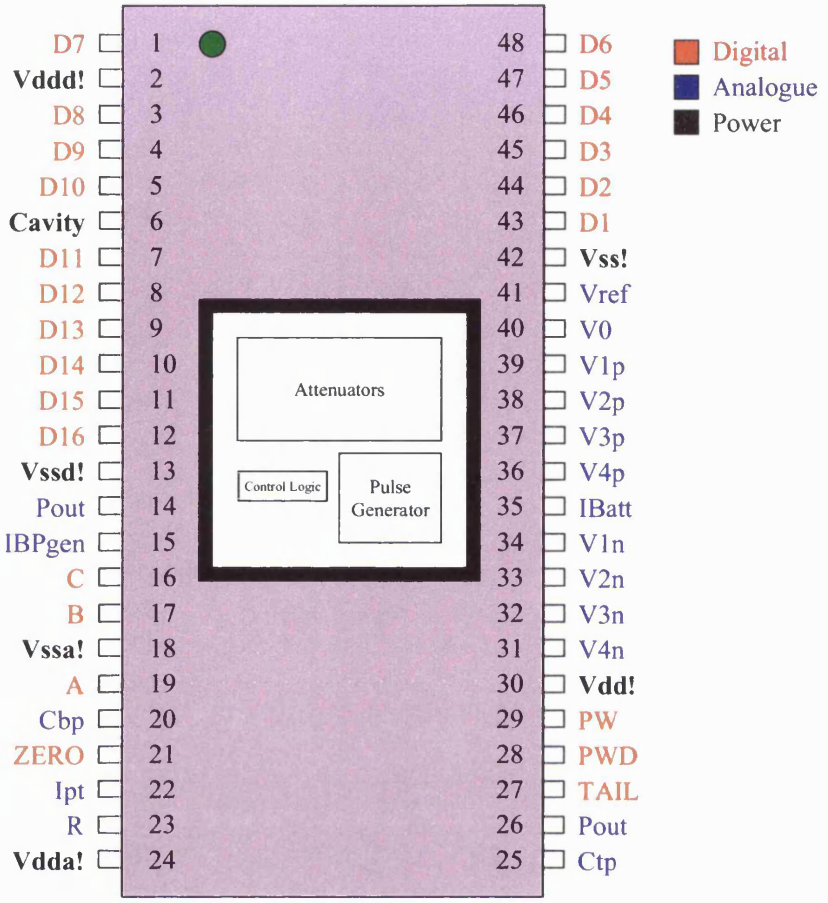

Figure 99. Pinout and floor plan of IC SSTIM1

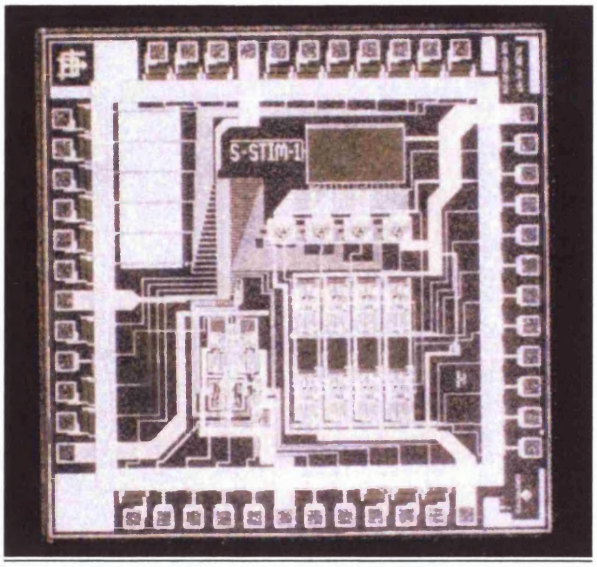

Figure 100. Photograph of IC SSTIM1

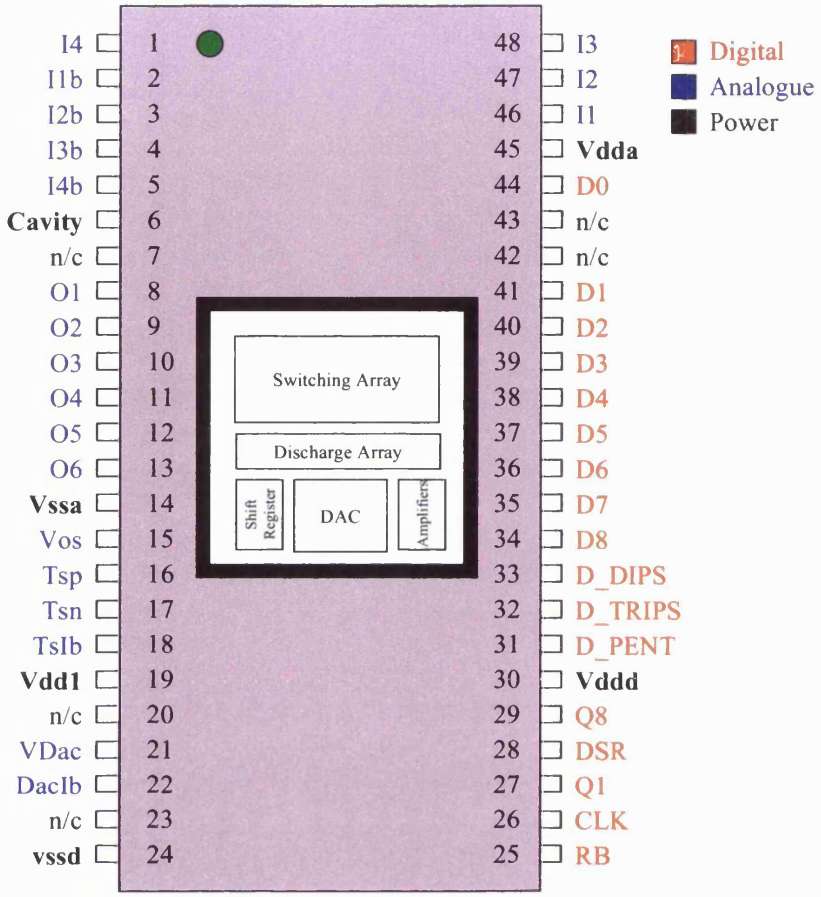

Figure 101. Pinout and floorplan of IC SSTIM2

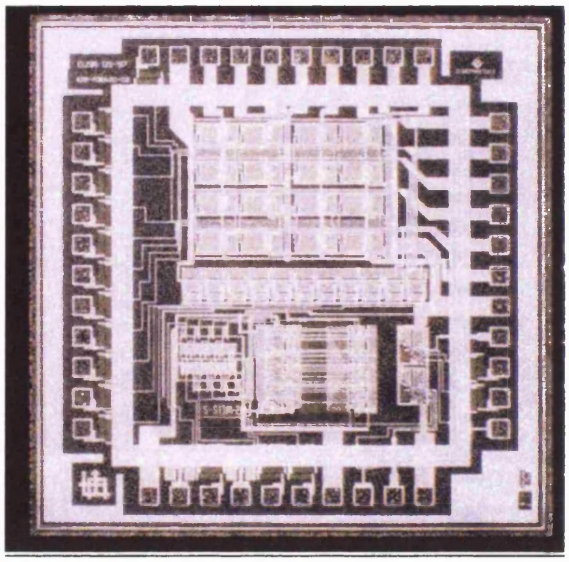

Figure 102. Photograph of IC SSTIM2

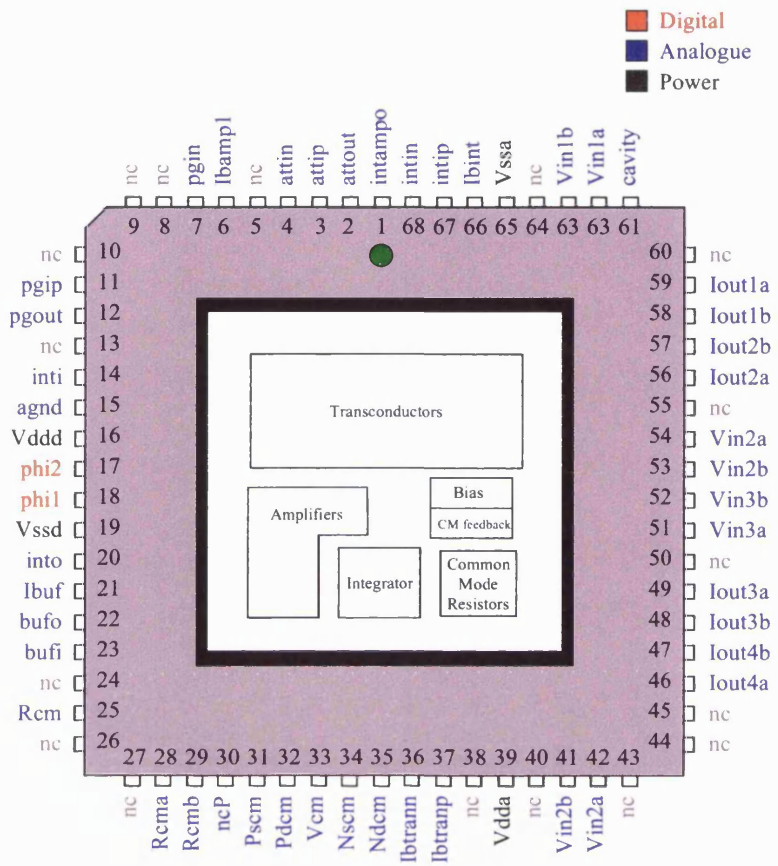

Figure 103. Pinout and floorplan of IC SSTIM3

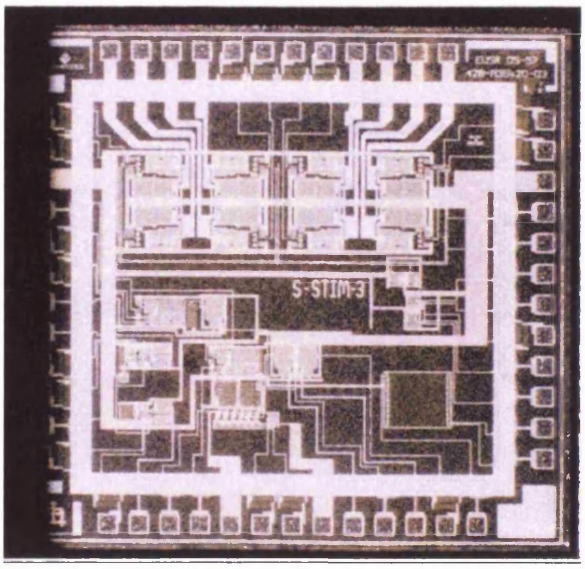

Figure 104. Photograph of IC SSTIM3

A1.2. Operational Amplifier Testing Configurations

Several operational amplifiers were designed for the stimulator circuits. The circuits shown in Figure 105 were used for testing the characteristics of all the amplifiers. Figure 105a allows the measurement of the amplifiers DC gain and AC frequency response. Figure 105b allows the amplifiers offset and slew rate of the amplifier to be measured. These circuits are contained on the PCBs for SSTIM2 and SSTIM3.

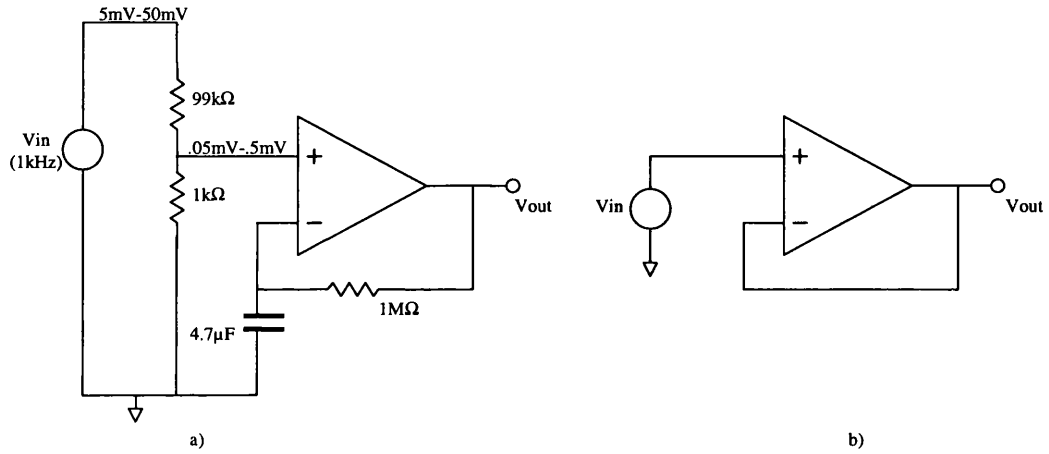

Figure 105. Amplifier configurations for a) DC gain, AC response b) Offset, Slew Rate

A1.3. PCB design and layout

A PCB was designed to test each of the integrated circuit. The PCBs were laid out using PROTEL [106], and fabricated in house at University College London. As the PCBs for all three ICs were mixed-signal, precautions were taken to prevent interference between the analogue and digital sections of the circuits. Separate power supply lies were used to minimise cross talk and noise injection. To further minimise cross talk, noise injection and interference separate ground planes were used, and were connected only at the power supply connection. All parts of the board not used for components were filled to improve the quality of the ground planes. To reduce noise on the DC power lines, these lines were de-coupled from the ground plane using 100nF capacitors, placed close as possible to the IC power supply pins. Low frequency ripple was minimised by placing 22μF capacitors in parallel with the power supply lines. 1μH inductors were placed in series with the DC power lines to prevent incoming noise from the DC power supplies and external cabling.

A1.3.1 SSTIM1

The schematic used to test SSTIM1 is shown in Figure 107 and the associated PCB in Figure 106. The test signals shown on the schematic are described in Table 48.

The PCB allows either internal or external control of all Digital control lines using switch SW4-B. The internal control of the Data lines is DC levels only, set using switches on the PCB. All analog signals to / from the integrated circuit are connected external test connector O1. This includes the output voltages of the attenuators and the pulse generator.

The inputs to both the attenuators and pulse generators are controlled either externally via connector O1 or via a DC signal defined by potentiometer P1 and J2-J4.

Table 48. Test signals on PCB for SSTIM1

Signal	Signal Description	Signal Type	Circuit
D0E - D15E	Gain of Attenuators 1-4	External	Attenuators
D0I - D15I	Gain of Attenuators 1-4	Internal	Attenuators
IbiasAtt	Attenuator Bias	Internal	Attenuators
V1p-V4p, V1n-V4n	Attenuator Outputs 1-4	Output	
A_E- C_E	Reverse Amplitude	External	Pulse Generator
A_E- C_E	Reverse Amplitude	Internal	Pulse Generator
PW_E, PWD_E	Plateau Duration *(pw)*	External	Pulse Generator
PW_I, PWD_I	Plateau Duration *(pw)*	Internal	Pulse Generator
POUT_E	End stimulation *(zero)*	External	Pulse Generator
POUT_I	End stimulation *(zero)*	Internal	Pulse Generator
TAIL_E	Exponential Tail On/Off	External	Pulse Generator
TAIL_I	Exponential Tail On/Off	Internal	Pulse Generator
IbiasPG	Pulse Generator Bias	Internal	Pulse Generator
Pout	Pulse Generator Output	Output	Pulse Generator
T1-T3	Pulse Generator test points	Output	Pulse Generator
SA0-SA1	Internal / External Data	Internal	All
vdda	Analogue Vdd	External	All
vssa	Analogue Vdd	External	All
agnd	Analogue Ground	External	All
vddd	Digital Vdd	External	All
vssd	Digital Vss	External	All
inp1	Input of Attenuators or Pulse Generator	Internal / External	All

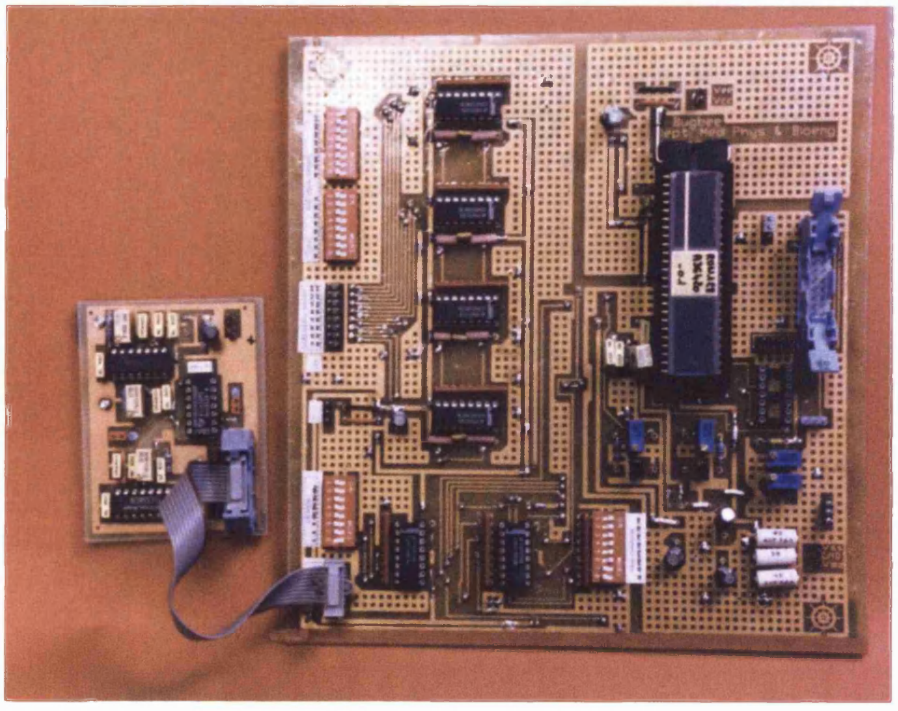

Figure 106. PCBs for testing SSTIM1

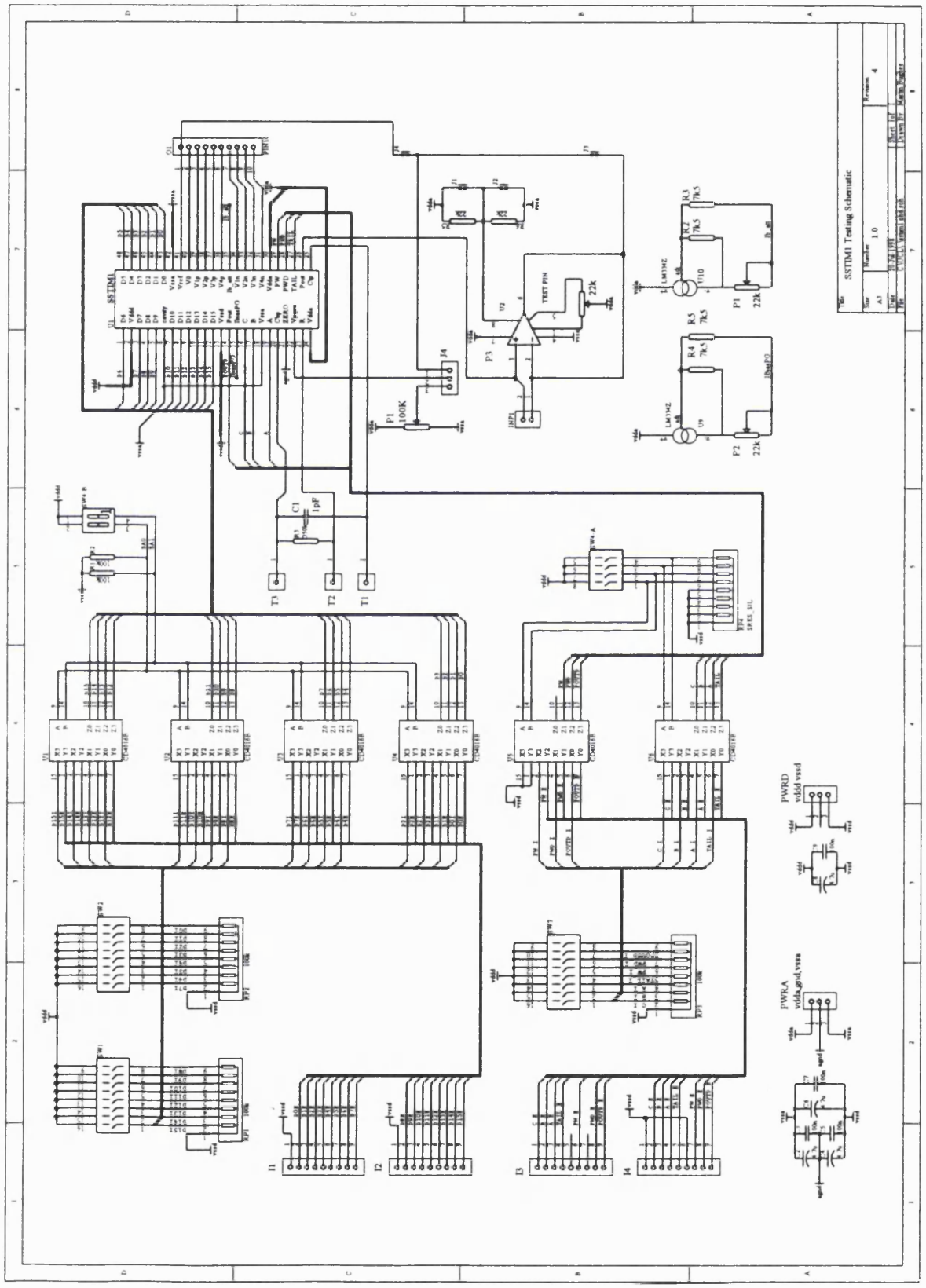

Figure 107. Schematic of circuit used to test SSTIM1

A1.3.2 SSTIM2

The schematic used to test SSTIM2 is shown in Figure 108 and the associated PCB in Figure 109. The test signals shown on the schematic are described in Table 49.

The PCB allows either internal or external control of all Digital control signals. The internal control of the Data lines is DC levels only; set using switches S1-S3 on the PCB. All digital inputs are connected to connectors I1 and I2.All analog signals to / from the integrated circuit are connected external test connectors O1-O4. The inputs to both the attenuators and pulse generators are controlled either externally via connector O1 or via a DC signal defined by potentiometer P1 and J2-J4.

Table 49. Test signals on PCB for SSTIM2

Signal	Signal Description	Input / Output	Circuit
D0-D8	Switching Array Data Lines	Input	Switching Array
D_DIPS	Discharge Array (Dipoles)	Input	Discharge Array
D_TRIPS	Discharge Array (Tripole)	Input	Discharge Array
D_PENT	Discharge Array (Pentapole)	Input	Discharge Array
I1-I4, I1b-I4b	Switching Array Inputs	Input	Switching Array
O1-O6	Switching & Discharge Array Outputs	Output	Switching & Discharge Arrays
Vso	DAC test amplifier Vo	Output	DAC
Vsp	DAC test amplifier Vp	Input	DAC
Vsn	DAC test amplifier Vn	Input	DAC
TSIbias	DAC test amplifier Bias I	Input/Output	DAC
DACIbias	DAC Amplifier Bias I	Input/Output	DAC
CLK	DAC Shift Register Clock	Input	DAC
DSR	DAC Shift Register Data In	Input	DAC
RB	DAC Shift Register Reset	Input	DAC
Q1,Q8	DAC Shift Register Bits 1&8	Output	DAC
VDAC	DAC output voltage	Output	DAC
vdda	Analogue Vdd	Input	All
vssa	Analogue Vdd	Input	All
agnd	Analogue Ground	Input	All
vddd	Digital Vdd	Input	All
vssd	Digital Vss	Input	All

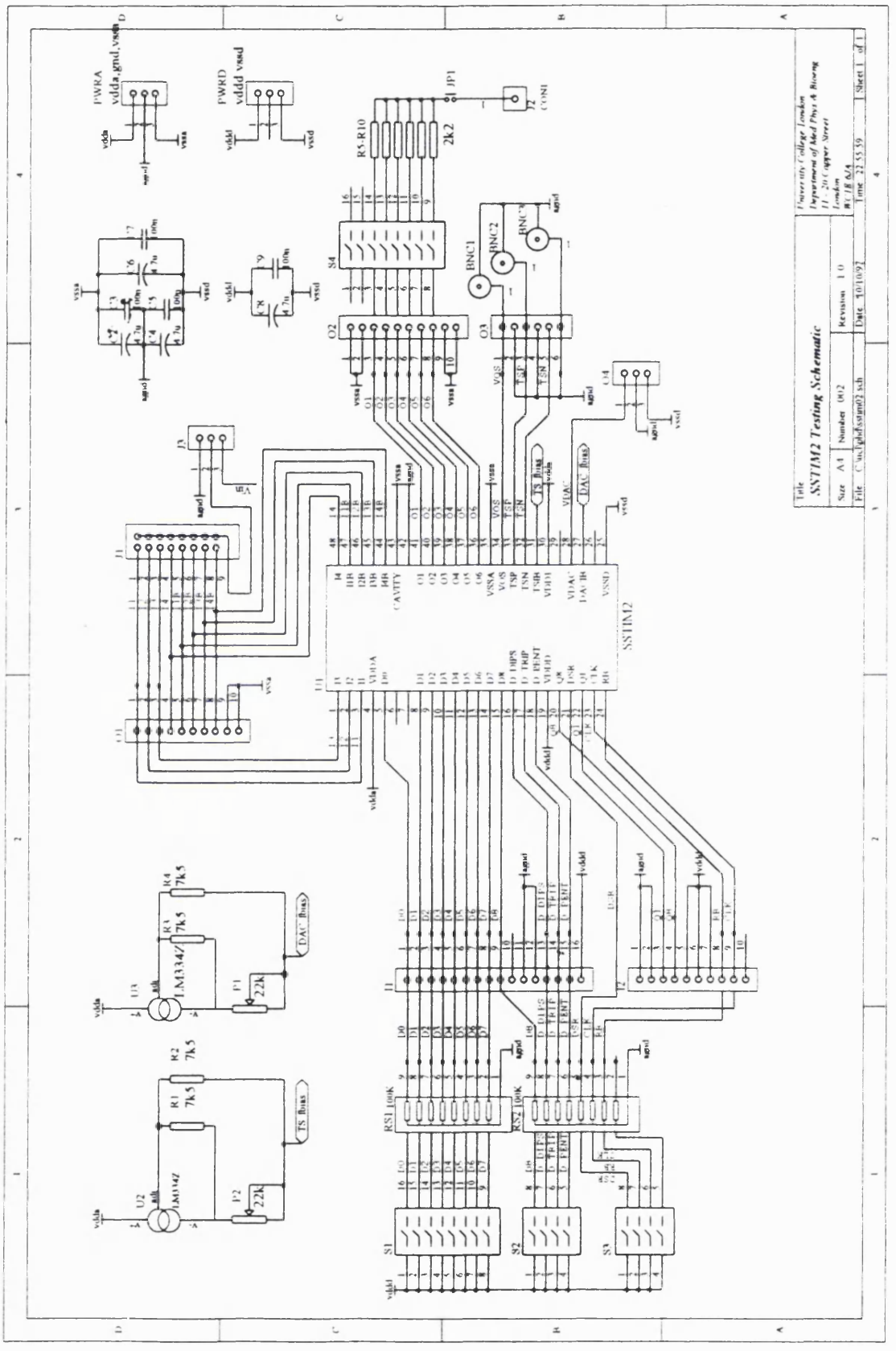

Figure 108. Schematic of circuit used to test SSTIM2

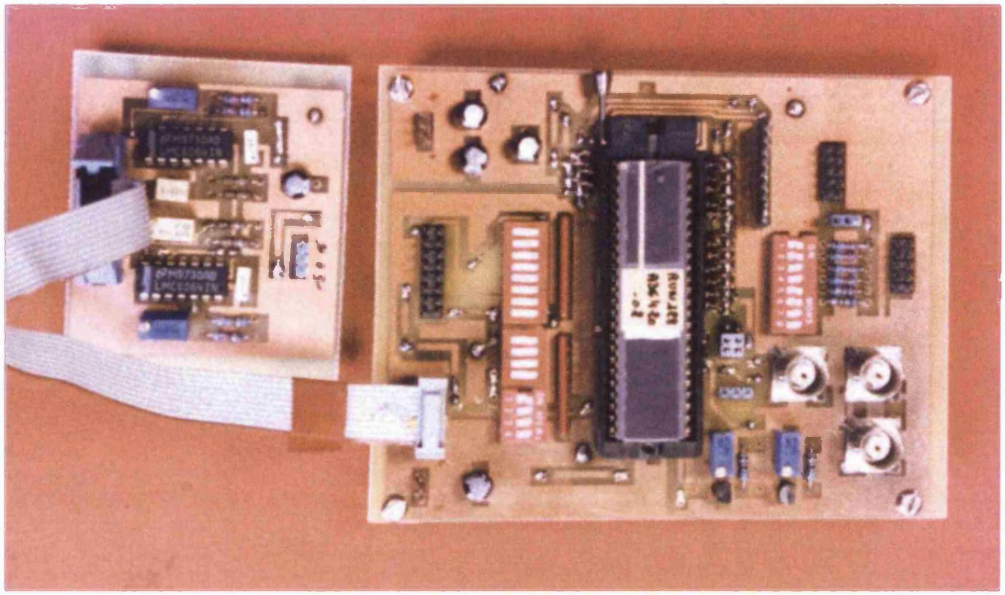

Figure 109. PCB used for testing SSTIM2

A1.3.3 SSTIM3

The schematic used to test SSTIM3 is shown in Figure 110 and the associated PCB in Figure 111. The test signals shown on the schematic are described in Table 49.

The PCB allows external control of all analogue control signals, and moitoring of all output voltages and currents. Switches S1-S2 are used to configure the outputs of the transconductors in differential of single sided operation. J1-J9 define which amplifier is under test and which of the configurations shown is Figure 105 is being used.

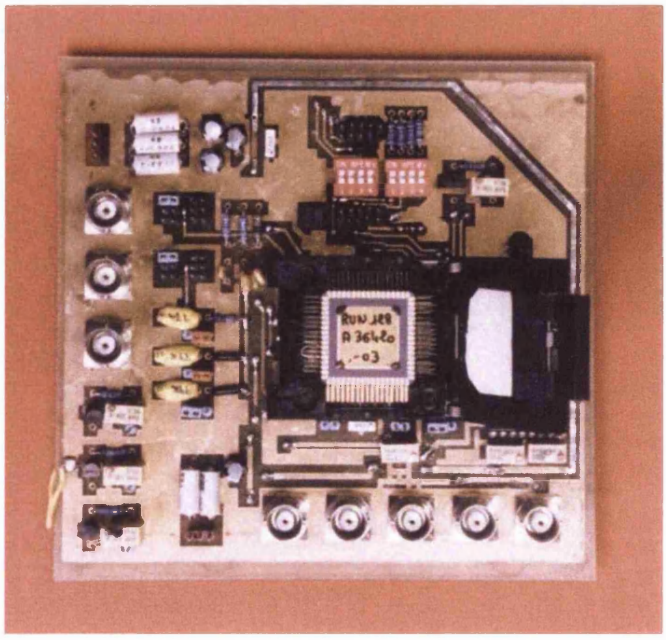

Figure 110. PCB used for testing SSTIM3

Table 50. Test signals on PCB for SSTIM3

Signals	Signal Description	Input / Output	Circuit
Pga_vn, atta_vn, tamp_vn	Inverting inputs of test amplifiers (pulse generator, attenuator and integrator)	Input	Test Amplifiers
Pga_vp, atta_vp, tamp_vp	Non-Inverting inputs of test amplifiers	Input	Test Amplifiers
Pga_vo, atta_vo, tamp_vo	Outputs of test amplifiers	Output	Test Amplifiers
I1a-I4a, I1b, I4b	Transconductor output Currents	Output	Transconductors
Vi1a-V14b	Transconductor Input Voltages	Input	Transconductors
Intvin	Integrator Input	Input	Integrator
Intvo	Integrator Ouput	Output	Integrator
phi1, phi2	Integrator Clocks	Input	Integrator
buf_vi	Buffset Input	Input	Buffer
buf_vo	Buffer Output	Output	Buffer
vref+, vref-	Common Mode Feedback Bias voltages	Input	Common-Mode Feedback
rt_cm	Common-Mode Voltage	Output / Input	Common-Mode Feedback
ib_cas, ib_amps, ibn, ibp, ib_buf	Bias Currents for circuits: Integrator, other amplifers, transconductors, buffer	Input / Output	All
vdda	Analogue Vdd	Input	All
vssa	Analogue Vdd	Input	All
agnd	Analogue Ground	Input	All
vddd	Digital Vdd	Input	All
vssd	Digital Vss	Input	All

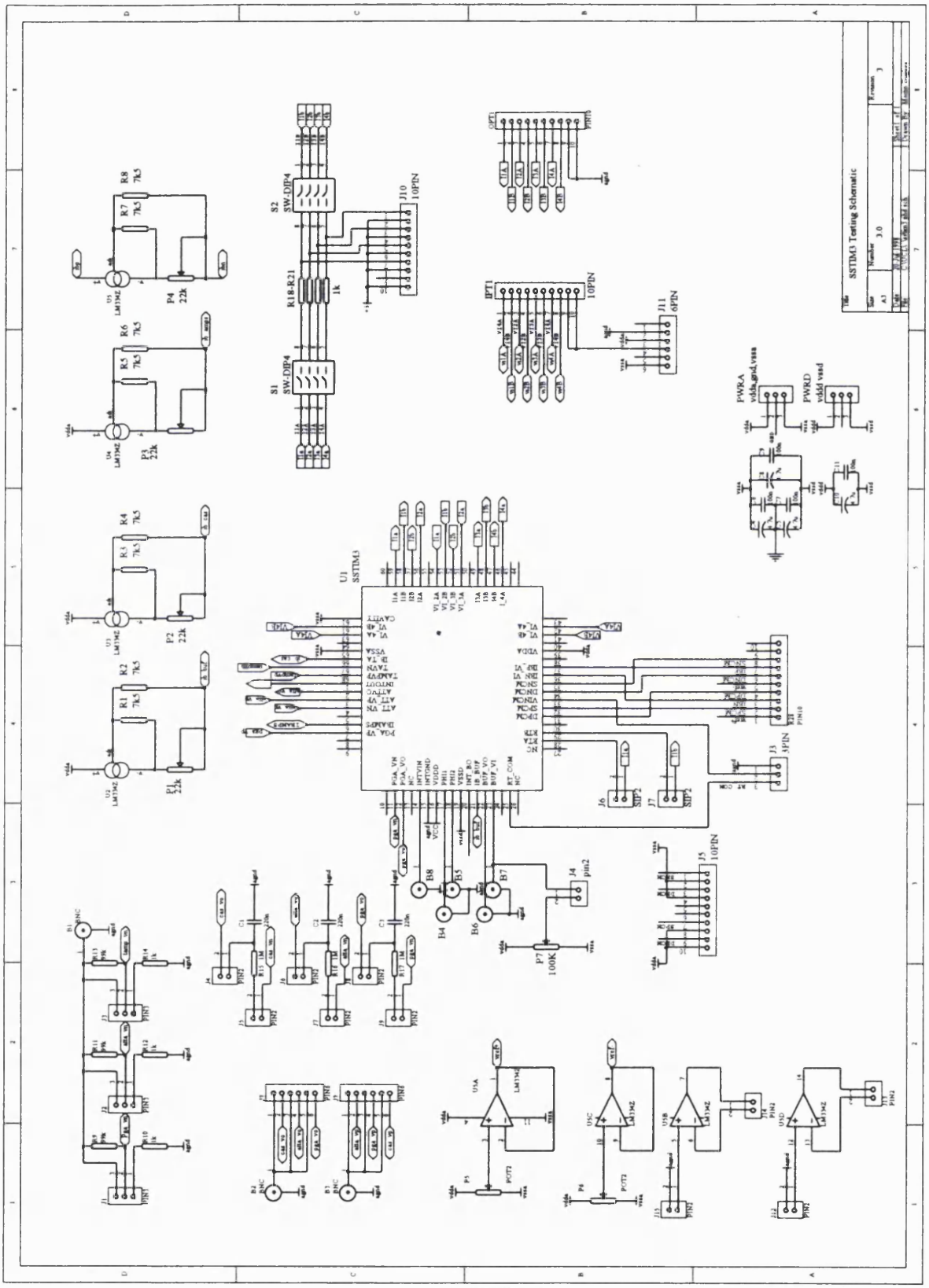

Figure 111. Schematic of circuit used to test SSTIM3

Appendix 2. Integrator Layout Precautions and Buffer Circuit

These sections have being placed in an appendix to separate the analysis from construction methods used for the integrator, which are not required for an understanding of the integrators behaviour.

A2.1. General layout

The integrator was laid out as shown in Figure 112. The switches and the amplifier are separated by a grounded n-well for shielding. The n-well has a single guard ring to bias the well and keep the digital cross talk to a minimum.

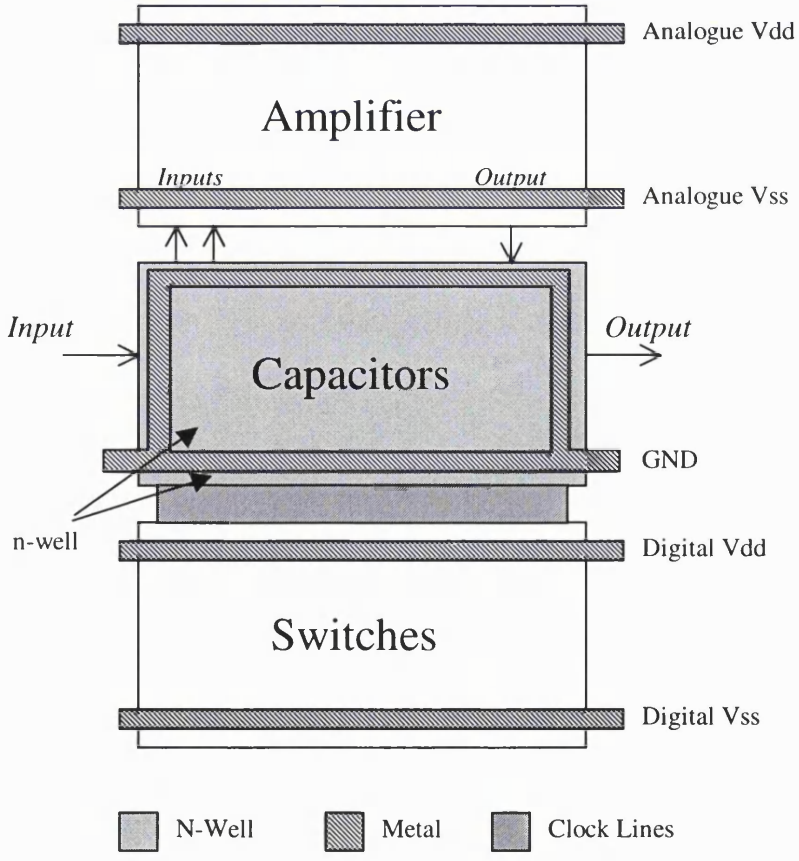

Figure 112. Layout of the T-Cell integrator

A2.1. Capacitor Layout

The layouts of the capacitors in the switched capacitor integrator are based around a standard unit capacitor. All larger capacitors were constructed by abutting these units. The use of this layout allows the periphery of the poly1-poly2 layers to be scaled easily along with the capacitor value. The layout of a unit capacitor is shown in Figure 113. The stubs on the capacitor top plate (poly2) serve a dual-purpose i) they allow a continuous layer of poly2 to be formed when the units are abutted and ii) they reduce the error caused by misalignment of the two poly-silicon layers. The theoretical value of the capacitors is 392fF. This value has being found to produce accurate capacitance ratios in switched capacitor filters manufactured using the Mietec 2.4μm process [126].

The capacitors were placed inside a grounded N-well to minimise noise injection from the substrate.

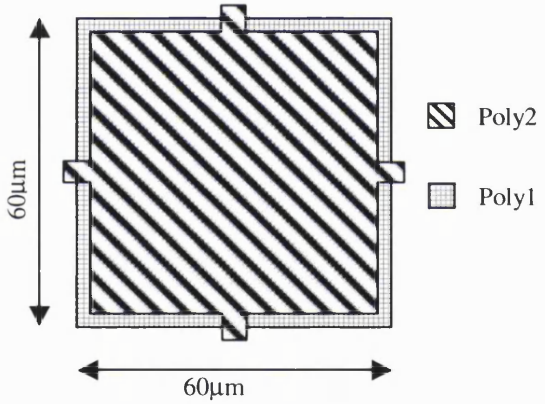

Figure 113. Unit capacitor layout for the integrator

During the layout of the integrator, where possible, the bottom plate of the capacitor was connected to the potential closest to ground, the reasoning behind this is a parasitic capacitor exists between the bottom plate and the N-well, the value of this capacitor is typically 1/6 of the capacitor's value. By connecting the bottom plate to ground, the effect of this parasitic capacitance is reduced. This is particularly important for the node connected to the large capacitor C_2 in the middle of the T-Cell as the node is parasitic sensitive. Care was taken to keep the interconnections as small as possible around this common node.

A2.3. Use of Dummy Transistors

Dummy transistors can be used to reduce the effect of charge injection from the switches. Connecting the drains and sources of switching transistors together and applying inverted clocks to oppose the charge injected from the main switching transistors implement dummy transistors. Only nodes inside the integrator that were simulated as been sensitive to charge injection had dummy transistors added (namely nodes A and B in Figure 81. The dummy transistors are half the size of the switching transistors of interest as only half the total charge injected by the switch flows into the node of interest.

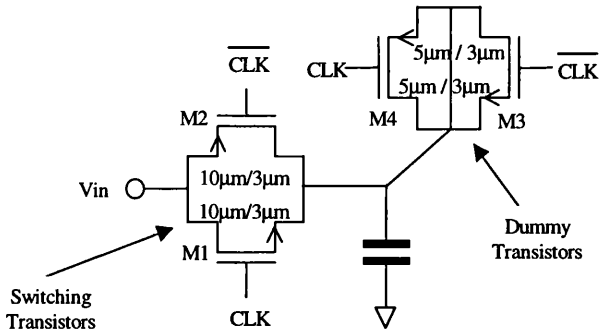

Figure 114. Dummy transistor implementation for a simple sample and hold stage

A2.4. Output Buffer.

Since the output of the folded cascode amplifier is high impedance it is incapable of driving a low resistance external load, which means that a low impedance output buffer had to be designed for of the output of switched-capacitor integrator to allow the output voltages to be observed. Ideally the buffers output impedance should be 50Ω, however the size of the transistors and the power consumed by such a buffer is too large. The buffer was designed with nominal impedance of 100Ω , as the probes connected to the output are high impedance[53]; the error introduced by the buffer will be minimal. The buffer schematic is shown in Figure 115.

[53] R ≈ 10MΩ, Hewlett Packard Inc [75].

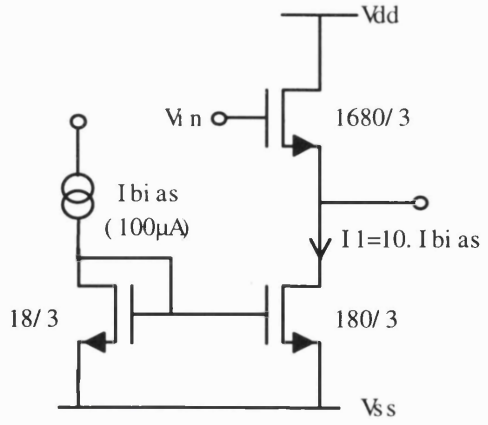

Figure 115. Output Buffer for the T-Cell amplifier

The low frequency output impedance of the buffer is given by:

$$gout = gm1 + gmbs1 + gds1 + gds2 \tag{4.25}$$

Using the simplification $gm1 + gmbs1 >> gds1 + gds2$

$$gout = gm1 + gmbs1 \tag{4.26}$$

For the circuit in Figure 115 the nominal theoretical output impedance is 116Ω. This agrees quite well with the simulated output impedance of 110Ω.

Table 51 compares the experimental measurements on the buffer with the simulated results.

Table 51. Integrator buffer simulated and experimental characteristics

Measurement	Simulated Range		Experimental Value
DC Gain	-0.36dB	-1.14dB	-0.57 ± 0.04dB
DC offset	-0.88V	-1.94V	-1.05V ± 0.05V
Power Consumption(±5V)	10.1mW	10.6mW	10.5mW ± 1mW
DC Output Impedance	104Ω	121Ω	114Ω ± 5Ω
-3dB Bandwidth	97MHz	112MHz	102MHz[54] ± 5MHz

[54] Extrapolated from experimental data up to 100MHz

The DC behaviour of the buffer is shown in Figure 116. The experimental results agree well with the simulated response.

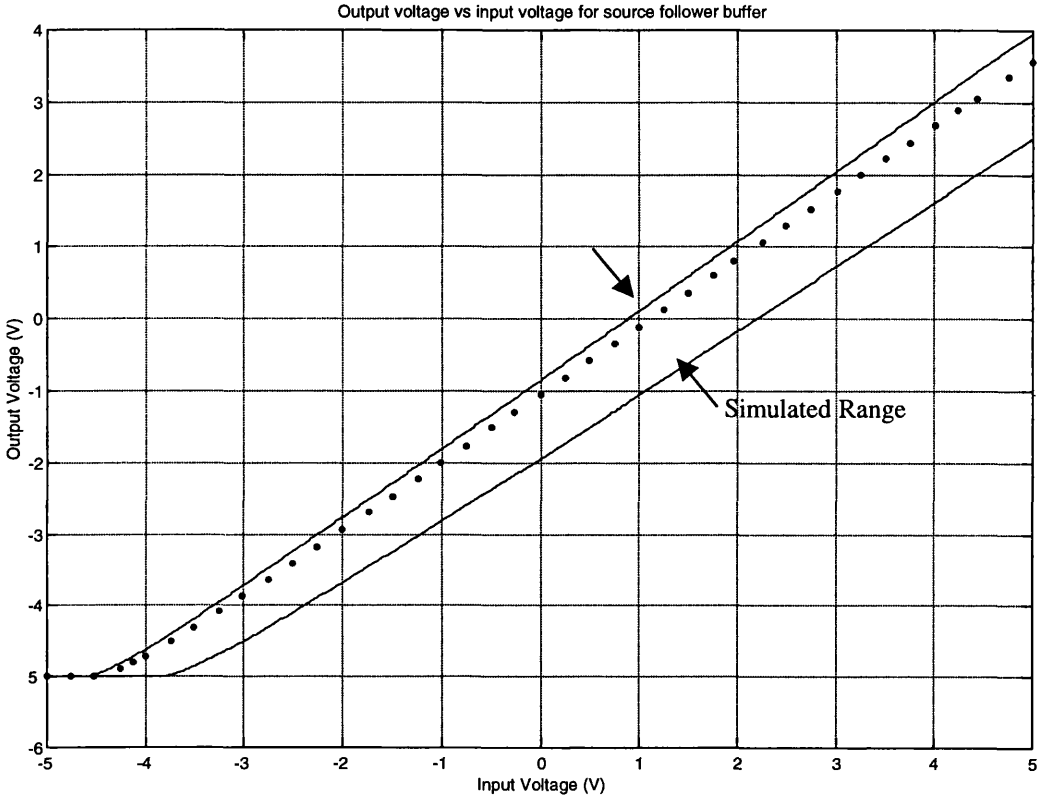

Figure 116. DC characteristics of the buffer with simulated tolerances[55] (Ibias=100μA)

[55] Mietec 2.4μm HSPICE models

Appendix 3. Transistor Equations

A3.1. Low Frequency MOSFET Models

Low frequency MOSFET models are given in equations A3.1 to A3.6 for n-channel and p-channel MOSFETS.

A3.1.1 n-channel MOSFET

$$I_D = 0 \qquad V_{GS} < V_T,\ V_{DS} \geq 0 \text{ (cutoff)} \qquad \text{(A3.1)}$$

$$I_D = \frac{k_n W_n}{L_n}\left(V_{GS} - |V_{tp}| - \frac{V_{DS}}{2}\right)^2 V_{DS} \qquad V_{GS} > V_T,\ 0 < V_{DS} < V_{GS} - V_T \text{ (ohmic)} \qquad \text{(A3.2)}$$

$$I_D = \frac{k_n W_n}{2L_n}\left(V_{DD} - V_{IN} - |V_{tp}|\right)^2 (1 + \lambda V_{DS}) \qquad V_{GS} > V_T,\ V_{DS} > V_{GS} - V_T \text{ (saturation)} \qquad \text{(A3.3)}$$

A3.1.2 p-channel MOSFET

$$I_D = 0 \qquad V_{GS} > V_T,\ V_{DS} \geq 0 \text{ (cutoff)} \qquad \text{(A3.4)}$$

$$I_D = \frac{k_p W_p}{L_p}\left(V_{GS} - |V_{tp}| - \frac{V_{DS}}{2}\right)^2 V_{DS} \qquad V_{GS} < V_T,\ 0 > V_{DS} > V_{GS} - V_T \text{ (ohmic)} \qquad \text{(A3.5)}$$

$$I_D = \frac{k_p W_p}{2L_p}\left(V_{DD} - V_{IN} - |V_{tp}|\right)^2 (1 + \lambda V_{DS}) \qquad V_{GS} < V_T,\ V_{DS} < V_{GS} - V_T \text{ (saturation)} \qquad \text{(A3.6)}$$

Where $V_T = V_{T0} - \gamma\sqrt{\phi + V_{BS}} - \sqrt{\phi}$

W = channel width

L = channel length

K = transconductance parameter

V_{TO} = threshold voltage for $V_{BS} = 0$

γ = bulk threshold parameter

ϕ = strong inversion surface potential

λ = channel length modulation parameter

The effective resistance of a MOSFET in the ohmic region can be derived from A3.2:

$$R_{DS} = \frac{2L}{KW(V_{GS} - V_T)} \tag{A3.7}$$

A3.2. Small Signal MOSFET Models

The small signal behaviour for both n and p channel devices are described by equations A3.8-A3-10.

$$g_m = \sqrt{\frac{2I_{DQ}KW}{L}} \tag{A3.8}$$

$$g_{mb} = \frac{\gamma}{\sqrt{\phi - V_{BSQ}}} g_m \tag{A3.9}$$

$$g_{ds} \approx \lambda \left| I_{DQ} \right|, \; r_{ds} = 1/g_{ds} \tag{A3.10}$$

Where I_{DQ} is defines the quiescent operating current

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