Electrical Engineering Department
California Polytechnic State University

Senior Project Final Report

USB-C Power Adapter for DC House Project

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Acknowledgments

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Abstract

Despite the importance of electricity and the impact it has on our daily lives, many people around the world still live without this essential utility today. According to the International Energy Agency (IEA), approximately 1.1 billion people in the world did not have access to electricity in 2017 [1]. The DC House Project at Cal Poly aims to provide electricity to people living in rural areas by directly utilizing DC energy generated from renewable or human powered sources without the need for DC-AC conversions. However, one significant issue is the lack of a standardized DC wall socket. Standards for AC wall sockets exist in different countries around the world making it simple for consumers to power their appliances and electronics. No such standard currently exist for DC power delivery to consumer devices. This makes DC power within the house inconvenient for consumers as there is no single plug that all their electronic devices can share.

In pursuit of the DC House Project's overall goal, our project is to design and build a USB-C Power Adapter for the DC House Project. The power adapter will interface with the DC House's existing 48VDC infrastructure to deliver up to 100W at 20V to various electronic loads, such as laptops. Although USB-C is a new and emerging technology, it is well placed to become a standard for DC power delivery. IHS technology projects that USB-C will be utilized in nearly five billion devices by 2021 [5]. Additionally, Apple vouched for the versatility of USB-C's power delivery capability by replacing all of the ports on their current laptops, including the charging port, with USB-C ports. Thus, this project aims to standardize the wall socket utilized within the DC House Project and potentially other DC powered homes so that DC power can be as convenient for consumers as AC power.

1 General Introduction and Background

1.1 Off-Grid Power Systems

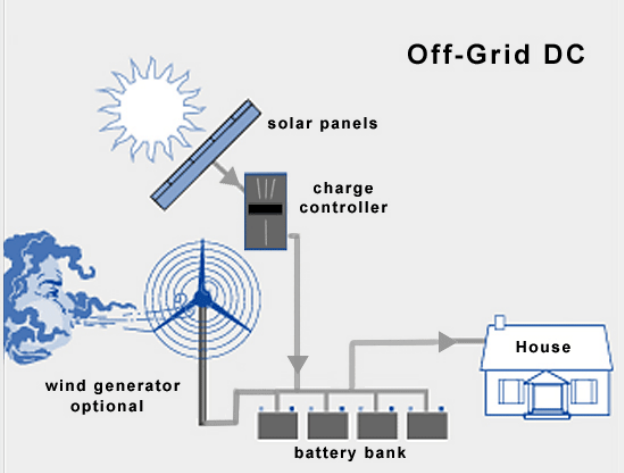


Figure 1.1: Basic Diagram of DC off-grid system

Historically, power systems primarily consisted of AC power. The use of transformers in AC circuits provided a cost effective way to step-up and step-down voltages which gave AC power systems an advantage over DC power systems. The efficiency of transmission over long power lines is greatly increased when high voltages are used. As a result, most consumers are connected to an AC grid and utilize AC power connections for their various devices, which is usually converted to DC before being utilized. However, in rural areas where people rely on smaller scale alternative methods of power generation, such as solar, DC power is much more attractive. The primary off-grid renewable power generation method, solar, often utilizes battery banks to store energy for later use. Since batteries cannot store energy in AC form, the energy generated from renewables sources in grid-connected systems must be inverted and conditioned. This introduces additional power loss and lowers the system efficiency. However, in an off-grid system the inverter may be eliminated by ensuring the loads connected to the system can utilize DC power, and thus increasing the efficiency and simplifying the system. Additionally, the AC-DC converters utilized for most devices could be eliminated, further increasing the efficiency of the renewable energy system.

1.2 DC House Project

The DC House Project is a project started by Professor Taufik at California Polytechnic State University San Luis Obispo. The objective of the project is to develop the DC technology necessary to accommodate multiple renewable energy sources to power off-the-grid homes. In addition to obtaining the power from renewable sources, the DC house may also obtain its source from human powered generators. This project therefore aims to aid access to electricity for people living in rural and remote communities that are out of reach from the utility grid. The International Energy Agency (IEA) reports that approximately 1.1 billion people in the world did not have access to electricity in 2017 [1]. The project aims to directly utilize the generated DC power without any conversions and therefore reducing the system's power losses, cost, and improving the overall efficiency. In the end, the DC House Project is a humanitarian effort to help improve the quality of life of others around the world who are less fortunate.

1.3 USB-C

Over the last 20 years the primary function of USB cables and associated devices has shifted dramatically. Traditionally, the primary function of USB cables and associated devices was to provide a link between devices for data transfer. However, since the advent of the modern smartphone, USB connections have changed, and now most USB connections are used for charging or powering consumer electronic devices. As such, USB-C devices utilize the same data specification from USB-3.1 with the primary upgrades in the physical characteristics of the connector and power delivery capability. The USB-C physical connector features a compact 24-pin design that is two-fold rotationally-symmetrical [2]. That is, a USB-C cable can be plugged in two distinct orientations and operate correctly.

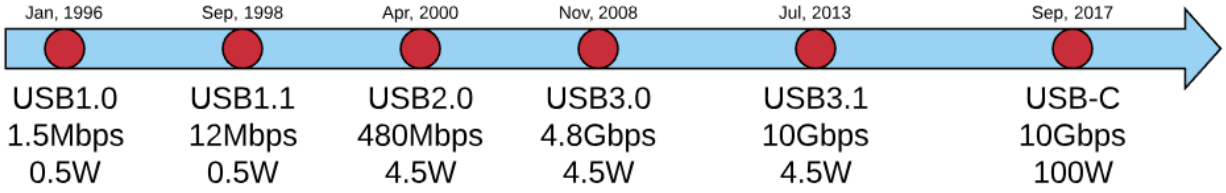


Figure 1.2: Historical Timeline of USB Power Delivery

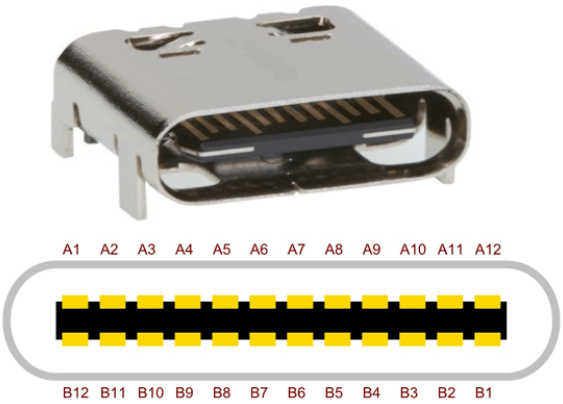


Figure 1.3: USB-C Plug and Pinout

A USB-C connection which meets the USB-C power specification is capable of powering devices at voltages beyond the traditional 5V with additional voltages at 9, 12, 15, and 20V [3]. Currently the standard boasts maximum power delivery potential at 60W compared to Type-A USB connectors which boast a maximum power delivery potential of 18W. As such, USB-C is well positioned to become a future standard for data transmission and power delivery for a wide variety of consumer electronic devices.

1.4 Power Electronics and Buck Converters

The design of converters for power adaption between different devices, especially in DC-DC conversions, greatly relies on power electronics utilizing switching topologies. That is, non-linear converters which utilize solid state switches to achieve more efficient power conversion between a source and load. Some examples of basic switching converter topologies for DC-DC conversion include: boost converter, buck-boost converter, and most importantly for this project buck converter. Buck converters utilize solid state switching to step-down source voltage to an appropriate voltage for the load in an efficient manner. The efficiency gained utilizing these switching converters doesn't merely save power, but reduces the heat generated by the converter allowing use in microelectronic devices. As such, power electronics and switching converters facilitate the creation of microelectronic devices which make modern electronics like cellphones possible. This introduction doesn't begin to exhaust the methods and applications within Power Electronics. However, Power Electronic concepts and specifically that of the buck converter serve as the cornerstone of the project outlined.

2 Background

2.1 Problems and Their Significance

This section lists some of the problems addressed by the USB-C Power Adapter project. It further explains the need for the project and highlights the significance of the issues defined. The points discussed focus on various topics: the increasing popularity of off-grid power systems and the on-going effort in reducing power losses experienced in currently available solutions, the promising future for USB-C Power Delivery, and the improvements and benefits that a reliable method for powering consumer electronic devices brings to rural and secluded communities.

2.1.1 Increasing Popularity of Off-Grid Power System Setups

In October of 2015, Governor Brown signed a Bill that mandates that 50% of the California's energy is generated from renewable sources by 2030 [4]. This development shows that the world is slowly but at an increasing rate shifting toward production of energy from renewable sources. DC power becomes more promising as smaller more localized forms of power generation are considered and implemented. People are becoming more aware of the negative impacts that our present energy generation system has on the environment; thus, expanding the market for localized off-grid or distributed power systems. However, a factor damping the adoption of DC power systems is the lack of a standardized DC power connector for consumer electronic devices.

2.1.2 High Potential for USB-C Power Delivery

USB-C has been considered to be the future of DC power delivery to household electronics. It is projected that approximately 5 billion devices will utilize USB-C adapters by 2021 [5]. The USB-C power delivery standard allows for increased power levels of up to 100W [6]. As a result of USB-C's power delivery capabilities and high data transfer rates, it is set to become a candidate for "universal" DC power delivery method replacing the various charging ports that are currently utilized.

2.1.3 Reducing Isolation and Aiding Development of Rural and Secluded Communities

With the rapid advancement of technology and increased technological dependence, a reliable method to power electronic devices in rural communities has become more of a necessity than an added luxury. Electronic devices, phones and laptops in particular, reduce the isolation of rural and secluded communities and contribute to their development. Access to Information and Communications Technology (ICT) can improve living standards in rural and secluded communities through commercial, social and educational benefits [7]. In addition, smartphones and medical devices can be used to monitor the health of users in rural communities and shorten the distance between the patients and medical providers. All these benefits further affirm the importance of a reliable method for powering consumer electronic devices in rural and secluded communities and the relevance of the overall goal of the DC House Project as a whole.

2.1.4 Reduce Power Losses

Current renewable energy systems utilize inverters to power different electronic devices. While inverters are becoming more and more efficient, the conversion between AC and DC power results in some losses. Additionally, some manufacturers mentioned that their inverters have efficiencies greater than 90%; however, that is only true under ideal conditions. The efficiency of inverters depends on the inverter load. At peak efficiency, the inverter might have an efficiency of 90-95%. However, the efficiency is reduced when the output power is higher or lower than that at peak efficiency [8]. This is especially true when the output power is lower than 10-15% [8]. Sinewave inverters can be used for most household electronics; however, they experience significant power loss due to harmonic frequencies [9].

Portable power banks are another common product currently used to charge electronics off-grid. Although these products have the advantage of portability, the battery life deteriorates over the lifetime of the device. Additionally, it is easy to misplace or lose the power bank.

2.2 Relevant Works

This section outlines previous works and research into the issues addressed by the project outlined in this report. Some of the work analyzed in this section relates to academic papers completed outside of the DC House project that provide context for the extent and nature of the problems considered in this report. In addition, previous senior projects completed for the DC House project are described and compared to our project, highlighting major improvements our project proposes from previous solutions.

2.2.1 Smart DC/DC Power Plug

A previous paper outlines the veracity of USB-C for powering consumer electronic devices from a 350V micro-grid system [6]. To this end, a DC-DC converter is designed and tested to convert 350V to the various voltages required for USB-C based power. However, this project was completed before commercial USB-C power delivery controllers were available. As such, they emulated the USB Power delivery negotiations through the use of LPC 1830 Xplorer microcontrollers [6]. Furthermore, they could ensure their system operated through these emulated power negotiations, but without demonstrating their system would power actual consumer devices.

The same paper outlines a problem unique to USB-C based DC power delivery. That is, USB-C based DC power requires communication between the load and the source. Since several voltages can be utilized by USB-C devices the load and source must agree on what voltage to operate at. This power negotiation takes

place in a fashion outlined by the USB Implementers Forum [6]. However, this unique problem presents a great advantage. Each consumer devices doesn't require its own specialized power adapter to operate since the source can conform to its requirements dynamically. Our goal is to improve on the design presented in this paper by utilizing commercial USB power delivery controllers not previously available. As such, our system will be able to charge and power unmodified consumer electronic devices.

2.2.2 Type-C Interface Reliability Concern of Electrical Overstress

Another paper outlines the electrical reliability concerns that arise from physical characteristics of the USB-C interface [10]. The paper asserts that the decrease in pin-pitch increases the likelihood of an electrical overstress event. Additionally, the increased power voltage increases the potential for damage in an electrical overstress event [10]. These overstress events primarily entail high power pads shorted to data pads at the USB-C interface between the source and the load causing overcurrent or overvoltage events in the load device[10].

This paper further emphasizes the necessity and importance overvoltage and overcurrent protection. Since, we will only be designing a source for USB-C based devices, it is imperative to include proper circuity to handle situations which may create electrical overstress in our source or in the load. Additionally, it emphasizes the importance of testing to ensure the long term reliability of USB-C based devices. Although evaluating long term reliability is beyond the scope of this project, it is important to design for long term reliability in any way we can.

2.2.3 12 Volt Wall Outlet for DC House Project

A similar project completed in 2012 for the DC House Project, titled 12 Volt Wall Outlet for the DC House Project, aimed to provide 12VDC wall power from a 48V solar system utilizing a switching power converter. The 12VDC output produced a peak output power of 100W and achieved an efficiency over 90% at full load [11]. To this end, a single-phase synchronous buck converter topology utilizing the LT3845 synchronous buck controller was constructed. Beyond this, the converter was adapted to potential loads using a standard AC wall plug. Thus, creating a 12VDC wall-plug for powering DC electronic devices.

In many ways this project mirrors that outlined in this report. We also seek a 100W standard DC wall plug to power DC consumer electronic devices utilizing switching power converters. However, the project outlined in this report represents a significant evolution of the DC wall-plug concept advanced by the 12V Wall Outlet Project. Firstly, the physical adapter used for powering electronic devices is changed from a standard "Type B" AC wall outlet to a female USB-C port. This represents a significant improvement since many consumer devices charge through USB-C ports without requiring any modifications. Additionally, our system will protect against potential damage to AC powered devices by accidentally connecting an AC power cord to the DC wall plug. Secondly, our power adapter is capable of charging at 5V, 9V, 15V, or 20V depending on the requirements of the connected load. This is enabled by power negotiation done between the source and load per the USB-C standard and will be further explored in the "Design" section of this report. Thirdly, we aim to improve the short-circuit and over-voltage protections significantly over the converter used for the 12 Volt Wall Outlet Project. The existing design doesn't attempt to limit the output voltage in any significant way. However, our design will protect the load and converter utilizing a USB-C power delivery controller. The power delivery controller will disconnect the load and the source in the case of a situation which would damage the load or source, such as fault current.

In this way this previous work closely represents the goal of this project. However, the evolutions outlined

advance the concept significantly. These evolutions transform the outlined previous work to a system which can be utilized with a wide variety of unmodified consumer devices. As such, this project improves on concept outlined by the 12 Volt Wall Outlet to create a system which may be properly useful for its intended purpose.

2.2.4 Cell Phone Charger for the DC House Project

Another project completed in 2012 aims to create a dual output cell phone charger for the DC House project. The converter utilizes the 48V DC House battery system as an input source and charges cellular devices at 5V with a full load efficiency of 71%. At full load, the Cell Phone Charger project supplied the load with approximately 5W. To achieve this goal, the LT3748 isolated flyback controller was used to design the converter and the charger was assembled on a conductor board. The final product was packaged in a box to cover the inner circuitry and only show the USB ports and connections required to operate the charger[12].

Although the Cell Phone Charger project was a success, our project aims to take this project a step further and offers significant improvements. One of the main improvements that our project offers is the capability of charging electronic devices at multiple output voltage levels. Our power adapter will charge devices at 5, 9, 12, 15, and 20 V depending on the voltage level required by the load device. For load devices specifically requiring 5V, the adapter will supply the load device with up to 3A resulting in output power up 15W, compared to only 5W from the Cell Phone Charger project. Additionally, our adapter aims to improve the full load efficiency, output and input voltage ripple, and line and load regulation outlined in the Cell Phone Charger project. A USB-C port will be utilized to connect to and charge the electronic devices. As mentioned previously, USB-C offers many improvements over the USB-A connectors used in the Cell Phone Charger project. For packaging, the end user will access our power adapter through female USB-C connectors on a wall socket. Packaging the device in a wall socket compared to a standard box casing reduces the clutter around the wires visible to the end user and provides additional safety and protection against children playing around the power adapter.

Overall, the project outlined in this report offers many improvements over the Cell Phone Charger project designed for the DC House project in 2012. The various improvements previously outlined will allow for a much more flexible and useful charging solutions for consumer electronic devices.

2.3 Closing Statements

Standards for AC wall sockets exist in different countries around the world making it simple for consumers to power their appliances and electronics. No such standard currently exists for DC power delivery to consumer devices. This makes DC power within the house inconvenient for consumers as there is no single plug that all their electronic devices can share.

To address this problem, our project is to design a USB-C Power Adapter for the DC House Project. The power adapter will interface with the DC House's existing 48VDC infrastructure to deliver up to 100W at 20V to various electronic loads, such as laptops. Although USB-C is a new and emerging technology, it is well placed to become a standard for DC power delivery. IHS technology projects that USB-C will be utilized in nearly five billion devices by 2021 [5]. Additionally, Apple vouched for the versatility of USB-C's power delivery capability by replacing all of the ports on their current laptops, including the charging port, with USB-C ports.

The USB-C power adapter designed in this project will utilize the DC House's current power generation infrastructure to power electronic devices utilizing USB-C connectors directly without the need for DC-AC or AC-DC conversions. The goal is to design and construct a DC-DC converter that takes in 48VDC and outputs voltages at 5, 9, 12, 15, or 20 VDC and more than 40W.

3 Design Requirements

3.1 System Block Diagrams

The following section shows level 0 and level 1 functional block diagrams for the USB-C power delivery system. The level 0 block diagram describes the systems overall inputs and outputs. This is depicted in Figure 3.1. The level 1 functional block diagram expands the systems internal blocks into functional components that make up the system, as illustrated in Figure 3.2. Between these block diagrams the basic system will be described. In future, these blocks can be further defined and then replaced with actual circuit designs. For further details on these block diagrams, Table 3.1 and Table 3.2 lists and describes each of the parameters shown in the level 0 and level 1 block diagrams, respectively.

3.1.1 Level 0 Block Diagram

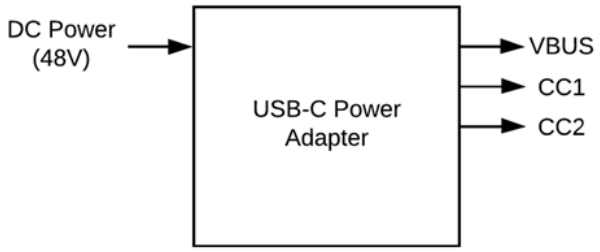


Figure 3.1: Level 0 Block Diagram for USB-C Power Adapter System

Table 3.1: Description of the level 0 block diagram inputs and outputs

DC Power	The input power originates from a 48V battery bank in conjunction with a solar installation. This DC power will be need to be stepped down from 48V to the level negotiated by the power delivery controller.
VBUS	Represents the power path between the power adapter and the consumer electronic device connected. VBUS will be 5V, 9V, 15V, or 20V depending on the power level the load negotiates with the power adapter. Additionally, VBUS will carry a maximum of 20V at 5A to deliver on the 100W power delivery capacity of USB-C.
CC1, CC2	These outputs in conjunction perform several key functions to control USB-C based power delivery functions. Firstly, CC1 and CC2 are used to detect when a USB device is attached. Additionally, the power delivery negotiation between the load device and the power adapter is completed on these pins. Through CC1 and CC2 the power adapter can determine and deliver the correct VBUS voltage for the attached load.

3.1.2 Level 1 Block Diagram

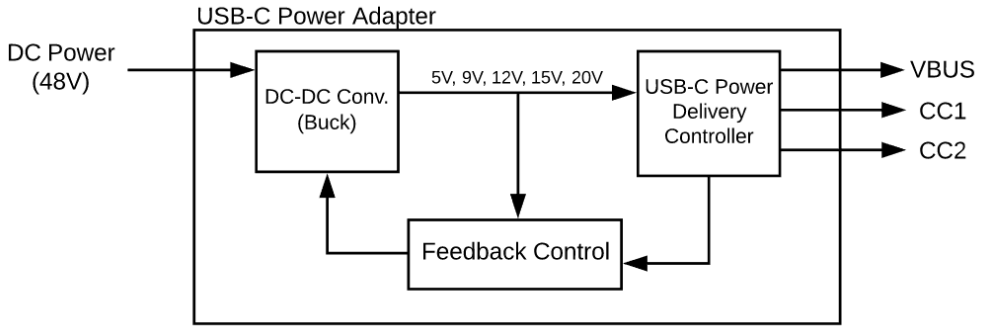


Figure 3.2: Level 1 Block Diagram for USB-C Power Adapter System

Table 3.2: Description of the level 1 block diagram components

USB-C Power Delivery Controller	The power delivery controller serves as the mediator between our DC-DC converter and the connected load. It utilizes CC1 and CC2 to negotiate the voltage and power level that the load can handle, then adjusts the feedback control which is simply a resistive network causing the DC-DC converter to output the load's desired voltage. If the connected load is not capable of doing USB power negotiations the power delivery controller will default to 5V at the lowest power level. In this way the power delivery controller prevents damage to loads connected to it.
Feedback Control	The feedback control is responsible for adjusting the feedback given to the DC-DC converter to change the output voltage level. It is simply a resistive network which can be reconfigured by GPIO outputs from the power delivery controller. This block ensures that the DC-DC converter is outputting the voltage which the power delivery controller has negotiated with the load.
DC-DC Converter (Buck)	The DC-DC Buck converter is responsible for stepping the 48V input voltage down to the level which is controlled through the power delivery controller and feedback control. The voltages that the converter will produce is either 5V, 9V, 15V, or 20V at more than 40W and a maximum of 100W. This converter is the heart of the system and responsible for providing the power utilized by the load for power or charging.

3.2 Technical Design Requirements

This section outlines the technical design requirements for the USB-C Power Adapter System. To this end, requirements are first laid out in the language of the customer to ensure derived technical requirements properly address customer needs related to our system. Finally, additional commentary is given for each requirement to ensure our rationale is properly converted. Thus, design decisions can be made to properly address the various technical requirements.

Table 3.3: Technical requirements for the USB-C power adapter with comments

Req #	Requirement in Language of Customer	Technical Requirement	Comments
1	Product must interface easily with an existing DC power system, such as a solar system.	System must operate with an input voltage of 48VDC.	Ensures system compatibility since medium to large scale systems are commonly 48V.
2	Product must be compatible with devices which utilize the USB-C port for charging or power.	System must have USB-C ports to charge electronic devices at 5, 9, 12, 15, and 20 V with more than 40W.	Covering these voltages will ensure nearly all USB-C based devices can be powered from this adapter.
3	Product must be cheaper than a typical inversion setup for AC powering of consumer electronic devices.	Product price below $200.	This price point can easily be adapted in the DC House Project since our system doesn't require a separate charge controller for each device.
4	Product must be easier to install and maintain compared to a typical inversion setup for AC powering of consumer electronic devices.	When installing the system, the only connection required is the source voltage from the DC power system.	This implies the final system will be a single contained unit.
5	Product must be more efficient than a typical inversion setup for AC powering of consumer electronic devices.	System must exhibit an efficiency above 82% at full-load.	This efficiency is quite achievable with typical market available buck converters boasting efficiencies above 90%.
6	Product must have sufficient safeguards to prevent damage to connected devices or systems.	System must exhibit load regulation below 2%, line regulation below 2%, and short-circuit protection up to 24V	The short-circuit protection is particularly important due to the small size of the USB-C connector and its contacts.
7	Product must exhibit similar or better reliability and longevity compared to analogous systems.	90% of units do not fail before 40,000 hours of operation.	This equates to about 5 years of continuous operation.

3.3 Measurable Project Specifications

The following section outlines specific and measurable project specifications for the USB-C Power Adapter System. The section is broken up into three sections which outline requirements within a particular category. "General Electrical Requirements" define requirements which are derived specifically from the USB-C standard. "System Electrical Requirements" translate the aforementioned general electrical requirements into requirements specific to a DC-DC converter based on the Buck topology. Finally, "System Physical Requirements" outline requirements related to the physical size and nature of the final system. Thus, these specifications can be utilized to objectively determine whether our system meets design expectations.

3.3.1 General Electrical Specifications

The following lists the general electrical specifications for the project:

- Output voltage $\pm 5\%$ of expected value
- Maximum output settling time following load transient of 5ms
- Current Limit Accuracy $\pm 5\%$ of expected value
- Exhibit sourcing capabilities as outlined in Figure 3.3

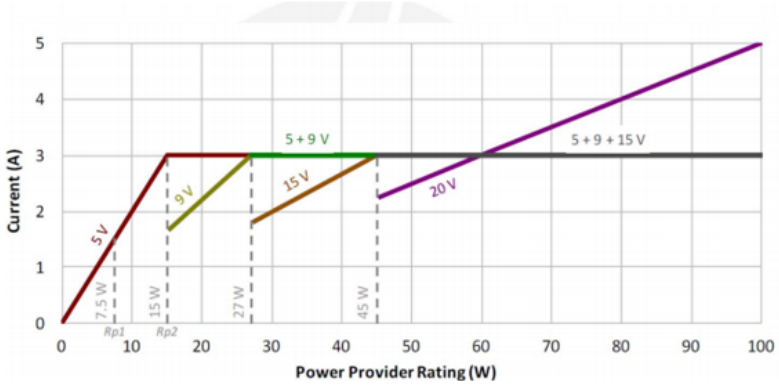


Figure 3.3: Power Ratings for USB-C PD standard

3.3.2 System Electrical Specifications

The overall system electrical requirements are listed below showing their targeted values and desired performances.

- Input Voltage Source: 48VDC
- Max Output Current: 5A
- Efficiency at full-load: greater than 80%
- Output Voltage Ripple at full load: less than 1%
- Line and load regulation: less than 2%
- Topology: 2-phase synchronous Buck converter
- Switching Frequency: 200-250 kHz

3.3.3 System Physical Specifications

In addition to electrical design specifications, the project will have to conform to several mechanical or physical design requirements to ensure that the final product can physically fit within the DC House. The following lists these requirements.

- User access to power adapter through a USB-C port on a standard wall socket
- PCB Specifications:
  - Layers: 4 layers
  - Dimensions: less than 150x100x40 mm
- Overall adapter should fit in a container less than 8.5X5.5X2.75 inches
- Depending on the time and flow of the project, two options arise for the PD controller:
  - Option 1: Integrate PD controller onto the designed PCB
  - Option 2: Utilize a TPS25740B-741 evaluation module (EVM) for the PD controller
    - Bypass Buck-Boost converter stage on the EVM
    - Converter assembled on a separate PCB from the EVM

4 Design and Simulations

4.1 Solution Statement

This section further explains the proposed solution for the problem outlined in Chapters 1 and 2. Additionally, the section details the design processes and simulations used to verify that the requirements outlined in Chapter 3 are met. To this end, the Level 2 block diagram shown in Figure 4.1 shows how the proposed solution will address problem outlined previously. This solution statement will serve as the base for the various more detailed design considerations made in this chapter.

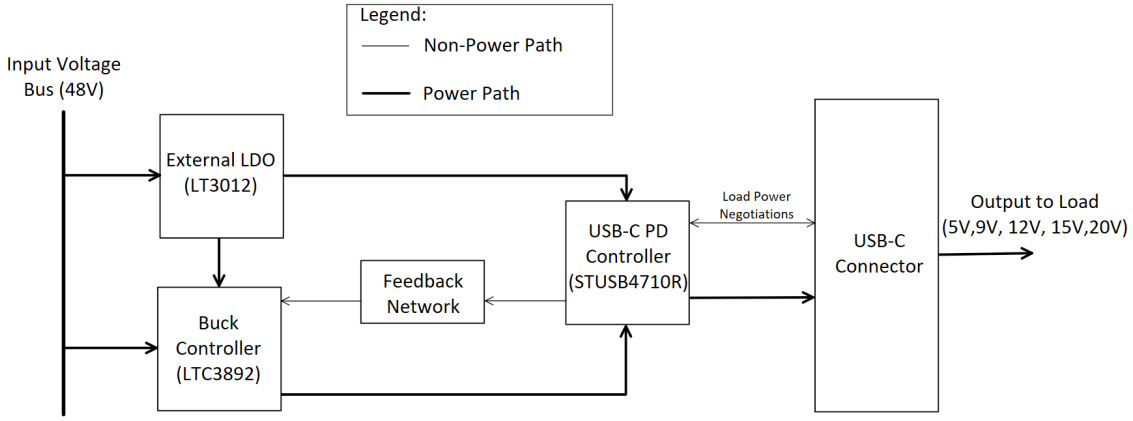


Figure 4.1: Level 2 Block Diagram of Proposed Solution.

The proposed solution aims to fulfill the need for USB-C based power delivery from a 48V input bus. This is performed primarily through a 2-phase buck converter utilizing the LTC3892 Dual-Phase Buck Controller. The USB-C Power Delivery controller negotiates with USB-C devices to determine the charging voltage and power required by the load devices then adjusts the feedback network of the buck converter to produce the desired output voltage. Finally, the LT3012 regulates the input voltage to 12V for the gate drivers of the buck converter. This prevents the buck converter's internal LDO from heating the buck controller chip and causing possible damage. The proposed solution features many significant advancement from systems previously fielded for similar use in the DC House Project. Firstly, the physical adapter used for powering electronic devices is changed from various non-standard adapters to a female USB-C port which allows for potential standardization. Secondly, our power adapter is capable of charging at 5V, 9V, 15V, or 20V depending on the requirements of the connected load. Thirdly, we aim to improve the short-circuit and overvoltage protection superior to similar projects fielded for the DC House Project. The design will protect the load and converter utilizing a USB-C power delivery controller. The power delivery controller will only connect the load in the case of a successful power negotiation between the source and load. This represents a significant reduction in the risk of damage to devices in the case of user error. For these reasons our system represents a significant evolution of USB based DC power adaptation utilized for the DC House Project. Next, the system shown in Figure 4.1 will be further defined and components sized to actualize our solution.

4.2 Design Procedures

This section outlines component sizing and selection for the various subsystems which make up the system represented by the block diagram of Figure 4.2. The sizing and selections will make up the design which will be simulated and evaluated later within this chapter.

4.2.1 General Synchronous Buck Converter

This subsection details design aspects of the "General" Synchronous Buck Converter. That is, aspects of the Buck converter design which are not specific to controller selection.

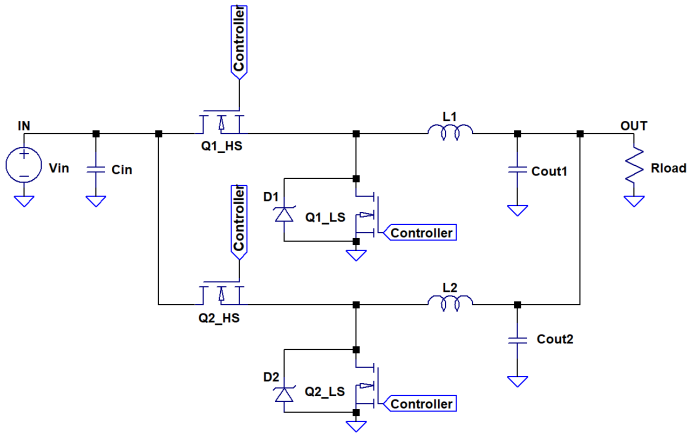
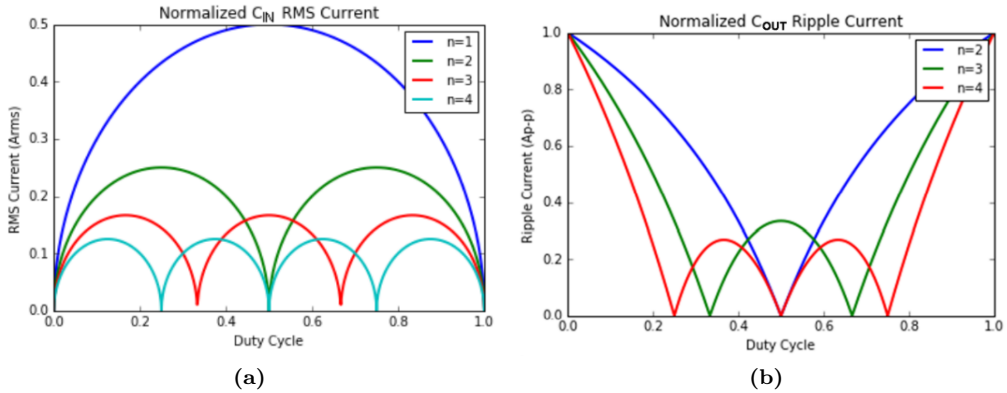


Figure 4.2: Diagram of "General" Two-Phase Buck Converter.

4.2.1.1 Number of Phases

The number of phases stems from the balancing of several distinct system considerations. That is, physical size, cost, efficiency, and size of input/output filters. Single phase buck presents several clear benefits in terms of costs and physical size. Additionally, the design process and forthcoming layout design would be significantly simpler. However, single phase bucks generally suffer from lower efficiency and larger input/output filters compared to multi-phase buck designs. Weighing these concerns a multi-phase topology will be utilized in this design.



(a) **(b)**

Figure 4.3: (a) Normalized Input RMS Current for Various Phase Numbers
(b) Normalized Output RMS Current for Various Phase Numbers

A two phase buck converter topology is chosen for this design. This is determined by various considerations. First, the size and costs of two phase buck converter is significantly less than three or four phase systems. Additionally, the multi-phase systems show different reductions in input and output RMS currents based on the system duty cycle. As evident in Figure 4.3, a two-phase buck converter yields a minimum in input and output RMS current around 50% duty cycle. Since, our system's high power case will yield a duty cycle close to 50% this makes the two-phase system desirable. Finally, the complexity and component count will be significantly less in a two-phase system compared to three or four phase systems.

4.2.1.2 Duty Cycle and Switching Frequency

The switching frequency relevant to component selection is chosen such that the output ripple for the two-phase buck is approximately 500kHz. The switching frequency isn't exactly 225kHz; however, due to limitations of available standard resistor sizes.

$$f_s = 230kHz$$

The Duty Cycle, as in all standard buck converters is determined for the highest power state as it is most relevant to component sizing.

$$V_{in} = 48V \quad V_{omax} = 20V$$

$$D = \frac{V_{omax}}{V_{in}} = 0.417$$

4.2.1.3 MOSFET Selection

Three primary considerations were made concerning MOSFET selection: maximum V_{DS}, maximum drain current, $R_{DS(on)}$, and gate charge. The RJK0651DPB was chosen and its merits evaluated using its datasheet [14]. Firstly, the maximum allowable V_{DS} of 60V is well above the 48V input voltage to the converter. Secondly, the maximum allowable drain current is 25A well above the approximately 7A maximum drain current the MOSFET will experience in operation. The $R_{DS(on)}$ of this MOSFET is $11m\Omega$. The associated conduction losses should be acceptable for the purposes of this converter. Finally, the gate charge of 15nC is among the lowest seen in comparable MOSFETS. The gate charge is proportional to the current required to drive the gate of the MOSFET. As such, this value should be minimized to reduce the chance of damage to the controller's gate drivers.

4.2.1.4 Schottky Diode Selection

Three primary considerations were made concerning Schottky Diode selection: maximum repetitive reverse voltage, non-repetitive surge current, and forward voltage. The SS26T3G was chosen and its merits evaluated using its datasheet [15]. Firstly, the maximum repetitive reverse voltage is 60V which is well above the 48V input voltage which will appear across the diode. Secondly, the non-repetitive surge current is 40A which is well above the expected surge currents of around 7A. Finally, the forward voltage is 0.51V which is comparable to the forward voltage of similar diode. As such, the power dissipated in the diode will be at its reasonable minimum.

4.2.1.5 Inductor Sizing

Inductors are sized based on the critical inductance. The primary design consideration magnitude of the inductor current ripple, ΔI_L. General guidelines suggest that the inductor current ripple between 30% and 40% of the maximum output current [16].

$$I_{omax} = 5A$$

$$\Delta I_L = (.35)I_{omax} = 1.75A$$

$$L_c = \frac{V_{omax}(1 - \frac{V_{omax}}{V_{in}})}{\Delta I_L * f_s} = 28.99\mu H$$

$$L_{eq} = 33\mu H$$

The next standard highest standard inductor value is used for the inductor on each phase. Thus, the inductance chosen is $L_{eq} = 33\mu H$.

4.2.1.6 Output Capacitor Sizing

The output capacitor is chosen by two primary characteristics: the capacitance and rated RMS current. Firstly, the capacitance is chosen such that the output remains within spec as described by $\%V_{out}$ both during transients and in steady state. I_{step} represents the maximum "instantaneous" change in load current and is chosen, somewhat arbitrarily, to be half of the maximum output current.

$$V_{omin} = 5V \quad \%\Delta V_{out} = 0.01$$

$$C_{ss} = \frac{\Delta I_L}{8 f_s V_{omin} * \%\Delta V_{out}} = 19.02\mu F$$

$$I_{step} = (0.5)I_{omax}$$

$$t_{und} = \frac{L_{eq} * I_{step}}{V_{in} - V_{omax}} = 2.588\mu s \quad t_{ov} = \frac{L_{eq} * I_{step}}{V_{omin}} = 14.49\mu s$$

$$Q_{und} = \frac{1}{2} t_{und} I_{step} = 3.235\mu C \quad Q_{ov} = \frac{1}{2} t_{ov} I_{step} = 18.12\mu C$$

$$C_{und} = \frac{Q_{und}}{V_{omin}\% * \Delta V_{out}} = 64.70\mu F \quad C_{ov} = \frac{Q_{ov}}{V_{omax} * \%\Delta V_{out}} = 90.58\mu F$$

$$C_{omin} = max([C_{ss}, C_{und}, C_{ov}]) = 90.58\mu F$$

Then maximum output capacitor ripple current is found to ensure longevity and performance of the capacitor.

$$phases = 2 \quad mp = floor(D * phases) = 0$$

$$I_{o\_norm} = phases * \frac{(D - mp * \frac{D}{phases})(\frac{1 + mp * D}{phases} - D)}{(1 - D)D} = 0.286$$

$$I_{oripple} = \Delta I_L * I_{o\_norm} = 0.5A$$

As such, the output capacitance will need to exceed about $100\mu F$ and be rated to handle more than about 0.5A peak to peak ripple current.

4.2.1.7 Input Capacitor Sizing

The input capacitor is chosen by two primary characteristics: the capacitance and rated RMS current. Firstly, the capacitance is chosen such that the output remains within spec as described by $\%V_{in}$.

$$\Delta V_{in} = 0.01$$

$$C_{in\_min} = \frac{D(1-D) * I_{omax}}{f_s * \%\Delta V_{in} * V_{in}} = 11.01\mu F$$

Then maximum input capacitor RMS current is found to ensure longevity and performance of the capacitor.

$$I_{in\_norm} = \sqrt{(D - mp * \frac{D}{phases})(\frac{1 + mp * D}{phases} - D)} = 0.186$$

$$I_{in\_rms} = I_{omax} * I_{in\_norm} = 0.932A$$

As such, the input capacitance will need to exceed about $15\mu F$ and be rated to handle more than about 1A of RMS current.

4.2.2 Dual Phase Synchronous Buck Controller (LTC3892)

This subsection details design aspects of the Dual Phase Synchronous Buck Controller. That is, aspects of Buck design which are specific to controller selection.

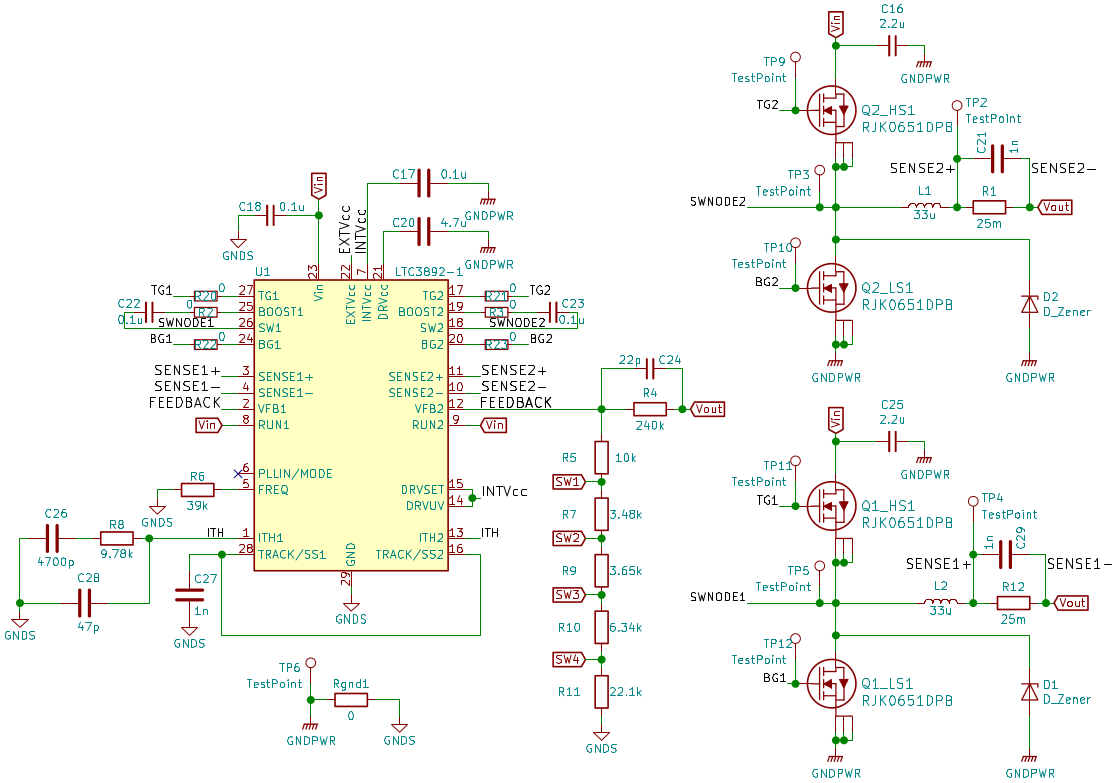


Figure 4.4: Circuit schematic focalized to the LTC3892 buck controller

4.2.2.1 Frequency Resistor - R_6

The frequency resistor is chosen such that the system exhibits a switching frequency of 230kHz. Section 4.2.1.2 gives the reasoning for the selection of this switching frequency. The datasheet of the LTC3892 doesn't give a numerical expression of switching frequency versus frequency resistor value. However, Figure 4.5 shows graphically the aforementioned relationship.

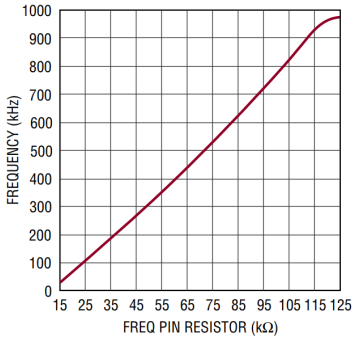


Figure 4.5: Frequency vs resistor value as given in the LTC3892 datasheet[17]

Using Figure 4.5 the nearest standard resistor value for a switching frequency near 230kHz is chosen to be $R_6 = 39k\Omega$.

4.2.2.2 Current Sense Resistor - R_1, R_{12}

The current sense resistor's voltage drop sets the current limit of the buck controller. This controller infers maximum current operation when the voltage drop across the current sense resistor is 75mV [17]. The maximum load current is 5A; however, to account for the inductor current ripple the resistor is designed to produce a 75mV drop at 6A. Since, each phase carries the same amount of the output current each current sense resistor will see 3A.

$$R_{sense} = \frac{75mV}{3A} = 25m\Omega$$

As such, a $25m\Omega$ resistor is chosen for the sense resistors in each phase.

4.2.2.3 Feedback Resistor Ladder - R_5, R_7, R_{9-11}

The resistor ladder sets the feedback and thus output voltage of the buck converter. The resistor ladder is designed such that the USB-C Power Delivery Controller may control the output voltage of the buck converter by grounding legs of the resistor ladder to change the feedback network. R_5 is chosen such that the remaining resistances calculated for the resistor ladder fall near standard resistor values. The calculations are performed as outlined in the STUSB4710's datasheet[18].

$$R_4 = 240k\Omega, \quad V_{ref} = 0.8V$$

$$V_{out} = 20V => R_5 = \frac{V_{ref}R_4}{V_{out} - V_{ref}} = 10k\Omega$$

$$V_{out} = 15V => R_7 = \frac{V_{ref}R_4}{V_{out} - V_{ref}} - R_5 = 3.52k\Omega$$

$$V_{out} = 12V => R_9 = \frac{V_{ref}R_4}{V_{out} - V_{ref}} - R_5 - R_7 = 3.62k\Omega$$

$$V_{out} = 9V => R_{10} = \frac{V_{ref}R_4}{V_{out} - V_{ref}} - R_5 - R_7 - R_9 = 6.27k\Omega$$

$$V_{out} = 5V => R_{11} = \frac{V_{ref}R_4}{V_{out} - V_{ref}} - R_5 - R_7 - R_9 - R_{10} = 22.10k\Omega$$

For each respective resistor an appropriate standard resistor value is chosen.

4.2.2.4 Soft Start Capacitor - C_{27}

The Soft Start Capacitor sets the ramp time for the initial rise of V_{out} from 0V to its final regulated value. We don't plan to utilize this feature initially; however, we would like to be able to utilize it in future if necessary. As such, a very small capacitor is utilized to prevent the start up time from being slowed by the charging of the Soft Start Capacitor.

$$C_{27} = 1nF$$

4.2.2.5 Note on Compensation Loop - R_8, C_{26}, C_{28}

The compensation loop can be adjusted to optimize the transient response of the buck converter. These values were given by the LTC3892 datasheet[17] as reasonable starting values. They shouldn't need to be changed except to tune the transients of the converter. However, possible tuning of the compensation loop will need to be postponed until the system is constructed and tested.

$$R_8 = 9.78k\Omega$$

$$C_{26} = 4700pF$$

$$C_{28} = 47pF$$

4.2.2.6 Note on Various Other Components

Various other capacitors are used in the design for "general" purposes. That is, either a bypass capacitor to smooth the output of a supply or attempt to dampen noise in various parts of the circuit. An example, of the aforementioned bypass capacitor is C_{20} which provides bypass for the output of the LTC3892's internal

LDO which powers the chip. An example, of a smoothing capacitor is C_{29} which serves prevent harmful noise from reaching the sense pins on the LTC3892. The values of these components are set according to the general guidelines of the LTC3892 datasheet[17].

4.2.3 Low Dropout Linear Regulator (LT3012)

This subsection details design aspects specific to the Low Dropout Linear Regulator used in the design.

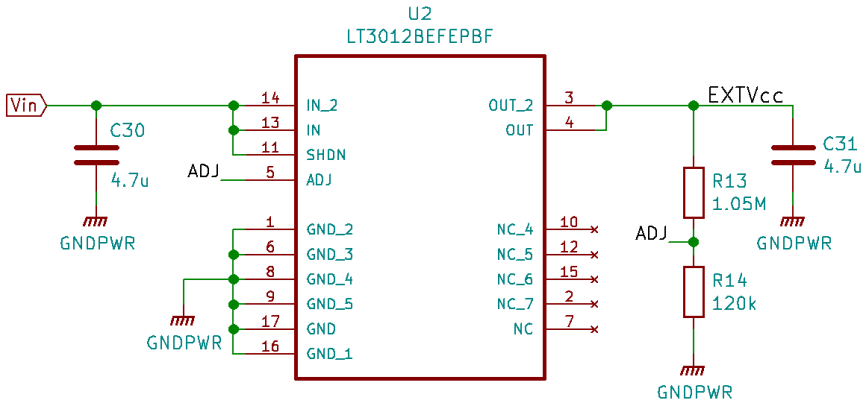


Figure 4.6: Circuit schematic focalized to the LT3012B low dropout linear regulator

4.2.3.1 Input Capacitor Sizing - C_{30}

A bypass capacitor is included at the input of the LDO to reduce the noise on the input voltage signal. The LT3012B datasheet recommends an input capacitor in the 1-10μF range [19]. Thus, a 4.7μF capacitor is placed on the input of the LDO.

4.2.3.2 Output Capacitor Sizing - C_{31}

According to the LT3012B datasheet, a minimum 3.3μF output capacitor with an ESR less than 3Ω is required at the output to prevent oscillations [19]. For this reason, a 4.7μF capacitor is placed at the output of the LDO. When selecting the component, careful consideration is given to the ESR to ensure that it is less than 3Ω.

4.2.3.3 Feedback Resistor Ladder - R_{13}, R_{14}

The feedback resistor ladder is used to set the output voltage of the LDO to the desired voltage level. In this case, an output voltage of 12V is desired. By setting R_{14} to 120kΩ, the value of resistor R_{13} is determined using the following equation [19]:

$$V_{out} = 1.24V \times (1 + \frac{R_{13}}{R_{14}}) + (I_{ADJ})(R_{13})$$

where $I_{ADJ} = 30nA$, $R_{14} = 120k\Omega$ and $V_{out} = 12V$ then:

$$R_{13} = \frac{V_{out} - 1.24V}{\frac{1.24V}{R_{14}} + I_{ADJ}} = 1.04M\Omega$$

Rounded to the nearest standard resistor value, $R_{13} = 1.05M\Omega$

4.2.4 USB-C Power Delivery Controller (STUSB4710R)

This subsection details design aspects specific to the USB-C Power Delivery Controller used in the design.

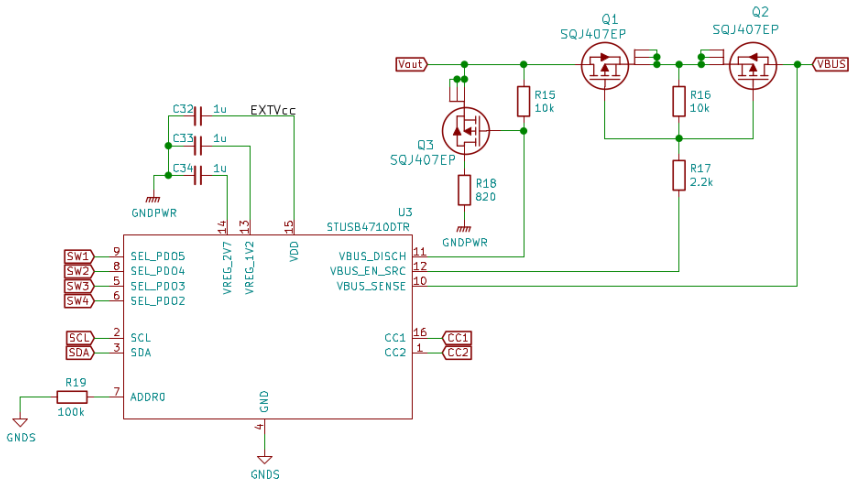


Figure 4.7: Schematic diagram for the STUSB4710R USB-C power delivery controller

4.2.4.1 Bypass Capacitors - C_{32}, C_{33}, C_{34}

These capacitors serve as bypass for the power delivery controller's input voltage and two internal regulators. The capacitor values are set based on suggested values from the STUSB4710R's datasheet[18].

$$C_{32} = C_{33} = C_{34} = 1\mu F$$

4.2.4.2 I2C Address Resistor - R_{19}

The resistor simply serves as a pull-down to set the power delivery controller's I^2C address at start-up[18]. As such, a relatively high resistance value is chosen to prevent to reduce current flow from the ADDR0 pin.

$$R_{19} = 100k\Omega$$

4.2.4.3 MOSFET Selection

The SQJ407EP was chosen and its merits evaluated using its datasheet [20]. Firstly, these are P-type MOSFETs which easily meet our required drain current and drain to source voltage. These MOSFETs aren't periodically switched like in the buck converter. As such, $R_{DS(on)}$ minimization takes precedent over low gate charge. As such, the $R_{DS(on)}$ of this MOSFET is $4.4m\Omega$ and the total gate charge is 169nC. As such, the expected conduction loss at full load is 220mW.

4.2.4.4 Note on Power Path Layout

The layout of power path in Figure 4.7 mirrors that of the suggested layout in the STUSB4710R datasheet[18]. One point of interest is the series MOSFET combination of Q1 and Q2. Initially, it may seem odd since it doubles the conduction losses of this portion of the circuit; however, it performs an important function. MOSFETs feature an inherent diode drop. As such, using a single MOSFET would see V_{bus}, the ouput bus to the USB-C Port, being a diode drop below V_{out}. Adding the second MOSFET removes this diode drop allowing V_{out} and V_{bus} to have the same potential.

4.3 Simulations

In this section, several simulations are performed using LTspice to verify proper operation of the USB-C power adapter, and that the design meets the specified requirements. Figure 4.8 shows the schematic diagram of the LTspice simulaion file. The simulations include the LTC3892 Dual Phase Synchronous Buck Controller, and the LT3012 Low Dropout Regulator. Switches 1-4 resemble the power delivery controller adjusting the feedback path to the buck controller so that the desired output voltage level is supplied to the load. The input voltage source is modeled by a DC voltage source set to the nominal input voltage of 48V. All simulations are performed under full load, with an output current and voltage of 5A and 20V, respectively.

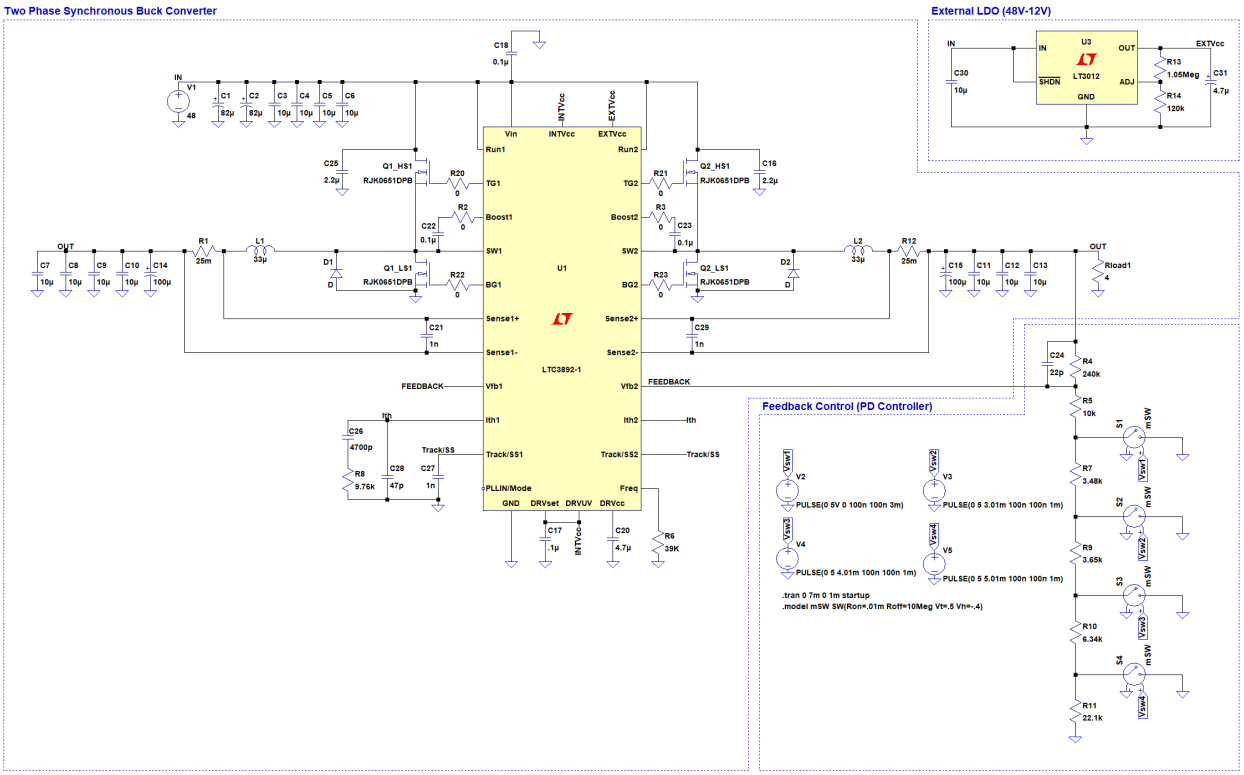


Figure 4.8: Schematic diagram for the LTspice simulation file

4.3.1 Output Voltage at Multiple Levels

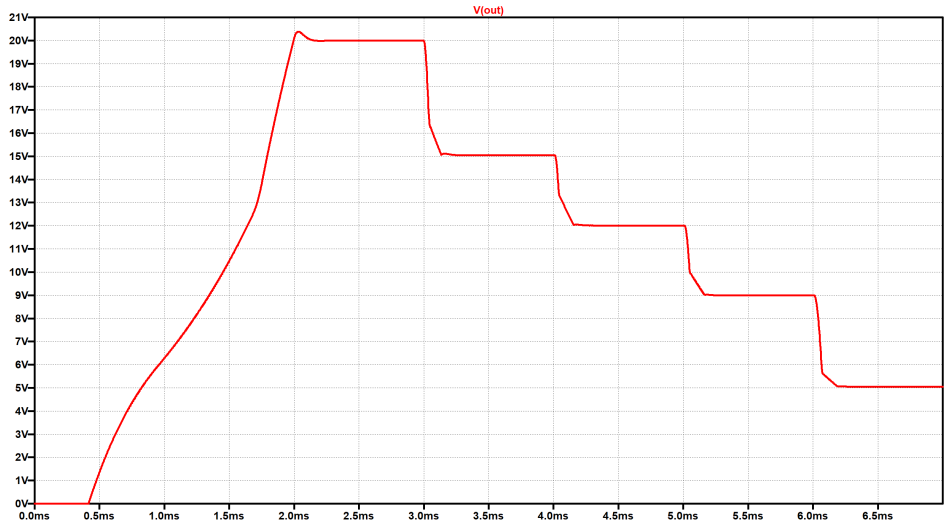


Figure 4.9: LTspice simulation of the output voltage at multiple levels

Figure 4.9 demonstrates the system's capability of supplying various output voltages. Utilizing the switches shown in Figure 4.8 to mimic the power delivery controller, the voltage is changed between 5, 9, 12, 15, and 20V. The simulation verifies that the system operates as intended and that the correct output voltages are supplied to the load.

4.3.2 Full Load Output Current and Voltage

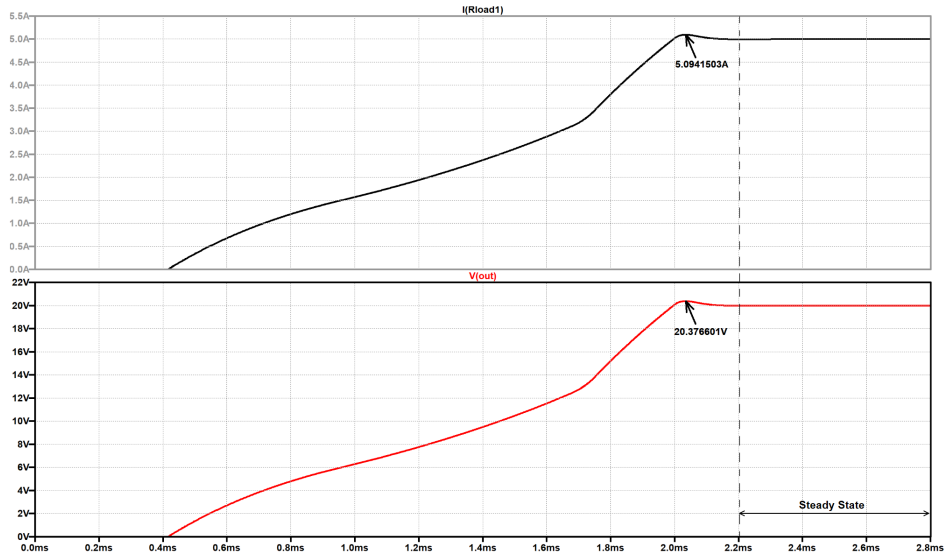


Figure 4.10: LTspice simulation of the output voltage and current

The output voltage and current waveforms of Figure 4.10 reach steady state at approximately 2.2 ms. The transient time is well within the 5 ms output settling time specified in Chapter 3. The voltage peaks at approximately 20.4V and the current peaks at approximately 5.1A before reaching steady state.

4.3.3 Inductor Current and Voltage

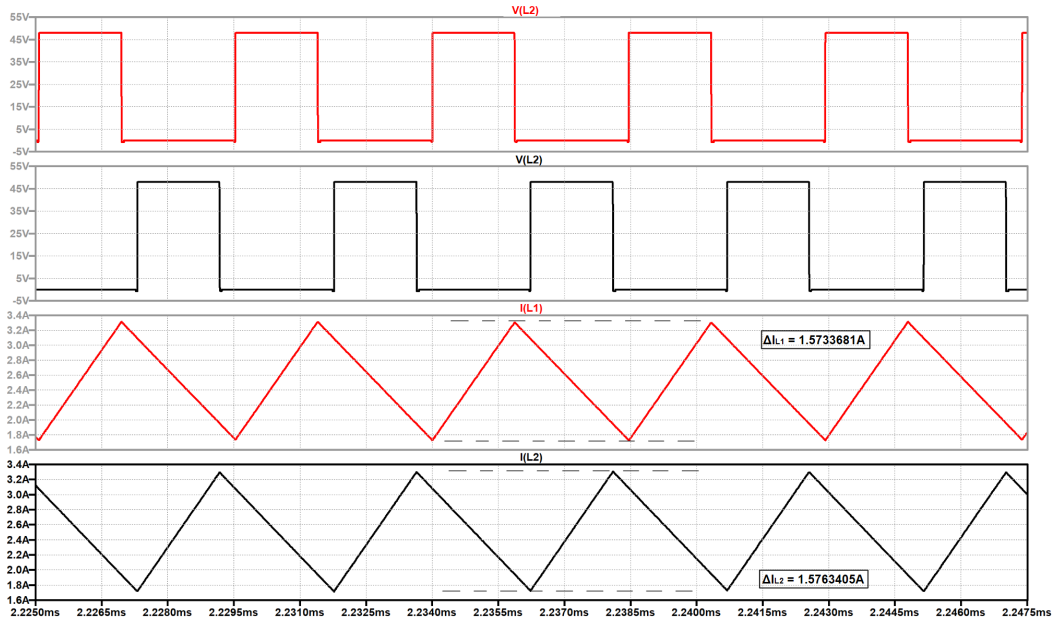


Figure 4.11: LTspice simulation of the inductor voltages and currents for both phases.

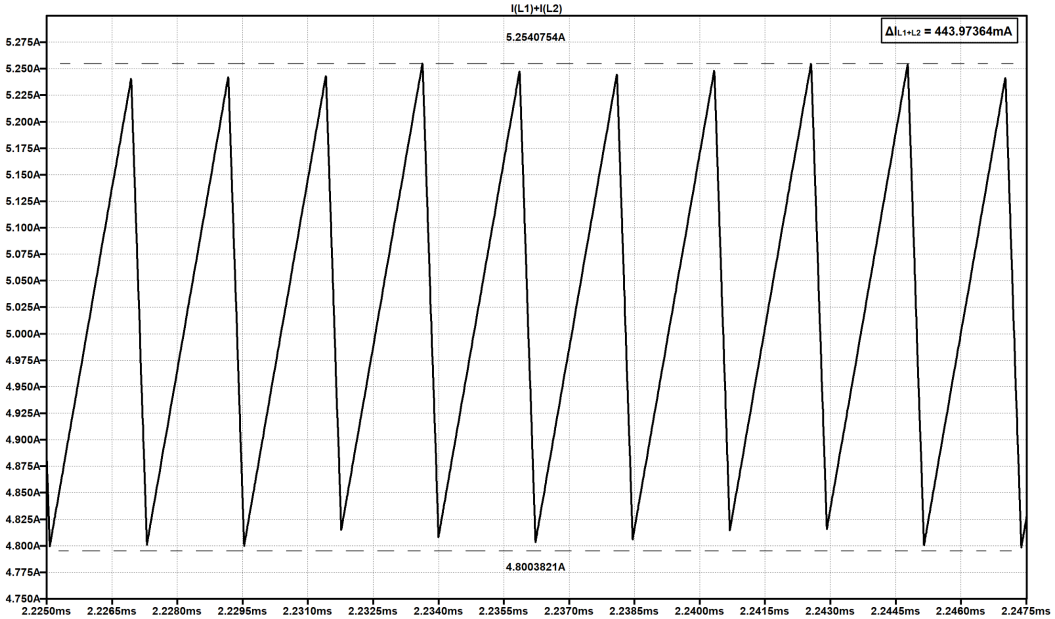


Figure 4.12: LTspice simulation showing the sum of the inductor currents

The inductor ripple currents are approximately 1.57A for each individual phase, which is close to the 1.75A ripple current specified previously under the inductor sizing section. One of the main advantages of using a two phase buck converter is observed when summing the two inductor currents. The ripple of the inductor currents summed together is about 444mA. This significant reduction in ripple current lowers the amount of output capacitance required to keep the output voltage ripple within a desired range.

4.3.4 MOSFET Switching Waveforms

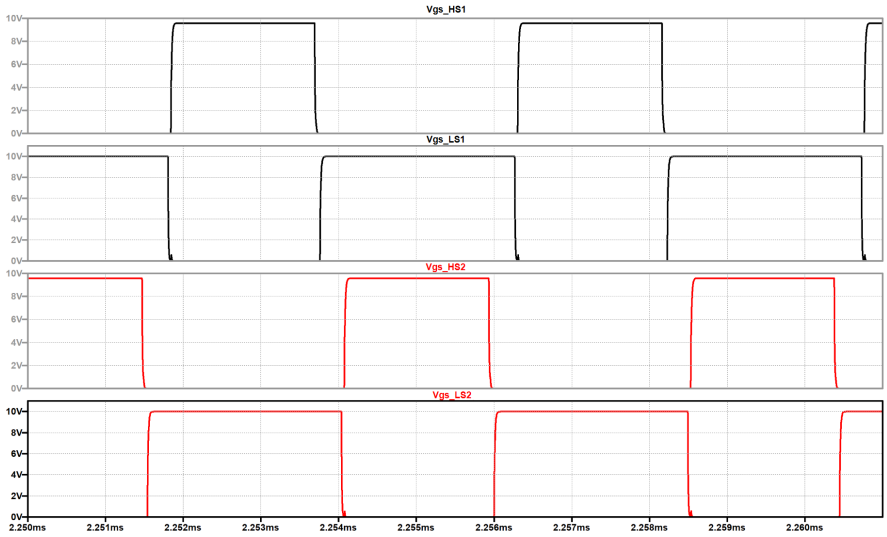


Figure 4.13: LTspice simulation of showing the MOSFET switching in both phases

The waveforms shown in Figure 4.13 verify proper operation of the two phase synchronous buck converter. As expected, the high side MOSFET's are 180^o out of phase with each other. The low side MOSFET's are the compliment of their corresponding high side MOSFET. That is, when the high side MOSFET conducts, the low side MOSFET of that phase does not conduct.

4.3.5 Output Voltage Ripple

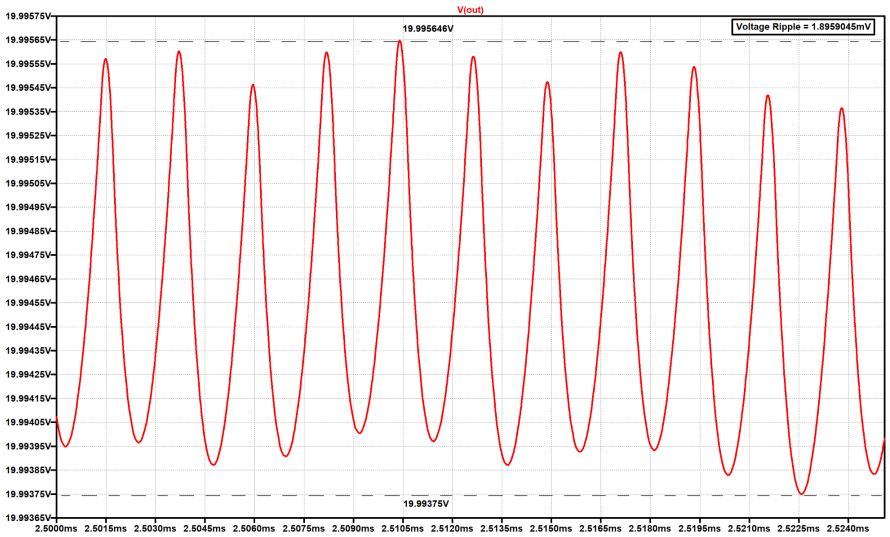


Figure 4.14: LTspice simulation of the output voltage ripple

The output voltage ripple shown in Figure 4.10 is approximately 1.9 mV. This voltage ripple is less than 0.01% of the 19.994V average output voltage. The voltage ripple is well within the ±1% output voltage ripple specified in Chapter 3.

4.3.6 Output Capacitor Current

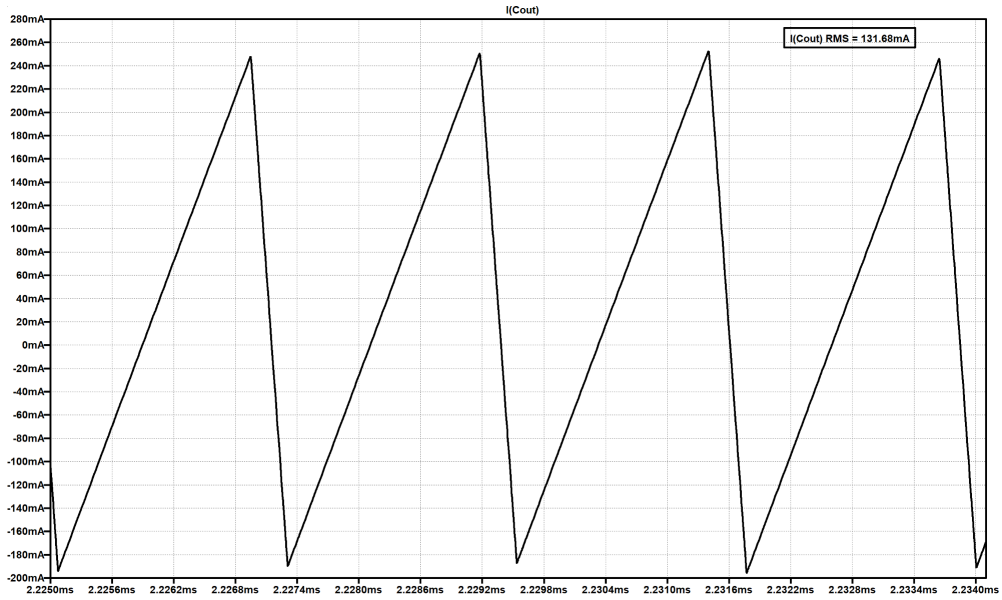


Figure 4.15: LTspice Simulation of the output capacitor current

The output capacitor current in shown in Figure 4.11 has an RMS value of 131.68 mA. The peak to peak value of the capacitor current is about 440 mA, which is equal to the ripple produced by summing the inductor currents from both phases. The simulation verifies that the output capacitor current is the AC component of the inductor current, which further signifies the benefit of using a multi-phase buck converter.

4.3.7 Line and Load Regulation

For load regulation, two separate simulations were performed with the input voltage set to a nominal 48V and full load current at 5A. The simulations were performed at 10% and 90% of full load. The output voltage is recorded for both the low and high load conditions and used to determine the expected load regulation.

$$Load\ Regulation\ =\ \frac{V_{out(low-load)} - V_{out(high-load)}}{V_{out(high-load)}} \times 100\% = \frac{19.995V - 19.994V}{19.994V} \times 100\% =\ 0.005\%$$

For the line regulation, the nominal input voltage to the system is expected to be around 48V. However the input source may vary by $\pm$ 10%. To calculate the expected line regulation, simulation results are recorded for the output voltage with the input source set at its nominal, high, and low values.

$$Line\ Regulation = \frac{V_{out(high-input)} - V_{out(low-input)}}{V_{out(nominal-input)}} \times 100\% = \frac{19.995 - 19.994V}{19.995V} \times 100\% =\ 0.005\%$$

4.3.8 Efficiency

In chapter 3, it was specified that the desired full-load efficiency must be greater than 80%. The 97.63% efficiency obtained from the simulation is well above that 80% limit.

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{99.946W}{102.37W} \times 100\% = 97.63\%$$

4.3.9 Summary of Simulations

Table 4.1: Tabulated simulation results for the full load case

Parameter	Desired Value	Simulated Value	Units
Output Voltage (Average)	20	19.994	V
Output Voltage (Ripple)	<1	0.01	%
Output Current (Average)	5	4.9986	A
Output Current (Ripple)	-	0.012	%
Time to steady-state	<5	2.2	ms
Inductor Current per phase (Ripple)	1.75	1.573	A
Sum of Inductor Currents (Ripple)	500	444	mA
Switching Frequency	230	224.508	kHz
Output Capacitor Current (Ripple)	500	444	mA
Output Capacitor Current (RMS)	-	131.68	mA
Efficiency	>80	97.63	%

Table 4.2: Tabulated simulation results for miscellaneous cases

Parameter	Desired Value	Simulated Value	Units
Output Voltage(s)	15	15.04	V
	12	12.01	V
	9	8.991	V
	5	5.046	V
Line Regulation	<2	0.005	%
Load Regulation	<2	0.005	%

4.4 Conclusion

The solution statement is realized through the design considerations and simulations outlined in this chapter. The simulations verify the design process, and confirm that the proposed system behaves as intended. The design requirements outlined in chapter 3 are met, and the simulated results correspond to the desired values. As shown in Table 4.1, the line and load regulation are well within the intended range. In addition, the system is highly efficient at 97.63%, which is more than the desired 80% full load efficiency.

The significant improvements over the previous works detailed in Chapter 2 are realized in this Chapter as well. The system displayed versatile output characteristics with the output voltage alternated between 5, 9, 12, 15, and 20V depending on the desired output voltage level. In addition, the 97.63% efficiency of this system is much higher than the 71% efficiency reported in the DC House cell phone charger project [12].

Although the specifications listed in Table 4.1 are most likely to worsen with the actual hardware implementation of system, the simulations offers a glimpse into what the expected results would look like. The hardware test results are not expected to vary significantly from the simulated results, however, careful hardware design considerations much be taken into account to ensure that the possible error sources are minimized.

5 Hardware Test and Results

5.1 Hardware Actualization

In this section, the physical implementation of the design outlined in Chapter 4 will be discussed. These physical aspects primarily concern component selection, PCB design, and PCB assembly. These design aspects are just as important as the circuit design outlined in Chapter 4, especially for switching power supplies. However, due to the number of small design choices which contribute to the overall design, this report will only detail those which need specific note. This section then prepares the design of Chapter 4 for hardware testing in later sections.

5.1.1 Selection of Design Software

There are many PCB design suites which would provide the functionality needed to design our PCB. KiCAD Electronic Design Automation Suite is chosen for a number of reasons. Firstly, KiCAD is cross platform across the three major desktop platforms, open-source, and free. Secondly, members of our team are most familiar with KiCAD making the learning curve of PCB design within the software shallower. One typical downside of KiCAD compared to other PCB design suites is the lack of an auto-router; however, this wasn't an issue for this project. This is because in a power electronic circuit design the placement, size, and routing of traces are important to the proper functioning of the circuit. As such, we route every trace manually and deliberately. In all, KiCAD is a sufficient PCB design suite and it serves as an important design tool.

5.1.2 Schematic to be Actualized

This section, outlines the entire and final schematic used for the hardware design of this project. Figure 5.1 shows the final schematic. This schematic is primarily a composite of schematics show in Figure 4.4, Figure 4.6, Figure 4.7, and Figure 4.8. However, additional components are added related to connections off-board including the USB-C connector itself. Hardware design aspects related to the schematic of Figure 5.1 will be further considered to detail the physical manifestation of the aforementioned schematic.

5.1.3 Component Selection

Table 5.1 shows the hardware selected for each component in the schematic of Figure 5.1. Due to the number of components these selections won't be detailed individually; however, some general guidelines used to make these selections will be discussed, as well as a few noteworthy selections. First, all resistors with the exception of R1 and R12, the current sense resistors, weren't on the power path. As such, these resistors were chosen primarily by size. Resistors with an 0805 footprint are chosen since they are small enough to reduce PCB area and cost, but can still be soldered by hand. Capacitors in the power path were chosen primarily to satisfy the maximum voltage and ripple current needs at their point in the circuit. These requirements for relevant capacitors are discussed in Chapter 4. The inductors used in the system were chosen such that the saturation and rated current exceed the maximum instantaneous inductor current and average output current of the system, respectively. MOSFETs were primarily chosen such that the maximum V_{DS} drop and the maximum average drain current weren't exceeded. Finally, other components such as the power delivery controller were chosen with packages that would be relatively easy to solder by hand.

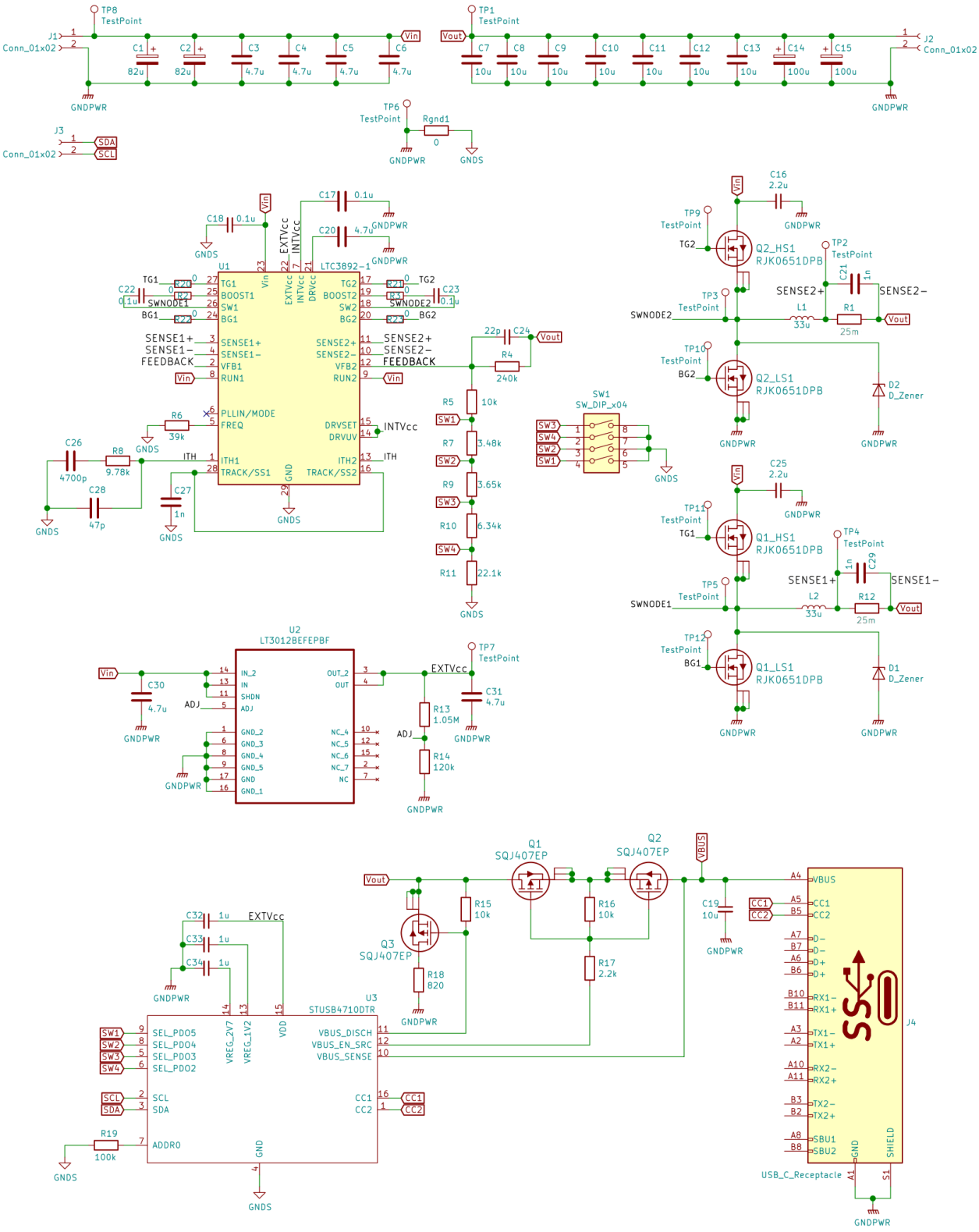


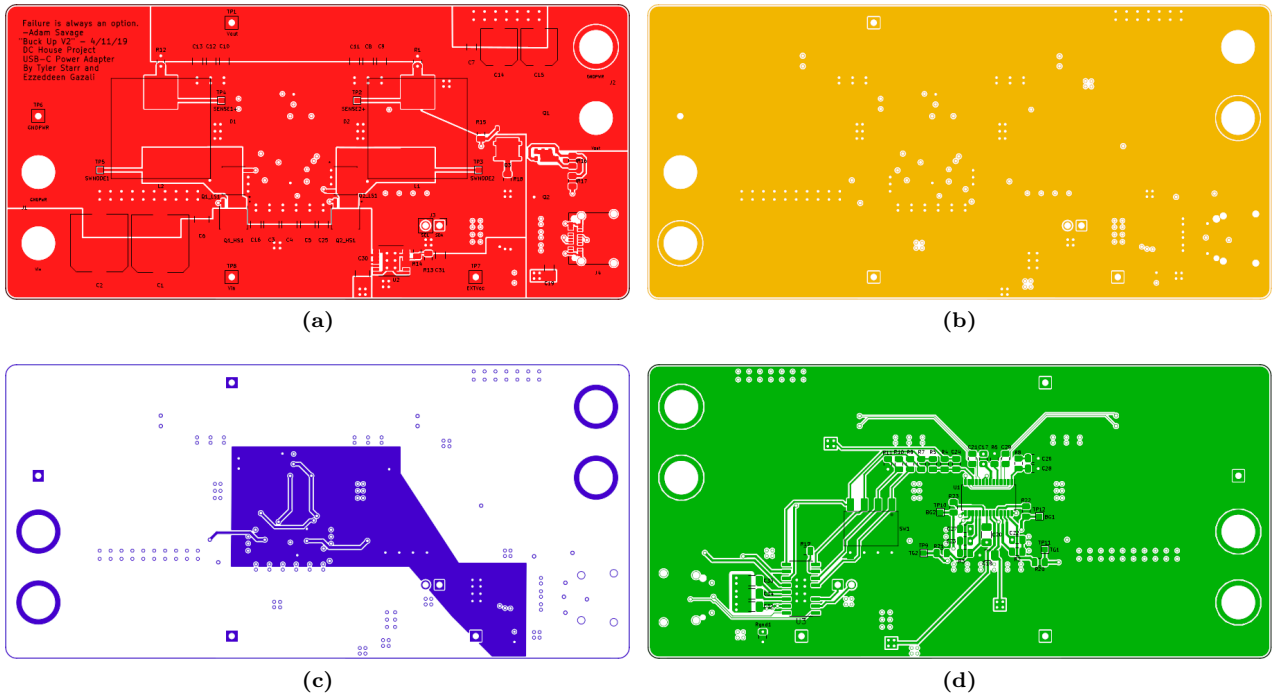
Figure 5.1: Full schematic of system to be actualized

Table 5.1: Tabulated list of components selected for design

Index	Identifier(s)	Description
1	R1, R12	RES 0.012 OHM 1% 1/2W 0805
2	R8	RES SMD 9.76K OHM 1% 1/8W 0805
3	R6	RES SMD 39K OHM 0.5% 1/10W 0805
4	R4	RES SMD 240K OHM 0.5% 1/10W 0805
5	R5, R15, R16	RES SMD 10K OHM 0.5% 1/10W 0805
6	R9	RES SMD 3.65KOHM 0.5% 1/10W 0805
7	R11	RES SMD 22.1K OHM 0.1% 1/8W 0805
8	R13	RES SMD 1.05M OHM 1% 1/8W 0805
9	R14	RES SMD 120K OHM 1% 1/8W 0805
10	R10	RES 6.34K OHM 1% 1/8W 0805
11	R7	RES SMD 3.48K OHM 1% 1/8W 0805
12	R2, R3, R20, R21, R22, R23, Rgnd1	RES 0 OHM JUMPER 1/8W 0805
13	R17	RES SMD 2.2K OHM 1% 1/8W 0805
14	R19	RES SMD 100K OHM 1% 1/8W 0805
15	R18	RES SMD 820 OHM 1% 1/8W 0805
16	C1, C2	CAP ALUM POLY 82UF 20% 63V SMD
17	C7,C8,C9,C10,C11,C12,C13,C19	CAP CER 10UF 50V X5R 1206
18	C3,C4,C5,C6,C30	CAP CERAMIC 4.7UF 100V X7S 10% P
19	C18	CAP CER 0.1UF 100V X7R 1206
20	C16,C25	CAP CER 2.2UF 100V X7S 1206
21	C17,C22,C23	CAP CER 0.1UF 50V Y5V 0805
22	C14,C15	CAP ALUM POLY 100UF 20% 35V SMD
23	C21,C27,C29	CAP CER 1000PF 50V C0G/NP0 0805
24	C24	CAP CER 22PF 50V C0G/NPO 0805
25	C26	CAP CER 4700PF 50V X7R 0805
26	C28	CAP CER 47PF 50V C0G/NP0 0805
27	C20,C31	CAP CER 4.7UF 25V X7R 1206
28	C32,C33,C34	CAP CER 1UF 25V X7R 1206
29	L1, L2	FIXED IND 33UH 8.5A 21.7 MOHM
30	D1,D2	DIODE SCHOTTKY 40V 2A DO214AA
31	Q1_HS1, Q2_HS1, Q2_LS1, Q2_LS1	MOSFET N-CH 60V 25A LFPAK
32	Q1, Q2, Q3	MOSFET P-CH 30V 60A POWERPAKSO-8
33	U1	IC REG CTRLR BUCK 28TSSOP
34	U2	IC REG LIN POS ADJ 250MA 16TSSOP
35	U3	STAND-ALONE USB PD CONTROLLER (W
36	J1, J2	CONN BANANA JACK THREADED RED
37	J1, J2	CONN BANANA JACK THREADED BLACK
38	J3	CONN HEADER VERT 2POS 2.54MM
39	J4	CONN RCP USB3.1 TYPEC 24P SMD RA
40	SW1	SWITCH SLIDE DIP SPST 25MA 24V
41	TP1-10	PC TEST POINT MULTIPURPOSE WHITE

5.1.4 PCB Layout

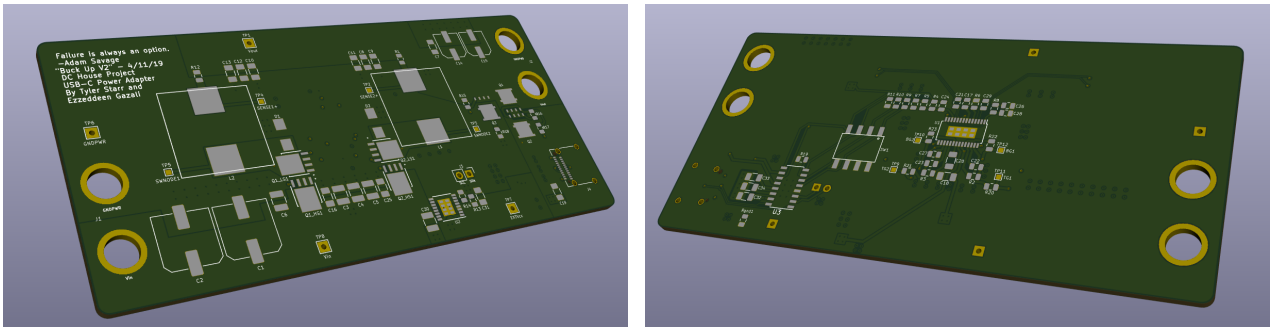
Figure 5.2 shows each layer of the board fielded for actualization and testing of the design outlined in Chapter 4. This will not be an exhaustive description of every design decision, but a description of a few relevant considerations, as well as generalized design principles exercised through the design. First, the design is a four layer PCB with a layer for power connections and components, a layer for power ground, a layer for signal ground, and a layer for signal connections and components. This choice of layering provides many key benefits. First, the solid power ground plane reduces ground loops and thus noise on converter's switching nodes. The large copper planes used for power connections ensures direct and low impedance paths for high current from input to output. Additionally, this separates noisy switching nodes from the sensitive signal nodes with two internal ground planes which act as an EMI shield. Finally, four layers provides routing flexibility which allows easy routing of the short and wide traces required for the buck controller's gate drivers. Additionally, switching nodes are minimized to reduce the EMI produced by the larger voltage swings seen at the switch node. Beyond this, many smaller design guidelines and considerations were made when designing the PCB many of which were derived from a particularly relevant application note by Analog Devices [21]. The final PCB design measures 114mm by 54mm. The PCB was then manufactured with OSHPark's four layer prototype service which features $1oz/ft^2$ copper on the top and bottom layers and $0.5oz/ft^2$ copper on the interior layers all on an FR408 substrate. Figure 5.2 shows colorized plots of each layer for the designed PCB with Figure 5.3 showing KiCAD's 3d render of the board without components.



(a) **(b)**

(c) **(d)**

Figure 5.2: (a) Layer 1 of fielded PCB (b) Layer 2 of fielded PCB (c) Layer 3 of fielded PCB (d) Layer 4 of fielded PCB

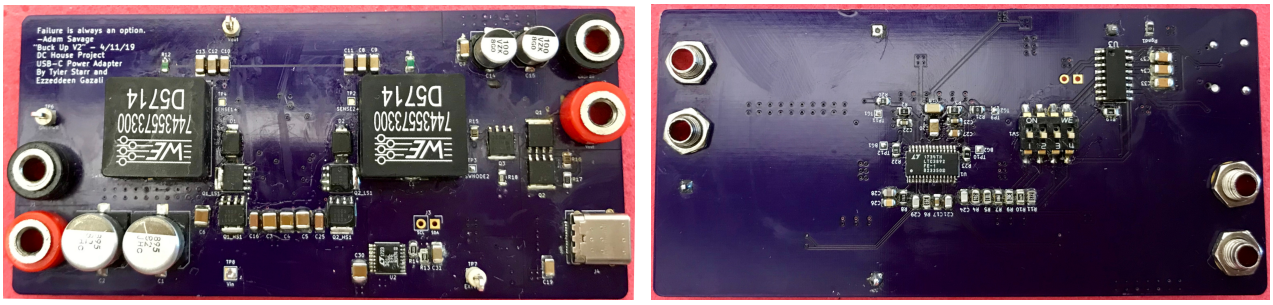


(a) **(b)**

Figure 5.3: (a) 3d render of the frontside of the PCB
(b) 3d render of the backside of the PCB

5.1.5 PCB Assembly

Upon receipt of our PCB prototype from OSHPark the board was visually inspected and tested for continuity various key nodes. This was particularly important since our input voltage, 48V, if shorted to certain nodes in the circuit could damage components. Since, the design was fielded with hand-soldering in mind the plurality of components were soldered by tinning the pads of the PCB with a soldering iron, applying liquid flux to the area, and reflowing the solder and component using a hot-air rework station. However, this technique wouldn't work for all components namely the USB-C connector itself. The USB-C connector has pads under the connector and plastic very near the pads. As such, a low melting solder paste, Kester EP256, was applied to the pads under the USB-C connector. Then a hot-air station at a low temperature was used to heat the opposite side of the board. This allowed for the proper reflow and connection of pads under the USB-C connector while preventing damage to plastic parts of the connector. Figure 5.4 shows the finished PCB assembled in the manner previously described.



(a) **(b)**

Figure 5.4: (a) Frontside of assembled PCB
(b) Backside of assembled PCB

5.2 Hardware Testing

In this section, the designed USB-C power adapter is tested to ensure proper operation. Various measurements are performed to verify the design specifications are met. The measurements are displayed in the following subsections, as well as a summary at the end of the section with tabulated data containing all relevant parameters.

5.2.1 Test Setup

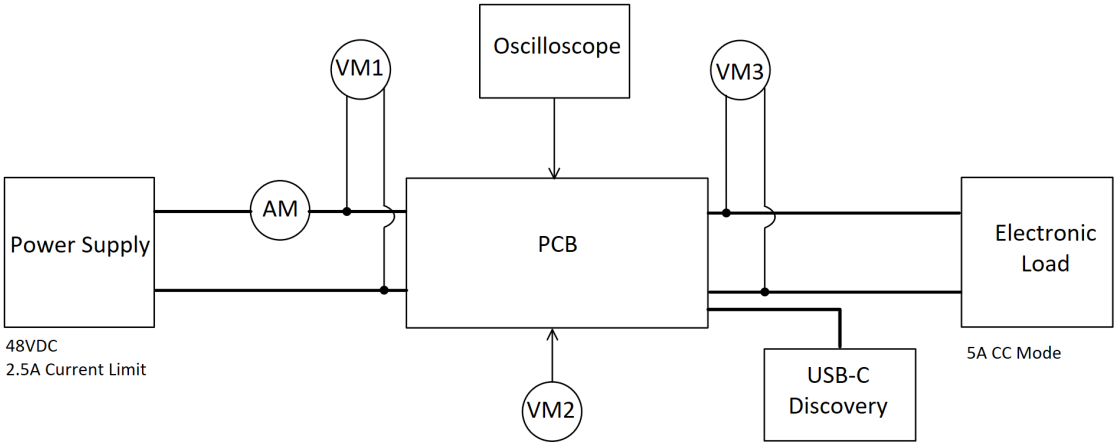


Figure 5.5: Block Diagram of the test setup

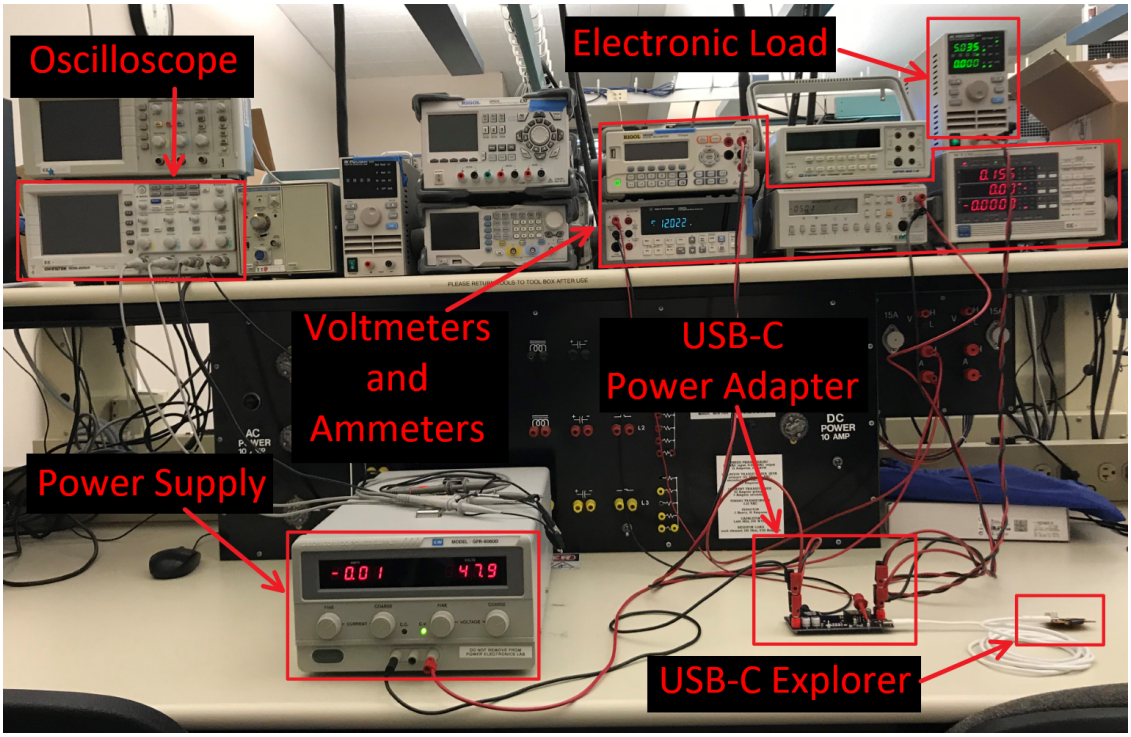


Figure 5.6: Image of the setup used to test the system

The block diagram of Figure 5.5 shows the setup, used to the test system. First, a power supply is used to supply the system with 48VDC, and electronic load set to draw a constant 5A is connected at the output of the system. An ammeter is used to measure the input current into the system. Additionally, a voltmeter (VM1) is used to measure the voltage directly at the input of the system to ensure that the input voltage is as accurate as possible and to account for any voltage drop from the cables used in the test setup. Similarly, a voltmeter (VM3) is placed directly at the output of the system. VM3 is used to measure across various pins on the PCB and to monitor the LDO output voltage. A 4-channel oscilloscope is used to measure the MOSFET switching, output voltage ripple, and inductor current and voltage waveforms. An image of the actual test setup is shown in Figure 5.6. The oscilloscope measurements are performed on the TELEDYNE LECROY HDO4104, however, since it is on another lab bench the oscilloscope in Figure 5.6 is shown as a place holder.

NOTE: The BK PRECISION 891 LCR Meter is used to measure the inductance of the inductor used in the power adapter, however it is not included in the block diagram of Figure 5.5

5.2.2 Overall System

In this section, the overall system is tested to ensure that the specifications detailed in chapters 3 and 4 are met. In addition, the thermal performance of the system is investigated as well.

5.2.2.1 Full Load Voltage Rise Time

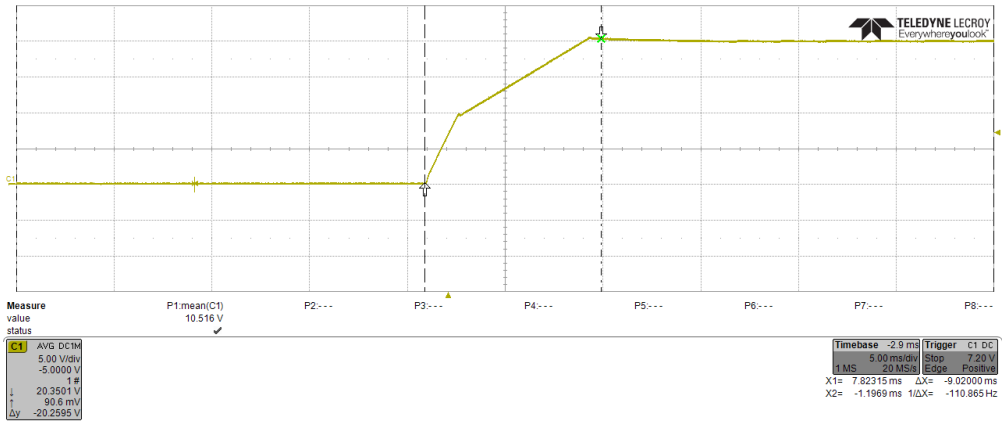
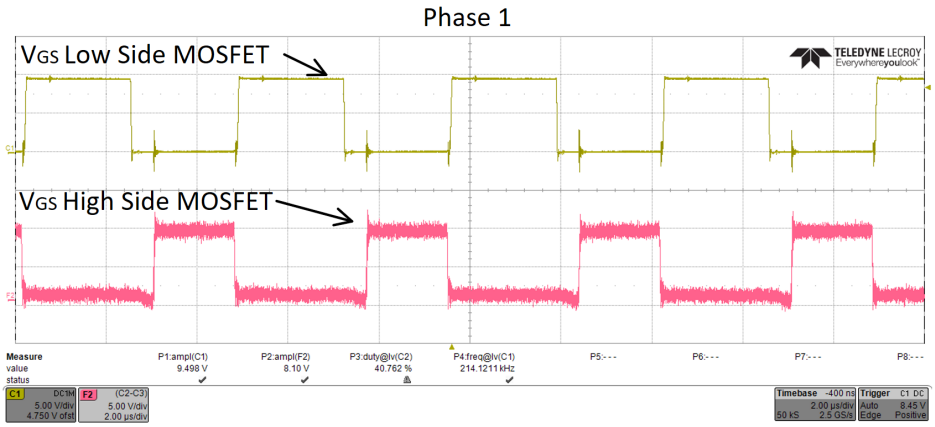


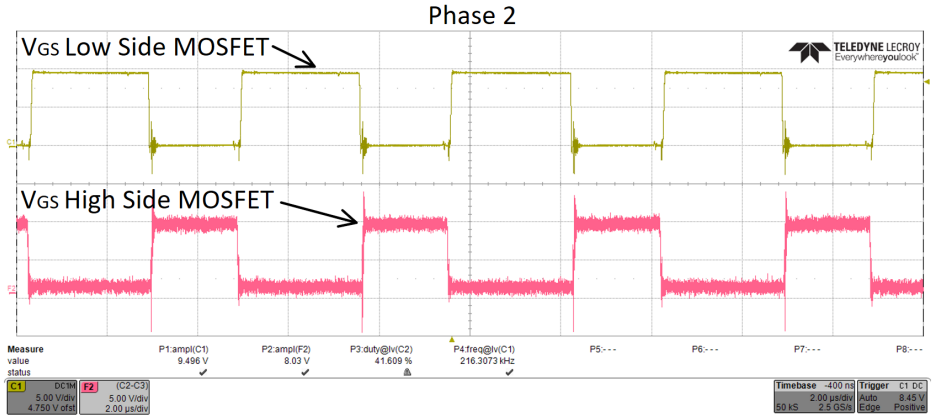
Figure 5.7: Output voltage waveform from start-up to 20V output

The waveform in Figure 5.7 shows the amount of time it takes for the output to rise from 0V to 20V at full-load. As evident, this time is 9.02ms. This is about 7ms longer than the simulated rise time in Chapter 4. However, this is expected since the soft-start capacitor was increased from $1nF$ to $0.1\mu F$ between the simulation and hardware testing. Furthermore, this isn't a concern for our required settling time as outlined in Chapter 3. Negotiations between source and load are made after the converter has achieved a 5V output. Thus, the increased start-up time due to the soft-start capacitor won't slow the converter output voltage transitions that result from power negotiations with loads.

5.2.2.2 MOSFET Switching Waveforms



(a)



(b)

Figure 5.8: (a) Low side and high side switching waveforms for phase one (b) Low side and high side switching waveforms for phase two

The waveforms shown in Figure 5.8 verify that the two phase synchronous buck converter operate properly. As expected, the low side MOSFET's are the compliment of their corresponding high side MOSFET. That is, when the high side MOSFET conducts, the low side MOSFET of that phase does not conduct and the opposite is true. Additionally, the switching frequency is about 215kHz and the duty cycle is around 40%.

5.2.2.3 Output Voltage Ripple

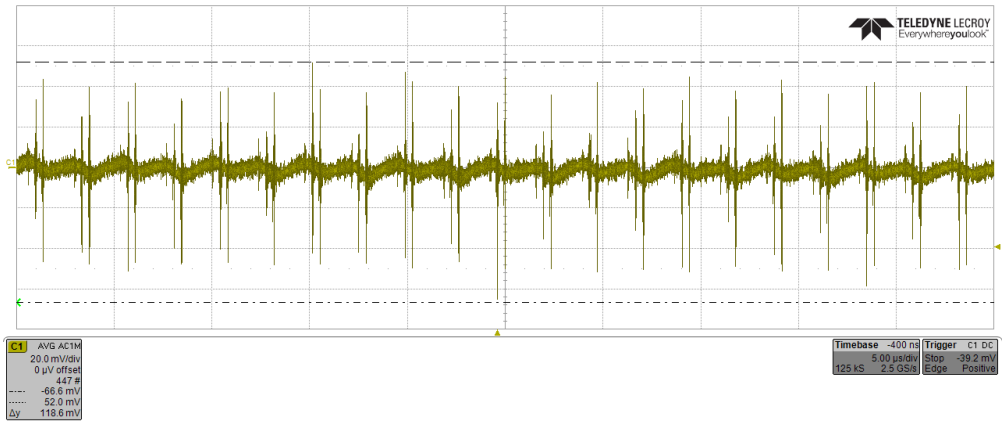


Figure 5.9: Output voltage waveform zoomed to show the ripple and voltage spikes

The output voltage ripple shown in Figure 5.9 is approximately 118.6 mV peak to peak. This voltage ripple is approximately 0.594% of the 19.95V average output voltage. The voltage ripple is well within the ±1% output voltage ripple specified in Chapter 3.

5.2.2.4 Inductor Current and Voltage

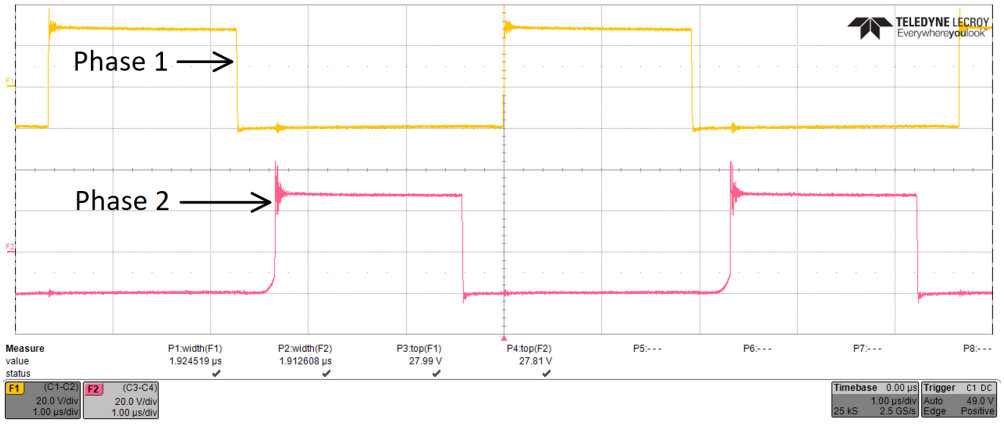
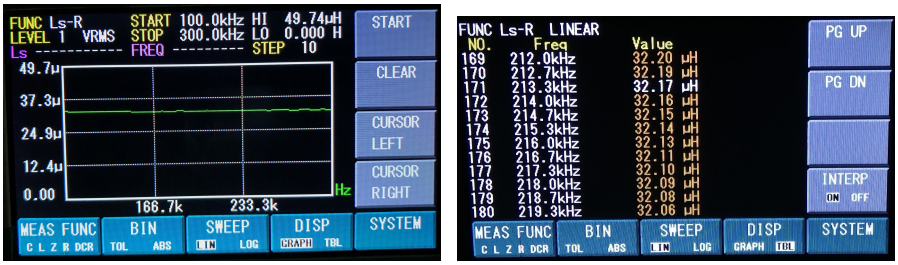


Figure 5.10: Inductor voltage for both phases of buck converter

The inductor voltage waveforms shown in 5.10 verify that the synchronous buck converter operates correctly. The two phases of the converter are compliments of one another. That is, when one phase conducts, the other phase is off. This behaviour is observed in the inductor waveforms. The inductor voltage alternate between $V_{in} - V_{out}$ when that particular phase is "on" and $-V_{out}$ when it is off.



(a) **(b)**

Figure 5.11: (a) Linear sweep of the inductance between 100-300kHz
(b) Tabulated results of the linear sweep

The inductor current couldn't be measured directly; however, it is calculated to be approximately 1.676A. The data obtained from the oscilloscope plot of Figure 5.10 and the inductance of the inductor from Figure 5.11 is used to calculate the current as follows:

Relevant data measured:
$V_{L,ON} \approx 27.99V$
$\Delta t_{ON} \approx 1.925\mu s$
$L \approx 32.14\mu H$ at approximately 215 kHz

$$\Delta I_L = \left(\frac{V_{L,ON}}{L}\right)\Delta t_{ON} = \left(\frac{27.99V}{32.14\mu H}\right)1.925\mu s \approx 1.676A$$

5.2.2.5 Line and Load Regulation

For the load regulation, the input voltage is maintained at its nominal level around 48V. The output voltage is recorded with the system supplying 0.5A and 4.5A, which is 10% and 90% of full load, respectively. The measurements are tabulated in Table 5.3 and the load regulation is calculated as shown previously in the simulation section of Chapter 4. The load regulation of 0.191% obtained from this measurement is well within the specified 2% in the design requirements of Chapter 3.

Table 5.2: Tabulated hardware test results for load regulation

$V_{out\,(low-load)}$	$V_{out\,(high-load)}$	Load Regulation
19.983V	19.945V	0.191%

For the line regulation, the input voltage is adjusted between its nominal level, and ±10% of its nominal level. That is, the input voltage is set to 43.2V, 48V, and 52.8V and the corresponding output voltage is recorded for each input voltage. The output voltages are then tabulated in Table 5.2 and the line regulation is calculated as shown previously in the simulations section of chapter 4. The line regulation of 0.35% obtained from this measurement is well within the specified 2% in the design requirements of chapter 3.

Table 5.3: Tabulated hardware test results for line regulation

$V_{out\,(low-input)}$	$V_{out\,(nominal-input)}$	$V_{out\,(high-input)}$	Line Regulation
19.940V	19.947V	19.946V	0.035%

5.2.2.6 Efficiency

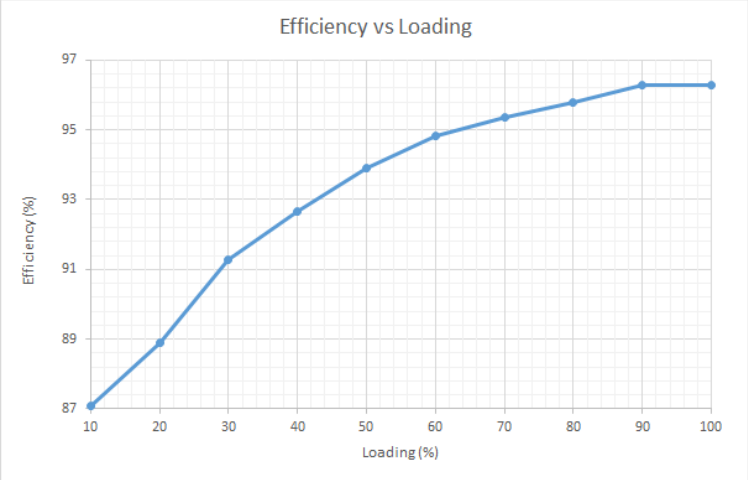
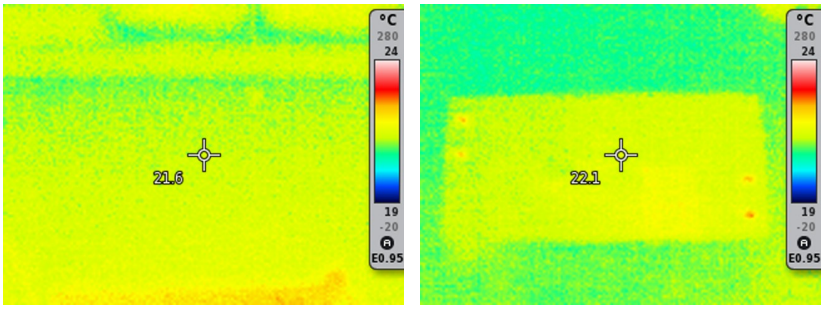


Figure 5.12: Efficiency plot for buck converter from 10% to 100% load

The efficiency plot in Figure 5.12 is obtained by measuring the system efficiency while the load is varied from 10% - 100% in 10% increments. The minimum efficiency of 86.71% is observed at 10% of full load, while the maximum frequency of 96.27% is observed at full load. The efficiency of the system is well above the specified 80% efficiency at full load.

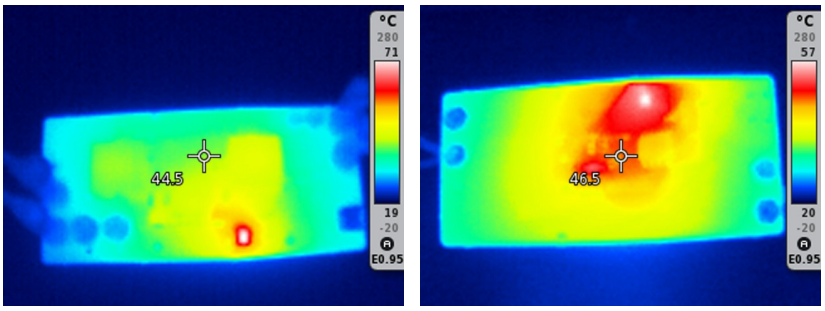
The efficiency measurements shown in Figure 5.12 exhibit the behavior expected from a buck converter. The converter losses consist of static losses related to the resistance of components in the system and dynamic losses related to the switching frequency and capacitance in the system. The losses remain relatively constant since the components and switching frequency are not changed as the load varies between light load and full load. However, output power does change as the load is varied. The output power is less at light loads and it increases at full load. Since, the efficiency is defined as $\eta = \frac{P_{out}}{P_{out}+P_{losses}}$, the effect of power losses becomes more significant at light loads contributing to a lower efficiency.

5.2.2.7 Thermals



(a) **(b)**

Figure 5.13: (a) Thermal image of front of PCB before test
(b) Thermal image of back of PCB before test



(a) **(b)**

Figure 5.14: (a) Thermal image of front of PCB after test
(b) Thermal image of back of PCB after test

As evident from the images of Figures 5.13 and 5.14 captured using the Testo 870-1 thermal imaging camera, the temperature increased from room temperature at 24^{o}C to a maximum of approximately 71^{o}C. The temperature increase is mainly centered around the LDO. This temperature increase is expected and amounts to less than half of the 150^{o}C that the LDO is rated for[19].

The LDO drops the 48V input source to 12V, resulting in a 36V drop across the component. If we assume that the LDO supplies around 25mA, which is a reasonable assumption given that we couldn't directly measure the current out of the LDO, the resulting output power is approximately 1W. According to the LDO datasheet, the temperature rises 50$\frac{^oC}{W}$ above ambient temperature[19]. This would result in a temperature rise of approximately 74^{o}C, which is around the temperature measured by the thermal imaging camera.

Without the LDO, the LTC3892 would use an internal linear regulator to drop the 48V input voltage to 10V, causing the chips temperature to rise significantly. To avoid this, the LDO was implemented so that the temperature is dissipated in the LDO rather than LTC3892. Future implementations of this system could benefit from a heat sink on the LDO for increased reliability; however, it is not a significant issue since the LDO is still well within its rated operational conditions.

5.2.3 Low Dropout Linear Regulator (LT3012)

In this section, aspects of the system related to the Low Dropout Linear Regulator are considered. This is done to ensure this part of the circuit is operating and supporting other parts of the circuit correctly.

5.2.3.1 Output Voltage

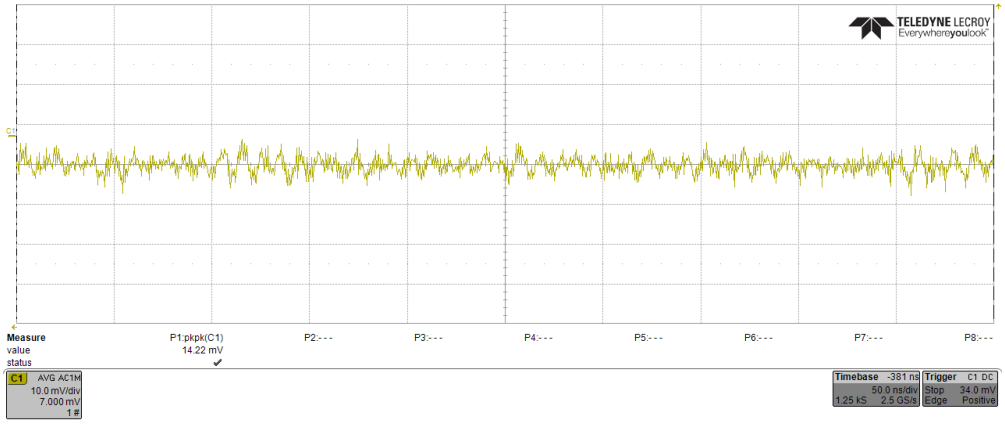


Figure 5.15: Output ripple voltage of LT3012

The output voltage ripple of LDO shown in Figure 5.9 is approximately 14.22 mV peak to peak. The average output voltage of the LDO measured using a voltmeter is approximately 11.984V resulting in voltage ripple of approximately 0.12%. The output voltage of the LDO was monitored throughout the entire course of hardware measurements and it remained constant without any unexpected behavior observed.

5.2.4 USB-C Power Delivery Controller (STUSB4710R)

In this section, aspects of the system related to USB-C Power Delivery Controller are considered. This is done to ensure the system can properly negotiate for and provide power to consumer devices through a USB-C port. Additionally, actual consumer devices are tested to ensure correct operation with USB-C based devices currently available in the market.

5.2.4.1 Power Delivery Profiles

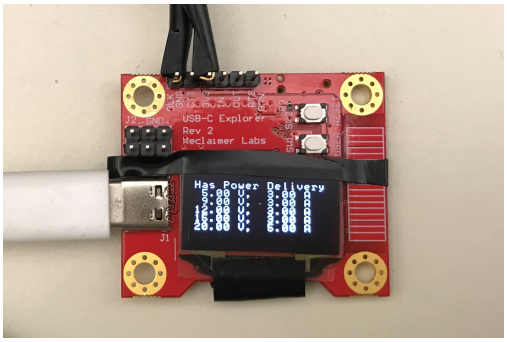


Figure 5.16: Power delivery profile negotiated between the USB-C Explorer and STUSB4710R

By default, the STUSB4710R PD controller advertises 3A for 5V, 9V, 12V, and 15V, and 2.25A for 20V. However, the PD controller can be reconfigured through the I2C pins to a specified power delivery profile. An MSP432 microcontroller is used with the code found in the Appendix section to configure the PD controller to the profile shown in Figure 5.16.

NOTE: For I2C communication between the MSP432 and STUSB4710R, external pull up resistor are required at both the SDA and SCL pins. A 10kΩ resistor could be used to pull up each pin.

5.2.4.2 Negotiated Output Voltages

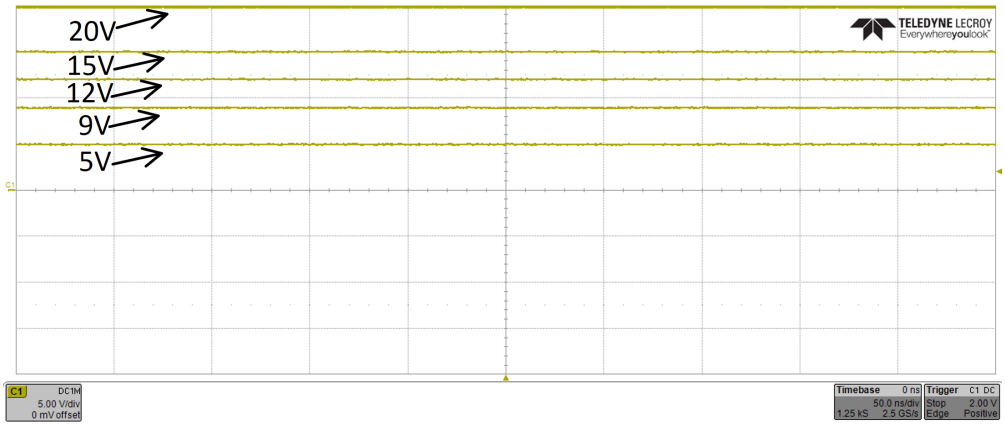


Figure 5.17: Oscilloscope plot showing successful power delivery negotiation

Table 5.4: Tabulated data for the voltages negotiated between the USB-C Explorer and the PD controller

Desired Voltage [V]	Negotiated Voltage [V]
20	19.896
15	14.986
12	12.025
9	8.977
5	5.023

The negotiation process between the USB-C Explorer and the PD controller is performed for the delivery profile that advertises the highest power. To ensure that the negotiation and advertising is performed properly, the PD controller is configured to advertise no current on all power delivery profiles except the specific profile that we want to test. The oscilloscope plot of Figure 5.17 is captured with 100% persistence on single trigger mode to capture all negotiated voltage levels on the same plot, while the power delivery profiles are adjusted on the PD controller digitally through a I2C interface. Each negotiated voltage was created by the PD controller re-configuring the feedback network of the buck converter. As such, this test represents automatic voltage reconfiguration of the system without power cycling or manual intervention through the switches. Table 5.4 lists the negotiated voltage levels.

5.2.4.3 Consumer Electronics Test

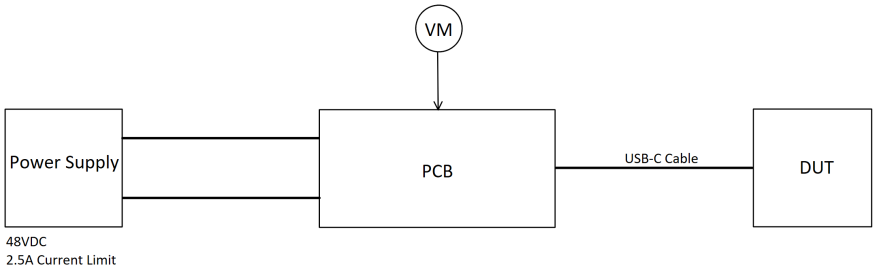


Figure 5.18: Block diagram of the consumer electronics test setup

The best way to test if the USB-C power adapter works with consumer devices is to actually use it to charge an electronic device, and monitor the adapters behavior. For this test, the adapter is connected between the device under test and the power supply with no additional connections except a voltmeter at the output of the adapter to ensure that the PD controller negotiates and outputs the maximum allowable power delivery profile for specific device. The test setup is constructed according to the block diagram of Figure 5.18.

Figure 5.19: Devices charged with the USB-C power adapter

The devices that are tested with the USB-C adapter are shown in Figure 5.19. A Nintendo Switch gaming console is shown above the Samsung Galaxy Buds. Each devices represents a unique type of devices which the system should be able to charge at an appropriate voltage and power. Firstly, the Samsung Galaxy Buds represent a "dumb" device. That is, the Samsung Galaxy Buds don't have specific hardware for performing USB-C power negotiations. These devices are assumed to be 5V devices and assigned a power delivery profile which features a 5V charging voltage. Additionally, the Samsung Galaxy is a new and relevant consumer device since it is released in March 2019. Secondly, the Nintendo Switch represents a "smart" device. That is, the Nintendo Switch has specific hardware for performing USB-C power negotiations. As such, the Nintendo Switch tests the systems ability to negotiate and supply a consumer device which requires a higher charging voltage than 5V. Released in March of 2017, the Nintendo Switch represents a relatively new and very popular consumer device that highlights the shift towards USB-C as the primary method for power delivery. Additional consumer devices may be tested in the future; however, these consumer devices were the only ones we currently have available.

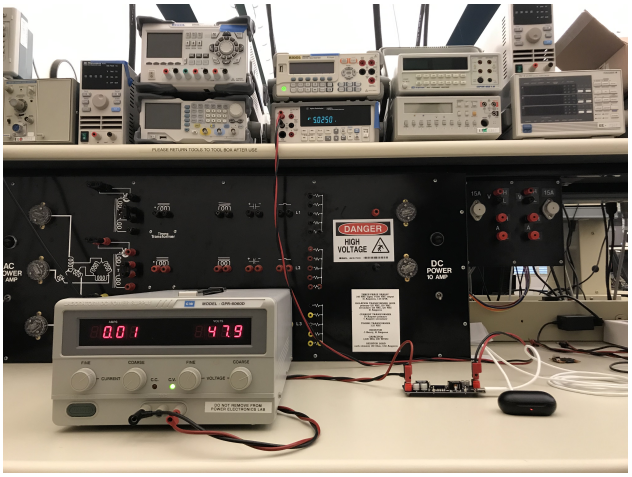


Figure 5.20: Samsung Galaxy Buds charging with the USB-C power adapter

As shown in Figure 5.20, a red led turns on indicating that the headphones are charging. Measuring the voltage at the output of the adapter yields approximately 5.046V. Since, measuring the output current over the USB-C port is difficult the power consumed by the Samsung Galaxy Buds is estimated to be 0.5W using the input source. Although the PD controller advertises 3A at 5V resulting in up to 15W of power charging capability, this is expected since the Samsung Galaxy Buds are small and low power device. Additionally, the headphones were near full charge at the time that they were connected to USB-C adapter and therefore require less power.

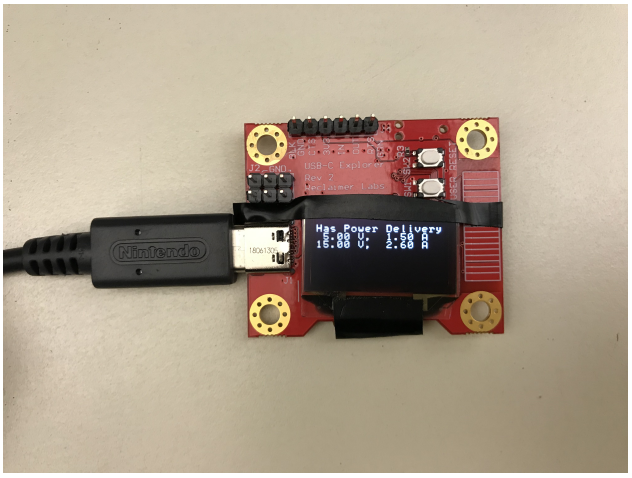


Figure 5.21: Charging capabilities of the Nintendo Switch

For the Nintendo Switch, the devices power adapter is connected to the USB-C Explorer to observe the charging capabilities of the device as shown in Figure 5.21. The device can charge at 5V and 15V with up to 7.5W and 39W, respectively. When charging the Nintendo Switch through the USB-C adapter, it is expected that the device will charge at the highest power delivery profile advertised by the PD controller, which is 15V and up to 45W.

(a) **(b)**

Figure 5.22: (a) Nintendo Switch charging with the USB-C power adapter
(b) Zoomed in image of the Nintendo Switch charging

As shown in Figure 5.22b, the top right corner on the Nintendo Switch screen shows a battery with a charging symbol indicating that the device is charging. Measuring the voltage at the output of the adapter yield approximately 14.931V. This indicates that power delivery negotiation process was successful and the devices is charging at the highest available power delivery profile. Similar to the Galaxy Buds, the voltages, the Nintendo switch was near full charge when connected to the USB-C adapter and required less power than the advertised 45W. A rough estimate based on the input power to the USB-C adapter indicated that the Nintendo Switch is charging between 6W - 7W.

5.2.5 Summary of Hardware Test

For the power delivery controller testing, the USB-C adapter was tested with two separate devices, the Samsung Galaxy Buds and the Nintendo Switch gaming console. Both device charged at the expected power profile and the charging was successful.

Table 5.5: Tabulated hardware test results for full load case

Parameter	Desired Value	Simulated Value	Actual Value	Units
Output Voltage (Average)	20	19.994	19.95	V
Output Voltage (Ripple)	<1	0.01	0.594	%
Output Current (Average)	5	4.9986	4.99	A
Output Current (Ripple)	-	0.012	-	%
Time to steady-state	<5	2.2	9.02	ms
Inductor Current per phase (Ripple)	1.75	1.573	1.676	A
Sum of Inductor Currents (Ripple)	500	444	-	mA
Switching Frequency	230	224.508	≈ 215	kHz
Output Capacitor Current (Ripple)	500	444	-	mA
Output Capacitor Current (RMS)	-	131.68	-	mA
Efficiency	>80	97.63	96.27	%

Table 5.6: Tabulated hardware test results for miscellaneous cases

	Desired Value	Simulated Value	Actual Value	Units
Output Voltage(s)	15	15.04	14.995	V
	12	12.01	12.002	V
	9	8.991	8.966	V
	5	5.046	4.9665	V
Line Regulation	<2	0.005	0.035	%
Load Regulation	<2	0.005	0.191	%
Temperature after 10 minutes of operation	21 - 24 (room temp.)	-	71	°C
LDO Output Voltage	12	12.15	11.984	V

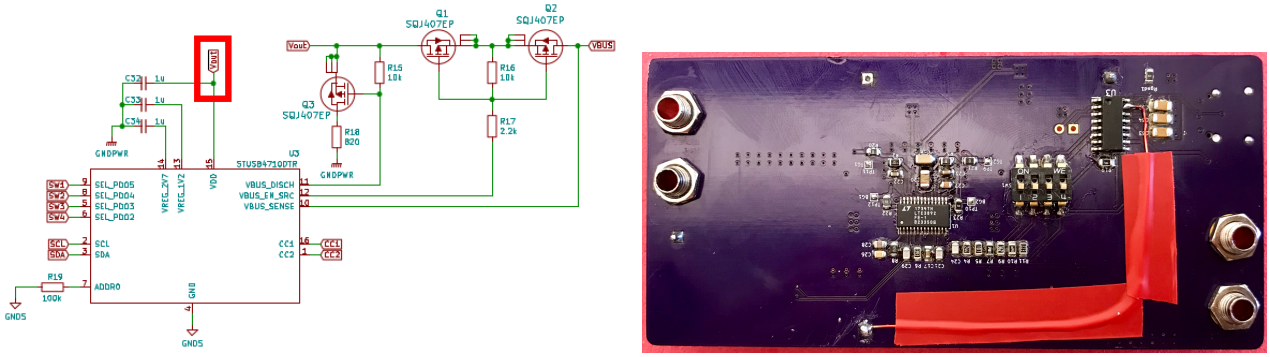
5.3 Revisions

This section serves to review the hardware revisions made to the design during the course of testing due to issues encountered. Firstly, during testing the converter would current limit and shutdown before the full output current of 5A is reached. This was determined to be due to incorrectly calculated resistances for the current sense resistors. These were calculated using the average current and ignoring the inductor current ripple. As such, the current sense resistors, R_1 and R_{12} of Figure 5.1, were changed from $25m\Omega$ to $20m\Omega$ to account for the inductor ripple current.

$$R_{sense} = \frac{75mV}{3.75A} = 20m\Omega$$

In addition, the soft-start capacitor, C_{27} of Figure 5.1, was changed from $1nF$ to $0.1\mu F$. This was done since the converter was exhibiting high input current as start-up. This is due to the high duty cycle the converter would set to attempt to push the output voltage up to the desired voltage. Increasing the soft-start capacitor prevents the converter from setting this high duty cycle and slows the transition to the desired output voltage.

Finally, 5.23 shows that the input power for the power delivery controller was changed from the output of the LDO to the output of the buck converter itself. The power delivery controller senses the output of the buck converter through its power pin to ensure the output is the correct voltage before it connects the output to the load. Since, the power delivery controller's power pin was always 12V since it was powered through the LDO the controller would lock up in an error state on start-up. Changing the source of the power delivery controller resolved this issue.



(a) **(b)**

Figure 5.23: (a) Schematic focalized to changes made to the power delivery circuit
(b) Revision implemented on circuit board using a bodge wire

5.4 Summary of Hardware Testing and Results

The implemented hardware is realized through the design considerations and various hardware tests outline in this chapter. The hardware tests verify the validity of the various design decisions made through the PCB layout design process and confirms that the actualized system operates as intended. The design requirements of Chapter 3 are met, and the hardware tests largely confirm our expectations from the simulations in Chapter 4. Table 5.5 and Table 5.6 summarize the hardware test results compared to that of the desired and simulated results. Additionally, the design is tested with the Nintendo Switch and Samsung Galaxy Buds which represent popular consumer devices which are powered via USB-C. This test with actual consumer electronics affirms the correct operation and full realization of the goal of powering consumer electronics from a DC source without inversion.

Hardware test results largely affirm the simulated results of the design. The full-load efficiency achieved with hardware is 96.27% compared to that of 97.63% of the simulation. This close match in efficiency bodes well for the design and proper operation of the device, especially over an extended period. Again, the achieved efficiency is much higher than the 71% efficiency reported in the DC House cell phone charger project [12].

Finally, the matter of revisions were broached. Throughout testing some relatively minor changes to the design were required to ensure correct operation of the hardware. These included some components swaps in the case of the current sense resistors and soft-start capacitor. However, an issue with the power delivery controller's source of power required a bodge wire to resolve. Given another revision this could be resolved; however, the timeline of this project didn't allow for that revision.

6 Conclusions

6.1 General Project Overview

Traditionally, consumers have received their power by connecting to the AC grid supplied by utility companies. However, most electronic devices convert that AC power to DC power before it can be utilized to charge the connected device. For consumers that are connected to the utility grid, there is no way around this inefficiency. However, with the increasing popularity and adaption of off-grid renewable energy power systems, there is no need for the AC-DC conversion between the power supply source and the load device. The energy generated from renewable sources is usually stored in the form of DC power in battery banks. Therefore, it makes sense to directly utilize the DC power stored in batteries, rather than first converting it to AC power then back to DC.

The DC House Project is a project started by Dr. Taufik at California Polytechnic State University San Luis Obispo. The goal of the project is to provide electricity to people living in rural and secluded communities out of reach of the utility grid. The off-grid homes are powered by renewable or human powered energy sources. The USB-C Power Adapter project presented in this report aims to the directly utilize the DC power stored in the DC House battery system to charge electronic devices. The power adapter takes in 48VDC as an input source and charges electronic devices at 5V, 9V, 12V, 15V, or 20V depending on the load device requirement. The adapter should be capable of charging devices with at least 40W, however the goal is to reach 100W if possible. By directly utilizing the generated DC power to charge the electronics devices, the conversions between AC and DC can be eliminated resulting in reduced power losses which contribute to a more cost effective and efficient system.

The designed system consists of several major components. A power delivery controller advertises the available power delivery profiles that the system can provide. A negotiation process is performed between the power delivery controller and USB-C load devices to determine the suitable power delivery profile for the device. Once the power delivery profile is established, the power delivery controller reconfigures the feedback of a dual phase synchronous buck converter to step down the 48VDC input source to the desired voltage level to charge the USB-C device. A block diagram of the system is shown in Figure 3.2.

6.2 Project Outcome

In this section, the overall end result of the project is presented. More specific discussion of results can be found in the final section of each Chapter. The results of the individual system components as well as the system as a whole is considered. Additionally, the challenges encountered during project are discussed. Finally, the section concludes with a resource analysis of the project.

6.2.1 Project Results

The overall project was a success and the desired specifications outlined in Chapter 3 were all met. The following sections go into more detail about the individual results pertaining to the dual phase synchronous buck controller, power delivery controller, and the overall system.

6.2.1.1 Dual Phase Synchronous Buck Converter

The dual phase synchronous buck converter performed as intended. The maximum output power of 100W was achieved with no issue. The dual phase synchronous operation of the converter was verified as well. As expected, the two phases of the converter were approximately 180^o out of phase. That is, when one phase conducts, the other phase does not conduct. In addition, the switching frequency was around 215kHz which is within the specified 200-250kHz range. Some of the slight variations between the actual converter and the designed and simulated results are likely due to the component tolerances, however, none of the variations were significant enough to become an issue or keep the system from meeting the required specifications.

6.2.1.2 Power Delivery

On the power delivery controller end of the system, the advertising and negotiation process was a success. The PD controller was configured to advertise 5V, 9V, 12V, and 15V with up to 3A, and 20V with up to 5A. The USB-C Power Delivery Explorer was used to verify the advertised power delivery profiles. To further test the PD controller, the system was tested with actual USB-C consumer devices and the results were satisfactory. The Galaxy Buds and Nintendo Switch were both charged without any issues. For the Galaxy Buds, the headphones charged at the lowest power delivery profile at 5V since they are only capable of charging at that specific profile. On the other hand, the Nintendo Switch is capable of charging at both the 5V and 15V power delivery profiles. Therefore, when connecting the Nintendo switching to the system, the device charged at the 15V power delivery profile as expected. The negotiation process between the PD controller and the load devices was successful and the device was charged at the highest available power delivery profile.

6.2.1.3 Overall System

Overall, the system met all the specifications and design requirements outlined in chapter 3. One of the main goals of this project is to provide the DC House Project with an efficient method to charge electronic devices. At full load, the system efficiency is about 96.27% which is well above the required 80% full load efficiency. Even at light loads, the efficiency was still around 86.71%. The output voltage ripple, line regulation, and load regulation were all within their specified ranges. In terms of thermal performance, the system reached a temperature of 71^oC after 10 minutes of operation. However, this temperature increase was mainly centered around the low drop-out linear regulator which is rated for approximately 2 times that temperature. Additionally, when connecting actual consumer devices to the system, they were charged without issue and at the proper power delivery profile.

6.2.2 Challenges Encountered

Although the overall project was a success, several challenges were encountered during the course of this project. These challenges were properly addressed and didn't significantly affect the final outcome of the project. The first and most significant problem encountered was the tendency of the gate drivers on the buck controller integrated circuit to cease working. This would result in a short within the buck controller which subsequently required replacement. The problem that causes this wasn't nailed down to a single factor but attributed to several deficiencies in the PCB layout of the multiphase buck circuit. As such, the improvement of several PCB layout factors, namely shorter and wider gate driver traces and additional ceramic capacitors at various noisy points of the circuit solved this problem.

Additionally, when testing the converter after the initial assembly, the power supply would current limit instantly. The first thought was that there was a short somewhere in the circuit, however after probing various nodes and components, no shorts were found. After careful review of the components selection and consulting with Dr. Taufik, it was determined that the soft-start capacitor used for the buck controller was too small. The converter would require a high input current at start-up in attempt to quickly push the output voltage to the desired level. Increasing the soft start capacitor from 1nF to a 100nF solved this issue.

After solving the soft start issue, the converter would work until approximately 85-90% of full load and shut down. This issue was quickly addressed by swapping the 25mΩ current sense resistor for a 20mΩ resistor. This issue arose due to miscalculations of the current sense resistor in the design stage of the project. The design calculations didn't account for the inductor current ripple and only accounted for the average value of the current.

Another issue was the incorrect connection of the power delivery controller's input power pin. Since the power delivery controller was connected to the output of the LDO, the power delivery controller couldn't detect the output voltage of the buck circuit and thus wouldn't connect the output of buck circuit to loads. This problem was resolved as in the "Revisions" section of Chapter 5.

In addition, an improper connection between the CC pins on the power delivery controller and the USB-C connector resulted in an intermittent connection between the load device and adapter. The surface mount USB-C port used in the power adapter was a little difficult to solder on at first. The port has a plastic piece inside where the pins are housed, which would begin to melt if hot air is applied directly above the connector before the actual solder would melt. To address this issue, low temperature solder paste is applied instead of the traditional solder used to solder the other components. The hot air gun was set at a low temperature of approximately 210^{o}C and used to heat the underside of the PCB directly below the connector. Using this technique, the plastic inside the USB-C connector remained unharmed and successful connection was achieved.

Lastly, when testing the device, the power supply input was incorrectly connected to the banana jack connectors on the output of the device. This back feeding incident caused the MOSFET's on one of the phases to "fry." This issue is likely due to the high V_{GS} drop that occurs when 48V is placed at the output. Although it took some time to trace through the circuit to determine what components were damaged, replacing the MOSFET's solved the issue and the system went back to normal operation.

Overall, the challenges encountered in this project were minor and didn't result in any lasting effect on the operation of the system after they were addressed. The challenges encountered during the course of this project offered a valuable learning experience that resulted in a deeper understanding of power electronics and an appreciation for power electronics design.

6.2.3 Resource Analysis

The EE department at Cal Poly covers up to $200 for each student in a senior project group. Since we have a total of two members working on this project, the EE department covers up to $400 towards expenses related to the project. Additionally, some parts required for the project were sampled through our advisor

and by group members individually. The final cost of the project is $515.19. The discrepancy between this figure and the bill of materials found in the appendix is due to many factors. Firstly, enough components were purchased for two complete prototype boards. Additionally, diagnostic equipment, such as the USB-C Explorer were purchased. The gate driver issue described in the "Challenges Encountered" section caused a few buck controllers to "fry" which increased our costs since the buck controller is the single most expensive component in our circuit. Thus, our project went over budget by about $115 dollars primarily due to our initial inexperience with design of DC-DC converter PCB layouts.

Throughout the project we utilized Calpoly's extensive on campus resources. Specifically, we utilized the power electronics lab for the entire duration of the project. This is an essential resource since most of the project's construction and testing was performed in the power electronics lab. Additionally, solder reflow ovens made available in the graduate student laboratory assisted in the assembly of circuits for testing. Finally, Dr. Taufik served as a key resource throughout this project. His expertise in the field of power electronics provided many insights and suggestions which helped shape key design decisions and ultimately lead to the success of this project.

6.3 Recommendations for Future Work

The efforts of this project are largely considered successful; however, there is room for many potential improvements. These improvements range from small corrections which maintain the current feature set and large overhauls which add significant functionality. Additional functionality will yield better DC based power delivery options for potential devices within the DC House Project.

A possible improvement to the system would include a heat sink for the LDO, or possibly replacing the LDO with a single phase buck converter. Although the temperature rise is insignificant, possible issues could arise from long hours of operation, or if the adapter is operated in climates with high temperatures. Additionally, the input power pin to the power delivery controller must be connected to V_{out}. This was done with a bodge wire in Figure 5.23; however, a true fix would require a slight redesign of the PCB to route V_{out}, rather than EXTVcc, to the power delivery controller. This change allows the power delivery controller to properly sense the output voltage of the converter and ensure the converters output voltage is correct before connecting it to the load. Additionally, 100Ω resistors should be added to the data pins of the USB-C port. This would ensure that other USB-C devices interpret the system as a source only device. Beyond this, the circuit implements the intended functionality as is.

Some larger improvements, which were outside the scope of this project, would yield an improved system for DC power delivery over a USB-C Port. The power delivery controller features start-up default profiles which can be reconfigured via I2C after start-up. Thus, an on board microcontroller can be utilized to reconfigure the power delivery profiles on start-up, instead of manually reconfiguring the profiles each time the power delivery controller is powered. Other improvements include the addition of more ports for USB-C based power delivery. This would likely require a significant overhaul to the design as each port would require its own power delivery controller and DC-DC converter. Finally, this project needs some system level design to ensure the connectors, form factor, and mounting options meet the needs of the DC House Project's use case for this type of device. In all, there are many directions to explore with this type of device, and with the explosion of devices supporting USB-C charging this project will only become more relevant.

References

[1] "Database", Iea.org, 2018. [Online]. Available: https://www.iea.org/energyaccess/database. [Accessed: 29- Sep- 2018].

Description: Statistics related to the energy access across the world. Specifically, it enumerates the number of people still without basic electricity. This reality provides impotence for the DC House Project and related projects.

[2] J. Hruska, "USB-C vs. USB 3.1: What's the difference?," ExtremeTech, 04-Jun-2015. [Online]. Available: https://www.extremetech.com/computing/197145-reversible-usb-type-c-finally-on-its-way-alongside-usb-3-1s-10gbit-performance. [Accessed: 20-Oct-2018].

Description: This source provides information about the upgrades the USB-C connector provides over USB3.1. In particular, this source was used for the physical and power delleivery related attributes of USB-C to justify its use in this project.

[3] "USB Power Delivery and Type-C," www.st.com. [Online]. Available: https://www.st.com /content/ccc/resource/sales_and_marketing/presentation/product_presentation/group0/5a /b1/8e/6c/2b/0d/46/3c/Apec/files/APEC_2016_USB_Power.pdf/_jcr_content/translations /en.APEC_2016_USB_Power.pdf. [Accessed: 18-Oct-2018].

Description: This source provides information about the different power delivery profiles associated with USB-C. Additionally, it suggests some basic circuit topologies for meeting those power delivery profiles. Additionally, it provides a detailed pinout for USB-C connectors with descriptions.

[4] "California Renewable Energy Overview and Programs", California Energy Commission, 2018. [Online]. Available: https://www.energy.ca.gov/renewables/. [Accessed: 20- Oct- 2018].

Description: This source provides an overview of California's renewable energy programs and initiatives. The sources is particularly useful in showcasing how the world is shifting towards renewable energy. It shows that there is a market and promising future for renewable energy power systems, to further support the DC House Project's choice of energy source.

[5] D. Kithany and N. Akhtar, "USB Type-C Report - 2018 - IHS Technology," 30-Nov-2017. [Online]. Available: https://technology.ihs.com/596230/usb-type-c-report-2018. [Accessed: 29-Sep-2018].

Description: A speculative study on the market share and role of the USB-C connector in consumer electronics in the next five years. This source helps make the case the USB-C is a good choice of connector for a standard DC adapter due to its likely future ubiquity.

[6] H. Reydarns, V. Lauwereys, D. Haeseldonckx, P. van Willigenburg, J. Woudstra and S. De Jonge, "The development of a proof of concept for a smart DC/DC power plug based on USB power delivery," Twenty-Second Domestic Use of Energy, Cape Town, 2014, pp. 1-4. doi: 10.1109/DUE.2014.6827761

Description: This source outlines design of a DC-DC converter and emulated power delivery controllers for USB-C based power distribution. It is primarily used to outline the importance and necessity of communication between the source and load in a DC based grid system in order to negotiate power transfer between the source and loads with various requirements.

[7] D. Rambim, S. Ogara, S. Liyala and F. Awuor, "Towards an integrated framework for rural development in Kenya," 2016 IST-Africa Week Conference, Durban, 2016, pp. 1-8. doi: 10.1109/ISTAFRICA.2016.7530641

Description: This source presents a study of Information and Communications Technology (ICT) initiatives for rural development. The study focuses on rural development in Kenya, however, the same ideas apply to development of rural communities elsewhere, and the information learned from the study is applicable for different communities as well.

[8] M. Fedkin, "11.5. Efficiency of Inverters — EME 812: Utility Solar Power and Concentration", E-education.psu.edu. [Online]. Available: https://www.e-education.psu.edu /eme812/node/738. [Accessed: 20- Oct- 2018].

Description: This source provides information on the efficiency of inverters. This source is relevant since efficiency is one of core customer needs as well a major selling point for the USB-C adapter design being proposed.

[9] D. Shukla, "Design: How to Improve Power Conversion Efficiency of Inverters", Electronics For You, 2018. [Online]. Available: https://electronicsforu.com/electronics-projects/electronics-design-guides/power-conversion-efficiency-inverters. [Accessed: 20- Oct- 2018].

Description: This source provides information on the efficiency of inverters. The source specifically talks about ways to improve the efficiency of inverters, but in the process, mentions some inefficiencies. The source is used when talking about the inefficiency of sinewave inverters, which are a common inverter for household electronics.

[10]S. E. Liu et al., "Type-C interface reliability concern of electrical overstress and design for mitigation," 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, 2017,pp. 3A-5.1-3A-5.4.doi: 10.1109/IRPS.2017.7936280

Description: This source outlines the electrical reliability concerns that arise from physical characteristics of the USB-C interface. This will be used primarily to discuss the necessity and type of electrical protection needed to safe USB-C based power delivery.

[11] D. Lant and C. Zhang, "12 Volt Wall Outlet for The DC House Project", California Polytechnic State University San Luis Obispo, 2012.

Description: The source outlines a senior project completed in 2012 at California Polytechnic State University San Luis Obispo. The projects documents the design of 48V to 12V DC-DC converting using a standard AC wall plug as its interface to potential loads. This is used as a comparison to the feature set outlined in this project.

[12] A. Hefner and A. Magdaleno, "Cell Phone Charger for the DC House Project", California Polytechnic State University San Luis Obispo, 2012.

Description: The source outlines a senior project completed in 2012 at California Polytechnic State University San Luis Obispo. The projects documents the design of cell phone charger for the DC House Project at Cal Poly. The source is used when considering previous works related to the USB-C power adapter designed in this project.

[13] USB Implementers Forum, "Universal Serial Bus Power Delivery Specification,", pp. 556 Jan. 2010 [Revised June. 2018].

Description: This is the USB power delivery standard as given by the USB Inplementers Forum. This is used to form the requirements our system must meet to power USB-C based consumer electronic devices.

[14] Renesas, "Silicon N Channel Power MOS FET Power Switching," RJK0651DPB datasheet, Jan. 2013 [Revised Apr. 2013].

Description: This is the datasheet for the N channel FETs used in the buck converter. This datasheet assists in justifying the selection and application of this FET in our system.

[15] ON Semiconductor, "Surface Mount Schottky Power Rectifier," SS26T3G datasheet, Sept. 2013 [Revised June 2017].

Description: This is the datasheet for the Schottky diode used in the buck converter. This datasheet assists in justifying the selection and application of this diode in our system.

[16] Texas Instruments, "Benefits of a multiphase buck converter," pp. 1-3, Jan. 2012 [Revised Jan. 2012].

Description: This application note discusses the improvement, and calculation, of input and output ripple current using multiphase buck converters. This source is used to assist in justifying the use of a multiphase buck topology and calculation of input and output ripple current.

[17] Analog Devices, "60V Low IQ, Dual, 2-Phase Synchronous Step-Down DC/DC Controller," LTC3892 datasheet, Dec. 2015 [Revised July. 2017].

Description: This is the datasheet for the dual phase buck controller used in the buck converter. This datasheet assists in justifying the selection and application of this controller in our system. Additionally, it provides many resources for the design of various components associated with the controller.

[18] STMicroelectronics, "Autonomous USB PD controller with integrated discharge path," STUSB4710R datasheet, Apr. 2017 [Revised Nov. 2017].

Description: This is the datasheet for the USB-C power delivery controller used in the system. This datasheet assists in justifying the selection and application of this controller in our system. Additionally, it provides many resources for the design of various components which interface this power delivery controller with the buck controller.

[19] Analog Devices, "250mA, 4V to 80V Low Dropout Micropower Linear Regulator," LT3012 datasheet, Jan. 2005.

Description: This is the datasheet for the low drop-out regulator used in the system. This datasheet assists in justifying the selection and application of this controller in our system.

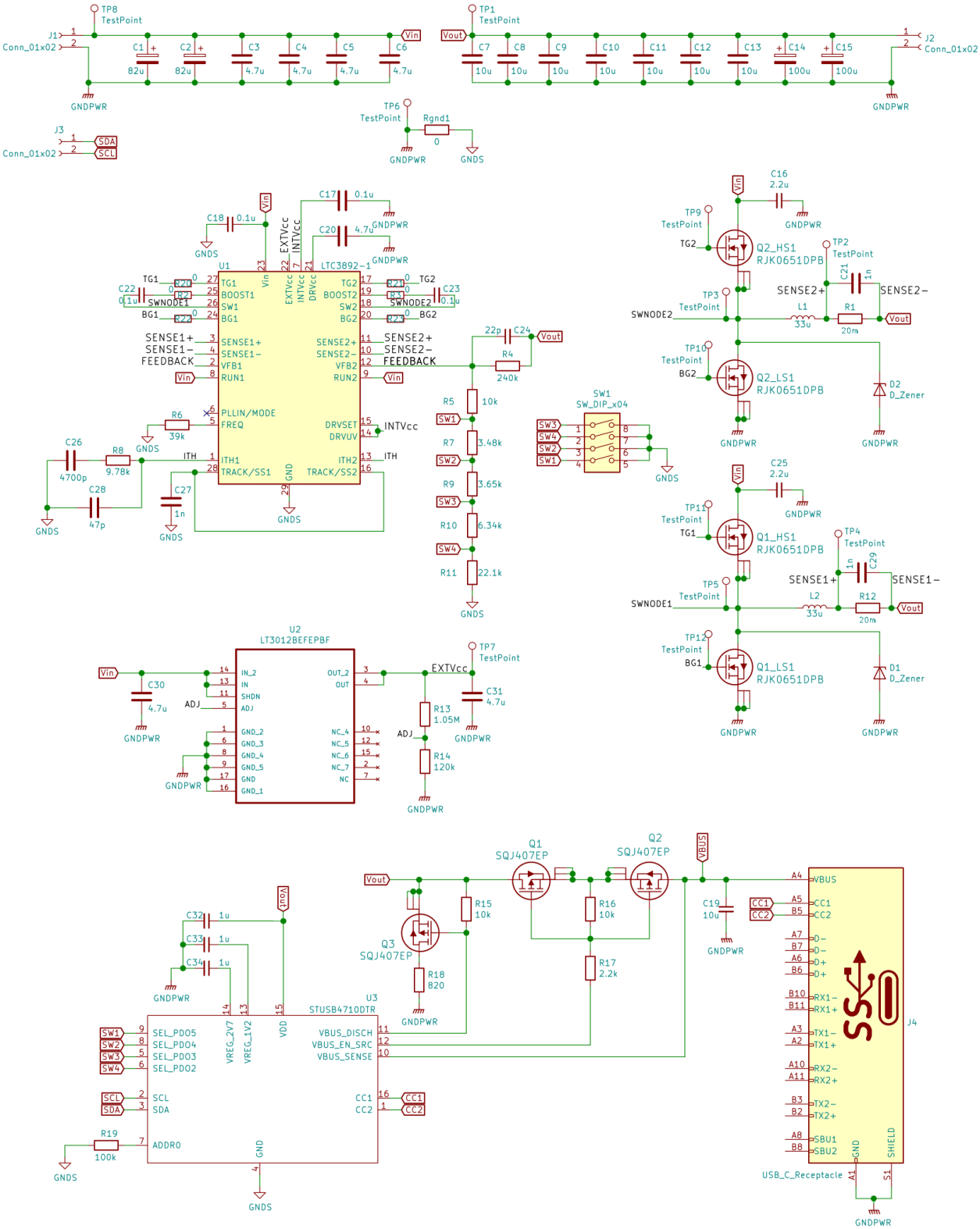
[20] Vishay, "Automotive P-Channel 30 V (D-S) 175 °C MOSFET," SQJ407EP datasheet, Jan. 2017 [Revised Feb. 2017].

Description: This is the datasheet for the P channel FETs used in the system. This datasheet assists in justifying the selection and application of this FET in our system.

[21] Analog Devices Inc, "PCB Layout Considerations for Non-Isolated Switching Power Supplies," June 2012.

Description: This application note discusses the layout of Buck converters. This application note assists us make informed design decisions when laying out the PCB for our system. Additionally, it identifies circuit nodes which need attention when routing.

A Final Schematic



B I2C code for Power Delivery Profile Configuration

main.c

```
/* Engineer(s): Ezzeddeen Gazali and Tyler Starr
 * Create Date: 5/14/2019
 * Description: Program that configures the STUSB4710R Power Delivery Controller
 *              through I2C communication using the MSP432 MCU.
 */
#include "msp.h"
#include "i2c.h"

int main(void)
{
    //Set DCO clock frequency and select as source for SMCLK
    CS -> KEY = CS_KEY_VAL;                     //enable writing to clock systems
    CS -> CTL0 = 0;                             //clear control register 0
    CS -> CTL0 |= CS_CTL0_DCORSEL_3;            //DCO frequency set to 12 MHz
    CS -> CTL1 |= CS_CTL1_SELS__DCOCLK;         //Set DCO as the source for SMCLK
    CS -> KEY = 0;                              //disable writing to clock systems

    WDT_A->CTL = WDT_A_CTL_PW | WDT_A_CTL_HOLD; // Stop watchdog timer
    __enable_irq();                             // Enable global interrupt

    Init_I2C(0x28);                             //Initialize I2C communication
    Write_I2C(0x81, 0xF4);                      //Set the advertised current
    Write_I2C(0x82, 0x41);                      //for 20V profile to 5A
    __delay_cycles(15000);
    while(1);
}
```

i2c.h

```
/* Engineer(s): Ezzeddeen Gazali and Tyler Starr
 * Create Date: 05/14/2019
 * Description: This library file implements useful functions for configuring the STUSB4710R PD Controller.
 *              The functions are documented prior to their source code.
 * Pin Assignments: P6.6 -> I2C -> SDA
 *                  P6.7 -> I2C -> SCL
 */
#include "msp.h"
//Device Identifier values
#define STUSB_ADDRESS_W       0x29  //standard 7-bit I2C slave address (with write bit)
#define STUSB_ADDRESS_R       0x28  //standard 7-bit I2C slave address (with read bit)

//number of cycles to delay for 1ms, 12MHz SMCLK
#define CYCLES                  12000

//bit definitions, I2 SDA -> P6.6 and SCL P6.7
#define SDA                     BIT6
#define SCL                     BIT7

//function prototypes
void Init_I2C(uint8_t Device_Address);
void Write_I2C(uint8_t MemAddress, uint8_t MemByte);
uint8_t Read_I2C(uint8_t MemAddress);
```

i2c.c

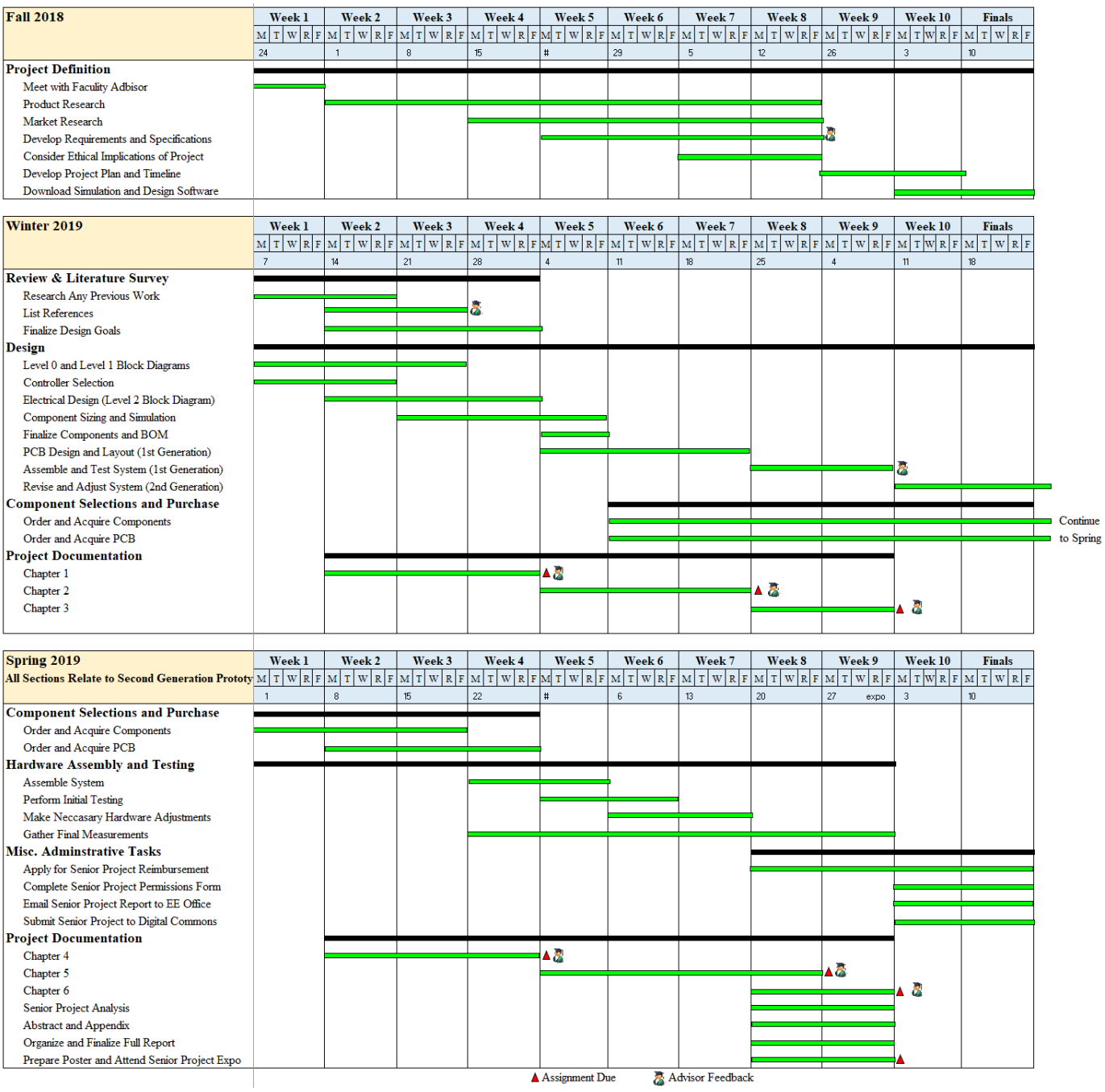
```
/*
 * Engineer(s): Ezzeddeen Gazali and Tyler Starr
 * Create Date: 05/14/2019
 */
#include "i2c.h"

//global variable definitions
uint16_t TransmitFlag = 0;
uint32_t REG1_CONTROL_WORD = 0;

/*
 * Function that initializes the I2C bus for communicating with MPL3115A2
 * INPUTS       uint8_t Device_Address = address of the MPL3115A2
 * RETURN       NONE
 */
void Init_I2C(uint8_t Device_Address)
{
    P6->SEL1 |= (SDA | SCL);                    // Set I2C pins of eUSCI_B3
    NVIC->ISER[0] = 1 << ((EUSCIB3_IRQn) & 31); // Enable eUSCIB3 interrupt in NVIC module

    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_SWRST;     // Software reset enabled
    EUSCI_B3->CTLW0 = EUSCI_B_CTLW0_SWRST   |   // Remain eUSCI in reset mode
                      EUSCI_B_CTLW0_MODE_3  |   // I2C mode
                      EUSCI_B_CTLW0_MST     |   // Master mode
                      EUSCI_B_CTLW0_SYNC    |   // Sync mode
                      EUSCI_B_CTLW0_SSEL__SMCLK;// SMCLK

    EUSCI_B3->BRW = 500;                        // baud rate = SMCLK / 500 = 24kHz
    EUSCI_B3->I2CSA = Device_Address;           // Slave address
    EUSCI_B3->CTLW0 &= ~EUSCI_B_CTLW0_SWRST;    // Release eUSCI from reset

    EUSCI_B3->IE |= EUSCI_A_IE_RXIE |           // Enable receive interrupt
                    EUSCI_A_IE_TXIE;
    return;
}
```

```
/*
 * Function that writes a single byte to the STUSB4710R.
 * INPUTS       uint8_t MemAddress = 1 byte STUSB4710R address to write to
 *              uint8_t MemByte = 1 byte value that is written in the specified address
 * RETURN       NONE
 *
 * Procedure :
 *     start
 *     transmit address+W (control+0)     -> ACK (from STUSB4710R)
 *     transmit data      (address)       -> ACK (from STUSB4710R)
 *     transmit data      (data)          -> ACK (from STUSB4710R)
 *     stop
 */
void Write_I2C(uint8_t MemAddress, uint8_t MemByte)
{
    uint8_t Address;
    Address = MemAddress;

    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TR;    // Set transmit mode (write)
    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TXSTT; // I2C start condition

    while (!TransmitFlag);                  // Wait for  address to transmit
    TransmitFlag = 0;

    EUSCI_B3 -> TXBUF = Address;            // Send the high byte of the memory address

    while (!TransmitFlag);                  // Wait for the transmit to complete
    TransmitFlag = 0;

    EUSCI_B3 -> TXBUF = MemByte;            // Send the byte to write to STUSB4710R

    while (!TransmitFlag);                  // Wait for the transmit to complete
    TransmitFlag = 0;

    EUSCI_B3 -> CTLW0 |= EUSCI_B_CTLW0_TXSTP;   // I2C stop condition

    return;
}
```

```
/*
 * Function that reads a single byte from the STUSB4710R.
 * INPUTS       uint8_t MemAddress = 1 byte STUSB4710R address to read from
 * RETURN       uint8_t ReceiveByte = 1 byte value that is received from the STUSB4710R
 *
 * Procedure :
 *     start
 *     transmit address+W (control+0)     -> ACK (from STUSB4710R)
 *     transmit data      (address)       -> ACK (from STUSB4710R)
 *     start
 *     transmit address+R (control+1)     -> ACK (from STUSB4710R)
 *     transmit data      (data)          -> ACK (from STUSB4710R)
 *     stop
 */
uint8_t Read_I2C(uint8_t MemAddress)
{
    uint8_t ReceiveByte;
    uint8_t Address = MemAddress;

    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TR;        // Set transmit mode (write)
    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TXSTT;     // I2C start condition

    while (!TransmitFlag);                      // Wait for address to transmit
    TransmitFlag = 0;

    EUSCI_B3 -> TXBUF = Address;                // Send the high byte of the memory address

    while (!TransmitFlag);                      // Wait for the transmit to complete
    TransmitFlag = 0;

    EUSCI_B3->CTLW0 &= ~EUSCI_B_CTLW0_TR;       // Set receive mode (read)
    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TXSTT;     // I2C start condition (restart)

    while ((EUSCI_B3->CTLW0 & EUSCI_B_CTLW0_TXSTT)); // Wait for start to be transmitted

    EUSCI_B3->CTLW0 |= EUSCI_B_CTLW0_TXSTP;          // set stop bit to trigger after first byte

    while (!TransmitFlag);                        // Wait to receive a byte
    TransmitFlag = 0;

    ReceiveByte = EUSCI_B3->RXBUF;                // Read byte from the buffer
    return ReceiveByte;
}
```

```
//I2C Interrupt Service Routine, sets a transmit flag when transmit or receive is complete
void EUSCIB3_IRQHandler(void)
{
    if (EUSCI_B3->IFG & EUSCI_B_IFG_TXIFG0)     // Check if transmit complete
    {
        EUSCI_B3->IFG &= ~ EUSCI_B_IFG_TXIFG0;  // Clear interrupt flag
        TransmitFlag = 1;                       // Set global flag
    }

    if (EUSCI_B3->IFG & EUSCI_B_IFG_RXIFG0)     // Check if receive complete
    {
        EUSCI_B3->IFG &= ~ EUSCI_B_IFG_RXIFG0;  // Clear interrupt flag
        TransmitFlag = 1;                       // Set global flag
    }
}
```

C Project Schedule



D Bill of Materials

Identifier(s)	Quan.	Description	Part Number	Supplier	Unit Price	Extended Price
R1, R12	2	RES 0.012 OHM 1% 1/2W 0805	408-1545-1-ND	Digikey	$0.58	$1.16
R8	1	RES SMD 9.76K OHM 1% 1/8W 0805	541-9.76KCCT-ND	Digikey	$0.10	$0.10
R6	1	RES SMD 39K OHM 0.5% 1/10W 0805	RR12P39.0KDCT-ND	Digikey	$0.11	$0.11
R4	1	RES SMD 240K OHM 0.5% 1/10W 0805	RR12P240KDCT-ND	Digikey	$0.11	$0.11
R5, R15, R16	3	RES SMD 10K OHM 0.5% 1/10W 0805	RR12P10.0KDCT-ND	Digikey	$0.11	$0.33
R9	1	RES SMD 3.65KOHM 0.5% 1/10W 0805	RR12P3.65KDCT-ND	Digikey	$0.11	$0.11
R11	1	RES SMD 22.1K OHM 0.1% 1/8W 0805	P22.1KDACT-ND	Digikey	$0.36	$0.36
R13	1	RES SMD 1.05M OHM 1% 1/8W 0805	P1.05MCCT-ND	Digikey	$0.10	$0.10
R14	1	RES SMD 120K OHM 1% 1/8W 0805	P120KCCT-ND	Digikey	$0.10	$0.10
R10	1	RES 6.34K OHM 1% 1/8W 0805	RMCF0805FT6K34CT-ND	Digikey	$0.10	$0.10
R7	1	RES SMD 3.48K OHM 1% 1/8W 0805	311-3.48KCRCT-ND	Digikey	$0.10	$0.10
R2, R3, R20, R21, R22, R23, Rgnd1	7	RES 0 OHM JUMPER 1/8W 0805	RMCF0805ZT0R00CT-ND	Digikey	$0.10	$0.70
R17	1	RES SMD 2.2K OHM 1% 1/8W 0805	1276-5290-1-ND	Digikey	$0.10	$0.10
R19	1	RES SMD 100K OHM 1% 1/8W 0805	1276-3512-1-ND	Digikey	$0.10	$0.10
R18	1	RES SMD 820 OHM 1% 1/8W 0805	311-820CRCT-ND	Digikey	$0.10	$0.10
C1, C2	2	CAP ALUM POLY 82UF 20% 63V SMD	565-4791-1-ND	Digikey	$1.28	$2.56
C7,C8,C9,C10,C11,C12,C13,C19	8	CAP CER 10UF 50V X5R 1206	490-12457-1-ND	Digikey	$0.55	$4.40
C3,C4,C5,C6,C30	5	CAP CERAMIC 4.7UF 100V X7S 10% P	490-17693-1-ND	Digikey	$0.86	$4.29
C18	1	CAP CER 0.1UF 100V X7R 1206	732-12245-1-ND	Digikey	$0.14	$0.14
C16,C25	2	CAP CER 2.2UF 100V X7S 1206	445-6994-1-ND	Digikey	$0.75	$1.50
C17,C22,C23	3	CAP CER 0.1UF 50V Y5V 0805	311-1361-1-ND	Digikey	$0.13	$0.39
C14,C15	2	CAP ALUM POLY 100UF 20% 35V SMD	P121401CT-ND	Digikey	$1.75	$3.50
C21,C27,C29	3	CAP CER 1000PF 50V C0G/NP0 0805	478-1328-1-ND	Digikey	$0.20	$0.60
C24	1	CAP CER 22PF 50V C0G/NPO 0805	311-1103-1-ND	Digikey	$0.14	$0.14
C26	1	CAP CER 4700PF 50V X7R 0805	478-3545-1-ND	Digikey	$0.38	$0.38
C28	1	CAP CER 47PF 50V C0G/NP0 0805	478-1312-6-ND	Digikey	$0.15	$0.15
C20,C31	2	CAP CER 4.7UF 25V X7R 1206	1276-3178-1-ND	Digikey	$0.26	$0.52
C32,C33,C34	3	CAP CER 1UF 25V X7R 1206	732-7700-1-ND	Digikey	$0.18	$0.54
L1, L2	2	FIXED IND 33UH 8.5A 21.7 MOHM	732-2178-1-ND	Digikey	$5.63	$11.26
D1,D2	2	DIODE SCHOTTKY 60V 2A SMB	SS26T3GOSCT-ND	Digikey	$0.44	$0.88
Q1_HS1, Q2_HS1, Q2_LS1, Q2_LS1	4	MOSFET N-CH 60V 25A LFPAK	RJK0651DPB-00#J5CT-ND	Digikey	$1.37	$5.48
Q1, Q2, Q3	3	MOSFET P-CH 30V 60A	SQJ407EP-T1_GE3CT-ND	Digikey	$1.60	$4.80
U1	1	IC REG CTRLR BUCK 28TSSOP	LTC3892EFE-1#PBF-ND	Digikey	$10.51	$10.51
U2	1	IC REG LIN POS ADJ 250MA 16TSSOP	LT3012BEFE#PBF-ND	Digikey	$4.51	$4.51
U3	1	STAND-ALONE USB PD CONTROLLER	97-18020-1-ND	Digikey	$1.95	$1.95
J1, J2	2	BANANA JACK THREADED RED	BKCT2230-2-ND	Digikey	$0.75	$1.50
J1, J2	2	BANANA JACK THREADED BLACK	BKCT2230-0-ND	Digikey	$0.75	$1.50
J3	1	CONN HEADER VERT 2POS 2.54MM	S1012EC-02-ND	Digikey	$0.06	$0.06
J4	1	CONN RCP USB3.1 TYPEC 24P SMD RA	12401610E4#2ACT-ND	Digikey	$2.24	$2.24
SW1	1	SWITCH SLIDE DIP SPST 25MA 24V	732-6963-1-ND	Digikey	$2.30	$2.30
TP1-10	4	PC TEST POINT MULTIPURPOSE WHITE	36-5012-ND	Digikey	$0.35	$1.40
-	1	Designed Four Layer PCB for System	-	Oshpark	$95.90	$95.90
Total(s)		**Component Count**				84
		Cost				$167.08

E Analysis of Senior Project

Project Title: USB-C Power Adapter for DC House Project
Students: Tyler Starr, Ezzeddeen Gazali
Advisor: Dr. Taufik

1. Summary of Functional Requirements
   The USB-C power adapter designed in this project will charge electronic devices at standard USB-C Power Delivery voltages. The adapter operates from a 48 VDC input source and supplies electronic devices with 5, 9, 12, 15,or 20 VDC at more than 40 W. The exact voltage exact voltage level supplied will depend on the requirements of the load.

2. Primary Constraints
   The primary constraints for this project is that the adapter must charge electronic devices at standard USB-C power delivery voltages. Additionally, the components used must come in packages that can be easily soldered. However, most power delivery controllers come in QFN packages which complicates the power adapter assembly process and limits the options we can choose from.

3. Economic Impact

   (a) Human Capital The development of this product will create jobs in the engineering, manufacturing, and sales sectors. Although most of the components are bought from U.S. based companies, many of those companies manufacture there products in other countries which will benefit those countries as well. Additionally, the products will be shipped to consumers in various locations which will contribute to more jobs as well.

   (b) Financial Capital The goal of this product is to design an adapter that is charges USB-C devices more efficiently. Increasing the efficiency provides cheaper method of charging household electronics from renewable energy sources. Additionally, this product will benefit small businesses and companies that operate in the renewable energy industry by providing them with more business.

   (c) Natural Capital
   The USB-C adapter will utilize IC's and circuit components that come from natural resources. Semiconductors require large amounts of water during the fabrication and contribute to air and water pollution in some countries.

4. If manufactured on a commercial basis:

   (a) Estimated number of devices sold per year: 2000

   (b) Estimated manufacturing costs: $85 (factors in cost of manufacture and transport)

   (c) Estimated purchase price for each device: $150

   (d) Estimated yearly profit: $130,000

   (e) Estimated costs for user to operate: Users of this product utilize renewable energy thus the costs is in the degradation of the devices used to power this product. Assuming a user has a $10,000 solar setup that lasts 25 years and utilizes the power adapter 24 hours a day, the cost comes to 4.6 cents per hour (however the solar setup wouldn't only be used for this adapter)

5. Environmental

   As mentioned previously, the USB-C power adapter will contain some IC's and other circuit components that are produced from natural resources. Manufacturing an integrated circuit on a 300-mm wafer requires approximately 2,200 gallons of water. Despite water's abundance, excessive water use eventually harms the ecosystem and natural resources, and more specifically threatens the livelihood of animals and fish that depend on those water sources.

   Despite the negative impacts on the environment, the USB-C adapter will provide more incentive for consumers to use renewable energy power systems. Replacing non-renewable energy sources, such as coal, with renewable energy will benefit the environment and counter some of the negative effects.

6. Manufacturability

   The primary issue with manufacturing for this project is the requirement that the final design will be hand assembled. Thus, we can't use many of the smaller circuit packages like QFN due to the difficulty of soldering. Many modern controllers for USB-C power delivery and buck conversion utilize the QFN package. As such, our choice of controllers is severely limited by our manufacturing process.

7. Sustainability

   The USB-C adapter will supply electronic devices with more than 40W and the possibility of going up to 100W. Some of the anticipated challenges is ensuring a long product lifetime since the device components will be subjected to large amounts of power. A long product lifetime is the first step in ensuring a sustainable and well balanced environment. Additional steps such as using RoHS compliant components and educating consumers on proper methods for recycling the device could further contribute to this effort.

   A possible upgrade that can improve the reliability of the device and possibly extend its lifetime is using a synchronous multi-phase buck converter for the DC-DC conversion instead of a typical buck converter. This will reduce the likelihood that one single component fails and improve the efficiency of the converter. Thus, contributing to an improved design and more sustainable product. However, using the mulit-phase buck converter adds complexity to the design of the system and introduces more components. The addition of more components could defeat the cause if these components are manufactured in was non-environmentally friendly manner.

8. Ethical Considerations

   Low costs is important for the target audience of this project. However, performance must be maintained such that the device is safe to operate and doesn't damage attached systems. Additionally, we must consider the impact of the manufacturing process, operation, and disposal has on the environment. Lastly, we must consider the safety of consumers by implementing sufficient protection circuitry to protect against accidental damage to consumer devices or injury to the consumers themselves.

9. Health and Safety

   The manufacture of electrical devices poses many health and safety risks to those who work in the industry and the associated communities. Mishandling of waste associated with the manufacture process pose a severe risks in many places. Additionally, our project deals in relatively high voltage and power. As such, there is risk of shock or burns to consumers due to the nature of the devices. Finally, electronic devices contain many heavy metals which can threaten the health and safety of consumers when the devices are disposed of in landfills.

10. Social and Political

    (a) Social Issues: Since this project may be utilized by previously un-powered communities some issues can arise. Most would agree that electrical power represents an unmitigated increase in standard of living. However, some contend that the consequent ceasing of traditional activities like hunting damage the culture of these communities. As such, we should always ensure the communities utilizing our products have autonomy in their choice to use it.

    (b) Project Impact: The primary impacts include making existing and future off grid power systems more convenient by providing an easy and standard power adapter for consumer devices. This represents an increase in the standard of living for people relying on these off grid systems. Additionally, the project potentially makes renewable off grid systems more attractive contributing to the adoption of renewable energy.

11. Development

    This project requires power electronics beyond that learned in classes so far. These include additional circuit topologies and design considerations especially considering the type and operation of the controller used in these converters. Additionally, knowledge and operation of PCB design software independently pursued to produce a PCB for this project. Perhaps most significantly an understanding of the USB-C power delivery standard was independently researched to ensure our system can interface with any other device which follows the standard. Finally, aspects of project management and design process is and will be explored beyond what has been done in the classroom to ensure a punctual and effective solution to the problem we face.