Method for selecting coupling and by-pass capacitors in multi-stage linear circuits

Vladimir I. Prodanov, Dale S. Dolan

Department of Electrical Engineering, California Polytechnic State University, San Luis Obispo, CA, USA
E-mail: vprodano@calpoly.edu

Abstract: A method for selecting a set of coupling and by-pass capacitors is presented. The approach uses short-circuit time-constant analysis and for a given −3 dB cut-off frequency minimises the total capacitance used. This study offers a derivation of design formulas and shows their use via examples.

1 Introduction

The sum in (1) estimates the lower cut-off frequency of a multi-stage AC-coupled circuit. Here C_1 through C_n are the values of the coupling capacitors and r_{C1} through r_{Cn} are the resistances seen by each capacitor when all the other capacitors have infinite values [1–3]. The RC products are called short-circuit time-constants (SCTCs) [2–5]

$$\omega_{-3\,\mathrm{dB}} \quad \frac{1}{r_{C1}C_1}+\frac{1}{r_{C2}C_2}+\cdots+\frac{1}{r_{Cn}C_n} \tag{1}$$

The SCTC expression (1) has both analytic and design utility. Indeed, it allows us to select coupling and by-pass capacitors to meet a desired cut-off frequency [1–4]. The basic procedure, discussed elsewhere [2, 3], selects capacitors to satisfy (2) and obtains a particular solution by making one of the $1/RC$ terms dominant while giving equal and much lesser weight to the other terms. While assigning a dominant term is always possible, such assignment is not always meaningful. The next section clarifies this statement using examples

$$\frac{1}{r_{C1}C_1}+\frac{1}{r_{C2}C_2}+\cdots+\frac{1}{r_{Cn}C_n}=\omega_{-3\,\mathrm{dB}}^{\mathrm{spec}} \tag{2}$$

This paper describes an alternative design approach where the values of the coupling and the by-pass capacitors are computed without explicit use of a 'one-term dominance'. They are obtained by solving (2) and (3)

$$C_1\sqrt{r_{C1}}=C_2\sqrt{r_{C2}}=\cdots=C_n\sqrt{r_{Cn}} \tag{3}$$

Satisfying (3) is significant because it minimises the overall capacitance used as demonstrated in the last section of this paper.

2 Design formulas and examples

Despite the complexity of (2) and (3), their simultaneous solution is always possible. Indeed, using (2) and (3) we derive (4) and once one capacitor is known the others we decide using (5)

$$C_1=\frac{1}{r_{C1}\,\omega_{-3\,\mathrm{dB}}^{\mathrm{spec}}}\left(1+\sqrt{\frac{r_{C1}}{r_{C2}}}+\cdots+\sqrt{\frac{r_{C1}}{r_{Cn}}}\right) \tag{4}$$

$$C_j=C_1\sqrt{\frac{r_{C1}}{r_{Cj}}}\quad \text{for } j=2 \text{ to } n \tag{5}$$

2.1 Example #1

Consider the common-emitter amplifier circuit depicted in Fig. 1. The design goal is a corner frequency not exceeding 100 Hz set by the proper choice of C_1, C_2, and C_3. This problem is solved in [2] page 502 using the one-term dominance approach. The authors assign an 80% weight to the term related to the emitter node (capacitor C_2) and divide the leftover 20% between the other two capacitors. The procedure yields $C_1 = 2.1$ µF, $C_2 = 27.6$ µF, $C_3 = 1.2$ µF and a cut-off frequency of 89.8 Hz according to Spice. While successful, the solution seems contrived due to the arbitrarily assigned percentage values.

Next, we solve the design problem using (4) and (5). The starting point is the same: numeric values for the small-signal resistances seen by each capacitor. They are below listed:

$$r_{C1}=R_s+R_B||r_\pi \simeq 7.44\ \mathrm{k}\Omega$$

$$r_{C2}=r_e+\frac{R_B||R_s}{\beta+1}\simeq 72\ \Omega$$

$$r_{C3}=R_c+R_L=13\ \mathrm{k}\Omega$$

Then, according to (4), the base coupling capacitor must be 2.55 µF.

$$C_1=\frac{1}{7440\,(2\pi 100)}\left(1+\sqrt{\frac{7440}{72}}+\sqrt{\frac{7440}{13000}}\right)=2.55\ \mu\mathrm{F}$$

For the values of the other capacitors, C_2 and C_3, we have 25.9 and 1.93 µF

$$C_2=2.55\ \mu\mathrm{F}\times\sqrt{\frac{7440}{72}}=25.9\ \mu\mathrm{F}$$

$$C_3=2.55\ \mu\mathrm{F}\times\sqrt{\frac{7440}{13000}}=1.93\ \mu\mathrm{F}$$

In practice, all values are rounded up the next standard one. Assuming 10% tolerance rating those would be 2.7, 27, and 2.2 µF.

We remark that minimising of the overall capacitance gives greater weight to the low impedance nodes. Indeed, here the $1/C_2 r_{C2}$ term evaluates to 536 rad/s and accounts for 85% of the specified 200π rad/s (100 Hz). This means that the proposed technique does not prevent term dominance but eliminates the need for guessing.

2.2 Example #2

The problem with the dominant term approach becomes clear when we try to set the corner frequency of the passive circuit in Fig. 2.

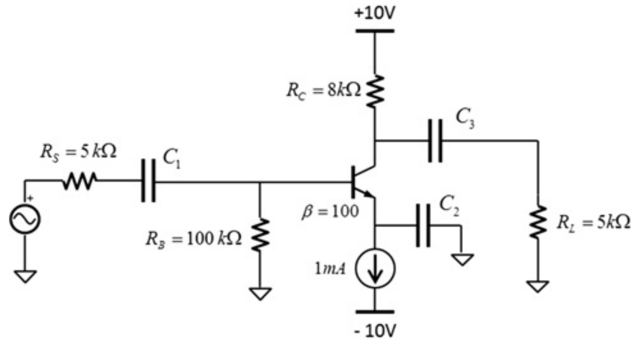

Fig. 1 *Schematic of a simplified common-emitter amplifier where C_1, C_2, and C_3 are selected to achieve a −3 dB cut-off not exceeding 100 Hz*

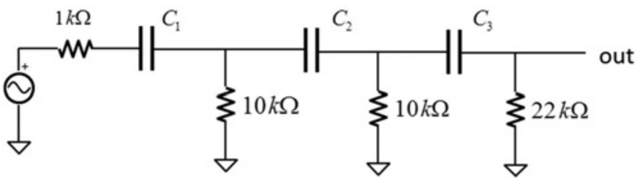

Fig. 2 *Three-stage passive high-pass filter where C_1, C_2, and C_3 are selected to achieve a −3 dB cut-off not exceeding 1 kHz*

The resistances experienced by each capacitor are below listed.

$$r_{C1} = 1\ \text{k}\Omega + 10\ \text{k}\Omega||10\ \text{k}\Omega||22\ \text{k}\Omega = 5.07\ \text{k}\Omega$$
$$r_{C2} = 1\ \text{k}\Omega||10\ \text{k}\Omega{+}10\ \text{k}\Omega||22\ \text{k}\Omega = 7.78\ \text{k}\Omega$$
$$r_{C3} = 1\ \text{k}\Omega||10\ \text{k}\Omega||10\ \text{k}\Omega + 22\ \text{k}\Omega = 22.83\ \text{k}\Omega$$

Since these resistances are comparable in value, we cannot justify enforcing a dominant term. The good news is the proposed strategy does not call for pre-assigned percentages. For the targeted cut-off of 1 kHz, with the aid of (4) and (5), we get

$$C_1 = \frac{1}{5070\ (2\pi 1000)}\left(1 + \sqrt{\frac{5070}{7780}} + \sqrt{\frac{5070}{22830}}\right) = 71.5\ \text{nF}$$
$$C_2 = 71.5\ \text{nF} \times \sqrt{\frac{5070}{22830}} = 57.7\ \text{nF}$$
$$C_3 = 71.5\ \text{nF} \times \sqrt{\frac{5070}{22830}} = 33.7\ \text{nF}$$

Similar to the earlier example one would need to choose standard values by rounding up the calculating values.

3 Specified versus actual −3 dB frequency

The proposed approach for determining coupling and by-pass capacitors is based on the premise that setting the sum in (1) to $\omega_{-3\ \text{dB}}^{\text{Spec}}$ produce $\omega_{-3\ \text{dB}}^{\text{actual}}$ with a similar value. At 92.4 and 796 Hz, according to SPICE, the actual cut-off frequencies for both designs are lower than the specified values of 100 Hz and 1 kHz.

$$\omega_{-3\ \text{dB}}^{\text{actual}} < \frac{1}{r_{C1}C_1} + \frac{1}{r_{C2}C_2} + \cdots + \frac{1}{r_{Cn}C_n} = \omega_{-3\ \text{dB}}^{\text{spec}} \qquad (6)$$

This finding concurs with the theory developed in [5] where the authors prove the sum in (1) is an upper-bound for the cut-off frequency. A strict inequality exists for systems with two or more coupling capacitors (see expression (27) in [5]). This property is desirable because it leads to conservative solutions with a 'built-in' design margin.

4 Origin of expression (3)

As stated in Section 1, (3) stems from minimising the total capacitance while meeting (2). So, the task is a classic constrained optimisation problem solved using the method of Lagrange multipliers; the details are presented next.

We start by defining three functions: $f(\boldsymbol{c})$, $g(\boldsymbol{c})$ and $F(\boldsymbol{c}, \lambda)$ as follows:

$$f(\boldsymbol{c}) = C_1 + C_2 + \cdots + C_n \qquad (7)$$

$$g(\boldsymbol{c}) = \frac{1}{r_{C1}C_1} + \frac{1}{r_{C2}C_2} + \cdots + \frac{1}{r_{Cn}C_n} - \omega_{-3\ \text{dB}}^{\text{spec}} \qquad (8)$$

$$F(\boldsymbol{c},\lambda) = f(\boldsymbol{c}) + \lambda g(\boldsymbol{c}) \qquad (9)$$

The function we want to optimise is $f(\boldsymbol{c})$ while $g(\boldsymbol{c})$ here accounts for the imposed constraint. According to theory, to find the vector ($\boldsymbol{c}$) that optimises $f(\boldsymbol{c})$ we must solve $n+1$ equations obtained by partial differentiation of F ($\boldsymbol{c}$, λ). The first n equations have the same structure captured as

$$\frac{\partial}{\partial C_j}F(\boldsymbol{c}, \lambda) = 1 - \lambda\frac{1}{r_{Cj}C_j^2} = 0 \quad \text{for all } j \qquad (10)$$

The above simplifies to (11) which is recognised as (3)

$$C_1\sqrt{r_{C1}} = C_2\sqrt{r_{C2}} = \cdots = C_2\sqrt{r_{C2}} = \sqrt{\lambda} \qquad (11)$$

Differentiating $F(\boldsymbol{c}, \lambda)$ with respect to λ and equating the result to 0 returns $g(\boldsymbol{c}) = 0$ which is recognised as the original constraint (2). This development proves the earlier assertion that simultaneous solution of (2) and (3) gives the desired optimum set of coupling and by-pass capacitor values.

5 Conclusion

This study benefits analogue circuits and systems designers by enhancing their ability to apply DC blocking and by-pass capacitors in the signal chain. The presented approach builds upon a classic design strategy involving the so-called short-circuit time-constants. This study shows that imposing the requirement for least total capacitance turns an under constrained design problem into one with a unique solution. The optimum capacitor values obey a very specific relation to one another and to their respective resistances. Namely, the products of capacitor value and the square-root of the corresponding resistance are fixed, same for all capacitors in the set. The derivation is straight forward and the design formulas quite simple as shown in the provided examples.

6 References

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