DESIGN AND ANALYSIS OF A NOVEL MULTILEVEL SINGLE PHASE INTERCONNECTED H-BRIDGE INVERTER

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ABSTRACT

Design and Analysis of a Novel Multilevel Single Phase Interconnected H-Bridge Inverter

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Inverters allow the use of residential solar power to run household appliances and electronics by converting DC to AC power just like the AC power from the grid. This study looks at the design and implementation of a novel multilevel inverter topology called a single phase interconnected H bridge inverter. By utilizing reduced switching complexity, the multilevel inverter can lower the cost of a typical inverter without sacrificing the power quality. The design is developed and analyzed through simulation and hardware testing to demonstrate a working model. Load testing is performed on the inverter output as well as analysis of a custom filter to optimize the output total harmonic distortion (THD). Results from measurements done in simulation and hardware demonstrate the functionality of the proposed inverter topology, providing quality outputs at no load condition. The thesis will also identify and offer solutions to the problems encountered during the construction and testing of the proposed inverter.

ACKNOWLEDGMENTS

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Chapter 1. Introduction

Renewable energy represents a hot topic in today's society encompassing many types of energy sources. From well established and known sources like solar, wind, and hydroelectric to biomass and tidal power in the experimental phase, all fall under the renewable umbrella. A key contributor for all this talk lies in the rise of global warming. More and more people in the world are accepting the scientific evidence for this phenomenon and have sprung into action to reduce its rise [1]. One facet along with energy efficiency is the expansion of renewable energy as an alternative to classical fossil fuel. Technology has improved over time in this field leading to the greater expansion. A key component of the renewable energy systems is the inverter. This is mainly due to the more prevalent use of residential and utility scale photovoltaic systems [2].

Solar energy has become more affordable and accessible over time [2]. Advancements in technology and manufacturing efficiency and yields increase adoption rate worldwide. In many cases, it is economically attractive to have solar power energy to save money over time to offset utility cost. Combined with government incentives, higher utilization demands improved power quality from the solar power to the grid. Solarcity is one of the solar panel providers who recently innovated in the form factor of the solar panels by integrating them in the shape of roof tiles [3]. This solution solves the aesthetic drawback of having solar panels on your roof. Although residential solar installations have grown steadily, innovated ideas like this will help increase the number of people buying solar. The large scale developments have seen a significant rise over the last few years. Solar farm projects have opened up in many areas of the country and the largest are in California. Solar Star, Topaz Solar Farm and Desert Sunlight Solar

Farm are the largest in the world after India's Kamuthi Solar Power Project that just completed [4].

Figure 1-1. Topaz solar farm [5].

These solar farms also include solar thermal sources that use parabolic concentrators. Solar thermal panel efficiency is 70-90% efficient and have added benefits of predictable power by storing excess energy in molten salt [6]. They generate energy by using mirrors to concentrate sunlight into a small area and then generating steam with the heat for a turbine. The first utility size project with this concept is in Nevada desert called Crescent Dunes [7]. Solar thermal can also be used for heating water and the home [8].

Figure 1-2. Crescent Dunes solar energy plant [7].

Another source of renewable energy is wind. 2015 was a record year for wind with a record global 63GW added. China led in new installations with nearly half of the global total [9]. Turbine manufacturers also broke installation records.

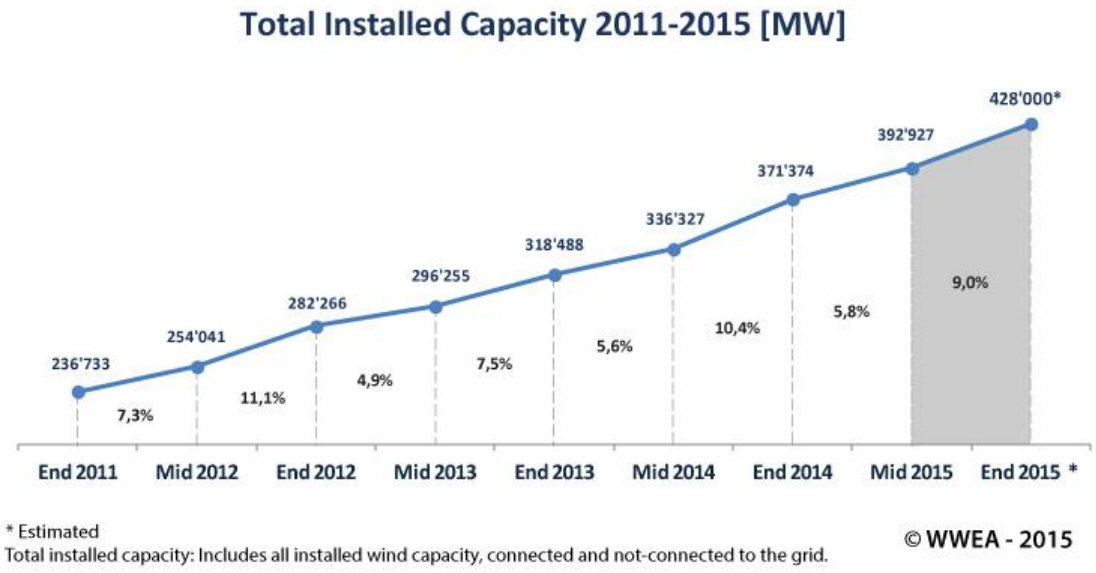


Figure 1-3. Worldwide wind capacity [10].

With the uncertainty of oil supplies in some regions, cost reduction of implementing wind, and lastly the need to reduce air pollution has all played a role in the growth of wind. For example, the global average cost for wind is $83 per megawatt-hour vs. $84 for coal and $98 for gas [11]. In China, energy independence and air pollutions were concerns that contributed to the government to invest in the wind market. Advancements in wind technology to build wind turbines taller and blades longer have contributed to lower cost while outputting more power [12].

Hydropower still remains the largest source of renewable energy in the world with 16% of electricity generation overall and 85% of the global renewable electricity [13]. To balance solar and wind energy generation, hydropower plays an important role in controlling the fluctuations that those sources bring [13]. In other words, hydropower fills the gap when other sources are unable to supply electricity to the grid.

As global warming becomes more accepted as a threat in the world, more countries have committed to the need to curtail greenhouse gases. In 2016, the Paris Agreement of the United Nations Framework Convention on Climate Change's 21st Conference of Parties committed 195 countries to limit global warming to below 2 degrees Celsius [14]. Commitments were made to increase renewable energy and energy efficiency based on each countries contribution to global warming. Take note that reduced power consumption or efficiency is a key component of tackling global warming. In the US, regulations on automobile fuel efficiency have improved emissions even though fossil fuels remain a significant fuel source. Especially as fossil fuel prices have declined it will remain a central part of people's lives. But on the bright side, even with the decline in prices, renewable energy has seen tremendous growth. Credit the uncertainty of fossil fuel prices over the years for the confidence in investing in renewable energy as well as the advances leading to more cost effective solutions.

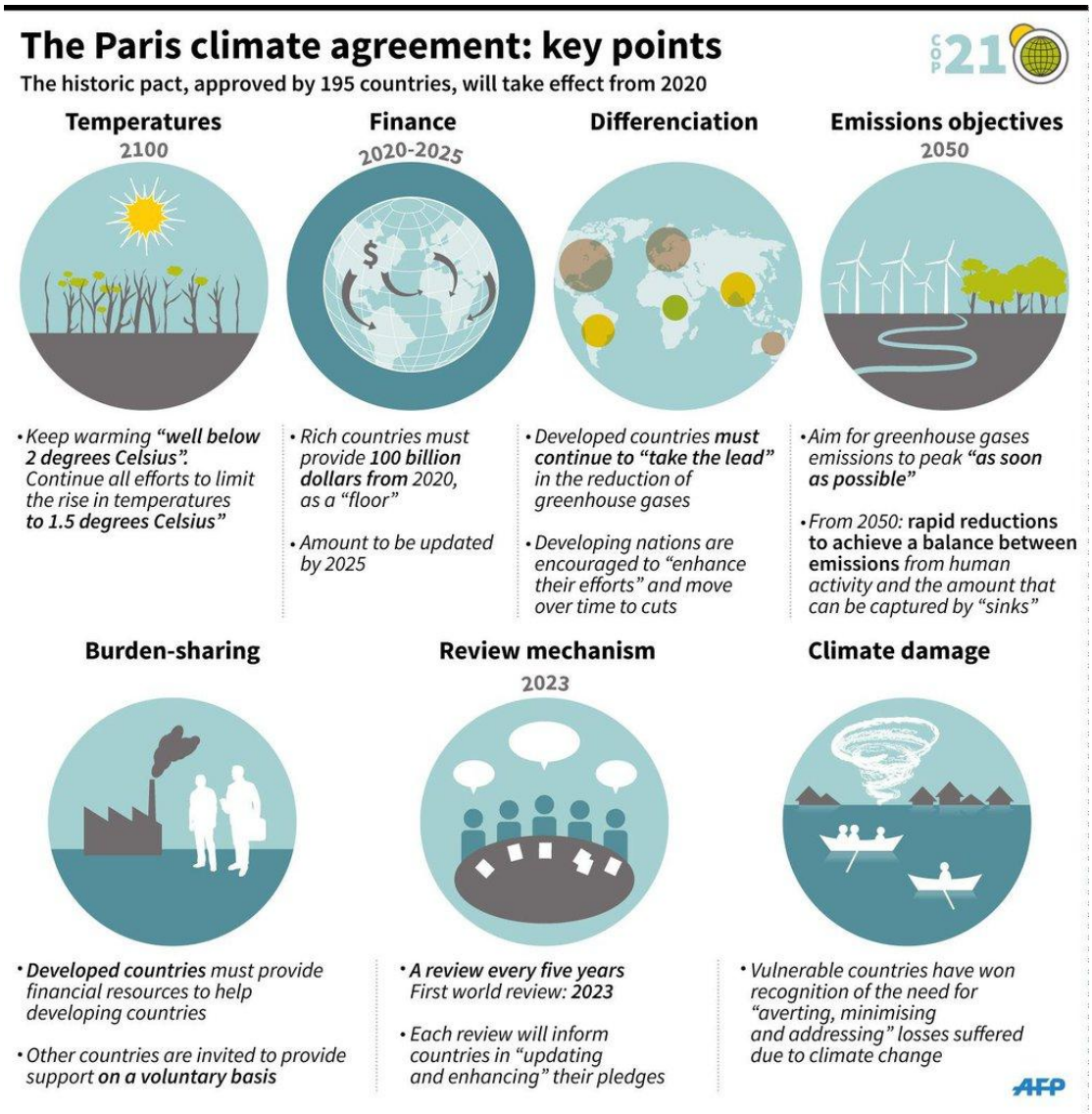


Figure 1-4. The Paris agreement infographic [15].

Renewable energy also plays an important role in self sufficiency in underdeveloped regions. Distributed energy generation plays a key role in energy access in rural areas. Locations not connected to the grid can use solar panels as a source of electricity. Even small panels can be used for lighting to replace more hazards kerosene lamps for example. Places like Uganda have 80% of the population living off the grid [16]. In fact, solar powered lighting is cheaper and also provides more lighting. Water pumping and heating are other benefits of off grid power that can be delivered to

rural areas [17]. This type of energy infrastructure can be built on rather than using a traditional centralized grid. It is easier to maintain and operate. Problems can be seen in China where the need to tie large scale wind farms to the grid and manage the excess power can lead to wasted generation or curtailment where available energy is not accepted due to other sources being more reliable or weak connections. Some of these wind turbines generate DC power. Generally, DC must be converted to AC for most things that run on electricity.

Figure 1-5. Electricity for rural homes [17].

Advancement in inverters, the tool that converts DC to AC, represents a part of the puzzle that has helped advance renewable energy. Improved efficiency and power quality help with integrating DC generated from renewable sources to the AC power that are needed in transmitting power to the grid. Better inverters also mean lower cost in circuitry by eliminating additional conversions. We can directly tie solar power to run motors for water pumps or heating. Our current electricity infrastructure involves sending AC power over miles of power lines to our homes. From there, many electronics in our home come with a rectifier to convert AC to DC for use. In order to be compatible with the existing electricity powered instruments, we must convert all DC sources to AC and

then have the individual tool convert back to DC. That is where in rural areas or isolated systems we need a way to convert DC generated from renewable sources like solar and wind to invert them to AC power. Although convoluted, the inverter remains a critical part of the equation.

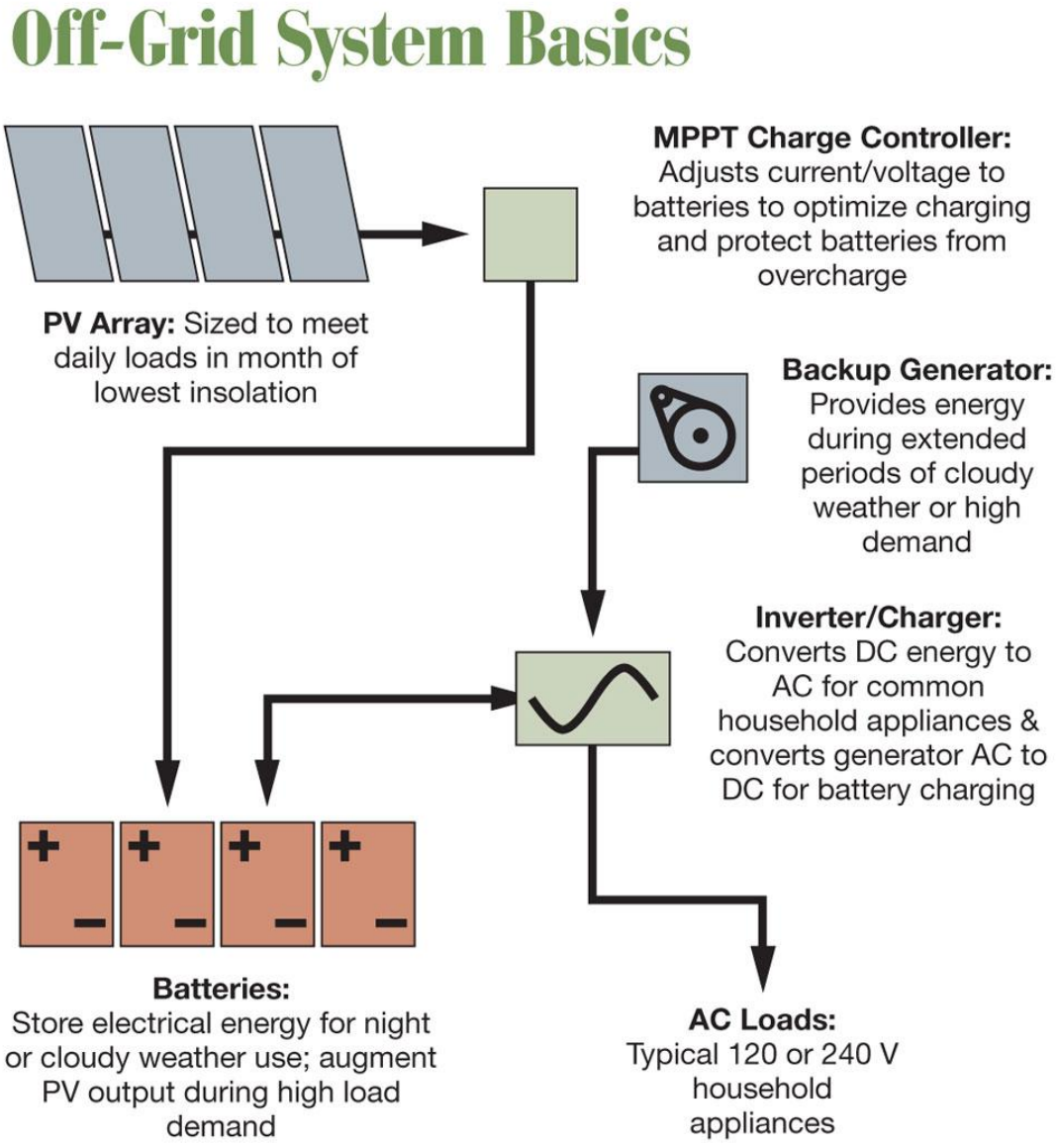


Figure 1-6. Inverters in off grid systems [18].

Chapter 2. Background

2.1. Inverter Theory

An inverter is an electric circuit that converts direct current [DC] power to alternating current [AC]. The input is either varying or non-varying and the output is of a specific voltage and frequency. Inverters are commonly used in fuels cells, solar panels, and wind turbines as well as uninterruptible power supplies and variable frequency drives. Individual inverter can be used to generate AC power from batteries for off grid loads.

To generate AC power, there are many different inverter circuit designs and output types. This can be done by switch mode inverters that have controlled switching sequences to convert DC to AC.

The two types of switch mode inverters topologies are voltage source inverter or current source inverter. Current source inverters (CSI) have input that acts like a current source (typically large inductor) and output that acts like an AC current source. This kind of inverter is used in high power AC motor drive applications. Voltage source inverters output AC voltage from a DC source. From there, inverters are categorized based on the switching method: square wave or Pulse Width Modulation [PWM].

The square wave inverter produces a square wave whose output RMS and frequency are based on the input voltage used and frequency of the switching controls. While easy to implement, the disadvantage lies in the shape of the output waveform having high harmonic content due to the not fully sinusoidal output. The significant presence of low frequency harmonics causes the square wave inverter to become complex and costly.

2.2. PWM Switching

The pulse width modulated inverter controls both the magnitude and frequency through its switching control circuitry. Specifically, a sinusoidal reference signal at fundamental frequency is compared with a triangular waveform at switching frequency to produce the PWM signals. This will improve harmonics by moving them to multiples of the switching frequency which will be much higher than the fundamental or desired frequency.

2.2.1. Bipolar Switching

Furthermore, PWM inverters have two different types based on the switching control method. Known as bipolar and unipolar switching, each output closely resembles the name given. First, the bipolar switching inverter switches between positive and negative input voltage. As a PWM switching scheme, the switches turn on and off based on the logic of the control signal and triangle signal. The output will take on either a +Vdc or –Vdc state. Figure 2-1 shows the unfiltered AC output of the Bipolar PWM inverter.

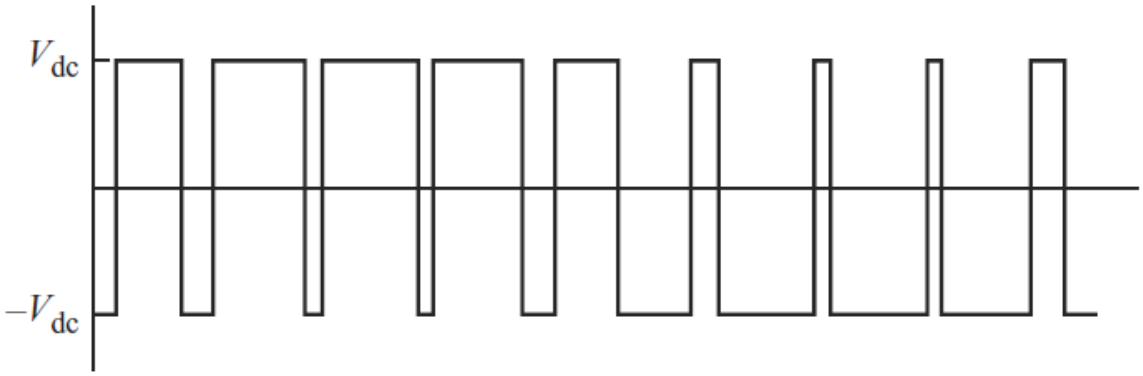
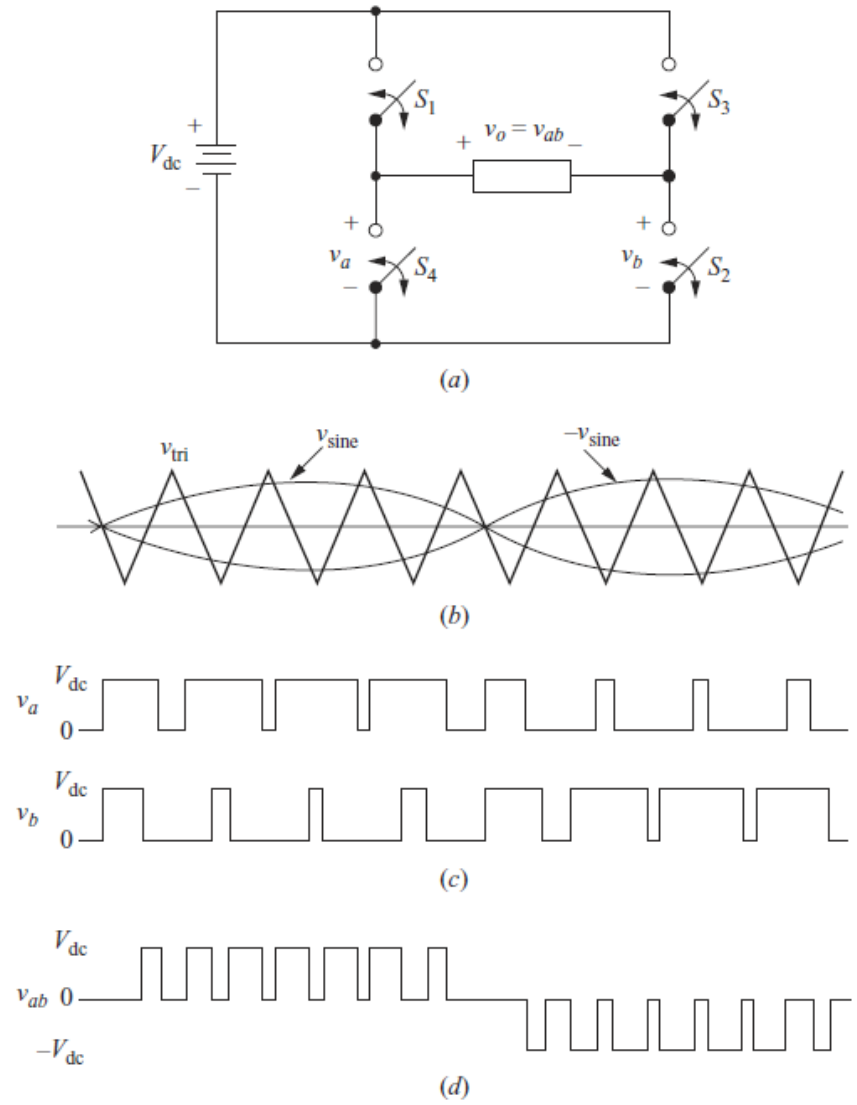


Figure 2-1. Bipolar PWM inverter output [19].

2.2.2. Unipolar Switching

Unipolar switching, the other PWM inverter switching method, will still have a triangular wave and sinusoidal waveform as control signals. The high frequency triangular wave establishes the switching frequency while the lower frequency sine sets the fundamental frequency. As previously mentioned, the control scheme creates pulses with modulated duty cycles at the output. Similar to the bipolar, the difference lies in the signature zero voltage state. In addition to positive input voltage and negative input voltage states, unipolar also features a zero voltage state. The zero voltage state reduces switching frequency harmonic level by lowering the voltage transients with an intermediate level. This will consequently reduce the noise level generated by the inverter as well as the output filter requirement.

The switching logic used in unipolar switching may be generated by two methods: Type 1 and Type 2. Type 1 consists of two sine control signals and a triangle signal. The switching is fast due to the greater number of times triangle and sine wave cross. The triangle waveform is the carrier wave and it generates the carrier frequency which all four switches operate at. Referring to Figure 2-2, switches S1 and S4 are in the opposite state of S2 and S3. For the added complexity, the scheme yields a better harmonic response. In contrast, type 2 switches operate at both the carrier frequency and the control frequency which is based on the sine wave as shown in Figure 2-3. Due to the slower control frequency, type 2 has less switching losses.



S1 is on when Vsine > Vtri

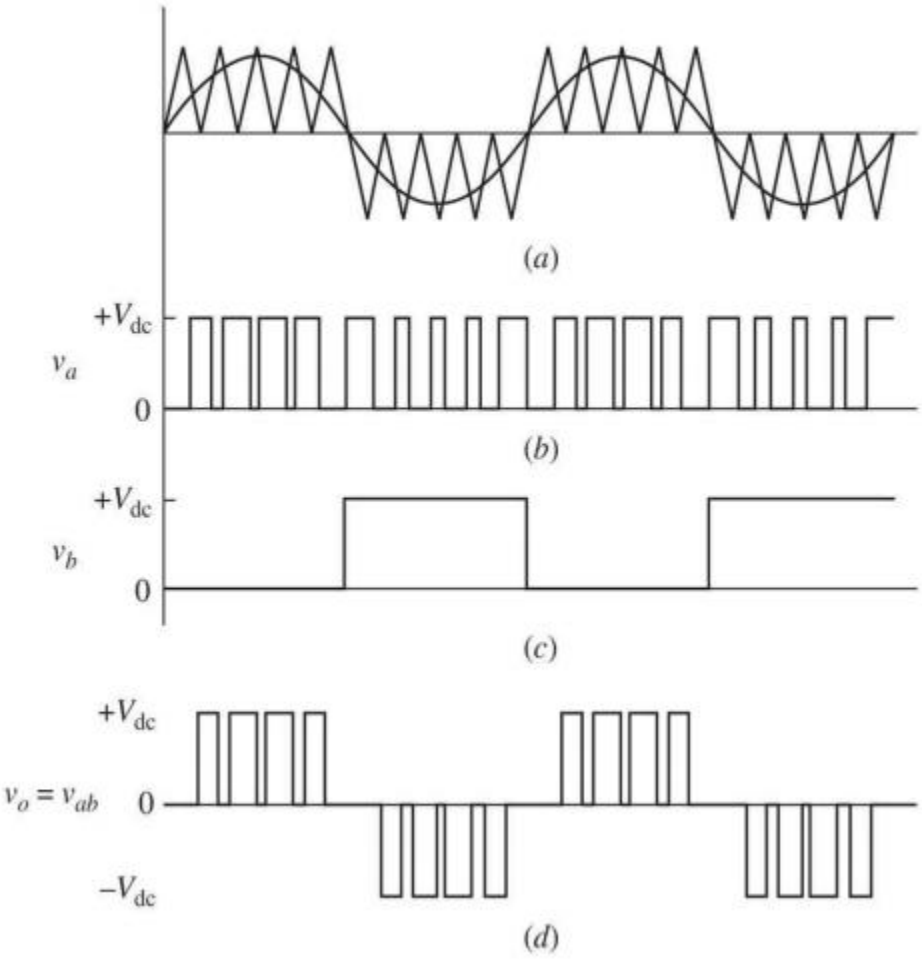
S2 is on when -Vsine < Vtri

S3 is on when -Vsine > Vtri

S4 is on when Vsine < Vtri

Figure 2-2. Unipolar PWM Type 1 switching and states; (a) Full-bridge converter for unipolar PWM; (b) Reference and carrier signals; (c) Bridge voltages V_a and V_b; (d) Output voltage [20].

Unipolar switching is typically featured in full bridge topologies due to the switching method utilizing all states made possible by the topologies. Advantages include less EMI noise due to higher frequencies making harmonics easier to filter. The higher frequency of the switching is separated from the sine waves fundamental frequency. Although the many states also help reduce the filter requirement, the complexity adds to the cost. The need for controls also adds to cost. Other disadvantages include the need for input voltage to be greater than the output peak.



S1 is on when Vsine > Vtri (high frequency)

S4 is on when Vsine < Vtri (high frequency)

S2 is on when Vsine > 0 (low frequency)

S3 is on when Vsine < 0 (low frequency)

Figure 2-3. Unipolar PWM Type 2 waveform and states. (a) Reference and control signals; (b) V_a; (c) V_b; (d) output V_a-V_b [19].

2.3. Half Bridge Inverter

The half bridge inverter is the most basic circuit among inverters. Consisting of only two switches, the circuit can generate AC from a DC source using a unique switching sequence. The load will see one of two states either a positive or negative source voltage at the load. Figure 2-4 shows the power stage of the topology.

The half bridge inverter is built with two capacitors and two switches. The half bridge name is derived from half of a full bridge converter. The half bridge inverter uses two equal capacitors to effectively provide two DC supplies voltages. The capacitors need to be large in order to maintain a constant voltage of Vdc/2. Along with the two switches, two output voltage states of positive Vdc or –Vdc are generated.

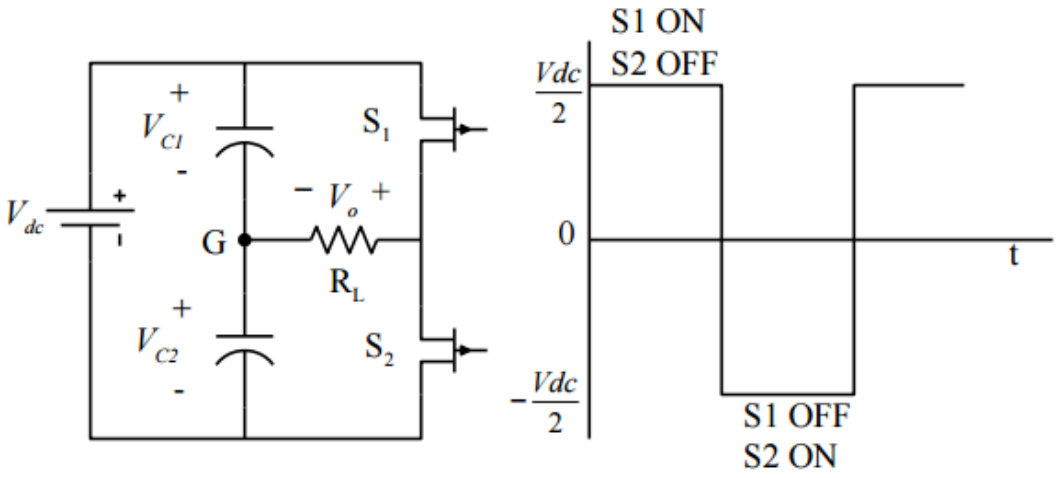


Figure 2-4. Half bridge inverter circuit and output [21].

Two switches allow for four combinations for the control signals. The four basic states are as follows. First, switch S1 is ON thus applying a positive current and voltage, VDC at the load. Secondly, switch S2 is ON and S1 OFF causing the load voltage to go negative VDC. There is also the both ON or both OFF state. Both ON is a short to the supply, while both OFF represents a dead time 0V to the load. A voltage imbalance can arise from using capacitors due to its leakage current. To prevent this, balancing resistors can be used to generate equal voltages but at the cost of more losses to the system.

The advantages of using the half bridge topology are its simplicity. Two switches represent two fewer than the full bridge inverter. As a result, the simple topology realizes lower cost and minimizes components used. Fewer switches also mean a straightforward control system that can reduce overall system cost. Typical cost associated with the control circuitry is also reduced. Simplicity also has its disadvantages. The key disadvantage stems from only having two output states. Fewer output states can result in increased Total Harmonic Distortion [THD] and a lower quality output. On top of needing a split supply to generate those two output states, they are only half the peak voltage possible with a full bridge.

2.4. Full Bridge Inverter

The full bridge inverter is one of the many great classic topologies used for inverters. The topology is also known as an H-Bridge inverter due to the placement of the load and switches. At a base level, the full bridge inverter generates AC voltage from a DC voltage. The full bridge inverter has four switches seen in Figure 2-5. Using two additional switches compared to the half bridge, the full bridge can output three unique states rather than two.

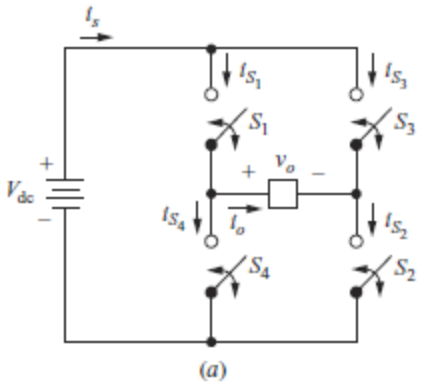


Figure 2-5. Full bridge inverter [19].

Table 2-1. Full Bridge Inverter States

Switches Closed	Output Voltage
S_1 and S_2	$+V_{DC}$
S_3 and S_4	$-V_{DC}$
S_1 and S_3	0
S_2 and S_4	0

The H-bridge inverter is capable of generating five useful states. Starting with S1 and S2 ON, this state will put +Vdc to the load. Followed by S1 and S3 turned ON, to place 0V at the load. After that, S3 and S4 are ON to send the load to –Vdc as seen in Table 2-1. Finally S2 and S4 are on to send 0V to the load again.

Unlike the half bridge, a supply split using capacitors is not needed to provide the two voltage levels. Although the full bridge does need capacitors for the supply voltage, it does have two additional switches and a slightly more complex control system for them. With the additional complexity, the unipolar inverter can utilize four states as opposed to the half bridge that does not use the 0V state.

2.5. Literature Review

The literature review looks at the foundation of the inverter topology. By understanding each stage, a better understanding of the topologies and challenges can be gained. When looking at the previously researched topics, the same basic building blocks apply. Eventually the thesis, after thorough literature review, can make a case for a unique solution or an improvement of previous work of an inverter.

One of the commonly used inverters is the square-wave H-bridge inverter. In its basic topology, the square-wave inverter is simple both in the topology and control scheme. However, the inverter suffers from high harmonic content on its output voltage due to square-wave like shape of the AC output. Therefore, this type of inverter is not ideal for sensitive applications or for any applications requiring sinusoidal AC waveform [22]. This is where the multilevel inverter can offer a better solution.

Multilevel inverters fall into several categories of research. Conventional multilevel inverters include cascaded H-bridge, diode clamped, and flying capacitor multilevel inverter types as depicted in Figure 2-6 and as surveyed by Rodriguez et al [23]. Some multilevel topologies utilize innovative switching approaches like the full-bridge with bi-directional switching interconnections [24].

Multilevel inverters with varying number of levels have been explored. Each design has different advantages such as improved output waveform, filter size, and lower EMI which constitute major concerns in inverters [23]. Multilevel inverters specifically improve AC power quality by converting the DC input into small voltage steps to shape the AC output waveform to be close to a sinusoidal shape, which results in lower harmonic distortion compared to the simple square-wave inverter [24].

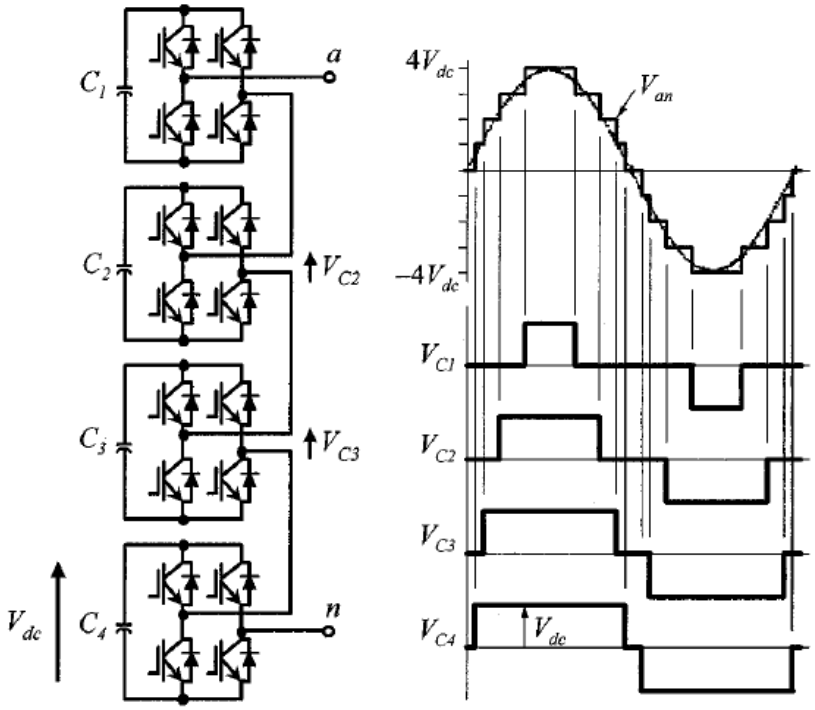


Figure 2-6. Cascaded inverter circuit topology [23].

One example of multilevel inverter involves topologies that produce a five level square wave AC output voltage. Reference [24] discusses a five level topology that has a fifth switch in between two half capacitors for improving harmonic components compared with that of a traditional full-bridge three level PWM inverter. A proposed seven-level topology was also discussed in [24] by adding two additional switches. This will further improve the output voltage waveform although the increased number of switches does increase switching losses and total cost. The paper, however, lacks investigation and detail of loaded operation with LC filter. In [23], a second single-phase five level PWM inverter design utilizes a deadbeat control scheme to improve dynamic performance. This design adds a switch and four diodes to the center-tap of a DC power supply. Doing so allows for half of the DC supply voltage to be generated. The deadbeat

control scheme is adopted to replace LC filter and switching frequency based sinusoidal output. Two control loops are used to control amplitude, harmonic components, and compensate the filter inductor. The resulting output waveform shows the ability of the topology with the control scheme to maintain a sinusoidal output regardless of load. Unfortunately, this design requires a complex control algorithm while only slightly improves the THD from a cascaded five level inverter. The proposed five step inverter described in this thesis promises significantly less complex control scheme while improving THD.

This thesis expands upon prior works done on senior projects on multilevel inverters, specifically the interconnected H-bridge power inverter. In the previous works, the first step involves recreating the circuit in question using computer simulation followed by hardware implementation which includes digital control signal portion. But each project approaches the problem in a slightly different way and comes away with their own conclusions.

In Soares' senior project [25], the multilevel topology implements Complex Programmable Logic Device (CPLD) for switch control and signal amplifiers instead of switch drivers. The focus of the project was to generate control signals from the CPLD. Unfortunately, the system lacks dead time leading to crossover or shoot through. A finite state machine is used to organize the many switching states and dead time intervals. The circuit also utilizes anti-parallel diodes to handle reverse current spikes. Issues include capacitor discharge, resistive losses in the circuit and RDS-on of the MOSFET, all affecting full load operation. It is also noted that the safe operating area of the MOSFETs used turns out to be an issue at low VDS values. As a result, full load operation was not successful.

Next, Steven Lee and Raul Alexander Aidama's senior project [26] also used the same topology that produces a six step output and reduced total harmonic distortion.

The specifications look to support 50W with 12V input voltage as a mid-range commonly used voltage by batteries. Highlighted challenges include writing the FPGA based microcontroller codes in VHDL for the switching logic and component selection for the hardware. The results though were not as expected with the Vdc/2 step missing. Also past 50% of full load, the power supply used hits the current limit and hence it was unable to support loads of that level. Improvements suggested include using a PCB board to reduce noise from leads used to connect the MOSFET and drivers.

Another work is by Muehleck [27] which has eight steps instead of six by using nine switches as illustrated in Figure 2-7. The project concludes with seven step inverter which has lower harmonics compared to the five and standard square wave inverter. Unfortunately, the project did not attempt a hardware prototype, and so it lacked any load testing.

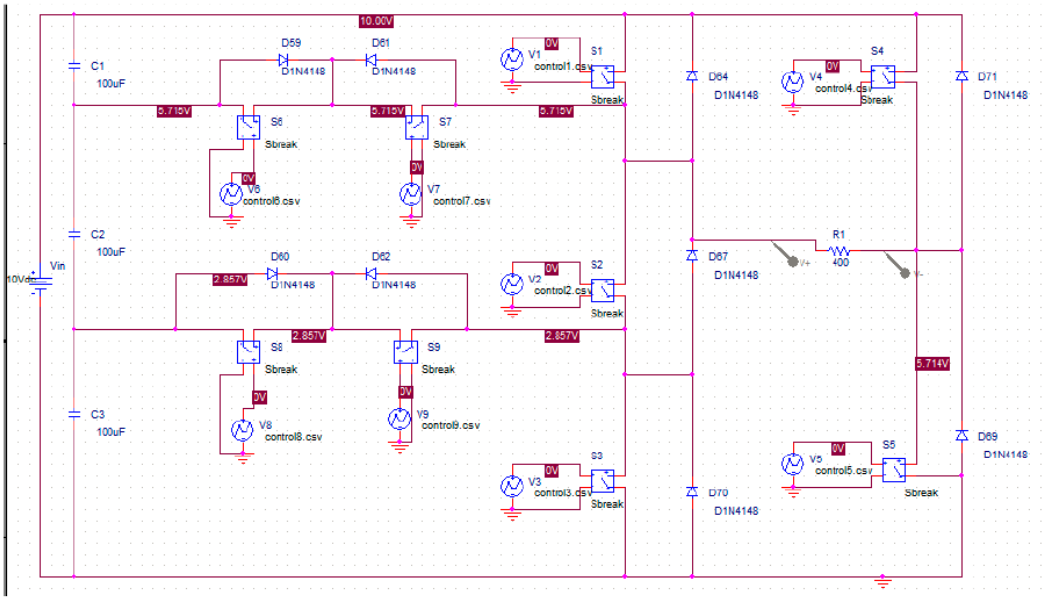


Figure 2-7. Multi-step inverter by Muehleck [27].

The objective of this thesis is to design and build a five level inverter implementing digital circuit to produce the switching signals. Furthermore, the thesis also

explores the implementation of digital circuit to produce switching signals and investigates a suitable output filter design to lessen the harmonic content of the output voltage. As a thesis statement, the proposed five level inverter with microcontroller to produce the switching signals will provide a less complex control circuitry and easier adjustment of inverter's output voltage parameters compared to their analog counterpart.

Chapter 3. Project Overview and Constraints

3.1. Overview

The proposed design will improve on previous attempts on the H bridge interconnected multilevel inverter. Figure 3-1 shows a block diagram of the major components of the inverter circuit design. It consists of an input stage, inverter switching, control system, and output filter. At the most basic level the circuit is essentially a square wave inverter with a few additional steps. As for any other inverters, the goal is to generate an AC output voltage from a DC supply.

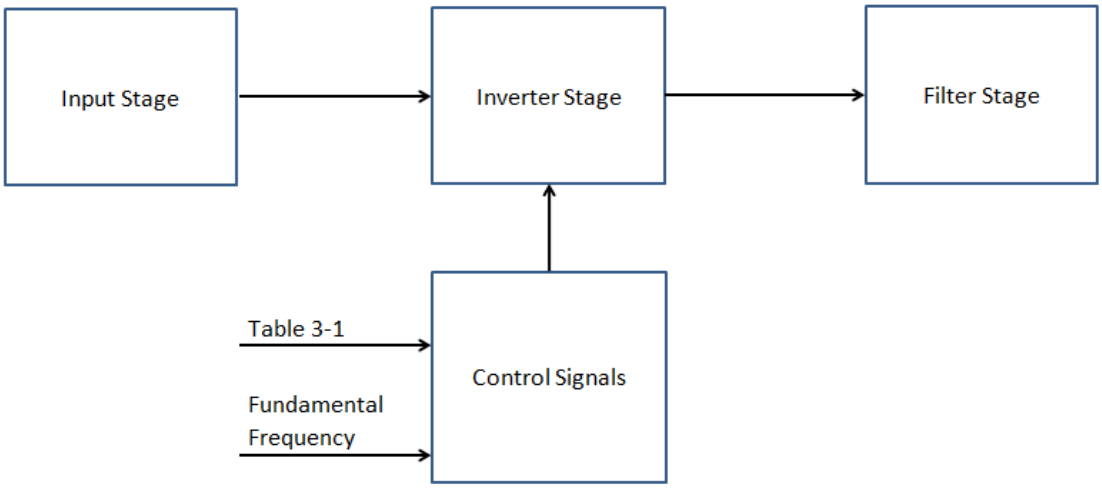


Figure 3-1. General block diagram of inverter circuit.

For the proposed inverter, the input stage consists of a DC power supply such as a battery and two DC balance capacitors. By putting two equal capacitors in series, they can act as voltage dividers for the DC source voltage and create two DC supplies to the inverter. All together the DC source voltage will be the positive and negative DC voltage rails, and capacitors will create intermediate steps between these rail voltages and zero.

Next the control signals will be exclusively generated by a microcontroller in place of discrete components. The main reason for using microcontroller lies on the complexity of timing the switching signals if discrete components are utilized. The software based custom control signals will definitely make it more convenient to manage the switch timings. Accurate timing is crucial in multilevel inverters as it directly affects the quality of AC output voltage waveform.

The control signals are connected to the inverter stage, which consists of FETs used as switches and driver ICs. The FETs will switch depending on the bias voltage outputted by the drivers following the microcontroller switching signals. The output voltage from the driver will be increased based on which FET it is driving. This section is responsible for connecting the DC side to the AC side of the inverter by switching at predetermined timings. By doing so, power is delivered to the load at different voltage levels, hence creating the multilevel effect on the AC output voltage waveform.

Lastly, the filter stage will be responsible to shape the AC output voltage waveform to be closer to a sinusoidal shape. This is done through suppressing the higher frequency content of the multilevel AC waveform, thus making the fundamental frequency component (60Hz or 50Hz) the most dominant. Ideally, the AC output voltage waveform should only contain the fundamental frequency component. However, this is not viable due to cost constraint of designing the filter as well as parasitic components in the filter. The filter will be a low pass LC filter in order to preserve the fundamental frequency of the signal. Depending on the DC voltage input to the inverter, the AC output waveform may need to be stepped up to a desired RMS voltage.

The proposed inverter's output consists of 5 unique voltage levels and 8 states per cycle. Table 3-1 summarizes the different switch states with the corresponding proposed circuit as shown in Figure 3-2. An example of steady-state five-level unfiltered AC output voltage waveform is depicted in Figure 3-3.

Table 3-1. H-Bridge Interconnected Inverter States

State	Switches Closed	Output Voltage
1	SW3 and SW4	0
2	SW4 and SW5	$+V_{DC}/2$
3	SW2 and SW4	$+V_{DC}$
4	SW4 and SW5	$+V_{DC}/2$
5	SW3 and SW4	0
6	SW1 and SW5	$-V_{DC}/2$
7	SW1 and SW3	$-V_{DC}$
8	SW1 and SW5	$-V_{DC}/2$

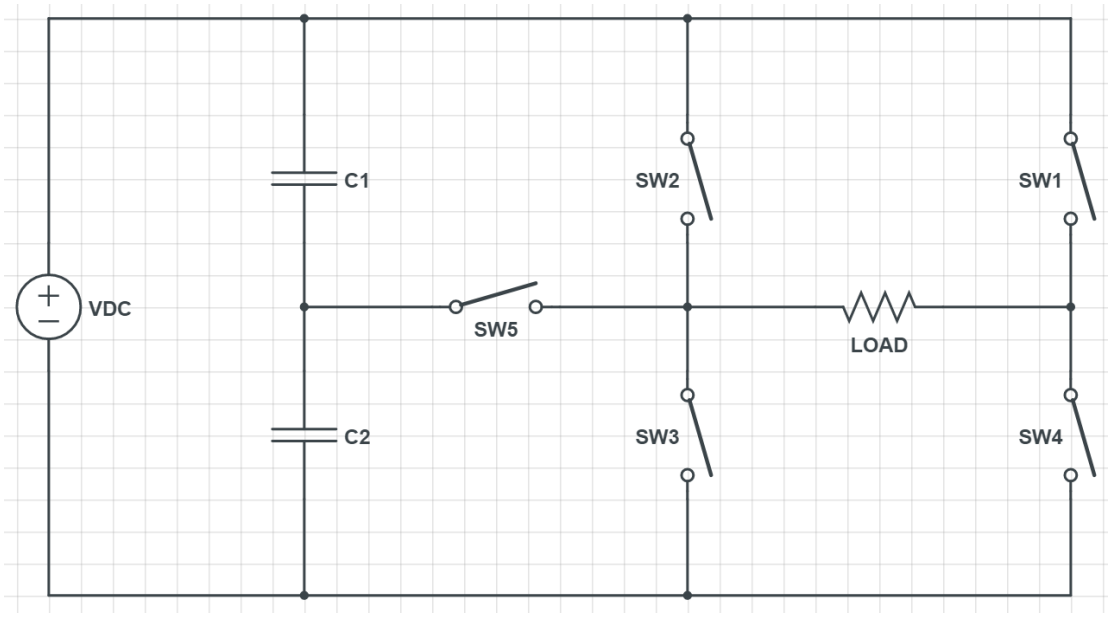


Figure 3-2. H-Bridge interconnected inverter circuit.

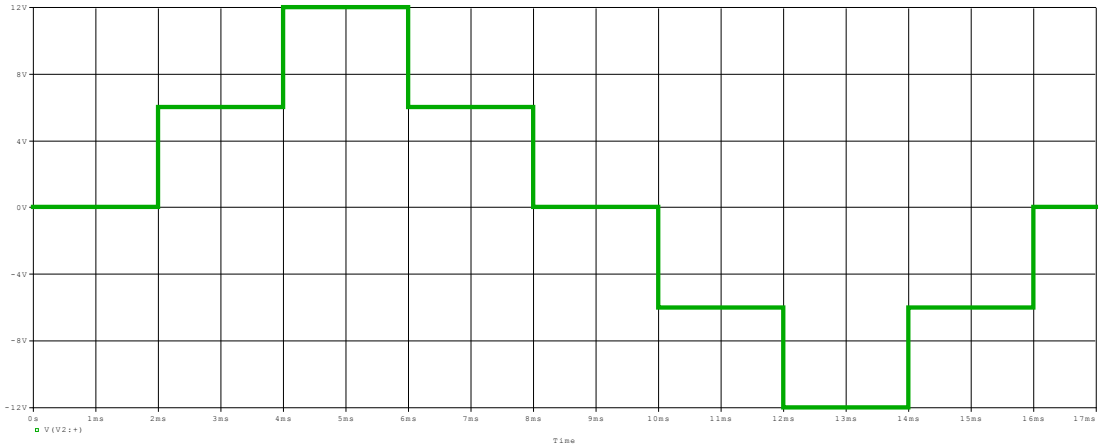


Figure 3-3. H-Bridge interconnected inverter output.

3.2. Criteria

The objective for this thesis is to implement a unique inverter design, specifically the single phase interconnected H-bridge inverter, which ultimately reduces typical inverter circuit complexity while maintaining or improving quality of output voltage. Previous attempts with the design will be leveraged and improved upon; thus, focusing on issues that have come up in the past including high output loads and physical hardware execution and design.

To achieve the desired output for the inverter, there are several specifications that need to be noted starting with the input voltage. Since the input voltage will be DC, the proposed input will be a 12V which will represent a typical battery voltage. In order to easily integrate with existing applications, the output voltage will need to represent the main voltage with 120Vrms 60Hz operation by stepping up the voltage with a transformer.

As one of the main goals is to maintain a high quality output, an output filter will need to be designed to obtain the near perfect sinusoidal shape output. The filter will be simulated and constructed for hardware testing. To track the quality of the inverter output

before and after the filter, the THD will be measured in simulation and in the hardware implementation. An analysis of THD values of a basic square wave inverter will be simulated as a reference point to compare with the proposed design. Ideally, the output THD would meet IEEE established standards to properly integrate with the main voltage line.

In terms of the output power, the goal is to support up to 50W at greater than 90% efficiency at full load. The mid-level power output is sufficient for prototyping purpose and it can still provide power to a number of applications including a typical light bulb. A variable resistor will be used to create and report an efficiency curve over load variation.

Lastly, the design will be built on a PCB to improve organization and quality of the hardware testing. The PCB will need to account for cooling requirements to handle the high inverter loads. When necessary, additional hardware will be used to manage the heat throughout the board.

Table 3-2. Summary of Inverter Design Constraints

Design Variable	Design Specification
Input Voltage	12V
Output Voltage	120Vrms
Output Power	50W
Switching Frequency	60Hz
Total Harmonic Distortion	5%
Full Load Efficiency	90%

.

Chapter 4. Design and Simulation

This chapter explains the design process focusing on the selection of the main components in the proposed inverter topology. With the specifications to meet and design in mind, a wide ranging research phase was conducted. Upon completion of the design process, a computer simulation using OrCAD Pspice was then performed to verify the functionality of the design. Results of the computer simulation will also be presented in this chapter.

4.1. FET Selection

The maximum voltage rating and current limit of the FET are the two major specifications to focus on. The maximum voltage is equal to the input voltage of 12V. By adding some headroom to account for any parasitic inductance, the maximum Vds voltage of the FET was chosen to be 30V. Secondly, the maximum average drain current comes out to be 50W/12V=4.16A for the inverter. As long as the maximum continuous drain current is high enough to also account for heating, the FET will function properly. From the parameters calculated, a baseline was created in selecting which switch to use. Next, a list was created that meets these specifications. The list tracked package type, Vds, Id, Qg, and Rds. These parameters were used to calculate a figure of merit to determine which FET would perform best. The figure of merit (FOM) was the product of the gate charge Qc and on-state resistance Rdson. The gate charge parameter is important because it offers the gate to source capacitance value that needs to be charged to increase the gate threshold voltage necessary to turn on the switch as illustrated in Figure 4-1 [28]. This correlates with the speed at which the switch can be turned on and is tied to the switching losses that can be improved upon. In the end, the lowest gate charge and high current capacity was selected to ideally reduce shoot

through and any heating issues arising from the current requirements. Also, taken into consideration was the availability of samples as well as spice models for the simulation. The STP95N3LLH6 by ST Microelectronics was chosen based on the specifications seen in Table 4-1.

Table 4-1. FET Specifications.

Part #	STP95N3LLH6
Package	TO-220
Vds (V)	30
Id (A)	80
Qg (nC)	20
Rds (Ω)	0.0075
FOM	0.150

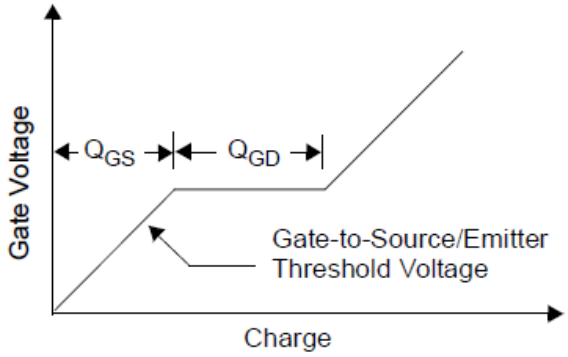


Figure 4-1. Gate charge waveform [28].

4.2. Microcontroller Selection

A microcontroller will be needed to program and generate switching control signals as seen in Figure 4-3. Research into available hardware options for control sought a flexible tool for the unique switching scheme to be implemented. Considering the custom signal needed, a microcontroller based digital solution offered the most

promise toward the desired signal. Equipment that was readily available was also taken into consideration. Between Microchip and Atmel, the Atmel ATMega256 was readily available and thus chosen for this project. In addition, the ATMega256 had a long list of features that were promising for the project requirements. These features include programmable memory to retain the signals, PWM modules to support the switch signals, and also multiple general purpose output pins for any other hardware needs.

4.3. MOSFET Gate Driver Selection

In terms of the driver, there are many available on the market which range widely in functionality and options among vendors. When it comes to selecting one, there are no simple guidelines on what to choose and how to go about it. The application notes go in depth which actually adds to the complexity. Details regarding how each pin from the driver IC interacts with the external I/O present unfamiliar territory that explore things like output impedance, power pins, and digital I/Os. Capacitance and oscillation on the inputs are other considerations that need attention. Research was done to understand these requirements and the interactions with the other components. For example, the source inductance and parasitic capacitance on the gate will create a resonant circuit that needs to be damped by the gate resistor which is part of the series resistive components [28].

A list of potential drivers was created and each was individually reviewed to check for the required functionality and any unfamiliar ones that need additional review for full understanding. Specifications vary per driver thus each driver raises a new set of questions. Bootstrap operation support differs between parts. Also, charge pump implementation differs, where some require external parts and others don't. Programmable dead time is also a key feature that could minimize distortions on the

output [29]. Each of these unique driver features are new topics critical to understanding how drivers work.

When considering which drivers to choose, the specification difference between low and high side is also something that needs to be considered. The high side will have to support a higher voltage range. Also the current capacity needs to be high enough to charge the gates and switch quickly. Larger FETs will generally require more current to switch. The final solution selected [UCC27424] offers two outputs per IC; thus, high side and low side switches are driven by the same driver part.

Some full bridge and half bridge driver ICs require high input logic thresholds that the ATMega256 is not capable of providing. The ease of obtaining samples also factored into which vendor to use. Some app notes were consulted from TI and Microchip for determining the right driver for this application. Peak gate current and input voltage ratings were listed and compared. The table in Figure 4-2 of similar parts from other manufacturers was also reviewed [30].

General Purpose MOSFET Drivers: Pin-Compatible Devices

Texas Instruments	MicroChip	Micrel	Maxim	ON Semi	Texas Instruments
UCC37323 and UCC27423 4 A dual inverting	TC426 TC1426 TC4423 TC4426	MIC426 MIC1426 MIC4423 MIC4426	MAX626 TSC426 MAX4426	MC33151 MC34151 NCP4413 NCP4423	**TPS2811** 2 A dual inverting
UCC37324 and UCC27424 4 A dual non-inverting	TC427 TC1427 TC4424 TC4427	MIC427 MIC1427 MIC4424 MIC4427	MAX627 TSC427 MAX4427	MC33152 MC34152 NCP4414 NCP4424	**TPS2812** 2 A dual non-inverting
UCC37325 and UCC27425 4 A Dual (one inverting, one non-inverting)	TC428 TC1428 TC4428 TC4428	MIC428 MIC1428 MIC4428 MIC4428	MAX628 TSC428 MAX4428	MC33153 MC34152 NCP4425	**TPS2812** 2 A dual (one inverting, one non-inverting)
UCC37321 Single 9 A inverting		MIC4420 MIC4421 MIC4451		NCP4421	
UCC37322 Single 9 A non-inverting		MIC4429 MIC4422 MIC4452		NCP4422	

Figure 4-2. Driver selection table [30].

Several other categories of ICs were also surveyed as potential building blocks for the design. This included PWM controllers, multistep inverter, and other types of inverters. Since PWM controllers are associated with inverter switching, these controllers may aid in the design depending on how PWM switching can be controlled. Research shows there are currently no ICs for any type of power inverter. The power requirements make integrating the FET not feasible but control and drive circuitry is available in aiding inverter designs.

4.4. Capacitors

There are several capacitors in the design each of which serve a different purpose. The input capacitors will store energy to support any large changes in the load. The capacitor values will also need to be equal to act as a voltage divider for the mid-level voltage for the multilevel output voltage. A simulation was run to determine what value of capacitor is sufficient. Different capacitor values were used until the voltage levels were stable on the output. In the end, 1800µF aluminum electrolytic capacitors were selected due to low ESR and high capacitance characteristics. Also, the design had a peak voltage of 12V and the capacitors also had to account for any overshoots on the input; thus, a 16V rating was selected.

The design also includes bypass capacitors for the drivers. The 0.1µF and 100µF capacitors were recommended by the UCC27424 datasheet to prevent noise and help with high current peak to the load.

Lastly, the output filter will also feature a capacitor. The capacitor will be determined by the filter design which will be discussed later.

4.5. Simulation

The first set of simulations look at the various parts that make up the inverter design in order to lay the foundation for future analysis. To start, simulations were run on each FET to verify the gate voltage thresholds. The STP95N3LLH6 in this case has a 2.5V threshold. Next, two capacitor DC sources were also tested to see how each performs as a DC supply. Lastly, the four control signals were generated and compared side to side to ensure proper timing as seen in Figure 4-3.

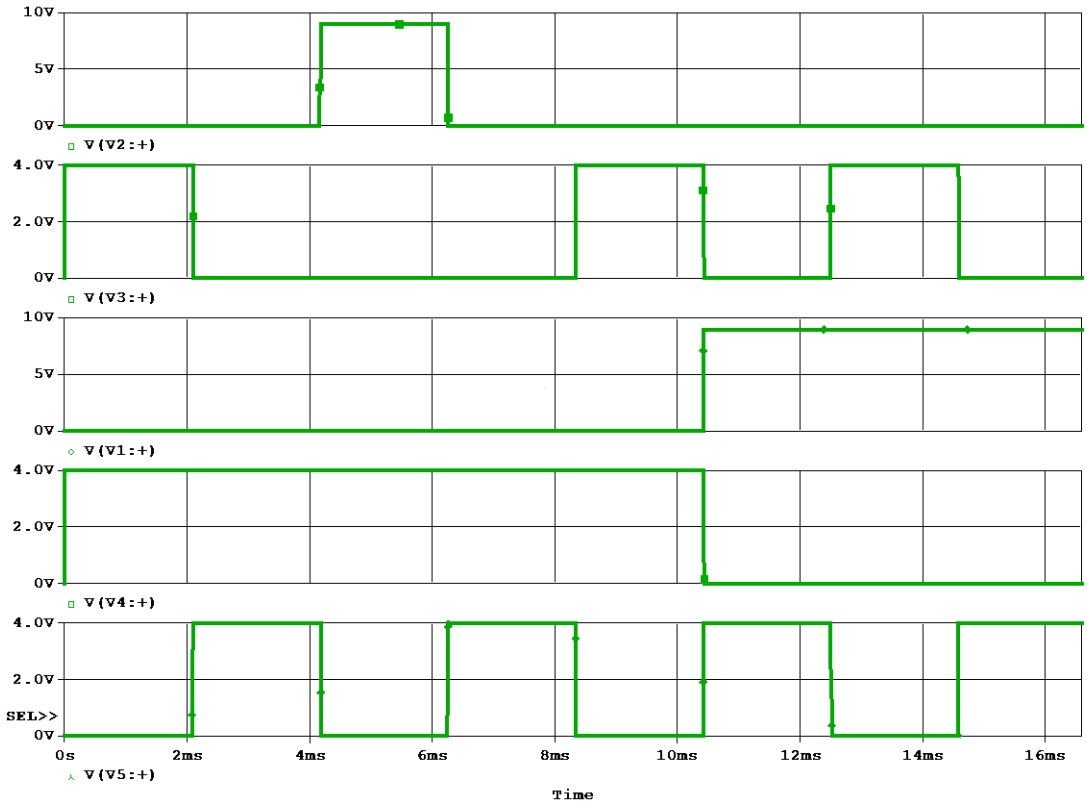


Figure 4-3. Switching control signals.

After simulating the individual blocks, the first circuit simulation involves the baseline circuit using generic switches as seen in Figure 4-4. The first simulations done had very large input capacitors to hold the half supply voltage with input voltage starting

out at 10V. Also at this point, the four custom control signals had been implemented, and a fixed resistive load was used to generate and observe an unfiltered output. Figure 4-5 shows the output voltage waveform.

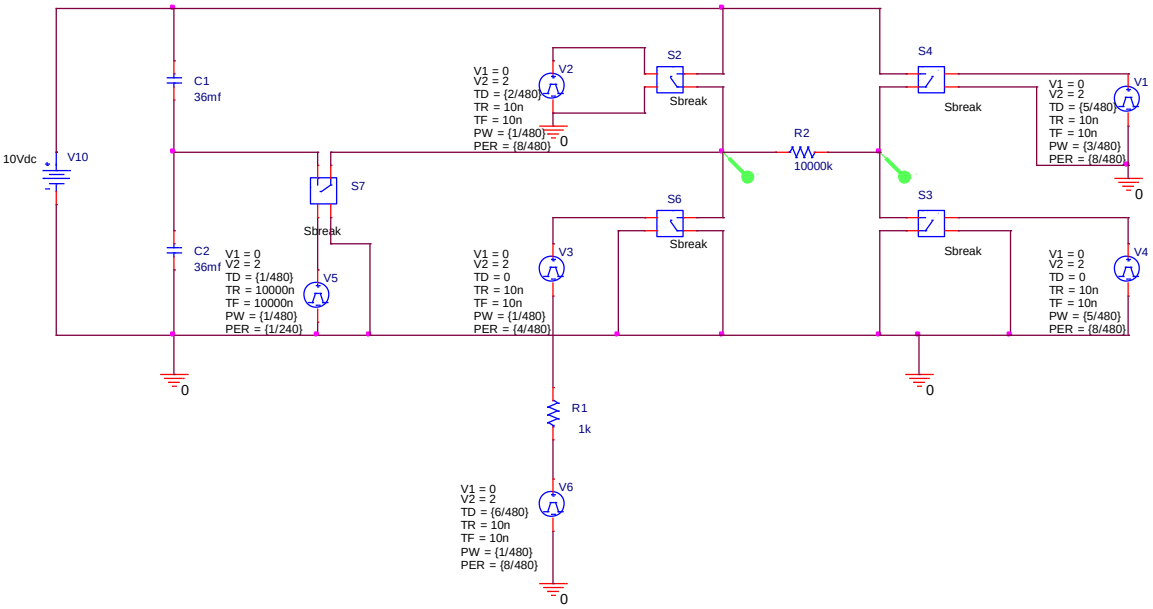


Figure 4-4. Basic simulation circuit for multilevel inverter.

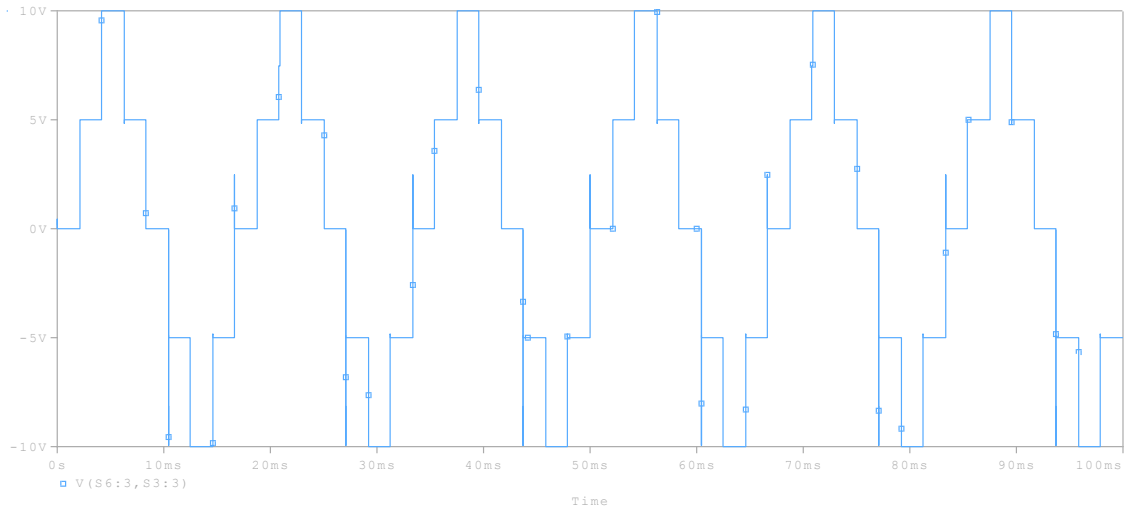


Figure 4-5. Multistep single-phase inverter output.

4.6. MOSFET Simulation

The next step in the simulation involves adding a FET to the model to see if the results are the same as previously obtained with generic switches. In this schematic model shown in Figure 4-6, a filter capacitor was put on the load to remove any high frequency noise and input capacitors were increased to maintain the VIN/2 level.

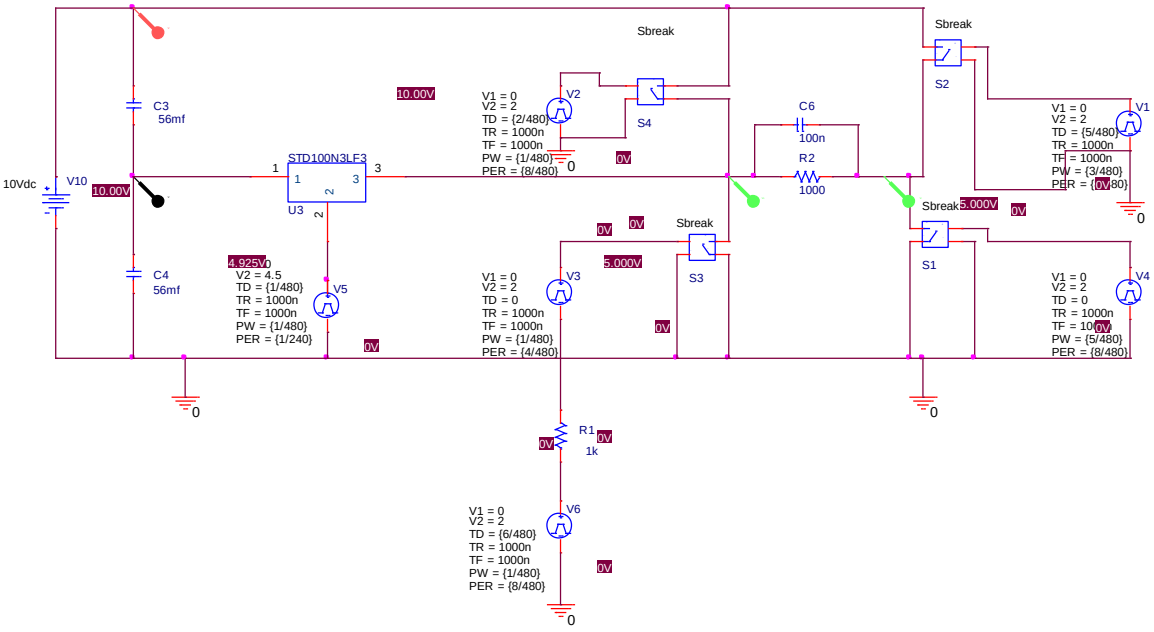


Figure 4-6. Simulation circuit with FET integrated.

The output shows issues with multiple voltage levels mainly with positive voltage side as seen in Figure 4-7. The cause of the issues was later traced back to the FET that was put in.

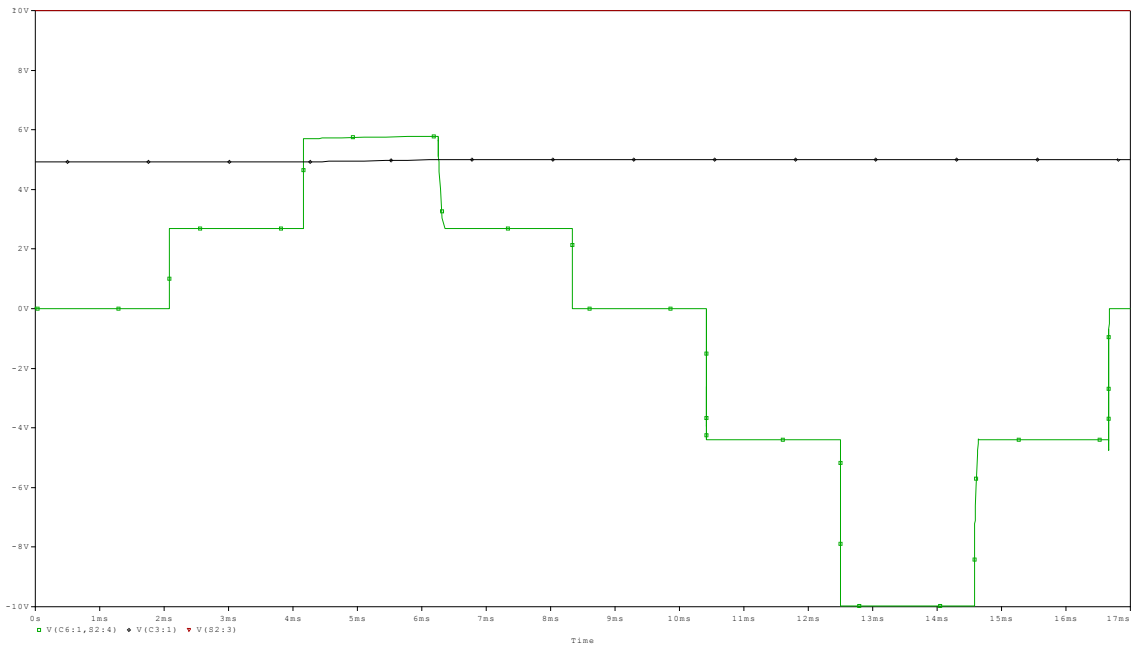


Figure 4-7. Inverter output voltage of circuit in Figure 4-6.

Considering the only major change made to the previous model was the 5th switch, the next schematic seen in Figure 4-8 leaves the 5th switch generic while the other 4 are replaced with the STD100N3LF3 FET model. Simulation results in Figure 4-9 show that the integration of the FET model was successful.

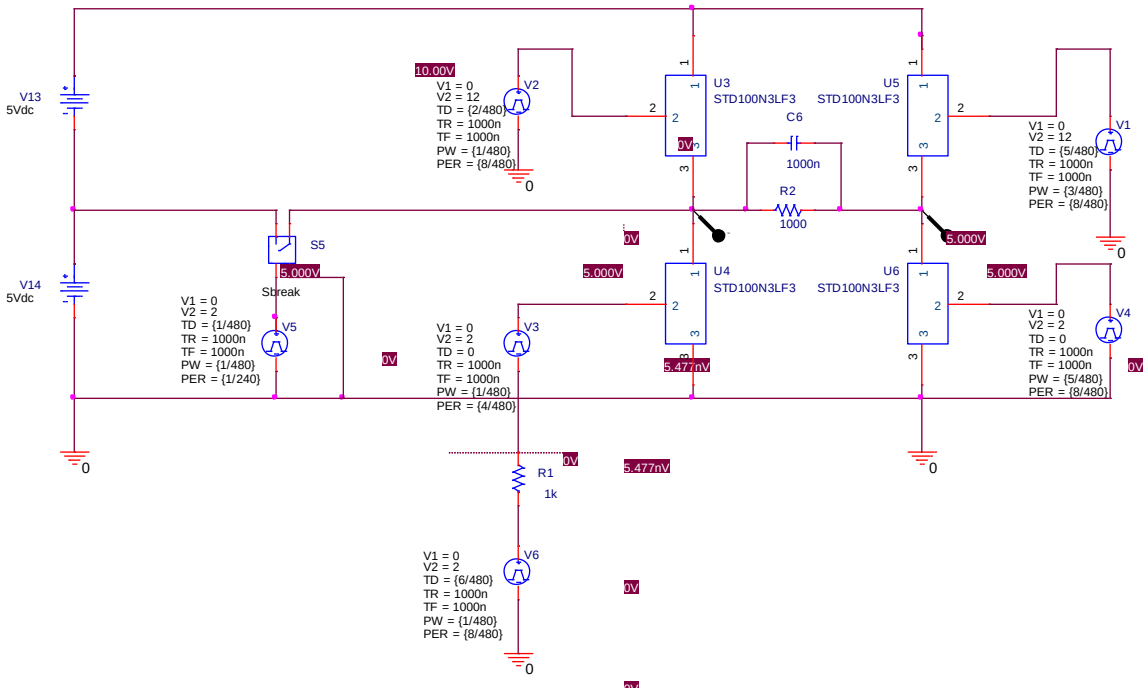


Figure 4-8. Simulation circuit with four FETs.

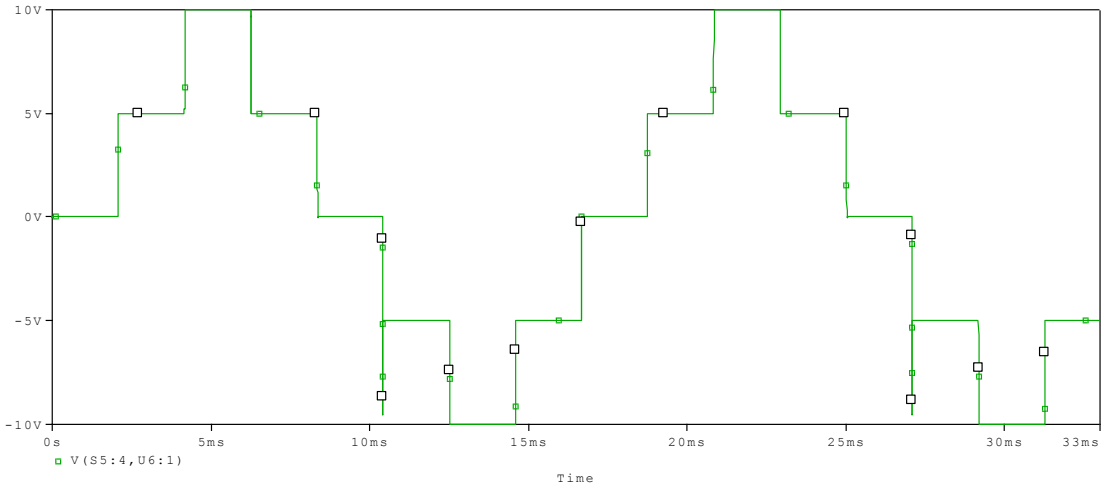


Figure 4-9. Inverter output voltage of circuit in Figure 4-8.

Further research shows the STD100N3LF3 has a freewheeling diode that can be problematic for the certain states of the multilevel inverter. When the 5th switch is off, current can flow through the diode and cause havoc on the voltage levels of the inverter output. To prevent this issue, the concept of putting two FETs back to back with the

diodes of each pointed in opposite directions was explored. A simulation was run on the back to back FET configuration in Figure 4-10 to test the behavior of the current flow. Note that both FETs are driven by the same control signal. In Figure 4-11, the input voltage can be seen on load resistor R3 with the pattern of the control signal as expected.

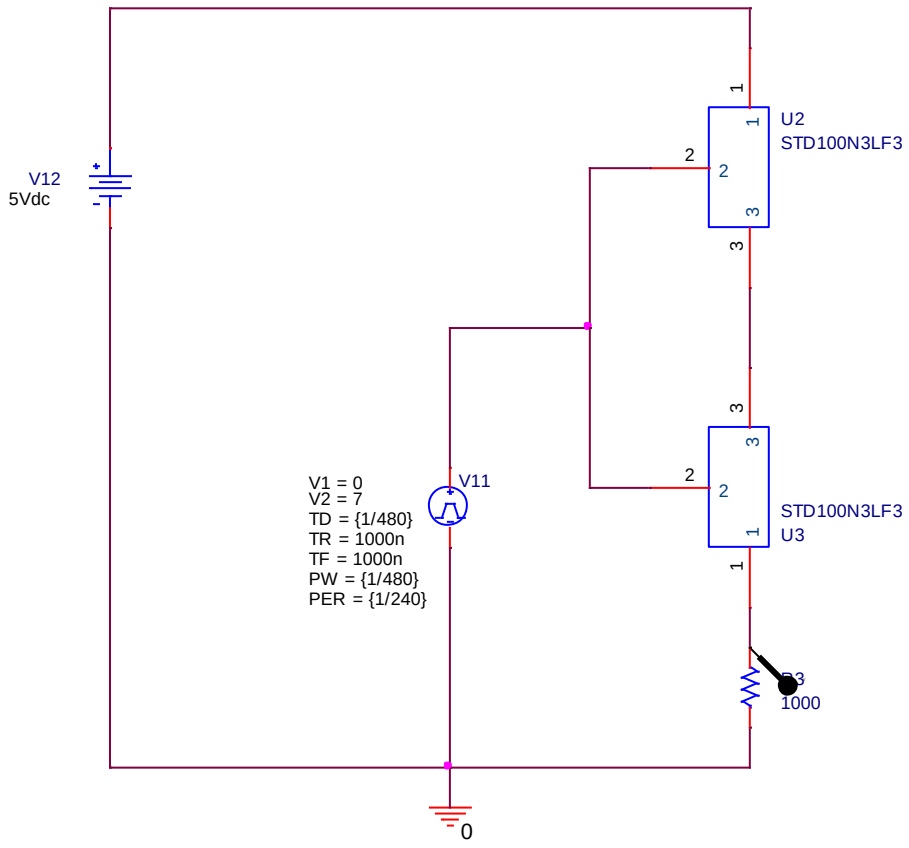


Figure 4-10. Back to back FET circuit.

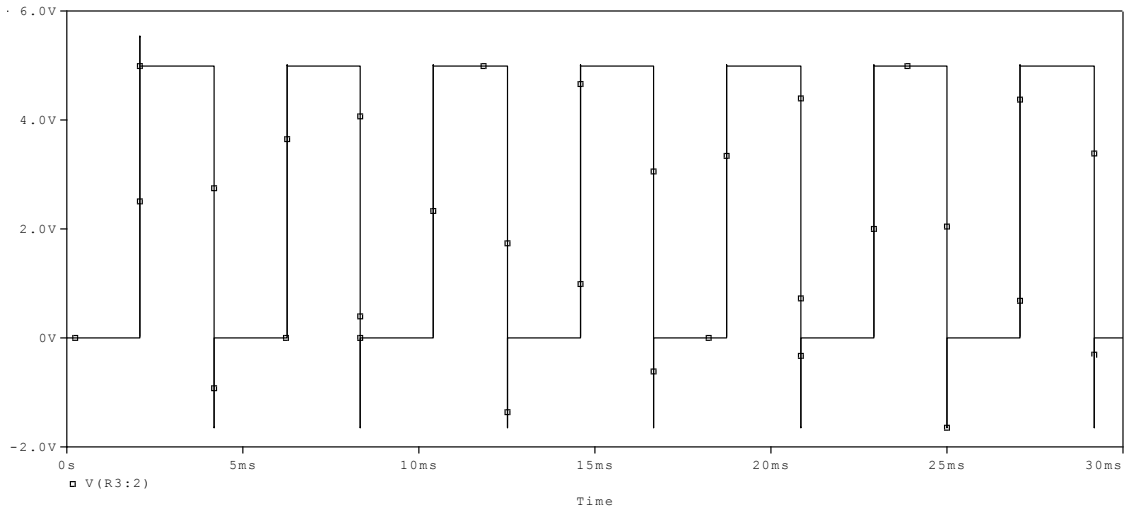


Figure 4-11. Simulation result of FET circuit with switches ON.

With the solution to the 5th switch issue, all generic switches were replaced with FETs to run the simulation once again. However, using FETs in the simulation caused convergence issues. To solve these issues, the auto converge feature was used [31]. The updated circuit in Figure 4-12 was simulated resulting in a clean inverter AC output waveform. As shown in Figure 4-13, the capacitors adequately hold the mid level voltage 6V to provide a proper multilevel inverter AC output.

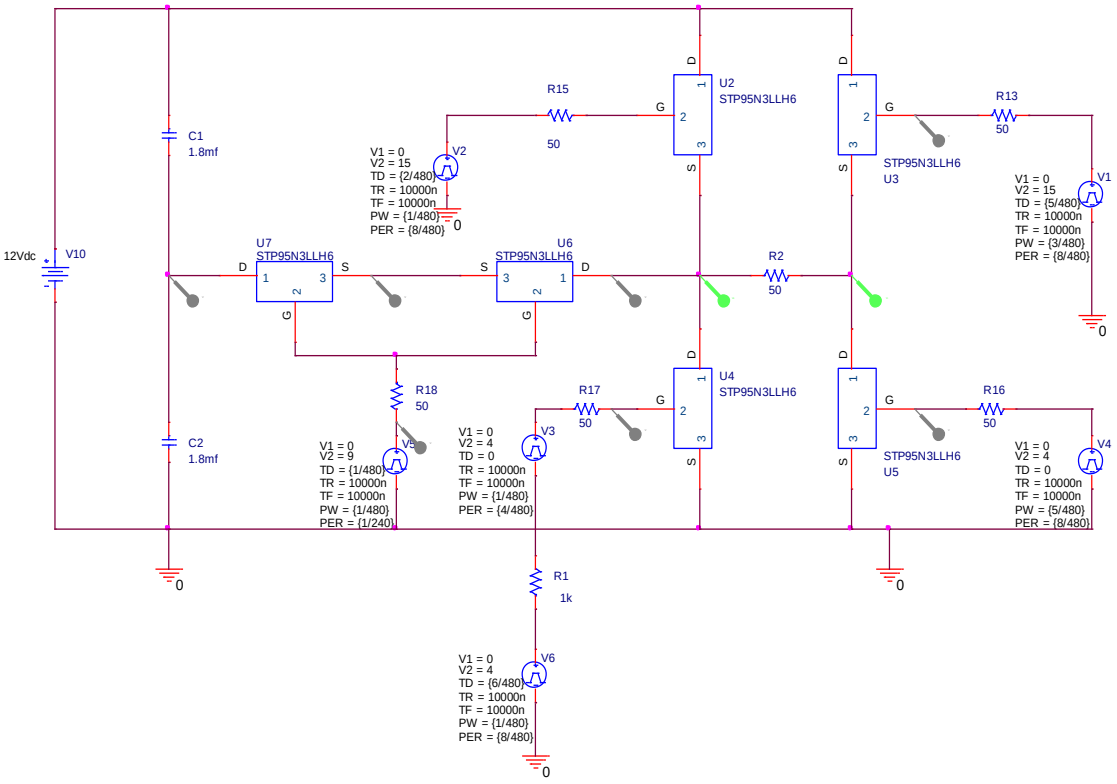


Figure 4-12. Inverter circuit with capacitor divider voltage source.

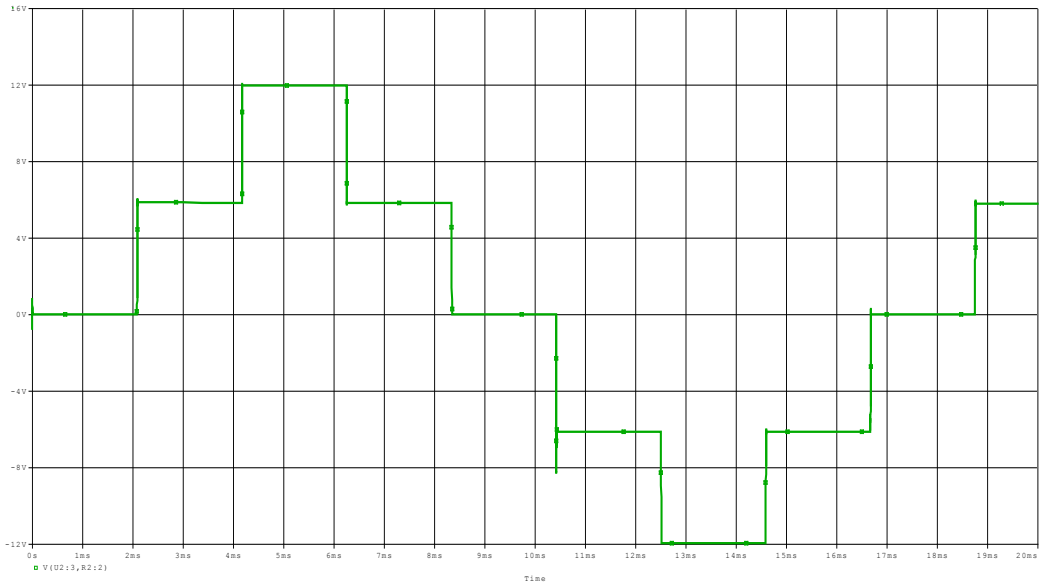


Figure 4-13. Inverter simulation output with capacitor divider voltage supply.

4.7. Complete Circuit Simulation

The next step involves simulating the drivers ICs and LCL filter. To simulate the drivers, the models for the UCC28624 were obtained from the vendor. Importing the model to the design and replacing generic sources previously used, the model will more accurately predict the outputs of the design.

The driver models were first tested separately to verify their expected operation. Given the fact that the part is an 8 pin driver, the integration was a bit more involved. The data sheet provides an application circuit to guide how to properly bias and place passive components on each I/O. A different set of parts were needed for high side and low side drivers. This way the two sides are isolated from each other in terms of control. Each driver in the simulation is fed a custom control signal generated by the VPULSE source model. Also the drivers are fed two separate DC sources for the two DC levels needed by the FETs. Lastly, the schematic includes test point connectors but these did not affect the simulation. The complete circuit can be seen in Figure 4-14.

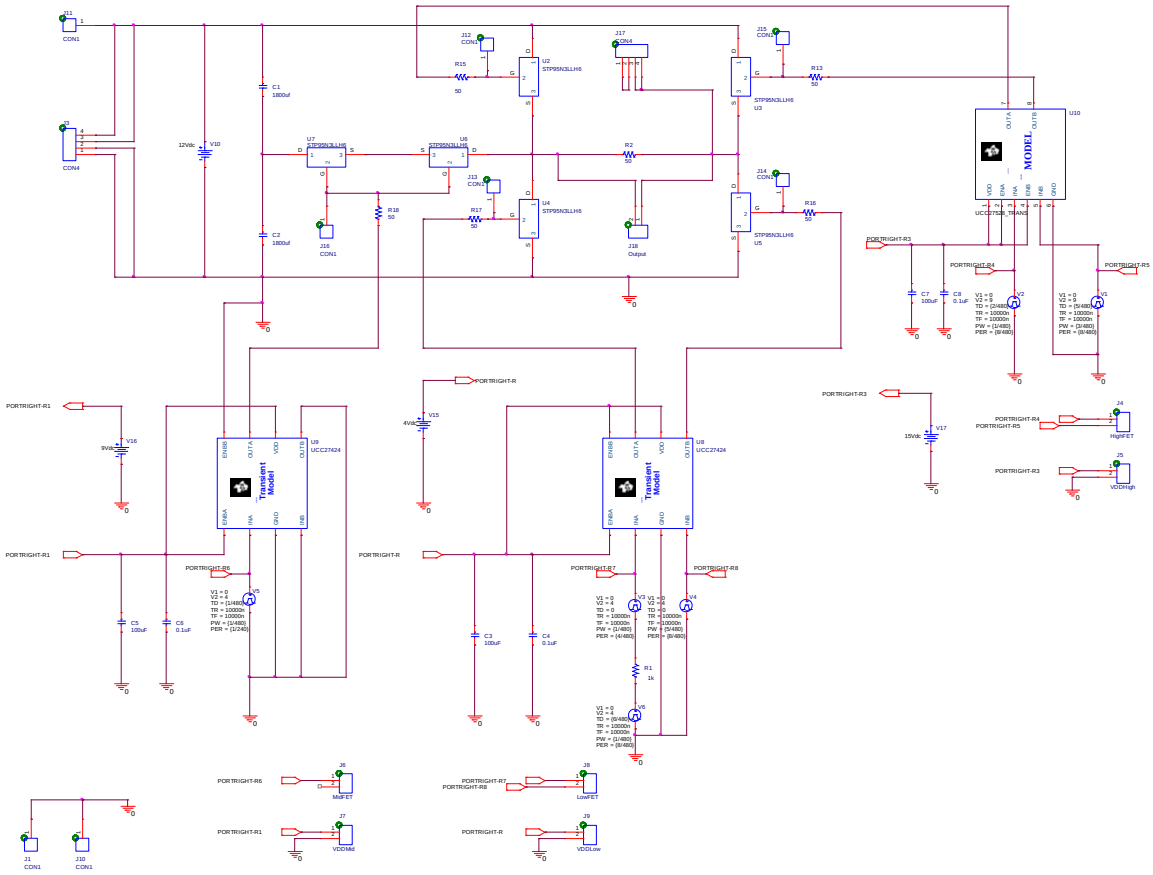


Figure 4-14. Complete circuit.

4.8. Filter Design

A closer look into more detail and progression of how the filter was designed and tested starts with a single capacitor in parallel with the load. This reduced the high frequency noise seen on the five-step inverter output. The capacitor value used largely depends on the cutoff frequency and anticipated operating and switching frequencies.

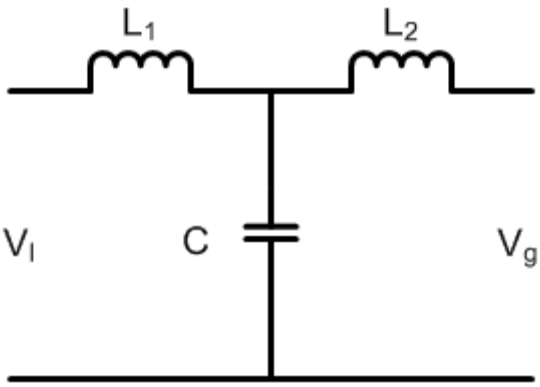


Figure 4-15. LCL filter.

Next, the LCL low pass filter as shown in Figure 4-15 is utilized to obtain a more sinusoidal output voltage waveform. The filter specifications were narrowed down to optimize the filter's effectiveness. Various formulas were used to determine the cutoff frequency depending on the type of filter configuration used [32][33]. Details on what cutoff frequency to use are explained in the article by Kahlane et al. [33]. Another design consideration for the filter is the physical component availability. The parts used for the filter has to consider size and cost limitations. For example, high inductor values with large current ratings are large and extremely expensive. To compensate, increasing the capacitor value directly lowers the inductor requirement.

$$f_c = \frac{1}{2\pi} \times \sqrt{\frac{L_1 + L_2}{L_1 \times L_2 \times C}} \qquad (4\text{-}1)$$

When choosing the resonance point and cutoff frequency, a key rule of thumb is to have the attenuation point be at least half the switching frequency from cutoff. Equation (4-1) was used to determine inductor and capacitor values for the LCL filter. Several frequencies were tested to see the component requirement can be relaxed by operating at a higher frequency.

Table 4-2. Filter Design Values

Component	Value
L_1 (H)	0.0047
L_2 (H)	0.0047
C (F)	0.000144
ω (rad/sec)	1719.04
f_c (Hz)	273.6

One filter design includes a capacitor at the output of the LCL filter for additional reductions. In some circumstances during the prototype build this showed promise and effectiveness. Upon further testing, the later configurations did not see any improvement with the additional output capacitor.

Other adjustments considered include adding a diode to control the direction of current flow to reduce shoot through seen at switching edges. This was more prevalent when using large electrolytic capacitors due to their high impedance causing unwanted loading behaviors especially in AC applications. An attempt was therefore made to use smaller capacitors in place of the electrolytic. With the current value implemented in mind, other smaller values that add up to the current value were researched. Unfortunately, the substitute solution was not practical since numerous high voltage ceramic capacitors would take up too much space.

For sizing the components of the output filter, computer simulation was used to optimally filter out the high frequency noise up to 5A of load. Using only passive components for the filter, maintaining the correct frequency range over a wide load requirement was difficult to achieve. The LCL filter design was iterated and updated several times.

4.9. Simulation Results of Output Filter

The first filter simulation model involves the previously designed LCL filter with L1=L2=4700µH, and C=144µF. The chosen values are selected to eliminate everything greater than the 5th harmonic of the 60Hz fundamental frequency. Initially, the inductor was the largest available inductor at the time. By working within this limitation, the capacitor is adjusted accordingly to obtain the desired result.

Next, a resistive load is chosen to provide a reliable passive fixed load for simulating filter performance. Meanwhile, the LCL filter is arranged in a Wye-Delta configuration to maximize the number of poles and zeroes generated. A simulation was run on the inverter with the LCL filter in question and the result is seen in Figure 4-16 with LCL component values of L1=L2=4700µH, and C=144µF. The results show a heavily attenuated amplitude because of the filter.

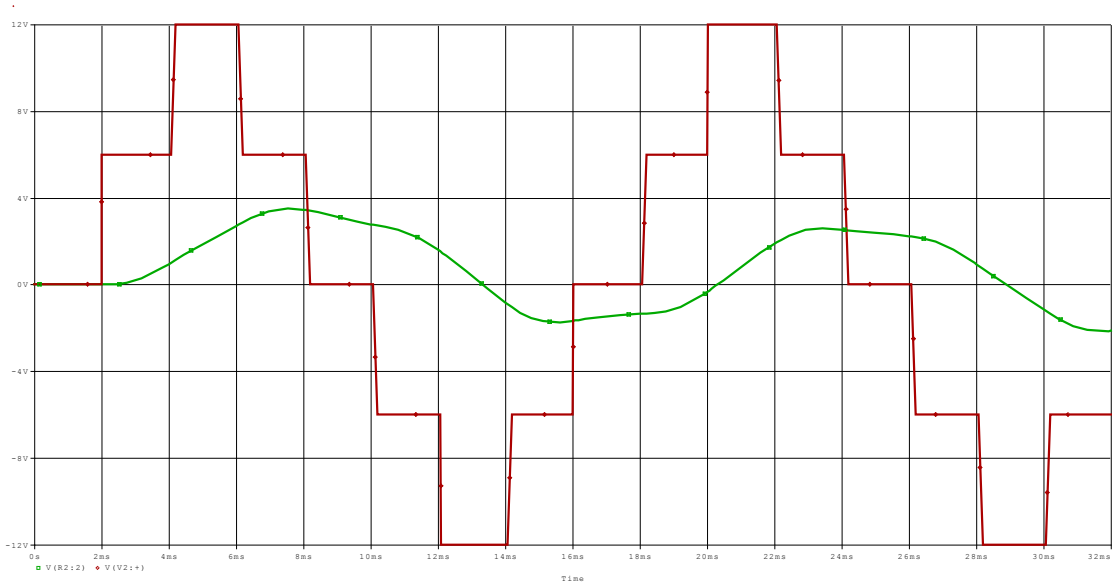


Figure 4-16. Inverter simulation of output voltage before and after LCL Filter.

4.10. Piecewise Simulation of Inverter Output Voltage

Simulating filters involved breaking down the expected output of the five step inverter to a piecewise function to replicate a perfect five-level waveform. For purposes

of focusing on the filter design, which is the main source of design challenges, the multilevel unfiltered signal will be hard coded and fully ideal. The arbitrary waveform will be accurate and meet specifications of a five step multilevel signal with 60Hz main frequency. A piecewise function source is used to generate the unfiltered output signal shown in Figure 4-17.

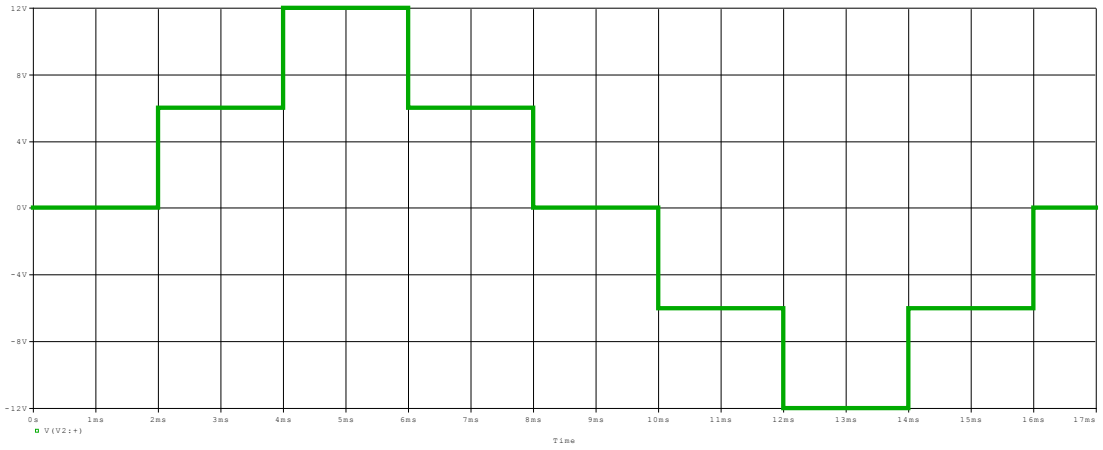


Figure 4-17. Piecewise function of output voltage.

By using the piecewise waveform as the input to the LCL filter, adjustments were made to the filter to improve the filtered output voltage waveform. Secondly, the filter solutions previously outlined were tested as well using the perfect five step output. Alternative solutions discovered though the filter design process were also simulated in this way.

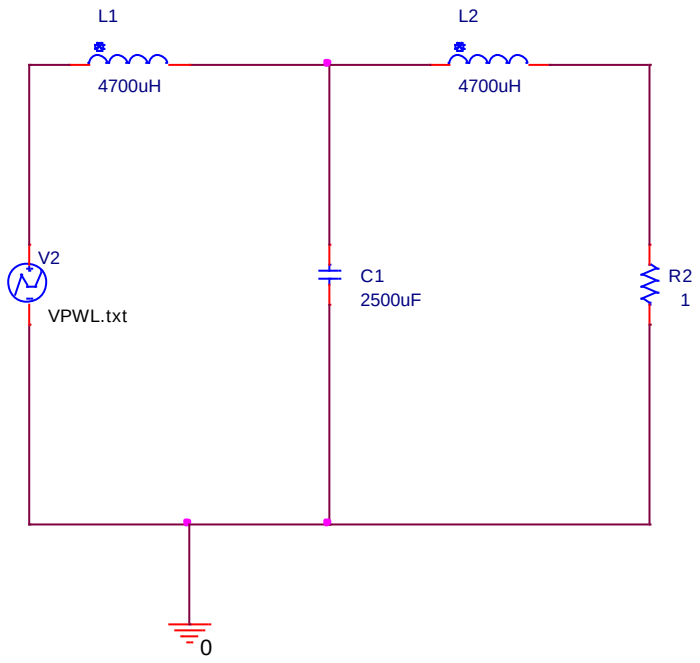


Figure 4-18. Updated LCL filter circuit with ideal multilevel input source.

The LCL filter (L1=L2=4700µH and C=144µF) is updated by increasing C to 2500µF in Figure 4-18, thus lowering the cutoff frequency to 65Hz and increasing the output amplitude. The output takes time to reach steady state but eventually settles to a sinusoidal waveform as seen in Figure 4-19. Unfortunately, a 2500µF capacitor will most likely require a polarized capacitor, which is not suitable for AC outputs.

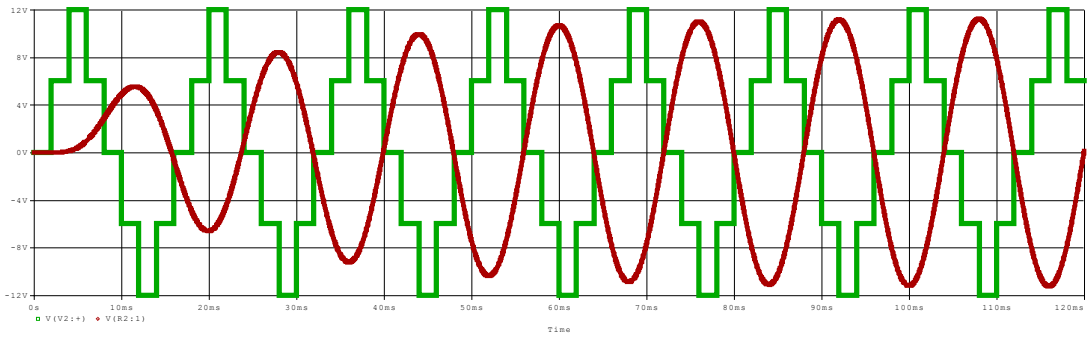


Figure 4-19. LCL filtered output [green] of ideal multilevel inverter waveform [red].

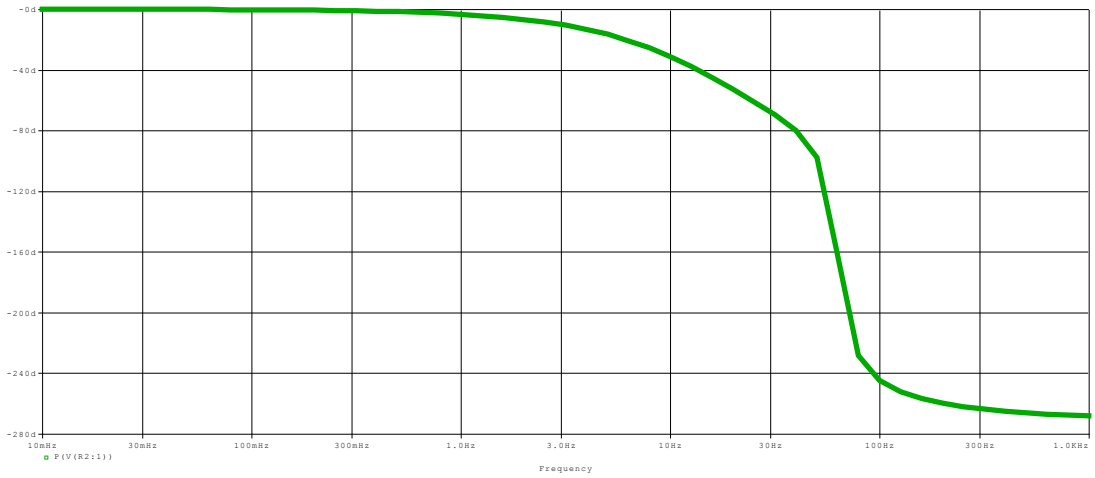


Figure 4-20. Phase Response of the LCL filtered output.

The filtered output waveform has a phase shift from the input waveform as depicted in Figure 4-19. The transfer function of the filter only has poles so the output waveform is shifted right relative to the input. A frequency response was run on the filter circuit to understand the phase shift better. The resulting phase response is shown in Figure 4-20 confirms a -148 degrees shift at the 60Hz main frequency.

To quantify the quality of the output, the total harmonic distortion (THD) of each waveform is simulated in PSPICE. Starting with the square wave output as a baseline, the total harmonic distortion was 39%. While the modified square wave, which has an intermediate step at zero volts between the positive and negative peak, has a 37% THD. As expected, the square wave based outputs have fairly poor total harmonic distortion. In the five step multilevel output however, the distortion value improves upon the square wave with an 18% total harmonic distortion, thus confirming the effectiveness of adding more steps. Furthermore, the filtered response shown in Figure 4-18 lowers the total harmonic distortion all the way to 7%. The THD of each output type is summarized in Table 4-2.

Table 4-3. Total Harmonic Distortion Summary

Square Wave	39%
Modified Square Wave	37%
Five Step Multilevel Output	18%
Post Filter Output	7%

To further explore more design options, the load and filter values are adjusted to see how the output responds. The first filter design variation with a cutoff frequency of 143Hz aims to remove 180Hz harmonic but retains 60Hz and 120Hz harmonic content. The corresponding LCL filter circuit is shown in Figure 5-32. The filtered 5 ohm output in Figure 4-20 shows an attenuated but constant voltage output.

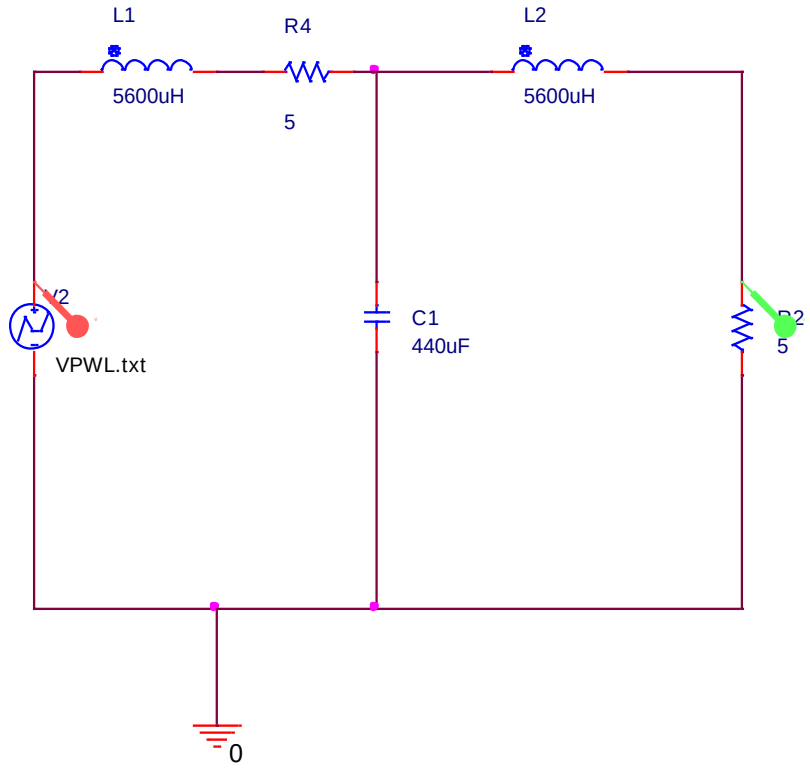


Figure 4-21. Filter testing circuit.

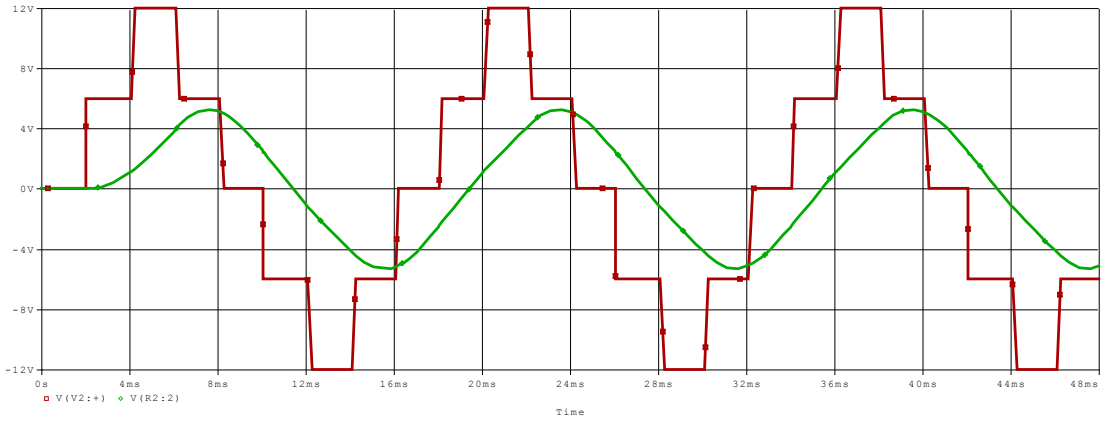


Figure 4-22. Source [red] and filtered output [green] of circuit in 4-21.

Due to the high cost and complexity of building or purchasing a large high current inductor, a test to increase the capacitor value instead was run. Unfortunately, this is not suitable as large capacitors are often polarized as previously mentioned. Assuming a bipolar capacitor, the filtered output amplitude is further reduced in this filter configuration as seen in Figure 4-24.

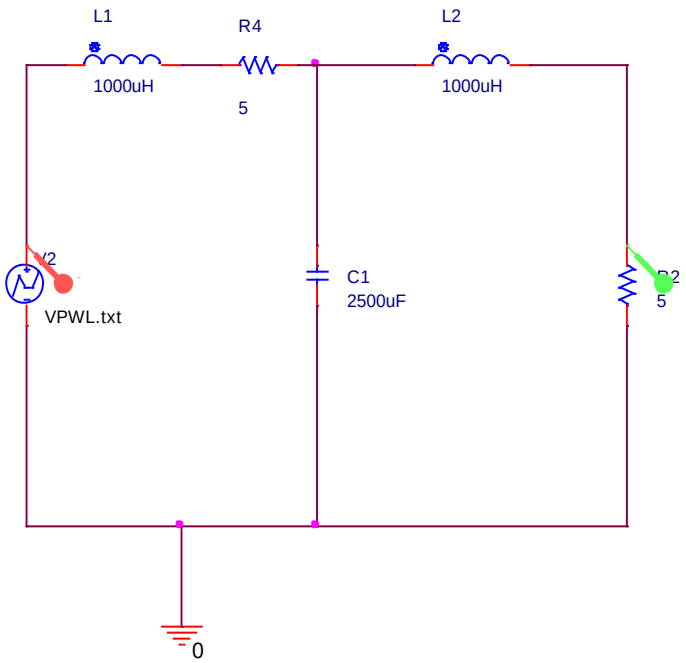


Figure 4-23. Filter with increased C and smaller L test circuit.

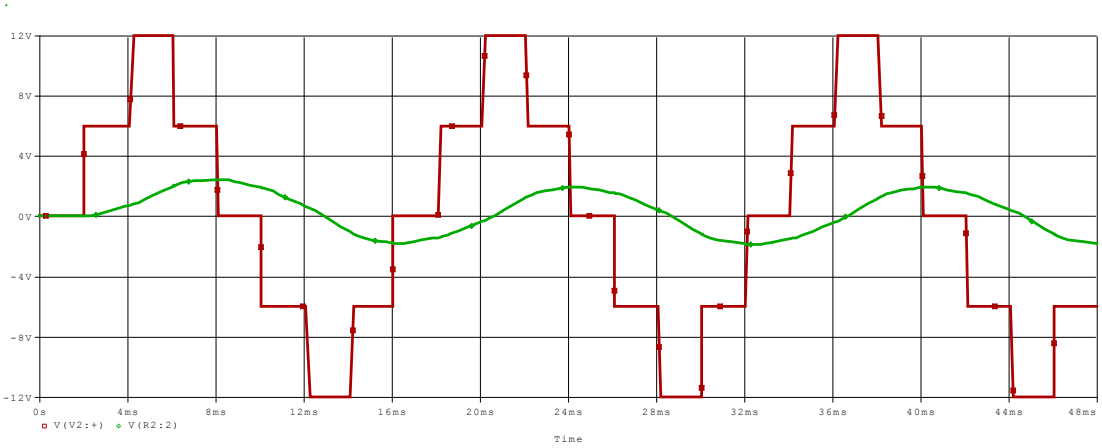


Figure 4-24. Source [red] and filtered output [green] of circuit in 4-23.

The opposite circuit configuration is simulated by increasing the inductor value and reducing the capacitor below the first design. This experiment is to see if high inductor values also impacts the output waveform like the capacitor does. The results show little change from the original design in Figure 4-22 to the one seen in Figure 4-26. The current waveform is added to Figure 4-27 to document and verify the current capacity required by the inductors.

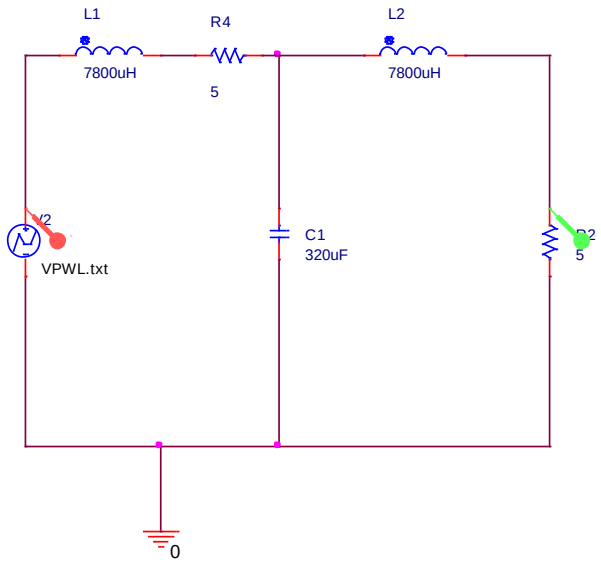


Figure 4-25. Filter with new cutoff frequency test circuit.

Table 4-4. Filter Design Calculations

Component	Value
L_1 (H)	0.0078
L_2 (H)	0.0078
C_1 (F)	0.00032
ω (rad/sec)	895.14
f_c (Hz)	142.4

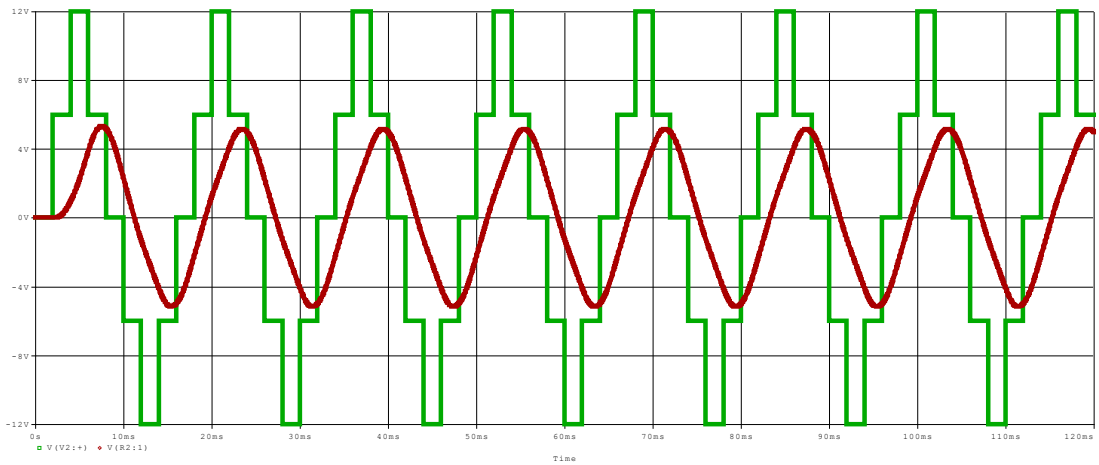


Figure 4-26. Source [green] and filtered output [red] of circuit in 4-25.

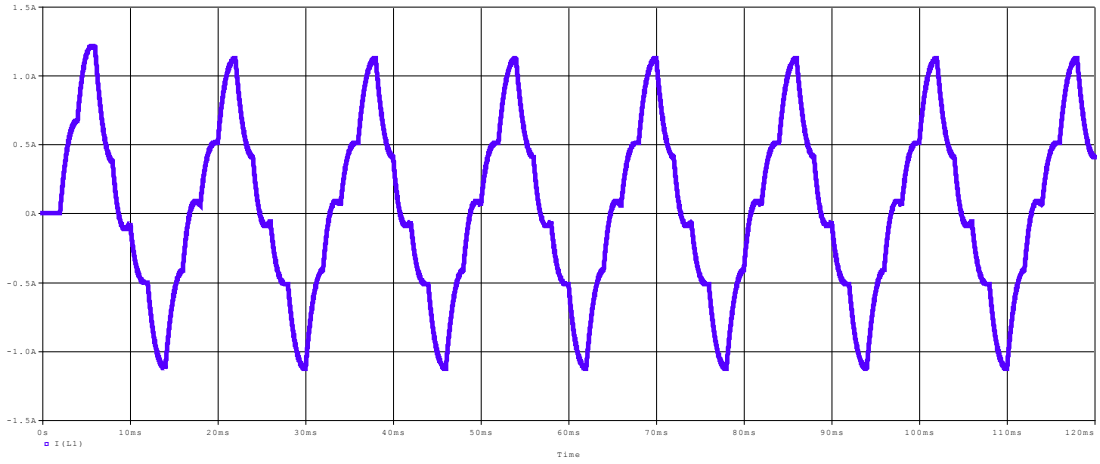


Figure 4-27. Current waveform of inductor L1 in 4-25.

Results show a wide range of variables that influence the filtered output waveform. Even starting with an ideal multilevel output from the inverter, the filter design proves difficult to solve. The load present on the output directly impacts how the filtered output looks because of the limitations of a passive filter.

Chapter 5. Hardware Design and Testing

5.1. Hardware Component Verification

The initial steps taken with simulation mirrored the process used for the hardware prototype. After receiving parts, each part was individually tested for characterization. The parts tested include through-hole pin version of the UCC27424 driver, along with the STP95N3LLH6 MOSFETs. By avoiding the microcontroller generated control signals for simplicity and isolated testing, signals were arbitrarily generated on a function generator to test the driver and MOSFETs.

The first hardware test involves testing the driver. Based on the data sheet, the logic high input threshold for the driver is 2V. The driver input has a 2.7V high voltage seen in green in Figure 5-1. The input signal is applied to a UC27524 driver with Vdd supply voltage set to 5.6V. The driver output shown as the top signal in Figure 5-1 has a high voltage (VOH) = Vdd and low voltage (VOL) = 0V. In this case, the driver works as expected.

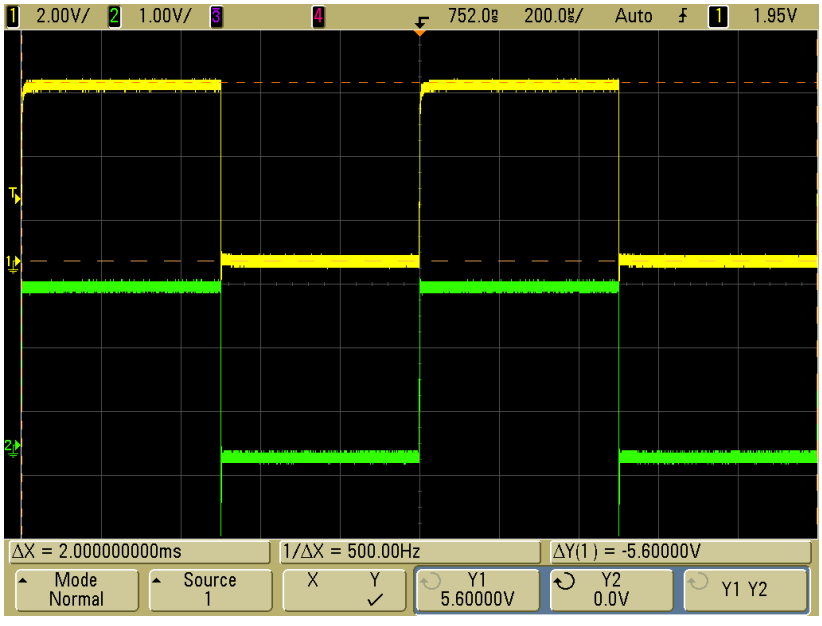


Figure 5-1. MOSFET driver testing with driver output (top) and driver input (bottom).

Each of the microcontroller generated switching signals was measured on the scope to verify the timing and voltage levels. Output levels match those set by the Atmel Stuido software, and waveforms also match those observed in simulations.

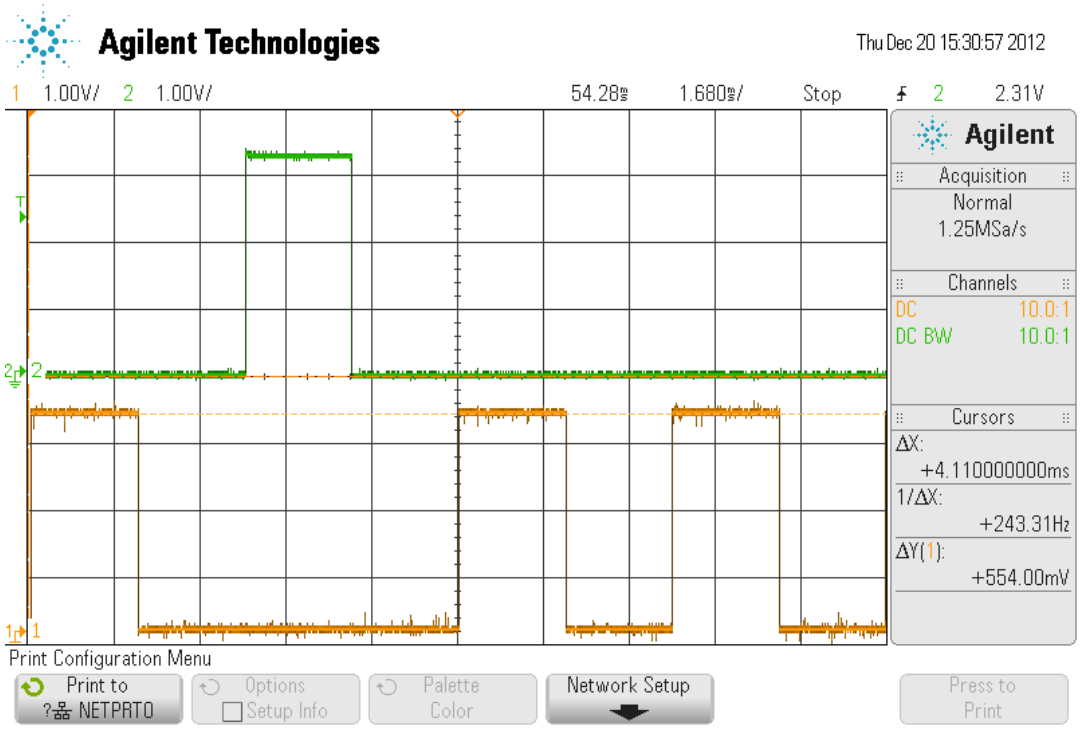


Figure 5-2. Microcontroller switching waveforms for switches 2 (green) and 3 (yellow).

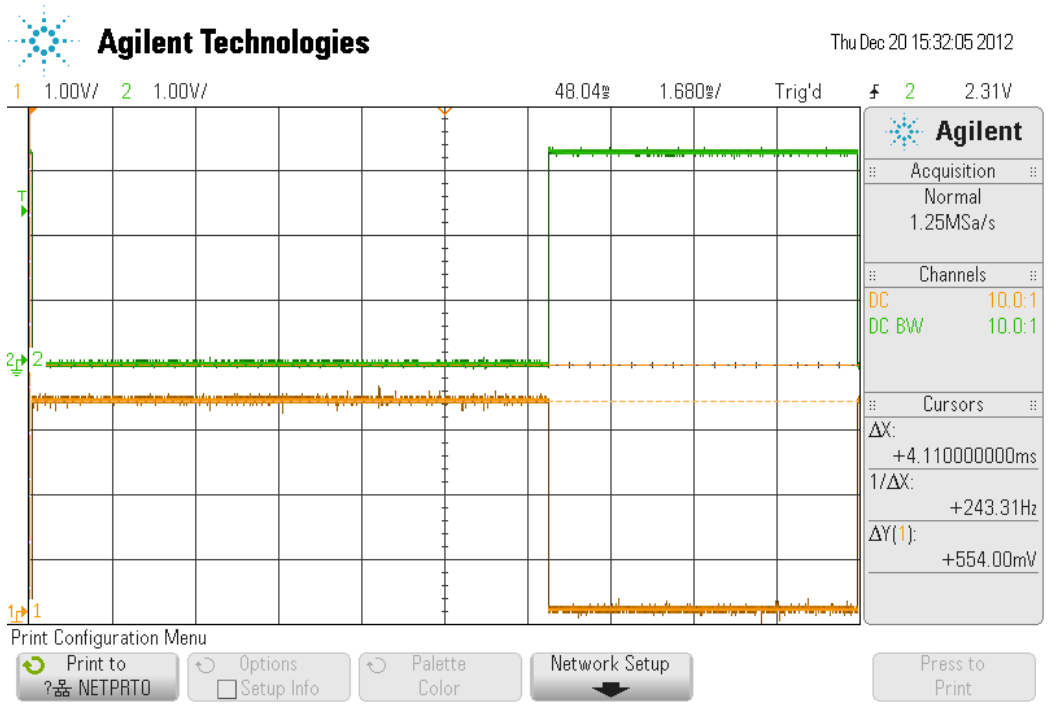


Figure 5-3. Microcontroller switching waveforms for switches 1 (green) and 4 (yellow).

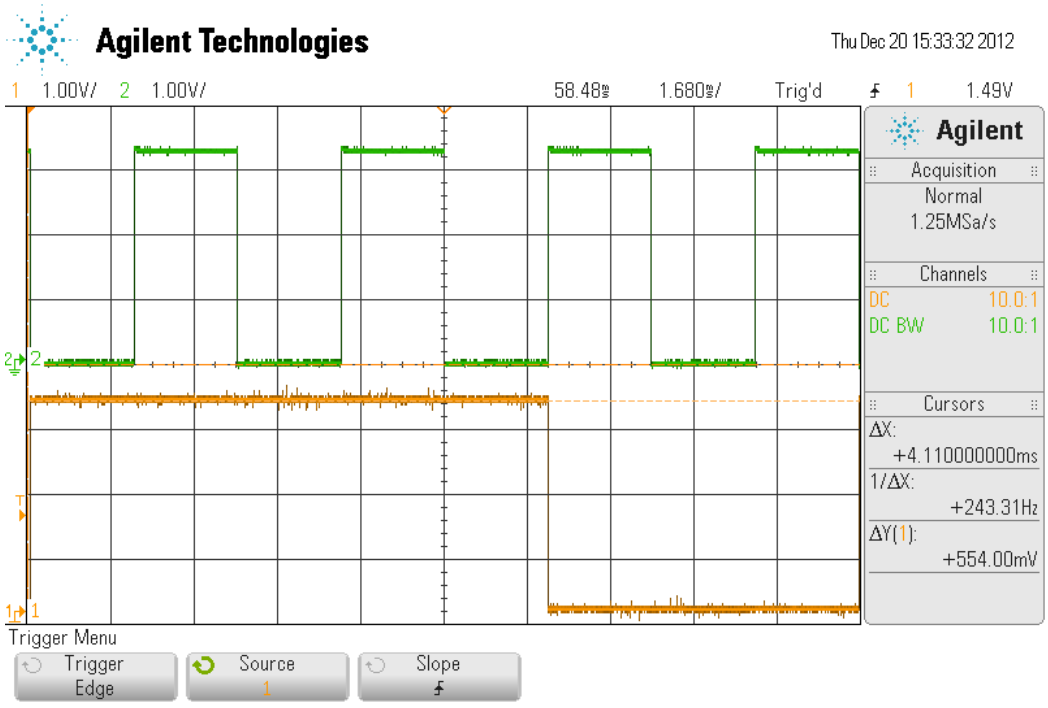


Figure 5-4. Microcontroller switching waveforms for switches 4 (yellow) and 5 (green).

Next, the driver is separately tested by applying the microcontroller generated signals. In Figure 5-5, the output signal in green shows noise on the output high. Measurements show the voltage levels of both the input and output of the driver are similar due to the Vdd used for the driver. Zoomed in captures of the edge show some overshoot and oscillation after transitioning to the high level. A 0.1uF capacitor was applied to the driver output to smooth it out. As seen in Figures 5-8 and 5-9, the output high is clean. As a side effect, the rise time of the clean signal in Figure 5-11 is slightly slower due to the charging of the capacitor.

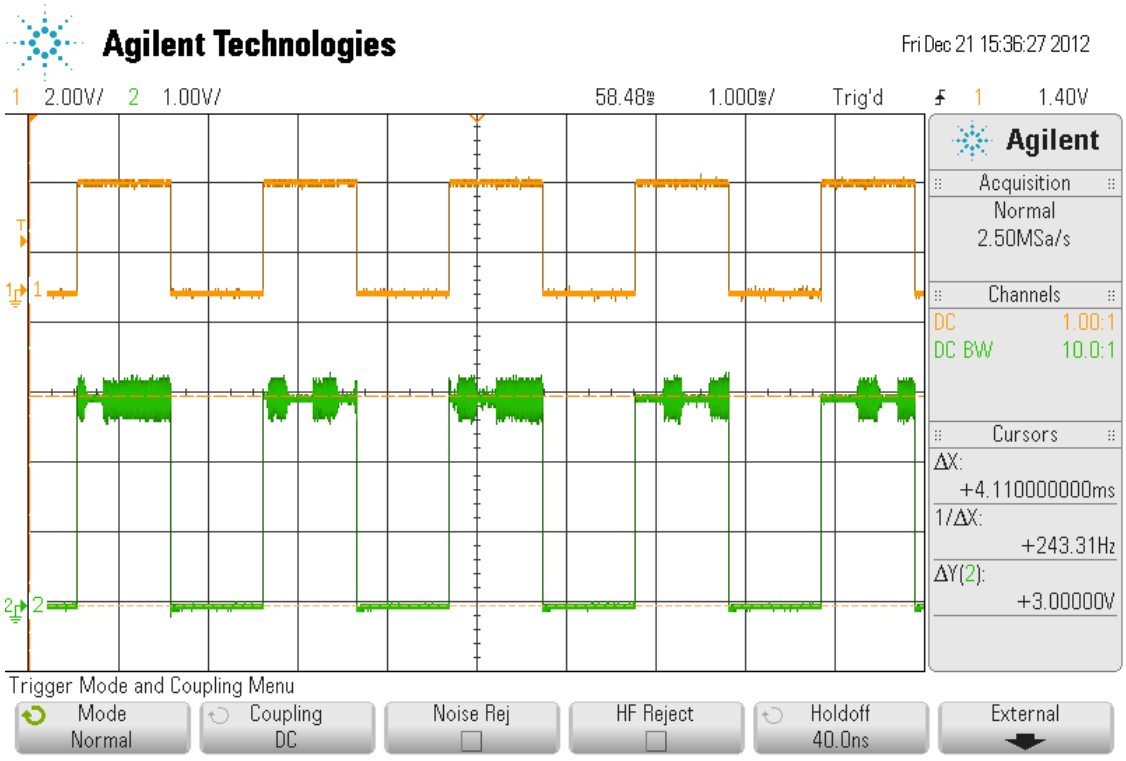


Figure 5-5. Measuring the driver output amplitude of switch 5 with driver input (yellow) and output (green).

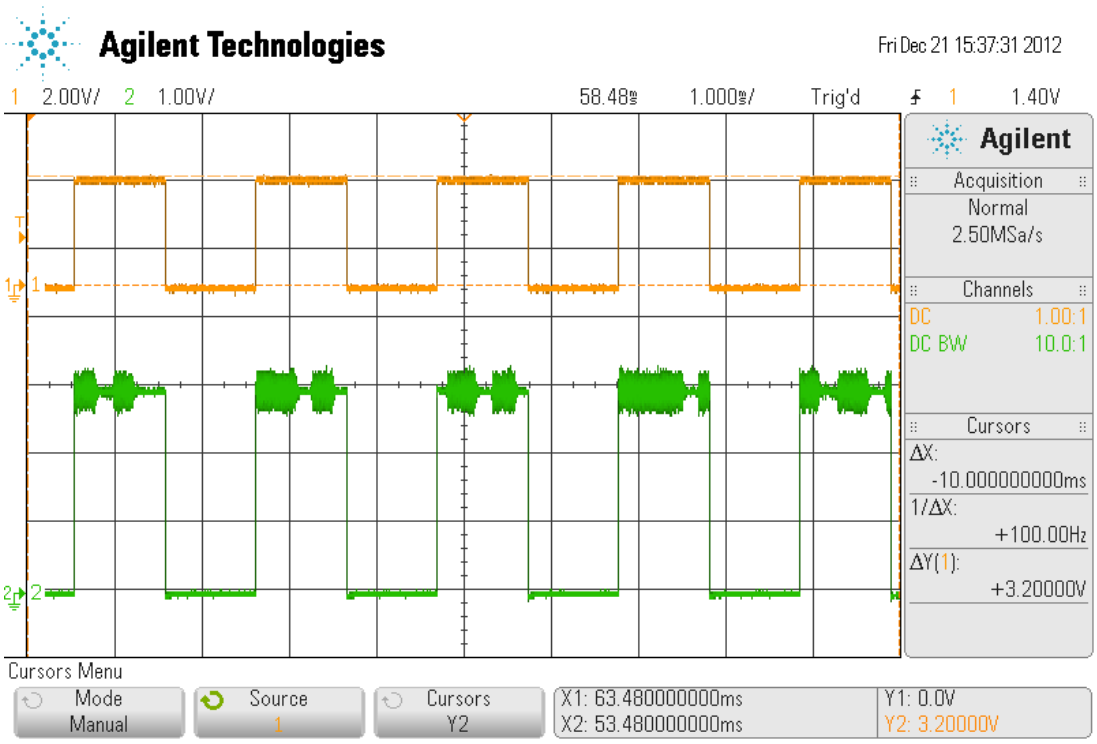


Figure 5-6. Measuring the control signal amplitude of switch 5 with driver input (yellow) and output (green).

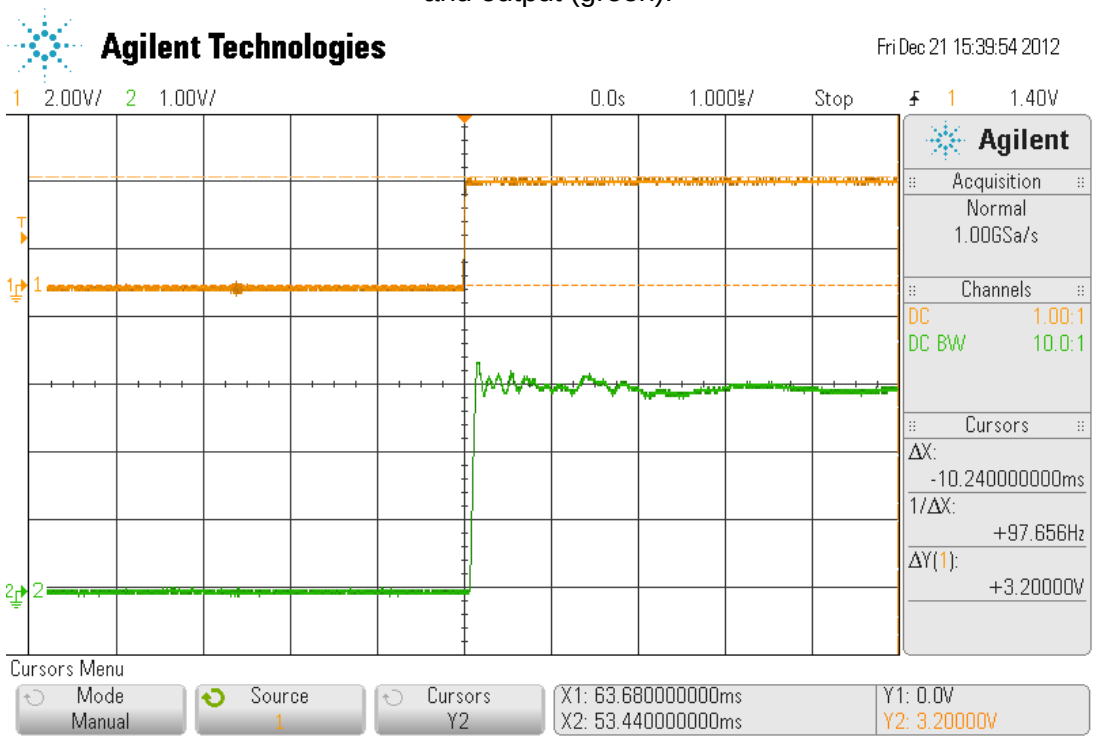


Figure 5-7. Microcontroller and driver output edge waveform of switch 5 with driver input (yellow) and output (green).

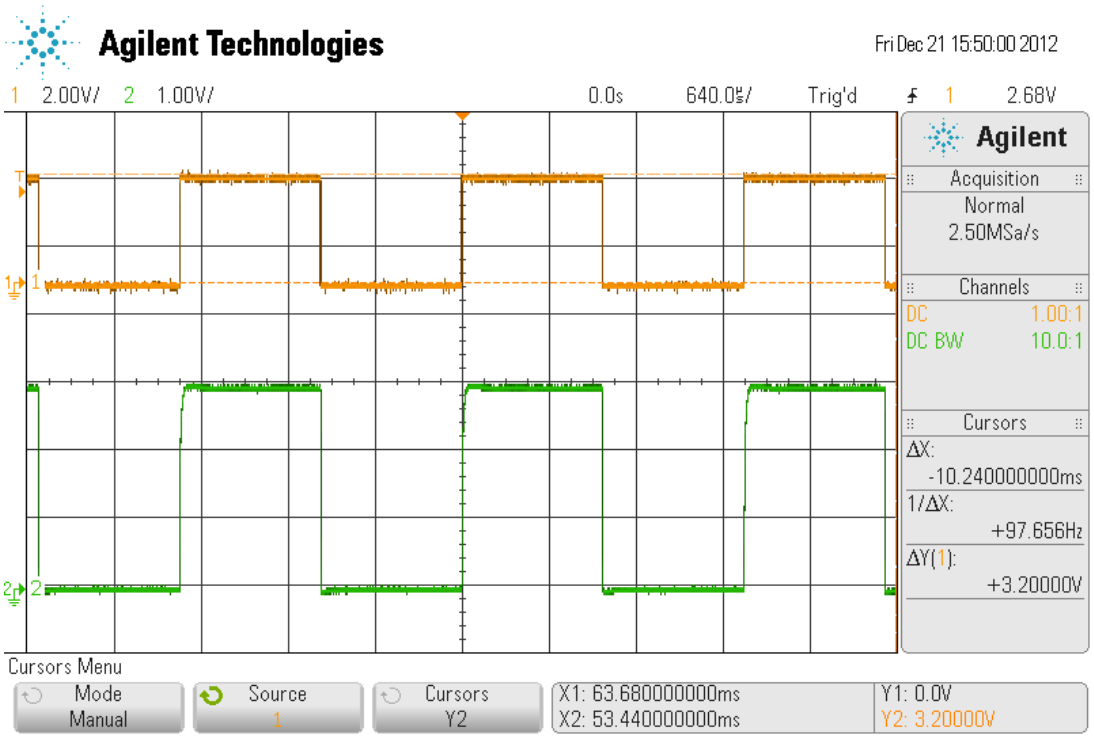


Figure 5-8. Improved control signal to driver measurement of switch 5 with driver input (yellow) and output (green).

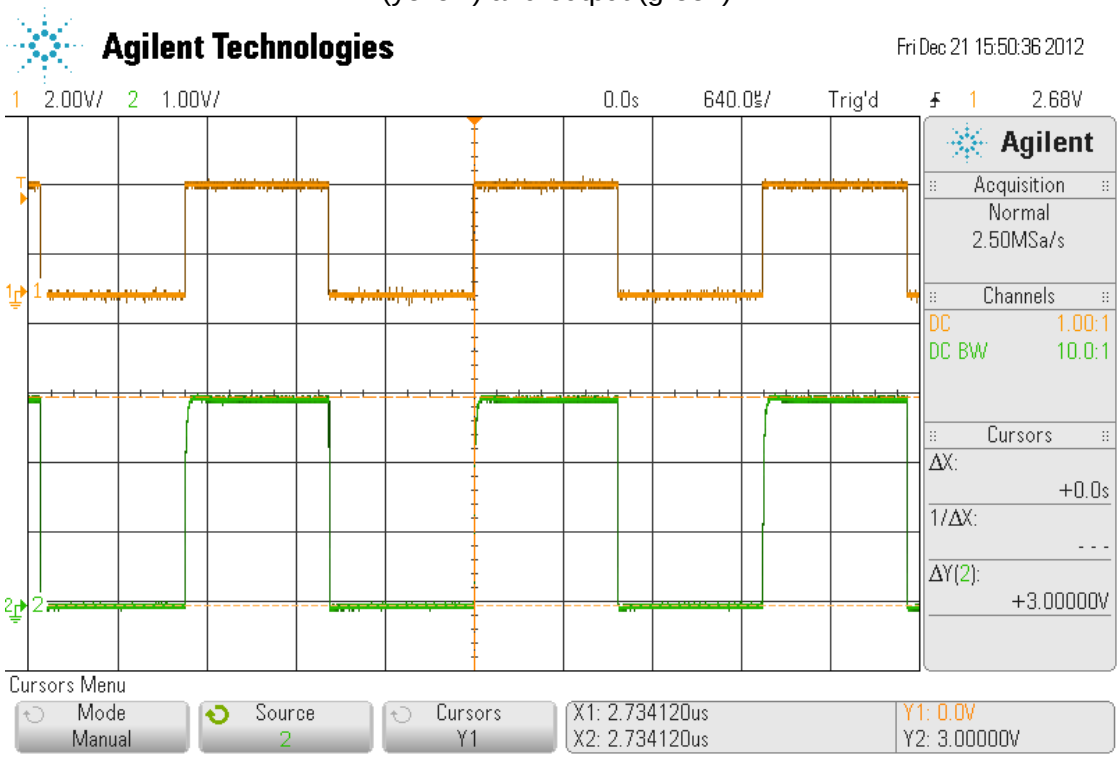


Figure 5-9. Clean driver output amplitude measurement of switch 5 with driver input (yellow) and output (green).

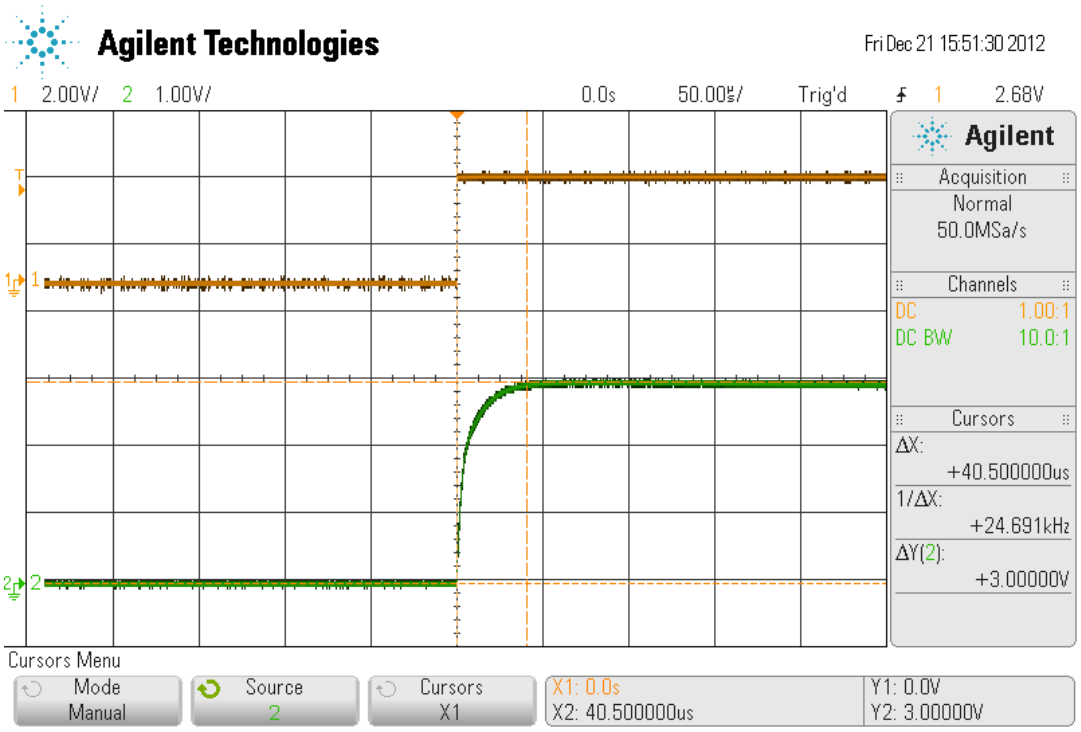


Figure 5-10. Measure amplitude of driver edge waveform of switch 5 with driver input (yellow) and output (green).

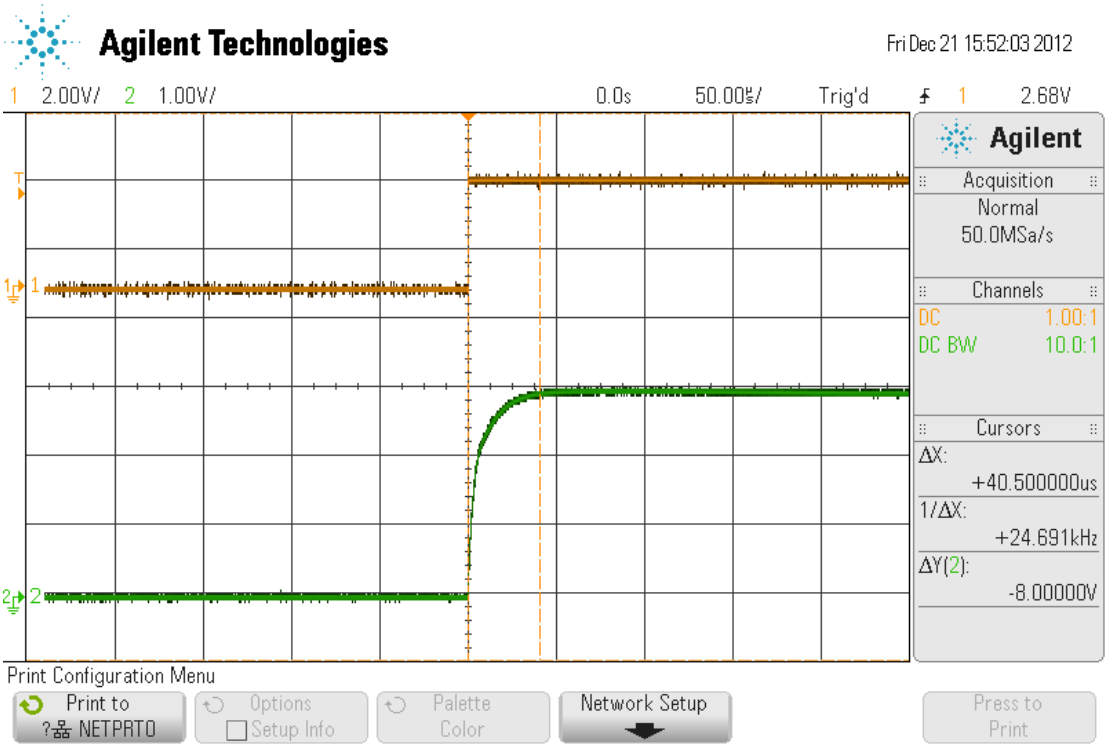


Figure 5-11. Capture driver output edge rise time of switch 5 with driver input (yellow) and output (green).

The threshold levels were recorded and verified on the oscilloscope. Knowing the logic highs on the driver and the different outputs and supplies needed were the first step in fully understanding and meeting expectations.

5.2. Digital Design

To kick off the hardware design, microcontroller programming was constructed to generate the switching control signals as seen in Figure 5-12. Research into available hardware options for control sought a flexible tool for the unique switching scheme to be implemented. Considering the custom signal needed, a microcontroller based digital solution offered the most promise toward the desired signal. Equipment that was readily available was also taken into consideration. Between Microchip and Atmel, the Atmel ATMega256 was available, and thus chosen for this project. In addition, the ATMega256 had a long list of features that were promising for the project requirements.

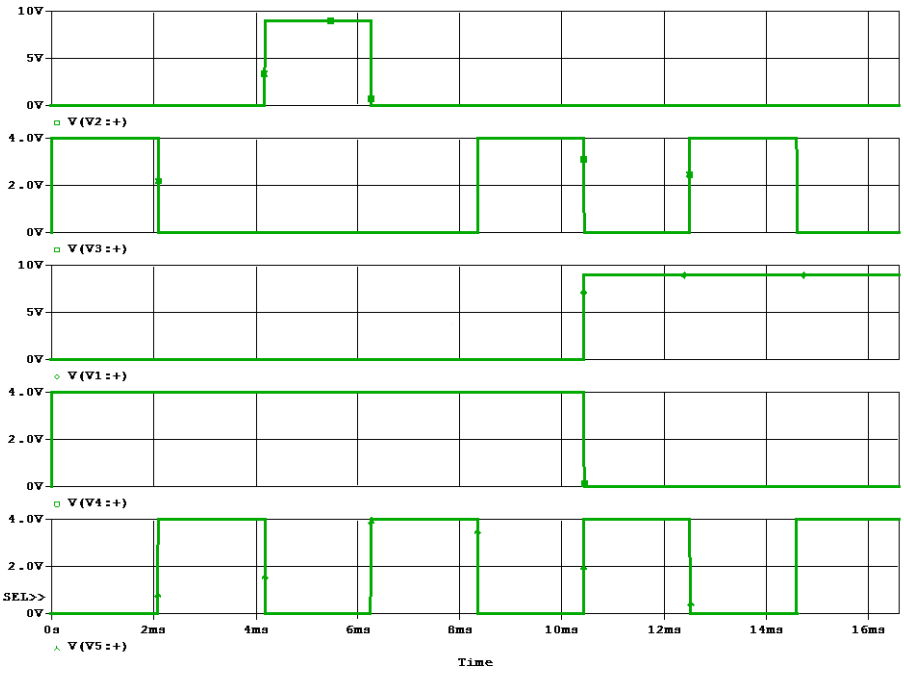


Figure 5-12. Switching control signals.

Beginning development focused on using the PWM module to generate switching signals of varying length. The implementation plan involved starting and stopping the several PWM modules and routing the outputs to use for one switching signal and when off use it for a different signal. The goal was to combine multiple PWM module outputs with varying frequency and delays to generate the five switching sequences needed. Routing a single output to two or more signals was a complex timing situation. Since the PWM modules were set based on a certain frequency and duty cycle it was not very flexible. After considering various outputs and even using a digital inverter for some signals, the PWM module was ruled out.

Next, an alternative solution using the microcontroller was further researched. The GPIO ports allowed for either output high or output low. By applying a delay during an output high or low, the signal or pulse can last the desired length. Applying this logic to all five signals, any pattern can be generated for the five switches. Two different methods were initially used to code the output. At first, the method of controlling each individual bit was used before switching to controlling the ports, which contain 8 bits each, as a whole that is currently implemented.

Each of these outputs used for the switching signals are checked individually and then all together to verify proper timing on the oscilloscope. Initially, as mentioned before, there was massive overlap between all the signals. To fix this, an additional state was created between pulses to prevent overlap. In this state, one signal is shut down while the other transitions to their next state. By using this sequence, at no time are both on.

Following the completion of the switching signal generation, focus was put on the microcontroller and driver interface. The output from the microcontroller was 1.8V when high. This voltage level meets the requirements of the driver logic input. From this logic input, the higher Vdd voltage fed into the driver will be used and the Vdd voltage will

output to the gate of the FETs. With a properly biased 8-pin driver, the driver operation was next tested. The output from the driver was checked against the output from the microcontroller. The two signals properly matched up; thus, yielding a successful microcontroller to driver pairing.

The programming on the ATMega256 was done in C on Atmel Studio. Once the code was finished, the firmware is flashed to the microcontroller through the Atmel Studio IDE. There is an option to adjust the output voltage levels through the software if the driver requires higher logic high threshold.

5.3 Hardware Prototype

In the first iteration of the hardware, a large breadboard was used to build and integrate the entire design on a single board. This included the drivers and FETS with thru-hole package types to fit on the board. Although breadboards are flexible and great for prototyping, many issues were encountered. First, there were times where connections between pins were not secure or a pin was damaged and not making contact. Secondly, using jumper wires crisscrossing throughout the circuit with connection points not labeled can lead to mistakes. In order to debug issues of this kind, it was necessary to reexamine point by point to find the problem area. Many times the problems discovered was due to improper grounding at some points that led to floating levels on the multilevel output. While other times issues came from a missing connection from some point in the circuit. The prototype design can be seen in Figure 5-13.

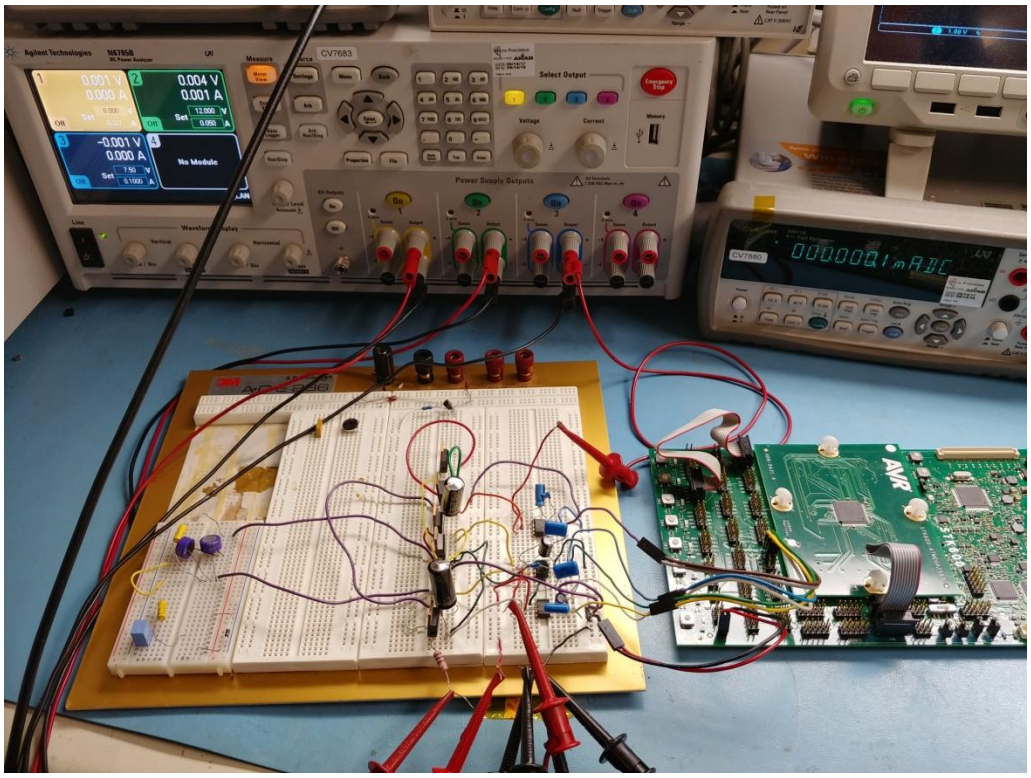


Figure 5-13. Working prototype design.

While testing the design on the breadboard, a few changes were made to improve it. Initially, the output did not have a load and was just shorted. A current limiting resistor for the input was needed to compensate for the high output currents caused by the shorted output. In hindsight, shorting the load was an obvious problem and output would not properly show up due to it. A load was needed to bias the FETs and capacitor to generate the multiple levels needed from the design. Now with the working load, initial measurements were made on the completed working design including the levels of load that it can support.

5.3.1. Prototype Issues

The prototype had many issues including noise due to the drivers and the parasitic inductances present from using breadboard and jumper wires. Making

connections between the digital interface, drivers, switches, and then the load can create many challenges and issues when done on a breadboard. One of those issues was keeping connections in the right place often turned into a puzzle with the number of connection points side by side. This was one case that can be made for upgrading to a PCB design. Although using a breadboard on one hand contributed parasitic capacitance and inductances and lacked organization, it offered immense flexibility in updating the design. A long process was undertaken to work through the issues and end up on the final design. For example, one of those issues was the proper location of the load and measurement points as critical in seeing the AC sinusoid on the output.

Testing the interaction between two switches was also done to look for any potential problems. The point at which switching occurs is susceptible to overlapping voltage and current during the transition. The overlap shows as spikes on the output waveform. To reduce this, dead time in the code was implemented to remove the overlap.

Initial testing of the prototype model resulted in the waveforms pictured in Figure 5-14. Output on the positive side of the load in yellow appears to be the expected waveform. Unfortunately, the green signal is not accurate thus resulting in the incorrect inverter output seen in red. The initial output results show further refinement and work is needed create the proper multilevel inverter output. One source of error is the FET biasing because improper biasing at switches can cause incorrect voltage levels and patterns on the output.

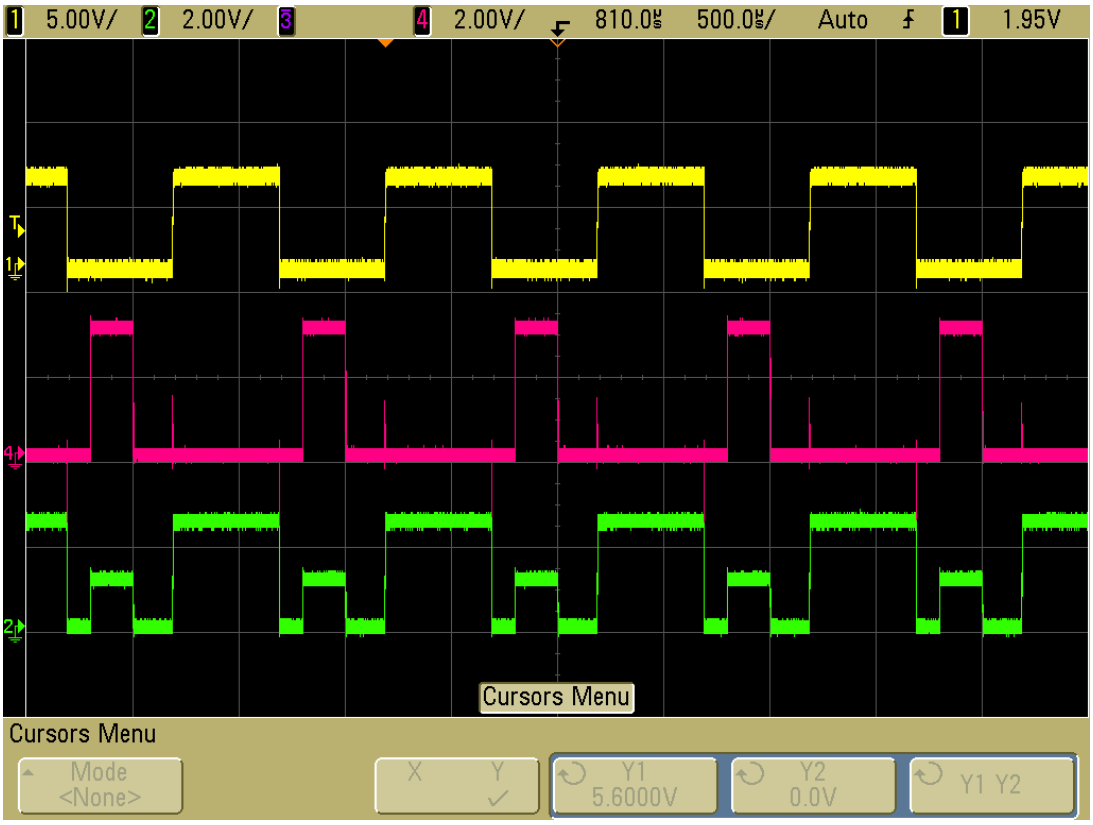


Figure 5-14. Output from original prototype inverter (red) with positive node (yellow) and negative node (green)

5.3.2. FET Biasing

In order to get the correct voltage levels on each of the output steps, the first step was to get the highest voltage step to 12V. Getting the output to 12V was a challenge because initially output was limited to 2V. The voltage levels for each driver had to be updated to pass 12V to the output. This was where a systematic process was used to check each driver output voltage and follow it through all the way to the inverter output. The goal was to provide the proper bias to each FET to pass 12V to the inverter output. Specifically speaking, each FET required a different voltage depending on the expected voltage level passing through it. In the end, the high side required 12V bias, mid FETs 7.5V bias and low side 4V to the gate.

5.3.3. Prototype Test Results

In Figure 5-15, the unfiltered output from the prototype circuit is shown. The output is with no load and properly generates 5 steps through the multilevel inverter.

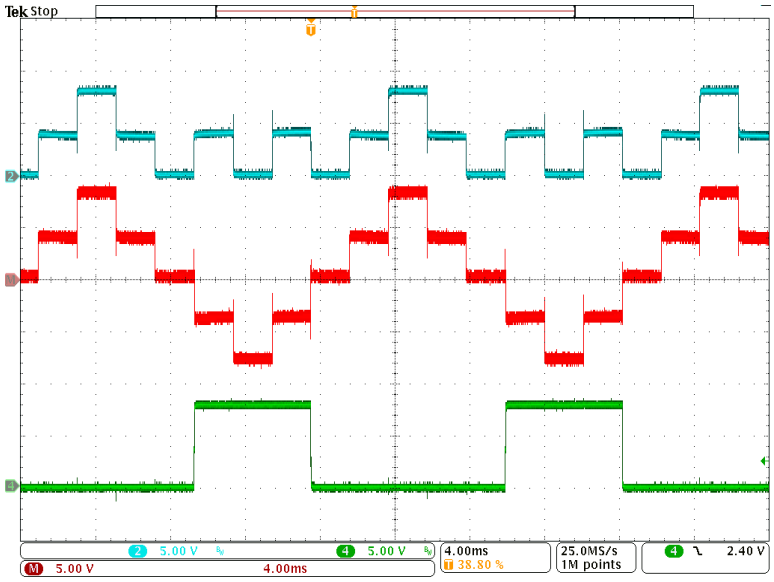


Figure 5-15. Prototype circuit no load unfiltered output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (green).

Figure 5-16 shows the filtered output from the inverter with no load. The waveform has proper AC sinusodal characteristics with 5Vpp amplitude.There is some shoot through from the switching that is not filtered out completely.

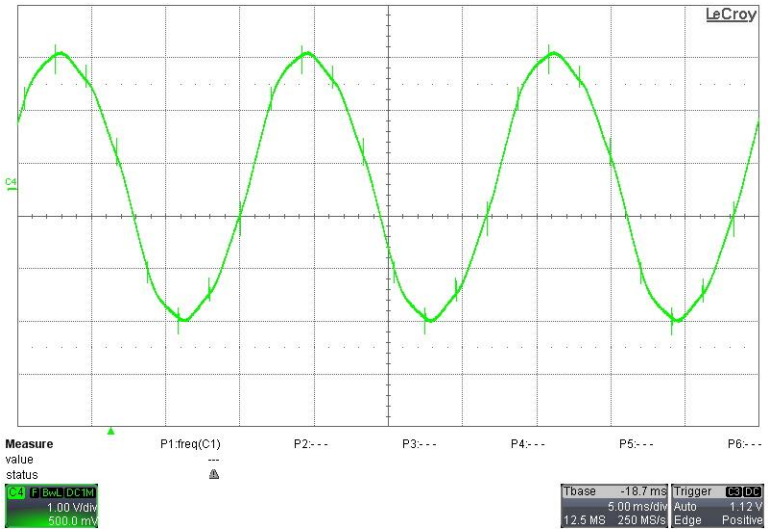


Figure 5-16. Prototype circuit no load filtered output.

By reducing the resolution of the captured waveform, a cleaner signal can be seen. This version in Figure 5-17 has less samples per second thus skipping over the high frequency noise coming from the switching edges. Although at no load, the waveform shows a properly filtered output and at least visually shows good Total Harmonic Distortion (THD) and AC output.

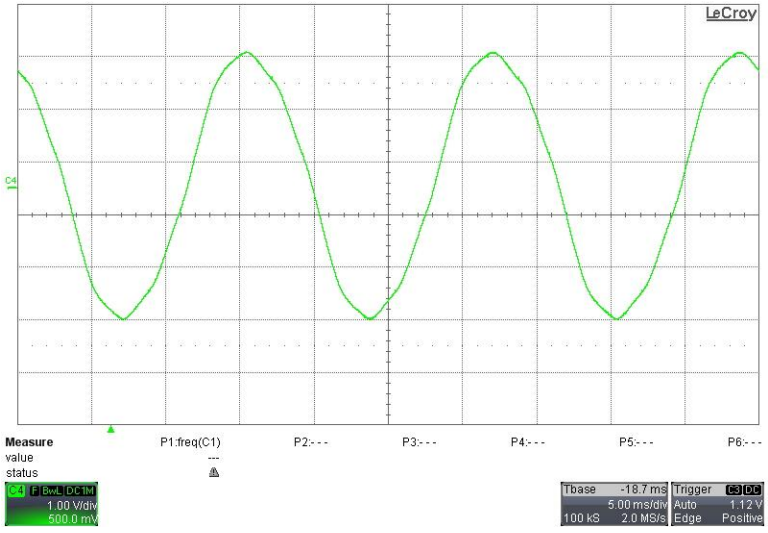


Figure 5-17. Prototype circuit no load filtered output [lower resolution].

To quantify the quality of the inverter output, the THD is a critical parameter to measure. The harmonics refer to the frequency components of the main signal that are integral multiples of the main frequency, while the distortion refers to the noise caused by the harmonics. For example, when looking at a square wave, it is far from single frequency sinusoidal waveform, and so the square wave has harmonic distortion [34]. The THD represents the ratio of RMS voltage of all harmonic frequencies over the RMS voltage of the fundamental. The closer the THD to zero, the more sinusoidal and higher quality of ac output the inverter has. The equation to calculate THD from [34] is:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_rms}^2}}{V_{fund\ \_rms}} \quad (5\text{-}1)$$

V_{n_rms} is the RMS voltage of the nth harmonic
V_{fund_rms} is the RMS voltage of the fundamental frequency

A FFT measurement is applied to the non filtered output to determine the baseline THD. Figure 5-18 shows the unfiltered signal in green with numerous cycles shown due to the large time division scale. By doing this, the FFT measurement has more samples to calculate the voltage of each harmonic shown in yellow.

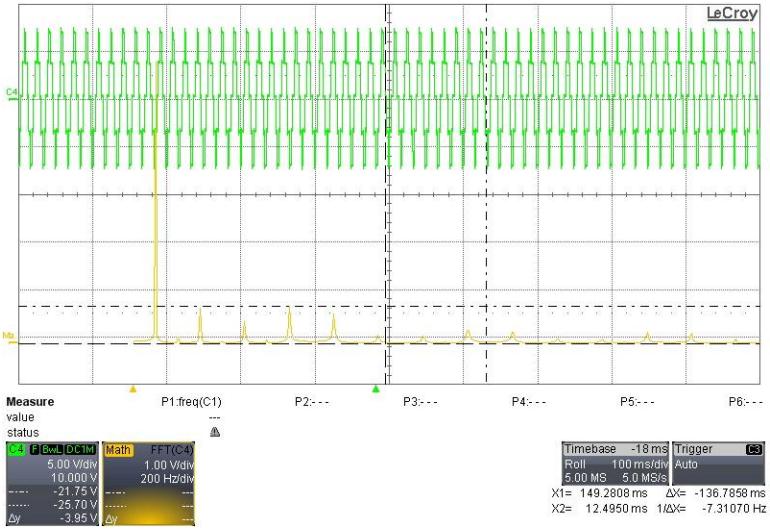


Figure 5-18. FFT measurement of unfiltered output with unfiltered signal (green) and FFT (yellow)

Next, the time base is increased further to include even more samples for the FFT. The results shown in Figure 5-19 have distinct peaks at the harmonic points that can be easily measured. For example at 180 Hz, the amplitude is 568 mV. By measuring the amplitude of each peak at the harmonic frequencies, the calculated total harmonic distortion is 28% for the unfiltered no load output.

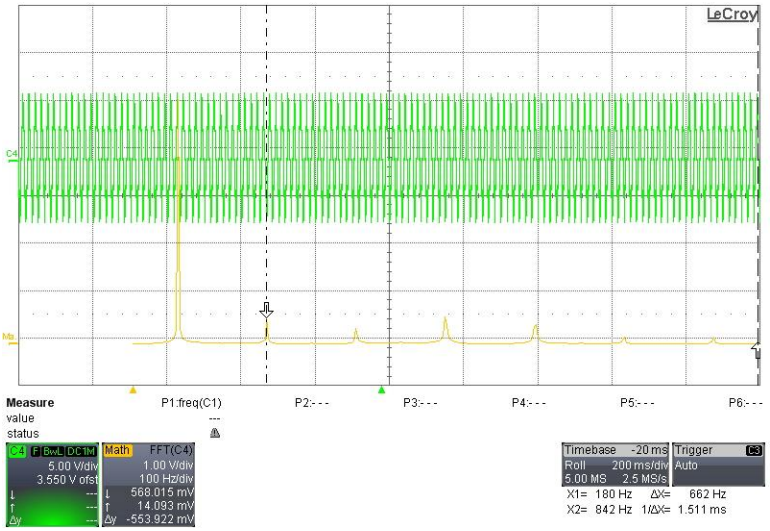


Figure 5-19. FFT Measurement Amplitude at 180Hz with unfiltered signal (green) and FFT (yellow)

An FFT measurement is similarly applied to the filtered no load output shown in Figure 5-20. This waveform also has a large number of samples in order to measure the amplitude of each harmonic. The calculated THD for the filtered output is much lower at 11% compared to 28% for the unfiltered output.

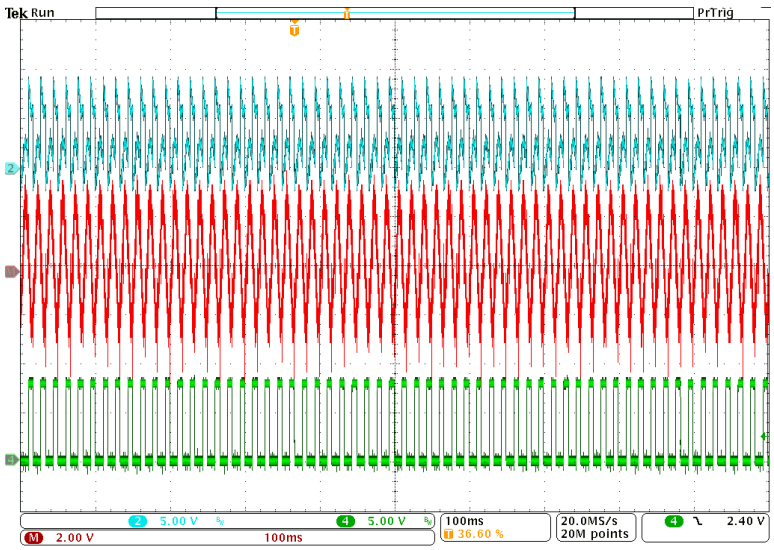


Figure 5-20. Prototype circuit no load filtered output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (green).

5.4. PCB Design

Starting from a completed schematic, the design was imported into the PCB editor to netlist. The parts library was then created with proper dimensions obtained from datasheets and documentation. Each part was carefully created to ensure part footprints were correct. In Allegro, each part has a region defined to indicate the boundaries of the part. The extra definitions sometimes created added constraint errors and undefined errors. Once the component library was completed, the board shape, planes, and traces were worked on next. Proper trace width and current capacity as well as via sizes allowing for proper current throughput were taken into consideration. The inverter involves high power loads, thus a good design needs to be followed to handle the

current. After board and part designs, the silkscreen needed to be mapped out for clear labeling.

5.4.1. PCB Board Assembly

For the first test of the fully assembled board, individual section was tested to compare expectations with what was measured. From this investigation, it was discovered that FET footprints were incorrect. Rework was done to the parts to guide the pins to its correct position. Another issue involved damage to the vias from forcing too much current through the vias. To fix this, direct connections between FET pins and the next connection had to be made physically with wires.

Issues were also seen when testing the design each time due to mix ups in the digital controls and grounding. Signals were missing or misplaced requiring additional debugging time. The populated PCB can be seen in Figure 5-21.

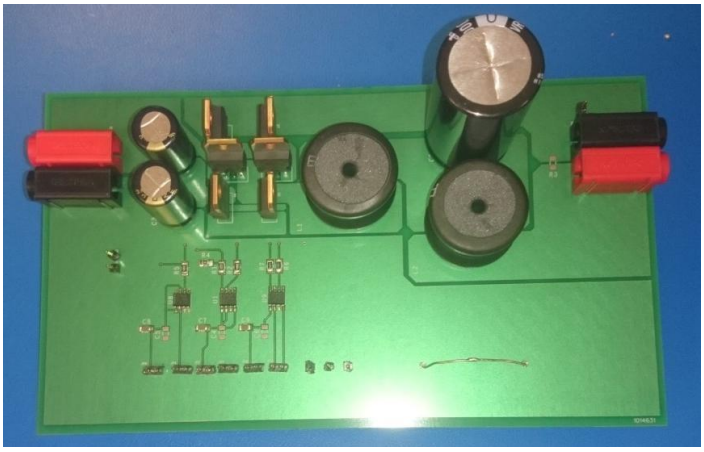


Figure 5-21. Populated PCB assembly.

The expectation of the PCB design was to yield better results than the prototype and deliver the answer to problem statement. The design was able to reproduce results previously obtained through our prototype board. The results from this implementation

improved upon the previous attempt as well, although they fell short of the goal under loaded conditions.

5.4.2. PCB Unfiltered Testing

The first PCB board test is to look at how much load the circuit can support. The first scope in Figure 5-22 looks at the base no load condition. The multilevel output in this case looks ideal with 5 steps created by the five switch topology. The input voltage used was 14V DC which is equivalent to 14Vpp and 8.57Vrms AC output.

In Figure 5-23, a small resistive load is used which loaded the output by 160mA AC. The output voltage was 4.04V AC. The output waveform shows a small distortion on some voltage levels but the multilevel output largely stays in form. Also a few more shoot through signatures can be seen.

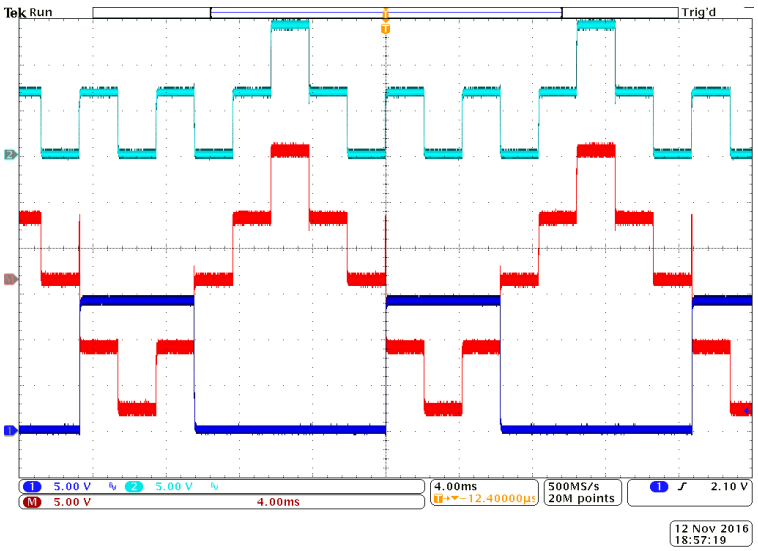


Figure 5-22. No load no filter clean output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

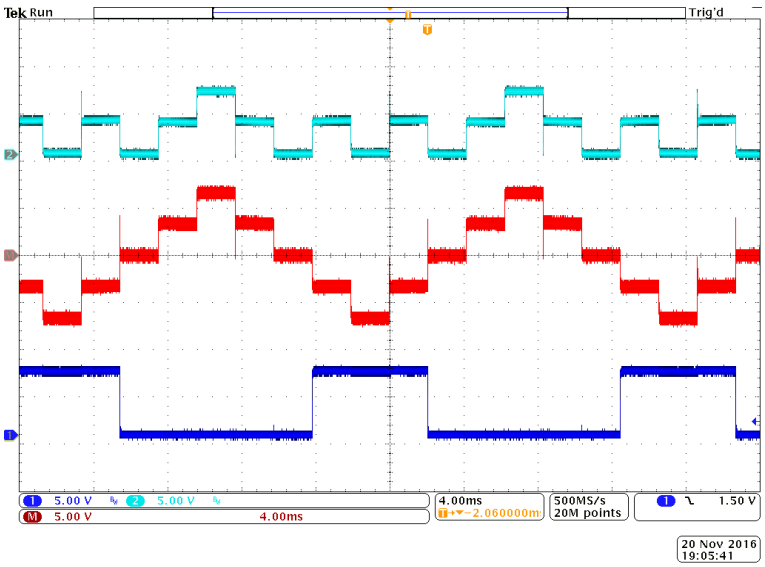


Figure 5-23. Unfiltered small load output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

By significantly increasing the load to 1.555A, the output in Figure 5-24 shows much more noticeable dips on the some voltage levels. This shows signs of the capacitors unable to maintain the voltage levels as the current increases. As current increases conduction losses and bias cause the voltage levels to shift. The balance in the capacitor voltage is also lost. The AC voltage drops to 3.838V in this circumstance.

Furthermore, additional increases to the load cause unrecognizable changes to the output. As seen in Figure 5-25, the middle voltage has collapsed and can barely maintain a voltage level. In the end, 0.925A AC load and 4.52V AC voltage can be seen at the output.

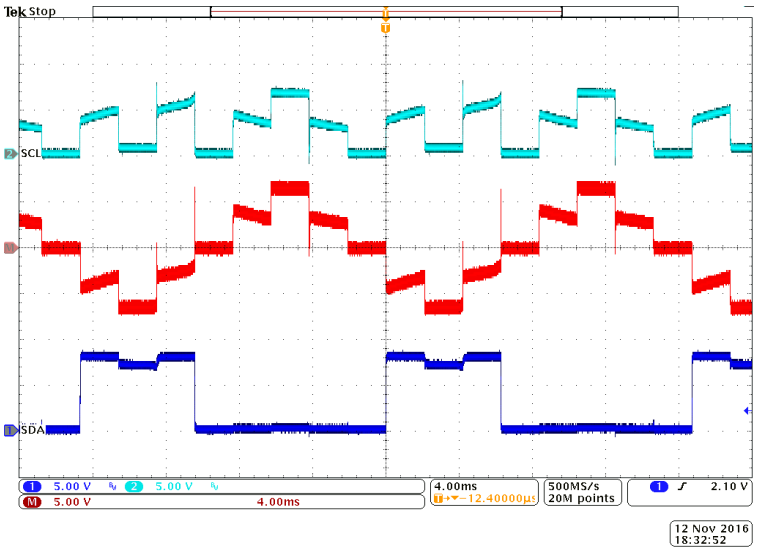


Figure 5-24. Unfiltered 1.5A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

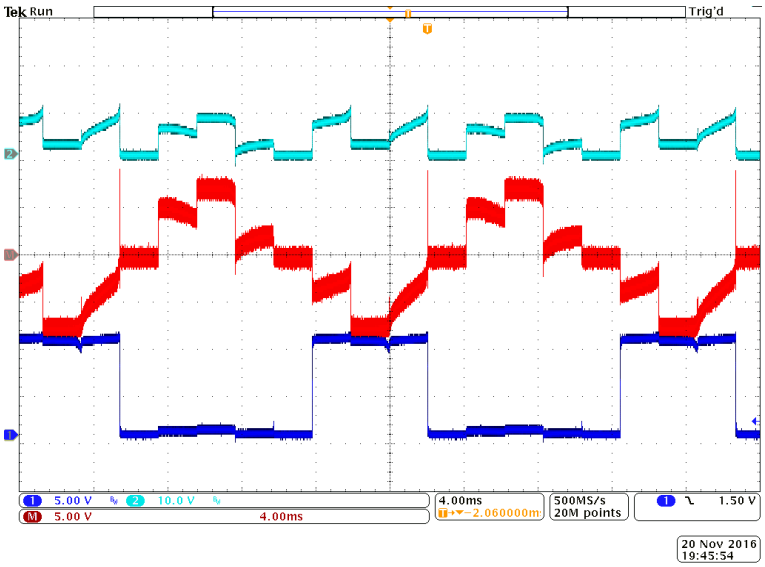


Figure 5-25. Unfiltered 0.9A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

The load is further increased to 2.29A causing the output voltage to decrease to 1.98V in Figure 5-26. As the load increases, the waveform becomes more and more unstable in terms of the voltage levels. Every step of the output waveform struggles to maintain the target voltage. The load is increased to the highest point possible in Figure 5-27. Here the load is 2.49A but the output voltage has decreased even further to

0.967V. The output waveform is similar to Figure 5-26 but with a bit lower amplitude. By increasing the input voltage slightly, the biasing changes and the waveform slightly shrinks as seen in Figure 5-28. Here the output current stays about the same at 2.46A but output voltage increases to 1.35Vrms. Although the output waveform looks lower, the RMS output has increased. Based on the trends observed, the target output load is not achievable so best possible output is looked at next.

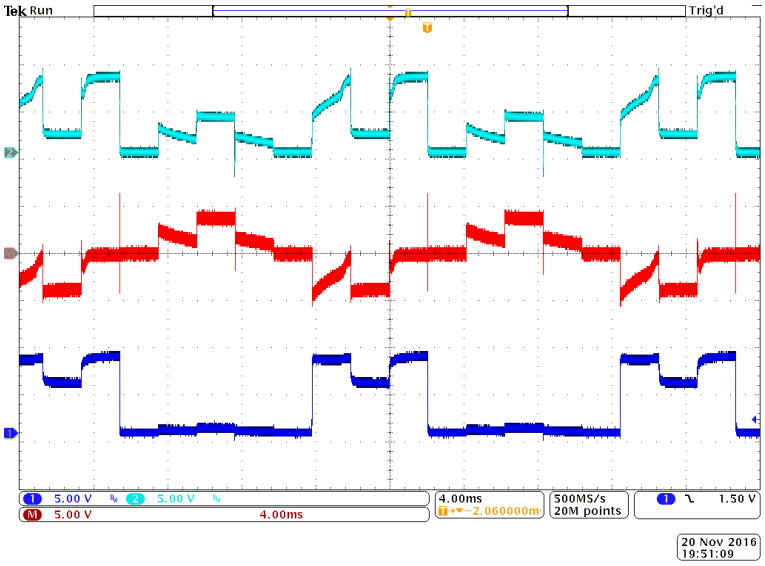


Figure 5-26. Unfiltered 2.29A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

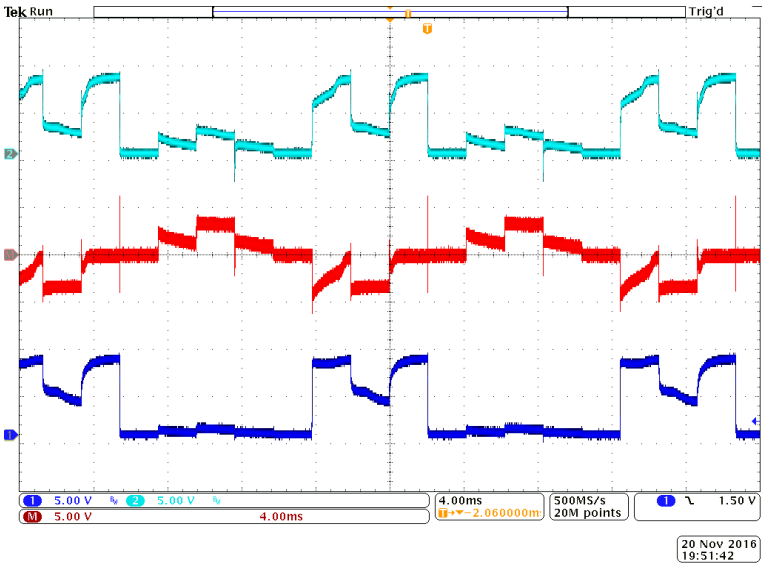


Figure 5-27. Unfiltered 2.49A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

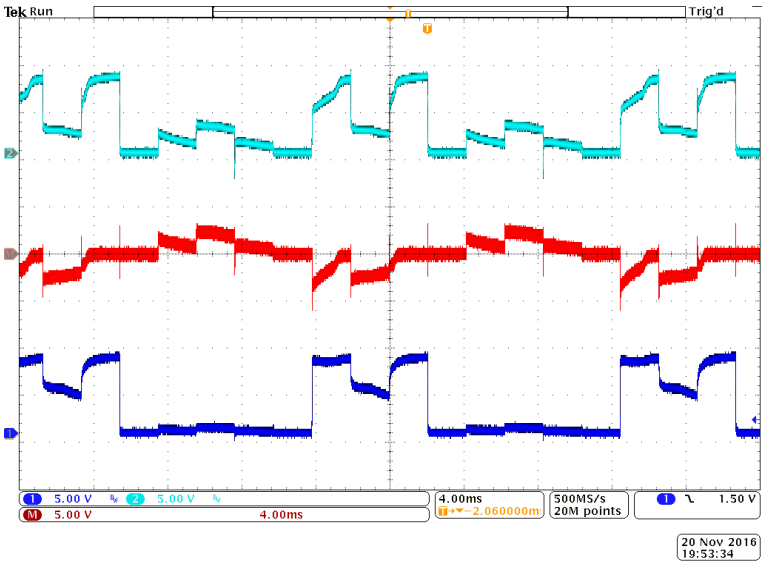


Figure 5-28. Unfiltered 2.46A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

Lastly, the load is lowered until a reasonable output waveform is maintained. In order to determine the highest load possible with a good multilevel inverter output, the output is monitored to check for output voltage steps that are level and well defined. In Figure 5-29, the current circuit configuration's best output maintains 7V AC and 1.34Arms current. On top of current capability, high output voltage also represents a critical parameter in the overall design performance. Keep in mind the original design specifications targeted 12Vpp output with 50W load. In terms of the application, lower voltage can also be an issue towards the operating conditions of the motor or converter.

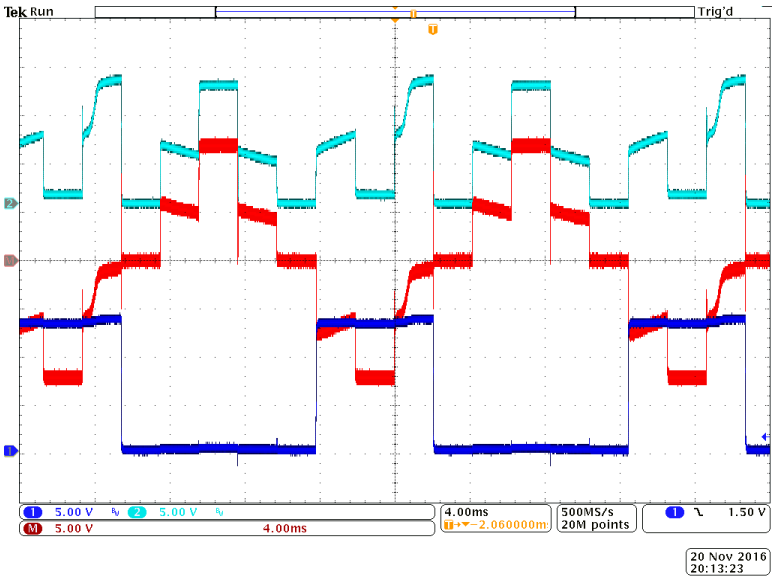


Figure 5-29. Unfiltered 1.34A loaded output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (blue).

5.4.3. PCB Filtered Testing

Similar to simulation and prototype testing, the multilevel design is also capable of generating a five step output with no load from the PCB implementation. Using the PCB design, load is added to see if the reduced parasitic compared to the prototype will improve the output. Unfortunately, increasing the load distorted the multiple voltage levels. Conduction losses increase as we increase the load leaving less than expected voltage at the high level capacitor and mid-level capacitor. Also, considering the switching speed, the energy at the input is insufficient to keep up with the input capacitors needs. As a result, the output further deteriorates as the load increases. To rectify the input energy demands and sustain the input voltage, a bulk input capacitor is needed to provide on-demand energy whenever it is needed.

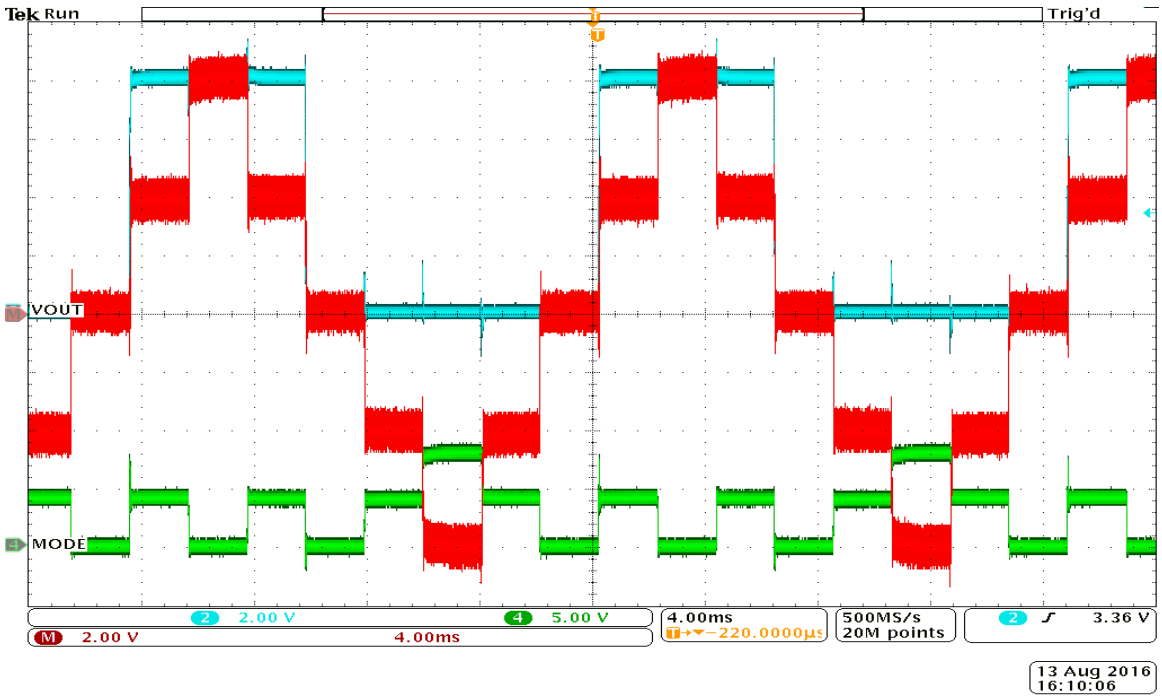


Figure 5-30. PCB Inverter Output (red), output node 1 (blue), output node 2 (green).

The no load pre-filter output obtained from the PCB circuit and seen in Figure 5-30 meets design expectations for the multilevel inverter. From here the inverter output is passed through a filter to improve the THD or AC voltage quality, where ideally the output resembles a sinusoidal waveform. As explored previously in simulations, LC and LCL filters are used to obtain the target output.

During this time, LCL filter complications were discovered. LC values that were too high affected the magnitude making it drop and low LC values did not filter the output enough to lower the THD. Regulating the output voltage was another concern as the load and filter lowered what was seen at the output. In order to accommodate the maximum load, the input voltage was increased to maintain a 12Vp output voltage. Another issue with the LCL filter was the passive filter used only applies to fixed loads that the filter is designed for. Due to this characteristic, the filter would require a large inductor able to support high currents. To recall, the requirements specify 50W

maximum power output meaning approximately 4A at 12Vp is necessary. 12V as an input originated from using a standard 12V DC battery as a possible input to the inverter system. A transformer would also be necessary to step up from the 12Vp to 120Vrms nominal AC output used by the grid.

Following the simulations done with the filters, the PCB board based hardware will also look at the numerous configurations possible for the filter. Due to the unpredictable behavior of the filter, a range of values is tested. The target filter frequency can either attenuate the signal too much or not filter enough of the harmonics. By turning all the knobs including inductor and capacitor values, the goal is to move the cutoff frequency to a spot where amplitude and shape is retained.

The first filter design consist of the LCLC basic filter transferred over from the prototype board. In this case, results are the same as observed from the prototype as seen Figure 5-31. The output being measured is across the load beyond the filter. The waveforms still show some signatures of noise due to shoot through.

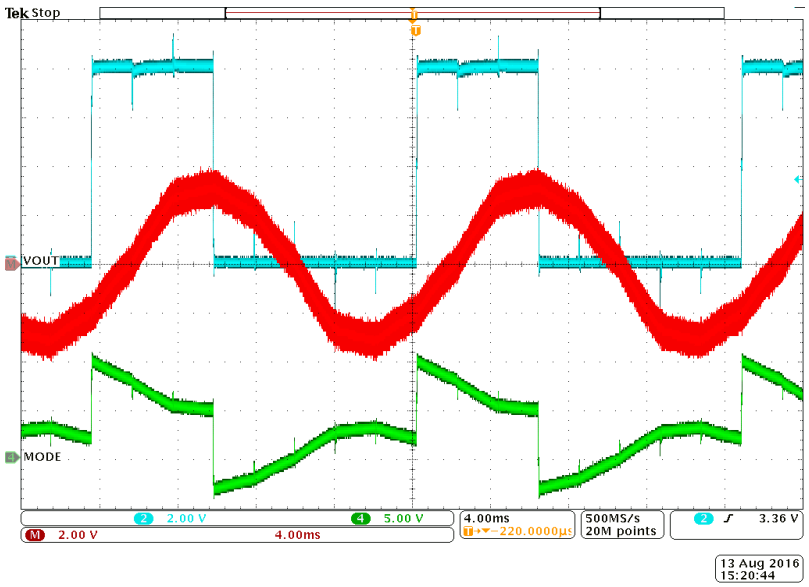


Figure 5-31. LCLC Filtered Output (red) with V_{OUT}+ (turquoise) and V_{OUT}- (green).

In Figure 5-32, the original unfiltered output from the PCB design version of the inverter can be seen when just 44µF capacitor is used as a filter. There appears to be no change when only a capacitor is used. On the other hand, the peak to peak voltage of this waveform is set to 12V as desired and the frequency of the signal is good.

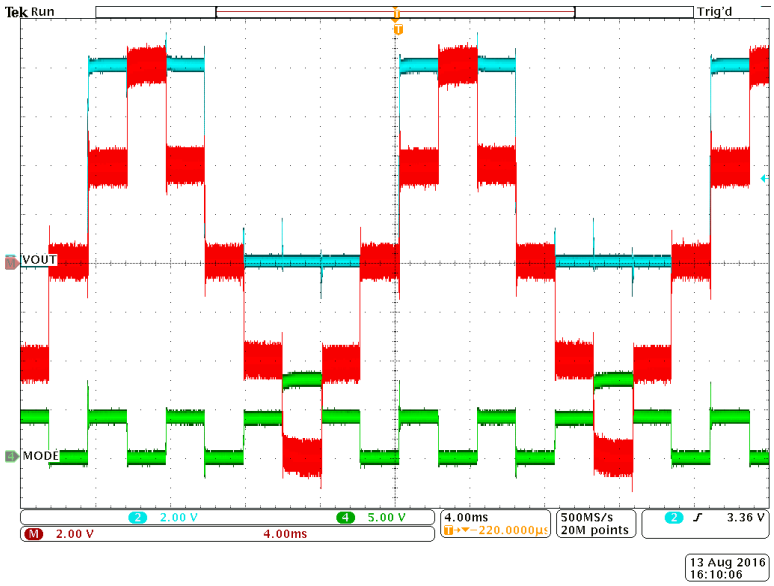


Figure 5-32. Single C Filtered Output (red) from PCB Testing with V_{OUT}+ (turquoise) and V_{OUT}- (green).

By adjusting the filter to an LCL configuration, the output has better AC characteristics as seen in Figure 5-33. In this waveform, a 44µF capacitor is used along with two 5.6mH inductors. There is some distortion but the peak to peak voltage is close to 12V. To further improve the output shape, a 100µF capacitor is added to the 44µF for a total of 144µF. The result of which can be seen in Figure 5-34. By adding 100µF, the tradeoff is the peak to peak voltage is reduced to by approximately half to 6V, but the output signal is much improved.

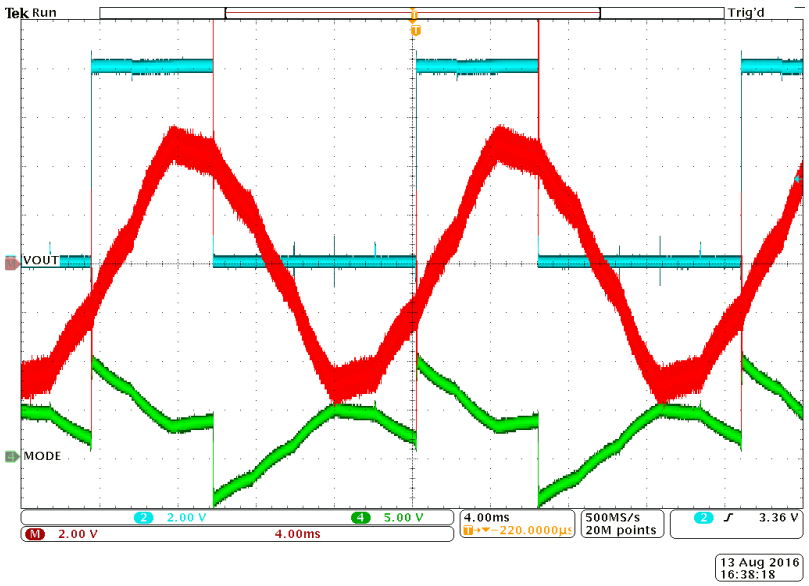


Figure 5-33. LCL Filtered Output with C=44µF (red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

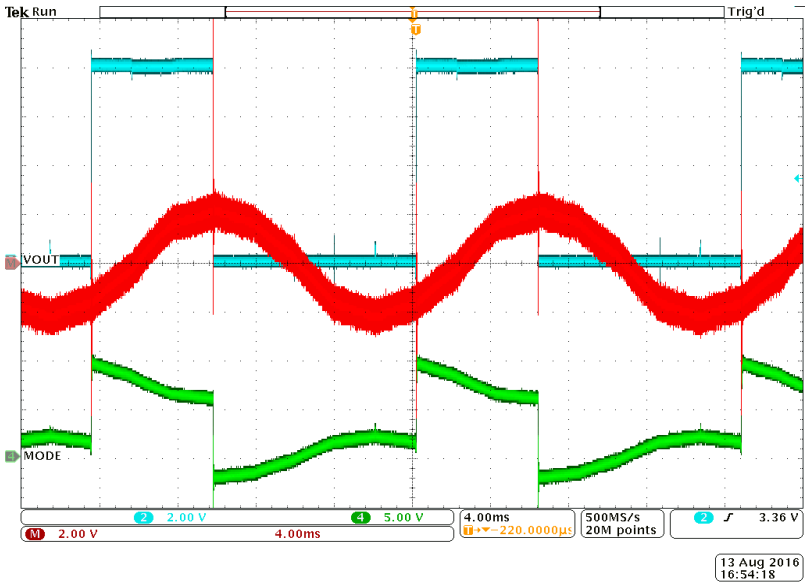


Figure 5-34. LCL Filtered Output with C=144µF(red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

To check the possibility of lowering the inductor size, a 560µH inductor is used in place of one of the 5.6mH. In addition, the capacitor needs to be increased to compensate for the lower inductor value and maintain the cutoff frequency. The total capacitance in the previous figure is increased by replacing the 100µF with a 470µF for a total 514µF capacitor. The result shows massive oscillation on the filtered output which

can be seen in 5-35. The waveform shows a need to adjust the filter values higher. In Figure 5-36, 100µF is added to the previous configuration for a total of 614µF. By doing so, the oscillations are reduced and thus improving the output.

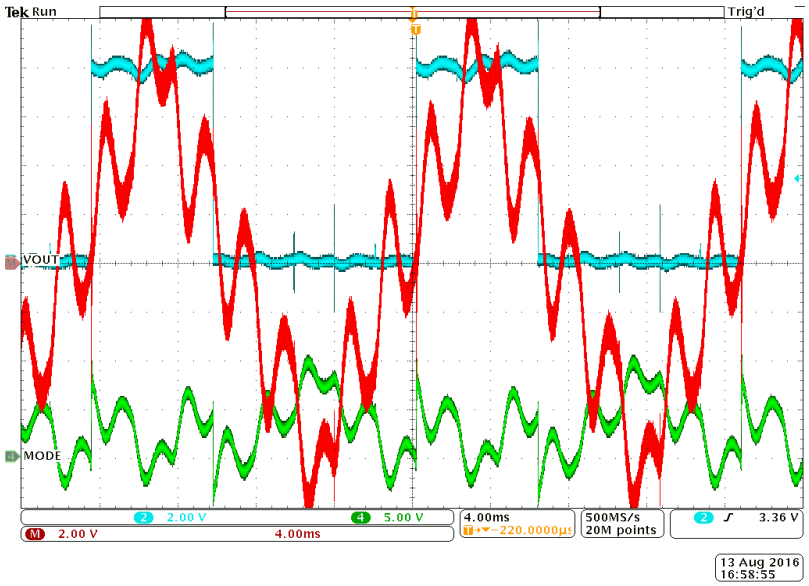


Figure 5-35. Smaller Inductor and Larger C Filtered Output (red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

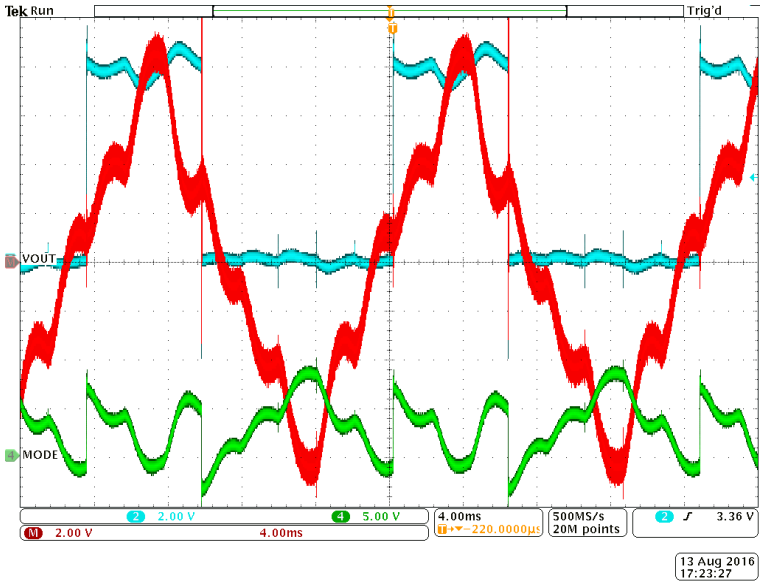


Figure 5-36. Increased C to 614µF from Figure 5-33 with Output (red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

Due to the constraints of the inductor component availability, the second inductor is also reduced to 560µH for testing. Starting with the capacitor value back to 144µF, the waveform in Figure 5-37 shows large oscillations as seen previously. Again, the capacitor needs to be drastically increased to compensate for the lower impedance contribution from the inductor. By increasing the capacitor gradually, the optimal filter capacitor turned out to be 614µF. The waveform in Figure 5-38 shows similar results to those previously found in Figure 5-36.

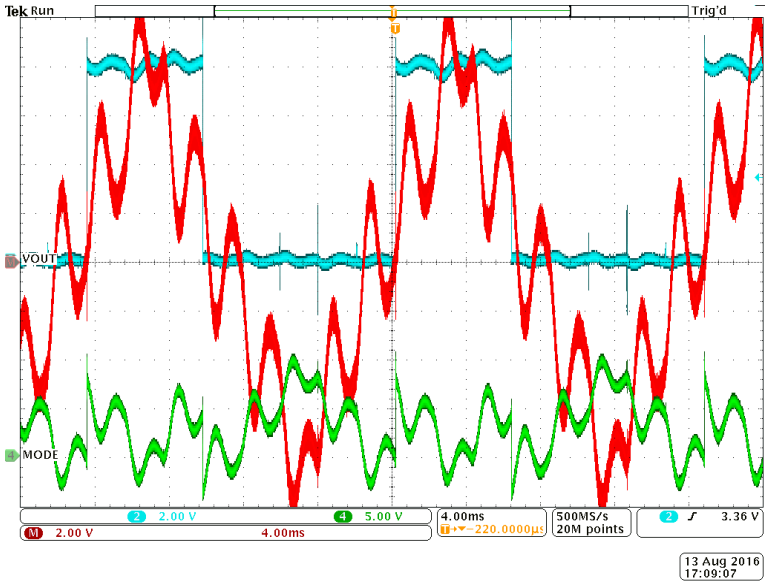


Figure 5-37. L1, L2=560µH and C=144µF Filtered Output(red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

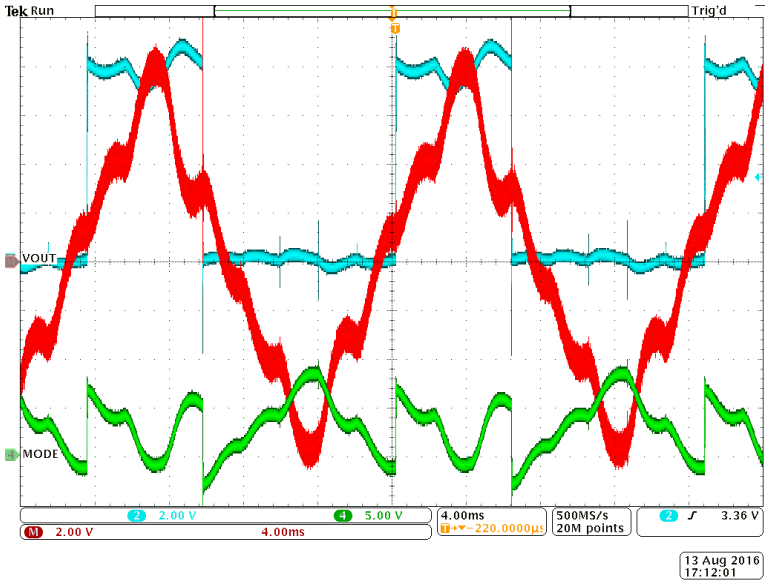


Figure 5-38. Increased C to 614µF from 5-35 with Output (red), V_{OUT}+ (turquoise) and V_{OUT}- (green).

The conclusion was reached after implementing the design on a PCB board and monitoring the output. As the load is increased, corresponding noise was seen on the output. Again, the electrolytic capacitors turned out to be an issue because they do not work in a bipolar direction limiting the capacitor's effectiveness on the negative cycle.

Chapter 6. Conclusion

This thesis looked at the design and implementation of a single phase H-bridge interconnected inverter. The goal was to use this unique topology to improve the power quality but also utilize a lower complexity design to improve inverter outputs. To do so a long process involving research, design, and testing was done to study the inverter by utilizing simulations and hardware test.

There were many steps along the way to getting to the final results. The first part involved testing each of the blocks and baseline simulation using generic parts. After getting that working, the FETs were integrated into the simulation. Although there were issues with convergence, those issues were solved by revising some of the simulation parameters and rise times used in the control signals.

Another key aspect of the simulations was implementing a piecewise signal to represent the ideal output for the inverter. Using the signal helped reduce compounding issues with the inverter output and filter design.

Each hardware part was also successfully tested including the microcontroller design. The microcontroller programmed control signals was a critical step in the overall project. The timing of the signals had to be accurate to avoid shoot through in the switches. Also, working through the features available to get the multiple control signals was a challenge.

Once the individual blocks were tested, the inverter was built on a prototype board. The design was incrementally tested from individual driver and control signal testing to full circuit integrated testing. The output without the filter was first successfully implemented showing a clean multilevel signal. Following such testing, the filtered testing produced smooth sinusoidal outputs. THD measurements confirmed a quality inverter output.

After successful prototype testing on the proto-board, the entire design was recreated on a PCB. The design took considerable development time to build from scratch using Allegro. Development went into learning and executing part footprints, board routing and planes, board vias and pads, alignment, silkscreen label implementation and more. From the completed design, the board was fabricated and assembled.

Using the completed board, unfiltered load testing was done to see how the design holds up. At the baseline of no load, output looked good with multiple steps as expected. As the load was increased, however, the levels on the output started to distort.

This was the first sign of issues with the design. The distortion can be attributed to the bulk capacitor's failure when sudden high levels of current are needed from the input. Also, part of this issue is attributed to capacitor balancing used on the input to maintain voltage levels. The final cause was due to the characteristics of electrolytic capacitors. Under negative bias, the capacitors become low impedance and can sink a lot of current resulting in heating problems and expected interactions with the output. Issues with how capacitors were used can be an area of future work.

The greatest area of difficulty encountered was the proper implementation of high power filters. Not only can filters be difficult to design under normal circumstances, high power applications present a whole another beast. Just from the LCL filter testing, issues were encountered whenever a load was applied. Attempts at changing the filter values were done but the issues caused by the current persisted. The source of the problem comes from the inductor value changing as load increases thus affecting the filter response. The saturation of the inductor can be improved by a custom inductor to handle higher currents, which can be another area for future improvement.

To tackle the high power filter issue, major research was done to look at possible options. The solution could not be included in this project since the improvements are difficult topics in their own right. The first area looks at changing from a passive filter to active filter to properly handle a wider range of loads. With an active filter, the feedback path can adjust the filter characteristics accordingly as the load changes. Another option as mentioned earlier was to build a custom inductor which can support high current loads. A multistep design looking at the core material, air gap, and number of windings would need to be looked at. Lastly, a higher switching frequency for the control signals would loosen the filter constraints allowing for smaller more readily available components to be used.

As part of applying a faster switching frequency, future work would include looking at other means to provide control signals due to the microcontroller's frequency limitations. Further down the line with a working filter and load support, the efficiency can be tracked to quantify the possibility of using it in an application. Also, in order to support an application, a transformer would need to be added to step up to 120Vrms mains voltage.

In the end, the design was successfully implemented. Software and hardware implementations were fully executed showing the expected 60Hz multilevel output voltage waveform. The filtered output at no load condition was also observed to be a good sinusoidal output waveform with low THD, demonstrating the potential of the proposed multilevel inverter topology.

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