

DESIGN OF AN ACTIVE HARMONIC REJECTION N-PATH FILTER FOR HIGHLY
TUNABLE RF CHANNEL SELECTION

A Thesis
presented to
the Faculty of California Polytechnic State University,
San Luis Obispo

In Partial Fulfillment
of the Requirements for the Degree
Masters of Science in Electrical Engineering

by
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June 2017

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ABSTRACT

Design of an Active Harmonic Rejection N-Path Filter for Highly Tunable RF Channel Selection

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As the number of wireless devices in the world increases, so does the demand for flexible radio receiver architectures capable of operating over a wide range of frequencies and communication protocols. The resonance-based channel-select filters used in traditional radio architectures have a fixed frequency response, making them poorly suited for such a receiver. The N-path filter is based on 1960s technology that has received renewed interest in recent years for its application as a linear high Q filter at radio frequencies. N-path filters use passive mixers to apply a frequency transformation to a baseband low-pass filter in order to achieve a high-Q band-pass response at high frequencies. The clock frequency determines the center frequency of the band-pass filter, which makes the filter highly tunable over a broad frequency range. Issues with harmonic transfer and poor attenuation limit the feasibility of using N-path filters in practice. The goal of this thesis is to design an integrated active N-path filter that improves upon the passive N-path filter's poor harmonic rejection and limited out-of-band attenuation. The integrated circuit (IC) is implemented using the CMRF8SF 130nm CMOS process. The design uses a multi-phase clock generation circuit to implement a harmonic rejection mixer in order to suppress the 3rd and 5th harmonic. The completed active N-path filter has a tuning range of 200MHz to 1GHz and the out-of-band attenuation exceeds 60dB throughout this range. The frequency response exhibits a 14.7dB gain at the center frequency and a -3dB bandwidth of 6.8MHz.

Keywords: N-path filter, band-pass filter, harmonic rejection, mixers, frequency transformation, LNA, CMOS, software defined radio, tunable, integrated circuit

ACKNOWLEDGMENTS

I would like to thank Dr. Tina Smilkstein for all of her insight and guidance over the course of the last two years. I am also grateful for my family's unwavering support and encouragement. Special thanks go out to Bijan Shirazi-Wu and Sung Tran for all of their help during the design process.

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1. Introduction

According to a CTIA survey, Americans' wireless data traffic increased from 9.65 trillion MB to 12.72 trillion MB between 2015 and 2016 (a 42% increase) and shows no signs of slowing down [17]. As the demand for data increases so does consumers' demand for higher data rates. Data speeds can be improved using spectrally efficient modulation methods such as OFDM, but the biggest bottleneck preventing faster data rates is the limited availability of bandwidth. Because the frequency spectrum is finite, the FCC grants licenses for specific frequency bands to particular users, restricting the amount of bandwidth available for each communications channel. This limitation will become more prominent as the number of wireless devices continues to increase.

Although most of the RF spectrum is already licensed, much of the spectrum remains underutilized. In many cases, licensed users do not fully utilize the bands allotted to them. In many cases, licensed users do not broadcast in certain geographic locations, and in regions where they do, most users do not continuously broadcast on their licensed bands at all times [19]. This method of fixed spectrum access limits available bandwidth, which creates a needless bottleneck for data rates.

One proposed method of relaxing the strict bandwidth limitations is dynamic spectrum access. Using this policy, the FCC can license frequency bands to primary users who are allowed unrestricted access to the frequency bands allocated to them. When the primary user is not actively broadcasting over the bands allotted to them, secondary users would be permitted to utilize the vacant frequency bands as long as the bands are not in use. Using this dynamic spectrum access system would dramatically improve spectral efficiency and allow users more bandwidth as it becomes available [18]. With this in

mind, much research has been conducted in the last 8 years on cognitive radios that are capable of dynamically sensing spectral availability and switching to unutilized bands. The bands between 470MHz to 700MHz are particularly noteworthy due to the existence of white space at these frequencies following the switch from analog to digital TV transmission [19]. In practice, implementing a cognitive radio requires a software defined radio (SDR) to provide the flexibility needed to dynamically switch its transmission parameters. However, the flexibility of the RF front end is the limiting factor for implementing an all-inclusive software defined radio.

The need for a flexible RF front end is not just a matter of convenience, but also economics. Many computers in today's modern world communicate over multiple communications standards using a wide range of frequency bands. A typical smart phone in the United States, for example, utilizes GSM, CDMA, Wi-Fi-, Bluetooth, and GPS signals. Currently, each standard requires its own dedicated hardware in the receiver chain due to the unique bandwidth, modulation and dynamic range requirements for each standard. In addition, some standards also require dedicated hardware to cover multiple bands. A Wi-Fi module operates at either 2.4GHz or 5.8GHz, for example. From a designer's standpoint, implementing all of these communications protocols with dedicated hardware increases the cost of the bill of materials and increases circuit board area. For mobile and satellite applications in particular where board area comes at a premium, integrating a flexible all-inclusive wireless communications system is expensive. Using an SDR, many of the processes currently handled in hardware, such as demodulation and amplification can be implemented in software instead, allowing the ADC to be placed earlier in the receiver chain. This allows for a small set of tunable

receiver circuitry to be used for a variety of communication protocols. Implementing such a radio could decrease radio cost and increase flexibility at the same time. In addition, the ability to dynamically sense spectral usage and reallocate bandwidth as it is available will allow for radio systems to optimize their data rates at a given moment without causing interference over adjacent channels.

A flexible radio design that is capable of switching between channels over a wide frequency range requires an equally flexible RF front end. Two of the biggest limitations of implementing a flexible radio capable of operating over many communications standards and a wide frequency range is the tunability of the channel-select filter and the linearity of the LNA. One potential solution for implementing a high Q band-pass filter is the N-path filter which features a wide tuning range and good linearity. Over the last eight years, much research has been conducted on passive N-path filters to replace the resonance based filters used in modern receiver designs.

This thesis paper details the design and implementation of an active N-path filter with improved harmonic rejection capable of operating between 200MHz to 1GHz.

Implementing the N-path filter as an active circuit improves the out-of-band attenuation and can potentially combine the channel-select filter and into a single circuit.

Chapter 2 of this thesis paper describes the traditional superheterodyne receiver architecture and discusses the need for a more flexible RF front end. Chapter 3 describes the N-path filter, a novel band-pass filter topology that exhibits high quality factors over a tunable frequency range as well as its limitations. Chapter 4 seeks to expand on the original N-path filter design and explore methods of improving its out-of-band attenuation and harmonic rejection. Chapter 5 covers the design and implementation of

an active N-path filter featuring harmonic rejection using the CMRF8SF 130nm CMOS process. Chapter 6 compares the new N-path filter's performance to previous works and discusses its potential use as a channel-select filter in a flexible receiver design. Chapter 7 summarizes the findings of this thesis paper and proposes ways to expand on this thesis project.

2. Background and Motivation

The architecture for a standard superheterodyne receiver is shown in Figure 1. The primary source of nonlinearity in the RF front end is the low noise amplifier (LNA). Every circuit in the RF front end contributes additional noise to the input signal. An LNA is optimized to maximize signal gain while minimizing its noise contribution. The LNA amplifies the signal early in the signal chain in order to prevent the noise from subsequent stages from corrupting the desired signal. Because of this, placing the LNA before the mixer is critical for maximizing the receiver's ability to detect small signals. The tradeoff for this improved sensitivity is a reduction in linearity.

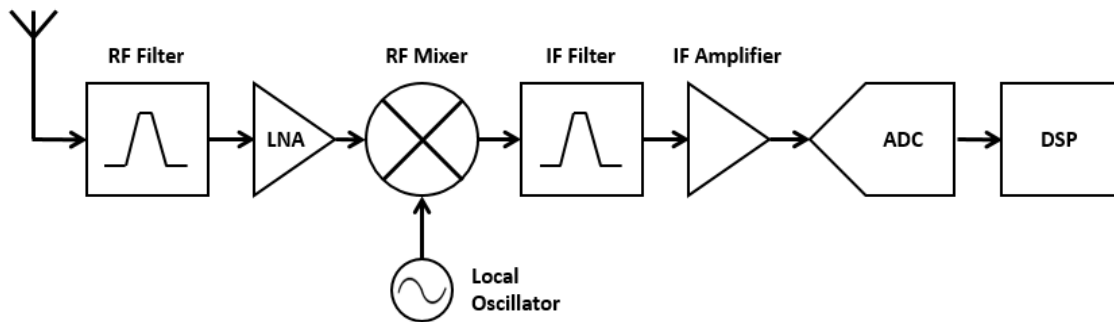


Figure 1: Black box diagram of a typical superheterodyne receiver

In practice, the antenna picks up not only the desired signal but also out-of-band signals called interferers. In some cases, these interferers may exist at much higher power levels than the desired signal. This can cause several undesired behaviors. Interferers at power levels exceeding the LNA's 1dB compression point will saturate the LNA, which reduces the gain of the intended signal. In extreme cases, this causes permanent damage to the LNA. In addition, because the LNA is a nonlinear device, it produces intermodulation distortion between the out-of-band interferers and the signals in nearby channels. If the

resulting intermodulation products fall near the desired channel, the resulting distortion corrupts the data on that channel.

In order to minimize the intermodulation distortion in the output, an RF band-pass filter precedes the LNA to remove any large out-of-band interferers. The band-pass filter, or channel select filter, should have a high quality factor and out-of-band attenuation in order to maximize the attenuation of the interferers, low noise figure to maintain high sensitivity to small input signals and high linearity to minimize distortion resulting from large signals [8]. This band-pass filter is typically not integrated on-chip and is designed to operate over a narrow set of frequency bands. This thesis focuses on the design of an integrated high-Q band-pass filter with a tunable center frequency and harmonic rejection.

In RF communications, most systems are designed to utilize very narrow frequency bands in the radio spectrum. The band-pass filter determines the bandwidth of the signal that feeds into the LNA so in many cases, the tuning range of the receiver is limited by the frequency range of the band-pass filter.

Many band-pass filter topologies for the RF channel-select filter are available, each of which have their own advantages and disadvantages. The simplest method of filtering out-of-band interferers involves using passive filters. Lumped element filters such as LC ladder filters are simple to design, and because they are designed entirely with passive components, they have optimal linearity. Several factors make lumped element filters impractical to integrate in CMOS. Integrated inductors have very low quality factors, which increases insertion loss, and they take up a lot of area on the chip. Capacitor and inductor values can be tuned by electromechanical means, but doing so also changes the

bandwidth of the system. In addition, the parasitic inductance and capacitance of these lumped element circuits cause the components to self-resonate at high frequencies elements cause these lumped elements to self-resonate at high frequencies.

Another potential option for band-pass filtering at high frequency involves using active filters such as transconductor-C (gm-C) circuits. These gm-C filters use operational transconductance amplifiers (OTAs) and capacitors in order to emulate LC ladder filters. Small transistors are able to replace inductors for these circuits, which make them much easier to integrate in CMOS at the cost of dynamic power consumption. The center frequency of these filters is tunable by modulating the gain of the transconductors, but the biggest disadvantage with the gm-C filter for the receiver front end is the compromise between gain and linearity. Transconductance amplifiers are notoriously nonlinear. Decreasing the filter's gain improves linearity, but attenuation of the signal prior to the LNA degrades the filter noise figure of the entire RF front end, which reduces the receiver's sensitivity to weak signals.

Most current CMOS receivers used today utilize electromechanical resonators such as surface acoustic wave (SAW) and bulk acoustic wave (BAW) filters for high frequency channel-select filters. These filters take advantage of the piezoelectric behavior of their crystal structures to resonate at precise frequencies. These filters exhibit high quality factor (Q), out-of-band attenuation and can be designed for a wide range of frequencies up to a few GHz. The downside of this filter however, is that the resonant frequency is fixed based on the filter's crystal structure. Designing a highly tunable RF front end for a SDR requires the usage of multiple SAW filters to encompass the entire frequency range. This increases the cost of the bill of materials and increases board area. A relatively new

option to implement a tunable high Q band-pass filter at high frequencies is the N-path filter, which will be discussed in Chapter 3.

3. N-Path Filters

3.1. The Ideal N-Path Filter

One option to replace the traditional resonator-based filters at high frequencies is the N-path filter. An N-path filter is a high frequency band-pass filter composed of switches and passive components that enable baseband to RF filter transformation. Both discrete-time and analog N-path filters have been researched, but this paper focuses on the implementation of analog N-path filters. Initial research into N-path filters began as early as 1947 and continued through the early 1960s [2]. Although initial research into N-path filters was promising, poor matching of integrated capacitors of the time rendered the N-path filter too impractical for use. However, advances in CMOS technology over the last 20 years have made the implementation of N-path filters practical for modern receiver designs. Using current CMOS technology, integrated capacitors are very well matched and due to improved CMOS scaling, and low resistance switches can easily be implemented at GHz frequencies, which makes N-path filter design more feasible for SDR receiver designs.

The fundamental theory behind N-path filtering is shown in Figure 2. In the ideal case, the RF input signal is mixed with a sinusoidal local oscillator, LO, that is driven at the same frequency as the incident wave to perform a direct conversion of the RF signal to baseband. The resulting signal is passed through a baseband low-pass filter, and then passes through another mixer to shift the frequency back to RF. In theory, the resulting frequency response is identical to that of a band-pass resonator when the LO frequency matches the RF frequency. Typically, a first order RC low-pass filter is used for the baseband filter, however, a high-pass filter can be used instead to implement an RF notch

filter. A minimum of two paths, with their LO's 90° out of phase with each other is needed to eliminate the filter's sensitivity to the phase of the input signal.

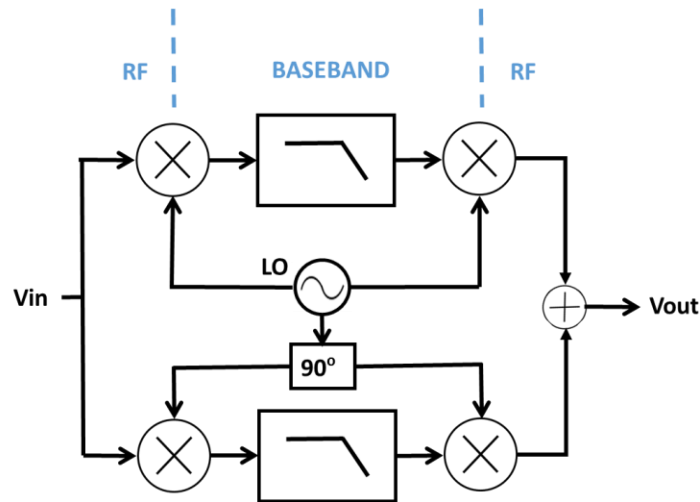


Figure 2. The basis of the N-path filter. A low-pass filter can be transformed to an RF band-pass filter by mixing an RF input down to baseband, passing it through a low-pass filter and mixing it back up to RF

The benefits of this low-pass to band-pass transformation are twofold. The primary benefit is that the center frequency of the resulting band-pass filter matches the clock frequency. Because the RF signal is directly converted and filtered at baseband, the center frequency is easily tunable by changing the clock rate. This type of band-pass filter can have a much wider operating frequency range than a resonance-based filter because the frequency range is limited by the VCO's linear range rather than by the relatively inflexible electromechanical structure of a resonator such as a SAW filter.

Another benefit of the low-pass to band-pass transformation method is the increase in quality factor resulting from the up-conversion of the baseband filter's frequency response to RF. After the signal passes through the baseband filter, the second mixing operation performs a frequency-domain convolution between the baseband spectrum and the impulse at the LO frequency as shown in Figure 3

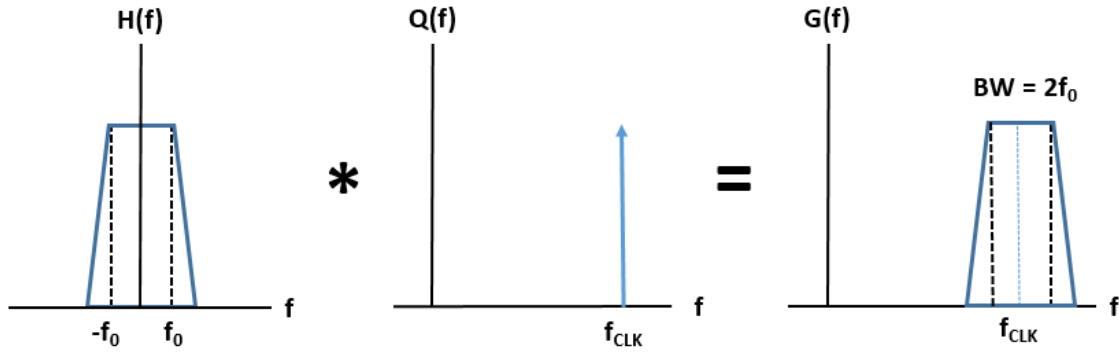


Figure 3. Cascading a low-pass filter with a mixer transforms the baseband filter to a high frequency band-pass filter.

If the LO is an ideal sine wave, it can be shown that the resulting Fourier Transform is identical to the baseband filter, but shifted to the LO frequency due to the convolution of the baseband spectrum and the impulse at the LO frequency. Because both the positive and negative components of the baseband spectrum are shifted up to high frequency, the half power bandwidth of the resulting band-pass filter is exactly double that of the original baseband filter. This transformation can make a low order baseband filter behave like a high order band-pass filter at sufficiently high frequencies. If the clock frequency is 500MHz and the baseband filter is a first order RC low-pass filter with a bandwidth of 3MHz, the resulting band-pass filter will have a bandwidth of 6MHz, which corresponds to a quality factor of 83.

In practice, N-path filters are implemented as a collection of N identical networks consisting of two mixers and a linear time-invariant baseband filter with an impulse response $h(t)$ as shown in Figure 4. The mixers are composed of passive switches, driven by N non-overlapping clock phases with a duty cycle of $1/N$. Passive switching mixers provide several benefits over their active counterparts for the purpose of channel-select filtering. MOS switches have very high linearity compared to active CMOS mixers such

as the Gilbert cell. In addition, the amplitude of the output waveform is independent of the voltage swing of the mixing waveform, which makes N-path filter design relatively simple to scale with variable voltage ranges.

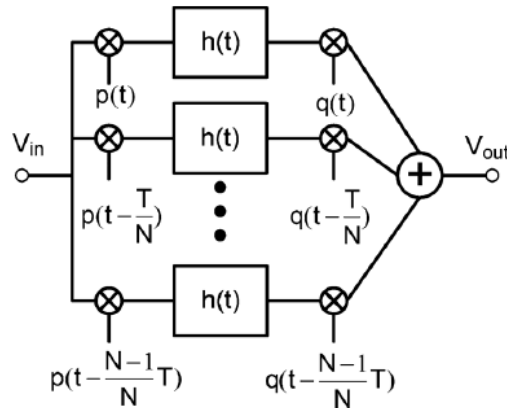


Figure 4. Architecture of an N-path filter. The mixing function is split between N phases with a clock period of T and duty cycle 1/N. The up-converted outputs are summed together at the output [1].

Figure 5a shows the simplest implementation of an N-path filter. For this analysis of this circuit, we will assume that the clock phases in Figure 5c each have a duty cycle of 1/N, are $360^\circ/N$ out of phase with each other, and have zero rise and fall times, so there is no overlap between any of the clock phases. In addition, each pair of mixers in the same path is clocked with the same clock phase. With these assumptions in mind, it is apparent that since only one path is ever active at any given moment due to the non-overlapping clock structure, no charge sharing occurs between the capacitors. Because of this, each path can share the same resistor. In addition, since both mixers in the same signal path share the same clock signal, their functionality can be combined into a single switch. These modifications allow for the circuit in Figure 5a to be simplified to the circuit in Figure 5b. Looking at Figure 5c and d, if the input frequency matches the clock frequency, each clock phase will be active for the same segment of the input wave during every period.

Because each switch is connected to a single capacitor and the clocks never overlap, each capacitor in turn only sees the same part of the input signal every period.

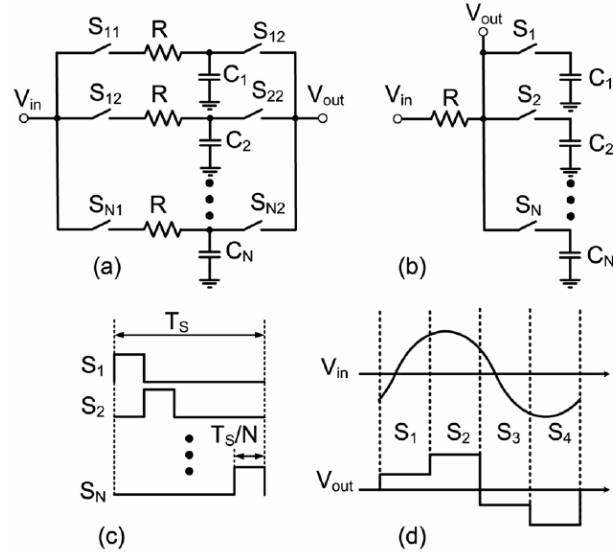


Figure 5. (a) Basic single-ended double port N-path filter. (b) single-ended single port N-path Filter
 (c) Multiphase non-overlapping clock structure (d) Input and output signal where $f_{clk} = f_{input}$ [1]

Each segment of the input signal can be broken up in terms of its DC component (average) and a high frequency component. During each active clock phase, the associated capacitor integrates the segment of the input that it sees. After many clock cycles, each capacitor charges up to the average value of its associated segment of the input signal, and the output voltage appears like a sampled version of the sinusoid, sampled at a rate of Nf_{CLK} . In short, each phase of the N-path filter performs a direct conversion of each phase of the input signal to baseband, filters out any high frequency signals, mixes the signal back up to RF and then sums each of the N paths to regenerate the original sine wave.

Conversely, if the clock input frequency does not match the input frequency, the mixer operation outputs an intermediate frequency (IF) instead of directly converting the input

to baseband. If the IF falls outside of the bandwidth of the filter, it will be suppressed by the baseband filter as shown in Figure 6.

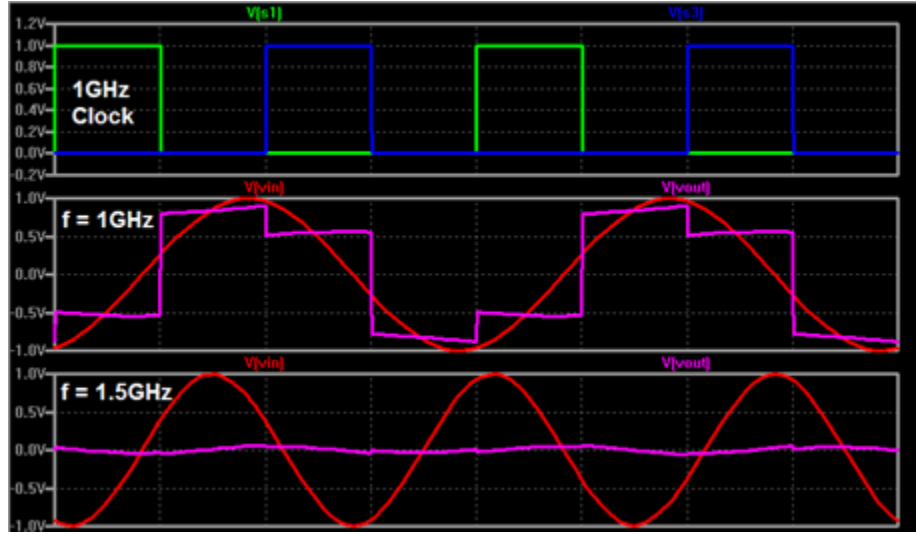


Figure 6. Time domain waveforms of an N-path filter (N=4)

Because the series resistor sees each baseband capacitor $1/N$ of the each clock cycle, the filter bandwidth cannot be calculated directly from the component values of the baseband filter. The actual transfer function depends on the clock frequency and the duty cycle. A RLC equivalent model for the ideal behavior of the N-path filter is proposed in [1] and displayed in Figure 7.

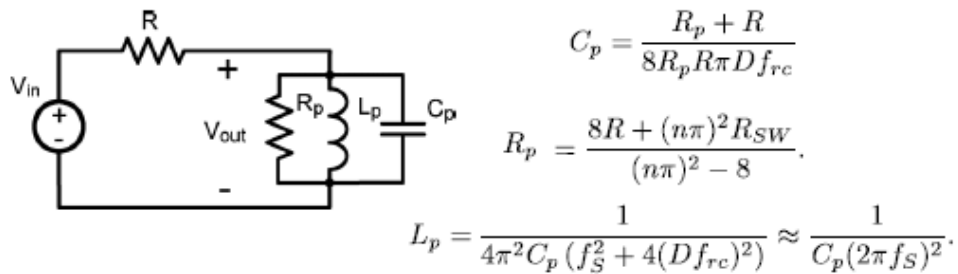


Figure 7. RLC model for the ideal N-path filter.

3.2. Drawbacks of N-Path Filtering

3.2.1. Harmonic Transfer

N-path filters suffer from several issues that limit the application of N-path filters for flexible radio receiver applications. One primary concern is the unwanted transfer of harmonics in the frequency response.

An ideal mixer can be treated like an analog multiplier driven by a pure sinusoidal local oscillator (LO) as shown in Figure 8. When presented with an input signal and LO, the mixer outputs new signals at the sum and differences of the two input frequencies

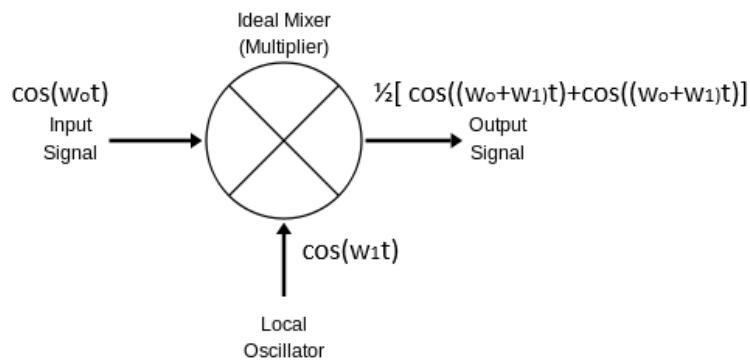


Figure 8. Operation of an ideal square-law analog mixer

In the case of the N-path filter, each mixer is implemented as a passive switch. The pure sinusoidal LO is replaced by driven by periodic rectangular pulses with a duty cycle, D , of $1/N$.

The Fourier series representation of the periodic pulse waveform is as shows.

$$a_n = AD \operatorname{sinc}(\pi n D) = \frac{A}{N} \operatorname{sinc}\left(\frac{\pi n}{N}\right), \quad b_n = 0$$

For simplicity, if we assume that $A=N$, we can expand the series into the Fourier representation of the periodic pulse as follows.

$$FT\{q(t)\} = \text{sinc}\left(\pi \frac{f}{Nf_{clk}}\right), \quad \text{for } A = N$$

Based on the Fourier series representation of the $1/N$ duty cycle clock, it is apparent that the spectrum of the LO waveform is non-ideal. When the $1/N$ duty cycle clock is used as an LO, the passive mixer multiplies the input signal with all of the clock signal's harmonics as well as the fundamental. Because the mixing operation can be divided into a down-conversion stage and an up-conversion stage, the magnitude of the harmonic spurs determine the envelope of the transfer function shown in Figure 9. A time domain waveform of the harmonic transfer is shown in Figure 11.

$$Envelope(f) = \text{sinc}^2\left(\pi \frac{f}{Nf_{clk}}\right)$$

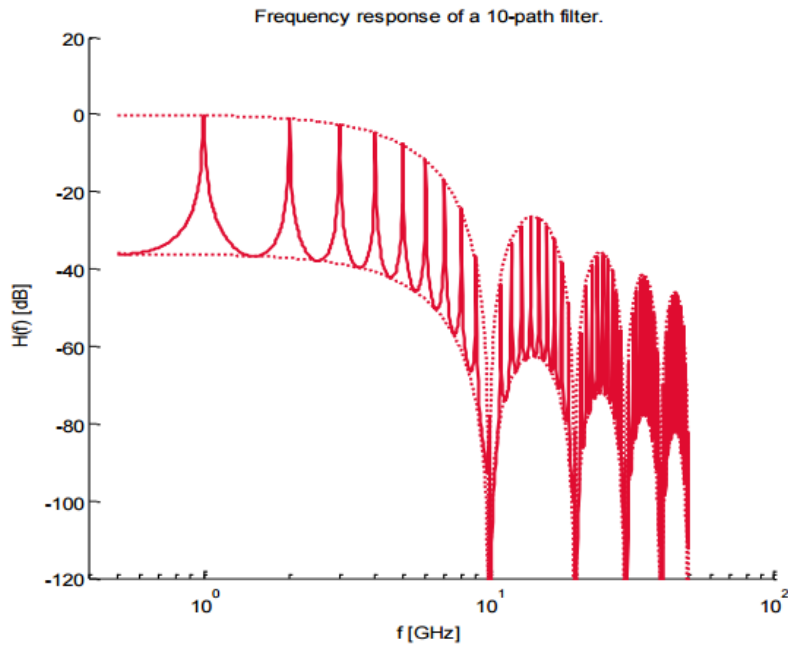


Figure 9. Transfer function of a 10-path filter. The harmonic transfer is due to the mixing of the $1/N$ duty cycle clocks [5]

In nonlinear systems, using a fully differential circuit removes the even harmonics from the frequency response. This occurs because the output voltage is taken as the difference between two output nodes. Taking any real number to an even power removes the sign from the signal so all even harmonics cancel out as shown.

$$V_{out}^+ = a_0 + a_1 \cos(\omega_1 t) + a_2 \cos^2(\omega_1 t) + a_3 \cos^3(\omega_1 t) + \dots$$

$$V_{out}^- = a_0 - a_1 \cos(\omega_1 t) + a_2 [-\cos(\omega_1 t)]^2 + a_3 [-\cos(\omega_1 t)]^3 + \dots$$

$$V_{out,diff} = V_{out}^+ - V_{out}^- = 2a_1 \cos(\omega_1 t) + (a_2 - a_2) \cos^2(\omega_1 t) + 2a_3 [\cos(\omega_1 t)]^3 + \dots$$

$$V_{out,diff} = 2a_1 \cos(\omega_1 t) + 2a_3 [\cos(\omega_1 t)]^3 + \dots$$

All of the even harmonics can thus be eliminated from the frequency response by using the fully differential implementation shown in Figure 10. Each capacitor is clocked differentially, with both clock inputs on each capacitor 180° out of phase with the other. The removal of the even harmonics slightly relaxes the filtering requirements of any subsequent low-pass filters needed to suppress the harmonics.

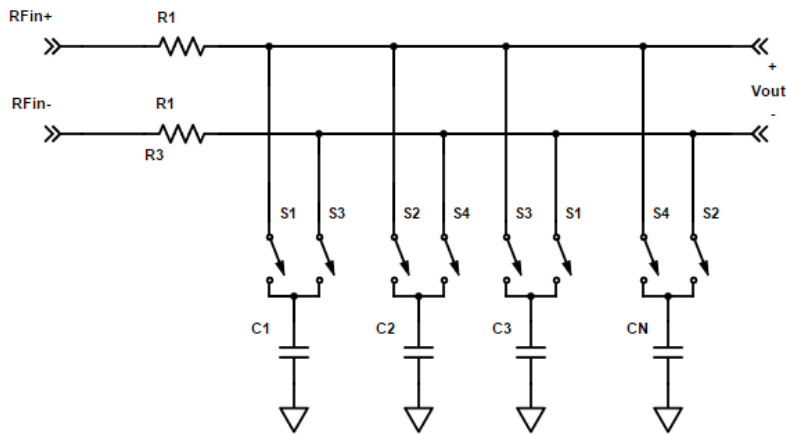


Figure 10. Differential 4-path filter (duty cycle = 0.25)

3.2.2. Harmonic Folding

The N-path filter's poor harmonic rejection performance is one drawback of the filter, however, in practice a low-pass filter is able to remove these odd harmonics at any stage in the signal path. The bigger issue regarding the N path filter is its harmonic folding behavior. This phenomenon can be easily understood by considering the fundamentals of sampling theory.

At its core, the N-path filter behaves like a sample-and-hold circuit. When the input signal's frequency matches f_{CLK} , the output signal looks like a sine wave sampled at a rate of Nf_{CLK} . When the input frequency exceeds $Nf_{CLK}/2$, aliasing begins to occur. The filter removes the aliased signal if it falls outside of the filter's bandwidth, however, frequencies at $(kN \pm 1)f_{CLK}$ fold over directly onto the fundamental frequency. Once the folding signal folds onto the fundamental frequency, it is indistinguishable from the intended signal. These folding frequency, often referred to as folders, must be removed from the signal path prior to N-path filtering. The harmonic folding is apparent in Figure 11. All of the harmonics at frequencies of $(kN \pm 1)f_{CLK}$ exhibit this folding behavior, but typically only the harmonics for $k=1$ are considered since these frequencies fold back with the greatest power and are closest in the frequency spectrum, making them the most difficult to remove via filtering.

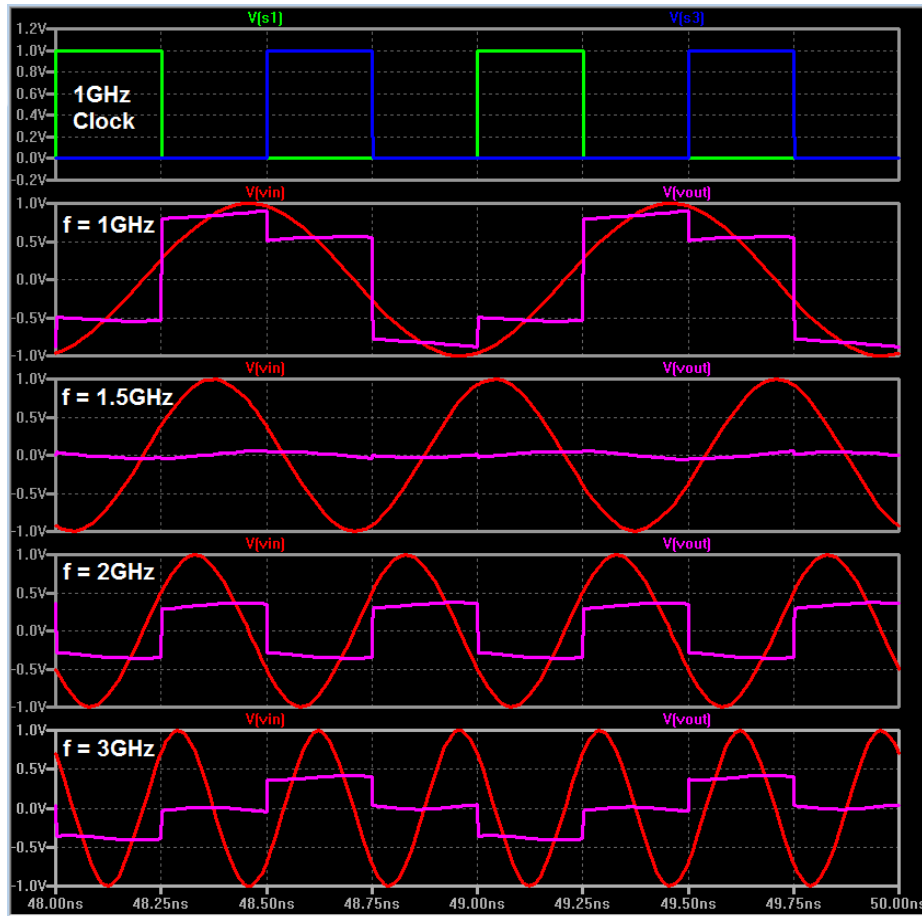


Figure 11. Single-ended 4-path filter outputs at 4 input frequencies. The 2nd harmonic is weakly attenuated, and the 3rd harmonic folds back onto the fundamental. Only two clock phases are shown for clarity. ($R=500\Omega$, $C=12\text{pF}$, $R_{sw}=10\Omega$, $f_{clk} = 1\text{GHz}$).

3.2.3. Limited Out-of-Band Attenuation

Another drawback of the simple N-path filter topology is the limited out-of-band attenuation. The reason for this is apparent when looking at Figure 12. Unlike ideal switches, practical NMOS switches have a non-zero resistance when they are in the conducting state. Because only one switch is ever conducting at any given time, the switch resistance, R_{sw} , can be modeled as a single resistance at the input of N ideal switches.

The output voltage of the filter is measured at the node between the junction between the input resistor, R , and R_{sw} . It is trivial to show that as the input frequency exceeds the

cutoff frequency of the baseband filters, the frequency response approaches a maximum attenuation corresponding to the voltage division between R and R_{SW} [3].

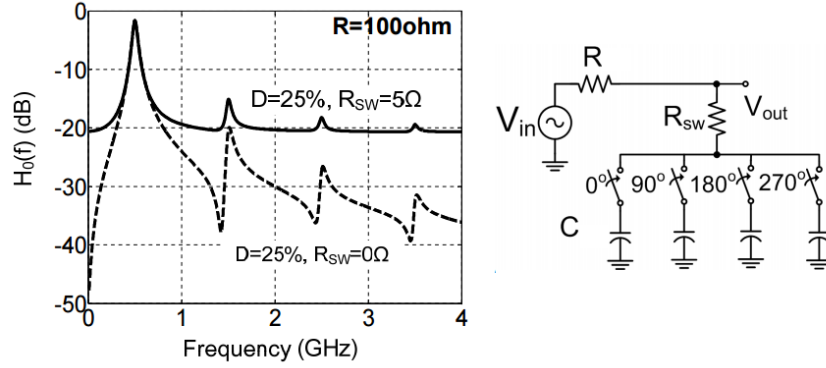


Figure 12. Modeling of non-ideal switches in a 4-path filter. The non-zero switch resistance limits the out-of-band attenuation for the filter's frequency response [3].

$$Max\ Attenuation = \frac{R_{SW}}{R + R_{SW}}$$

Increasing the out-of-band attenuation requires cascading of multiple first-order N-path filters or increasing the width of the switches. Both of these methods require an increase the effective gate capacitance of the switches as seen from the clock generation circuitry. Increasing the gate-source capacitance increases the power requirements of the switch driving circuitry.

$$P = C_{gs} V_{gs}^2 f_{clk}$$

Increasing the input resistance of the filter also improves the out-of-band attenuation, but doing so increases the insertion loss of the filter. Because one of the potential applications of the N-path filter is to be used directly after the antenna, a large insertion loss should be avoided because it adds the potential to attenuate weak signal in the desired band to fall below the system's noise floor.

4. Theory of a Harmonic Rejecting N-Path Filter

4.1. Rejection of Odd-Order Harmonics

4.1.1. The Issue of Harmonic Transfer

The biggest issues facing the simple N-path filters discussed in Chapter 3 are the poor harmonic rejection and the folding of the N-1 and N+1 harmonics onto the fundamental. Using a fully differential circuit removes all even-order harmonics from the frequency response circuit. The harmonic folding behavior can be minimized by selecting a large value for N and preceding the N-path filter with an anti-aliasing filter to remove the folders from the signal path before the mixers fold them onto the fundamental. Increasing N relaxes the filtering requirements of the anti-aliasing filter.

Although folding behavior can be negligible for sufficiently large N, a designer must always consider the poor odd-harmonic rejection when designing an N-path filter because all odd harmonics are present in the frequency response, independent of the value of N. [8] discusses the design of N-path notch filters, which can be implemented by switching the position of the N capacitors and switches with the resistor in Figure 5. N-path notch filters exhibit the same harmonic behavior as the N-path band-pass filters, so they can remove their own odd-harmonics from the frequency response. For example, cascading an N-path band-pass filter, clocked at f_{clk} , with an N-path notch filter, clocked at $3 \cdot f_{\text{clk}}$, allows for the rejection of the 3rd, 9th, 15th, etc harmonics from the band-pass response. This method requires more circuitry and each notch filter only rejects harmonics that share a common denominator between their fundamental frequency and the fundamental of the band-pass filter. Because of this, all odd harmonics that are prime numbers require

a dedicated notch filter to remove them since they have no common denominators. This is especially problematic because the first three odd harmonics (3,5,7) are all prime numbers [5]. This makes the cascaded notch filter method impractical for improving the harmonic rejection of the N-path filter, especially for large values of N.

4.1.2. Harmonic Rejection Mixers

As discussed in Chapter 3.2.1, the N-path filter's harmonic transfer is caused by the odd-order harmonics of the mixing signal. Replacing the square wave mixing waveform with a sinusoidal wave solves this issue in theory, however, mixing with a sinusoidal LO in CMOS requires the use of active mixers. The tradeoff for this improvement in the harmonic rejection is that active mixers have poor linearity, which makes them ill-suited for a flexible SDR receiver design. Ideally, the mixers in the N-path filter design should have the high linearity of a passive mixer with the improved harmonic rejection of a square-law mixer. Passive CMOS mixers are implemented as voltage-controlled switches with a low on-resistance and high impedance in the off state, so the mixers must be driven by square waves. Since passive mixers require square wave driving waveforms, improving the mixer's harmonic rejection requires a method of conditioning the square LO waveform to make it seem more like an ideal sine wave.

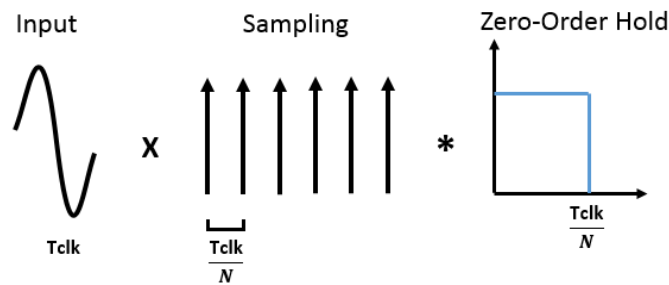


Figure 13. Sample and hold operation of a sine wave in the time-domain

The key concept of the harmonic rejection mixer (HRM) is best understood by considering the frequency response of the sample and hold operation shown in Figure 13. In the frequency domain, passing a sinusoid with a frequency of f_{CLK} with an ideal sampler at a rate of $f_S = Nf_{CLK}$ results in a series of impulses at $(kN \pm 1)f_{CLK}$. The zero-order hold operation holds the sampled value constant for T_{CLK}/N . In the frequency domain, this is expressed as a sinc function with zeros at $2kf_{CLK}$ [7]. The frequency spectrum of the resulting signal is obtained by multiplying the spectral content of the sampled sine wave with the envelope of the sinc function. The resulting spectra is composed of the series of impulses from the sampling operation, whose amplitudes are scaled by the envelope of the sinc function as shown in Figure 14.

When $N=2$, the sinusoid is sampled at the Nyquist frequency, and the filter outputs a square wave, assuming the sample pulse and input signal are in phase. In the frequency domain, the square wave is composed of f_{CLK} and all of its odd harmonics. Increasing N from 2 to 8 increases the sampling rate and eliminates the 3rd and 5th harmonics. In theory, increasing N will always yield improvements in harmonic rejection, however, bandwidth limitations, phase noise as well as component mismatch limit the practical range of N . The practical limitations of N are not explored during the writing of this thesis.

A sampled sine waveform can be generated using a voltage controlled oscillator and a sample and hold circuit, or generated directly from an ADC, however, the LO waveform must be a square wave in order to drive the passive switches.

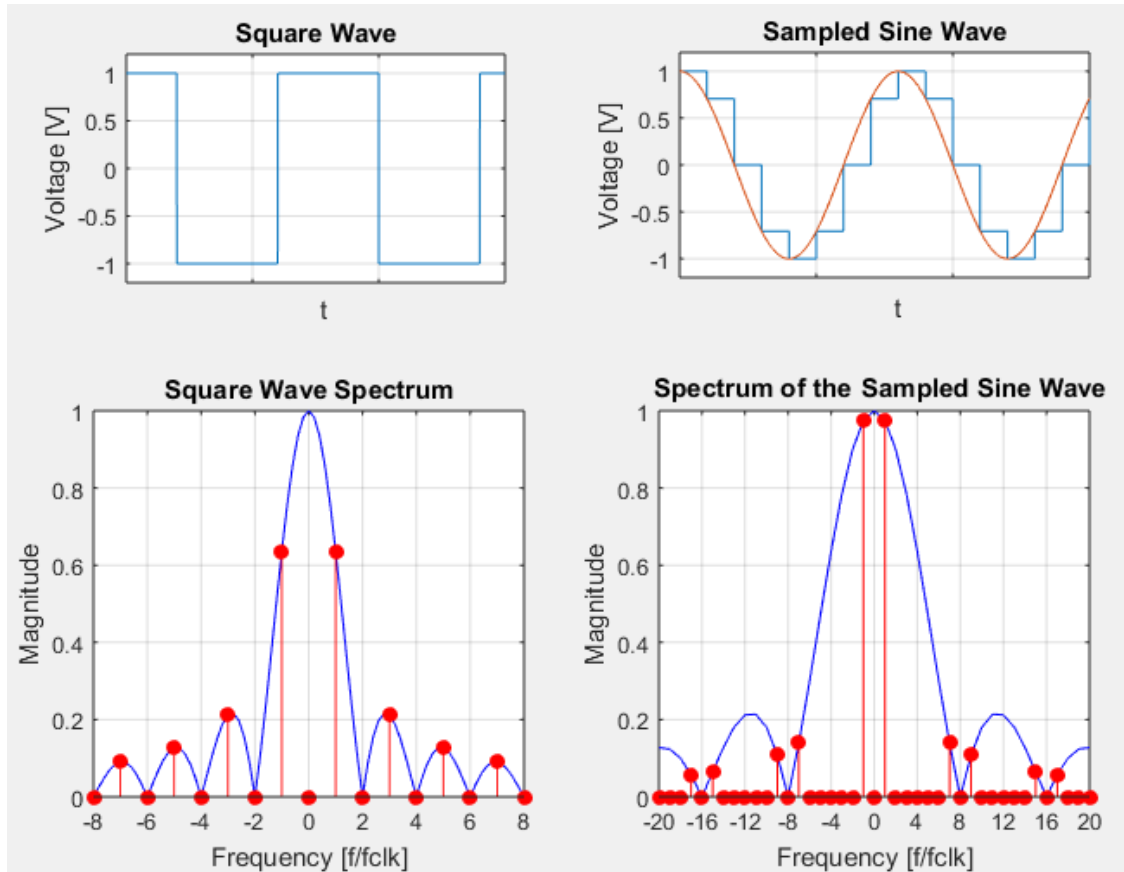


Figure 14. Frequency spectrum of a square wave and sampled a sine wave ($N=8$). Magnitudes normalized to 1 for clarity. Both signals have a fundamental frequency of f_{clk}

In practice, HRMs make use of amplitude scaled, phase-shifted square waves in order to approximate the shape of the sampled sine wave. The phase shift between each square wave is $360^\circ/N$ for a sine wave sampled at Nf_{CLK} . The amplitude weighing coefficient, G_n , corresponds to the magnitude of a sine wave on the active edge of the corresponding phase [6]. The G_n coefficients for an 8-phase HRM are shown in Figure 15.

One possible implementation of an HRM is shown in Figure 16. In this case, the LO waveform is a series of non-overlapping pulses with a duty cycle of $1/N$, and each value of G_n corresponds to the value of each sample of the sampled sinusoid. This structure closely resembles the simple N -path filter discussed in Chapter 3 with the key difference of each path having a different scaling factor. This HRM has N separate paths and takes

the place of the down-conversion mixer in the original filter. A passive harmonic rejection N-path filter using this HRM technique was designed in [5] and requires N^2 mixers and amplitude scaling circuits in order to operate.

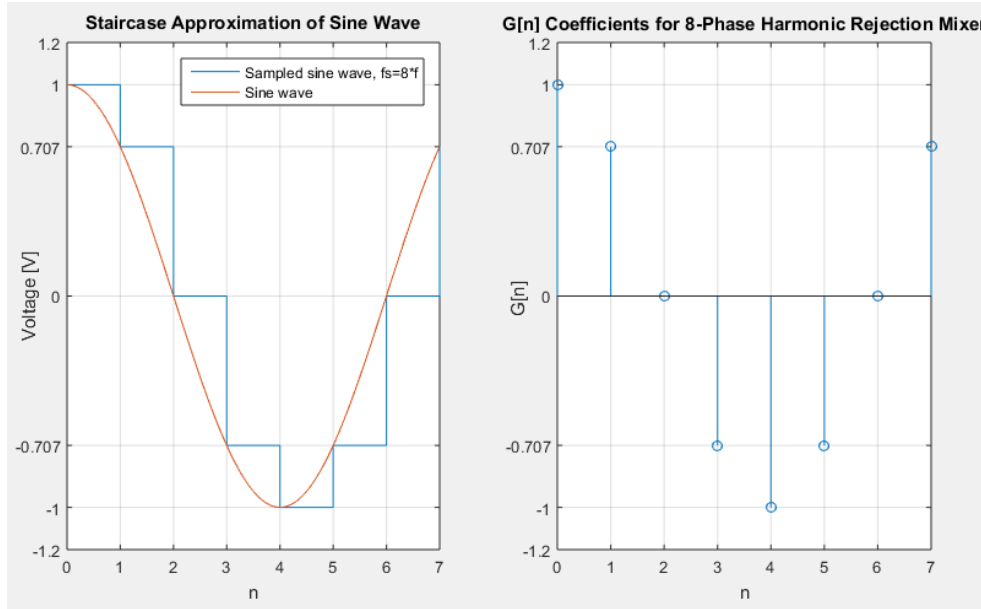


Figure 15. Sine wave after a sample and hold operation. The relative amplitude of each sample make up the weighing functions for each phase of the HRM

Looking at the G_n coefficients in Figure 15, some simplifications can be made in the clocking method in order to reduce the amount of hardware needed. It is apparent that for even N , $G_n = -G_{n+N/2}$ and $\phi_{n+N/2} = \phi_n + 180^\circ$. These weighing coefficients can be combined into a single block by increasing the duty cycle of the square wave to 50%. The rising edge of the clock now corresponds to G_n and the falling clock edge allows for the scaling factor

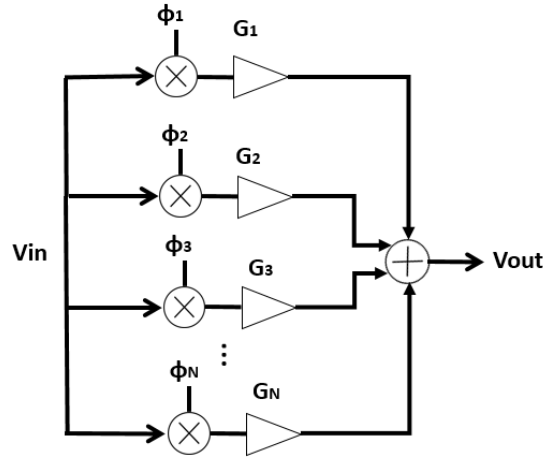


Figure 16. Basic implementation of a HRM for an arbitrary N. Duty cycle = 1/N

Increasing the duty cycle from 1/N to 50% cuts the number of parallel paths needed for harmonic rejection in half. This method is illustrated in Figure 17 for N=8. Four clock signals 45° out of phase with each other can generate a staircase approximation of a sinusoid. The switching of each square wave in both directions corresponds to a new sample taken of the prototype sine wave [6]. The value of each weighing coefficient G_n determines the relative step size between each new sample from the staircase-approximated sine wave rather than the absolute magnitude as was the case for the 1/N duty cycle HRM.

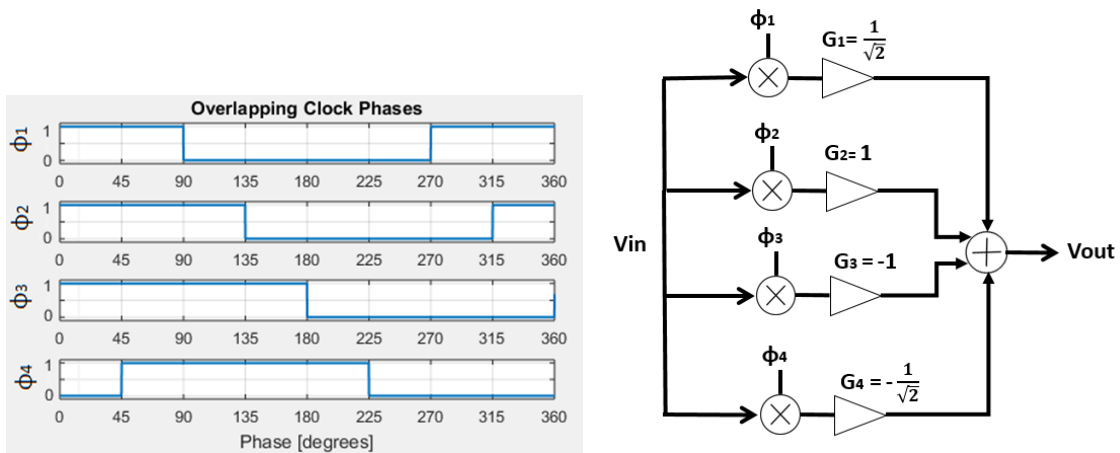


Figure 17. Harmonic rejection mixers can use overlapping clock phases with a 50% duty cycle to reduce the number of paths needed to achieve harmonic rejection (N=8, 4 phases shown).

The resulting staircase approximated sine wave resulting from the harmonic rejection mixing function is shown in Figure 18. The step size between each sample matches the weighing coefficients of Figure 17. The staircase approximated wave reaches its maxima when only ϕ_1 and ϕ_2 are high, and it reaches its minima when only ϕ_3 and ϕ_4 are high. When all of the clock phases are high, the waveform reaches zero.

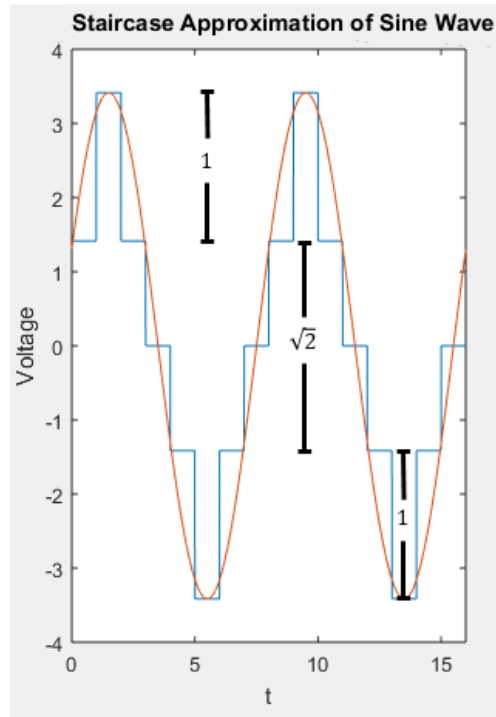


Figure 18. Staircase approximation of a sine wave by summing 4 scaled and shifted square waves. For even N, half of the coefficients are negative. For these coefficients, the negative input is applied to the corresponding phase of the HRM, assuming the input is differential. Ignoring the sign of the negative coefficients maintains the same scaling factor for the staircase approximated sinusoid, but introduces a DC offset in the LO waveform. A DC offset on the LO increases the RF feedthrough to the mixer output. If the N-path filter's baseband filter's cutoff frequency is significantly lower than the lowest clock frequency, the baseband filter may be sufficient to block any RF feedthrough. The best practice,

however, takes advantage of a fully differential input to minimize feedthrough. A practical realization for the HRM is shown in Figure 19. For simplicity, a single-ended output is shown, but all circuit implementations are assumed to be fully differential due to the even harmonic rejection that a fully balanced filter provides

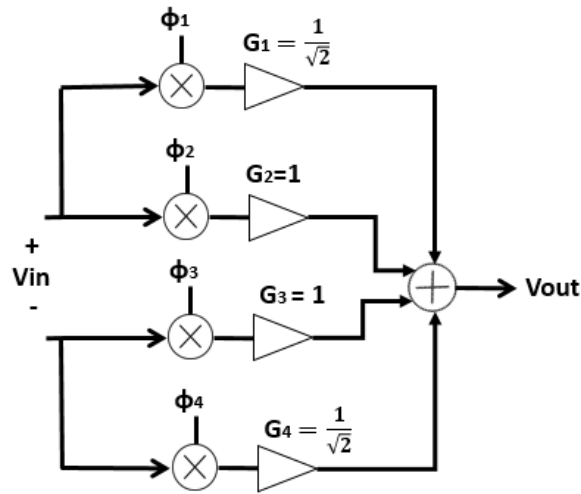


Figure 19. Basic implementation of a differential-input, single output HRM. $N=8$

The poor harmonic rejection of the original N -path filter results from the initial down-conversion mixing operation. Using the HRM structure in Figure 19 suppresses the 3rd and 5th harmonic so any IF created between those frequencies and the staircase approximated LO will be attenuated by the baseband filter in each path. The up-conversion operation can then be conducted by a simple MOS switching mixer prior to the construction of the output signal.

4.2.Addition of Outputs

After each of the baseband signals is up-converted back to high frequency, the output signals from each path need to be added together. For the original N -path filter, the addition of the N paths is accomplished by shorting the outputs together, however, this is

only possible for a non-overlapping clock structure. If the clock phases overlap, charge sharing occurs between each of the paths, degrading the isolation between the paths. If the up-converted outputs are not buffered, this overlap will cause the up-converted signals from each path to be down-converted backwards through the adjacent paths, which results in undesired distortion at the output. This challenge is discussed in [5].

4.2.1. Summing Voltages

One straightforward method of adding voltages is using the simple op amp circuit shown in Figure 20. The output voltage for this summing amplifier is given as.

$$V_{out} = -(V_1 + V_2 + \dots + V_N)$$

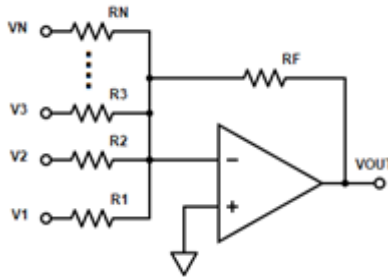


Figure 20. Active summing amplifier using an op amp

The advantage to the op amp summing amplifier is the simplicity of its design and its relatively good linearity. Unfortunately, this circuit is impractical for use at the high frequencies required by the receiver due to the high unity gain bandwidth requirements of the op amp in order to perform the addition at frequencies exceeding 1GHz. The bandwidth can be improved somewhat by reducing the gain of this summing amplifier below 0dB by selecting $R_1 > R_f$. This may not be practical, however, when implementing an active N path filter with a large N . As the number of parallel paths increases, the closed loop amplifier requires more loop gain to maintain the same bandwidth, so more

attenuation is needed. Due to the tradeoff between bandwidth and attenuation, op amp voltage summing is not further considered in this paper.

4.2.2. Averaging Voltages

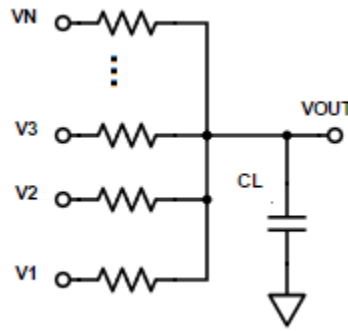


Figure 21. Passive addition of outputs by averaging

A different method of recombining the output signals is by connecting them together using resistors like shown in Figure 21. If each of the resistor values are matched, the output voltage will be the average of each of the individual voltages. This method provides two key benefits. If implemented as physical resistors, the resistors require no additional power to operate and provide the best linearity possible, however, the performance benefits come at a cost. If the resistor values are selected to be too small, the passive averaging circuit will load the baseband amplifiers, which causes attenuation of the output signal. This problem can be circumvented by using larger resistors, however, large-value resistors contribute more thermal noise to the output. Also, the resistors used to perform the averaging form a low-pass filter with the load capacitance, so selecting large-value resistors limits the bandwidth of the system based on the load capacitance. The poor noise performance of this method is discussed in [5] and is not further considered in this paper.

4.2.3. Summing Currents

After ruling out active addition using a feedback amplifier and passive averaging of voltages, another option for adding the phases together is converting the voltages to currents and summing them together. This can be done using operational transconductance amplifiers (OTAs) like shown in Figure 22. Current-mode addition is much easier to achieve than voltage addition because currents can be added in parallel by shorting the outputs of the OTAs together. The currents can then be converted to an output voltage by driving a small resistive load.

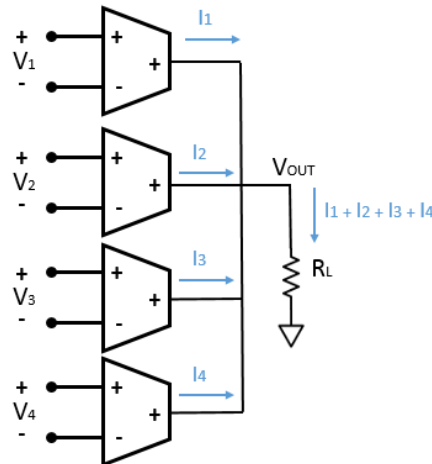


Figure 22. Summing of currents using parallel transconductance amplifiers

The circuit in Figure 22 can easily be scaled to accommodate more filter paths by adding more OTAs in parallel. One disadvantage of this method is that the amplifiers operating in the open loop makes them more sensitive to device mismatch than feedback amplifiers. Mismatch between the g_m of each OTAs can cause distortion in the output although this can be minimized using good layout techniques. In addition, many OTA circuits have poor linearity compared to op amps and resistors. Due to the OTA current summing circuit's scalability and good isolation between paths, this thesis focuses on this method of adding the outputs of each path.

5. Harmonic-Rejection N Path Filter Circuit Design

5.1. Telescopic Operational Amplifier

5.1.1. Design Requirements

The op-amp in the N-path filter design is used to provide the baseband filtering as well as provide the gain for the baseband waveforms. The desired filter response for the band-pass filter has a bandwidth of 7MHz for use in unused TV bands between 470-700MHz. This corresponds to a -3dB cutoff frequency of approximately 3.5MHz for the baseband filter. An op-amp with a unity gain bandwidth of approximately 200MHz is sufficient to ensure that there is enough loop gain to provide up to 20dB gain at the edge of the bandwidth after accounting for process variation. Using standard 130nm CMOS processes, this specification is difficult to achieve using the standard 2-stage op-amp topology due to the presence of two parasitic poles in the signal path. Instead, the two op amp topologies considered are the folded-cascode and telescopic op amp circuits shown in Figure 23.

The telescopic op-amp has two internal nodes in the signal path, X and Vout. Since the input of the cascade stage, X, is low-impedance, the telescopic amplifier has only one dominant pole due to at Vout, which optimizes the speed of this topology. However, the common mode levels of the input and output nodes must be different in order to keep the transistors in saturation, which limits the voltage swing of the amplifier.

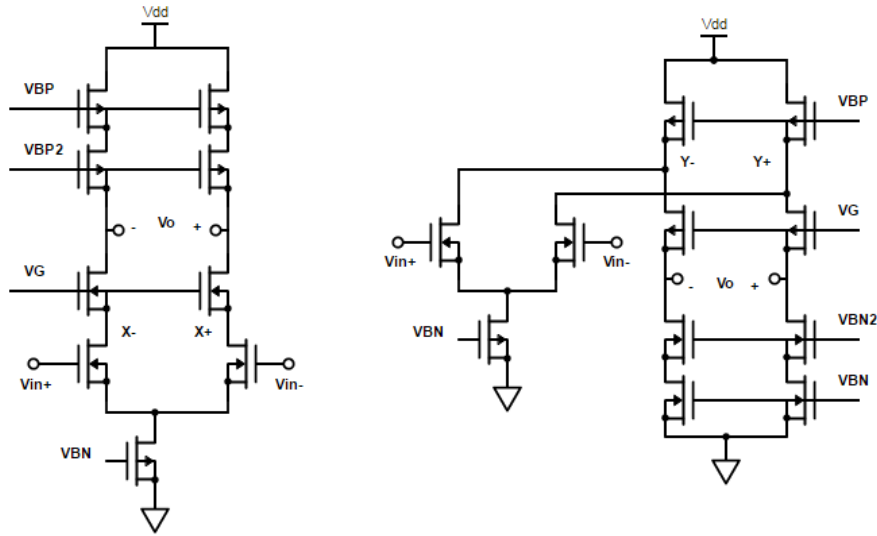


Figure 23. Telescopic (left) and folded cascode (right) op amp circuits

The folded-cascode amplifier decouples the common-mode level of the output from the input common-mode level, increasing the potential voltage swing of the op amp. The folded-cascode topology presents two issues regarding its use for the N-path filter. The third branch in the folded-cascode op amp requires current to flow. Because the op amp is used four times in the final filter design, any additional current requirements are quadrupled as well. Another disadvantage of the folded-cascode op amp is the additional noise contribution of transistors at the folding junction, node Y. Improving the folded-cascode's noise performance requires increasing the gain at the folding junction by increasing the R_{out} at node Y. This decreases the frequency of the pole at Y, which degrades the phase margin. Since the active N-path filter precedes and can potentially replace the LNA in the RF front end, care must be taken to prevent unnecessary sources of noise to the circuit.

For this design, the telescopic op amp was selected due to its improved noise performance at high frequency compared to the folded-cascode. The common-

drain buffer allows for the input and output stages to have the same common mode level to minimize DC currents resulting from common-mode mismatch. In addition, a fully differential op amp structure of the op amp doubles the effective output swing which makes up for the limited swing inherent to the telescopic op amp topology.

5.1.2. The Telescopic Op Amp

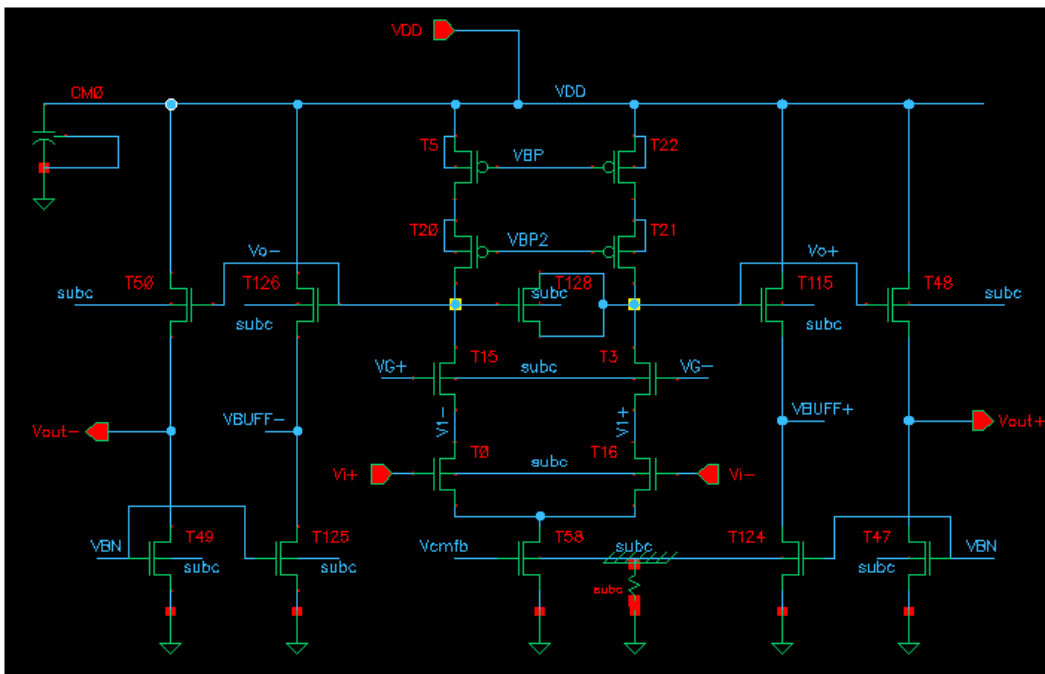


Figure 24. Telescopic op amp schematic with two common-drain buffers

Table 1. Transistor sizes and DC operating point of the core telescopic op amp circuit

[Redacted due to NDA agreement]

The core telescopic op amp circuit is displayed in Figure 24. This core circuit is designed as a standard gain-boosted telescopic op amp topology. The gate voltage of the NMOS current source is driven by a common-mode feedback (CMFB) loop (not shown). The transistors in the common-source and common-gate stages are sized at double the unit transistor length to reduce nonlinear short-channel effects.

Ideally, the op amp should have both high bandwidth, high linearity and low noise. Biasing the transistors in the strong inversion region where $V_{GS} > V_{TH}$ optimizes speed and linearity. Noise performance is optimal in subthreshold operation where $V_{GS} < V_{TH}$. For this thesis, the telescopic op amp is biased in moderate inversion, where $V_{GS} \approx V_{TH}$ and all transistors are operating in the saturation region. This strikes a compromise between the noise performance of the subthreshold biasing and the linearity of the strong inversion bias [9].

Transistor T128 implements a MOS capacitor between the output nodes of the active load in order to improve the circuit's phase margin. The gates of the transistors used in the common-mode feedback loop (not shown) capacitively loaded the output of the common-drain buffer during initial tests. This reduced the frequency of the secondary pole and reduces the phase margin of the amplifier.

To reduce the impact of this capacitive loading, two separate common-drain buffers are used. The first pair of common drain amplifier lowers the effective output impedance of the op amp to prevent the feedback resistors from loading the output. The second pair of buffers are used as inputs to drive the CMFB loop. This two-buffer technique reduces the capacitive loading of the op amp output, but if the buffers are mismatched, the common mode feedback loop will introduce a common-mode error on the output. To prevent this issue, the both buffers are biased such the overdrive voltage, V_{OV} , is the same for both buffers.

$$V_{OV} = \sqrt{\frac{I_D}{\frac{K}{2}WL}}, \text{ in saturation}$$

The CMFB buffer drives a purely capacitive load, ideally only at DC, so a low output impedance is not necessary, which allows a much smaller current to be used. V_{OV} for the CMFB buffer is designed to match the output buffer's V_{OV} by reducing the transistor width proportionally to the reduction in current with respect to the output buffer. The implemented transistor sizes are displayed in Table 1.

5.1.3. Bias Circuit

The bias circuit for the telescopic op amp is shown in Figure 25. Transistors T131-T134 make up the V_{BE} -based current reference along with a diode-connected BJT and resistor. The diode and resistor degenerate the PMOS current source and the NMOS current mirror regulates the two currents to match the currents in both paths. This circuit forces a V_{BE} voltage drop across the resistor. As long as the resistor is sufficiently large, the current reference forces V_{BE}/R current through both paths.

The telescopic op amp inherently has a low voltage swing potential. Transistors T24-T26 compose the low-voltage cascode current mirror that biases the op amp's active load. This circuit improves the voltage swing of the cascode by biasing T26 on the edge between the linear and active region. This biasing method provides a good tradeoff between R_{out} and maximum output swing.

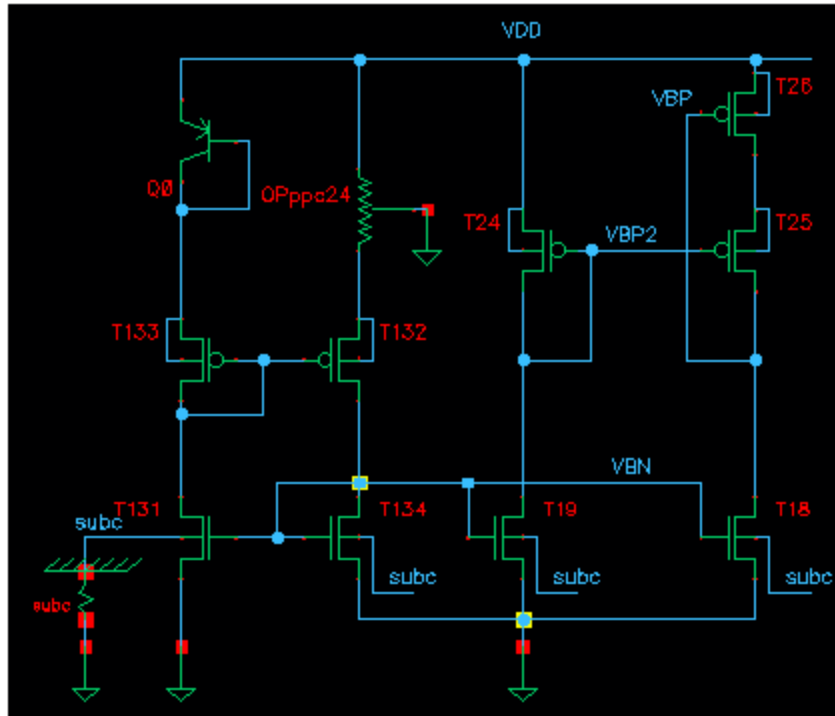


Figure 25. Bias circuit for telescopic op amp
 Table 2. Transistor sizes and DC operating point of the bias circuit
 [Redacted due to NDA agreement]

5.1.4. Common-Mode Feedback (CMFB)

In single-ended op amps, the op amp's feedback loop regulates its common-mode (CM) voltage on the output. The same is not true for differential op amps. The external feedback loops used in differential op amps provide only differential-mode feedback, which is insufficient for stabilizing the op amp's CM level at a fixed voltage.

Under ideal conditions in a simulation, a differential op amp can be biased such that the output common-mode voltage falls at a precise voltage with no CM compensation. In practice, however, it is impractical to regulate the op amp's CM level in an open loop configuration. Modern CMOS fabrication methods are imperfect so the parameters of the NMOS and PMOS transistors are not perfectly

matched, and their threshold voltages are dependent on temperature and subject to the body effect.

For example, consider the op amp in Figure 26 where the NMOS current source, Q_1 , is biased at I_D and the CM output voltage, V_{OCM} , is biased at V_{CM} . Both current mirrors in the active load must then source $I_D/2$. Due to process variation, Q_1 may attempt to drive I_D as well as an additional offset current, ΔI_D . If ΔI_D is positive, V_{DS} on Q_4 and Q_5 increase in order to compensate for the increased current draw through the active load, which decreases V_{OCM} . The active load has a fairly large R_{out} , so even small offset currents may cause large increases in V_{OCM} , forcing Q_2 and Q_3 into the triode region. Conversely, if ΔI_D is negative, V_{OCM} increases and Q_4 and Q_5 are pulled into the triode region. In either case, current mismatch between the current source and active load decreases the amplifier's gain and reduces its linearity [11].

To alleviate this biasing issue, differential op amps need a common-mode feedback (CMFB) loop in order to stabilize the common-mode level within the common-mode range. The CMFB loop consists of a common-mode detector and a differential amplifier as shown in Figure 26. If the output voltage of the amplifier is differential, the common-mode detector averages the differential signal and outputs V_{OCM} . The amplifier in the CMFB loop senses the common-mode error between V_{OCM} and the desired common-mode level, V_{CM} , and then adjusts the bias voltage on Q_1 . The feedback loop stabilizes the bias of the amplifier at a state where $\Delta I_D=0$ and $V_{OCM}=V_{CM}$.

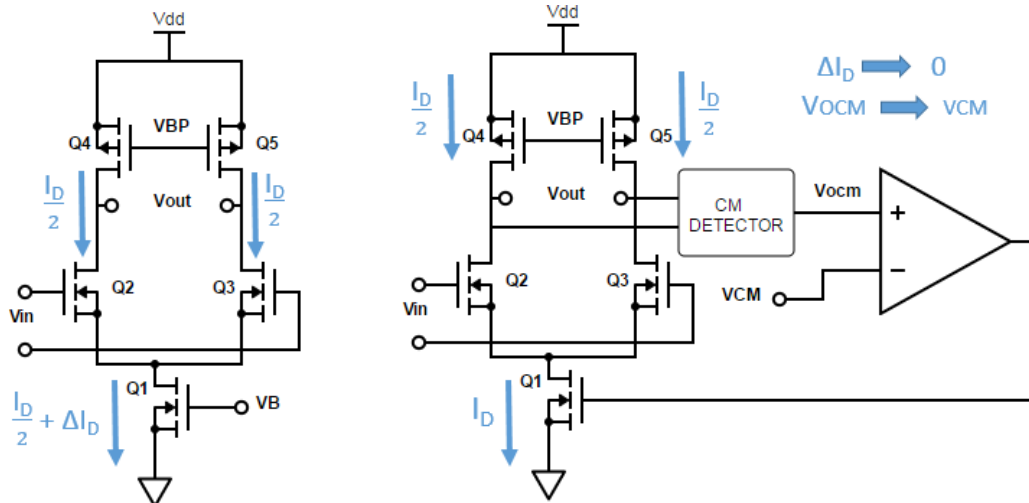


Figure 26. Single stage differential amplifier without common-mode feedback (left) and with common-mode feedback loop (right)

The simplest method of detecting the common-mode level is by connecting the output terminals together using two resistors. The voltage at the node connecting the two resistors is the average, or common-mode voltage. This resistive common mode detector loads the amplifier if small value resistors are used, which decreases amplifier's DC gain. Large value resistors take up a lot of area on the chip, and contribute thermal noise to the amplifier, making a resistive common-mode detector impractical for a low-noise amplifier design. Active CM detection circuits use common-source or common-drain buffers to prevent loading the output, at the cost of reduced linearity [11].

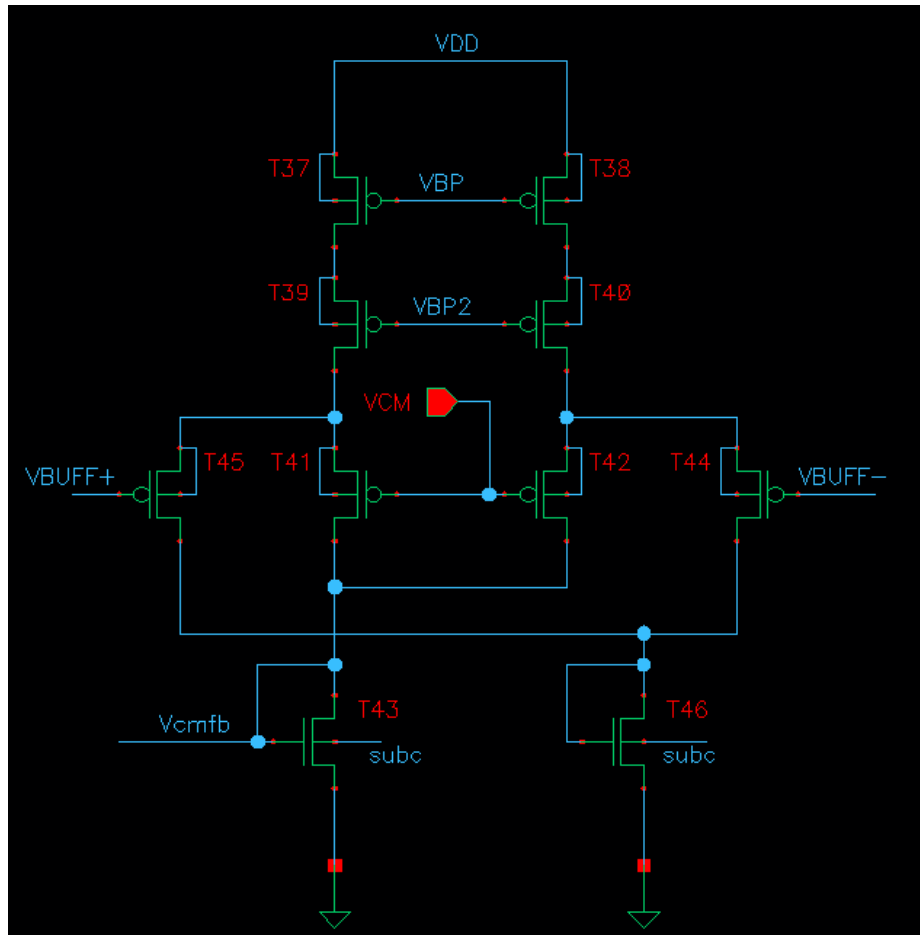


Figure 27 Common-mode feedback circuit for telescopic op-amp
 Table 3. CMFB circuit transistor sizing

[Redacted due to NDA agreement]

The CMFB circuit used for the telescopic op amp in Figure 27 resembles a pair of differential pairs with their outputs shorted together. The transistors at the input of the CMFB circuit have a transconductance of g_{m0} . The diode-connected FETs at the output present a small resistive load at the drains of the differential pair. If the op amp's output is differential and the input transistors are perfectly matched, the CMFB circuit integrates the sum of the buffered differential output voltages, V_{BUFF} , which eliminates the AC component of the output signal, and only the CM component remains.

The transistor sizes for the implemented CMFB circuit are shown in *Table 3*. The feedback loop was tested under typical conditions and all four corners to ensure that the CM level is stable under all conditions. For each case, the simulated CM level falls within 15mV of the targeted CM voltage.

Table 4. Common mode feedback circuit performance ($V_{cm} = 0.5V$)

[Redacted due to NDA agreement]

5.1.5. Gain-Boosting Stage

Typically, high-gain op amps rely on cascaded gain stages to achieve higher gain, whereas high speed op amps are designed as a single stage amplifiers with short channel lengths and high currents [10]. Gain boosting is a common technique used to overcome the inherent gain limitation in the single stage cascoded op amp.

$$Av = g_m R_{out} || R_{Load}$$

$$GBW = \frac{g_m}{C_{LOAD}}$$

Based on the equation for voltage gain, it is apparent that increasing the DC gain of an op amp requires increasing either g_m or R_{out} . Changing g_m also changes the gain bandwidth product so the best way to increase the gain of an op amp with a fixed gain-bandwidth requirement is to increase R_{out} . For a cascode amplifier, the simplest way to increase R_{out} is to stack multiple cascode stages, however, for low-voltage CMOS, there is generally insufficient voltage headroom for this method to be practical.

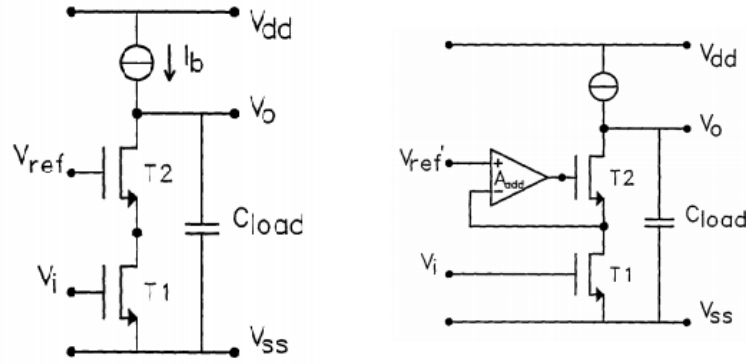


Figure 28. Simple cascoded gain stage (left) and gain-enhanced cascode (right) [10].

The R_{out} for the simple cascode in Figure 28 can be calculated as follows.

$$R_{OUT} = (g_{m2}r_{o2} + 1)r_{o1} + r_{o2}$$

The gain boosting architecture shown in Figure 28 drives the cascode transistor with an amplifier to reduce the sensitivity of the drain current on V_o . If V_o increases, T_2 will attempt to draw more current. However, if V_{GS1} is fixed, an increase in current requires V_{DS1} to increase. The amplifier senses this change in V_{DS1} and lowers the gate voltage on T_2 to regulate the drain current. This feedback decouples the output voltage from the drain-source junction between T_1 and T_2 . This corresponds to an increase in R_{out} , based on the amplifier gain, A .

$$R_{OUT} = (g_{m2}r_{o2}(A + 1) + 1)r_{o1} + r_{o2}, [10]$$

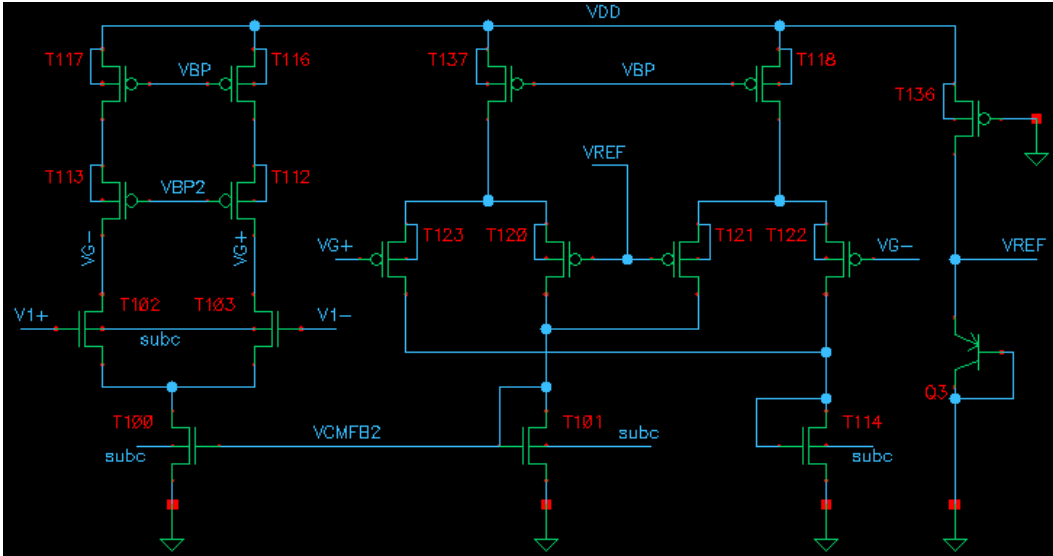


Figure 29. Gain-boosting stage with second common-mode feedback loop

The implemented gain-boosting stage along with its CMFB loop are shown in Figure 29. The circuit closely matches the core telescopic amplifier circuit in Figure 24, but without the NMOS cascode stage. The inputs and outputs of the gain-boosting circuit are connected to the source and gate terminals of the NMOS cascode in Figure 24, respectively. The lack of a cascode stage reduces the R_{out} of the gain-boosting amplifier and limits the bandwidth due to the increased Miller capacitance, which reduces the speed of the gain-boosting amplifier compared to the core op-amp circuit. The reduced speed of the gain-boosting stage is acceptable as long as its unity gain bandwidth exceeds the frequency of the dominant pole for the core amplifier [11].

The MOSFET T136 and diode-connected BJT, Q3, make up the 0.75V reference for the gain-boosting stage's CMFB loop. This simple reference voltage is fixed and is insensitive to changes in the supply voltage, which limits its practicality for different supply voltages. A more complex voltage regulator is required in order

for the telescopic op amp to operate at VDD levels other than 1.5V. The final transistor sizes for the gain-boosting stage are shown in Table 5

Table 5. Transistor sizes for gain-boosting stage and its CMFB loop

[Redacted due to NDA agreement]

5.1.6. Op Amp Testing

The gain-boosted telescopic op amp's frequency response is shown in Figure 30 and Figure 31. The fully implemented design has a DC gain of 60dB, 61° phase margin and a unity gain bandwidth of 294MHz as shown in Table 6.

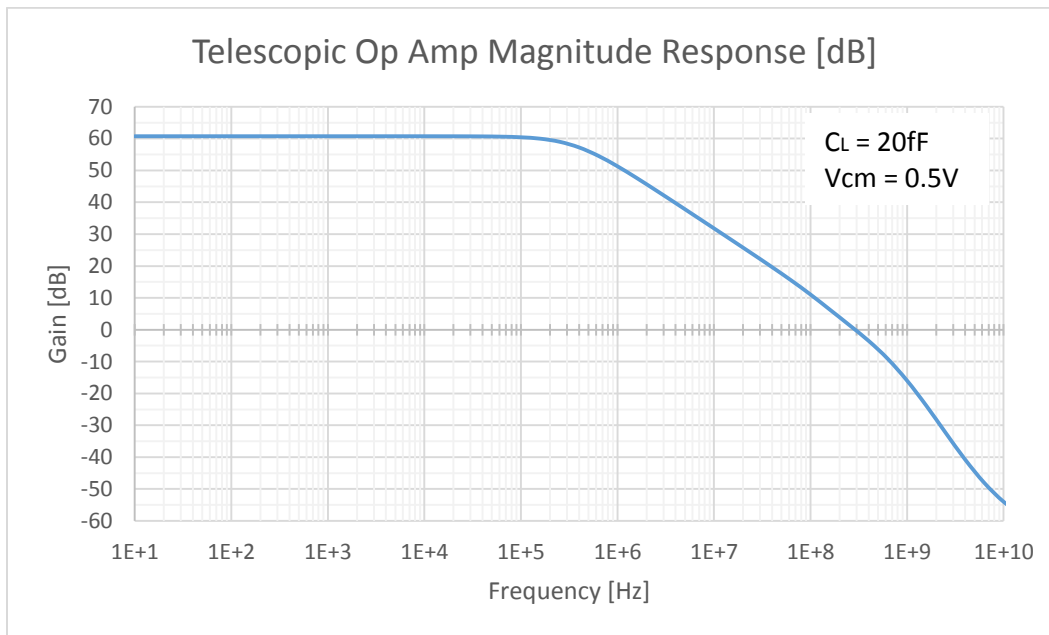


Figure 30. Telescopic Op Amp Magnitude Response

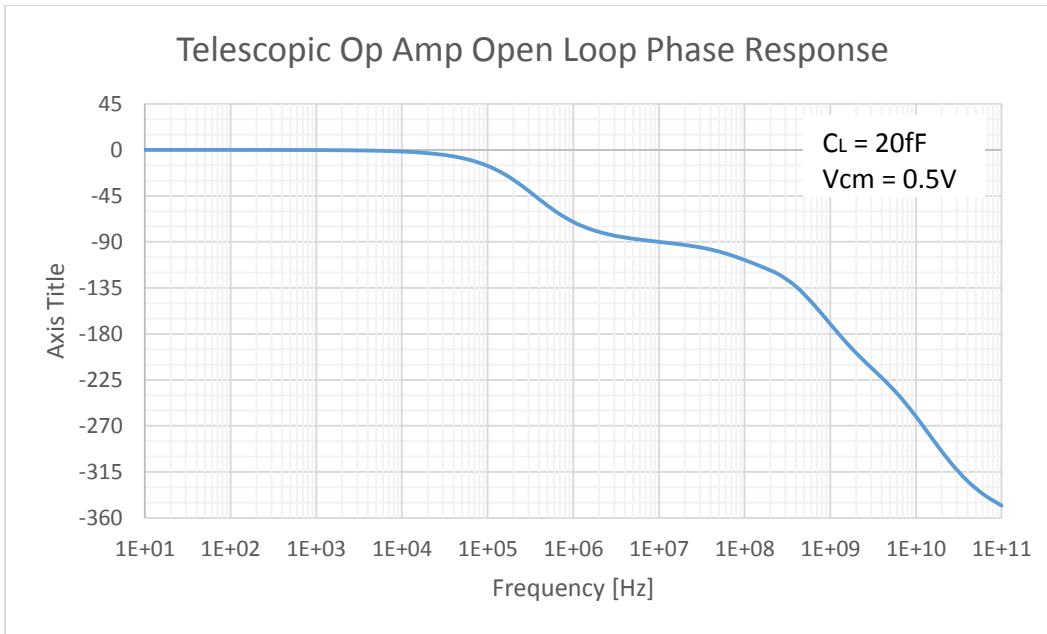


Figure 31. Telescopic Op Amp Open Loop Phase Response

Table 6: Simulated Telescopic Op Amp Specifications

Specification	Value	Unit
Supply Voltage	1.5	V
Supply Current	730.5	μA
Common-Mode Voltage Range	0.42 – 0.86	V
Output Resistance	315	Ω
DC Gain	60.7	dB
Unity Gain Bandwidth	294	MHz
Phase Margin	61.7	degrees
Gain Margin	23.86	dB

5.2.Mixer Circuits

Passive mixers, often called switching mixers are often used for their good linearity and because the output voltage is independent of the LO voltage. As discussed in Chapter 4.1, the 3rd and 5th harmonic can be rejected by adding four amplitude scaled square waves that are 45° out of phase with each other. The amplitude weighing function for each square wave can be achieved through either passive or active means. In [5], the harmonic rejection mixer's weighing function is achieved using scaled resistor values. This is the method used for the active N-path filter designed for this thesis.

A single implemented active N path filter stage is displayed in Figure 32.

Together, the switches and resistors feeding into the op amp inputs make up the harmonic rejection down-conversion mixer. The down-conversion operation is integrated into the op amp circuit, but the switches draw no DC current so the mixing operation is still passive. For an 8-path filter, there are only two positive gain coefficients, $|G_1|=1$ and $|G_2|= 1/\sqrt{2}$. The currents through the input resistor, R_1 , is inversely proportional to the value of R_1 . Because of this, the amplitude scaling is achieved by dividing R_1 for each path by its corresponding weighing coefficient.

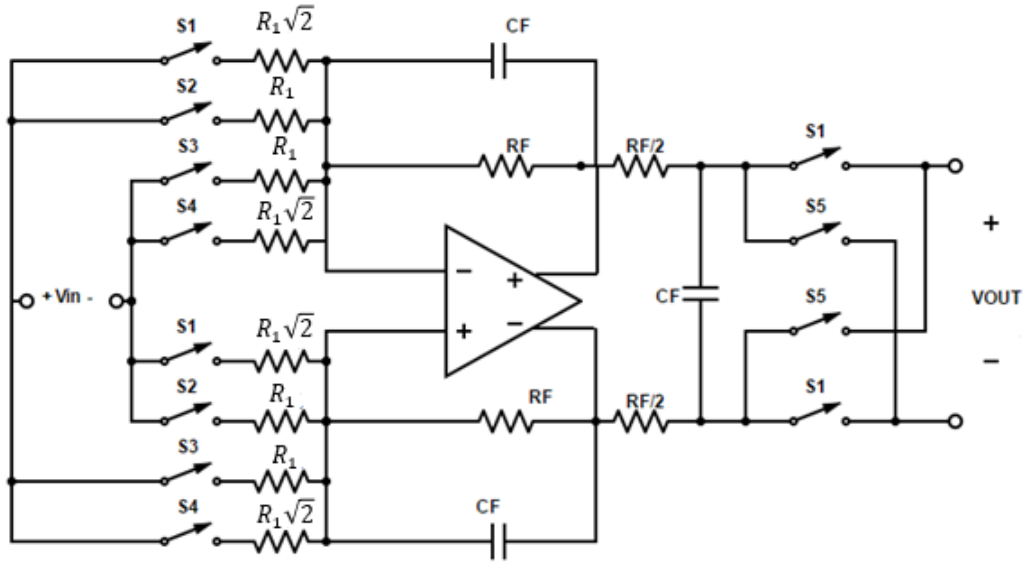


Figure 32. Single phase of the differential active N-path filter.

The active N path filter in Figure 32 differentiates itself from the original N path filter in several key ways. First, the op amp provides voltage gain at baseband, rather than at high frequency, where voltage gain requires higher currents. In addition, the active N-path filter decouples the filter's bandwidth from the value of N. The original N-path filter's bandwidth changes based on the baseband filter components as well as the value of N because the duty cycle varies how long the input resistor sees each baseband capacitor. In this active N-path filter, the baseband capacitors, C_F , are always connected to the load. Because of this, the bandwidth is determined entirely by the value of C_F and R_F in the feedback loop. This makes it slightly easier to redesign the same N-path filter for different values of N.

The op amp structure also provides improves the out-of-band attenuation compared to the original N-path filter. For the original filter, the voltage division between the switch and the input resistor limits the maximum attenuation of the original filter. For the active N-path filter, the switches used for the down-

conversion mixer are in series with the input resistors. The switch resistance provides negligible resistance to the current path as long as $R_1 \gg R_{\text{switch}}$. In addition, because the op amp's output is buffered, an additional low-pass filter is added to the output to provide additional out-of-band rejection.

The R_1 value should be selected to change the gain of the op amp circuit. Large resistor values contribute thermal noise to the output, but for a fixed gain and bandwidth specification, small resistors require larger baseband capacitors to achieve the same bandwidth. In addition, R_1 must be significantly larger than the switch resistance. Failure to account for the switch resistance can introduce gain mismatches between the gain weighing coefficients may occur. This reduces the mixer's harmonic rejection capability.

In general, lower values of R_{switch} are beneficial, but increasing the gate width increases the gate capacitance. This increases the power requirements for the circuit driving the switches. The tradeoff between switch resistance and gate capacitance is shown in Figure 33. A switch width of $30\mu\text{m}$ is selected. This provides a series resistance of 27Ω and a gate capacitance of 20fF . To minimize potential distortion from resistor scaling mismatch, the switch resistance is subtracted from each of the resistor values on the input of the op amp circuits so that the sum of their resistances is properly weighted to reject the 3rd and 5th harmonics.

[Redacted due to NDA agreement]

Figure 33. NMOS switch resistance and capacitance versus gate width

The active N-path filter can be arranged as eight parallel paths consisting of the circuit in Figure 32 with each path's clock phases shifted 45° . Since the filter is fully differential, the design can be simplified. The square wave LO waveforms used in path 5 are 180° out of phase with the LO waveforms used in path 1. The output voltage of paths 5 is then the output voltages of path 1 multiplied by -1. Because of this, the 8-path filter can be implemented using four fully differential paths. One limitation of condensing the filter into only four paths using the circuit in Figure 32 is that the number of active switches is not constant over time. This results in a change in the filter's input impedance based on how many switches are on at a given instant. If the N-path filter is connected directly after the antenna, this change in input impedance may cause undesired time-dependent reflections on the transmission line, which can corrupt the signal. This can be avoided by including a second down-conversion mixer to each op amp circuit, clocked with a complementary LO signal. This is shown in Figure 34 and ensures that the number of active switches is constant.

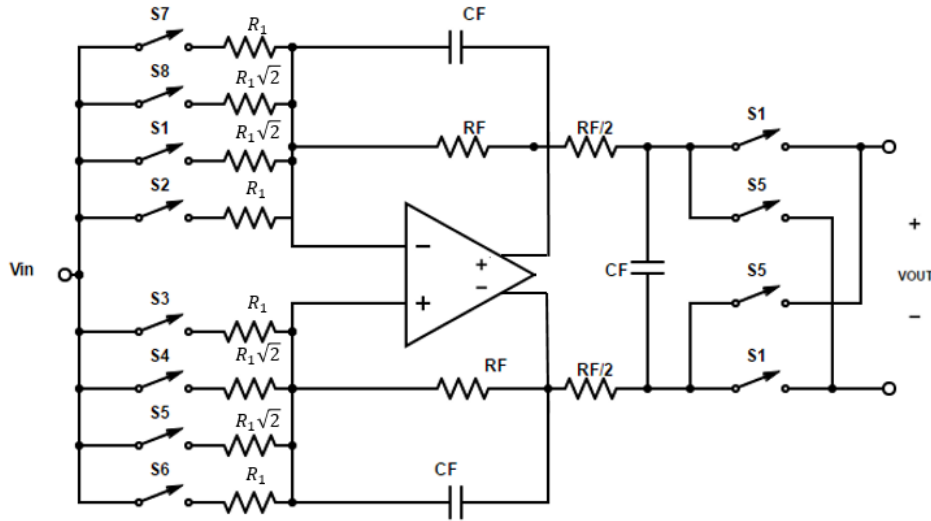


Figure 34. Adding a complementary harmonic rejection mixer on the input. For clarity, only the positive input is shown.

The up-conversion mixer is made up of two pairs of NMOS switches. The transistors are clocked differentially to double the voltage swing on the output. In addition, the differential clocking ensures that the outputs never reach a high impedance state where the load capacitance is unable to fully discharge as the switches open. The final component values for the down-conversion and up-conversion circuits are shown in Table 7. After the input signal is down-converted, filtered, and then up-converted in each path, a summing amplifier is needed to combine the outputs from each path to regenerate the signal.

Table 7. Component values for the op amp mixer circuit

Parameter	Value
R1	1.3kΩ
Rf	6.5kΩ
CF	4.9pF
NMOS Switch Width	[Redacted due to NDA agreement]

5.3.Current-Mode Summing Amplifier

5.3.1. Operational Transconductance Amplifier

As discussed in Ch4.2, high frequency filters can be implemented using operational transconductance amplifiers and capacitors. Transconductance amplifiers operate in an open loop configuration, which makes them useful for high frequency applications.

One of the simplest CMOS transconductance amplifiers topologies available is the simple CMOS inverter in Figure 35. The simple inverter is often used as a high frequency transconductor due to the simplicity of its design and its lack of internal nodes. In [12], Nauta notes that a transconductance element with no internal nodes has no parasitic poles or zeros, and thus its bandwidth is dependent entirely on its output capacitance.

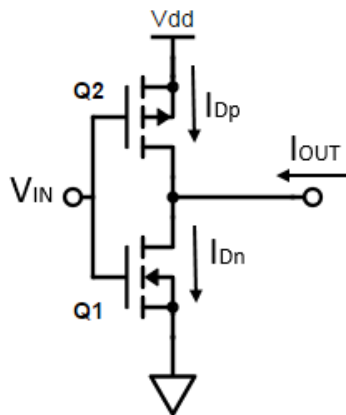


Figure 35. The CMOS inverter, the simplest transconductance amplifier

The transconductance of the simple inverter can be determined based on the IV characteristics of its component FETs operating in strong inversion in the saturation region.

$$I_{Dn} = \frac{k_n}{2} (V_{GSn} - V_{Tn})^2 \quad I_{Dp} = \frac{k_p}{2} (V_{GSp} - V_{Tp})^2 \quad (\text{in saturation})$$

$$I_{out} = I_{Dn} - I_{Dp}$$

$$G_m = \frac{dI_{out}}{dV_{in}} = (k_n - k_p)(V_{in} - V_{tn}) + k_p(V_{DD} - V_{Tn} + V_{Tp}), [12]$$

If the process conduction parameters for the NMOS and PMOS FETs are mismatched, that is if $k_n \neq k_p$, then the transconductance of the CMOS inverter becomes nonlinear. This 2nd order nonlinearity can be eliminated by using a fully differential implementation using matched inverters like shown in Figure 36.

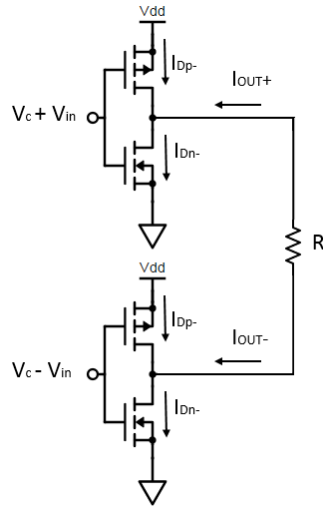


Figure 36. Differential inverter implementation

It can be shown that taking the output current differentially, $I_{OUT} = I_{OUT}^+ - I_{OUT}^-$ removes the nonlinear components of the inverter's transconductance, despite mismatches in k_n and k_p . V_C corresponds to the bias voltage where the input voltage and output voltage are at the same common-mode level.

$$G_{m,diff} = (V_{DD} - V_{Tn} + V_{Tp})\sqrt{k_n k_p}, [12]$$

$$V_C = \frac{V_{DD} - V_{Tn} + V_{Tp}}{1 + \sqrt{\frac{k_n}{k_p}}} + V_{Tn}, [12]$$

The differential inverter configuration is shown to have good linearity, but this is only true when the MOS transistors are operating in strong inversion and in saturation. CMOS inverters have very high gain, which makes them ideal for switching rapidly in digital circuits, but the high voltage gain limits the linear range of the inverter for use in analog circuits. Applying a large input signal forces the NMOS or PMOS into the triode region, and in addition, small offsets in the common-mode input level will cause the output to rail. Adding a feedback resistor, R_F , between the input and output of the inverter mitigates both issues.. The feedback stabilizes the inverter's bias voltage at V_c based on the relative drive strength of the NMOS and PMOS FETs used. In addition, R_F reduces the inverter's unloaded voltage gain by reducing its output resistance from $R_{OUT,P} || R_{OUT,N}$ to $R_{OUT,P} || R_{OUT,N} || R_F$, which improves the inverter's linearity. The linearity improvement comes with a tradeoff of simultaneously decreasing the input and output resistance of the transconductor, both of which are undesirable for transconductance amplifiers.

An alternative method of controlling the differential inverter-based OTA's voltage gain and common-mode level is using the Nauta OTA topology shown in Figure 37.

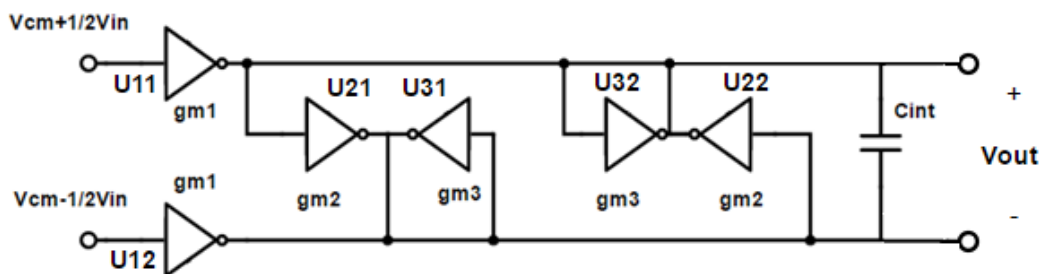


Figure 37. Nauta operational transconductance amplifier circuit made up of six inverters [12] Inverters U31 and U32 have their outputs shorted to their inputs, which stabilizes the output's common-mode level. These inverters behave as active voltage dividers with an equivalent resistance of $1/G_{m3}$. The positive output voltage, V_{out}^+ , can be calculated as follows.

$$V_{OUT}^+ = \frac{-G_{m1}V_{in}^+ + G_{m2}(V_{OUT}^-)}{G_{m3}}$$

It can be shown that the gain of the Nauta OTA varies depending on whether the input is differential or unbalanced. For common mode signals, the input transconductors, U11 and U12, are loaded by an equivalent resistance of $1/(g_{m2}+g_{m3})$. For differential mode signals, the equivalent load resistance is $1/(g_{m3}-g_{m2})$ as shown in Table 8.

Table 8. Common-mode and differential-mode active load resistance for the Nauta OTA

Signal Type	Load Resistance
Common-Mode	$\frac{1}{G_{m2} + G_{m3}}$
Differential-Mode	$\frac{1}{G_{m3} - G_{m2}}$

Good common-mode control is achieved by designing G_{m2} and G_{m3} to be significantly larger than g_{m1} . Changing the relative values of g_{m2} and g_{m3} tunes the differential-mode. In [12], Nauta notes that very high DC differential-mode gains can be achieved by selecting $G_{m2} > G_{m3}$ to load the transconductance amplifier with a negative resistive load. For the purpose of making a linear summing amplifier, however, a small load resistance is preferred to preserve the linearity of the N-path filter.

5.3.2. Summing Amplifier

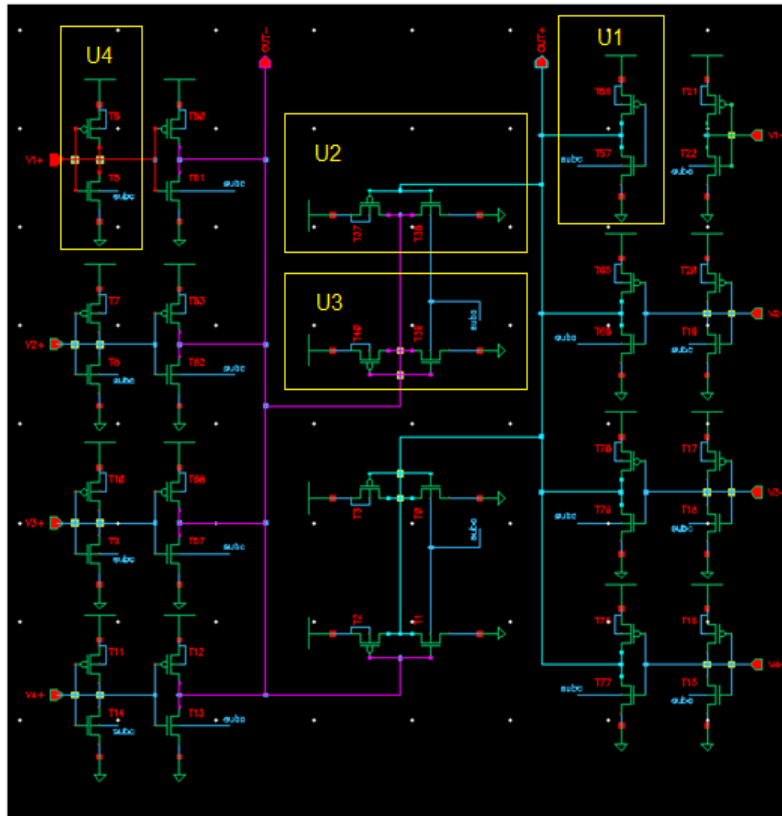


Figure 38. OTA summing amplifier schematic.

An OTA based summing amplifier is implemented as four parallel Nauta OTAs with their outputs shorted together. Because each of the active loads are in parallel, the load transistors from each amplifier can be combined into a single transistor with its width scaled up by a factor of four. The implemented summing amplifier is shown in Figure 38. The transistors are sized to be biased at 0.7V, however, because the circuit does not feature a common-mode feedback loop, the value of V_c is sensitive to process variation. V_c changes by up to $\pm 0.25V$ due to device mismatch. To resolve this issue, another inverter, U1, is connected to each inverter with its input connected to its output. U1 is sized to have the same V_c as the other inverters in the circuit with a decreased current draw to ensure that the input voltages are biased at V_c to ensure linear operation. Placing the inverters in

the same spatial region on the chip should be sufficient to prevent significant mismatch between the inverters. The inputs to the summing amplifier are AC coupled with 60fF capacitors.

5.3.3. Test Results

The DC operating point of the summing amplifier and transistor sizes are displayed in Table 9. Figure 39 shows the magnitude response of the summing amplifier with the input voltage applied to a single input. The amplifier exhibits 2.2dB insertion loss and has a -3dB cutoff frequencies at 120MHz of 1.74GHz.

Table 9. Transistor dimensions and DC operating point of summing amplifier ($V_C = 0.7V$)
[Redacted due to NDA agreement]

The summing amplifier passes all corner test cases and maintains good linearity at each corner as long as the input is biased at V_C . The amplifier has a linear range of 98.3mVpp as shown in Figure 40. A summary of the summing amplifier specifications is shown in Table 10.

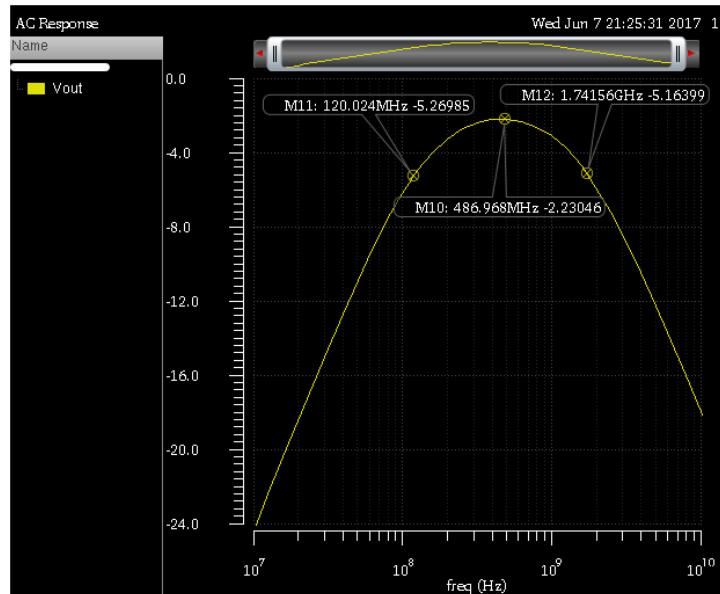


Figure 39. Magnitude response of the ac coupled summing amplifier with a single input applied

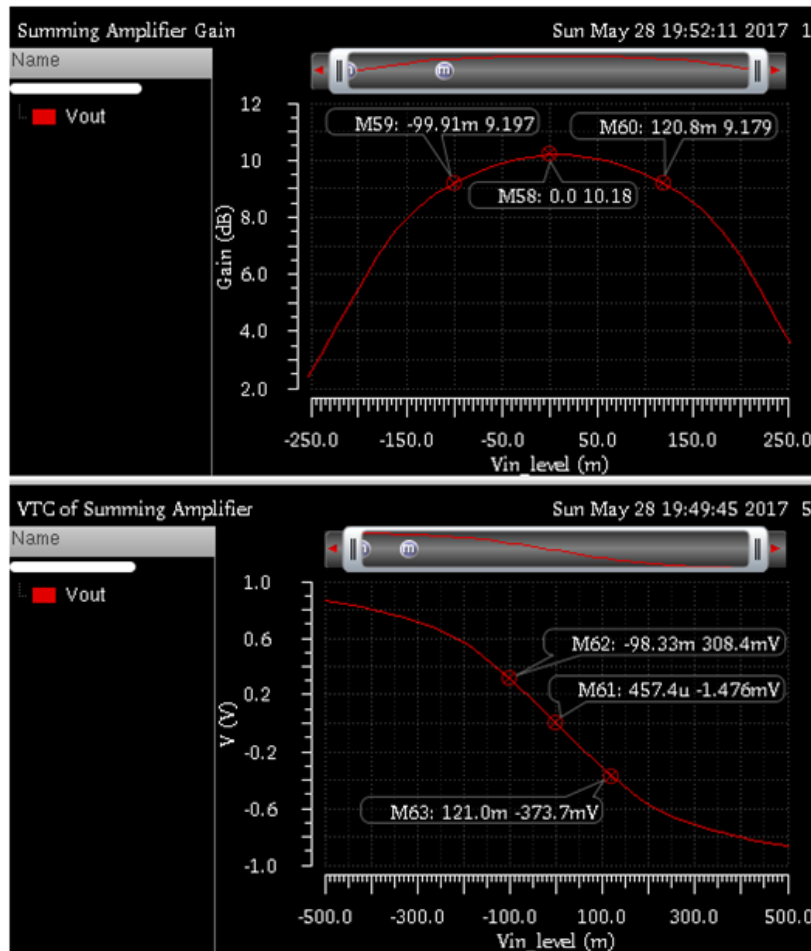


Figure 40. Voltage transfer characteristic and gain of the summing amplifier with all inputs shorted together. All voltages are expressed as peak-peak values. $V_C = 0.7V$

Table 10. Summing amplifier specifications

Specification	Value	Unit
Supply Voltage	1.5	V
Gain	-2.2	dB
Common-Mode Voltage, V_C	0.7	V
Center Frequency	480	MHz
-3dB Bandwidth	1.62	GHz
Worst-case Input Linear Range	98.3	mV _{PP}
Supply Current	2.52	mA
Power	3.78	mW
Common-Mode Rejection Ratio	28.2	dB

5.4. Multiphase Clock Generator

The harmonic rejection mixers requires a minimum of four differential clock phases (eight phases total) in order to reject the 3rd and 5th harmonic. This requires that each clock phase be 45° out of phase with the adjacent clock phases. This can be accomplished by using a voltage controlled ring oscillator. The harmonic rejection capability of the harmonic rejection mixers, however, is dependent on having precise phase shifts between each of the mixer paths as discussed in [3]. The simple ring oscillator has poor phase noise performance because the variance of the clock jitter increases as a function of time. Two alternative methods of generating the multiphase clock are shown in Figure 41.

The first method of reducing phase noise involves using a delay locked loop (DLL). The ring oscillator is replaced by a voltage controlled delay line with N delay elements and compares the final phase of the delay line with the reference clock. The charge pump and loop filter integrate the phase error and output a control voltage to keep the last clock output in phase with the reference clock. This feedback regulates the phase shift between each of the delay elements. This is a flexible, low-power method of generating clock phases, but the feedback loop can cause instability in the circuit.

Alternatively, the overlapping clock phases can be generated by a shift register with N D-Flip-Flops (DFFs). N/2 DFFs are used for a differential architecture. To generate a multiphase clock with frequency, f_{CLK} , a reference clock of frequency $N \cdot f_{clk}$ is divided down by N and applied to the first input of the SR. The

reference clock is applied to the CLK input of each DFF to obtain a $360^\circ/N$ phase shift between each clock phase.

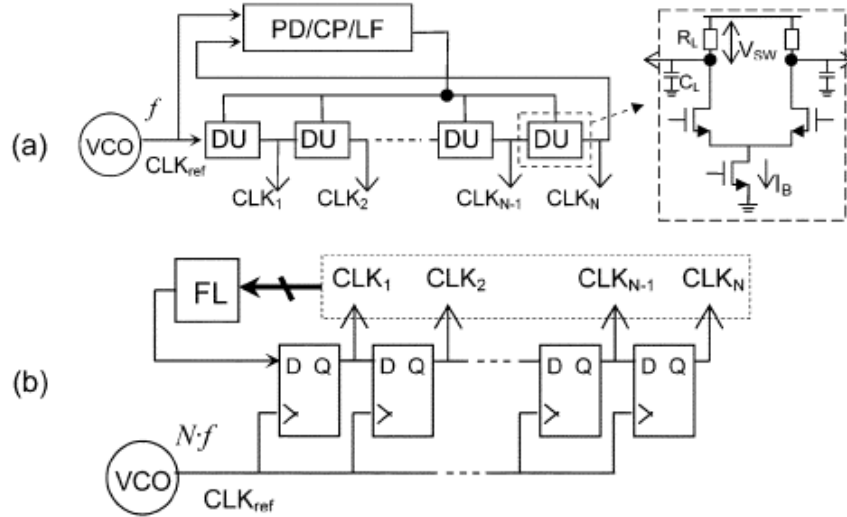


Figure 41. Multiphase clock generation using (a) a DLL and (b) shift registers [14]

The phase noise performance of both clock generation methods are discussed in [14]. For a fixed power budget, the shift register exhibits better phase noise performance than the DLL for a fixed power budget because the shift register does not accumulate phase error between clock phases. The disadvantage of the shift register method is the need for a higher frequency input clock and the relative complexity of frequency dividing by non-powers of two. This thesis paper focuses on the shift register method due to the reduction in phase noise and relative simplicity of designing a radix-2 frequency dividers using CML logic.

5.4.1. CML Shift Register

The core building block of the shift register is the D flip-flop (DFF), which is composed of two CML latches shown in Figure 42. On the clock's rising edge, transistor T5 becomes active and the latch tracks the input logic level. The falling

edge of the clock triggers the start of the latching state. During this period, the cross coupled latch made up of transistors T2 and T3 latch onto the new logic level. Transistors T7 and T8 are biased deep into the triode region so they behave as a resistive load due to their small size relative to real resistors. When the output is logic high, the resistive load pulls the output up to DVDD. The logic low level is a function of the load resistance and bias current.

$$V_{LOW} = DVDD - I_{BIAS}R_{LOAD}$$

The DFF is composed of two identical CML latches cascaded with their CLK input pins swapped. With the fully implemented DFF, the falling edge of CLK sets the second CML latch into tracking mode, which pushes the input to the output of the DFF. The falling edge of CLK will thus be referred to as the active edge throughout the rest of this thesis paper.

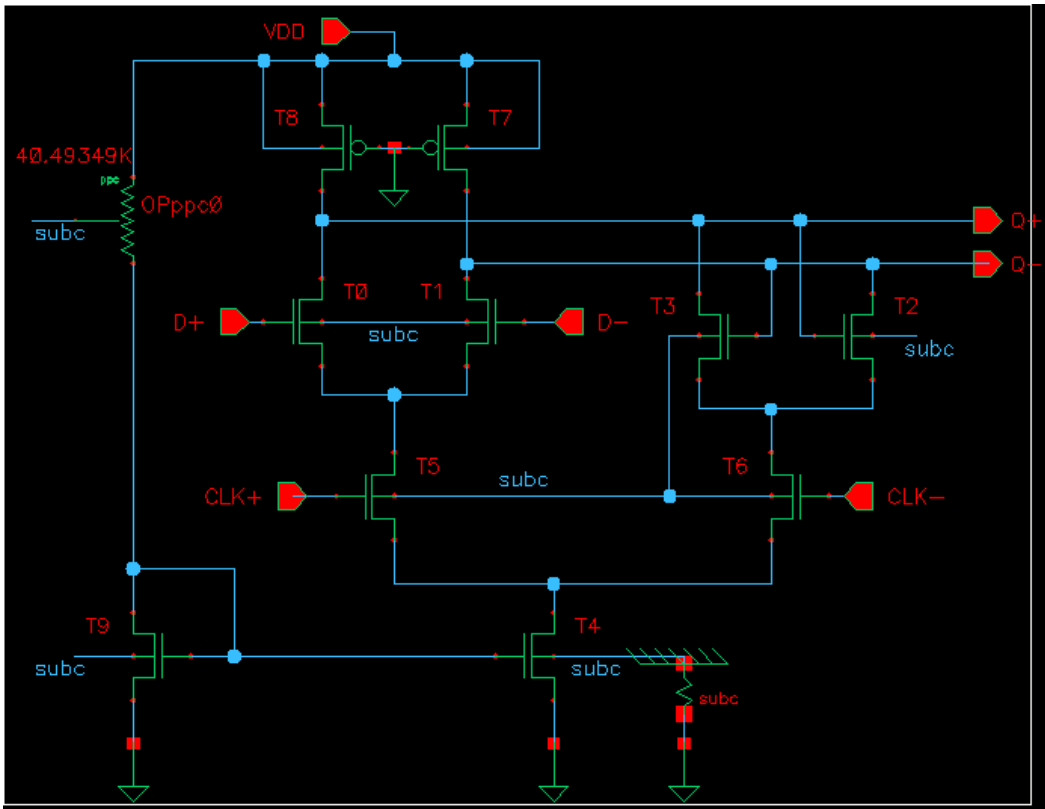


Figure 42. The simple CML latch is the building block for the DFF

Table 11. Transistor sizing for the CML latch used for the shift register

[Redacted due to NDA agreement]

The most critical specifications for the DFF are the propagation delay between the switching clock and output, t_{CLK-Q} , the setup time and the hold time. The test procedures for measuring these values are detailed in [15]. Setup time, t_{setup} , is the minimum time duration that the input data must be stable before the active clock edge in order for the data to be latched correctly. Let Δt_s refer to the time after the switching of the input signal but before the active clock edge. If $\Delta t_s < t_{setup}$, a setup time error occurs and the input is incorrectly latched. If $\Delta t_s \gg t_{SETUP}$, the 50-50 delay time between the active clock edge and the switching edge of the output

remains stable. This stable 50-50 delay time is the nominal t_{CLK-Q} . As Δt_s approaches t_{setup} , the t_{clk-Q} delay time gradually increases. The value of Δt_s that results in a 10% increase in the nominal t_{clk-Q} is the minimum setup time for the purposes of this thesis. The results of the setup time test is shown in Figure 43.

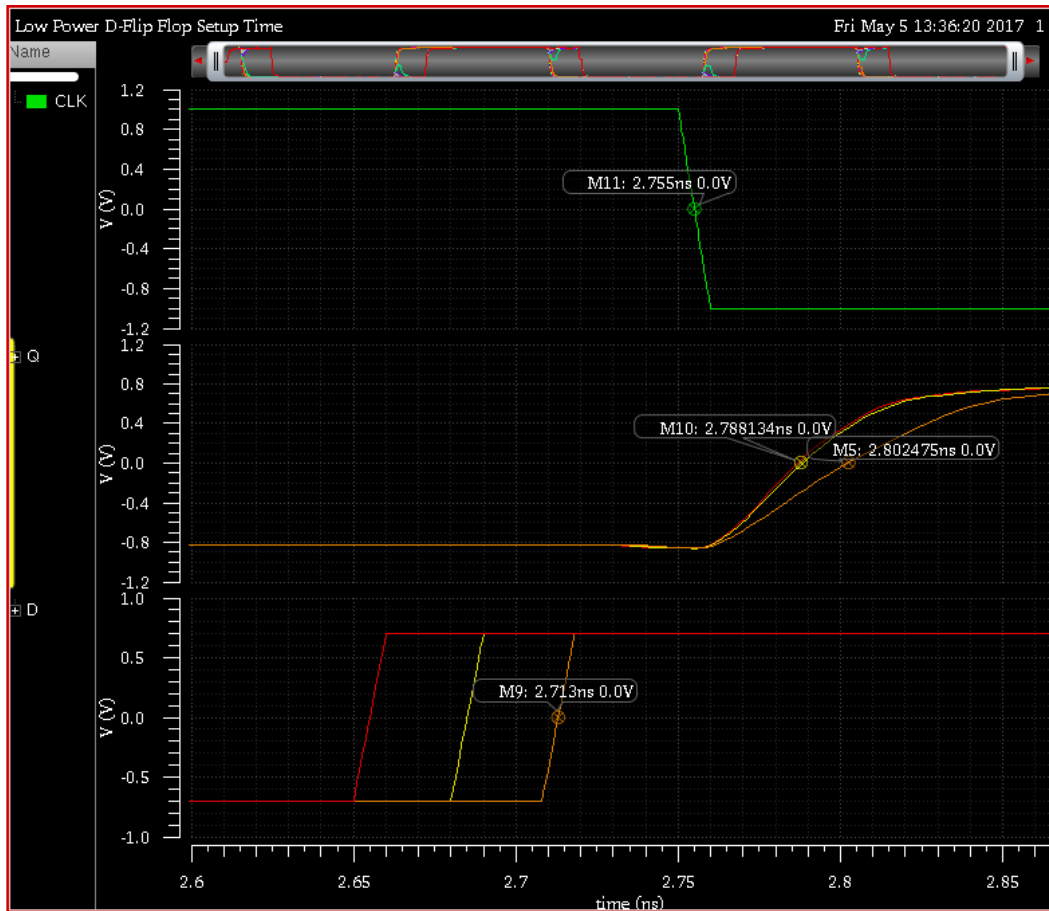


Figure 43 Setup time test waveforms for the CML D flip-flop ($C_L = 5fF$)

Hold time, t_{hold} , is the minimum amount of time after the active clock edge that the input level must remain stable. If Δt_h refers to the amount of time after the clock's active edge and before the switching of the input, a hold time violation occurs when $\Delta t_h < t_{hold}$. Similar to the setup time test, if $\Delta t_h \gg t_{hold}$, the t_{clk-Q} value stays stable at its nominal value. The value of Δt_h that yields a 10% degradation in the nominal t_{clk-Q} delay is the hold time as shown in Figure 44.

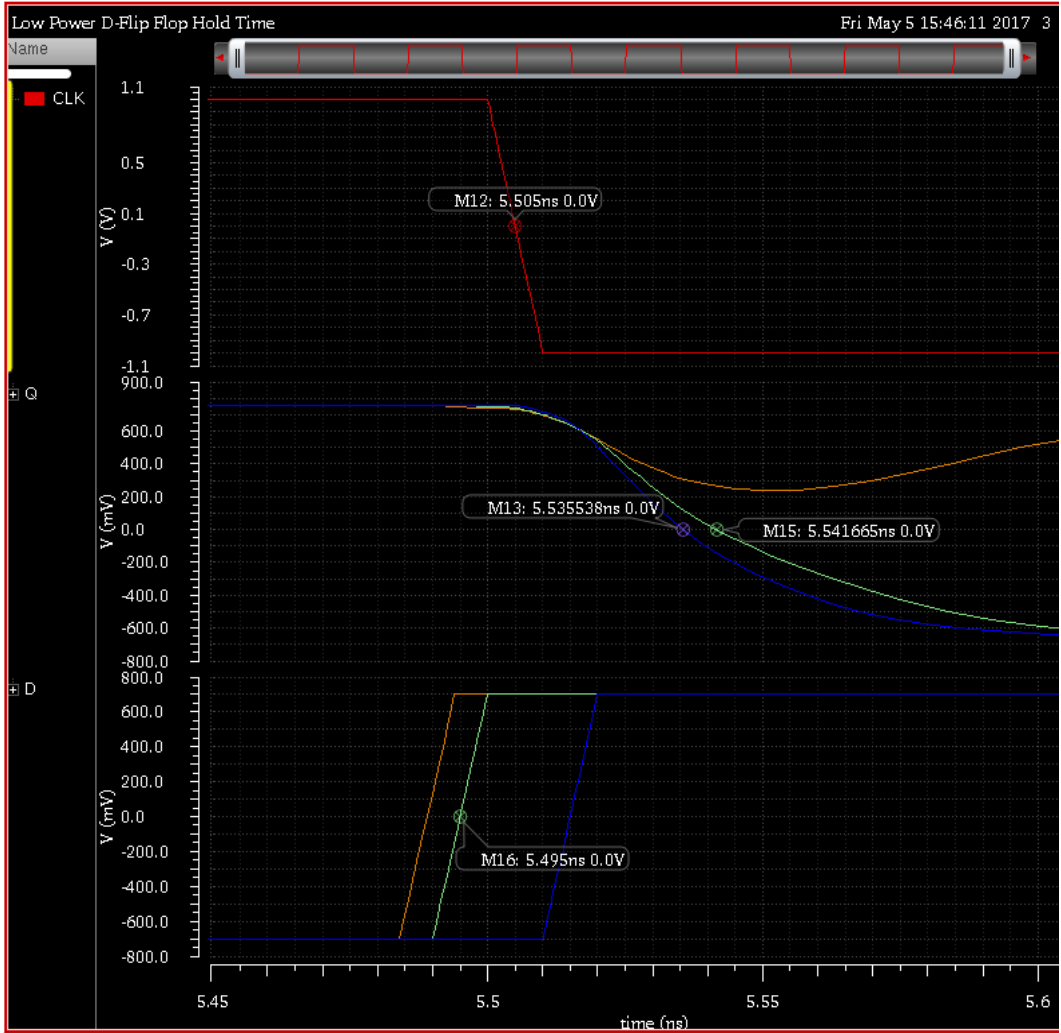


Figure 44. Hold time test waveforms for the CML D flip-flop ($C_L = 5fF$)

Table 12. Performance metrics for CML D-Flip Flop

Specification	Value	Unit
Rise Time	64.4	ps
Fall Time	64.4	ps
T_{clk-Q}	33.1	ps
T_{setup}	42	ps
T_{hold}	-10	ps
Total Current	275.2	μA

5.4.2. High Frequency D Flip Flop

Table 12 shows the performance specifications for the CML D flip-flop. The rise and fall times are both 64.4ps. The N-path filter's maximum operating frequency

is 1GHz, which means that the frequency divider must be able to operate at frequencies up to 8GHz. The latch circuit used for the original CML D flip-flop is not well suited for this high frequency. The parasitic capacitance of the tracking and latch circuits restricts the bandwidth of the DFF. Typically, circuit speed can be improved by increasing the supply current, however, this requires increasing the transistor widths, which in turn reduces the bandwidth of the circuit.

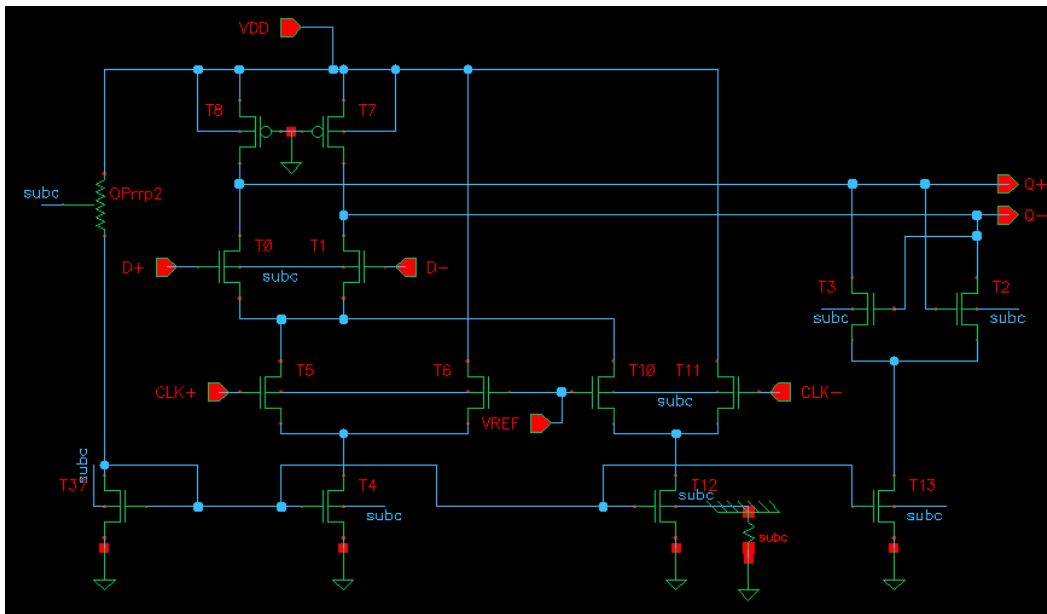


Figure 45. High frequency CML latch [16]

An alternative CML DFF is proposed in [16]. The new latch circuit improves the latch's high speed performance by separating the tracking circuit from the latching circuit. The cross-coupled latch is always active, which decreases the switching times during the tracking mode of operation. This occurs because the output nodes see the latch as negative resistance, which decreases the equivalent resistance at the output nodes. In addition, the latch always being on minimizes current spikes on the falling edge of CLK. The drawback to this topology is the increase in current due to the increase in the number of current paths. To offset

this, the latch current is slightly decreased. The final transistor sizes are shown in Table 13. The setup and hold time measurement procedure is identical to that of the lower frequency DFF and are shown in Figure 46 and Figure 47.

Table 13. Transistor sizing for the high-speed CML latch used for the frequency divider
[Redacted due to NDA agreement]

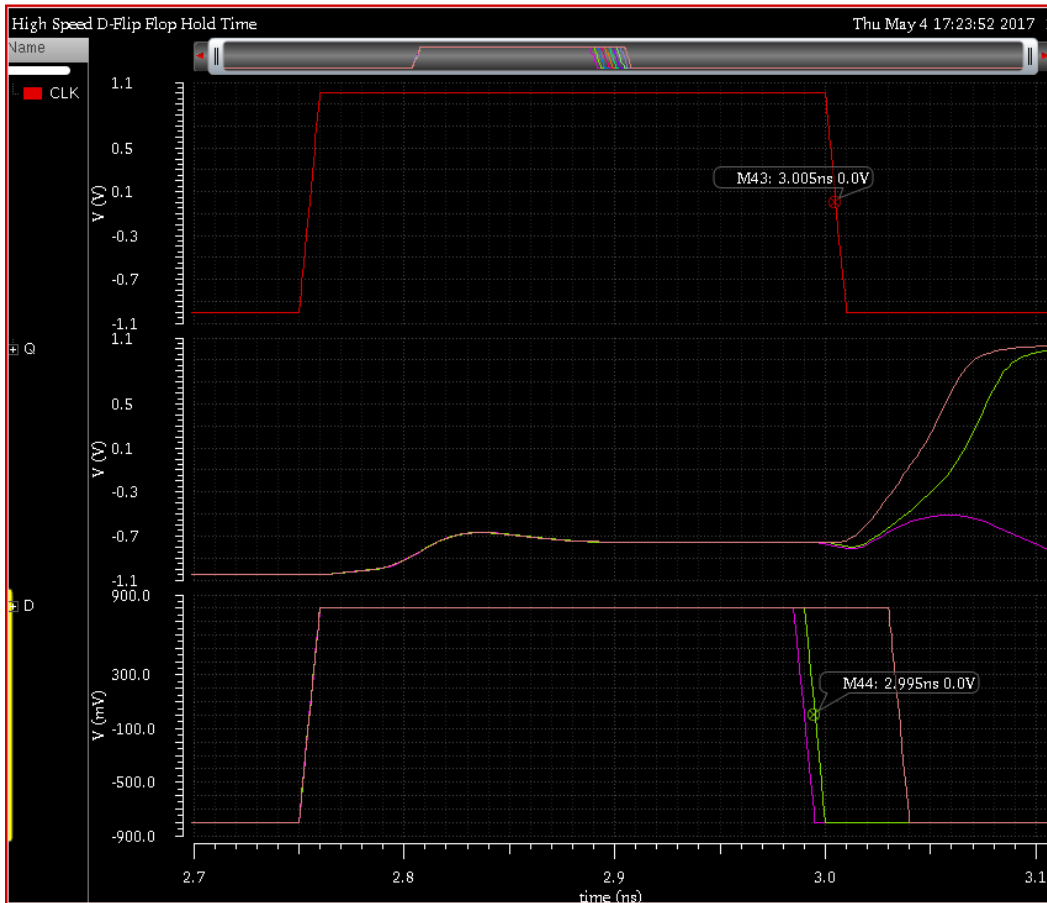


Figure 46. High speed D-Flip Flop Hold Time Measurement

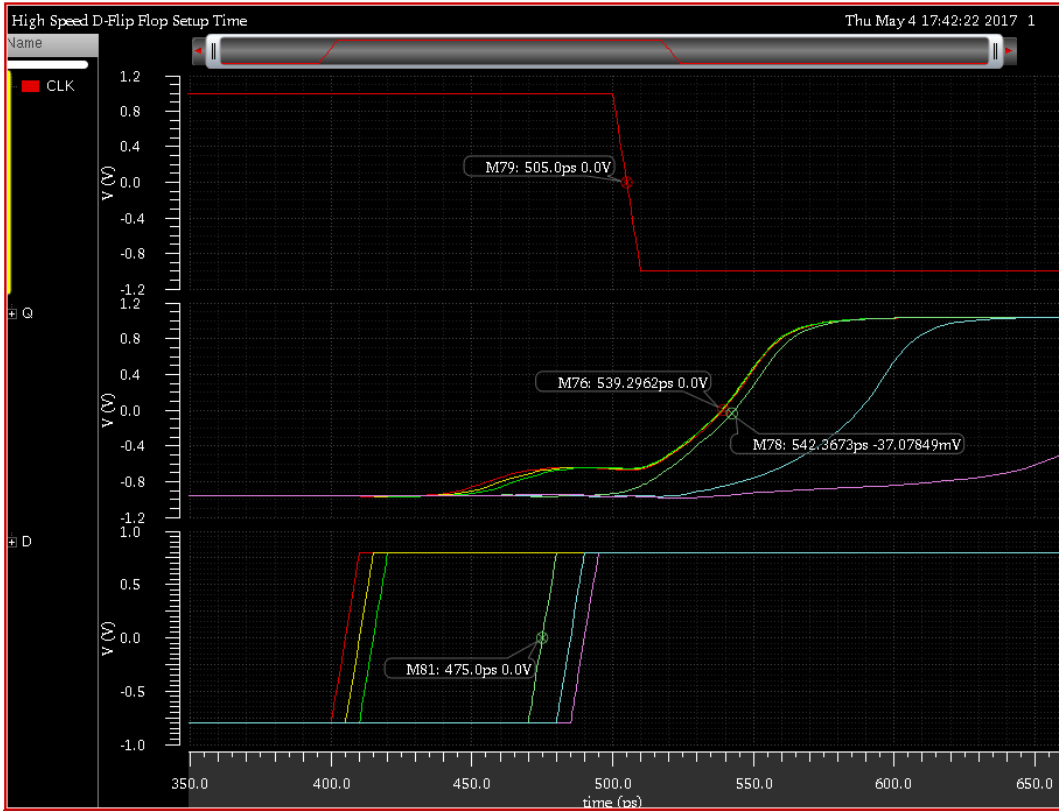


Figure 47. High speed D-Flip Flop Setup Time

The final performance metrics are shown below in Table 14. The high frequency DFF shows shorter rise and fall times compared to the lower frequency DFF as well as a slight improvement in setup time.

Table 14. Performance metrics for high frequency MCML D-Flip Flop

Specification	Value	Unit
Rise Time	48.6	ps
Fall Time	48.6	ps
$t_{CLK\ to\ Q}$	31.3	ps
t_{SETUP}	30	ps
t_{HOLD}	-10	ps
Total Current	449.6	μA

A divide-by-two frequency divider can be implemented by applying a known clock frequency to the CLK input and feeding the output of the DFF back to its input. A divide-by-eight counter can similarly be designed by cascading three

divide-by-two circuits, with the output of each DFF replacing the CLK input for the subsequent DFF in the division stage. This circuit is shown in Figure 48. After each stage of frequency division, the bandwidth requirements of each following stage are relaxed. Because of this, power can be saved by using the high frequency DFF only for the highest frequency dividers. For the circuit in Figure 48, the division of four is handled by the higher frequency DFF and the low frequency DFF performs the last division step. The implemented frequency divider is able to successfully perform a frequency division of eight for input frequencies up to 8.6 GHz.

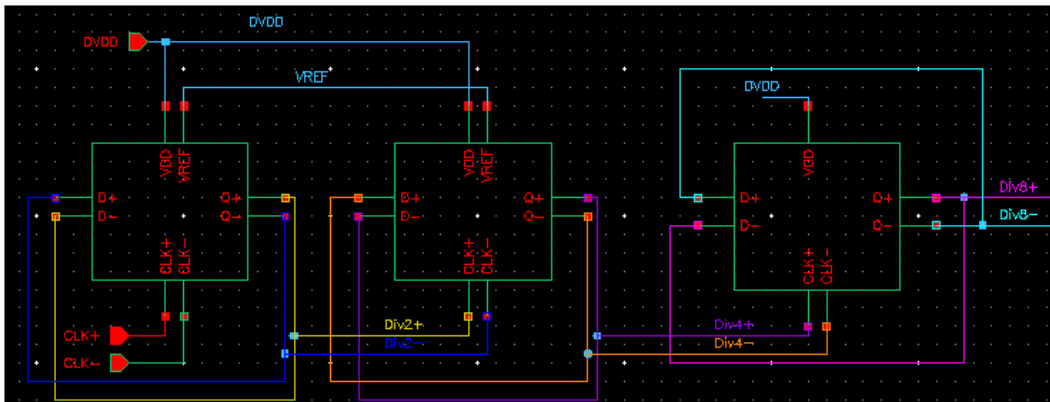


Figure 48. Divide-by-eight frequency divider

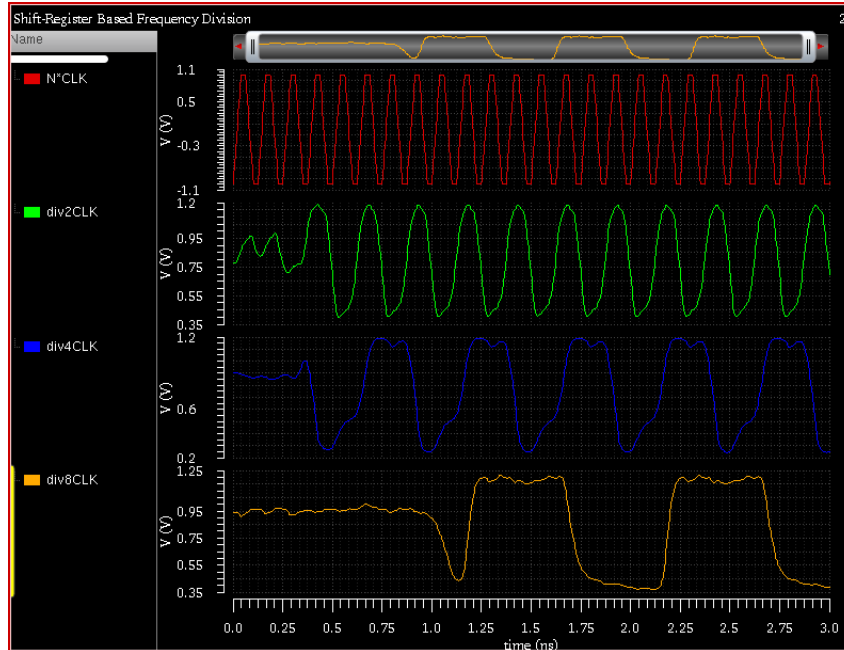


Figure 49. Time domain waveforms of the divide-by-eight frequency divider ($N_{fclk} = 8\text{GHz}$) The frequency divider passes all corner test cases except for sf, when the NMOS transistors are slow and the PMOS transistors are fast at N_{fCLK} frequencies exceeding 3GHz. This is likely due to the reduction in the gain of the latch for the high frequency DFF under this condition. On the active clock edge, during the transition from the tracking stage to the latching stage, the logic low level briefly spikes. Under the sf corner case at high input frequencies, this voltage spike is enough to cause a latching error. Increasing the latch current fixes this issue, but instead causes the divider to fail under the ss corner case, where both NMOS and PMOS transistors are slow.

5.4.3. Clock Buffer

Each of the switches used for the passive mixers has approximately 20fF of gate capacitance and each of the eight clock phase must drive ten switches. The DFF used for the shift register does not have enough current driving capability to drive

all of the switches at once. Instead a buffer is needed drive the gates. The CMOS inverter is selected as the gate driver due to its simplicity and low-power operation. To facilitate fast switching times, the inverter buffer is divided into five stages as shown in Figure 50. The shift register provides an input to U1, and the inverters U5x drive the gates of the NMOS switches. Because each clock phase drives ten switches, there are ten inverters U51 through U510. The gates of the ten U5x inverters present a heavy capacitive load so the gate widths of inverters U2, U3 and U4 are gradually increased to maximize the switching speed of these inverters.

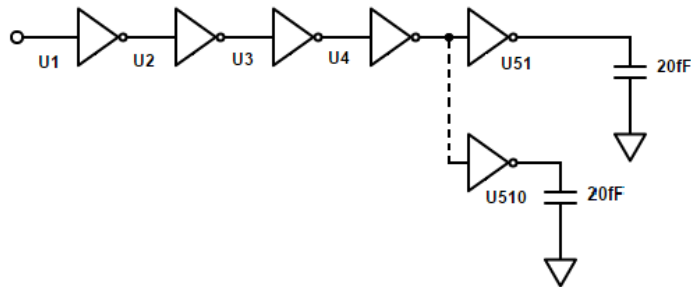


Figure 50. Clock buffer using inverters

The inverters used to drive the switches have a rail to rail logic swing, however, the CML buffers used for the shift register do not. This changes the duty cycle of the output of the inverter buffers. To resolve this, the W/L of the PMOS FET in U1 is strongly increased relative to its complementary NMOS FET to center its switching threshold well above the shift register's 0.6V logic low level of the shift register to maintain a 50% duty cycle. All inverter dimensions are displayed in Table 15.

Because the CMOS inverter consumes no static power, its power consumption can be closely approximated as a function of frequency and its load capacitance.

Since there are eight clock phases and ten 20fF switches per phase, the effective switch capacitance for the entire filter is 1.6pF. In addition, the gate-source capacitances for the all of the inverter buffers add up to 892fF, based on the final inverter dimensions displayed in Table 15. The dynamic power consumption of the switches and gate drivers can be approximated as follows.

$$P_{avg} = f_{CLK} C_{eff} V_{DD}^2$$

The final clock driver circuits consume an average power between 0.72mW to 3.6mW based on the clock frequency. The final specifications for the inverter-based switch driver are shown in Table 16.

Table 15. CMOS inverter buffer sizing (minimum transistor length)

[Redacted due to NDA agreement]

Table 16. Inverter switch driver specifications

Specification	Value	Unit
Rise Time (10%-90%)	56.9	ps
Fall Time (90%-10%)	45.4	ps
Average Power @ 1GHz	3.60	mW
Average Power @ 200MHz	0.72	mW

5.4.4. Multiphase Clock Generation

The multiphase clock generator is implemented by sending the divided clock signal through the shift register, clocked at the Nf_{CLK} . The resulting circuit successfully outputs 8 clock phases with a 50% duty cycle, phase shifted 45° with respect to each other. Four phases of the clock waveform are shown in Figure 52. The phase shift for each clock phase is determined by measuring the time delay

between each clock phase as it crosses 0.6V. The maximum delay error between adjacent clock phases is 2.3ps, which amounts to a 0.83° phase error at 1GHz.

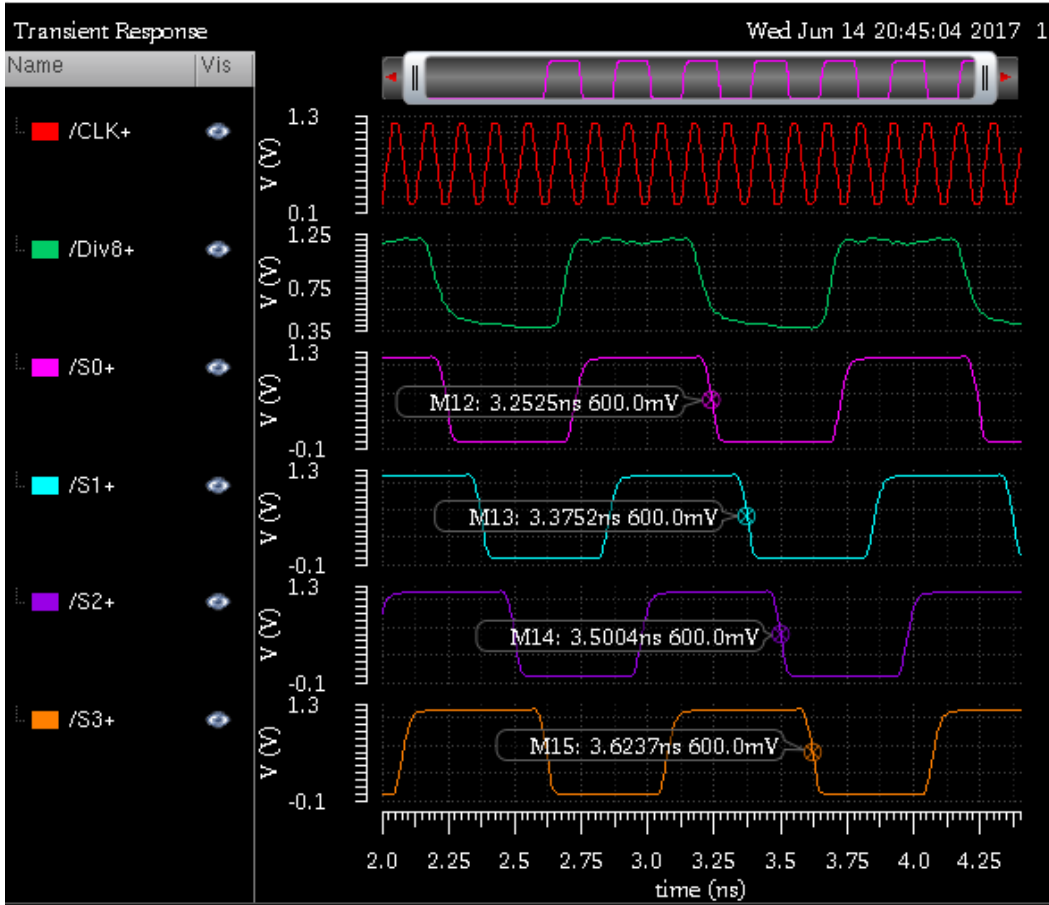


Figure 51. Multiphase clock generation based on shift registers $CL = 20fF$. Only positive clock phases shown

6. Filter Performance

The time domain waveforms of the harmonic rejection mixer is shown in Figure 52. The resulting waveform closely matches the expected staircase approximated sine wave detailed in Chapter 4.

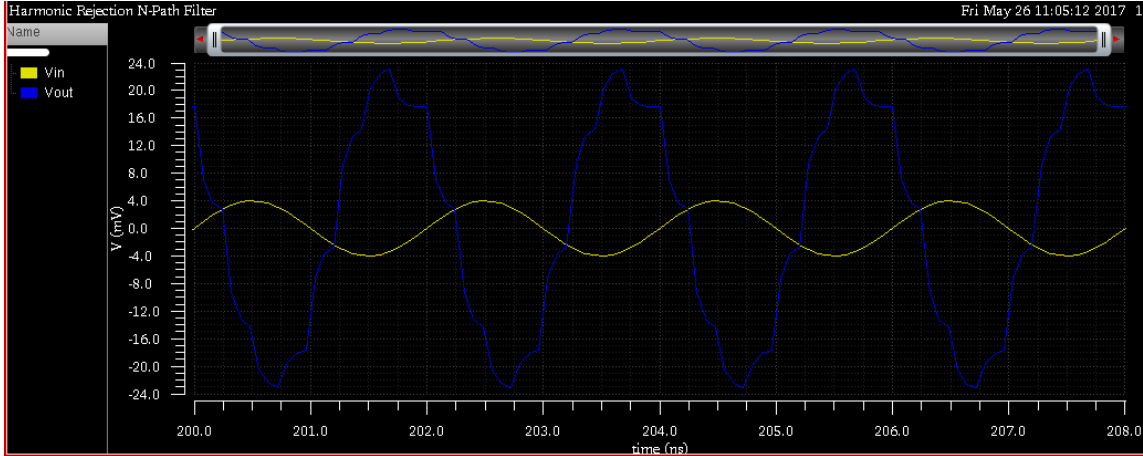


Figure 52. Time domain waveforms for the harmonic rejection N-path filter ($f = 500\text{MHz}$)

Figure 53 through Figure 55 show the frequency response of the differential N-path filter at 200MHz, 500MHz, and 1GHz. Because the mixing operation is nonlinear, an AC analysis in Spectre is unable to obtain these plots. Instead, the frequency response data is measured by running a transient simulation each frequency, then taking the FFT of the output waveform to determine the gain at each frequency. The results show that the N-path filter achieves a bandwidth of 6.8MHz throughout the frequency range and a gain of 14.6dB at the fundamental.

With a clock frequency of 200MHz, the filter suppresses the 7th harmonic by 33.7dB and the 9th harmonic by 40.2dB. At 1GHz, the gain at the fundamental is reduced to 13.8dB, but the harmonic rejection improves to 45.8dB for the 7th harmonic and 51.4dB for the 9th harmonic. This improvement in harmonic rejection is caused by the frequency roll-off of

the summing amplifier. The rejection of these harmonics can be improved by placing a low-pass filter after the N-path filter, if necessary.

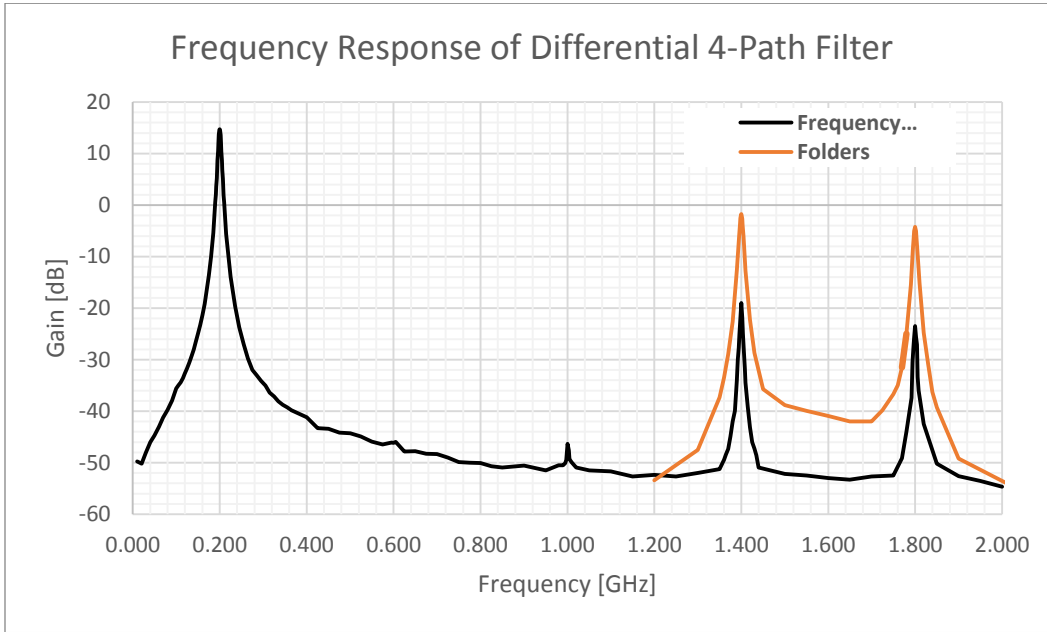


Figure 53. Frequency response of differential 4-path filter (fclk = 200MHz). The orange lines represent the folding of the 7th and 9th harmonics folded back into the fundamental

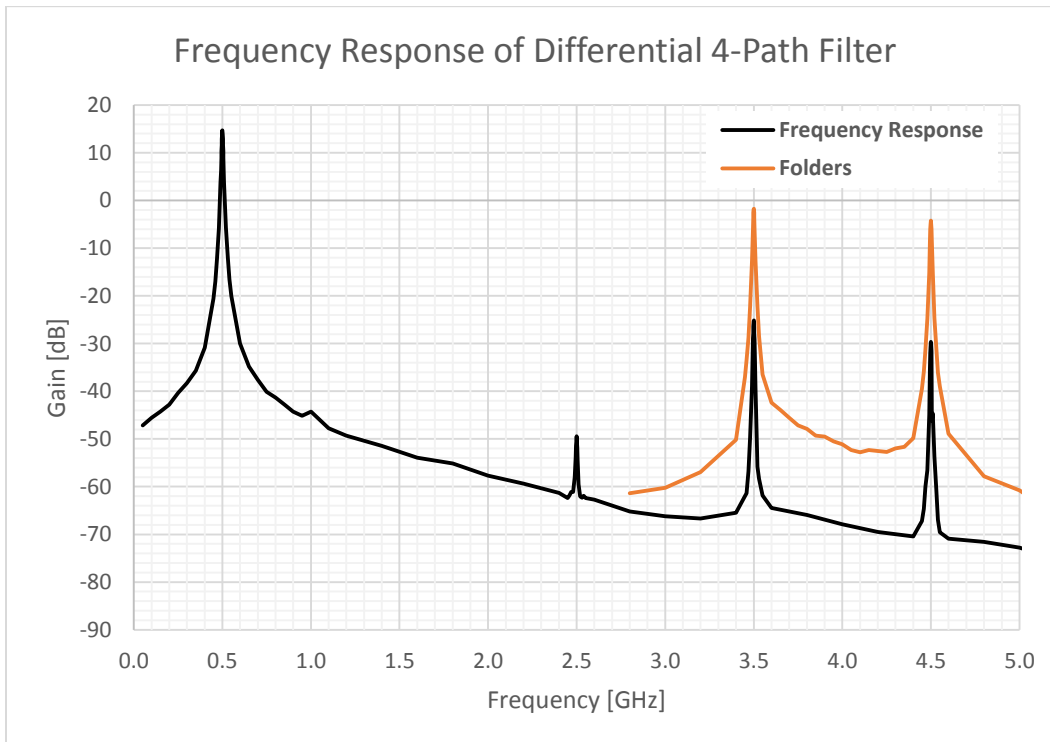


Figure 54. Frequency response of differential 4-path filter (fclk = 500MHz). The orange lines represent the folding of the 7th and 9th harmonics folded back into the fundamental

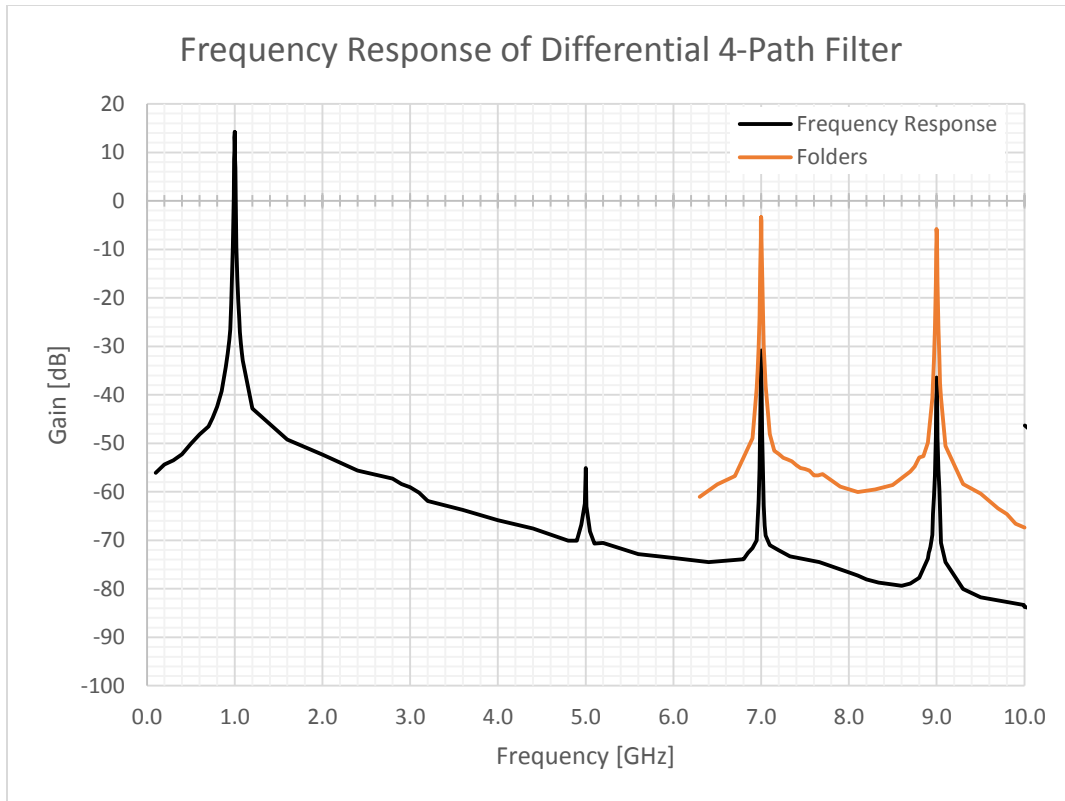


Figure 55. Frequency response of differential 4-path filter ($f_{clk} = 1\text{GHz}$). The orange lines represent the folding of the 7th and 9th harmonics folded back into the fundamental

Also shown on the frequency response plots is the harmonic folding, displayed in orange. Like the original N-path filter in [1], the $N \pm 1$ harmonics fold onto the fundamental during the first mixing stage. The $N \pm 1$ harmonics fold back with a strength of -16.4dB and -18.9dB relative to the fundamental, for the 7th and 9th harmonic, respectively. This closely corresponds to the predicted values of -16.9dB and -19.1dB predicted by the Fourier series model of the sampled sine wave from Chapter 4. The folded spectra cannot be removed from the signal after the first mixer, so the folders must be eliminated using an anti-aliasing filter prior to going through the N-path filter.

For each case, the 3rd harmonic is rejected completely, however, there is a small frequency spur at the 5th harmonic for each case. The incomplete rejection of the 5th harmonic likely results from non-idealities in the harmonic rejection function. Ideally, the

switches used for the mixer have zero rise and fall times and no overlap between them, but this is not true of the mixers used for the active N-path filter. Due to the finite rise and fall times, the switches do not instantaneously reach their minimum switch resistance. During the transition, the switch resistance is larger than the minimum resistance predicted by the model, which causes mismatch between the effective resistances of each path in the harmonic rejection mixers. This may explain why the 5th order spur is smaller for the 200MHz case than for the 500MHz or 1GHz case. Despite this, the filter achieves greater than 60dB of attenuation for the 5th harmonic for every case.

Because the filter is composed of non-ideal components, each component contributes some amount of noise to the circuit. The filter's noise figure (NF) quantifies the degradation in signal to noise ratio (SNR) between the input and output due to the noise sources within the circuit. To test the noise figure of the N-path filter for this thesis, a small sine wave (4mVpp) at 500MHz is applied to the input. The FFT for both the input and output signals is shown in Figure 56. In the FFT plot, frequency spurs exist at the $kN \pm 1$ harmonics, as predicted in Chapter 4. These spurs are expected behavior so are not considered for SNR measurements. Instead the SNR is measured by comparing the difference in the noise floors of the FFT plots at frequencies near the fundamental to the gain of the center frequency. An averaging filter is applied to the noise floor data to obtain a stable noise floor measurement. The gain at the center frequency is 14.67dB and the output noise floor exceeds the input noise floor by 20.8dB at 1.4GHz. This results in a noise figure of 6.13dB as shown below.

$$NF = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) = SNR_{in,dB} - SNR_{out,dB} = (P_{in} - P_{out}) + (N_{out} - N_{in}) = 6.13dB$$

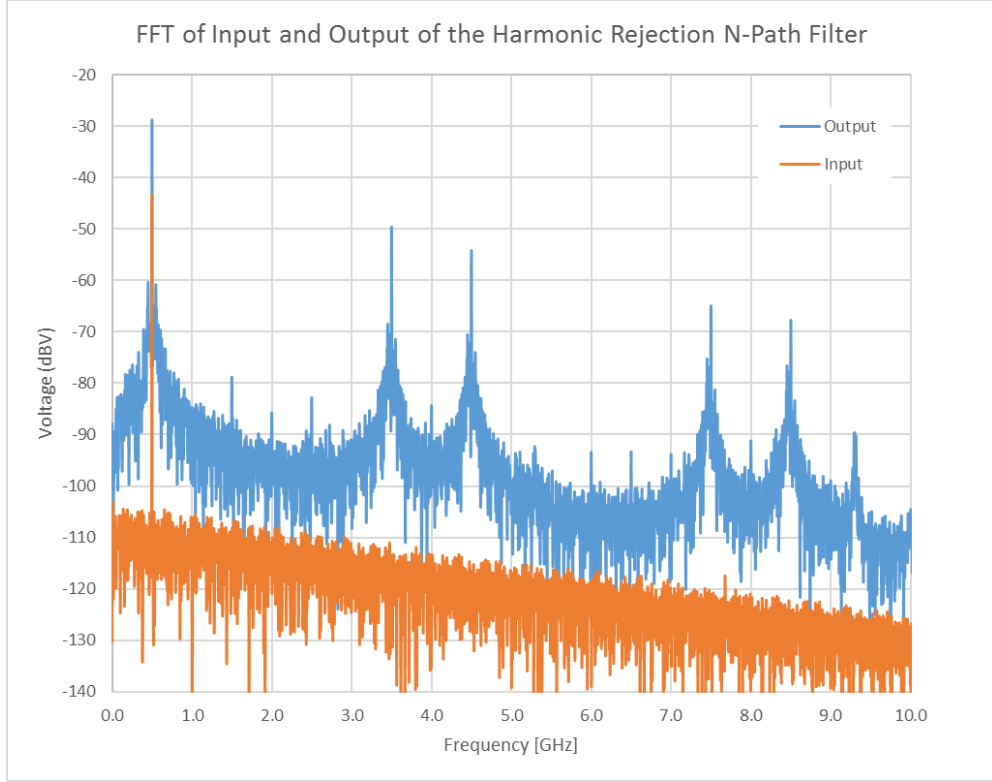


Figure 56. FFT of input and output signals used for noise figure calculation.

In theory, if the noise figure is low enough, this active N-path filter can replace both the channel-select filter and the LNA in RF front end of an SDR receiver. To judge the feasibility of this, the noise figure of this filter is compared to the worst-case noise figure of the implemented N-path filter designed in [1] cascaded with an LNA. The N-path filter in [1] has a worst case noise figure of 5dB and a gain of -2dB. Using Friis formula for noise factor, we can approximate the maximum LNA noise figure that can be placed after the original N-path filter to achieve the same 6.1dB noise figure obtained by the active N-path filter designed in thesis. It should be noted that Friis noise factor formula uses linear values for gain and noise factor.

$$F_{this\ thesis} = F_{[1]} + \frac{F_{LNA} - 1}{G_{[1]}} \text{ (Friis formula for noise factor)}$$

Friis equation shows that the passive N-path filter and LNA meet the 6.13dB noise figure achieved in this thesis when the LNA has a noise figure of 2.5dB. This is a reasonable noise figure for an LNA, however, this is a best case comparison. The noise figure measurement for this thesis project accounts for non-ideal device models and thermal noise from the resistors, but it does not account for device parasitics, device mismatch, or phase noise on the clocks. In practice, parasitics such as gate resistance and coupling between adjacent wires may significantly degrade the noise figure of the filter when it is implemented in silicon.

The two most important specifications for measuring linearity are the 1dB compression point and 3rd order intercept point (IP3). The P_{out} vs P_{in} curve in Figure 57 shows that for sufficiently small power levels, increases in the input power causes a proportional increase in output power. As the input signal power approaches the upper limit of the filter's dynamic range, the gain begins to compress as the filter is no longer able to provide a linear increase in gain. The 1dB compression point refers to the input power level that results in 1dB less gain than predicted by the trendline for the P_{out} vs P_{in} curve. This corresponds to an input power level of -16.8dBm for the harmonic rejection N-path filter.

In a non-linear system, as the input power increases beyond the 1dB compression point, the power at the 3rd harmonic increases at a slope of three. IP3 refers to the theoretical point where the asymptotic trend lines for the fundamental and 3rd harmonic meet. IIP3 and OIP3 represent the input and output power levels that characterize the IP3 point, respectively. Measuring IIP3 involves applying two tones f_1 and f_2 within the passband of the filter and measuring the relative power of the input tones to the 3rd order

intermodulation products. The 3rd order intermodulation products that fall within the filter's passband occur at $2f_1-f_2$ and $2f_2-f_1$. The results are displayed in and Figure 58.

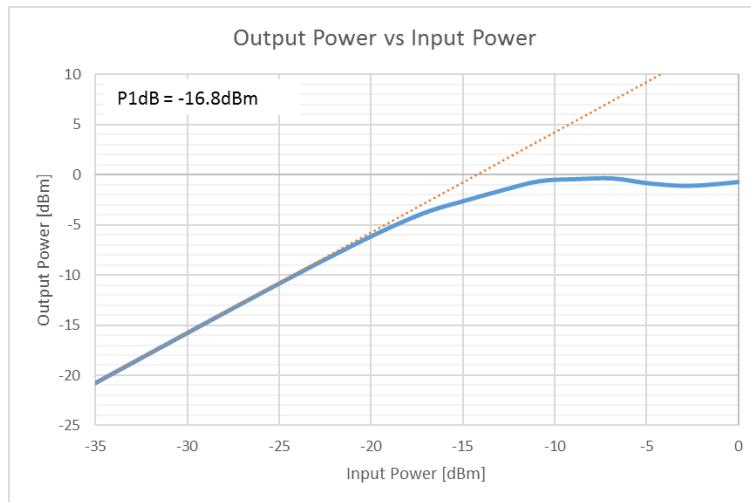


Figure 57. 1dB compression point test

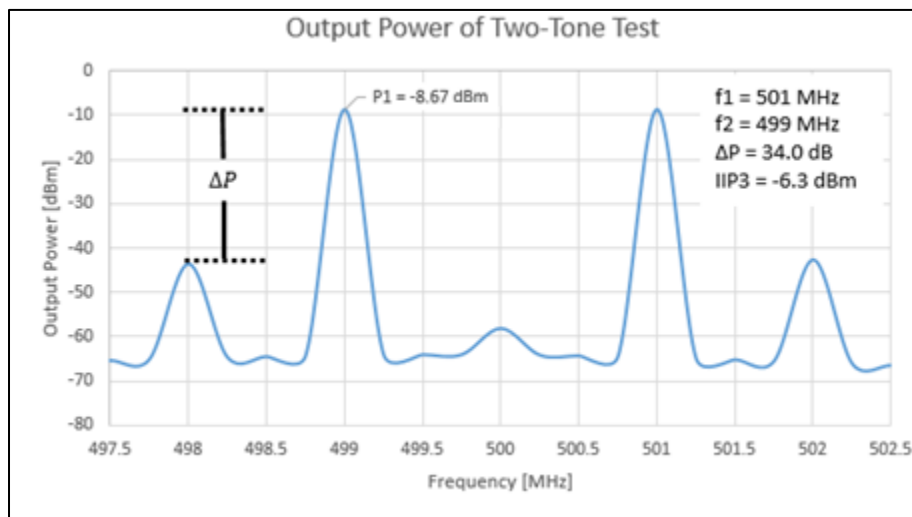


Figure 58. Measuring the IP3 of the active N-path filter using the two-tone method

$$OIP3 = P1 + \frac{\Delta P}{2} = -8.67dBm + \frac{34dB}{2} = 8.33dBm$$

$$IIP3 = OIP3 - Gain = 8.33dBm - 14.67dB = -6.34 dBm$$

The filter has an IIP3 of -6.3dBm. This value makes sense because it is approximately 10.5dBm larger than the 1dB compression point.

Another useful benchmark for linearity is the spurious-free dynamic range (SFDR). This is the ratio between the smallest input signal detectable by the filter and the 1dB compression point. An approximation for the SFDR can be made based on the noise figure and IIP3 value by treating all noise as thermal noise. The minimum detectable signal is the smallest signal that overcomes the thermal noise floor, including the noise contribution of the filter (noise figure). Using the asymptotic trend line for the fundamental power and the 3rd harmonic power level, the 1dB compression point occurs 2/3 of the way between the noise floor and IIP3. The spurious free dynamic range, SFDR, can then be approximated as follows.

$$SFDR = \frac{2}{3} [IIP_3 - (NF + 10 \log(KTB))] = 67.6dB \text{ (B=1GHz)}$$

Table 17 compares the implemented active N-path filter to previous works. Despite being composed of active components, this active N-path filter consumes less power than the original passive N-path filter in [1] and passive harmonic N-path filter in [5]. This is possible because this active filter design does not rely on extremely low-resistance switches in order to achieve good out of band attenuation and harmonic rejection. Smaller switches require much less current drive, which accounts for the vast majority of the power consumed in both of the passive examples. The tradeoff is that the active components always consume static power. As a result, the power consumption is nearly constant throughout the entire operating frequency range.

Table 17. Harmonic rejection N-path filter performance specifications

Performance	Value	[1]	[5]
Process	CMRF8SF 130nm CMOS	65nm CMOS	Simulated CMOS
Power Consumption	11.4-13.2mW	2-16 mW	~50mW @1GHz
Frequency Range	0.2– 1 GHz	0.1-1 GHz	1-5 GHz
Voltage Gain	+14.6 dB	-2 dB	+7.2 dB
Bandwidth	6.8 MHz	35 MHz	8 MHz
Quality Factor	29.4 - 147	3-29	-
P1dB	-16.8dBm	+2dBm	-
IIP3	-6.34dBm	+14dBm	-
OIP3	8.3dBm	+12dBm	
Spurious Free Dynamic Range	65.9 dB	-	-
Noise Figure	6.1 dB	3.5-5 dB	8.4 dB
Harmonic Rejection?	All below 7 th	No	All below 9 th

7. Conclusions and Future Work

This thesis sought to design an active harmonic rejection N-path filter capable of operating between the 200MHz to 1GHz bands. The filter was implemented in the CMRF8SF 130nm CMOS process and achieved a bandwidth of 6.8MHz throughout the frequency range with a voltage gain of 14.67dB. In addition, the harmonic rejection mixers on the down-conversion stage successfully suppress the 3rd and 5th harmonics. At 200MHz and 1GHz, the filter attenuates the 7th harmonic by 34dB and 45dB, respectively.

Higher clock rates increase the rejection of the 7th and 9th harmonics due to the frequency roll-off of the filter. As predicted for this N=8 filter, the 7th and 9th harmonic fold back onto the fundamental with a strength of -16.9dB and -19.1dB relative to the fundamental. This folding is a fundamental property of the N-path filter and these folding frequencies must be removed using an anti-aliasing filter before the N-path filter. The upper-bound of the N-path filter's tuning range is limited by the speed of the frequency divider.

Electrically speaking, there is no lower bound to the frequency range, however, decreasing the minimum frequency range will place the 7th harmonic of the lowest frequencies within the bandwidth of the filter, making them impossible to filter. An 8th order anti-aliasing filter with a cutoff frequency of 1GHz is needed to suppress the 7th harmonic of 200MHz by 40dB. The specifications for this anti-aliasing filter can be relaxed by increasing N or increasing the minimum frequency.

There are several improvements that can be made on future iterations of this filter. This active filter has a best case noise figure of 6.1dB. Under ideal conditions, this may be sufficient to replace the channel-select filter and LNA. However, this is an optimistic

result that does not account for device parasitics or mismatch. Some noise is contributed by the active components in the filter, and a significant amount of the noise is due to the large resistors used in the circuit. Using smaller value resistors reduces thermal noise, however, decreasing the feedback resistance requires increasing the feedback capacitance to achieve the same bandwidth. This does not present a problem as long as there is sufficient area available on chip, however, MOSIS limits educational chips to an area of approximately 0.8mmx0.8mm, including the IO pads. [Redacted due to NDA agreement]. Increasing the capacitance further requires larger die sizes or capacitors with a higher capacitance density, especially if more paths are used. In addition, the noise performance can be improved by increasing the power budget by biasing the op amps and summing amplifier at higher current levels. An alternative method of improving noise performance is replacing the physical resistors with their switched-capacitor equivalent as described in [5]. This improvement requires a reduction in switch resistance and hence increases the amount of power needed to drive them.

Another potential way to further develop the active N-path filter designed in this thesis is replacing the resistors in the op amp circuit with active CMOS resistors. Active CMOS resistors can be electrically tuned and implemented alongside an automatic gain control circuit in order to optimize the filter's dynamic range. For small input signals, the input resistors can be decreased to increase the gain, and for larger inputs, the resistances can be increased to prevent compression. Tuning the feedback resistor would allow for the bandwidth to be dynamically tuned in order to accommodate a variety of communications protocols. Future research can investigate whether the linearity improvement due to the gain control is enough to counteract the nonlinearities introduced by the active resistors.

In addition, improving the harmonic rejection of the active N-path filter requires the generation of more clock phases. This requires an improved method for generating the overlapping clocks. For this thesis, a divide-by-8 frequency divider generates the 8 clock phases needed to reject the 3rd and 5th harmonic by cascading three divide-by-two counters. This design is effective and straightforward but scales poorly for larger N. The next radix-2 frequency divider possible is a divide-by-16 counter, which requires twice as much bandwidth as the divider designed in this thesis. Designing such a filter for an N value that is not a power of two requires an alternative clock generation method. Implementing a 10-phase clock waveform to reject all odd harmonics before the 9th harmonic, for example, require either a delay-locked loop as mentioned in Chapter 5 or a divide-by-10 frequency divider.

This thesis does not address reducing the harmonic folding behavior inherent to the N-path filter. The most straightforward method of preventing harmonic folding is to increase N to relax the specifications of the anti-aliasing filter. In practice, increasing N will eventually yield diminishing returns as the device becomes more sensitive to phase noise as the phase difference between adjacent clock edges decreases. Future works should attempt to determine the optimal value of N that maximizes odd-harmonic rejection while minimizing sensitivity to phase noise.

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