# Design and Test of Wide Input and Output Constant Current LED Driver

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# Table of Contents

# List of Figures

# List of Tables

# Abstract

This senior project aims to provide design and test the performance of a DC-DC constant current LED driver for use in a larger DC smart building infrastructure. In this instance, a SEPIC topology is chosen to provide high efficiency output current at output voltages that can be above or below the input voltage. This is challenging since the same design must operate at similar efficiency for vastly different environmental conditions. As a part of a larger system, the design must be able to perform the given task consistently regardless of changes to the source and load power.

The design uses the LT3795 LED controller to operate power switches and inductors to transform the input power into usable output power for a string of LEDs. The controller is paired with an onboard microcontroller to provide error reporting and supplement the PWM dimming control features of the IC. Simulations were done to ensure the efficiency of the design remained above 93% within the full range of input and output voltages, along with a range of PWM frequencies and duty cycles.

After manufacturing and assembly, the board was found to be under specification regarding the input and output voltage ranges, as well as below the efficiency target. This was largely due to issues regarding the layout assembly of the finished product.

# Chapter 1: Introduction

Power electronics is a subdivision of Electrical and Electronics engineering that works to "Control the flow of energy from an electrical source to an electrical load with high efficiency, high availability, high reliability, small size, light weight, and low cost" [1]. As technology in the home has developed, the need for efficiency and reliability has risen leading to an increase in power electronics usage in the home. One instance of power electronics in consumers' daily lives has been personal electronics. The usage of smartphones and laptop computers has increased the amount of power the world uses to charge DC batteries and run DC systems. Part of power electronics focuses on the transformation of AC power to DC power, which is widely used in the personal chargers individuals use to power their electronics. In addition to this, there are many DC to DC converters required for power transformation inside the devices. With the complex network of subsystems and technologies there is a need for power controllers that can be used to service a wide range of loads. A single controller design that can be used in different parts of the product or across a family of products reduces engineering design costs. In future iterations of the product, sub-modules may be changed that require more power. The power controller must be flexible enough to be scaled up in power without requiring a re-design.

When interconnecting AC and DC systems, there are many options to convert one input power into another. These options can hold different stages in which a specific transformation is conducted and chained to complete the overall black box. Because of this ability to interconnect substantially different converters, there is high demand for a variety of power topologies, including topologies that have similar transfer functions but different methods of operation. These can be organized in many ways, but generally have simpler groupings based on their simplest form of operation. For example, in DC to DC conversion, three of the simplest converters are the buck, boost, and buck-boost converters which are the basic building blocks of more complex power converter designs.

The buck converter is a circuit topology of DC to DC converter that operates by switching current through an inductor into a capacitor to produce a lower output voltage than input voltage. By varying the duty cycle of the switch, the ratio of average output voltage to input voltage can be changed in real-time. This style of pseudo-digital control is very appealing and common in DC to DC power conversion since many control schemes can be used interchangeably. There are many

off-the-shelf IC's that can be purchased to provide a buck converter, as well as application specific designs for multiple input or output requirements.

The boost topology is another type of DC to DC converter that uses a power switch to vary the current through an inductor. Rather than generating a lower voltage, the boost converter creates a higher voltage output based on the duty cycle of the switching element. This also shares a similarly flexible control scheme to the buck converter. Both the buck and boost converters prioritize the flexibility, reliability, and efficiency of power electronics, and form a basis for DC to DC converters that is built upon.

One such implementation that build upon the two topologies is the buck-boost converter, which uses a switching element to generate an average output voltage to be higher or lower than the input voltage based on the duty cycle. While the simplest form of the buck-boost converter is relatively low efficiency and hard to use, there are many optional changes that can improve the performance. Utilizing a synchronous topology that uses two power switches rather than one would raise efficiency and simplify interfacing restraints present in the non-synchronous topology. In similar style, many power electronic converters can be modified to suit specific applications and increase efficiency and flexibility.

# Chapter 2: Background

## Switching to DC

Increasingly, many consumer devices can be powered by DC (computers, LED lights, bathroom fans, cameras). Home solar panels generate DC power which is perfect to supply these devices, but existing homes have an AC electrical grid inside the house instead of DC. To get around this, home solar panels use an inverter to convert DC to match the house's AC grid then each consumer device internally has a power rectifier to convert AC back to DC. This conversion back-and-forth makes room for inefficiencies and component malfunctions. A potential solution would be to convert the electrical grid inside the home to a DC network rather than AC. Consumers that wish to convert their house electrical grid from AC to DC lack a straightforward solution, they must retain a skilled electrician or engineer to build a parallel DC grid in their house.

An Internet search of DC house design plans reveals that many current projects are large scale bids to build what are effectively demonstration buildings. Companies and national committees are looking to fund the construction of DC buildings as a proof of concept rather than a usable home living environment. Companies are also looking to run servers off DC supplies, since the individual server sub-blocks already require DC inputs. The current solution is to do large scale conversion of line power into 12V or 48V DC, then feed this to the sub-blocks [2]. This technology is currently oriented towards servers rather than other industrial applications.

## Smarter Buildings

The "internet of things" (IoT) has been a rising topic in consumer electronics. The movement involves adding sensors to home products to collect data and facilitate human-machine interaction. These devices operate on wireless networks and frequently pull power from the wall outlet rather than a battery. In a house, there are generally high and low connectivity areas due to a lack of wireless broadcast points to cover the area evenly. Between the variable connectivity and the increased activity due to an increased number of wireless devices, the 2.4GHz and 5GHz bands are incredibly crowded. This problem only gets worse with more and more devices, bringing up

the need for higher power emitters and receivers as well as decreasing the performance of IoT devices. To alleviate this problem, devices can elect to use wired networking schemes to give better latency and lower data packet loss as well as lower competition on the wireless communication networks.

## Lumencache

This project is a partnership with Lumencache, a company looking to "Make buildings smart from the start." This project will contribute to the larger project of a full featured infrastructure. The nanogrid design prioritizes modularity in many ways, one of which being the ability to use different power supplies without changing the surrounding infrastructure. Different load types and load configurations in a building will call for different power solutions, and this project will be one of the solutions to choose from.

The overall project goal comes in two distinct parts: power and data. On the power side, they are building an infrastructure to place into buildings that runs DC power wiring around to the loads from a central circuit box containing most of the power electronics. This means that all the buck, boost, and buck-boost drivers will be centralized and accessible much like a circuit breaker is in current building designs. Cat5 wiring will be run from the central box to the different rooms and subsequently loads, allowing for a universal connector interface from supply to driven load. The next part of the project is data. Since there is already wiring in place to the different rooms in a building, data communication can be put in place as well, with smart-building behavior being integrated alongside the power component in the circuit box.

# Chapter 3: Design Requirements

## Block Diagrams

Figure 3-1 shows the three input and single output requirements of this design. The LED driver will take in one power and one control input to produce a variable output voltage for driving LEDs elsewhere in the system. The 12V supply will be used to operate the supporting microcontroller circuitry.

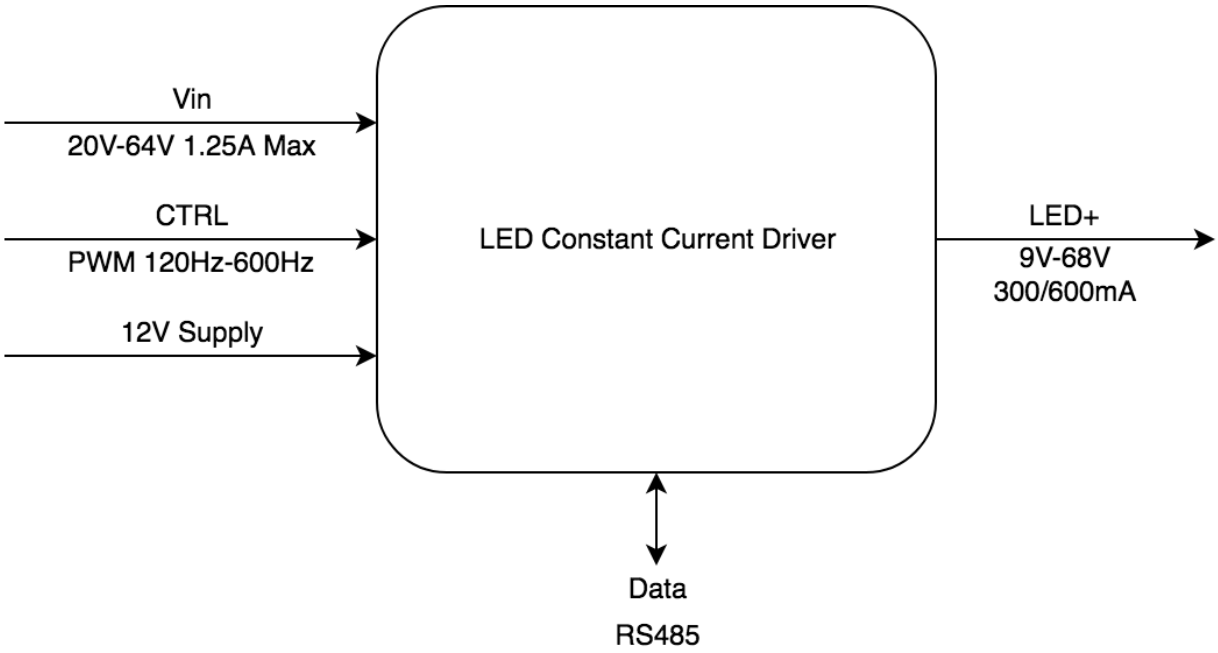


*Figure 3-1 Level 0 System Block Diagram*

Figure 3-2 shows the system level organization of the design, with the LED controller receiving the input power as well as the input control signal (routed through an optional control card) to drive the power switches and generate the required output. The daughter card will have further digital communication through the RS485 digital communication standard and will be used to provide further monitoring on the status of the power controller.

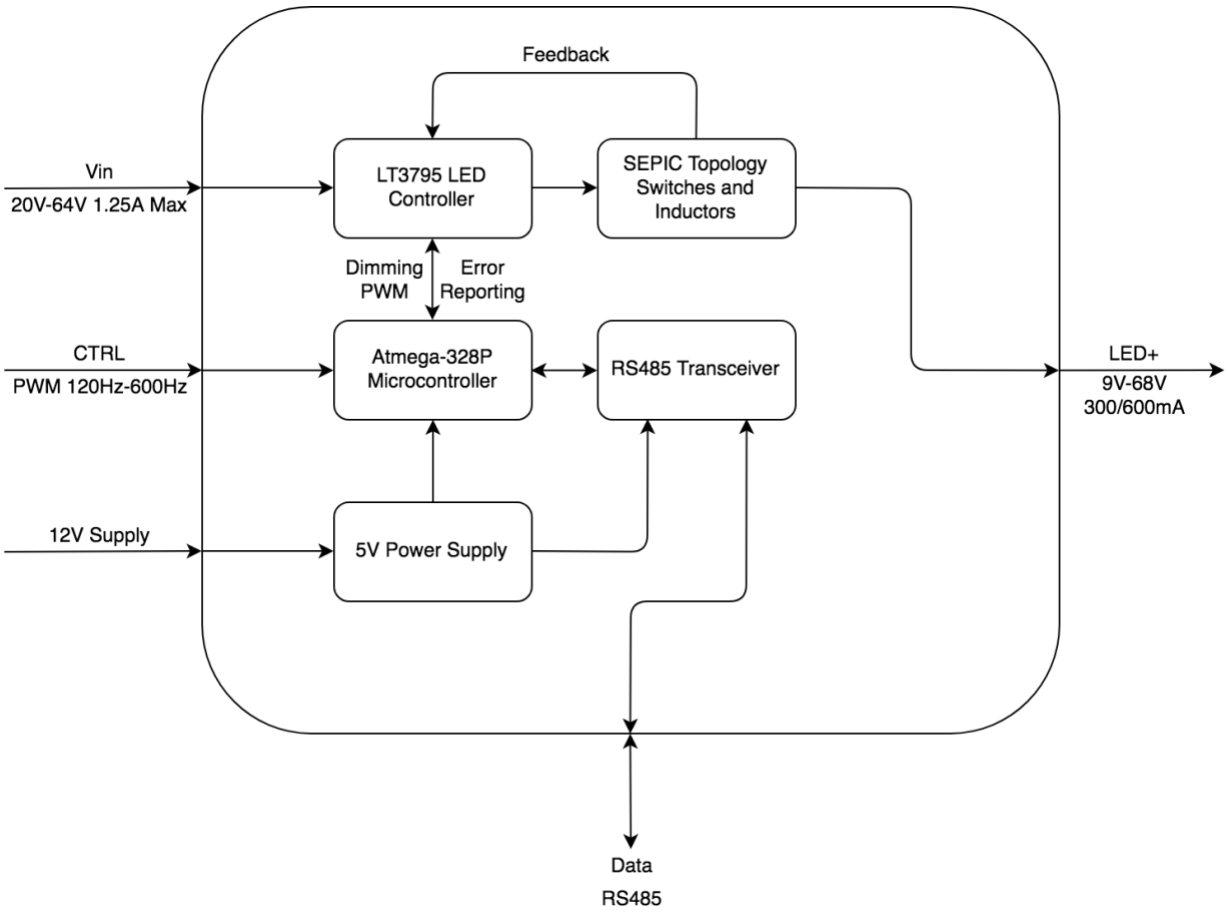


*Figure 3-2 Level 1 System Block Diagram*

## Technical Design Requirements

The input power signal is defined with a minimum voltage of 20VDC and a maximum voltage of 64VDC, operating at a typical 48VDC. This is defined by the power sourced to the controller by the power converters between the LED controller and the main source power (grid, solar, or battery). The maximum input current is calculated based on the maximum output power and the minimum input voltage resulting in a current of 2.5A.

The output voltage and current will be dictated by the combination of LED input behavior as well as the dimming control in the LED controller. The output voltage is defined with a minimum voltage of 9VDC and a maximum of 68VDC, with a typical of 40VDC. These values are specified based on the arrangement of load LEDs supported by this family of controllers. With more LEDs in a string, the output voltage must be increased to meet the turn-on voltage

requirement of each LED. The maximum output current is specified at 900mA with two typical currents of either 600mA or 300mA, each offered as different versions of the same product.

The control pin is a PWM signal ranging from 120Hz to 600Hz, fed into the LED controller to set LED brightness through output current. This control signal must be routed through the optional data communication card to allow for overriding in software. The optional data communication uses RS485 serial communication at 38400 baud rate by requirement of the exterior system. This is a bus communication protocol using two digital lines to communicate with a microcontroller on-board the optional daughter card to operate error reporting and alternative dimming control.

*Table 3-1 Design Requirement Specification Summary*

| Design Requirement | Specification |
|---|---|
| Input Voltage | Min: 20V<br>Typical: 48V<br>Max: 64V |
| Input Current | Max: 2.5A |
| Output Voltage | Min: 9V<br>Typical: 40V<br>Max: 68V |
| Output Current | Max: 900mA<br>Typical: 300mA, 600mA |
| Dimming Control | Min: 120Hz PWM<br>Max: 600Hz PWM |
| Digital Communication | RS485 Serial Protocol |

# Chapter 4: Design

## Converter Topology

In this design, the input and output voltages share similar ranges and are not always higher or lower voltage than each other. Due to this, a converter topology that can produce output voltages higher, lower, and equal to the input voltage is required. In this case, a Single-ended primary-inductor converter (SEPIC) has been chosen. The SEPIC is a DC-DC converter that uses a single switch to control the flow of energy from the input to the output through a boost converter followed by a buck-boost converter. The benefit of this is the ability to drive an output voltage above, below, and equal to the input voltage as well as an output voltage with the same polarity as the input voltage. This is in comparison to a traditional buck-boost topology, which can drive similar output voltages, but has a reversed polarity on the output. The reversed polarity of the output requires more circuitry to either reverse the output polarity to match the input voltage or provide safety due to the large "negative" voltage.

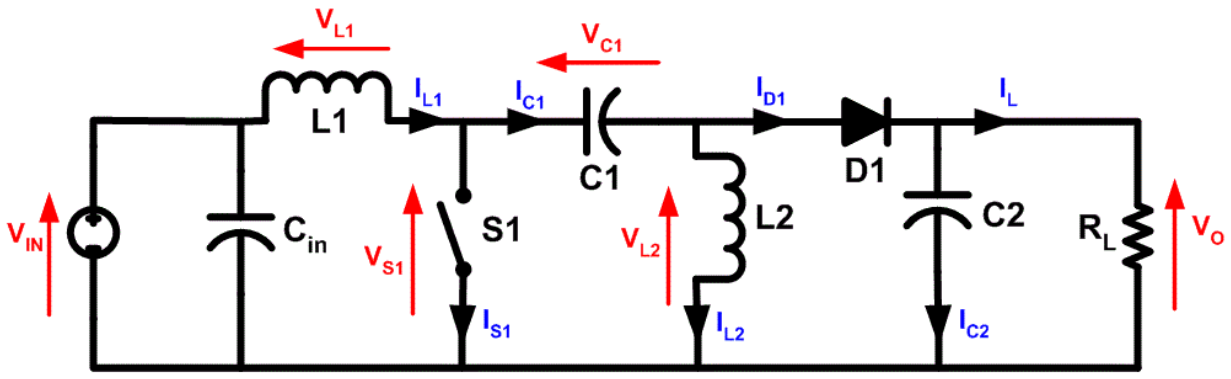


*Figure 4-1 Single-ended primary-inductor converter Operation Diagram [3]*

Another benefit of the SEPIC topology is the inherent short-circuit protection. Due to C1 being in direct path of current flow, a short circuit on the output of the converter will quickly drain the charge stored in the capacitor and the DC current will drop to zero amps. This is especially useful in the context of this project since a short circuit on an LED string will result in a large voltage present across an extremely low resistance path producing a large surge current.

## SEPIC Component Selection

The SEPIC design begins with selecting the inductors, coupling capacitor, and input/output capacitors. Assuming CCM (Continuous conduction mode), the duty cycle is set by $D = \frac{V_{OUT}+V_D}{V_{IN}+V_{OUT}+V_D}$, where $V_D$ is the diode forward voltage [4]. In this case, the maximum duty cycle is set using the maximum $V_{OUT}$ and the minimum $V_{IN}$ (68V and 20V respectively). This maximum duty cycle is used to find the critical inductance. The peak-to-peak inductor current was set at 40% of the maximum input current and resulted in 816mA. This results in an inductor value of $L = \frac{V_{IN(Min)}}{\Delta I_L * f_{SW}} * D_{Max}$; in this case the critical inductance was equal to 37.9µH. The peak inductor currents are also given at $I_{L1(Peak)} = I_{OUT} * \frac{V_{OUT}+V_D}{V_{IN(Min)}} * (1 + \frac{40\%}{2})$ and $I_{L2(Peak)} = I_{OUT} * (1 + \frac{40\%}{2})$, resulting in peak currents of 2.47A and 0.72A. The peak current of the power MOSFET is the sum of these two currents and is used for MOSFET selection.

The coupling capacitor was chosen based on the RMS current rating. $I_{Cs(rms)} = I_{OUT} * \sqrt{\frac{V_{OUT}+V_D}{V_{IN(min)}}}$ and is equal to 1.1A at maximum output voltage. The output capacitor must be rated for RMS current and sufficiently low ESR. The RMS current is the same as the RMS current of the coupling capacitor in a no-load situation. This means the output capacitor must be rated for the same 1.1A current. The ESR and capacitance is related to the output voltage ripple, which was selected as 0.5% of the maximum output voltage. This resulted in an ESR given by $ESR \leq \frac{V_{ripple}*0.5}{I_{L1(peak)}+I_{L2(peak)}}$ and minimum capacitance of $C_{OUT} \geq \frac{I_{OUT}*D}{V_{ripple}*0.5*f_{SW}}$. This works out to be 53mΩ and 5.47µF.

## Power Controller

The power controller selected is the LT3795 LED controller with spread spectrum frequency modulation [5]. This controller was selected due to the wide input and output voltage ranges, spread spectrum frequency modulation, and support for the SEPIC topology.

The control loop for the primary power MOSFET takes in input current, power switch current, output current, and output voltage as feedback paths. Since three of these values are currents, sense resistors are selected to convert the current value into voltage for direct comparison

within the controller. The input current sense resistor is selected based on the maximum input current expected, which is estimated as 2A average. With a peak-to-peak inductor current of 800mA, the peak input current should be less than 2.4A in normal operation. The LT3795 datasheet calls for $I_{in} = \frac{60mV}{R_{INSNS}}$ so $R_{INSNS}$ = 15mΩ. The primary switch sense resistor is set by $R_{SENSE} \leq \frac{V_{IN}*0.07V}{V_{LED}*I_{LED}}$ so $R_{SENSE}$ = 22mΩ. The output current is set by $R_{LED} = \frac{250mV}{I_{LED}}$ so $R_{LED}$ = 416mΩ or 833mΩ depending on which output current option is needed. The output voltage is set by a voltage divider from the output to detect short and open LED conditions. A resistor network is set to keep the feedback pin of the controller between 0.35V and 1.2V during nominal operation. With an output range of 9V-68V, this was accomplished with a resistor network shown in Figure 4-2. $V_{REF}$ is set by the internal reference voltage of the controller at 2V nominal.

## MOSFET Selection

The power MOSFET is a critical component in switch mode power supply design and has a large impact on the performance of the power supply. The LT3795 controls two MOSFETs, one primary switch used to drive the SEPIC and one output switch to provide dimming control for the output LED's. The primary switch is an ONSEMI FDD390N15A, selected for its low $R_{DSon}$ as well as low $Q_{gd}$ [6]. The peak current through this switch is equal to the sum of the peak currents through the two inductors and was found to be 3.2A. The rms current of the switch is given by $I_{Q1(rms)} = I_{OUT}\sqrt{\frac{(V_{OUT}+V_{IN(min)}+V_D)*(V_{OUT}+V_D)}{V_{IN(\min)}^2}} = 2.34A$. The low $Q_{gd}$ is to lower the switching losses with a switching frequency of 500KHz. The $V_{DSS}$ of the NMOS must also be greater than the maximum $V_{in}$ + $V_{out}$, which is 132V. The output switch is a PMOS with low $R_{ds(on)}$ to minimize conduction loss. The $V_{dss}$ is based on the maximum $V_{out}$ of 68V. The switch selected is a Diodes Incorporated ZXMP7A17G PMOS with $R_{DS(on)}$=160mΩ and $V_{DSS}$=70V [7]. Due to the low frequency of the PWM dimming signal, the switching losses affect the total power less, reducing the need for a low $Q_{gd}$.

# Simulation Results

Simulation was conducted in LTSpice since the power controller is a Linear Technology product. Figure 4-2 shows the circuit used for simulation, with an output load modelled with a diode and resistor. The diode is specified by a simple model with a forward voltage 1Vt below the target voltage, and the resistor is sized to give 600mA current when 1V is placed across it. This was to mimic the behavior of an LED string loosely without requiring as complex simulation while still maintaining the "turn-on" characteristic not shared by a resistive load.

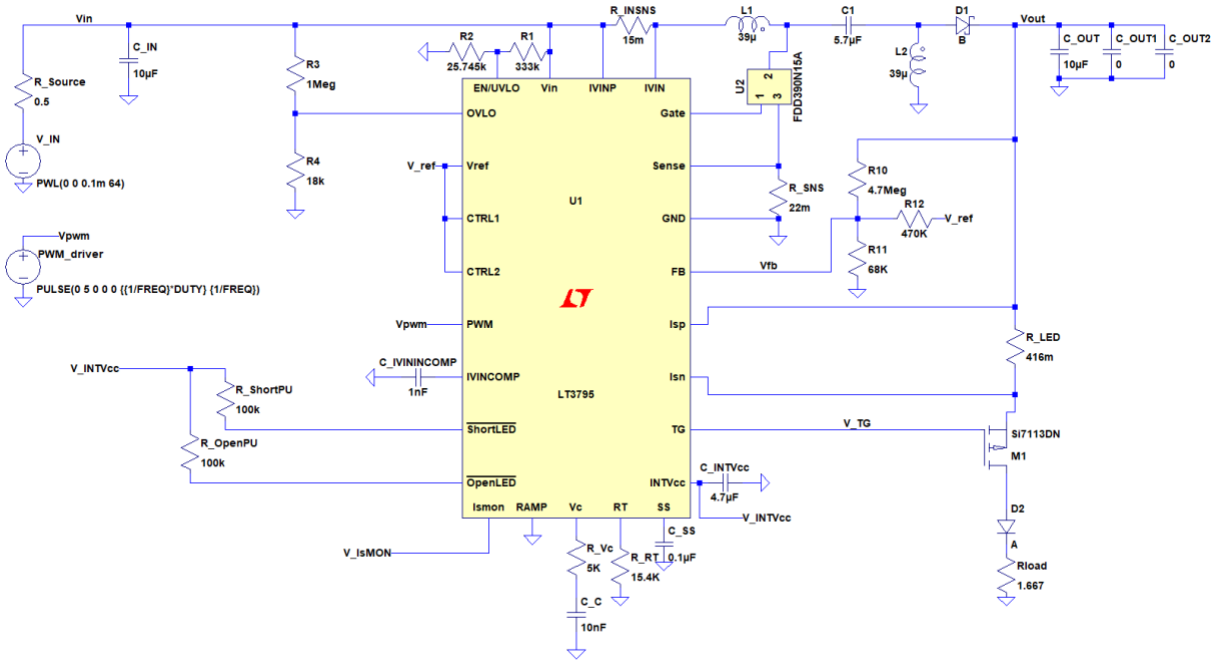


*Figure 4-2 LTSpice Simulation Circuit Diagram*

The first simulation was conducted at full 600mA current load at typical input and output voltages of 48V and 40V respectively. Figure 4-3 shows the output voltage reaching a steady state of 40V and the output current centering on 600mA. Data recording began at 1ms to account for the soft start time, and the voltage started at 15V due to initial conditions set to decrease repeated simulation times. Figure 4-4 shows the duty cycle of approximately 47%, close to the predicted 45.4% duty cycle given by the input and output voltages.

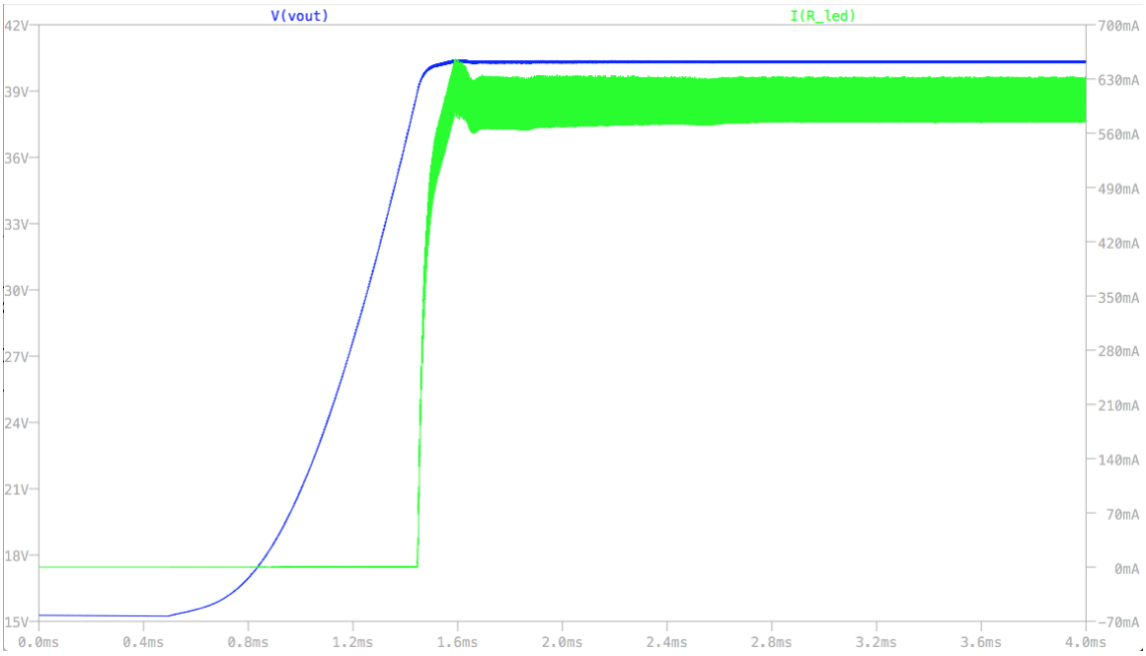


*Figure 4-3 Output Current and Voltage at 48V input and 40V output*

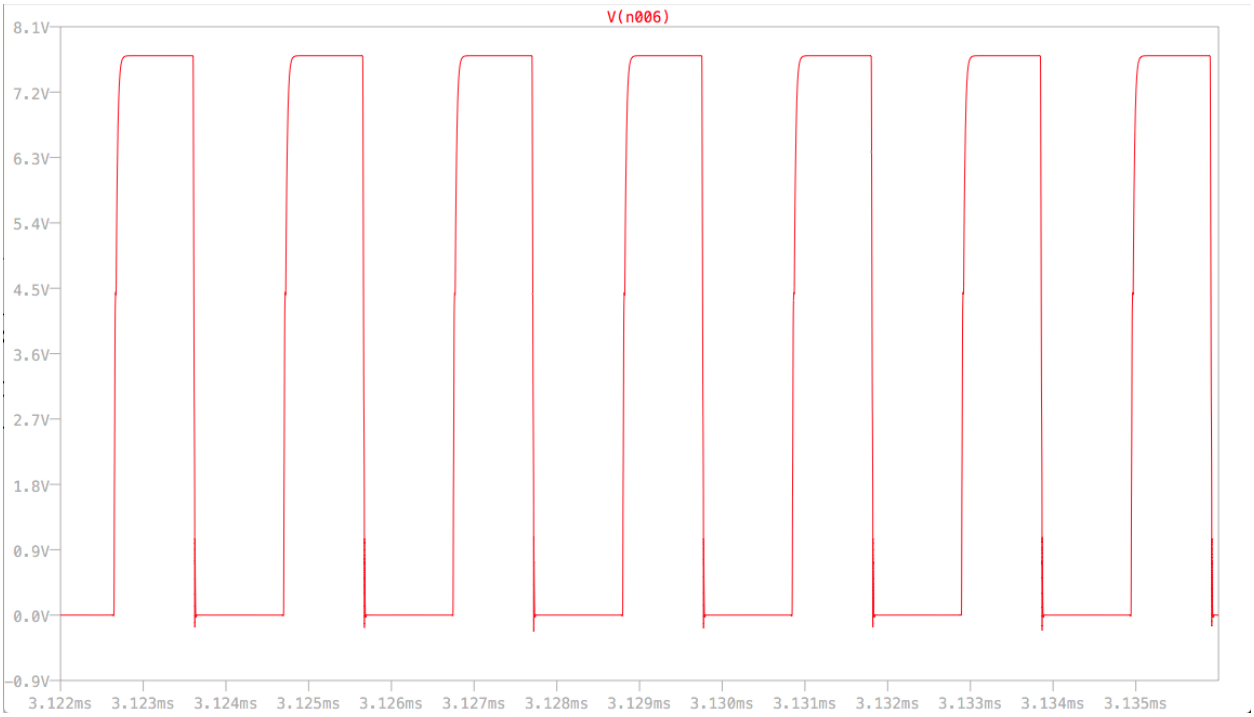


*Figure 4-4 Duty Cycle of 47% at 48V input and 40V output*

The second simulation was performed at the lowest input voltage of 20V and nominal output voltage of 40V. Figure 4-5 shows the output voltage reaching a steady state at 40V and

output current of 600mA. Slope 32.4KV/s. The ability for the converter to remain at the same output voltage and current with two different input voltages shows the versatility of the SEPIC topology for this problem. Figure 4-6 shows the duty cycle reaching 83%, which is above the calculated duty cycle of 67% for 20V input and 40V output. This is due to the current drawn by the load since the output voltage will not follow the same saw-tooth behavior as the no load condition.

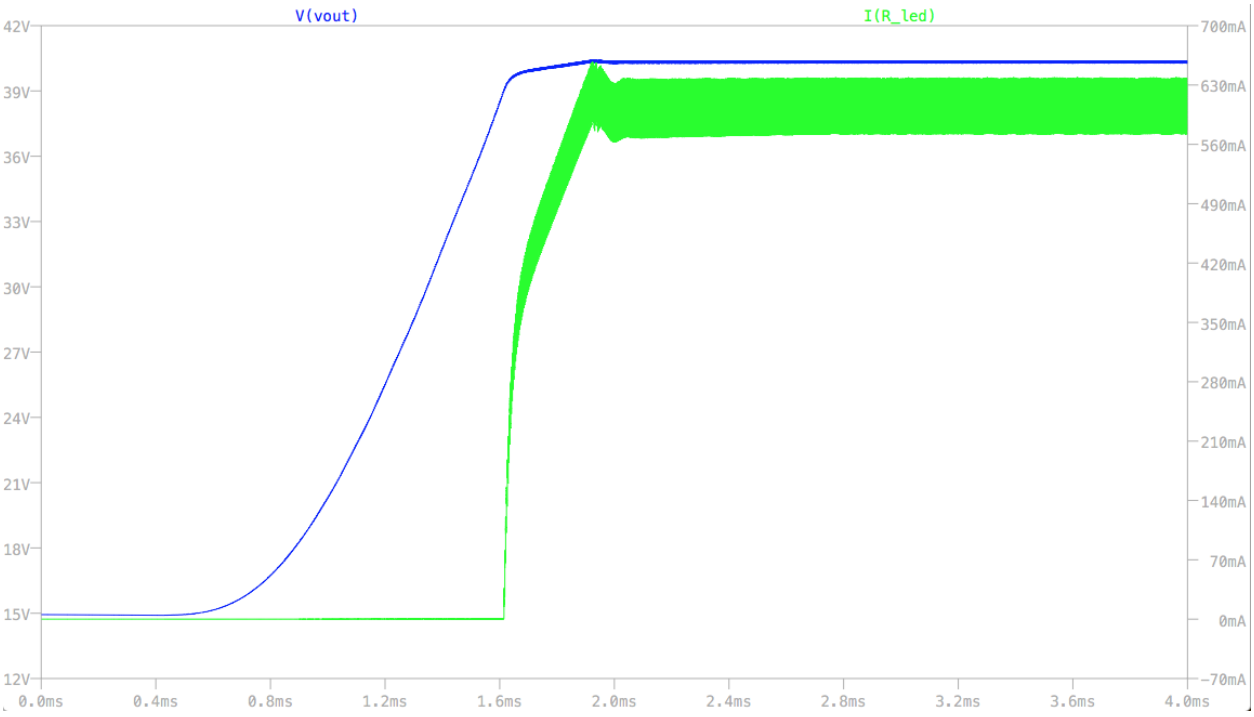


*Figure 4-5 Output Current and Voltage at 20V input and 40V output*

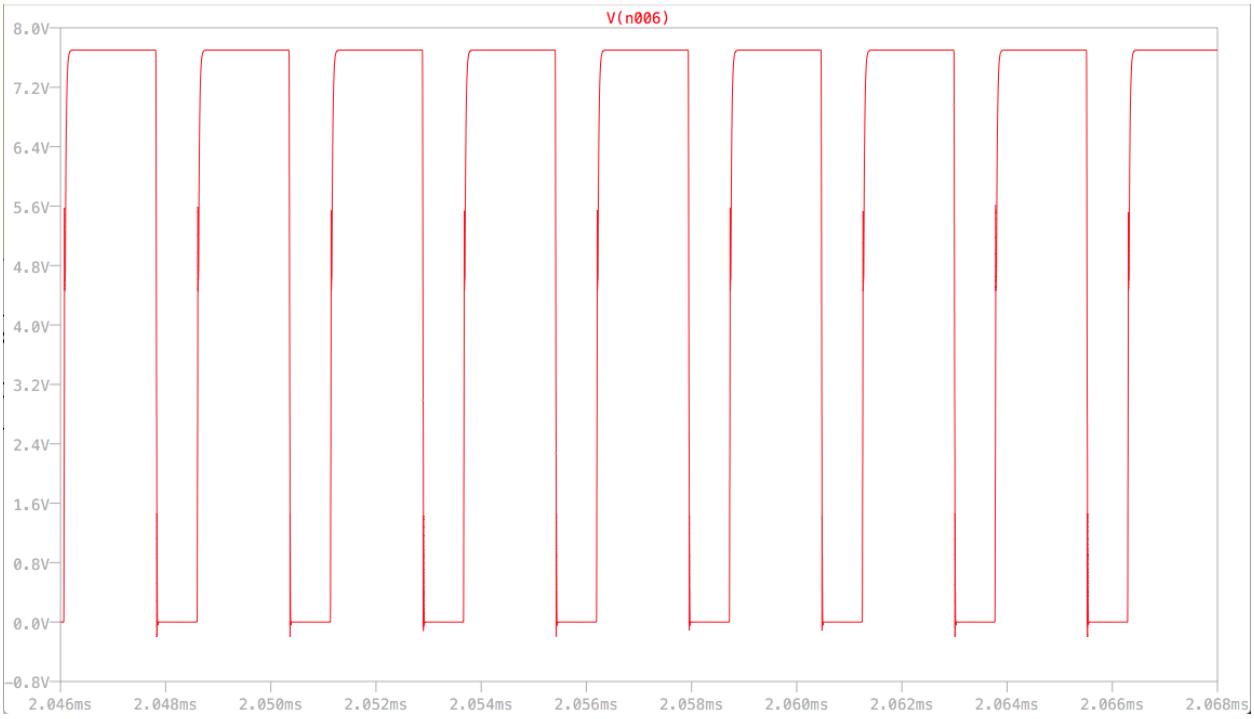


*Figure 4-6 Duty cycle of 83% at 20V input and 40V output*

The third simulation is the most extreme ratio of input to output voltage at 20V and 68V. This is the minimum input voltage and maximum output voltage, which results in the highest duty cycle. Figure 4-7 shows the output voltage at 68V and the output current averaging 600mA. Figure 4-8 shows a duty cycle of 82%, slightly higher than the calculated 77% duty cycle for this input and output voltage. With a lower output current, the duty cycle can be seen to decrease and move closer to the estimated value.

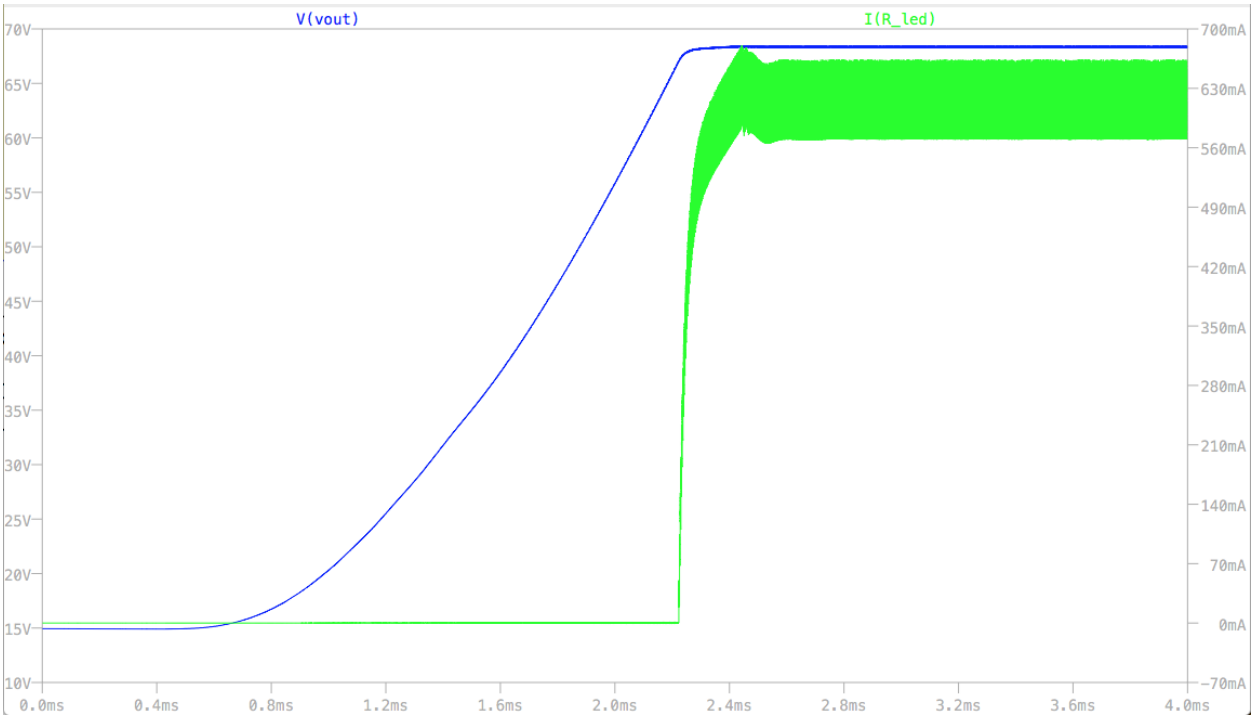


*Figure 4-7 Output Current and Voltage with 20V input and 68V output*

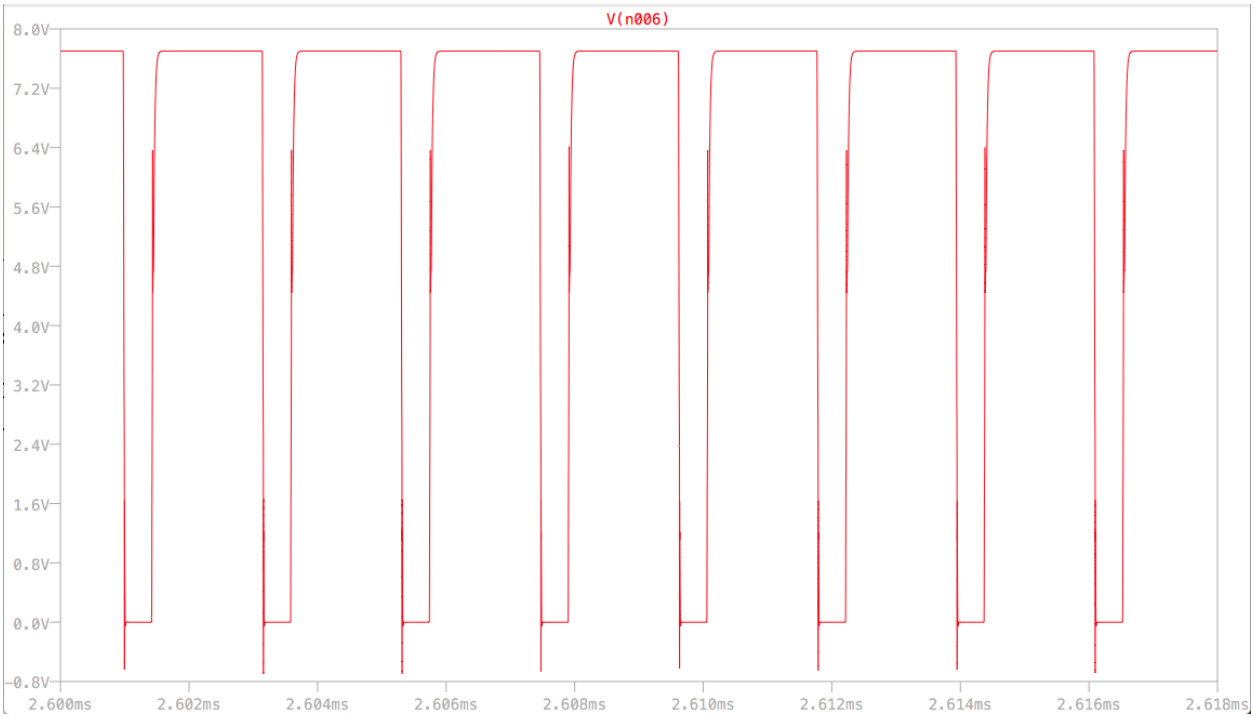


*Figure 4-8 Duty Cycle of 82% at 20V input and 68V output*

The last simulation is done at the opposite end of the spectrum, with the highest input voltage and lowest output voltage. This is done to demonstrate the ability of the converter to span a wide range of duty cycles, going as low at 7.1% shown in Figure 4-10. Figure 4-9 shows the

output at 9V, with some oscillation due to the output current. The expected duty cycle for this input-output condition is 12.3%, but due to the low duty cycle the controller alternates between a higher and lower duty cycle. In between each clock cycle, the output would droop a different amount resulting in different turn-on times for the NMOS.

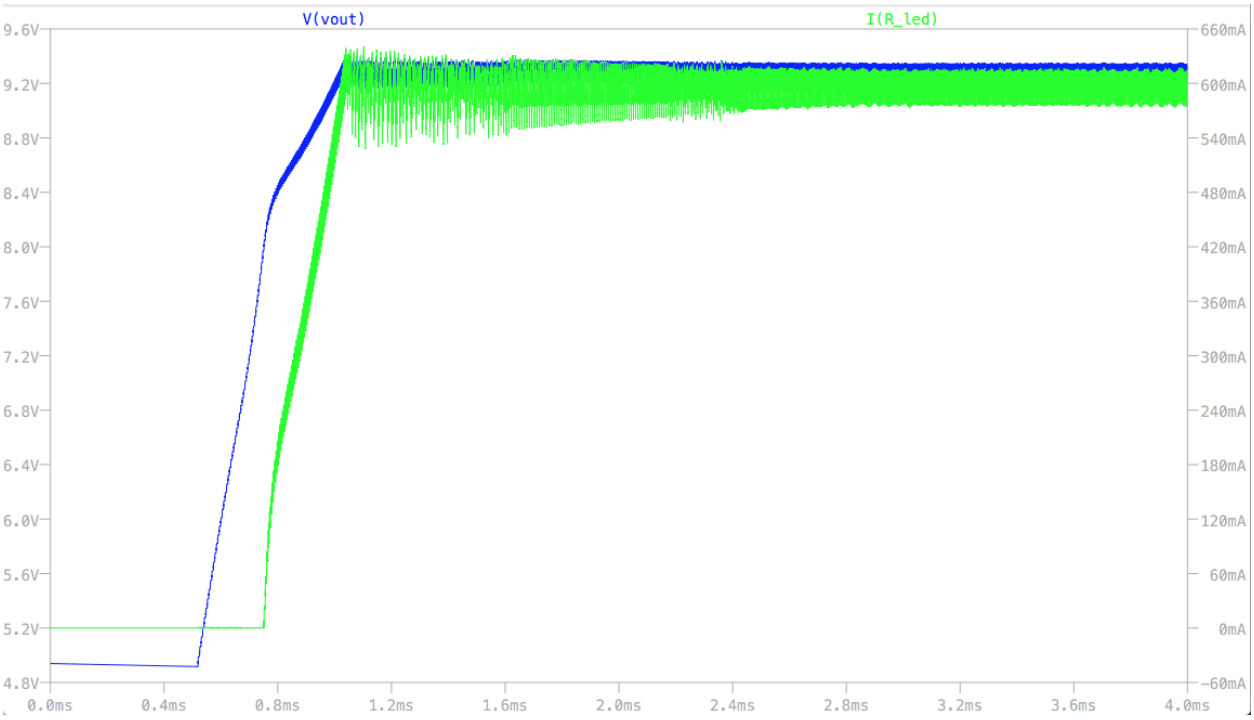


*Figure 4-9 Output Current and Voltage with 64V input and 9V Output*


*Figure 4-10 Duty Cycle between 18.1% and 7.1% at 64V input and 9V output*

These four simulations demonstrate the converter's ability to provide a steady 600mA current through the full input-output voltage range. If the converter is unable to do this, there would be little reason to favor the SEPIC topology over a buck or boost topology. Additional simulations show similar performance with a 300mA output current and PWM dimming.

# Chapter 5: Hardware Assembly and Test

## Board Layout

Due to the small size of the board (30mm x 45mm) and high density of signals near the microcontroller and supporting circuitry, a four-layer board was chosen to ease routing. While the routing was possible on two layers, there were concerns with the width of the power traces due to the crowding of signals around the LT3795 and Atmega328P. Using four layers allowed for wide power traces across the board without restraining the routing for smaller traces between other components.

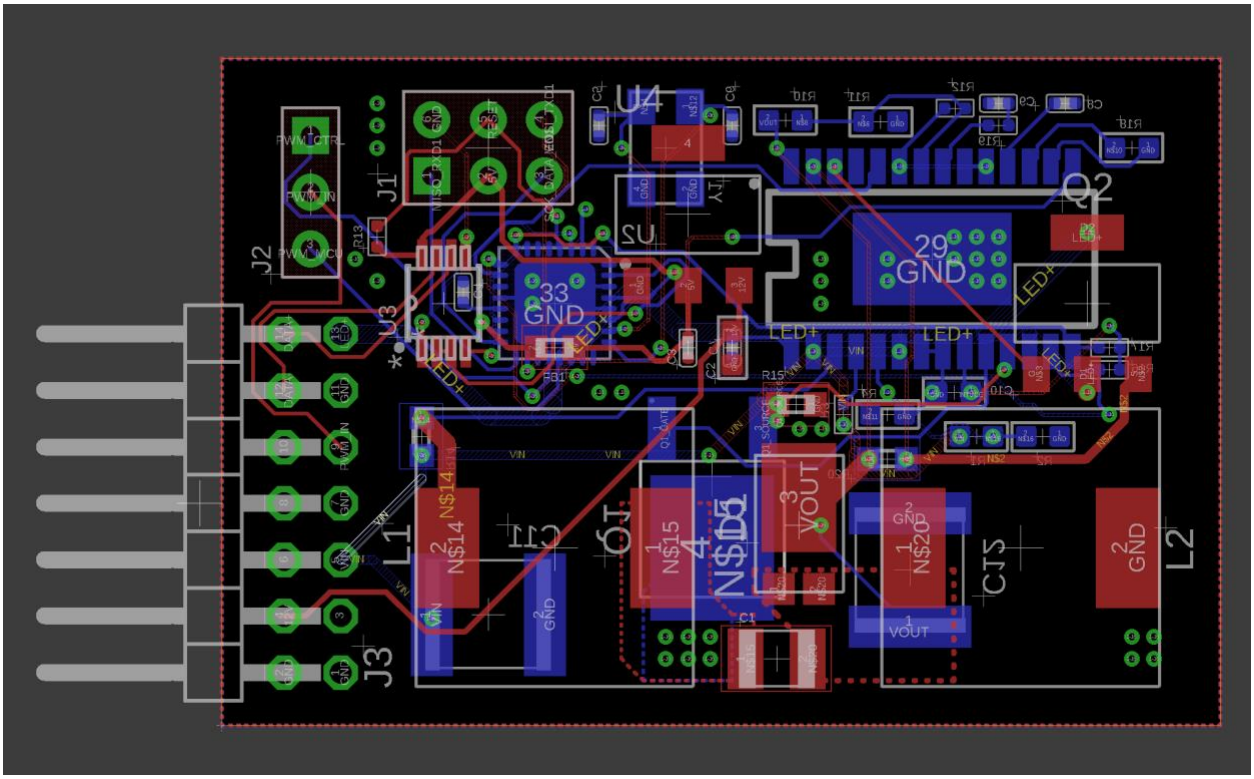


*Figure 5-1 Layout of 30mm x 45mm LED Driver Board*

Figure 5-1 shows the full layout of the board, including interior traces and component placements. In addition to the two-dimensional size constraint of the board, there was also a height limit of 12mm on the top side and 5mm on the bottom side. This meant that larger components such as the main coupling capacitor and the inductors could not be placed on the bottom of the

board. This resulted in the bottom of the board being used for the two main IC's as well as their required passive components. To help with ground loops, copper pours were placed on each layer of the board and tied to ground, as well as connected through VIA's where space allowed. This meant that ground connections should be low resistance and local to all components as needed.

## Fabrication and Assembly

Component selection was heavily influenced by the size of the board and even with small components many footprints were situated close together. All components are surface mount devices excluding the header pins. Because of the small packages and tight arrangement of components, fabrication and assembly were done by a company rather than on campus. Macrofab was used as a low quantity prototyping service that allowed for PCB manufacturing and SMD assembly on a low number of boards, in this case two. This greatly reduced the concerns of soldering the LT3795 and Atmega328P packages as well as the large number of 0402 passive components. This also was preferable since the inductor pads were located below the package and could not be easily soldered with a traditional iron.

After the layout and BOM were sent to the manufacturer, it became apparent that the LT3795 controller IC had the wrong footprint, meaning it could not be soldered onto the board. Figure 5-2 is an image sent from MacroFab highlighting the footprint mismatch which mandated an alternative solution. In industry, it would be typical to do a re-spin of the PCB and put the assembly on hold until the fixed layout was available, but this was not an option due to MacroFab policy. Instead, the LT3795 IC was soldered onto an adapter board which was then wired with 30 AWG wire to the footprint on the main board as shown in Figure 5-3. This introduced long trace resistances and inductances, as well as provided a perfect location for cross talk and EMI.

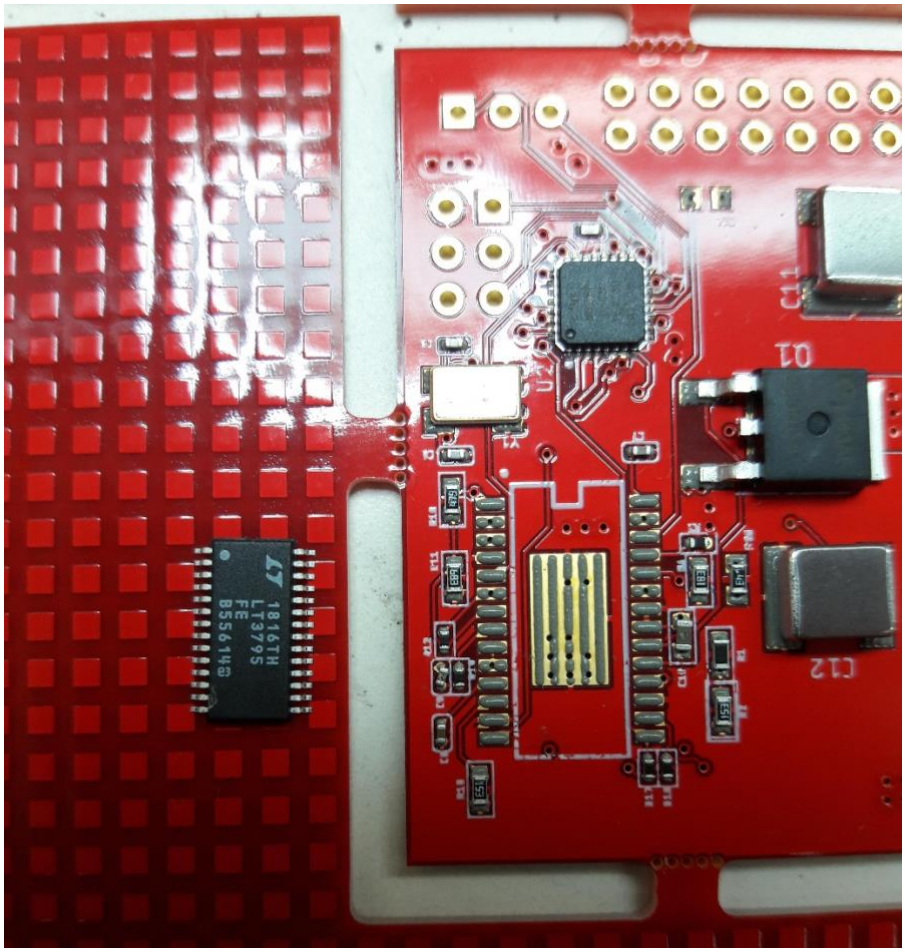


*Figure 5-2 MacroFab Support Sizing Mismatch*

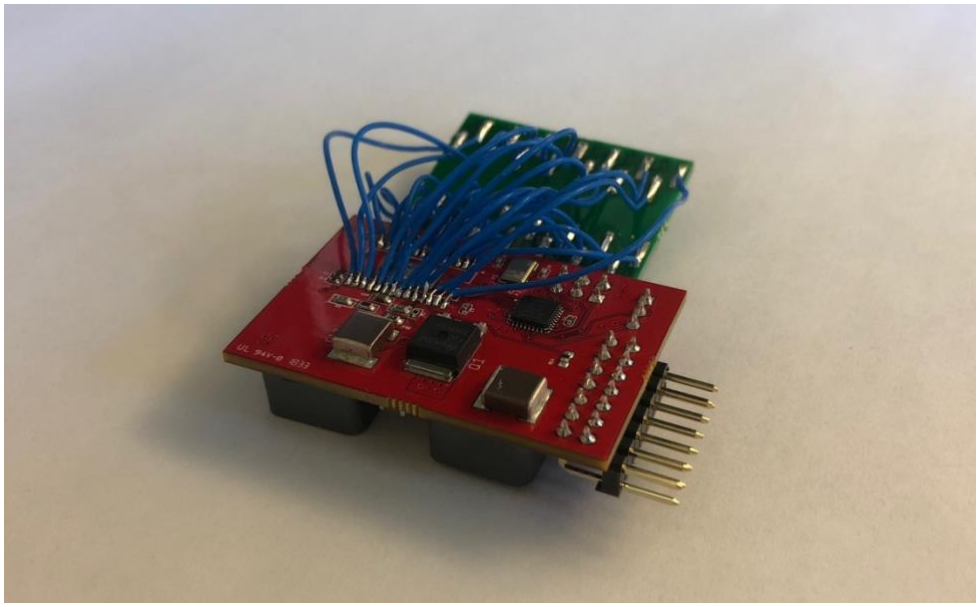

*Figure 5-3 Adapter Board Manually Wired to Main Board with 30AWG Wire*

# Lab Testing

The lab setup for testing this DC-DC converter consisted of a GW GPR-6060D DC power supply for input voltage, an Agilent U3401A digital multimeter used as an ammeter, a Rigol DG1062Z Function generator for the control signal, and a Clarostat 240-C power resistor decade box for the load. For additional measurement and oscilloscope captures a GW Instek GDS-1102B Oscilloscope was used. The measurement setup was to use the DC power supply in series with the digital multimeter to supply and measure input voltage and current, while loading the output of the converter with variable resistances to set output voltage. Since the project was designed to supply a constant current, the output voltage would vary with load resistance while current remained at the set 600mA. The function generator supplied a 4V square wave between 120-600Hz with varying duty cycle to modulate the voltage and current supplied to the load. Figure 5-4 show the lab setup with power supply, function generator, resistive load, and oscilloscope.

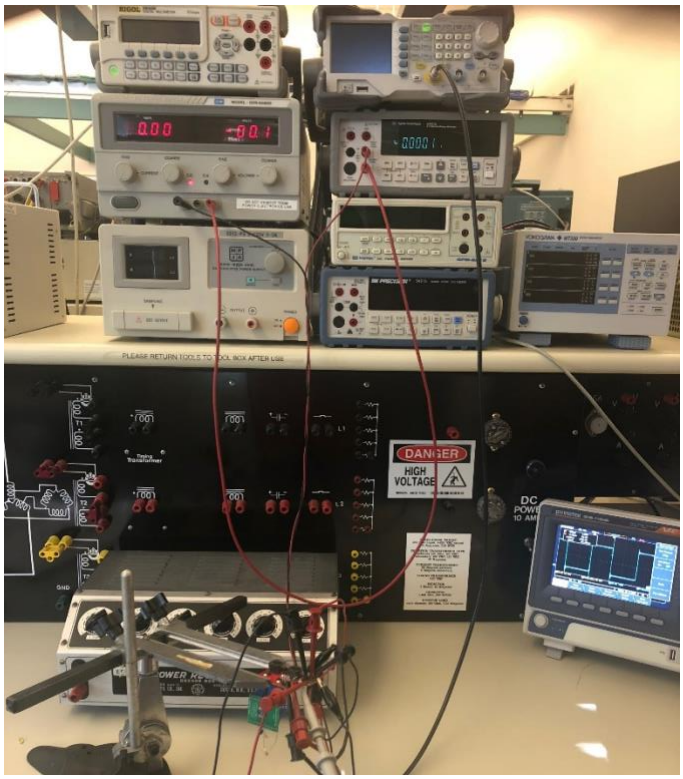


*Figure 5-4 Lab Setup in Power Electronics Lab 104*

# Results

The first test was to measure output voltage regulation at no load. Since this converter is a constant current device, measuring output voltage with no load attached would equate to measuring the maximum output voltage allowed by the controller, specified by the resistor network on the feedback pin. With a 55V input voltage and no resistor attached to the output the output voltage was 80.4V as shown in Figure 5-5.

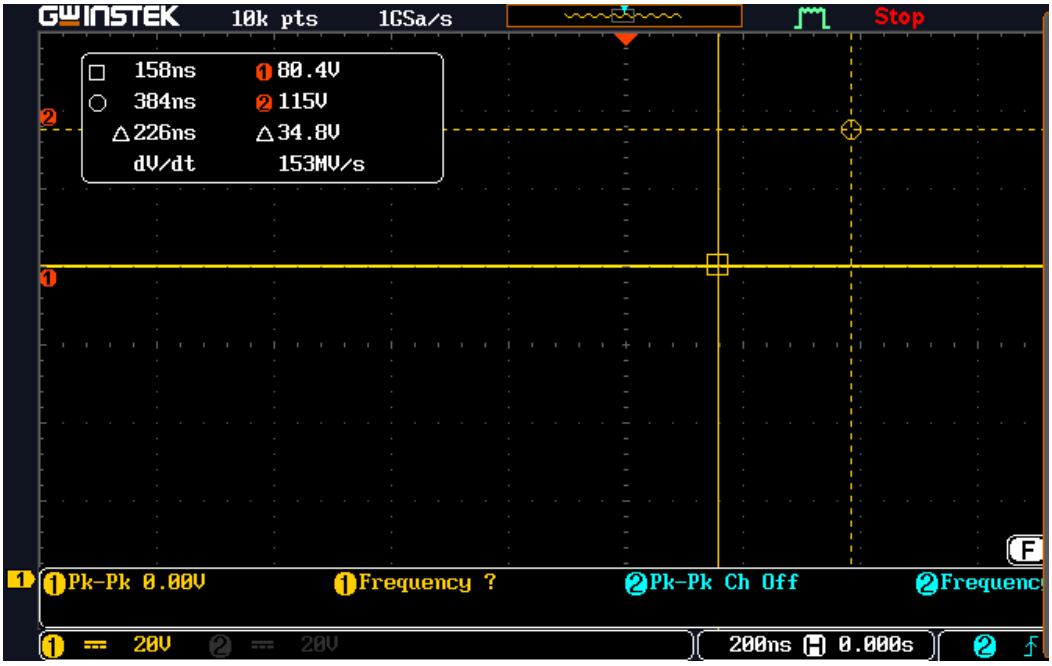


*Figure 5-5 80.4V Output with 55V Input and Open Load*

The next measurement was taken with the resistor decade box as a load to test output current. Figure 5-6 shows the output voltage of 39.2V across the 66Ω load, which is the result of a 594mA output current. This is close to the expected 600mA output current and can be attributed to variability in the 430mΩ LED sense resistor.

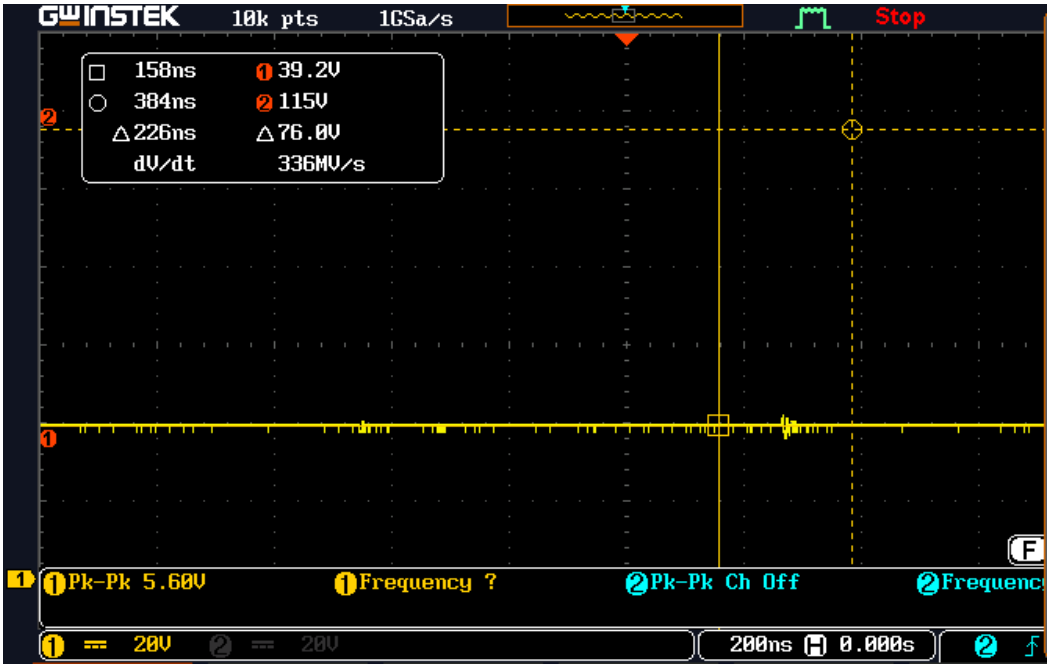


*Figure 5-6 39.2V Output with 55V Input and 66Ω Load*


*Figure 5-7 39.2V Output with 55V Input and 66Ω Load with AC coupled channel*

To check for voltage ripple, the oscilloscope input was set to AC coupling and measured a peak to peak ripple of 104mV. This ripple is 0.26% of the output voltage which is less than the 0.5% target used during the design. In addition to the voltage ripple, there were larger voltage

spikes that coincided with the switching frequency of 500KHz. This is likely due to crosstalk between the traces or the long wire running from the adapter board acting as an antenna. Since this was not related to the ability of the converter to regulate the voltage, it was not counted as part of the voltage ripple.

The next step was measuring performance with the PWM enabled between 120Hz and 600Hz. The function generator swung between 4V and 0V to emulate the signal generated by the onboard microcontroller. At the nominal frequency of 240Hz and duty cycle of 50%, the output voltage stayed consistent at 38.8V.

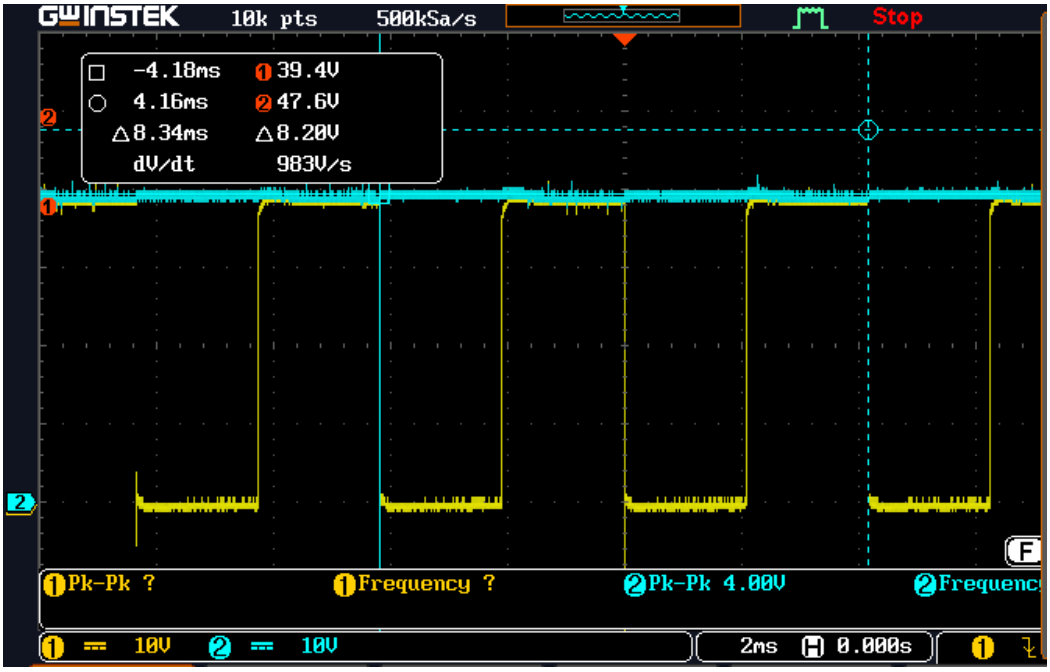


*Figure 5-8 Ch1: System Voltage output, Ch2: SEPIC Output Voltage before Output PMOS*

In Figure 5-8, channel 1 shows the output voltage across the 66Ω load resistor, while channel 2 shows the output voltage of the SEPIC before output MOSFET. During PWM operation, the output MOSFET switches on and off to provide an average current lower than 600mA based on the PWM duty cycle. In this case, the average output current was approximately 300mA since the duty cycle was set to 50%.

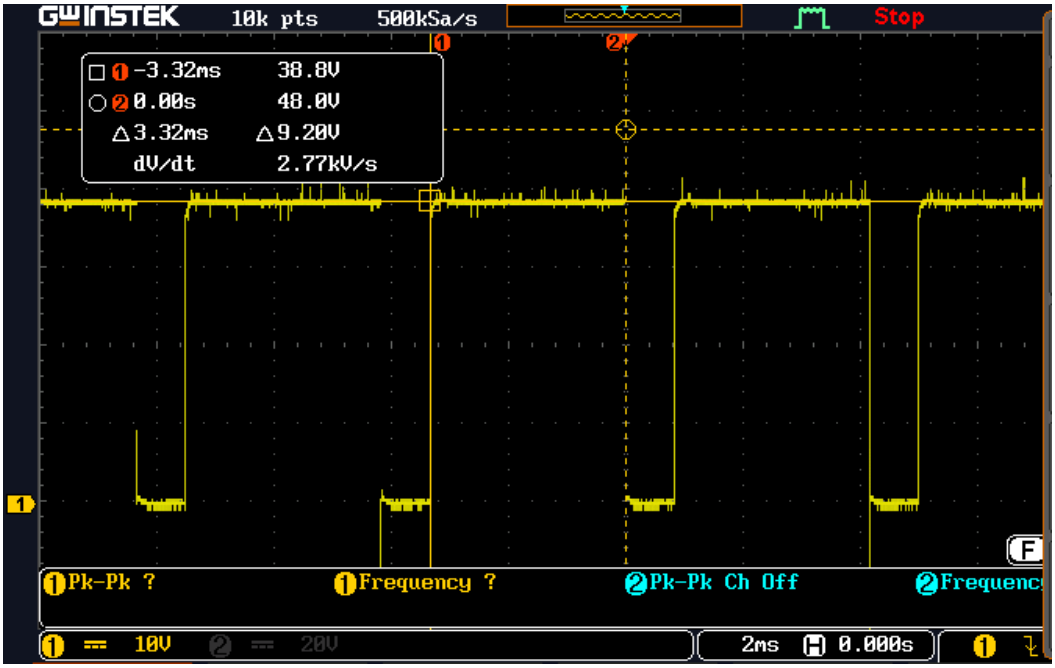


*Figure 5-9 38.8V Output with 55V Input and 66Ω Load at 80% Duty Cycle*

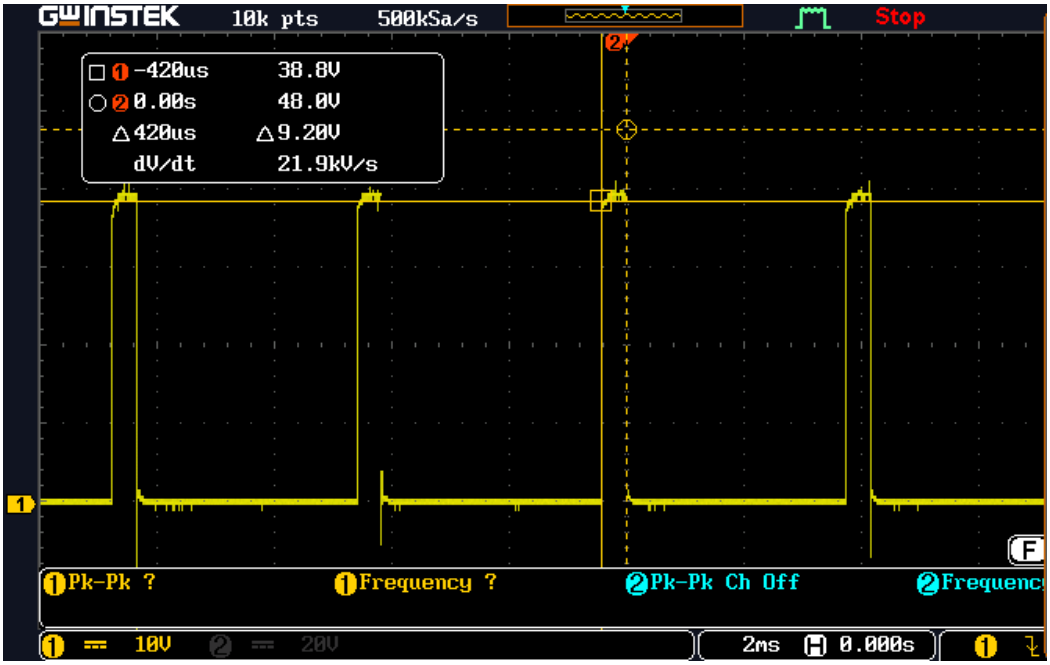


*Figure 5-10 38.8V Output with 55V Input and 66Ω Load at 10% Duty Cycle*

Increasing the duty cycle had little effect on the output voltage when the output MOSFET was turned on. The overall efficiency decreased slightly, partially due to the switching losses in the output MOSFET. Since the switching frequency is low at 240Hz, the switching loss has a small

effect on the system efficiency, reducing it from 87.4% to 85.9%. Figure 5-10 shows the same output voltage with a duty cycle of 10%, demonstrating that the converter can operate between 0% and 100%.

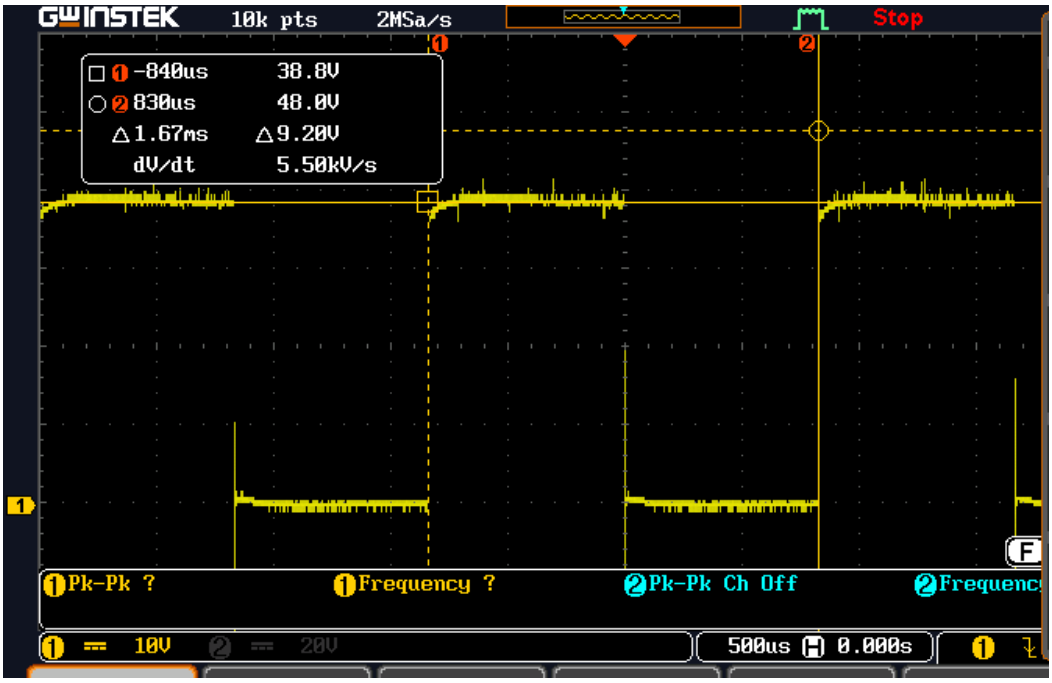


*Figure 5-11 38.8V Output with 55V Input and 66Ω Load at 600Hz PWM*

To continue testing the PWM control, the frequency was set to 600Hz to check the upper limit of the specification. Duty cycle was set to 50% to keep measurements consistent. The behavior in Figure 5-11 is as expected, with slightly more oscillation due to the increased switching frequency. This has a minimal effect on the output current of the device, especially in the specified LED application.

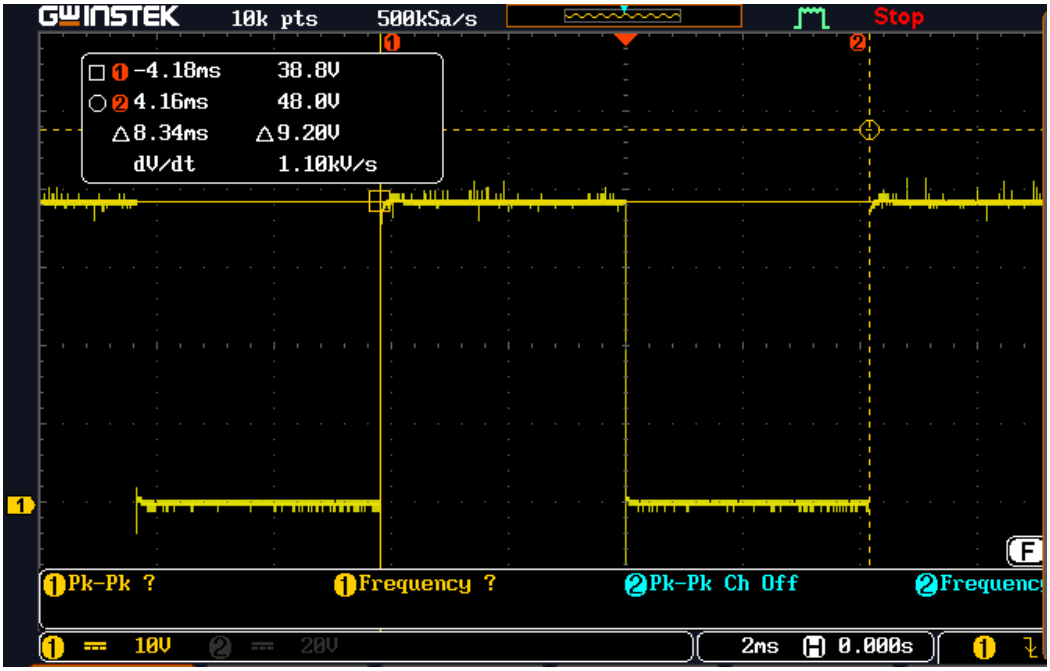


*Figure 5-12 38.8V Output with 55V Input and 66Ω Load at 120Hz PWM*

Setting the PWM frequency to 120Hz reduces the apparent oscillation on the output voltage, but still has little effect on the actual output. An increased frequency reduces the visible flickering of LEDs in operation. The efficiency comparison between these two frequencies is 84.3% versus 85.3% because the increased switching frequency introduces more switching loss in the output MOSFET.

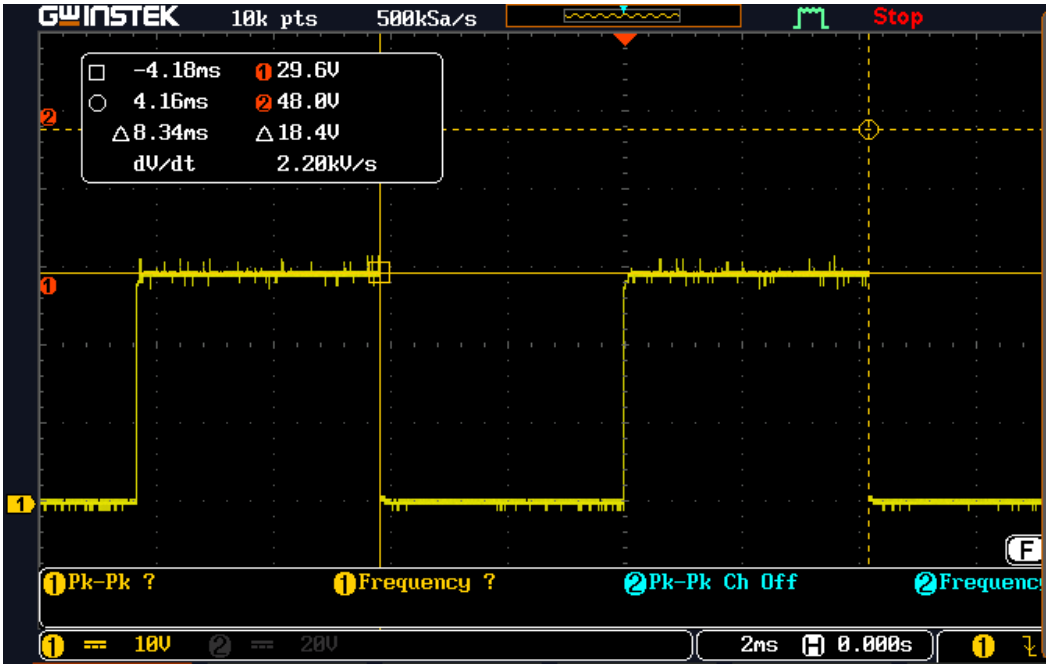


*Figure 5-13 29.6V Output with 55V Input and 50Ω Load*

The output resistance was decreased to 50Ω to test lower output voltage, resulting in the output voltage dropping to 29.6V. This is close to the expected voltage of 30V meaning the output current is remaining consistent with a lower load.

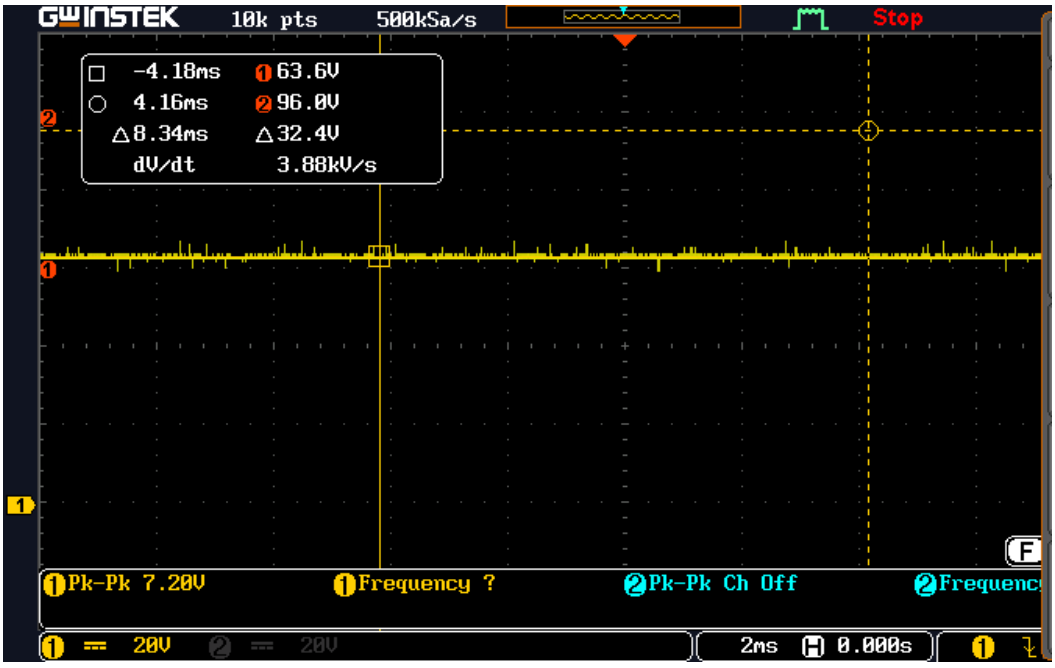


*Figure 5-14 63.6V Output with 55V Input and 110Ω Load*

Increasing the output resistance to 110Ω yields an output voltage of 63.6V, which is slightly off from the expected output voltage of 66V, but this can be explained by an inaccurate load resistance and slightly lower output current. The voltage feedback path of the converter allows the output voltage to drive up to 80V, as shown in the open load test, but is specified to drive up to 64V at 600mA in typical operation.

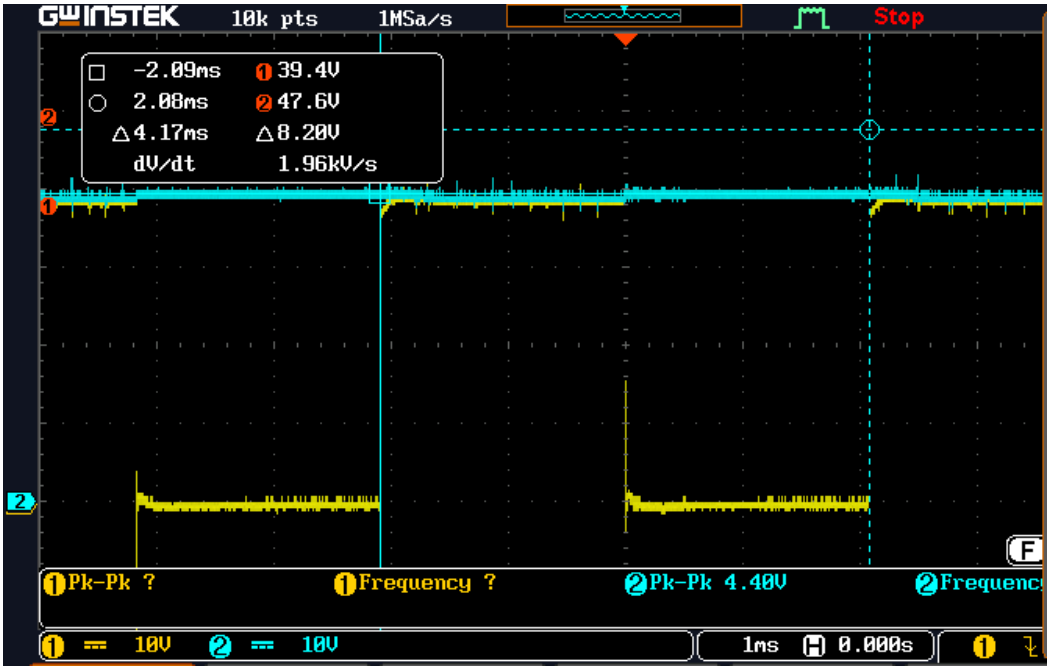


*Figure 5-15 39.4V Output with 50V Input and 66Ω Load*

The converter is also designed to operate at different input voltages, in Figure 5-15 the input voltage is reduced to 50V, but the output voltage remains consistent with previous tests. The same output voltage is found when increasing the input voltage to 60V. Unfortunately, due to the extra trace lengths added to each pin of the controller IC, the logic block of the controller creates faults and drives the system output low at the switching frequency of the primary MOSFET. This means that the device in the current assembly is not able to operate with an input below 40V without a 500KHz flickering.

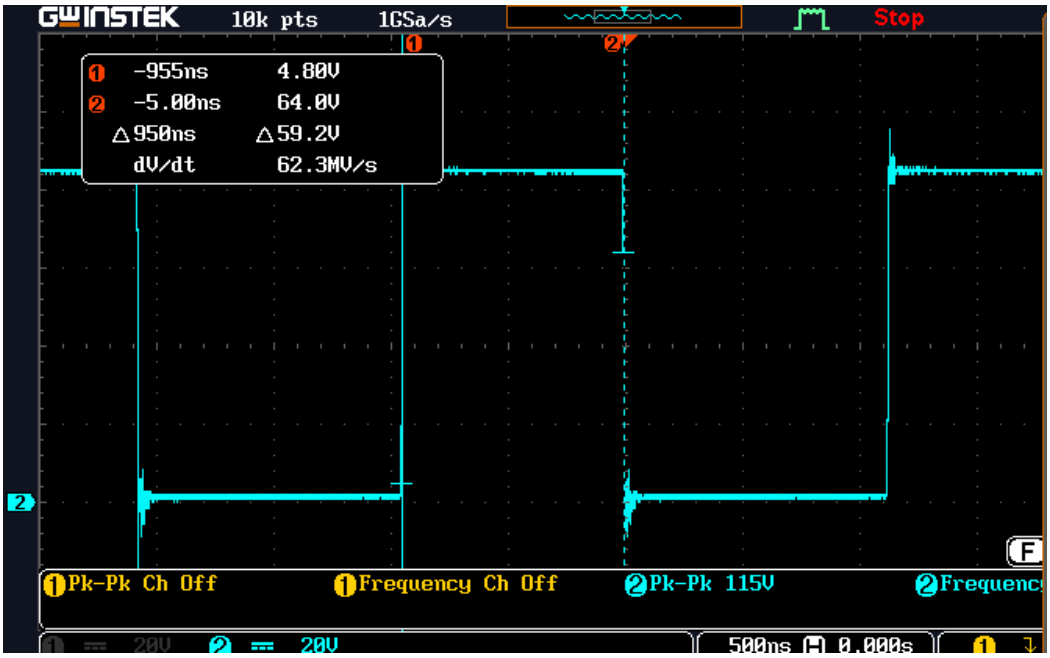


*Figure 5-16 Primary Switching Node with 52.5% Duty cycle at 500KHz*

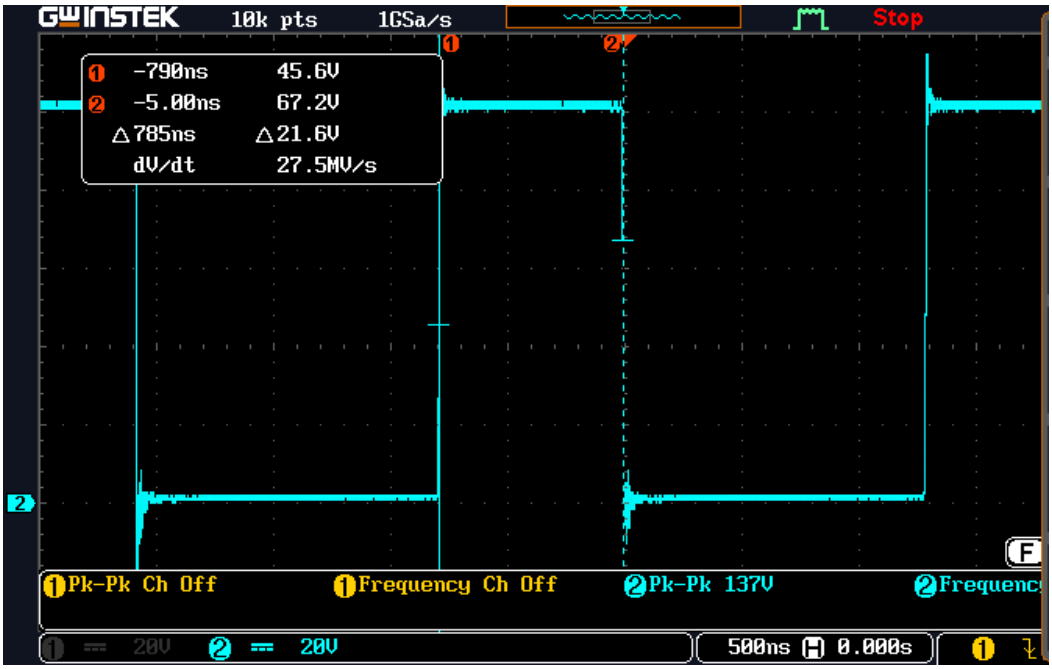


*Figure 5-17 Primary Switching Node with 60.1% Duty cycle at 500KHz*

Figure 5-16 shows the switching node oscillating at 500KHz with a duty cycle of 52.5%. Since the pictured trace is switching node voltage, the duty cycle of the switch is measured by the time spend at 0V. This is because the first half of the topology resembles a boost converter, with the primary MOSFET pulling the inductor down to ground. The duty cycle is expected to be

approximately 50%, since the input and output voltages are similar values. When the output voltage is increased in Figure 5-17, the duty cycle of the switch increases as well, in this case going up to 60.1%, which is close to the expected duty cycle of 61.7% for an input voltage of 38.6V and output voltage of 62.4V.

Unfortunately, due to the complications during the manufacturing and assembly, the LT3795 controller IC could not be directly soldered onto the main board and instead had to reside on an adapter board. This meant that each pin was no longer as local to the system as it was designed to be, and a finite amount of inductance, capacitance, and resistance was added to each trace. This resulted in issues with the board functioning in some parts of the input and output ranges, and inconsistent behavior of the internal logic of the controller.

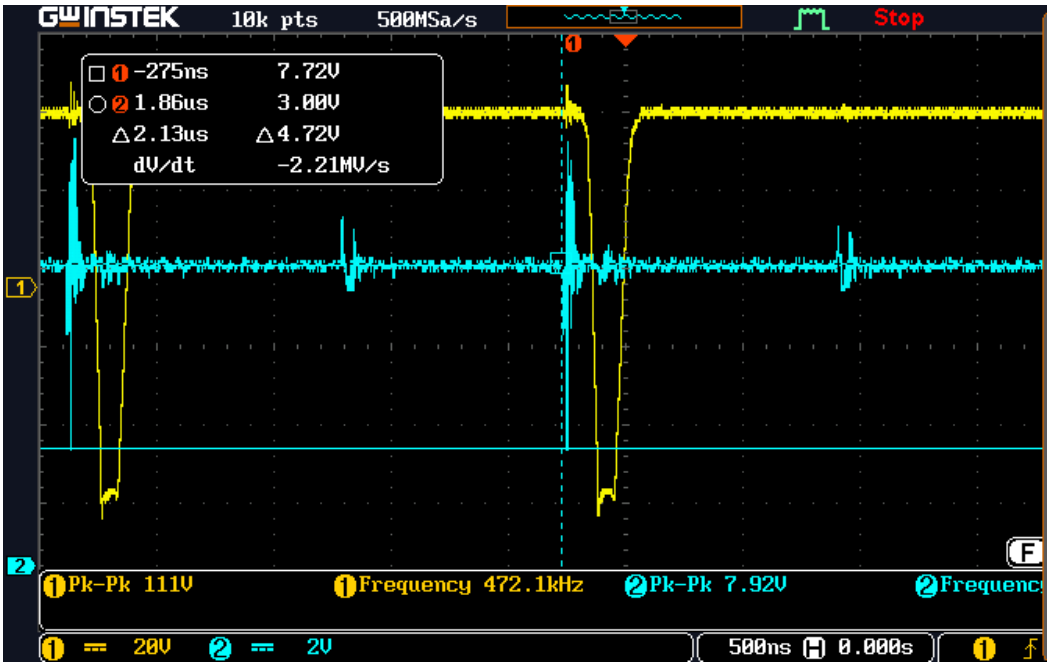


*Figure 5-18 Output Voltage Dipping Due to Internal Vcc Faults*

Figure 5-18 shows one of the more widespread issues where the internal Vcc pin, shown in channel 2, would suffer from voltage spikes induced from elsewhere in the system. This would cause the logic block of the controller to see a fault and turn off the output MOSFET at the switching frequency of the device. While a 500KHz oscillation would most likely not be visible on the output LED's, the average output current would be decreased, and the system would be under increased stress. The output PMOSFET was selected with a 600Hz maximum switching

frequency and was prioritized to have low RDSon with the trade-off of higher gate capacitance. While the MOSFET is capable of switching at a 500KHz frequency, this generates much more power loss through heat, meaning efficiency is much lower and the energy wasted as heat changes the behavior of the device.

*Table 5-1 Numerical Test Results Summarized*

| Parameter | Specification | Hardware Measurement | Additional Comments |
|---|---|---|---|
| Output Voltage Range | 9V-68V | 20V-68V | Output voltage was limited due to inconsistent logic block performance |
| Output Voltage Maximum | 80V | 80V | |
| Output Current Range | 0A-600mA | 0A-600mA | |
| Input Voltage Range | 20V-64V | 26V-64V | Input voltage correlated heavily with logic block performance, so intermittent faults would appear within the input voltage range |
| PWM Control | 120Hz-600Hz 0%-100% Duty Cycle | 120Hz-600Hz 0%-100% Duty Cycle | |

# Chapter 6: Conclusion

The goal of this project was to design and test a DC-DC constant current power supply for LED strings in a commercial application. This involved researching converter topologies, designing a power supply circuit around a controller IC, and creating a board layout to fit the required components for assembly. This finalized controller would be part of a larger system infrastructure to facilitate the design and construction of DC powered smart buildings.

The project was directed by a core set of specifications requiring a wide input and output voltage range with high efficiency, which led to choosing the SEPIC topology. The LT3795 controller was selected as an IC capable of providing the control logic while accepting the higher than average input and output voltages. Designing the complete circuit required selection and sizing of power components ranging from coupling capacitors to power inductors as well as feedback resistor networks and controller compensation networks. The completed design was then turned into a layout that was highly space constricted, only measuring 30mm x 45mm with a 12mm height limit. Due to the small size of the board, the components also were physically sized to fit the large number of passive components near their relevant subsystems.

Once the board was designed and assembled, testing revealed that the converter did not fully supply the proper output current in the input and output range, but it was still able to perform its intended role within a subsection of this range. The efficiency tended to be 10% - 15% lower than the simulated efficiency, but this can be partially explained by the suboptimal assembly required to work around manufacturing difficulties.

The next step for improving this design is to examine the feedback loops in the control system to make sure they are robust enough to withstand a wider range of operating conditions, as well as examine the performance of the board in different thermal conditions. Thermal simulation was not included in the design stage but would be very relevant in the final commercial application. In addition, the layout could be reexamined to minimize cross talk between switching signals, widen power traces to reduce resistive losses, and fix the footprint of the LT3795 IC to allow for much lower trace inductances.

# Works Cited


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[7] Diodes Incorporated, "Diodes Incorporated ZXMP7A17GQ 70V P-Channel Enhancement Mode MOSFET," March 2015. [Online]. Available: https://www.diodes.com/assets/Datasheets/ZXMP7A17GQ.pdf.

# Appendix C: Bill of Materials

| Part | Part Number | Count | Unit Cost | Cost |
|---|---|---|---|---|
| C11, C12 | 22201C106MAT2A | 4 | $2.89 | $11.56 |
| J3 | 61301421021 | 2 | $1.21 | $2.41 |
| U2 | ATMEGA328P-MU | 2 | $2.52 | $5.05 |
| FB1 | BLM18KG601SN1D | 13 | $0.12 | $1.59 |
| C10 | CGB3B1X5R1A475M055AC | 3 | $0.31 | $0.92 |
| Y1 | ECS-160-18-30B-JEM-TR | 3 | $0.71 | $2.12 |
| R1 | ERJ-3EKF2003V | 13 | $0.12 | $1.59 |
| R10 | ERJ-3GEYJ475V | 13 | $0.12 | $1.59 |
| R11 | ERJ-3GEYJ683V | 13 | $0.12 | $1.59 |
| R20 | ERJ-3RQFR43V | 13 | $0.23 | $3.02 |
| Q1 | FDD390N15A | 2 | $1.28 | $2.56 |
| C5, C6 | GJM1555C1H100FB01D | 15 | $0.28 | $4.20 |
| C7, C8 | GRM155R61E104KA87D | 15 | $0.12 | $1.83 |
| C9 | GRM155R71E103KA01D | 13 | $0.12 | $1.59 |
| C1 | GRM32ER71K475KE14L | 2 | $1.23 | $2.46 |
| U4 | LD1117S50CTR | 3 | $0.51 | $1.54 |
| U1 | LT3795EFE#TRPBF | 2 | $10.43 | $20.85 |
| C3, C4 | MF-CAP-0402-1uF | 4 | $0.07 | $0.29 |
| C2 | MF-CAP-0603-1uF | 2 | $0.06 | $0.12 |
| J2 | MF-CON-2.54mm-01x03 | 2 | $0.67 | $1.33 |
| J1 | MF-CON-2.54mm-2x3 | 2 | $0.27 | $0.54 |
| R16, R17 | MF-RES-0402-100K | 4 | $0.09 | $0.34 |
| R13 | MF-RES-0402-10K | 2 | $0.12 | $0.24 |
| R3 | MF-RES-0402-1M | 2 | $0.12 | $0.24 |
| R19 | MF-RES-0402-4.7K | 2 | $0.09 | $0.17 |
| R12 | MF-RES-0402-470K | 2 | $0.07 | $0.15 |
| R18, R2 | MF-RES-0603-15K | 4 | $0.06 | $0.24 |
| R4 | MF-RES-0603-18K | 2 | $0.06 | $0.12 |
| D1 | PDS4150-13 | 2 | $1.60 | $3.20 |
| R14, R15 | RU1608FR020CS | 5 | $0.49 | $2.44 |

| | | | | |
|---|---|---|---|---|
| U3 | SN65HVD3085EDGKR | 2 | $3.70 | $7.39 |
| L1, L2 | SRR1280-390M | 4 | $1.37 | $5.46 |
| Q2 | ZXMP7A17GQTA | 2 | $1.01 | $2.02 |
| PCB | N/A | 2 | $14 | $28 |
| Labor And Assembly | N/A | 1 | $40.66 | $40.66 |
| | | | Total | $159.42 |

# Appendix D: Analysis of Senior Project Design

Project Title: Design and Test of Wide Input and Output Constant Current LED Driver

Student's Name: Kean Wee Student's Signature: _____

Advisor's Name: Taufik Advisor's Initials: _____ Date: _____

**Summary of Functional Requirements:**

The goal of the project is to design a contained system that can convert 20V-64V input voltage into a constant current output of 600mA to an LED string with turn on voltage between 9V-68V with PWM dimming control.

**Primary Constraints:**

One of the primary limitations was the size of the board, which was required to be 30mm x 45mm, with a height limit of 12mm on the top side and 5mm on the bottom side. This was quite small for prototyping and left little room for routing and limited the size of components. The sensitivity of the control loop also meant that the layout was critical to the performance of the system and had to be tested as it would be manufactured on a large scale.

**Economic:**

The development of this project would create jobs related to the manufacturing of the design, as well as installation of the design as part of the larger infrastructure. If the cost of the manufactured device can be kept down, this would be a competitive solution for building contractors to install in future developments.

**If manufactured on a commercial basis:**

If the design is manufactured on a commercial basis, the number of products sold would depend on the number of buildings designed with the infrastructure in mind. Since each device should be able to supply for more than 50 LEDs, the number of devices sold would directly relate to the number of rooms being lit by the Lumencache system. The cost of manufacturing the prototype could be estimated to be $70 per board, but this number decreases greatly as it is scaled

up. The price could realistically be brought down to $20 per board and selling each unit for $40 would yield a profit per device of $20.

**Environmental:**

Since the goal of the DC building infrastructure is to minimize wasted energy in electric conversions, the environmental impact of the design would be a decrease in waste due to lighting buildings. Since the DC building infrastructure also supports intelligent communication built into each power supply, more energy can be saved through disabling or dimming lights automatically when users might forget or not be present.

**Manufacturability:**

The size restriction of the design has the benefit of producing a board that can easily be mass manufactured. With only four layers and a small board area, there are many facilities available in the world to produce these designs. The parts are relatively easy to source, and many components can be substituted with parts of similar specifications.

**Sustainability:**

The device specifications were built around an input interface to a wider infrastructure which allows for easy upgrading of the design and swapping of parts down the line. As a smaller part of a larger system, this project can be revised and replaced in the field as long as the input pinout remains the same. Since no assumptions where made on the input power or signals other than their voltage ranges, it should be easy to "plug and play" with newer models of this design in the future. If the device breaks, it can also be easily replaced since the LED string being powered is not directly connected to the board.

**Ethical:**

There are not many ethical issues with this design other than the potential inability of the design to perform to user expectations. As long as the capabilities of the device are properly stated, user expectation should be in line with device performance.

**Health and Safety:**

The PWM dimming can potentially cause user discomfort based on the frequency used. With the lower frequency of 120Hz, it's possible that a humming noise could be generated, and users with sensitive eyes might be able to detect flickering and feel discomfort.

**Social and Political:**

This design is more beneficial to new developments rather than old. While DC power may be appealing to many, it makes the most sense to supply this kind of design and infrastructure where buildings are new, rather than retrofitted.

**Development:**

The development of this project was very educational since it required high attention to detail from the beginning to end. The work began with research on topologies available for constant current supplies and carried into selection of controllers and components. The design stage required use of simulation tools such as LTSpice, as well as schematic and layout tools like EagleCAD. The layout portion of the project was especially educational since trace width for power traces was incredibly important, as well as creation of custom footprints according to datasheets, and placement of components based on locality to their related subsystems. Lab testing provided an opportunity for in-depth debugging, especially since the design did not initially work when it was brought into the lab. Communication with an exterior manufacturing company allowed for problem solving similar to that done within industry when last minute issues arise.