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Improving Signal To Noise Ratio And Time Resolution For Solid-State Nanopore Measurements

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Abstract
Nanopores have seen broad applicability as single-molecule sensors because of their spatiotemporally localized transduction and high intrinsic gain. In this dissertation, we seek to increase the bandwidths accessible to nanopore measurements through improvements to nanopores, associated measurements electronics, and their integration. Solid-state pores, in particular, can generate signals that are often more than an order of magnitude larger than their biological counterparts. These larger signals make solid-state pores much more amenable to high-bandwidth measurements. Earlier work showed DNA translocation measurements with sub-microsecond temporal resolution using silicon nitride nanopores. In this dissertation, we further improve the temporal resolution to 100 ns by a recently developed CMOS nanopore amplifier (CNP2) with 10 MHz bandwidth capacity using silicon nitride pores thinned with electronic beam techniques to < 3 nm thickness, with pore diameter compatible for ssDNA that hugs the molecules as it translocates. Overall signal-to-noise-ratio-limited bandwidth is optimized through appropriate choice of pore size, salt and bias voltage. To further reduce Cpore, we are passivating silicon-nitride pores with thick dielectrics. We have previously reported on fused-silica based solid state membrane carrying platform which allows us to reduce Cpore to values < 1 pF. We also make use of this versatile, low-capacitance platform to suspend other thin, two-dimensional membrane such as MoS2 to take advantage of the atomic thickness of these 2D materials to increase spatial resolution. In this dissertation, we present data of improvements in DNA translocation recordings in both time resolution and signal to noise ratio (SNR) from combining our custom electronics with these low-capacitance, high-conductance ultra-thin pores. The ultra-low measurement noise allows us to observe an excess current dependent noise due to the pore itself, and the rich dynamics as DNA translocate through the nanopore. We also explore other applications beyond single nanopore such as nanopore arrays and nanoribbon-nanopore devices.

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IMPROVING SIGNAL TO NOISE RATIO AND TIME RESOLUTION FOR SOLID-STATE NANOPORE MEASUREMENTS

Chen-Chi Chien

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ABSTRACT

IMPROVING SIGNAL TO NOISE RATIO AND TIME RESOLUTION FOR SOLID-STATE NANOPORE MEASUREMENTS

Chen-Chi Chien

Marija Drndić

Nanopores have seen broad applicability as single-molecule sensors because of their spatiotemporally localized transduction and high intrinsic gain. In this dissertation, we seek to increase the bandwidths accessible to nanopore measurements through improvements to nanopores, associated measurements electronics, and their integration. Solid-state pores, in particular, can generate signals that are often more than an order of magnitude larger than their biological counterparts. These larger signals make solid-state pores much more amenable to high-bandwidth measurements. Earlier work showed DNA translocation measurements with sub-microsecond temporal resolution using silicon nitride nanopores. In this dissertation, we further improve the temporal resolution to 100 ns by a recently developed CMOS nanopore amplifier (CNP2) with 10 MHz bandwidth capacity using silicon nitride pores thinned with electronic beam techniques to < 3 nm thickness, with pore diameter compatible for ssDNA that hugs the molecules as it translocates. Overall signal-to-noise-ratio-limited bandwidth is optimized through appropriate choice of pore size, salt and bias voltage. To further reduce C_{pore}, we are passivating silicon-nitride pores with thick dielectrics. We

have previously reported on fused-silica based solid state membrane carrying platform which allows us to reduce C_{pore} to values < 1 pF. We also make use of this versatile, low-capacitance platform to suspend other thin, two-dimensional membrane such as MoS_2 to take advantage of the atomic thickness of these 2D materials to increase spatial resolution. In this dissertation, we present data of improvements in DNA translocation recordings in both time resolution and signal to noise ratio (SNR) from combining our custom electronics with these low-capacitance, high-conductance ultra-thin pores. The ultra-low measurement noise allows us to observe an excess current dependent noise due to the pore itself, and the rich dynamics as DNA translocate through the nanopore. We also explore other applications beyond single nanopore such as nanopore arrays and nanoribbon-nanopore devices.

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Chapter 1

Introduction

Nanopores are nanometer-sized holes in thin membranes. They are used in many applications in nanoelectronics and nanomedicine, from detecting and studying different conformations of small bio-molecules, such as DNA [19, 26, 32, 57, 64, 83, 96, 109], RNA [86, 100], and proteins [56, 67, 99, 108], to desalinating water [12, 43, 91], synthesizing nanoparticles [97], and generating power [25]. The research in this dissertation focuses on solid-state nanopores as single-molecule sensors. Improvements on these solid-state nanopore devices are the primary focus of this work, specifically in terms of increasing the signal to noise ratio, and also increasing the measuring bandwidth. The first aim of increasing the signal to noise ratio was addressed by passivating thick dielectric materials around the nanopore to reduce noise. The second aim of increasing the measuring bandwidth was accomplished by the new custom-made complementary metal-oxide-semiconductor (CMOS) nanopore amplifier to extend the measurement bandwidth. These new tools and results enable researchers to further

the understanding and expand the functionality of nanopore devices as biomolecule sensors.

1.1 Basics of Nanopores

In experiments using solid-state nanopores, an ion current will flow through a molecular-scale-size hole in a thin membrane immersed in electrolyte solution under the influence of a driving transmembrane voltage. When a molecule, such as DNA or protein, is driven into the nanopore by the bias voltage, its presence blocks this current, and the magnitude of this blockage can be correlated to the molecule's physical properties, such as its volume and charge. The idea was similar to coulter counter where it was used to count and size the cells or bacteria in the solution. With the size of the pore becoming nanometer sized, the detection of a single-molecule as it translocates through the nanopore becomes possible.

1.1.1 Solid-state nanopore and biological nanopore

There are two main categories of nanopores: biological and solid-state nanopores. (Fig. 1.1) Biological pores are functional proteins or pore-forming peptides that sit on top of lipid bilayers. They could be found in naturally occuring biological systems, and are usually ion pumps controlling the movements of ions and molecules through the cell. Solid-state nanopores are made of inorganic thin-membrane materials such as silicon nitride. Recently, after the discovery of graphene, families of two dimensional materials such as boron nitride, and metal dichalcogenides (MoS_2,

WS_2, etc.) are popular research topics for nanopore because of their atomic thickness. The nanopore is formed usually by focused electron beam in a transmission electron microscope (TEM). [96, 100] Multiple other ways are developed to drill a nanopore on these membranes such as focus ion beam, [59] helium ion beam, [106] ebeam lithogrophy, [98] and dielectric breakdown, [27, 54] with each having its advantages and applications.

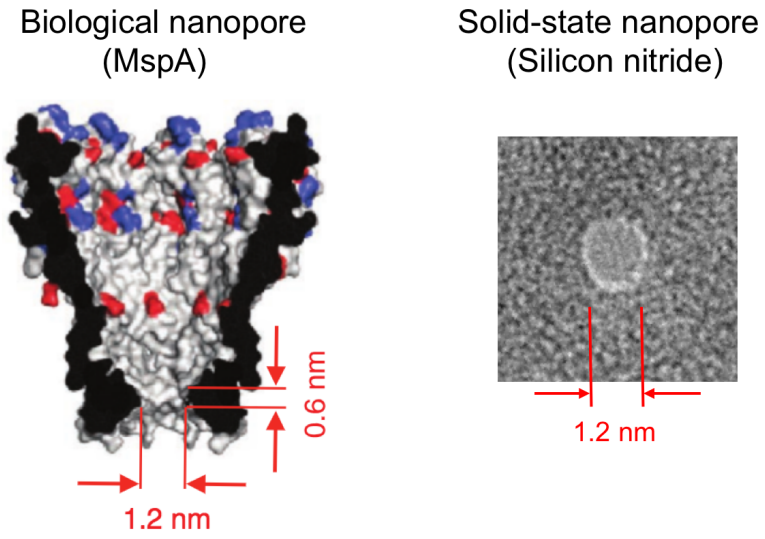

Figure 1.1: Left image is the image of the crystal structure of a MspA pore. Right image is a TEM image of a silicon nitride pore.

1.2 Nanopore for DNA sequencing

One of the major potential applications for the nanopore as a biomolecule sensor is fast DNA sequencing. Deoxyribonucleic acid, also known as DNA, is a strand of nucleotides consists of four nucleobases: cytosine [C], guanine [G], adenine [A] or thymine [T]. The sequence of these nucleobases carrys genetic information. Being able to sequence the DNA quickly and correctly hence has upmost significance in medical research since these DNA sequences help us further our understanding in genetics, which govern all living organisms. There are many commercially available DNA sequencing methods that produce reliable results, such as the sequencing-bysynthesis technology by Illumina. However, the current methods for DNA sequencing still suffer from low through-put, short read length and high cost, therefore there is much to be desired. Nanopore hence emerged as a candidate for high-throughput, long read length and low cost next generation DNA sequencing method. DNA strand could be driven through the nanopore by a biased voltage; as the different bases pass through the pore, due to the size differences of the A,T,C,G bases, one could read out the signal as it passes through the nanopore. A cartoon schematic in Fig. 1.2 shows the basic of DNA sequencing by nanopore. Recent development in engineered mutants of MspA pore supported by lipid bilayer membranes, which tracks the real-time operation of single enzyme molecules operating on a strand of DNA, have shown preliminary results in identifying DNA nucleotide bases. [57, 63] There are also several solid-state nanopore results using thin silicon nitride, and MoS_2 nanopores showing the ability to distinguish segments of homopolymers. [26, 96] Yet no nanopore technology as of now has exhibited the same reliability as the commercially available technology. This

potential application of nanopores for next generation DNA sequencing has been a holy grail for researchers studying and working on nanopores.

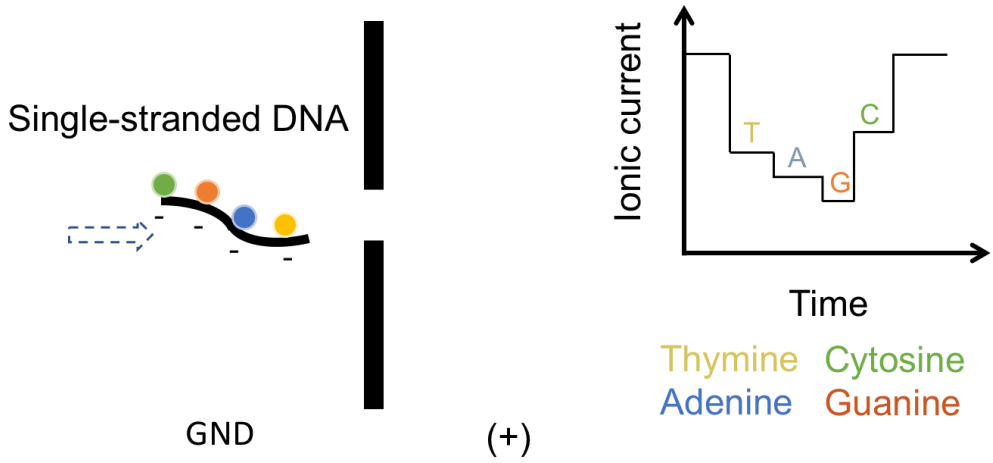

Figure 1.2: Single stranded DNA has 4 nucleobases- cytosine (C), guanine (G), adenine (A) and thymine (T). When it is driven through the nanopore by a bias voltage, the different sizes of each base would block the ionic current differently resulting in ionic signal changes allowing DNA sequence being read out directly.

1.3 Advantages and challenges of current solid-state nanopore technology

The robustness and tunability are the advantages of solid-state nanopores compared to biological nanopores. Since these nanopores are made in precise instruments such as TEM, we could control the size of the nanopore for our desired analytes. For instance, solid-state nanopores can be drilled at 20nm in size to measure nanoparticles,

or can be made as small as 1nm to measure single stranded DNA going through the pore. They share sizes comparable to protein pores but with signal levels that are at least an order of magnitude higher due to the thinner extent of the solid-state pores (sometimes down to the single nanometer range), and due to the higher trans-membrane voltages that can be supported across solid-state membranes.[96] Unlike biological pores that have to work in specific conditions, these solid-state membranes could also withstand extreme measuring environment such as acidic or basic environments, or high temperature. These characteristics make solid-state nanopore an ideal single-molecular sensor.

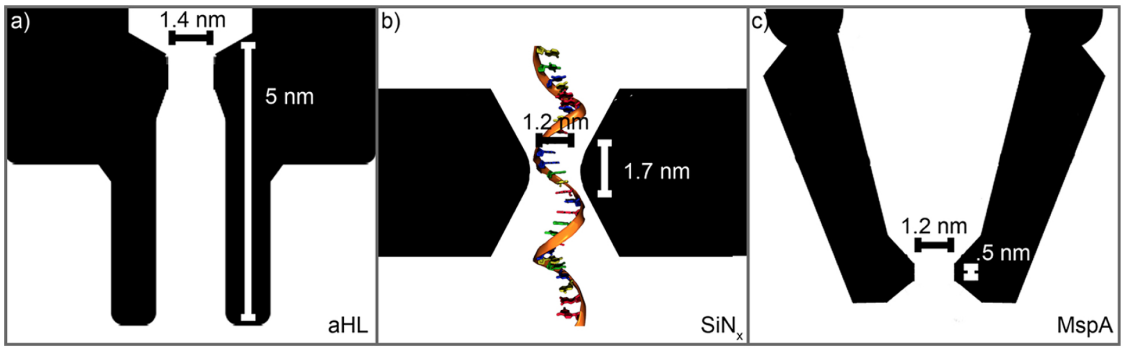

Figure 1.3: The comparable dimensions of solid-state and biological nanopores. (a)α-hemolysin (b)silicon nitride (c) MspA. Adapted with permission from [96].

However, there are still many challenges concerning solid-state nanopore sensors. For instance, the noise in the nanopore measuring system could overwhelm the signal that it produces. The noise comes at all frequencies in our measurement bandwidth, and especially at high bandwidth measurement as it is required for sensing purposes, the capacitive noise dominates the noise performance. The other challenge is the

lack of measuring bandwidth. For example, a short DNA segment passing through the nanopore only stays in the pore with a dwell time less than 1μs , which means at least 1MHz bandwidth is required for our instrument to detect these molecules passing through. The dwell time is even shorter for proteins due to its short length, and the lack of higher bandwidth measurement hinders their detections. [67]

This dissertation focuses on exploiting the advantages of these solid state nanopores and making improvements to overcome the challenges we face for using these nanopore sensors.

Chapter 2

Experimental Overview

2.1 Nanopore Fabrication

The conventional nanopore device consists of a thin membrane supported by a silicon substrate. There are many ways one could create a hole through a thin membrane supported by silicon, but to realize a pore that is merely several nanometer in size, there are specific protocols and instruments required to achieve this goal with high precision.

2.1.1 Bright-field TEM

Transmission electron microscopy is a microscopy technique that enables a high energy electron beam to transmit through thin materials. When the electron beam is focused, we could drill the nanopore on a silicon nitride membrane as thick as 100nm. In bright field mode of JEOL 2010F TEM operating at 200kV, at 800k magnification and alpha

selector 1 condition, one could drill through a 100nm in 10 minutes, or just a blink second for membranes that are 10nm thick. Depending on the focus and alignment of the instrument is and the exposure time to the beam, pore diameters ranging from 1nm to 30nm are possible. (Fig. 2.1) The nanopores drilled by this technique have hour-glass shape structures. [51, 96, 100]

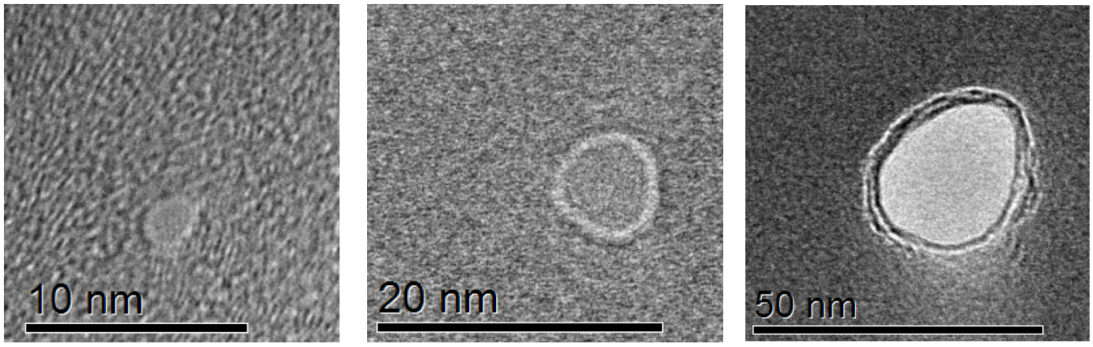

Figure 2.1: Different sizes of silicon nitride nanopores drilled under bright-field TEM mode

2.1.2 STEM thinning of silicon nitride

Thinning was accomplished by removing silicon and nitrogen from our sample by irradiating with an electron probe of the JEOL 2010F in STEM mode at 200kV. Electron-energy loss spectroscopy (EELS) allows for monitoring this ablation of silicon and nitrogen from the sample.[78] As electrons hit the sample, they are scattered by the atoms in a way that is governed by the energy levels of the atoms. The scattering corresponding to silicon atoms occurs at the energy level of around 100 eV, and the nitrogen atoms at around 400eV. The intensity of the number of electrons

scattered is proportional to the number of atoms in the sample, which is proportional to the thickness of the sample. Therefore, a ratio of the EELS scattering peak of silicon atoms before and after thinning gives the ratio of the thickness of the sample before and after thinning. The thickness of the sample is related only to the Si peak and nitrogen can be removed without changing the thickness. [78] The membrane thickness was monitored by observing the silicon scattering peak intensity (Si-peak) with EELS. This is done in two steps; firstly, at a high electron probe current while rastering over an area 100 nm (Fig. 2.2b, Region 2). The original thickness of the LPCVD grown low-stress silicon nitride was 50nm. This thickness was confirmed by ellipsometry. Thinning was continued until the Si-peak reached 20% of the original value. Therefore, this first step brings the membrane thickness to 10 nm (Fig. 2.2c). Usually at this stage the depletion of N peak is observed. Due to nitrogen's lower atomic number, it is sputtered out faster than the silicon resulting in only silicon atoms left. In the second thinning step the electron probe current was reduced and rastered over an area of 25 nm (Fig. 2.2b, Region 3), which allowed for finer control. The thinning continued until the Si peak reduced to 30-40% the intensity of the first thinning step, for a final thickness of 3-4 nm (Fig. 2.2d). The nanopore was made at this thickness by stopping the rastering of the electron probe and letting the Si-peak drop to zero background intensity.

Maintaining excellent focus on the membrane is key to even thinning. The whole process of thinning takes about half an hour to thin to 3nm. At 3nm thickness, pore formation takes less than 5 seconds. The nanopore diameter depends on how long the beam is kept steady on the sample and accurate focus. Typical nanopores open

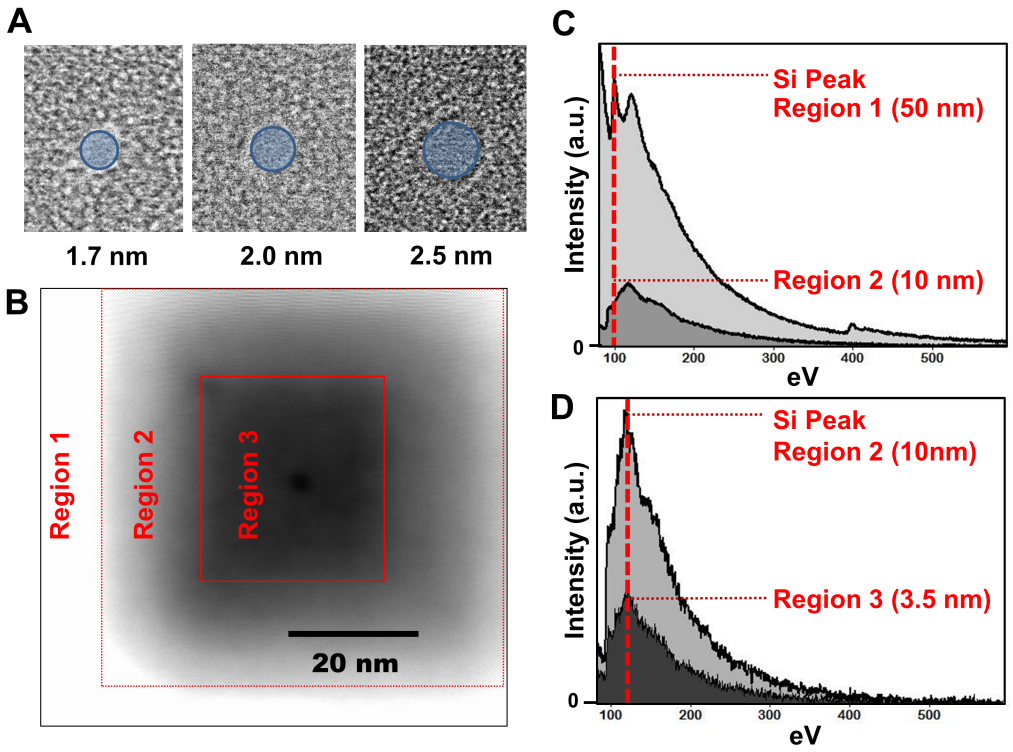

Figure 2.2: (a) Bright-field TEM image of nanopores made in STEM-thinned membranes. Circles indicating diameters of 1.7 nm, 2.0 nm, and 2.6 nm are shown in overlay with corresponding nanopores. (b) High-Angle Annular Dark Field image of STEM-thinned regions of silicon nitride. Regions are labeled according to the steps in the STEM-thinning process, with Region 1 unthinned, Region 2 thinned to 10 nm, and Region 3 thinned to 3.5nm. (c) Electron-energy loss spectra (EELS) taken of silicon nitride before (Region 1) and after (Region 2) initial thinning. Red markers indicate the Si peak, which drops to 20% of its original value; this corresponds to a thinning from 50 nm to 10 nm. (d) Electron Energy Loss Spectra (EELS) taken of silicon nitride before (Region 2) and after (Region 3) the second thinning process. Red markers indicate the Si peak, which drops to 35%, corresponding to a thinning from 10 nm to 3.5nm. All images were taken using a JEOL 2010F STEM instrument.

to a diameter between 1 and 2 nm with this technique shown in Fig. 2.2a. The pore drilled at STEM mode typically shows a cylindrical shape. [78]

2.1.3 Aberration corrected STEM

The aberration corrected TEM is an instrument that has the capability of resolving single atoms, and this will be suitable for precise control of nanopore drilling, especially for 2D membranes. By using the hexapole corrector to reduce the astigmatism and axial coma of the electron beam, the instrument could reach spacial resolution of 1 angstrom or better. For the purpose of drilling nanopore in single layer MoS_2 membrane, the instrument is operated at 80kV to prevent defects forming while scanning and focusing under STEM mode. A nanopore could be drilled in spot mode after precise focusing. It could open a nanopore by ablating away merely a single molybdenum atom.

2.2 Measurement of ionic current

After the nanopore is fabricated, we place the nanopore, usually supported by a silicon or glass substrate, between two electrolyte solution chambers. We apply a bias voltage across the nanopore, and an ionic current due to ion movements through the nanopore is measured by an amplifier. The most common electrolyte solution used in this application is potassium chloride (KCl), because of the similar mobility of potassium cation and chloride anion. [34] The standard electrode would be Ag/AgCl electrode for chemical redox reactions to happen at the solution/electrode interface

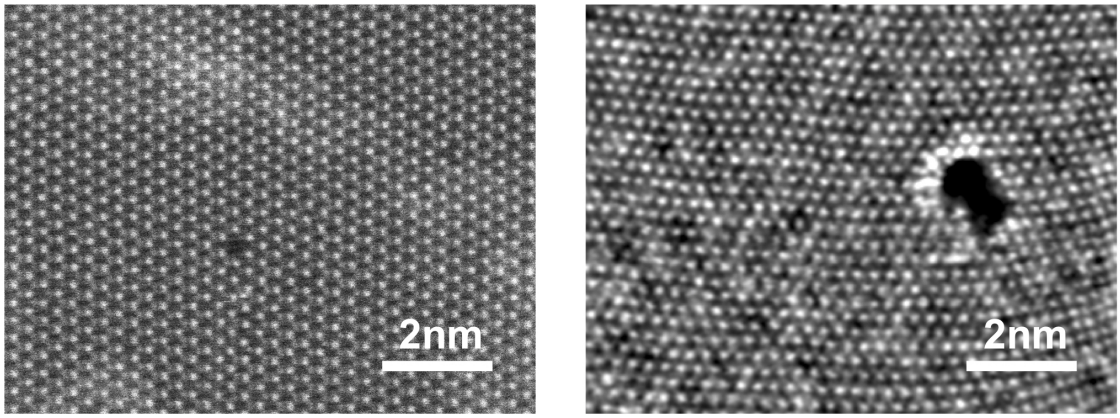

Figure 2.3: MoS_2 nanopores taken at 80kV in JEOL JEM-ARM200CF. The left image shows only a single molybdenum atom being displaced by the electron beam
.

to complete the full circuit. The Ag/AgCl electrode could be made by soaking the silver wire into bleach for a chloride layer to form.

A nanopore could be regarded as a resistor in solutions, with the resistance $R_{pore} = 4L/\sigma\pi d^2$ and the current flowing through the nanopore at a given bias voltage can be approximated by

$$I = V\sigma\Big(\frac{4L}{\pi d^2}\Big)^{-1}, \tag{2.1}$$

where V is the transmembrane bias voltage applied, σ is the conductivity of solution, L is the nanopore thickness, and d is the pore diameter. When the membrane is thin, the region that is immediately outside of the nanopore would start to have significant contribution to the overall resistance, acting as a resistor in series. The resistance of access region is $R_{acc} = 1/2\sigma d$. [38] This access resistance is present in both sides of

the pore. Hence, we could approximate the current flowing through the pore with the equation including the contribution of the access regions as

$$I = V\sigma\Big(\frac{4L}{\pi d^2} + \frac{1}{d}\Big)^{-1}. \tag{2.2}$$

2.2.1 DNA in nanopore

When DNA is present in the nanopore, part of the ionic current is blocked, and the blockage signal could be estimated by the equation

$$\Delta I = V\sigma\Big(\Big[\frac{4L}{\pi d^2} + \frac{1}{d}\Big]^{-1} - \Big[\frac{4L}{\pi d_{eff}^2} + \frac{1}{d_{eff}}\Big]^{-1}\Big), \tag{2.3}$$

Where d_{eff} is the effective pore diameter when DNA is in the nanopore, expressed as $d_{eff} = \sqrt{(d^2 - d_{DNA}^2)}$. The electrolyte solution for DNA translocation experiments are made with 1 mM EDTA solution for chelation of divalent ions and pH-buffered using 10 mM TrisHCl.

2.3 Noise and SNR in high bandwidth measurement

Noise is inevitably present in any electrical measurement. The noise comes at all frequencies in our measurement bandwidth. Low-frequency noise is primarily governed by flicker and thermal contributions whereas high-frequency noise is dominated by the voltage noise of the amplifier interacting with the capacitance at the amplifier's input as shown in Fig 2.4. [80, 87] I_{rms} is the root-mean-square input referred current noise. At high frequency, the noise is dominated by the f^2 part of the characteristics

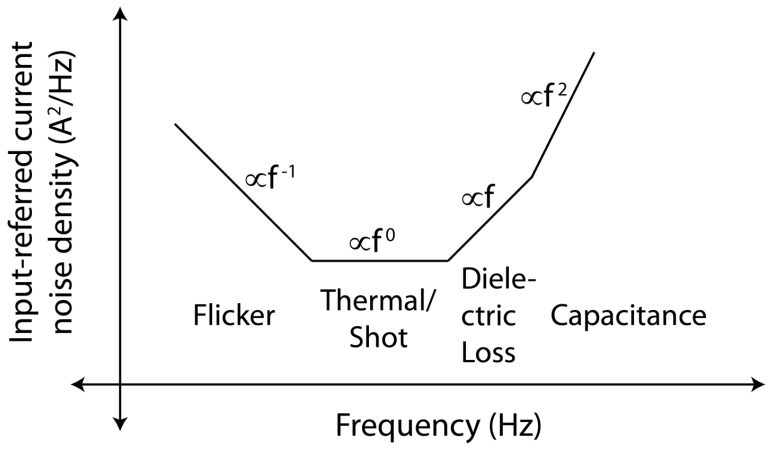

Figure 2.4: Illustration of typical input-referred current noise spectrum for a nanopore measurement. The axes are plotted in log-log scale.

shown in Fig 2.4. I_{rms} for high bandwidth measurement is then given by the equation

$$I_{rms}(B) = \frac{2\pi}{\sqrt{3}} B^{\frac{3}{2}} v_n C_{TOT}. \tag{2.4}$$

B is the bandwidth of measurement. C_{TOT} is the total capacitance of the measurement set-up, which is the sum of chip capacitance C_{chip}, capacitance of the wiring from the amplifier to the chip C_w, and the capacitance of the amplifier C_{amp}. And v_n is the input-referred voltage noise of the amplifier.

The other important concept for electrical measurements of this type is a sensor's signal to noise ratio (SNR). It is commonly defined as

$$SNR = \frac{\Delta I}{I_{rms}}, \tag{2.5}$$

I_{rms} here would be the noise in the baseline ($\sigma_{baseline}$). This ratio is the result of comparison of the desired signal to its background noise. As we seek to increase the performance of our measurement, an improvement in SNR by increasing ΔI or decreasing I_{rms} is necessary. In the following chapters, methods to improve SNR by increasing ΔI and decreasing I_{rms} as we continue to increase the measuring bandwidth will be presented.

Chapter 3

Low capacitance glass chip

In this chapter, we report the design and fabrication of chips consisting of suspended silicon nitride membranes spanning over small aperture on glass substrates. Two new chip designs are introduced: a simple chip design that routinely results in sub-2 pF capacitances, and also an improved two-step fabrication design resulting in sub-1 pF capacitance chips. The main design innovation is to replace the conventional silicon substrate which contributes to most of the device capacitance with an insulating glass substrate. The resulting total chip capacitance below 1pF leads to an improved noise performance in ionic current signals that we illustrate by low noise DNA translocation experiments, paving the way to more sensitive measurements for biomolecules detection and differentiation.

3.1 Introduction

Many personalized medicine, environmental, and mechanical applications require the use of membranes that could effectively and reliably separate two regions of empty space or fluids. Several thin membranes, sometimes as thin as one atom in the case of graphene, have proven impermeable to gas or fluid flow unless nanoholes are introduced into them [4]. In the presence of nanopores, molecular flow and analyte can be controllably driven through them, creating new opportunities for various applications. Progress in the field has been fast, in large part thanks to the development of new experimental techniques that enable unprecedented control at the nanoscale to grow and place membranes at desired positions relative to a substrate. [8, 65] The past few years have witnessed significant results in developing such thin yet robust membranes and using them in applications ranging from mechanics [4, 9] to nanoelectronics [29, 77, 105] and biomedicine [66, 102]. As mentioned in section 2.3, in many biomedically-relevant nanoelectronics applications, it is advantageous that the overall capacitance of the membrane chip is small in order to minimize the electrical noise produced when the voltage noise from the power source couples to total capacitance in the system. Frequently, the chip capacitance is the dominant capacitance and it governs the lowest current noise that can be achieved at a particular bandwidth. [1, 2, 80, 87] Specifically, this is important for the use of membranes for biomolecule detection, a class of applications attracting increasing interest and witnessing significant progress. However, the wide applicability of these results is limited by the noise in the ionic current signal when operating in high bnadwidth. One major approach to improve the noise, and consequently the signal-to-noise ratio, is to reduce the chip

capacitance. There have been several efforts to reduce the chip capacitance by bonding glass slides onto the silicon chip, [2] or transferring silicon nitride membranes onto glass substrates. [58, 73] Our thin silicon nitride membranes on glass chips reported here further reduce the chip capacitance to below what has been reported previously. [2] The fabrication process for silicon nitride membranes on glass reported here is transfer-free and suitable for large-scale production. We also demonstrate the use of this platform to suspend other 2D materials (graphene, MoS_2) on top of holes in silicon nitride membrane that are in turn suspended across the aperture. Besides, these chips are suitable to the harsh acid or plasma treatments often used to make chips hydrophilic or to clean the chips for reuse between experiments.

3.2 Glass Chips Fabrication

3.2.1 One-step etching design

Fig 3.1 demonstrates the fabrication process of the SiN_x membranes on glass chips. On both sides of the glass wafer of 200-500 μm, we employ an LPCVD technique to deposit a layer of 100-nm-thick SiN_x as the membrane material and 100-nm-thick amorphous silicon (a-Si) layer on top of SiN_x as a protection against the hydrogen fluoride (HF) etch later in the process. The glass used in this study is fused silica, which has a high softening point allowing the LPCVD process for depositing high quality SiN_x membranes. We spin-coat SPR-220 photoresist on both sides, and we pattern by photolithography squares of 10 μm in size at the center, and etch away the a-Si and SiN_x layers by CF_4 reactive ion etching. The glass substrate is etched

in a 49% HF solution until the hemisphere created by isotropic etching reaches the bottom SiN_x layer. The remaining photoresist and a-Si are stripped away by acetone and KOH respectively, resulting in the final glass chip with a silicon nitride membrane suspended at its center.

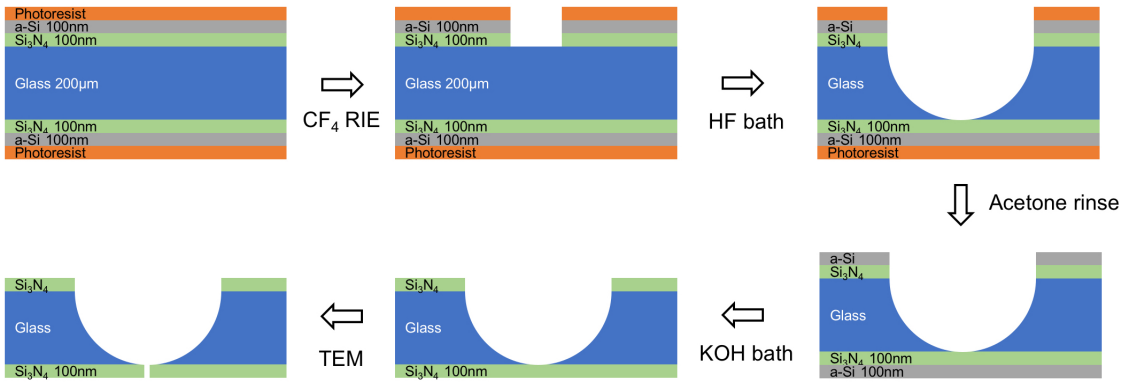

Figure 3.1: Glass chip fabrication by one-step etching design

3.2.2 Two-step etching design

In order to further lower the total chip capacitance, this fabrication process is refined to incorporate a two-step etching method illustrated in Fig. 3.2, obtaining a double etched hemisphere chip structure. In this two-step process we stop the HF etching when the etched hemisphere approaches the SiN_x layer at a distance of several micrometers. The main idea is to leave as much of the insulating material close to the center, while still being able to define a suspended membrane of desired size. We spin on the electron beam resist (anisole diluted ZEP520A) and perform electron beam lithography to create a patterned aperture smaller than 5 μm in radius at the

center. The whole chip is then etched again in the HF bath until the second etched hemisphere reaches the SiN_x layer and forms a suspended membrane.

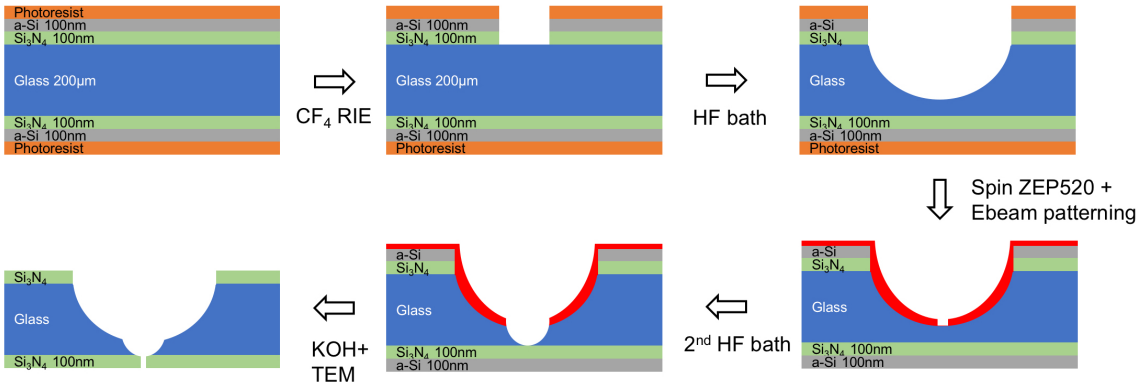

Figure 3.2: Glass chip fabrication by two-step etching design

Fig. 3.3a shows the wafer scale production of the glass chips on fused-silica wafer. Fig. 3.3b, c show optical images of the top and bottom view of the glass chip where the silicon nitride (SiN_x) membrane is suspended across a central aperture, several micrometers in size, where the glass is etched away. Fig. 3.3d, e shows another glass chip imaged by SEM. There are some charging up happening when imaging these glass chips in SEM due to charge build-up, yet this could be solved by slower scanning rate or applying discharging polymer. Being able to image these glass chips in SEM is important for the two-step etching method which will be described later.

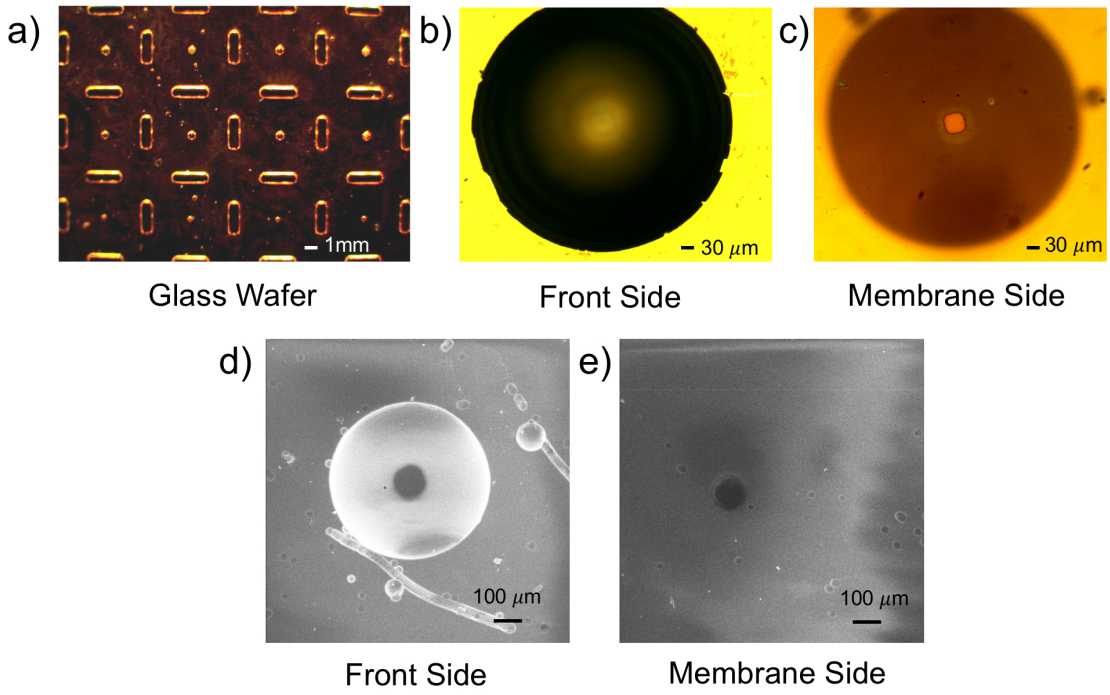

Figure 3.3: Image of glass chips. (a) Wafer-scale glass chips. The circle at the center of each chip is the etched hemisphere and the rectangular lines are to be broken apart to make individual glass chip. (b) Optical image of the front side of the glass chip showing the etched hemisphere. (c) Optical image of the membrane side of the glass chip showing the SiN_x membrane at the center of the circular shadow,which is the etched hemisphere. (d) SEM image of the front side with etched hemisphere showing. (e) SEM image of the SiN_x membrane.

3.3 Capacitance Estimation

To estimate the total capacitance of the resulting glass chip, we represent the glass chip as a set of individual capacitive elements and calculate each capacitance contribution to the total chip capacitance as shown in the color-coded regions in Fig. 3.4a. Each color-coded area represents parallel capacitors and could be summarized

by a circuit diagram as shown in Fig. 3.4b. The purple area is the freestanding SiN_x membrane with capacitance C_{mem}. The red area is the area where the glass substrate was etched away isotropically, creating a hemispherical structure. The capacitance in this area is estimated by integrating infinitesimal parallel plates over the whole hemisphere area and is given by

$$C_1 = 2\pi\epsilon R_1\Big[\ln(1+\frac{R_1}{t})\Big], \tag{3.1}$$

where R_1 is the thickness of the glass chip and also the radius of the hemisphere; t is the thickness of the SiN_x layer, and ϵ is the permittivity of glass. The green area is the remaining area of the chip covered by a layer of silicone elastomer (Kwik-cast, World Precision Instruments) as a seal to separate the two chambers of electrolyte solutions, and its capacitance is noted as C_{rest}. The estimated total chip capacitance is summed up to be $C_{mem} + C_1 + C_{rest}$.

Fig. 3.4c summarizes the results of the estimated total chip capacitance with glass thickness of 200 μm to 500 μm. Here it is assumed with feasible parameters of a membrane radius of 10 μm, with 0.5 mm Kwik-cast applied around the etched hemisphere, and an electrolyte solution droplet covering an area about 7 mm^2 (1.5 mm radius of circular area coverage) serving as electrolyte chamber. Glass chips designed by this method can reach capacitance below 1 pF for glass thickness below 300μm. The relatively large contribution to the overall capacitance comes from the red area in Fig. 3.4d where the dielectric layer is the thinnest.

The estimation for chip capacitance for glass chip etched by two-step process is similar. The total chip capacitance of this chip structure can be calculated by dividing

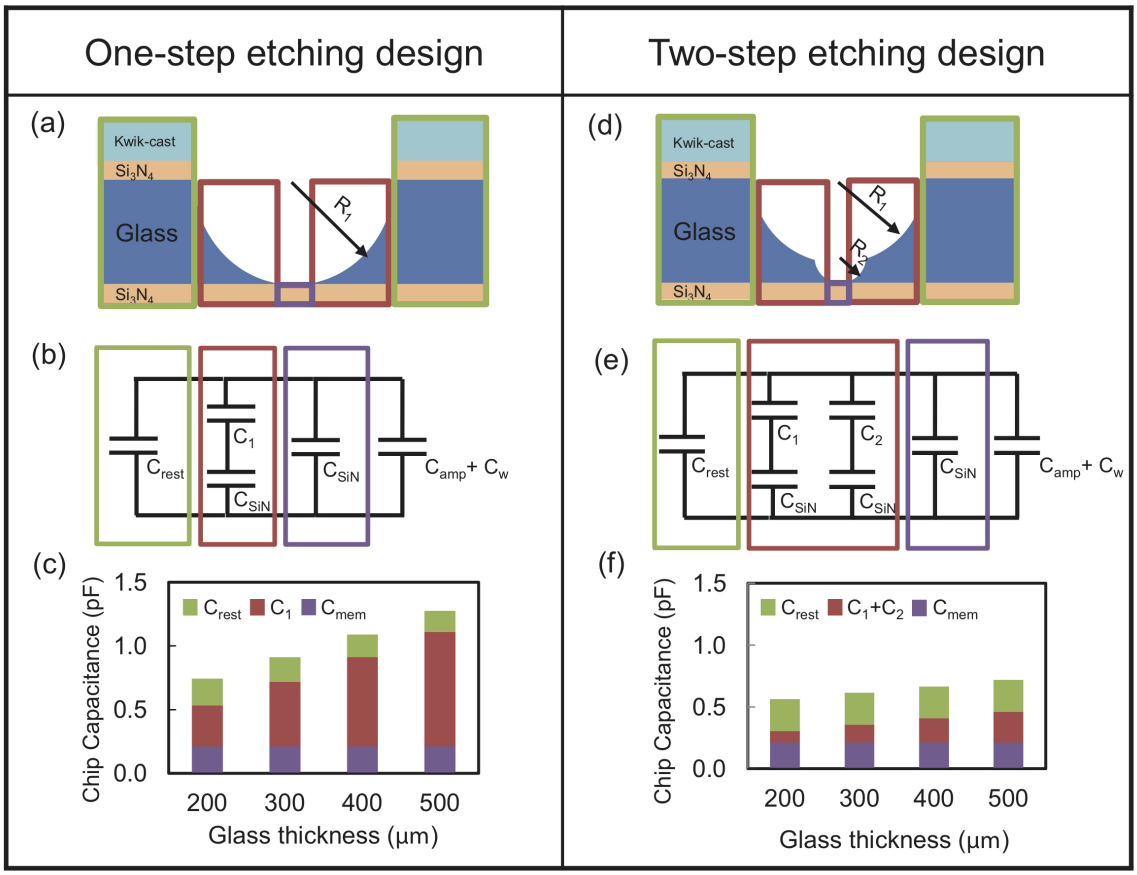

Figure 3.4: (a) Schematic of the glass chip with silicon nitride membrane in the center, with silicone elastomer (Kiwk-cast) applied on top as insulation. The different areas contributing to the chip capacitance are color-coded. C_{mem} is the capacitance of the membrane, C_1 is the capacitance of the spherical area, and C_{rest} is the capacitance of the rest of the chip. (b) The corresponding circuit diagram, where C_{mem}, C_1, C_{rest} are capacitances of the purple, red, and green area respectively. (c) Bar graph of chip capacitance for glass thickness of 200, 300, 400, and 500 μm, showing relative contributions from regions C_{rest}, C_1 and C_{mem}. The inset is the minimum capacitance as a function of glass thickness. The units are the same as the main figure. (d) Schematic of the glass chip device produced by a two-step etching; the first etched hemisphere has a radius R_1, and the second etched hemisphere has a radius R_2. The different areas contributing to the chip capacitance are color-coded. C_{mem} is the capacitance of the membrane, C_1 is the capacitance of the spherical area with radius R_1, C_2 is the capacitance of the spherical area with radius R_2, and C_{rest} is the capacitance of the rest of the chip. (e) The corresponding capacitor circuit diagram, where C_{mem}, C_1 + C_2, C_{rest} are capacitances of the purple, red, and green areas, respectively. (f) Bar graph of the chip capacitance for glass thickness of 200, 300, 400, and 500 μm, respectively, showing relative contributions from regions C_{rest}, C_1 + C_2 and C_{mem}. The inset is the minimum capacitance as a function of glass thickness. The units are the same as the main figure.

it into capacitors represented by different color-coded regions. The main difference between the two designs is that in this two-step etching process, there are now two etched hemispheres stacked on top of each other. The capacitance contribution of the red area is now given by

$$C_1 + C_2 = 2\pi\epsilon R_1\Big[\ln(1+\frac{R_1}{t+R_2})\Big] + 2\pi\epsilon R_2\Big[\ln(1+\frac{R_2}{t})\Big], \tag{3.2}$$

where R_1 is the radius of the upper hemisphere, and R_2 is the radius of the lower hemisphere. The sum of the radii of the two hemispheres is equal to the total thickness of the chip. The capacitor circuit diagram of this chip design is shown in Fig. 3.4e. With this chip design, the theoretical minimum of the total chip capacitance for glass in the 200-500 μm thickness range could be reduced by approximately 0.5 pF compared to that of chips produced by one-step etching. In this case, the contribution from the red area where the glass is etched away in a spherical shape is greatly reduced (Fig. 3.4f and Fig. 3.5). This reduction in capacitance is due to a thicker insulating glass layer remaining in the chip. It is useful to estimate the capacitance minimum as a function of the device thickness as shown in the inset of Fig. 3.4c, f. In both designs, the capacitance asymptotically approaches a minimum value of 0.5 pF given by the large Kwik-cast covered area when the glass thickness and hemisphere radius approaches zero. However, the capacitance of the two-step etching design is much less sensitive to the membrane thickness, allowing us to use more robust 300 μm glass chips in experiments. Glass wafers thinner than 200 μm are prone to shatter and crack during fabrications.

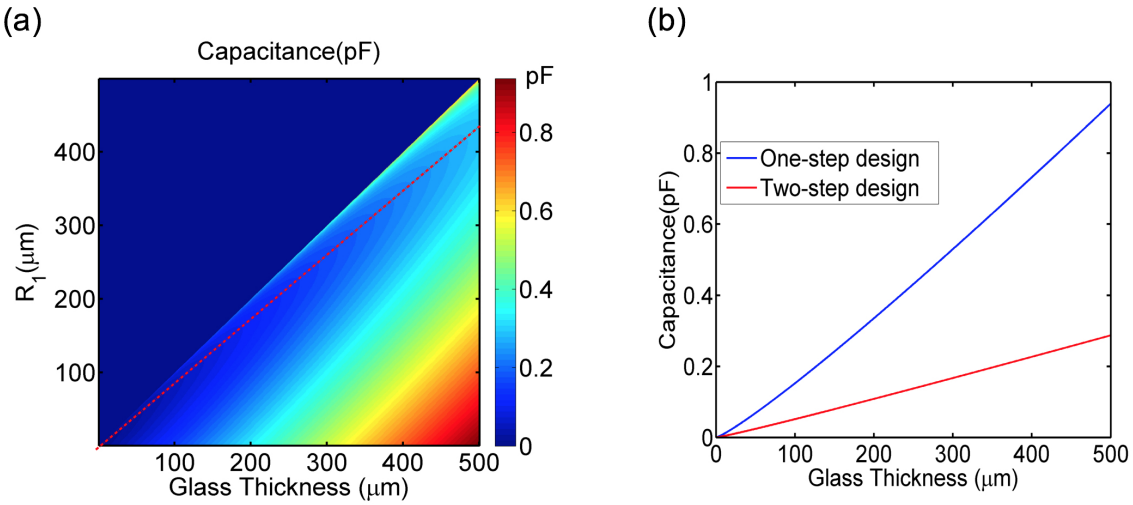

Figure 3.5: (a) Capacitance of the spherical part of the two-step design as a function of the glass slide thickness and radius of the bigger hemisphere (R_1). The red dotted line indicates the R_1 at which the minimum of the capacitance is found. (b) Comparison of the minimal capacitance as a function of the device thickness for the spherical part (red area in Fig. 3.4a and d) of the two designs.

3.4 Glass chips as 2D Material Carrier

Realizing nanopores in ultrathin membranes is of particular importance for two reasons: to maximize the ionic current signal level (by minimizing the nanopore thickness and therefore its resistance), and to maximize the spatial sensitivity (in order to sample a small part of the molecule, such as a single DNA base). These glass chips can be used as a more general platform to suspend 2D materials such as grapheme (0.3nm thick) and metal dichalcogenides (MoS_2, WS_2, 0.6nm thick) monolayer membranes. 2D materials due to its atomic-level thickness have been shown to be promising biomolecule sensors [22, 26, 32, 64, 83]. The low capacitance SiN_x-on-glass platform will enhance the sensing capabilities of such 2D materials by reducing noise.

Fig. 3.6a is a schematic illustrating a 2D membrane suspended over a 300-nm-size aperture formed in the SiN_x membrane over the glass chip. One example is the scanning electron microscope (SEM) image of a graphene sheet suspended in this fashion Fig. 3.6. The 300-nm-size aperture in the SiN_x membrane was first fabricated by electron beam lithography and plasma etching. CVD grown graphene characterized by Raman spectroscopy was then, using bubble transfer technique, [17, 31] transferred onto the membrane over the aperture. The device is placed between two chambers of electrolyte solutions, and bias voltage is applied to verify the current flowing through is nearly zero, suggesting complete graphene coverage over the aperture. Other 2D materials, such as metal dichalcogenides monolayer membranes could be transferred onto this SiN_x-on-glass platform as typically transferred onto Si substrate as demonstrated in Fig. 3.7. [36, 65] These 2D materials could subsequently be drilled in ACTEM as described in chapter 2.1.3.

3.5 Experimental Results and DNA translocations

Measured chip capacitance, C_{chip}, for 13 devices are summarized in Fig. 3.8a as solid circles, and the dashed blue line is the estimated minimum attainable capacitance. The chips are made with fused silica of thickness 300 μm and SiN_x membrane thickness 100 nm, fabricated by the two-step etching method described previously. Chip capacitance was measured by applying triangular-wave voltage pulses with the Chimera amplifier and measuring current vs. time in a fluidic cell as shown in the inset of Fig 3.8a. For membranes with radii smaller than 10 μm, experimentally mea-

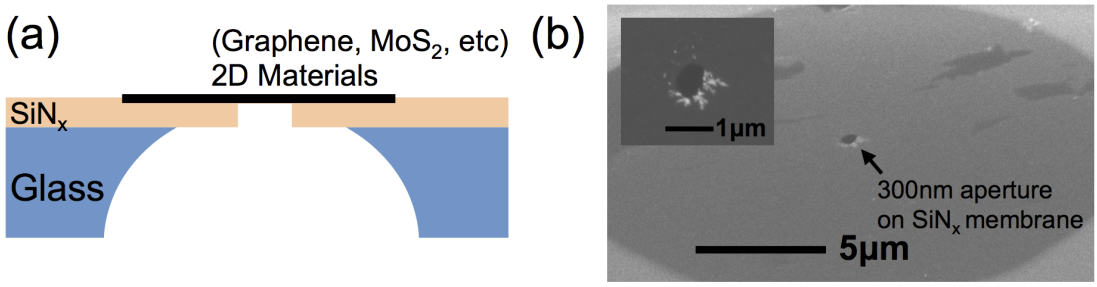

Figure 3.6: (a) 2D materials, such as graphene or MoS_2, on the SiN_x-on-glass chip serving as a sub- 1pF capacitance platform. (b) SEM image of a graphene sheet covering the 300-nm-large aperture in the suspended SiN_x membrane. The darker grey area is the circular SiN_x membrane, and graphene is covering most of the area of the SiN_x membrane, including the aperture at the center. The inset is the enlarged image of the aperture with graphene suspended on top. The white flakes around the suspended graphene area(circular dark area in the center) are residual PMMA after transfer.

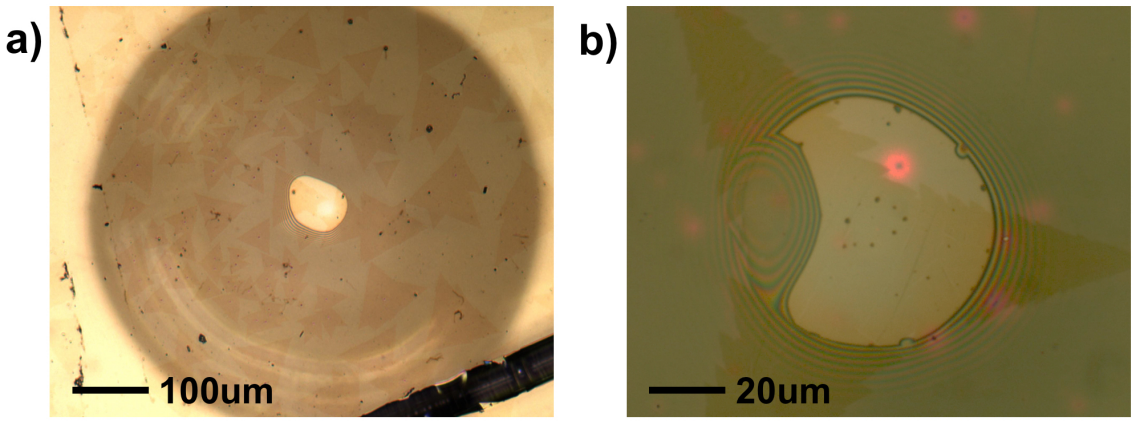

Figure 3.7: (a) High density CVD grown MoS_2 films are transferred onto glass chips. The monolayer MoS_2 are triangular in shapes and could be seen under optical microscope. (b) A higher magnification of an optical image showing MoS_2 membrane on top of the SiN_x membrane where a FIB drilled aperture is at its center.

sured C_{chip} values fall below the sub-1 pF regime, and C_{chip} scales with the membrane radius in accordance with our estimation. The experimental values are slightly larger than the theoretical estimate because of the actual radius of the second hemisphere is smaller than the radius R_2 (mentioned in Fig. 3.4d), which was used to estimate the minimum capacitance based on a two-hemisphere representation in Fig. 3.4f. This is largely caused by ZEP520 electron beam resist not being able to withstand long HF etch and flaking off before the desired etch time. Other possible factors include errors in estimates of the thickness of the silicon elastomer Kwik-cast and its distance to the membrane, and the size of the liquid droplet. When the capacitance of chips is on the same order of the internal amplifier capacitance (20 pF), we observe the contribution of the chip capacitance to the current noise (here shown for a 12 pF device in Fig. 3.8b). As the capacitance of these glass chips is much lower than the amplifier internal capacitance, the resulting ionic current noise we observed for these chips shown in Fig. 3.8b is undistinguishable from the open-headstage noise (approx. 110 pA_{rms}). In other words, in this case the noise is dominated by the amplifier. [2]

The silicon nitride membrane chips demonstrated here are interesting for applications requiring low capacitances, including the realization of nanopores for biomolecule analysis and DNA sequencing. We use these devices to demonstrate very low noise translocations of 3 kbp double-stranded (ds) DNA. Nanopore here is drilled in JEOL 2010F bright field TEM mode as described in section 2.1.1. The measurement cell has two chambers of 1 M KCl, 1 mM EDTA solution buffered using 10 mM TrisHCl. Experiments were conducted using a VC100 voltage-lamp amplifier (Chimera Instruments, New York, NY), to apply the bias voltage using Ag/AgCl electrodes and

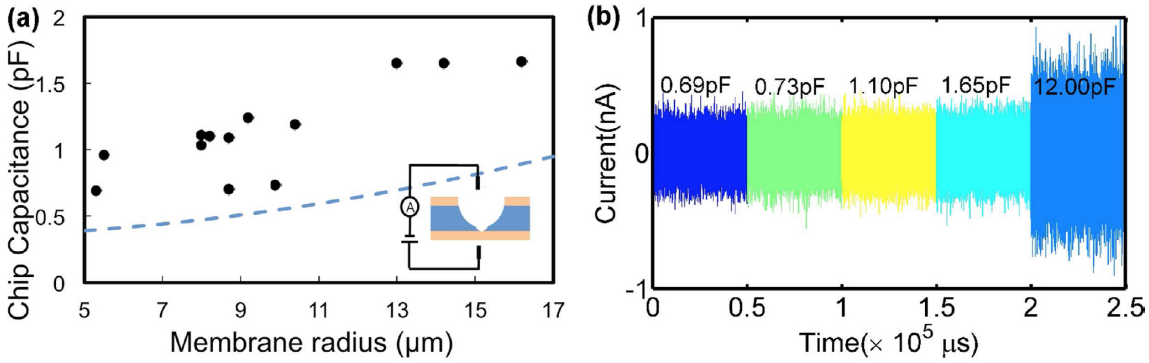

Figure 3.8: (a)Measured capacitance, C_{chip}, of the glass chips produced by two-step etching (Fig. 3.4 d) as a function of SiN_x membrane radius (μm). The blue dashed line is C_{chip} estimated from the model in Fig. 3.4f. The glass chip thickness is 300 μm and the SiN_x membrane thickness is 100 nm. The experimental errors are within the area of the solid circles. (b) Measured ion current temporal traces for several glass chips with capacitances C_{chip} = 0.69, 0.73, 1.1 pF, and 1.65 pF showing an amplifier-limited noise performance. A current trace from a 12 pF is shown for comparison.

measure the ion current through the nanopore. The amplifier applies a fourth order Bessel low-pass filter at 1 MHz. For translocation experiments bias voltages of 200 mV to 1V are applied across the nanopore. A TEM image of a nanopore drilled by focused electron beam on 100nm thick SiN_x membrane is shown in the inset of Fig. 3.9a. Fig. 3.9a shows an ionic current vs. time trace of translocation events measured at 1 MHz (blue trace) and filtered at 100 kHz (red trace) for 1V bias voltage, and Fig. 3.9b shows details of events with lengths from 0.5 ms to 10 ms. The total noise compares favorably to previous measurements at the same frequency [2, 80, 96] despite the higher applied voltage.

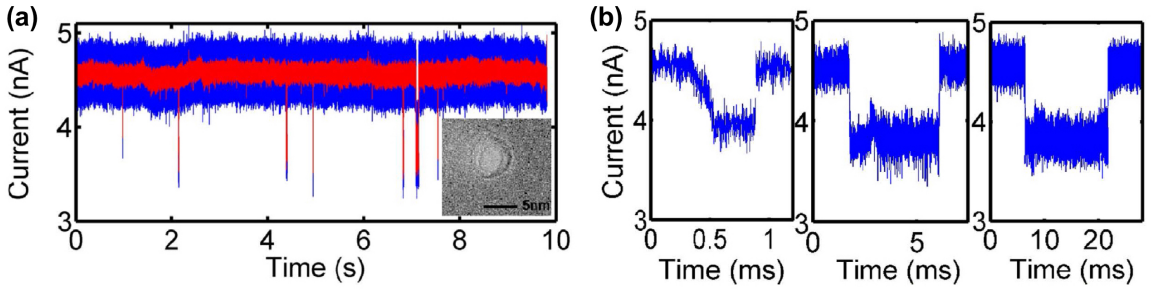

Figure 3.9: (a) Current vs. time trace of 3kbp (kilo base pairs) dsDNA segments translocating through one of the devices. The red trace is filtered at 100kHz, and the blue trace is filtered at 1MHz. The inset is a TEM image of a nanopore drilled with focused electron beam in the TEM. (b) Details of DNA translocation events with lengths from 0.5 ms to 10 ms

3.6 Summary

In summary, we designed an integrated process of producing membranes on glass chips with sub-1 pF capacitance and we demonstrated their use in DNA translocation experiments. Other biomolecule sensing applications utilizing nanopores also require to be performed at high bandwidth with enhanced signal to noise ratio to differentiate finer features of the biomolecules. The glass chip has shown significant improvement on reducing the chip capacitance by substituting glass for silicon as a substrate. One-step fabrication process could produce sub-2 pF capacitance and further sub-1 pF capacitance was realized by an improved two-step design, resulting in a low-noise device for biomolecules detection demonstrated by DNA translocation experiments. The lower noise level and the ease of production and cleaning make these glass chips superior substitutes for conventional silicon chips. Furthermore, this versatile platform could be used to suspend 2D materials and take advantage of its

robustness and atomic thickness membranes to achieve higher SNR levels in various nanoelectronics and biomolecule detection applications.

Chapter 4

High bandwidth measurements

In this chapter, the fastest ion current measurements through nanopores to-date with temporal resolutions approaching 100 ns is reported. This high measurement bandwidth is achieved through the use of low capacitance glass chip, as discussed in chapter 3, along with ultra-thin solid-state nanopores that offer signal levels as large as 30 nA measured using a custom-made CMOS-integrated nanopore (CNP) amplifier. Recording at such high bandwidths enables us to detect transient features within translocation events that are related to the translocation dynamics of ssDNA that are otherwise undetectable at lower bandwidths. The CNP amplifier is designed and manufactured by our collaborators gdho in Columbia University.

4.1 Introduction

One of the advantages of electronic approaches to single-molecule detection over fluorescence-based approaches generally is the higher signal levels. The current mea-

sured in solid-state nanopores can be as large as 30 nA. In contrast, typical organic fluorophores under laser pump powers on the order of 50 mW [37] deliver photon fluxes on the order of 3000 photons/s, [40] which amounts to a current of only 0.2 fA in an imager with a quantum efficiency of 40%. These signal levels limit single-molecule fluorescence experiments to temporal resolutions that are typically on the scale of 50 ms. [47] In contrast, the approximately 10^6 times higher signal levels from nanopores should translate into temporal resolutions on the scale of 100 ns (or better) at the same noise levels. Despite this potential, achieved temporal resolutions have been at best 1 μs, [80] using integrated complementary metal-oxide-semiconductor (CMOS) amplifiers, and more typically 10-100 ţs with discrete voltage-clamp amplifiers, such as the Axopatch 200B. [3, 53, 57, 101] The inherently transient nature of DNA translocation through nanopores, which can occur at rates higher than 10 bps/μs, reinforces the need for improved temporal resolution in these measurements. [30] For pores less than 5 nm in diameter, pore-molecule interaction could serves to reduce the average translocation rate to approximately 1-2 bases/μs for ssDNA[96] , but these rates are still very fast relative to achieved temporal resolution in measurement systems to-date. For proteins translocating through nanopores with diameters greater than 10 nm, over 90% of all events go undetected because of inadequate temporal resolution in the detection electronics. [74]

Because of the poor temporal resolution of typical nanopore instrumentation, a range of "slowing-down" approaches have focused specifically on reducing the translocation speed: by ratcheting the molecules using an enzyme,[11, 57] by lowering temperature [96] or using temperature gradients [101], by using higher viscosity solu-

tion and viscosity gradient, [26, 30, 75] and by changing to various salt solutions. [18, 53] While these techniques manage to reduce the average translocation rate, this is achieved at the expense of either increased sample preparation or reduced signal levels. In addition, for techniques that slow down translocation using enzyme dynamics, there are Poisson statistics at work in the ratcheting dynamics. [11, 57] High instrumentation bandwidth also improves error rates, because of one's ability to observe all events, including the rare ones that may be significantly faster than the mean.

4.2 SNR-limited bandwidth

It is noise that limits temporal resolution in nanopore measurements. Low-frequency noise is primarily governed by flicker and thermal contributions whereas high-frequency noise is dominated by the voltage noise of the amplifier interacting with the capacitance at the amplifier's input as discussed in chapter 2.3. Advances in nanopore treatment wetting protocols such as hot pirahana treatment have minimized flicker noise from the pores. [45, 92] As such, integrated noise in high bandwidth nanopore measurements are dominated by the contributions of the amplifier. [2] Several efforts have focused on improving these amplifiers either through adjustments to off-the-shelf amplifiers, such as the Axopatch 200B, [69, 85, 89] or more recently, through custom-designed amplifiers. [28, 49, 50, 80] Most custom amplifiers have exploited CMOS technology and have the additional advantage of allowing arrays of amplifiers to be supported on the same chip. These approaches have been able to extend measurement

bandwidths, as limited by signal-to-noise ratios (SNRs), up to 1 MHz, [80] offering microsecond temporal resolution.

Several important parameters determine the SNR in nanopore measurements. For a given blockade current ΔI, with a root-mean-squared (RMS) noise level of I_{rms}, the signal-to-noise ratio is defined as SNR = $\Delta I/I_{rms}$. At high frequency, the noise is dominated by the f_2 part of the characteristics as shown in chapter 2.3. As such, to maintain a certain level of SNR, the SNR-constrained bandwidth (B_{MAX}) obeys the equation

$$B_{MAX} = (\frac{\Delta I}{v_n \Sigma C_i})^{2/3} \tag{4.1}$$

, where v_n is the voltage thermal noise floor of the amplifier and Σ C_i is the net capacitance at the input of the amplifier, composed of contributions from the pore (C_{pore}) (Fig. 4.1), and the measurement electronics (C_{amp}) (Fig. 4.2a). [79] To further increase B_{MAX}, ΔI must be increased, while simultaneously lowering v_n and ΣC_i. ΔI can be increased by increasing the conductivity of the salt solution or by reducing the nanopore thickness as in Eq. 2.3. [100] While some commercial amplifiers can offer lower v_n than their integrated CMOS counterparts, this comes at the expense of higher ΣC_i. [2, 56, 86] Although some new discrete amplifiers have managed to reduce C_{amp} to as little as 20 pF, this value can still dominate ΣC_i in optimized nanopore structures, in which C_{pore} can be less than 5 pF. [2] Achieving the full temporal benefit afforded by a given I involves careful reduction of v_n, C_{amp} and C_{pore}.

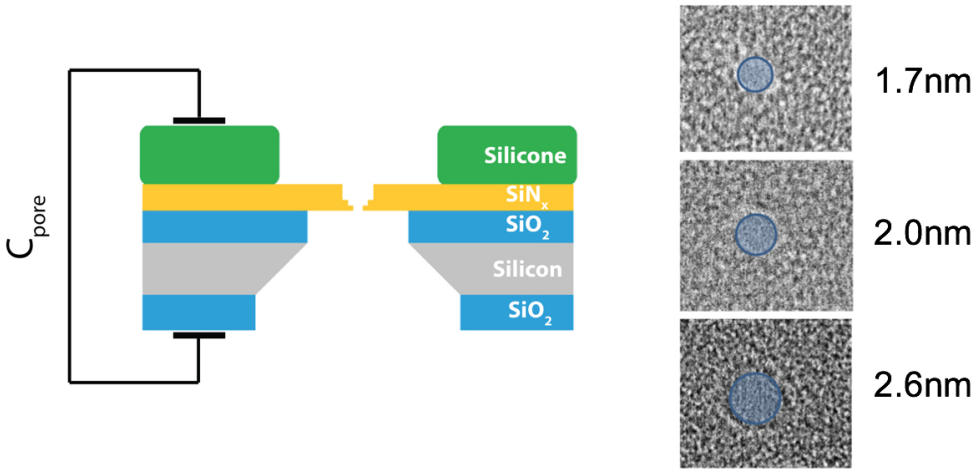

Figure 4.1: Left image is the chematic of the cross-section of the nanopore chip including silicon as the supporting substrate and the silicone passivation on the top. Right image is the bright-field TEM image of nanopores made in STEM-thinned membranes. Circles indicating diameters of 1.7 nm, 2.0 nm, and 2.6 nm are shown in overlay with corresponding nanopores

4.3 CNP2 amplifier details

Reduction of v_n and C_{amp} is achieved in the CNP amplifier with a custom-designed integrated circuit (IC) designed in a 0.18-μm CMOS technology. The IC contains 25 independent low-noise, high-bandwidth transimpedance amplifiers, each occupying 0.16 mm^2 in a 5 mm $\times$ 5 mm chip. Fig. 4.2b shows a die micrograph of the IC. The design of the amplifier follows from an earlier design [80] but has been further optimized for lower v_n. In this dissertation, we name our new design CNP2, as we refer an earlier design reported by Rosenstein et al. as CNP1. The feedback networks (shown as the parallel combination of R_F and C_F in Fig. 4.2a) in these amplifiers often differ in their implementation from their discrete counterparts. Since realizing large

valued resistors is difficult in CMOS processes and would add too much capacitance at the input, the feedback resistance R_F, is realized using an active current-divider circuit. [28] R_F is tunable and is set to either 7.5 MΩ (low gain) or 45 MΩ (high gain). These relatively low R_F values will reduce the SNR slightly at frequencies below 100 kHz, where the integrated noise is dominated by the white noise of R_F as mentioned in chapter 2.3, where noise current power spectral density, $S_n(f) = \frac{4kT}{R}A^2Hz^{-1}$. [79] This will not be a concern at MHz bandwidths where the integrated noise is dominated by the interaction of the amplifier thermal noise with the input capacitance [79, 90]. The lower R_F values yield a larger dynamic range with the amplifier being capable of tolerating baseline currents as large as $V_{DD}/2R_F$= 120 nA (20 nA) in the low (high) gain setting, where V_{DD}= 1.8 V is the supply voltage for the IC.

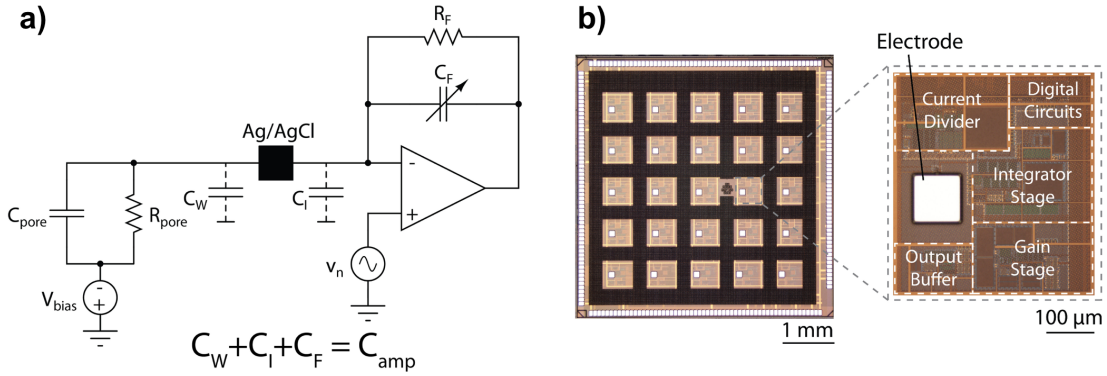

Figure 4.2: . (a) Simplified electrical schematic illustrating the various capacitances and noise sources that determine high-frequency noise behavior. Input current signals are converted to a voltage with a gain set by R_F. The net capacitance that determines the noise is C_{amp}+C_{pore}. (b) Die micrograph of the 5 × 5 mm amplifier chip with a zoomed-in micrograph of a single channel. The chip has 25 amplifiers, each of which implement the schematic illustrated in (a) and which can be operated independently of each other. Each channel has an Ag electrode that is converted to an Ag/AgCl electrode through postprocessing.

The feedback capacitance, required to ensure amplifier stability, is programmable and set to C_F= 0.9 pF (0.15 pF) in the low (high) gain setting. The combination of C_F and R_F limits the 3-dB bandwidth of the amplifier to approximately $1/(2\pi R_F(C_F/8))$, which is set to = 200 kHz for both gain settings. The output of the amplifier is then subjected to additional off-chip filtering to restore flat response up to 10 MHz. C_F directly contributes to C_{amp}. However, C_F also introduces an additional pole in the amplifier's response at a frequency proportional to $C_F/(\Sigma C_i)$ which we can effectively push beyond 10 MHz for $C_F/(\Sigma C_i)> 0.1$ for this amplifier design.

The CNP design allows the tight integration of the nanopore and the measurement electronics. Rather than having wires connecting nanopore electrodes to the input of the headstage, as is the case in most commercial systems, the nanopore is mounted directly on the amplifier chip. Connectivity between the amplifier input and the trans-chamber is achieved by realizing an Ag/AgCl electrode on the surface of the chip (Fig. 4.2b) through post-processing of the integrated circuit after fabrication in a CMOS foundry. This electrode contributes a series resistance of approximately 200 Ω, but the associated interconnection capacitance (C_W) is less than 2 pF. The input transistors of the amplifier present a capacitance C_I = 1 pF. Thus, the net input capacitance presented by the amplifier becomes C_{amp}=C_W+C_I+C_F=4 pF, significantly lower than the = 20 pF seen in most discrete systems.

The amplifier is designed to have a thermal voltage noise floor of $v_{(n,amp)}$=2.6 nV/$\sqrt{Hz}$. The resistance of the on-chip Ag/AgCl electrodes generates an additional thermal voltage noise $v_{(n,R_S)}$=$\sqrt{(4kTR_S)}$= 1.8 nV/Hz, which is uncorrelated with the amplifier's thermal noise. The net thermal noise floor of the setup in ionic measure-

ments is thus $v_n = \sqrt{(v^2_{(n,amp)} + v^2_{(n,R_S)})} = 3.15\ \mathrm{nV}/Hz$. Fig. 4.3 a shows the simulated and measured power spectral density (PSD) of the input-referred current noise in open headstage configuration. We note that the flicker noise at low frequencies, which contributes negligibly to the integrated noise at bandwidths greater than 1 MHz, is dominated by that contributed by off-chip amplifiers used to extend the bandwidth. The CNP amplifier has an integrated input-referred open-headstage noise level of 8.1 pA_{rms} at 200 kHz, 47.8 pA_{rms} at 1 MHz, 481 pA_{rms} at 5 MHz and 1.62 nA_{rms} at the full 10 MHz measurement bandwidth (Fig. 4.3b).

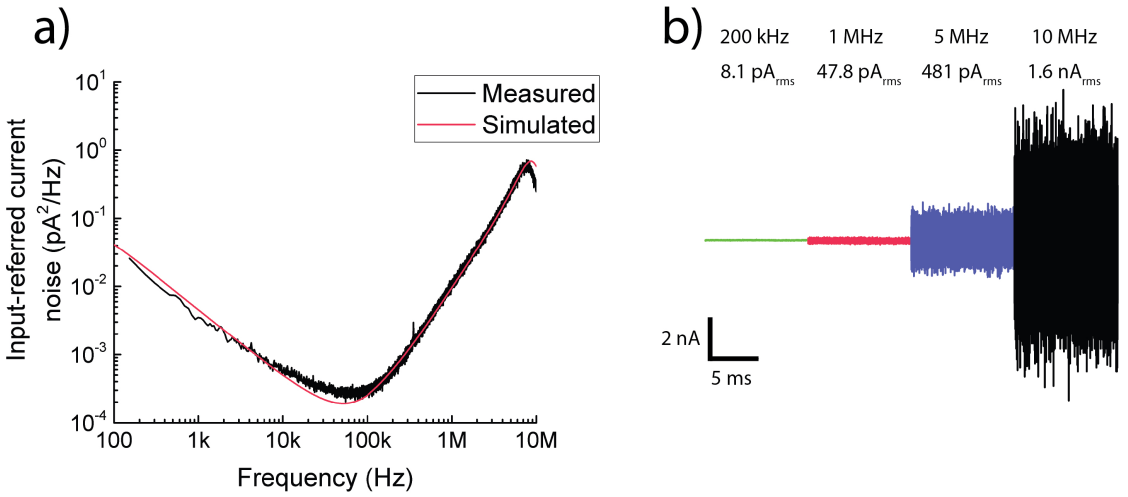

Figure 4.3: . (a) Input-referred current noise PSD for the open-headstage configuration of the CNP amplifier. Measurement results agree with the predictions of transistor-level simulations of the amplifier. (b) Concatenated time trace of a 10 ms long open-headstage measurement. Each section corresponds to the same trace filtered using a digital four-pole Bessel filter to cutoff frequencies of 200 kHz, 1 MHz and 5 MHz respectively. The 10 MHz trace already includes the effect of an analog four-pole Bessel filter and is not filtered further. I_{rms} values are indicated.

4.4 Measurements of Fast DNA translocation dynamics

Silicon nitride nanopores here were thinned to an absolute thickness of less than 4 nm, allowing for blockade current signals I, as high as 30 nA in 3M KCl at 900 mV bias. The ΔI of a nanopore sensor and can be estimated by Eq. 2.3. From the equation we could understand that ΔI is maximized when the pore thickness is small, and the pore diameter is as small as the cross-sectional width of the ssDNA.

Nanometer thicknesses are achieved using a scanning transmission electron microscope (STEM) based ablation technique that enabled precise thinning to near the theoretical limit (1 nm). [78] STEM thinning uses electron irradiation with rastering of the electron probe of a JEOL 2010F S/TEM over a defined area of silicon nitride as described in chapter 2.1.2. This causes the sputtering of silicon and nitrogen atoms [20] with the final membrane consisting of amorphous silicon, due to the higher rate of sputtering of nitrogen. [78] A two-step process is used, with an initial thinning of a 65 $\times$ 65 nm region of 50-nm thick freestanding silicon nitride membrane to 10 nm amorphous silicon by using a 2.5 nm probe size, with membrane thickness controlled by quantifying the mass loss using electron-energy loss spectroscopy (EELS). A second thinning in a smaller 25 $\times$ 25 nm region is made using a 0.5-nm spot size, bringing the membrane thickness down from 10 nm to less than 4 nm.

We tested several nanopores with different diameters (all less than 2.6 nm) (Fig. 4.1) and recorded translocation characteristics using them. C_{pore} is a major factor that determines the SNR-limited bandwidth in nanopore recordings. Previous efforts

have suggested different techniques to minimize this capacitance. [1, 2, 46] For our experiments, the membrane capacitance is reduced by using window sizes smaller than 25 $\times$ 25 μm for the membrane openings while augmenting a passivating oxide layer outside this window with a 5 μm with an additional layer of silicone. C_{pore} varies between pores, with some chips giving C_{pore} as low as 6 pF. Fig. 4.4a shows the power spectral density (PSD) of the output noise spectrum for Pore 1 (C_{pore}= 10 pF, d= 1.3 nm, h_{eff}= 1.4 nm) and Pore 2 (C_{pore}= 13 pF, d= 1.7 nm, h_{eff}= 1.2 nm) that were among the ones used for the experimental results presented here. We also perform some translocation experiments with a third pore, Pore 3 (C_{pore}= 15 pF, d= 1.9 nm, h_{eff}= 3.3 nm). As a representative example, the integrated input-referred noise for Pore 1 at 200 kHz is 23.2 pA_{rms}, at 1 MHz is 125.7 pA_{rms}, at 5 MHz is 1.43 nA_{rms}, and at 10 MHz is 4.19 nA_{rms} (Fig. 4.4b). The capacitance is estimated by fitting the high bandwidth component (100kHz above) of the PSD to equation [79]

$$S_n(f) = (2\pi f C_{TOT} v_n)^2 A^2 Hz^{-1}, \tag{4.2}$$

C_{TOT} is the total capacitance of the system. When the contribution of C_{amp} is subtracted, we could obtain an approximation of the the pore capacitance, C_{pore}.

We performed measurements with ssDNA samples that were either 40 or 100 nucleotides (nt) long and prepared in aliquots of 200 nM in 3 M KCl. Since ΔI plays a significant role in improving the measurement bandwidth, a 3M KCl concentration is used. Increasing molarity increases ΔI, but does not affect the relative blockade ΔI/I, where I is the baseline current level. The nanopore is biased at voltages ranging from 300 mV to 900 mV. Given the small diameter of the nanopores, voltage biases

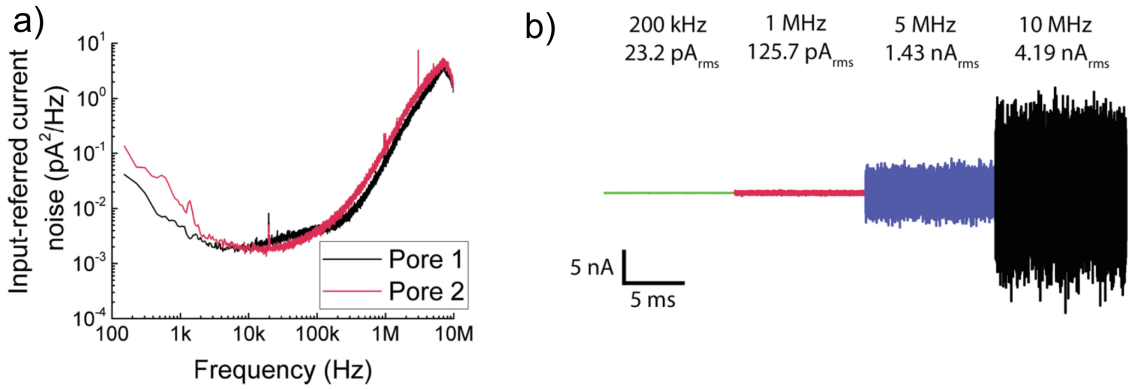

Figure 4.4: a) Noise performance of the CNP amplifier with two different pores summarized in input-referred current noise PSD. Pore 1 has C_{pore} of 10 pF while Pore 2 has C_{pore} of 14 pF. b) Concatenated time trace is for data from Pore 1.

lower than 300 mV frequently cause blockage of the pore. The data are recorded using a custom-designed data acquisition board and software at 40 million samples per second (MSPS) and subsequently filtered to the bandwidths presented here using a digital approximation of a four-pole low-pass Bessel filter. The post-filtered data is then resampled such that the new sampling rate is four times the filter cutoff frequency. Fig. 4.5a,b show translocation data for 100-nucleotide ssDNA through Pore 3 at different voltage biases and cutoff frequencies.

Several previous studies [7, 78, 80] have reported two-level translocation current waveforms as are observed in Fig. 4.5c. Because the diameters of the nanopores used in these experiments are smaller than in any of these previous studies, the access resistance R_{acc} now starts to play a more important role in determining the overall ionic current. In particular, modulation of R_{acc} by a molecule in the vicinity of the nanopore can be significant. The two-level behavior observed is attributed to a

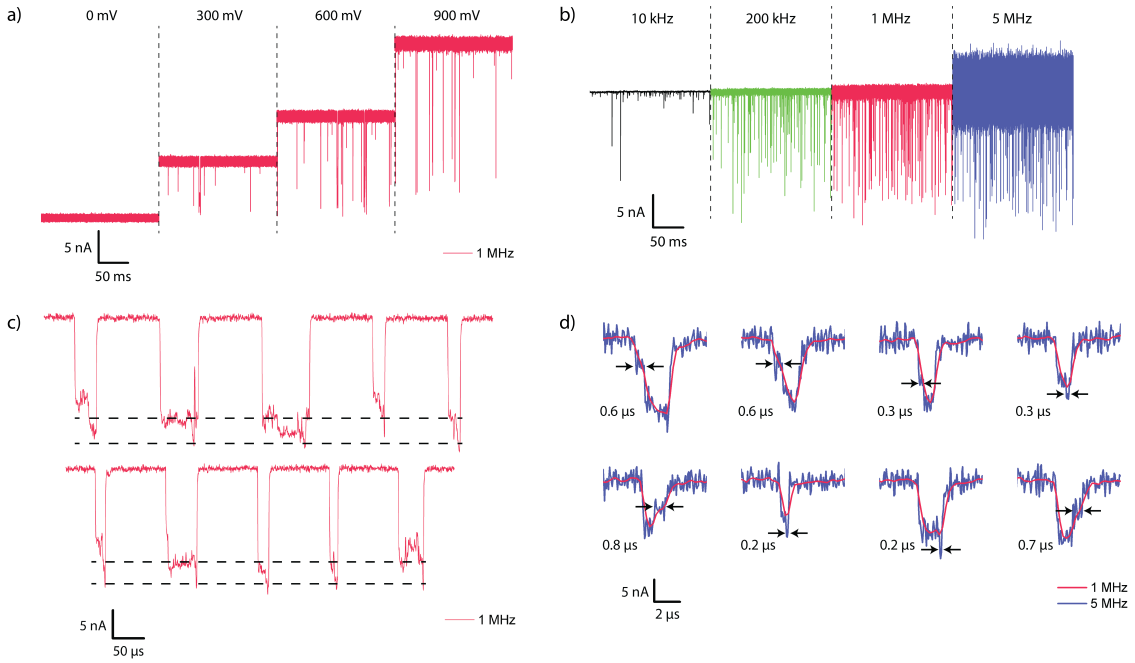

Figure 4.5: (a) Concatenated time trace of 100-nt ssDNA translocation recordings through Pore 3 at biases of 0 mV, 300 mV, 600 mV and 900 mV. Each trace is 0.2 s long and filtered using a 4-pole Bessel filter with a cutoff frequency of 1 MHz. (b) Concatenated time trace of a 0.2 s long recording of 100-nt ssDNA translocation through Pore 1 at 900 mV bias. The traces are filtered using a 4-pole Bessel filter to 10 kHz, 200 kHz, 1 MHz and 5 MHz bandwidths. Low cutoff frequencies show severe degradation of signal amplitudes. All data recorded at 40 MSPS and then resampled to 4x the cutoff frequency. (c) Concatenated events from 100-nt ssDNA translocation through Pore 3 at 900 mV bias padded with baseline points for reference. The dashed black lines indicate the shallow level corresponding to molecule being in the access region and the deep level corresponding to the actual translocation. The standard deviation of the current in the shallow region is significantly higher than even that of the baseline. (d) Example events from 100-nt ssDNA translocation through Pore 1 at 900 mV bias showing features visible at 5 MHz bandwidth (blue) that are invisible at 1 MHz bandwidth (red). Feature durations are indicated.

molecule that gets trapped as it enters or exits the pore. Such an explanation in our case is further bolstered by the fact that the standard deviation of the shallow levels

observed (σ = 834 pA_{rms} to 1.81 nA_{rms} for the data of Fig. 4.5c) is significantly higher than that of the baseline current itself (σ = 281 pA_{rms}). If a molecule in the vicinity of the pore is indeed the cause of the shallow level, then Brownian motion of the molecule could explain the increased standard deviation in the current. A shallow level is not always present at the onset of a translocation event, which is also consistent with previous results.

The need for a high-bandwidth measurement platform is best demonstrated by its ability to resolve and detect events and features that were undetectable previously. Fig. 4.5d shows examples of events filtered to 5 MHz and 1 MHz bandwidths. The four-pole Bessel filter used for filtering down to lower bandwidths has a rise time of 0.5 μs and 0.1 μs at 1 and 5 MHz cutoff frequencies respectively. Consequently, events with durations less than twice these times will have their amplitudes significantly attenuated. Fig. 4.5d shows examples of features that are visible only at bandwidths made possible by this work, some with durations of less than 200 ns.

Fig. 4.6a shows a scatter plot of average current blockade values as a function of dwell time for a 4-s trace recorded for 100-nt ssDNA at 900 mV bias. Event detection is determined by setting a threshold that is 6σ away from the baseline. As the filtering cutoff frequency is reduced, τ decreases, but so does the amplitude of short events which means that some events fail to get detected at lower bandwidths. Conversely, shallow and long events are more likely to be seen at lower bandwidths. Fig. 4.6b also shows fits of the dwell times to $A_1\ e^{-t/\tau_1} + A_2\ e^{-t/\tau_2}$ where $\tau_1 < \tau_2$, τ_1 is attributed to full translocation events while τ_2 is attributed to collision events. [101] More aggressive filtering increases τ_1 indicating that the increased bandwidth results

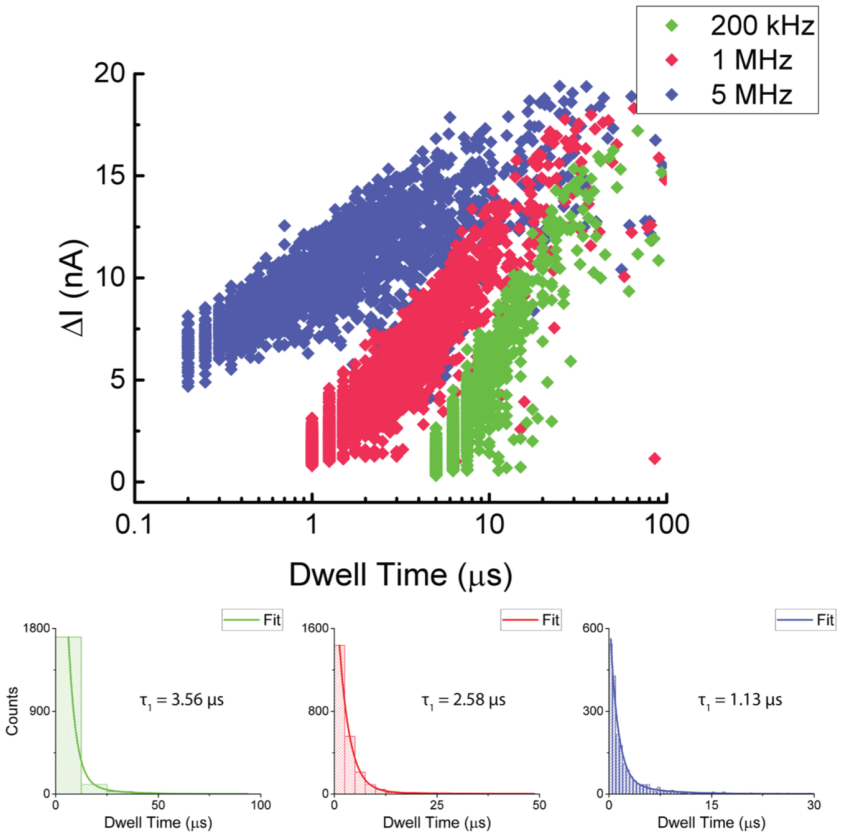

Figure 4.6: (a) Mean current blockage vs dwell time scatter plot for n= 2008 100-nt ssDNA translocation events through Pore 1 at 5 MHz, 1 MHz and 200 kHz filtering bandwidths (n indicated for the 5 MHz filtering bandwidth). Filtering to lower frequencies clearly indicates increased attenuation especially for events close to the inverse of the filter's cutoff frequency. (b) Histogram plot of counts vs dwell time for the data presented in (a). Each of the plots are fitted to$A_1\ e^{-t/\tau_1}+A_2\ e^{-t/\tau_2}$ andτ_1 is indicated for each of the fits where $\tau_1 < \tau_2$. Increasing the filtering bandwidth indicates a reduction in the characteristic dwell time for the event suggesting that even at bandwidths as high as 1 MHz, translocation events were distorted.

presented here are more accurate in capturing the average translocation rate.

4.5 Combination of CNP2 with glass chip

Instead of using the conventional silicon substrate as nanopore membrane carriers, we fabricated fused-silica based substrate as discussed in previous chapter. These glass chip could reduce the capacitance of the noise down below 1pF compared to the 10 pF for silicon substrate. We measure ionic current signals of 90 to 200 nts single stranded DNA translocating through 0.9 to 2nm diameter nanopores in 3 to 8 nm thick amorphous silicon/SiO_x membranes thinned with the STEM technique as described in chpater 2.1.2. The combination of glass chip and CNP2 allows us to achieve the lowest noise in the highest bandwidth available thus far. Fig. 4.7a shows the integrated input-referred noise for pore L (details of pore summarized in Fig. 4.10) at 1MHz is 65.7 pA_{rms}, at 2MHz is 183.1 pA_{rms}, at 5MHz is 690.2pA_{rms}, and at 10MHz is 2.5nA_{rms}. Fig. 4.7b shows the power spectral density (PSD) of the open headstage of the amplifier, the noise spectrum for pore L, and also the pore measured using the same amplifier by Shekar et al. [87] We record a significant reduction in noise at all frequency range. This is due to the effect of an increase in feedback resistance R_F, from 7.5MΩ to 45MΩ, which lowers the noise in the frequencies lower than 100kHz as discussed in section 4.3, and the lower overall capacitance C_{TOT} reduces the noise level for frequencies higher than 100kHz. At 1MHz bandwidth, the noise was only half of what previously measured at any solid state nanopore measuring system. The comparison of previous high bandwidth measurement effort has been summarized in table 4.1.

We perform DNA translocation experiments with a-Si/SiO_x nanopore of sizes smaller than 2nm, thickness from 3-8nm, salt solution of 1MKCl or 3MKCl, and

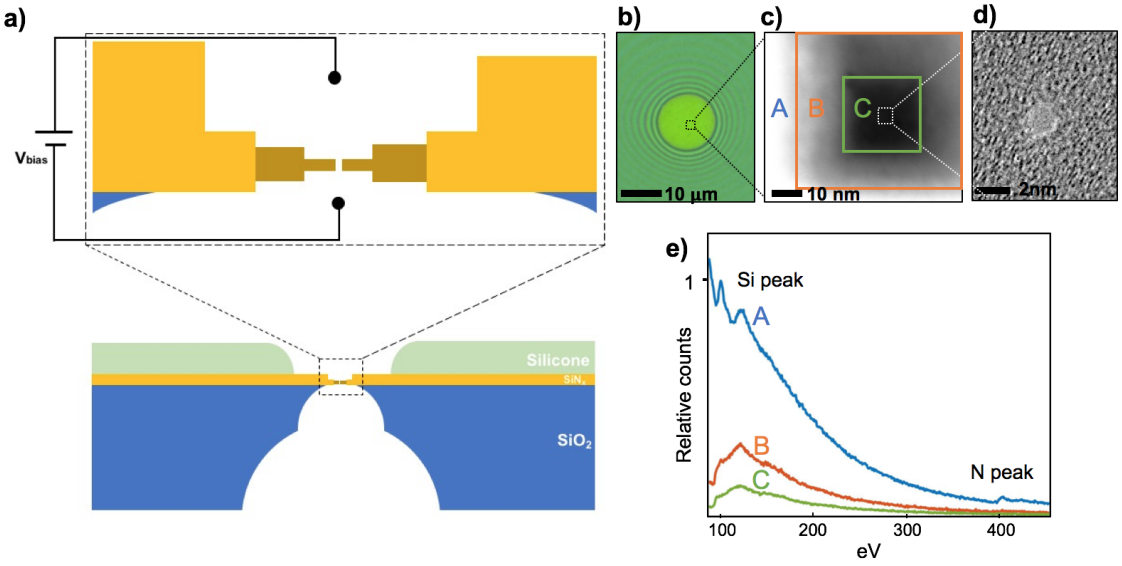

Figure 4.7: (a) Schematics of measurement set-up. (b) Suspended SiNx window on top of fused-silica substrate (c) HAADF image of pore geometry. A is the area that was thinned down to 30nm by RIE etching. B is the area that was thinned using STEM techniques down to about 10nm. C is the area of the second thinning step where we thin down the membrane to 3-8nm. (d) A bright field image of nanopore that is drilled in the thinnest region C in part (c). (e) The EELS spectrum of the respected region in part (c). We could see the N peak is completed depleted when a nanopore is drilled. The Si peak could be used to monitor the thickness of the thin membrane. The figures shows region C has roughly 0.1 relative counts with respect to region A, translating to 3nm thickness.

apply transmembrane bias voltage up to 900mV. Fig. 4.9a shows the translocation sample traces at the unfiltered 10MHz bandwidth, and also at 1MHz, 2MHz, and 5MHz filtering bandwidth filtered by 4 pole Bessel filters. With the reduced noise, we could also visually discern ssDNA translocation events at 10MHz without the need for additional filtering. Fig. 4.9b provides zoom-ins of unfiltered translocation events for various dwell time as short as 100nm. Despite not applying any filters, many

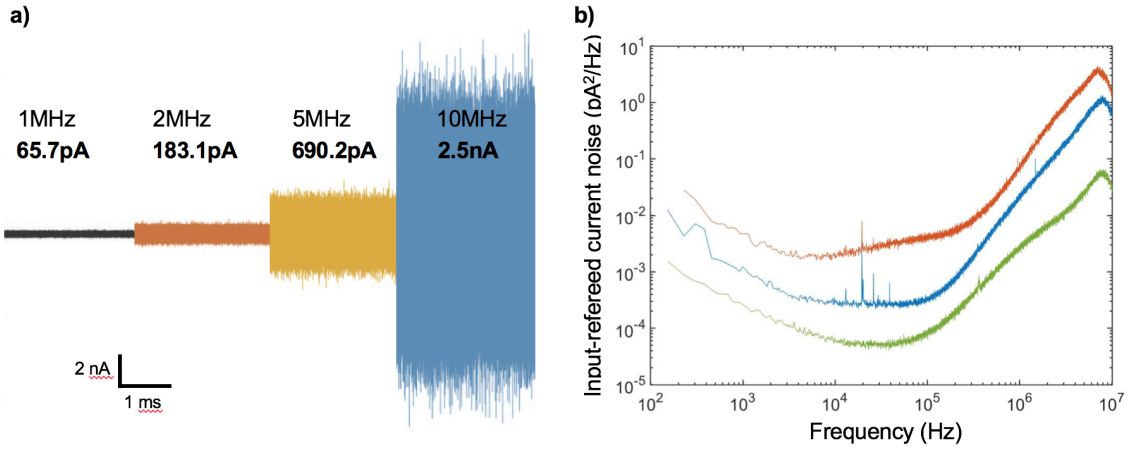

Figure 4.8: (a) Concatenated time trace of a 20 ms long, 0mV baseline measurement of chip1. Each section corresponds to the same trace filtered using a digital four-pole Bessel filter to cutoff frequencies of 1 MHz, 2MHz, and 5 MHz, respectively. The 10 MHz trace has no extra filtering except the effect of an analog four-pole Bessel filter while recording. I_{rms} values are shown below the filtering frequency. (b) Input-referred current noise PSD for the open-headstage configuration of the CNP amplifier (Green), PSD for pore L (Blue), and the PSD for silicon substrate Pore 1 measured in chapter 4.4.

	Rosenstein. et al.	Balan et al.	Shekar et al.	CNP2 + glass
Pore type	SiN_x	SiN_x	a-Si/SiO_x	a-Si/SiO_x
Pore thickness	10nm	100nm	3nm	3-8nm
Pore diameter	4nm	4nm	$<$ 2nm	$<$ 2nm
$V_n(nV/\sqrt{Hz})$	5	1	3.15	3.15
C_{amp}	2.15 pF	20 pF	4 pF	4 pF
C_{pore}	6 pF	1	10	2
Σ C	8.15 pF	21	14	6
Max bandwidth	1MHz	1MHz	10MHz	10MHz
Noise at 1MHz	$155pA_{rms}$	$110pA_{rms}$	$128pA_{rms}$	$65pA_{rms}$

Table 4.1: Comparison of work in high measurement bandwidth

events exceed the 5-sigma threshold, translating to a SNR more than 5. At 10 MHz recording bandwidth, due to the rise time of the event being 50ns, events shorter than twice of this time would be attenuated. As a result, only events longer than 100ns would be truthfully reported. These 100ns events were observed for the first time and these would have been missed or greatly attenuated if any filter being applied. This results also highlight the importance of this high bandwidth, low capacitance measurement capability. As we increase the bandwidth we are observing more event that was undetected previously. Therefore, without slowing down these DNA as it goes through the nanopore, measurements at 10MHz bandwidth or higher is desired and required.

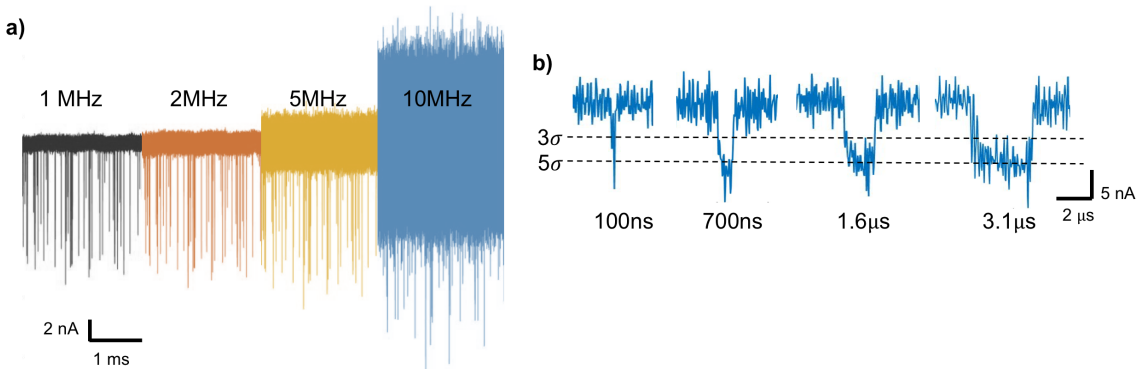

Figure 4.9: . (a) Concatenated time trace of a 0.1 s long recording of 90 nt ssDNA translocation through Pore 1 at 900 mV bias. The traces are filtered using a 4-pole Bessel filter to 1MHz, 2MHz, 5 MHz bandwidths, and also the 10MHz unfiltered data. All data recorded at 40 MSPS and then resampled to 4 $\times$ the cutoff frequency. (b) Sample events of unfiltered 10MHz data of various length. The shorted events are as short as 100ns. Only events that surpass the 5 sigma thresholds are shown here.

With the unprecedented low noise in our measuring system allowing the event traces to be filtered at 2MHz. The results of 13 working pores with short ssDNA

translocations are summarized in Fig. 4.10. It is important to point out that these a-Si/SiN_x pores are working constantly and producing consistent results. These nanometer-thick silicon based pores are as of now the best working devices for nanopore sensing applications. Despite an effort to push forward on 2D pores for its atomic thickness such as graphene, metal dichalcogenides, etc, the results are few and inconsistent and issues of wetting and DNA pore-wall interactions remain. [16, 33]

Chip	Pore diameter (nm)	ELLS Thickness (nm)	Max Voltage (mV)	Dwell Time (us)	I (nA)	△I(nA)	△I/I	Measured G (nS)	Estimated G (nS)	ssDNA (nts)	rate (nts/us)	Notes
A	1.8	3	900	1.39	13.3	4.18	0.31	14.78	21.42	80	57.55	
B	1.2	3	900	3.46	11.7	4.38	0.37	13.00	10.85	200	57.80	
C	1.7	3	900	3.07	18.8	5.98	0.32	20.89	19.58	200	65.15	
D	0.9	3	900	1.80	4.9	2.08	0.42	5.44	6.42	200	111.11	
E	1.8	3	900	3.04	16.1	5.24	0.33	17.89	21.42	200	65.79	
F	1.6	3	900	1.04	13.1	5.03	0.38	14.56	17.75	90	86.54	
G	1.6*2	3	900	1.64	17.8	5.07	0.28	19.78	21.22	200	121.95	4C
H	1.8*2.4	3	600	8.61	17.6	2.78	0.16	29.33	26.61	200	23.24	4C
I	1.6	3	900	0.52	9.3	1.87	0.20	10.3	5.92	90	173.08	1M KCl
J	1.8	5	900	1.56	11.5	2.79	0.24	12.78	4.99	90	57.69	1M KCl
K	1.4*2.2	5	900	3.14	8.8	2.37	0.27	9.78	4.74	90	28.67	1M KCl
L	1.2*1.7	8	700	0.54	18.1	3.73	0.21	25.8	6.09	90	166.67	
M	1.7	8	700	1.45	18.8	2.87	0.15	26.9	8.88	90	62.07	

Figure 4.10: Summary of experiments with ssDNA translocations through glass nanopore. All experiments are performed in 3M KCl, room temperature, glass chips, and STEM thin a-Si/SiO_x pores unless otherwise noted.

Due to the limited time resolution, most solid-state nanopore work assumes the nanopore translocation event as ideal square pulses, or define them as two-level events such as folding or pores being near the access region. [78, 96] However, with enough time resolution, we could see clearly that these simple multi-level assumptions do not capture the rich dynamics and complexity of ionic signals as DNA translocating through nanopore. It has been pointed out that with higher recording bandwidth, we could capture more DNA dynamics in and around the pore that were previously

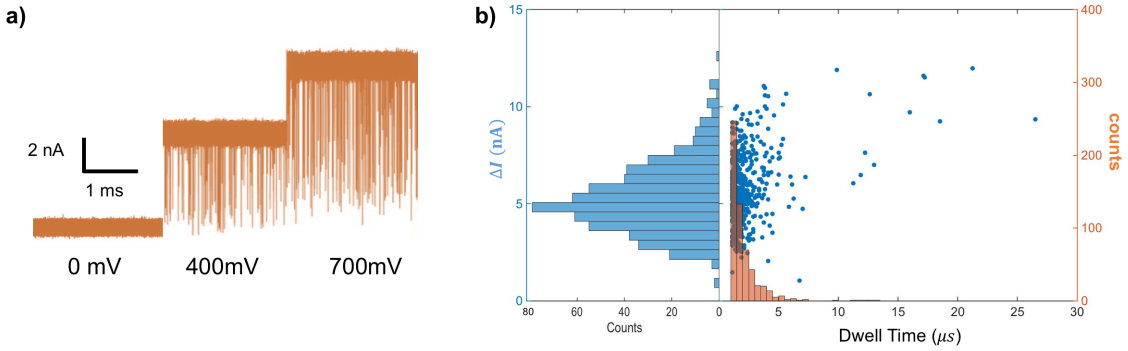

Figure 4.11: (a) Concatenated time trace of 90 nt ssDNA translocation recordings through Pore L at biases of 0, 400, and 700 mV. Each trace is 0.2 s long and filtered using a 4-pole Bessel filter with a cutoff frequency of 2 MHz. (b) The summary of pore L translocations filtered at 2MHz bandwidth. The left graph shows the ΔI vs counts histogram in light blue color. The dark blue color shows the dwell time versus ΔI scatter plots. The orange is Histogram plot of counts vs dwell time.

missing. [80, 87] As we can see in the sample events shown in Fig. 4.9, the events show no distinct two levels results from folding, which should be excluded due to the small pore size not allowing folded DNA to pass through. It exhibits ionic signals fluctuations that could be attributed to sticking, pore-wall interaction, the interactions with pore access resistance, or DNA molecules translocating in different orientations. [13] We quantify this DNA dynamics by defining the intra-event noise as the I_{rms} within a DNA translocation event subtracting the baseline noise as shown in Fig. 4.12a, and as described in the equation

$$I_{rms,intra-event} = \sigma_{intra-event} - \sigma_{baseline}. \tag{4.3}$$

Fig. 4.12b shows the $I_{rms,intra-event}$ for events measured at 700mV in 1 second for

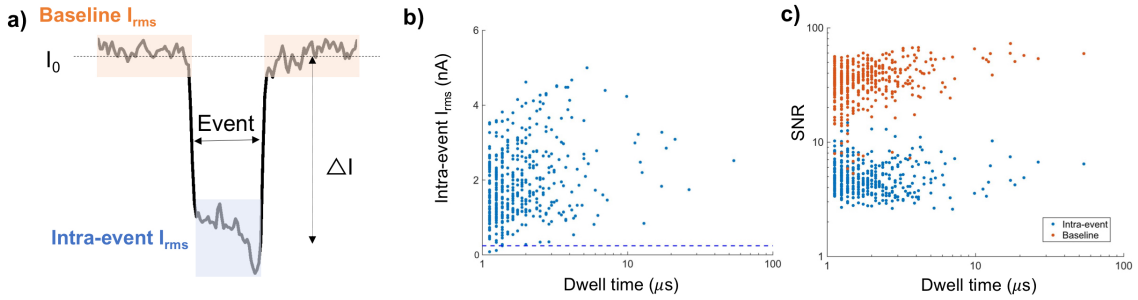

Figure 4.12: (a) Schematics of definition of baseline I_{rms} and Intra-event I_{rms}. (b) The scatter plots of the Intra-event I_{rms} v.s. dwell time. The dotted blue line is the I_{rms} baseline. (c) orange scatter plot shows the $SNR_{baseline}$ vs. dwell time, and the blue scatter plot shows the $SNR_{intra-event}$ v.s. dwell time.

pore L. There is a wide spread of $I_{rms,intra-event}$, with the noise within the event could be more than ten times of the baseline for shallow events, and more than a hundred times for deeper events. This drastic increase of the intra-event noise from the baseline could be due to the stochastic manner DNA translocation through the nanopore. In a measurement, besides noise, the SNR ratio is an indication how well a nanopore sensor perform, and the reliability of signal recordings. Due to the observation of high intra-event noise, it is necessary to define a new SNR to incorporate the effect of these intra-event noise to better quantify the capability of nanopore sensors. Here, we define $SNR_{intra-event}$ as

$$SNR_{intra-event} = \frac{\Delta I}{I_{rms,intra-event}} \tag{4.4}$$

, and ΔI is taken to be the mean value of the current blockage within a translocation event. Fig. 4.12c shows the difference of $SNR_{intra-event}$ and $SNR_{baseline}$. With conventionally defined $SNR_{baseline}$, as described in chapter 2.3, this particular

nanopore could reach SNR = 100 for some events, showing its strong sensing capability. Yet the $SNR_{intra-event}$ is much lower. When looking at the $SNR_{intra-event}$ of two different pores with different sizes in Fig. 4.13a. The smaller pore (1.2nm) shows a higher SNR ratio. This could suggest that smaller pores restrict the movements of DNA as it passes through the pore resulting the reduction in entropy to reduce the intra-event noise. We plot the $SNR_{intra-event}$ versus pore diameter of 13 pores to further examine this hypothesis and the results are summarized in Fig. 4.13b. It shows a slight increase of $SNR_{intra-event}$ when the pore sizes are smaller, yet the spread of the $SNR_{intra-event}$ values are high. There are also many variables that might play an effect here, such as the pore length, exact pore shape, bias voltages, etc. Specific conditions are different for each measurement, therefore more analysis and experiments have to be completed to obtain more conclusive results. Data and analysis presented here serves as a start of future endeavor for controlling the DNA movements as it goes through the nanopore. The reduction of intra-event noise could be achieved by adding secondary structures to channel the DNAs or making the nanopore exactly the right size and geometry to pass through the DNAs.

The DNAs we pass through these nanopores are either 200 nts of concatenated 50C50A50C50A ssDNA, 80 nts 20C20A20C20A ssDNA, or 90 nts 30C30A30C ssDNA. With the time resolution we have, even in the long events there was no observed distinct level corresponding these different nucleotides, mostly due to the high entropy of DNA movements when going through the pores having a more pronounced influence on the ionic current than the ion exclusion effects attributed to the different sizes of neucleotides.

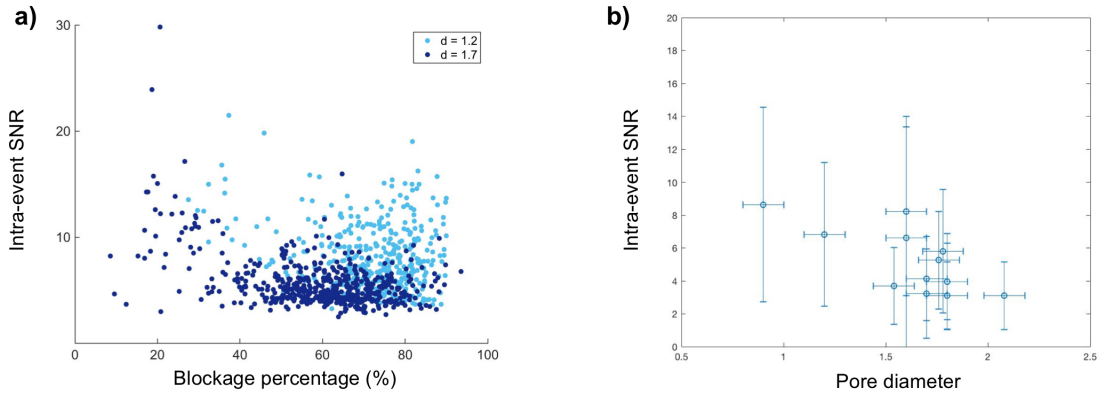

Figure 4.13: (a) Scatter plot of intra-event SNR of pores diameter = 1.2 nm and another pore with pore diatmer = 1.7nm. (b) Scatter plot of averaged intra-event SNR at different pore diameters. The error bar in diameter is chosen to be ± 0.1 nm for measurement error from the TEM imaging.

4.6 Summary

In conclusion, we presented a nanopore recording systems showing the highest bandwidth of DNA translocations at 10MHz bandwidth by combining the custom low capacitance CMOS ampliers and low capacitance nanopore device. We also highlighted the importance of performing analysis at high bandwidth and observe and analyze intra-event noise related to the DNA translocation dynamics. Improvements on reducing the intra-event noise would be as important as the common effort in reducing baseline noise. These high bandwidths measurement may enable new applications for nanopores that rely on the ability to resolve single-molecule transient events on heretofore unachievable time scales.

Chapter 5

Beyond A Single Nanopore

5.1 Nanopore array

The applications of nanopore devices are not only limited to having a single nanopore on the membrane. While a single-nanopore device is a powerful tool for single molecule analysis, there is a constraint to its capability due to the limited flux through a single pore. When there are multiple pores present on the same membrane, the volume flux or through-put could be increased. This is especially beneficial for applications that require large flux such as water desalination or nanosieve. [9, 94] One type of the multiple nanopore membranes, or nanoporous membrane, are randomly distributed defects on a solid-state membrane such as silicon nitride, graphene, and metal dichalcogenides, etc. This is achieved by controlling the growth process to create defects, or etching with acid, light, or oxygen plasma, or exposing it with high energy ions. [91, 93] The other type of the multiple nanopore membranes are ordered

nanopores patterned usually by lithography to create arrays of nanopores. This has found use in increasing through-put of fluorescent molecule detection with nanopore arrays, as zero-mode waveguides, or making antidots to tune the properties of the materials of 2D materials. [14, 52, 55]

5.1.1 Nanopore arrays on silicon nitride membrane

One straightforward method of fabricating nanopore arrays was using TEM. By using the TEM in STEM mode as described in chapter 2.1.2, this technique allows us precise control of the thickness of the membrane and position of the nanopore by monitoring the high angle annular dark field (HAADF) image and EELS spectrum. Nanopore arrays with small diameters of pores could be fabricated within half an hour as demonstrated in Fig. 5.1.

While the STEM technique could be used to fabricate nanopore arrays, it is relatively time consuming and low yield when a large number of pores are required. Hence, a protocol of electron beam lithography was designed to fabricate nanopore arrays that could covers the whole membrane with tunable pore sizes. [98] Fig 5.2 shows the flow of fabrication.

We spin coat anisole diluted ZEP520A (ZEP520A: anisole = 1:3) onto 25nm of LPCVD silicon nitride membrane. The membrane is put inside Elionix ELS-7500EX electron beam lithography to pattern arrays of nanopores. Dots-on-the-fly is the technique most useful when patterning these nanopore arrays. Instead of drawing patterns of hundreds of circles, we pattern a square of size of that of the membrane as we would want for conventional Ebeam, and increase the exposure shot pitch and

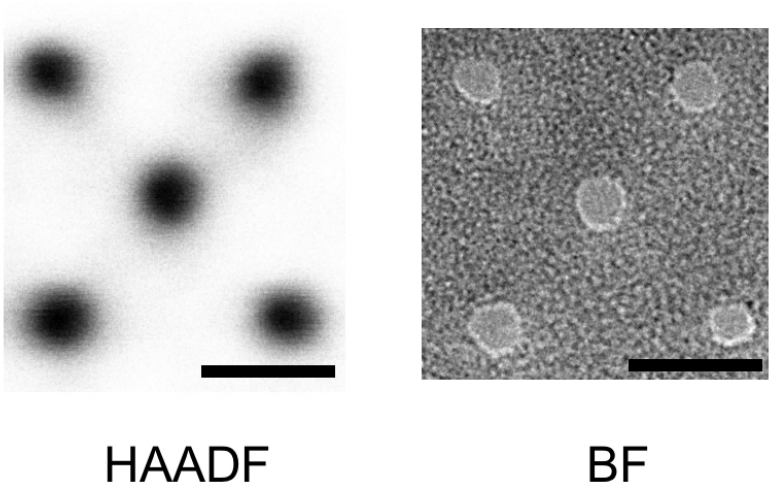

Figure 5.1: (a) HAADF and (b)BF images of the 2×1×2 nanopore array drilled in STEM mode.

electron dose at each spot to pattern the desired arrays. The increased shot pitch will make the electron beam exposure spot separated from each others resulting in arrays of ebeam dots. A schematic to show how the dot-on-the-fly technique is shown in Fig. 5.3. Elionix runs on a 20MHz fixed clock, therefore it could pattern thousands of pores within a minute. However, if we choose to pattern individual circles, the electron beam will have a rest time at the start of each pattern beyond the dose time, resulting in increased patterning time at least an order of magnitude. With this dots-on-the-fly method, we could make homogeneous circular pores as small as 20 nm in diameter across the whole membrane with a distance between each pore less than 100nm. After developing away the exposed region, the device is put inside RIE etcher to etch away silicon nitride membrane by CHF_3 and O_2, creating holes as

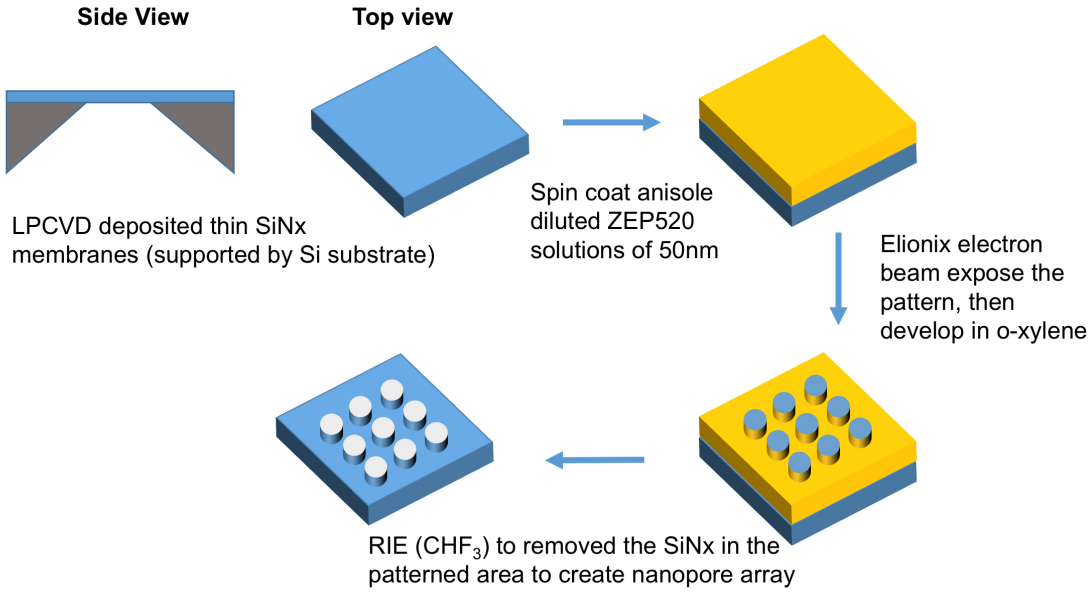

Figure 5.2: Illustration of fabrication of nanopore arrays in Ebeam lithography

shown in Fig. 5.4.

This type of high density nanopore array membrane has found use as molecular sieve or ultra-high permeable membrane device. [9, 94] Fig. 5.5 could further tune the size of nanopore by putting the nanopore arrays inside an ALD to shrink the pores by depositing Al_2O_3 all around the pores, across the whole membrane. [10] With the ALD shrinkage we were able to fabricate nanopore arrays with nanopore diameters less than 10nm.

5.1.2 Phosphorene nanopore arrays as antidots

Few-layer black phosphorus (BP) has prompted much interest recently due to the balance it brings between the semiconducting band gap and large on/off ratio of tran-

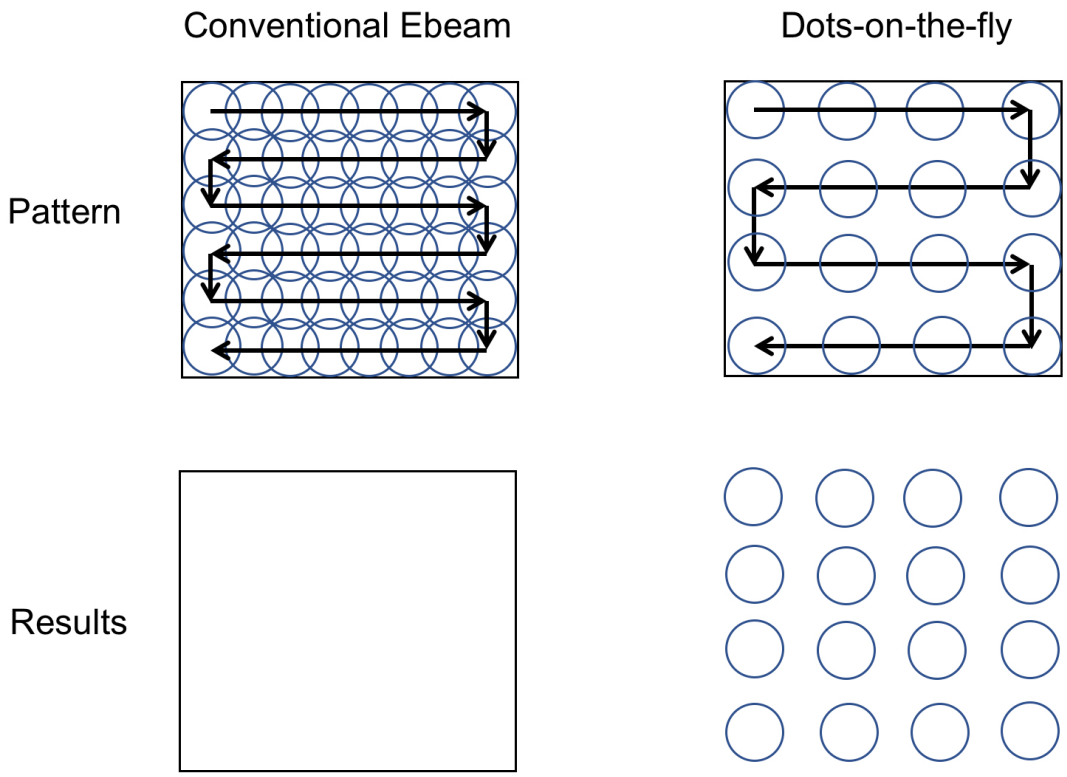

Figure 5.3: In conventional Ebeam lithography, when you draw a square, the electron beam will expose in a fashion illustrated on the top left corner. The electron beam exposure will overlaps creating a square feature. However, if we increase the shot pitch to leave space between each exposure spot, it would results in dots array instead of a complete circle. The dose could be tuned to alter the size of the nanopores.

sition metal dichalcogenides, and the high carrier mobility of graphene.[61] However, in order to make single-layer black phosphorus (phosphorene) more widely applicable in optoelectronic devices it is necessary to devise methods to tune its 2 eV electronic (transport) band gap as measured by scanning tunneling spectroscopy.[60] Nanostructures obtained by dimensionally reducing bulk BP to few-layers, nanoribbons

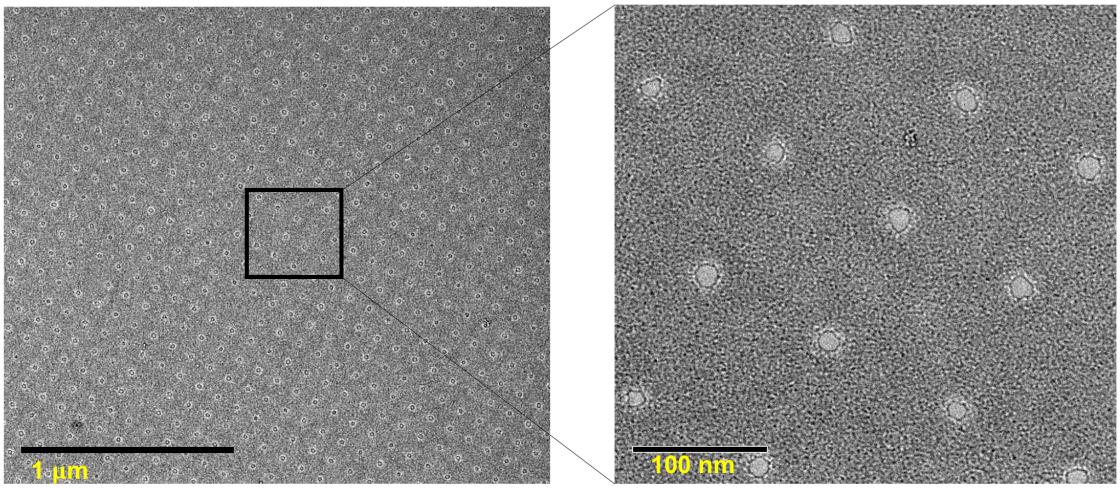

Figure 5.4: An example of nanopore arrays fabricated with Ebeam lithography. The nanopores could be less than 100nm apart from each others, and the pore sizes are less than 20nm.

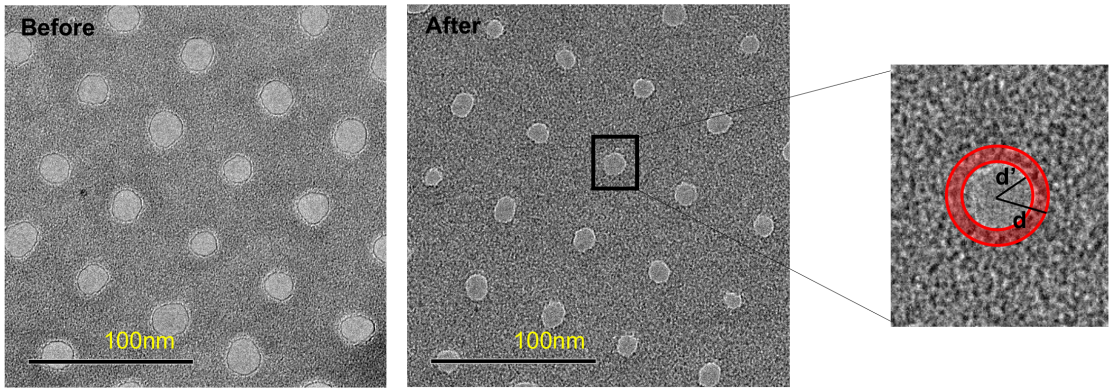

Figure 5.5: Images of the nanopore arrays before and after 40 minutes of Al_2O_3 deposition in ALD. The red rings area in the zoom-in image shows the Al_2O_3 layer, which could be estimated by the original pore radii (d) subtracting the final pore radii (d')

(NRs), and quantum dots exhibit shifts in the intrinsic band gap due to quantum confinement. [15] A dimensionally reduced form of phosphorene which has yet to be explored electronically is the antidot lattice,[104] which is a periodic array of holes embedded into a material. From the simplest perspective, shifts in the energy levels are expected due to quantum confinement in the nanoconstrictions between the holes. The entire structure can be also construed as a network of curved NRs in two dimensions. Effects due to edge configuration and dopant are also expected, as is the case for phosphorene nanoribbonss. [39, 72] Theoretical studies have already predicted a tunable band gap in antidot lattices composed of graphene, [70] MoS2, [84] and hexagonal BN. Nanoscale antidots in few-layer BP capped by an oxide layer are fabricated using plasma thinning along with electron beam (Ebeam) lithography. The structures are subsequently characterized by Raman spectroscopy.

Fig. 5.6 demonstrates the step-by-step fabrication procedure we developed to create antidot lattices in few-layer black phosphorus flakes using electron beam lithography, which has previously been used to fabricate similar structures in graphene. [21, 82, 88] Bulk BP flakes are first mechanically exfoliated onto SiO2/Si substrates and thinned using a previously reported oxygen (O2) plasma etching technique (Fig. 5.6a). [71] The thinning process allows for precise control of the few-layer BP thickness and introduces a phosphorus oxide (P_xO_y) capping layer that greatly improves sample stability during lithography and in-air Raman measurements (Fig. 5.6b). We find that a few-layer BP thickness of between 8 and 10 nm (13-16 layers) minimizes oxidation effects on the Raman map while maximizing signal-to-noise ratios. Since thinner BP samples experience an increased rate of oxidation and a drop in Raman

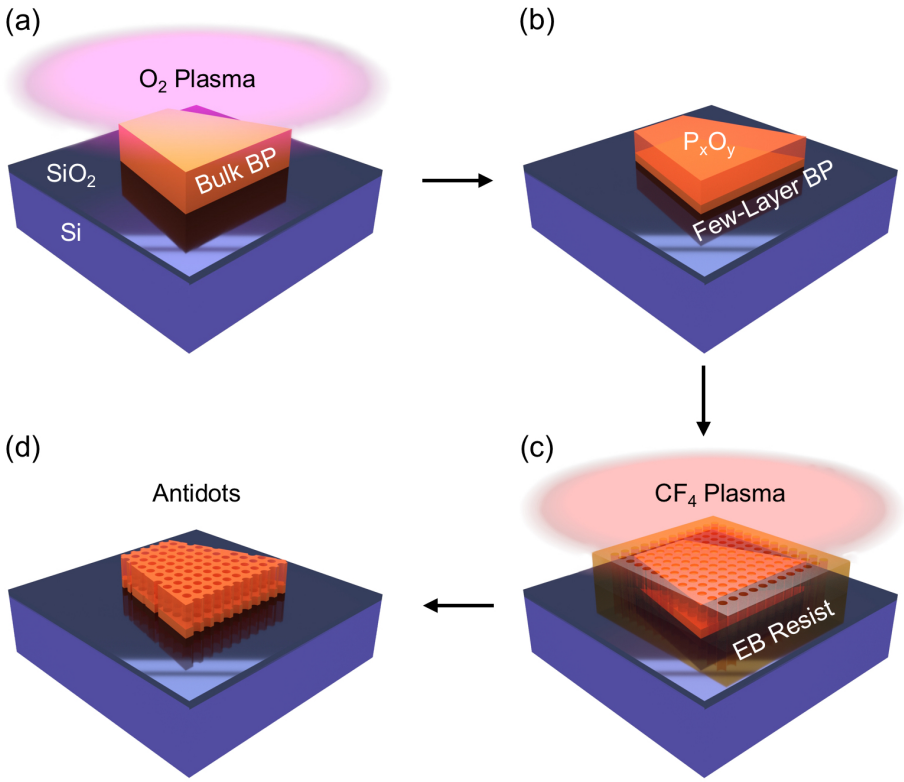

Figure 5.6: (a) Exfoliation and O_2 plasma thinning of bulk BP on a SiO_2/Si substrate yields (b) a P_xO_y-capped few-layer BP. (c) After the sample is coated in resist, antidot arrays are patterned using electron beam (Ebeam) lithography and etched in CF_4 to remove the exposed P_xO_y/BP. (d) Finally, the process yields a P_xO_y-passivated few-layer BP antidot lattice. Typical superlattice constants (SC) and antidot radii (R) are 60-65 nm and 13-23 nm, respectively.

signal intensity,[35] samples thinned to this range of 8-10nm allow us to obtain measurable Raman signals with minimal oxidation over time scales of 10-12 hours. After thinning, samples are coated with a thin layer of 50nm anisole-diluted ZEP520 resist and antidot arrays are patterned using Ebeam lithography (Fig. 5.6c) by dots on the fly technique as described in Fig. 5.3. Tetrafluoromethane (CF4) plasma is then

used to etch away the exposed material, resulting in an antidot-patterned few-layer BP flake passivated with P_xO_y (Fig. 5.6d). After resist removal, the flakes are exposed to an additional plasma-cleaning step. An optical image of a few-layer BP flake containing an antidot lattice is given in Fig. 5.7a. Due to the thickness, oxidation, and orientation-dependent properties of black phosphorus, [6, 61] regions (1) and (5) of the flake were not subjected to antidot patterning and are referred to as pristine. Regions (2), (3), and (4) correspond to a few-layer BP antidot lattice, P_xO_y, and a strip of the bare SiO_2/Si substrate, respectively. SEM images of multiple samples reveal highly uniform antidot lattices with superlattice constants (SC) of 60-65 nm and radii (R) of 13-23 nm (Fig. 5.7c), in line with the smallest reported graphene antidots fabricated via Ebeam lithography. [82]

Here, we use Raman spectroscopy in order to analyze the effects of forming antidots in few-layer BP. The Raman spectrum from a 532 nm excitation line for black phosphorus reveals one out-of-plane mode (A_g^1) and two in-plane modes that are associated with phonons in the zigzag (B_{2g}) and armchair (A_g^2) directions. In particular, the frequency of the A_g^2 mode exhibits a strong thickness dependence with shifts from 466 cm^{-1} for bulk black phosphorus up to 470-471 cm^{-1} for monolayer phosphorene. [23, 62] Thinned BP flakes, such as those found in region (1) from Fig. 5.7a, exhibit A_g^1 (362 cm^{-1}), B_{2g} (439 cm^{-1}), and A_g^2 (467 cm^{-1}) peaks that are consistent with a few layer (8-10 nm) structure (Fig. 5.7b). Upon patterning, the antidot region (2) exhibits negligible changes ($\pm$ 0.5 cm^{-1}) in the frequency of all three major Raman modes. Furthermore, this result indicates the structure is likely free of any strain since stretching- and compression-induced Raman frequency shifts up to 11 cm^{-1}

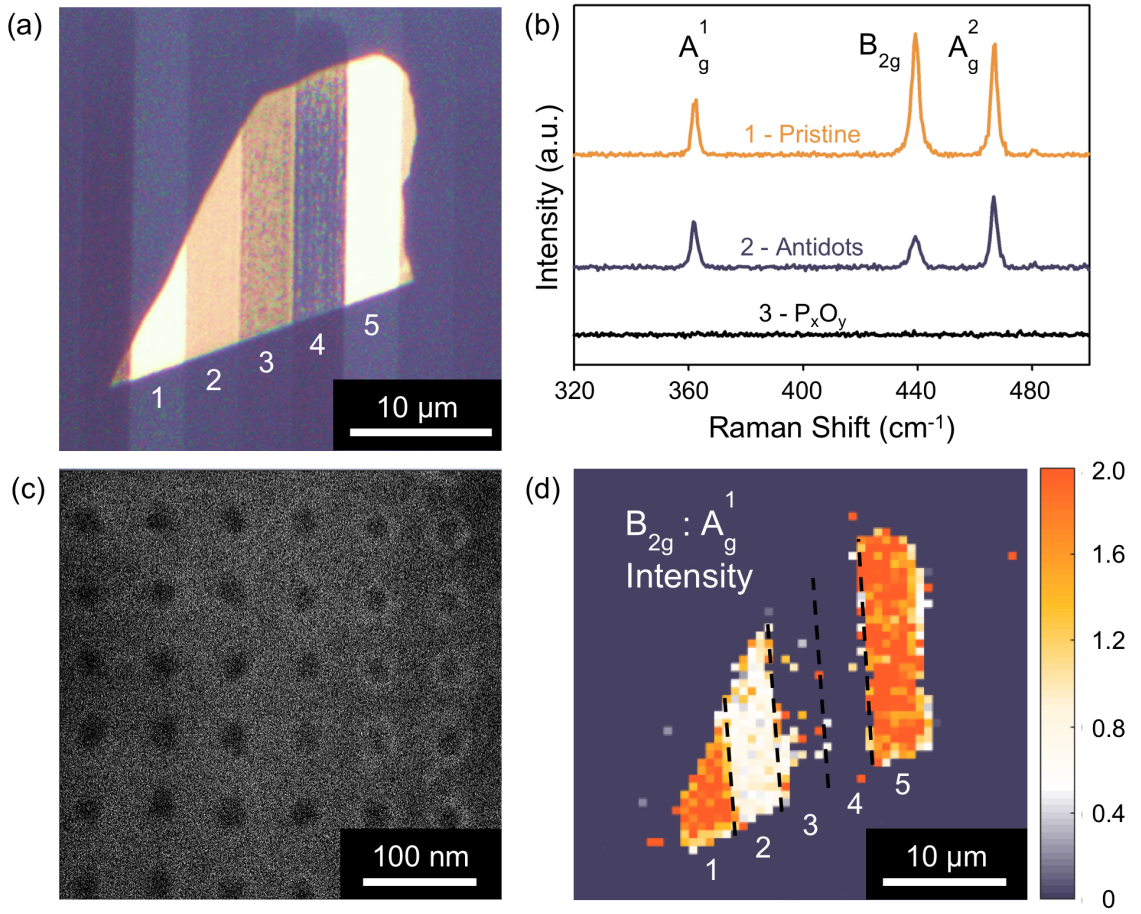

Figure 5.7: (a) Optical image of columnar regions with (1) pristine few-layer BP, (2) patterned antidots (SC = 60 nm and R = 23 nm), (3) P_xO_y, (4) bare SiO_2/Si substrate, and (5) pristine few-layer BP. (b) Raman spectra of (1) pristine few-layer, (2) antidot, and (3) PxOy regions normalized to the A_g^2 peak of (1), showing suppression of the in-plane modes (B_{2g} and A_g^2) in the antidot region. (c) SEM image of a square antidot array with SC = 65 nm and R = 13 nm. (d) B_{2g}: A_g^2 intensity Raman map from the sample in (a). Note: SC is the average in-plane superlattice constant and R is the average antidot radius.

(% strain) are expected in both phosphorene and few-layer BP.[24, 107] On a side note, over-etching results in only amorphous P_xO_y (region (3)), which displays no discernible Raman signature as expected (Fig. 5.7b). [71]

As shown in Fig. 5.7b, we observe suppression of both in-plane modes in the antidot lattices in comparison to pristine few-layer BP. Fig. 5.7d graphically shows that from the pristine few-layer BP to the patterned antidot region, the normalized B_{2g}:A_g^1 intensity ratio exhibits a significant drop from roughly 2.0 to 0.9, suggesting relatively strong suppression of the in-plane zigzag phonon mode. While strengthening of the in-plane Raman D mode in graphene antidot lattices has been shown to be due to fabrication-induced defects, suppression of the in-plane G mode has been attributed to a change in the phonon density of states (DOS) resulting from antidot-induced quantum confinement and follows a similar trend to what is demonstrated here.[44, 48, 110]

5.2 Nanoribbon-nanopore FET device

There are limits for nanopore as we measure transmbranes ionic signal as it is limited by the ion flowing through a nanometer-in-size constrictions. Therefore, ideas such as putting a field effect transistor (FET) device next to the nanopore to augment the signal, to multiplex, and to increase the measurement bandwidth was proposed and tried. Theoretical work of placing a graphene nanoribbon near a nanopore shows potential DNA base discrimination. [76, 81] Experimental work has been performed on placing a nanopore next to graphene ribbons or silicon nanowires. There have

been detections of DNA molecules by these devices, yet the experimental results are still few and the results are mixed. [42, 68, 77, 95, 103]

5.2.1 Poly-crystalline silicon nanoribbon

Here we demonstrate another method to fabricate these nanoribbon-nanopore device. As described in chapter 2.1.2, when rastering electron beam on silicon nitride membrane for a long enough time, the nitrogen atom will be completely sputtered out ahead of the silicon, leaving an area of amorphous silicon membrane. [78] We could make use of this technique and fabricate a suspended amorphous silicon nanoribbon surrounded by SiN_x as shown in Fig. 5.8a. The starting SiN_x membrane thickness is 75nm, and when the nitrogen is depleted, there are about 25nm think of a-Si remains.

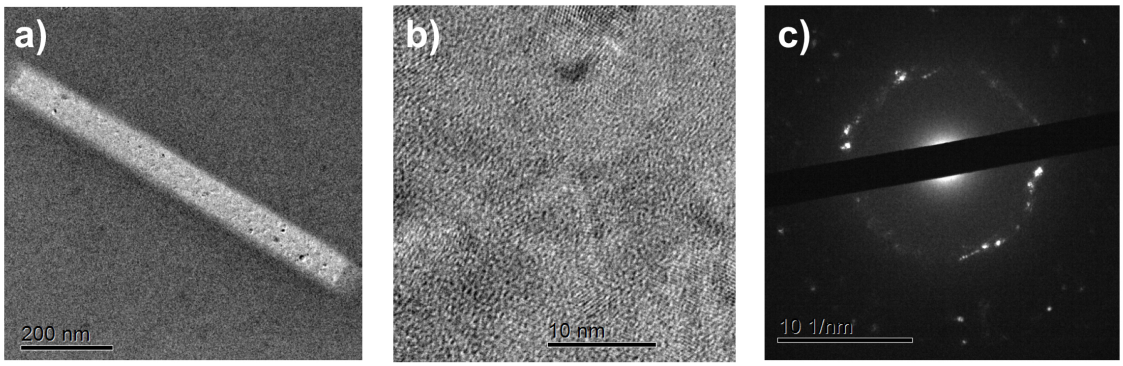

Figure 5.8: (a) An gallium-doped, annealed a-Si nanoribbon that is about 1μm long, and 50nm wide. (b) bright field TEM image showing poly-crystalline structures of the silicon nanoribbon (c) electron diffraction pattern showing different orientations of the silicon crystal structure

Gallium-doped silicon is an n-type semi-conductor.[5] We could expose the a-Si nanoribbon under gallium ion beam to fabricate Ga-doped silicon nanoribbon with a

dose of 5×10^{14} (ions/cm^2). This gallium doping could be confirmed by EDX signals in TEM (Ga Kα line peak at approximately 9.3eV as shown in Fig. 5.9.)

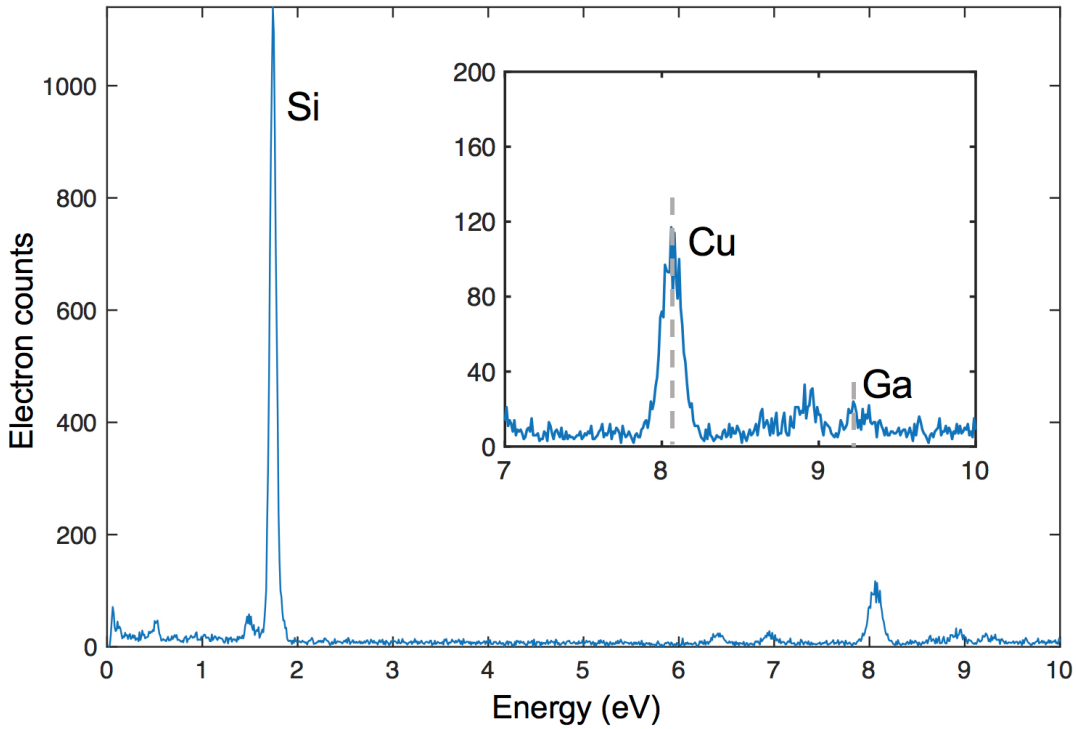

Figure 5.9: EDX spectrum of gallium doped a-S nanoribbon. We could detect the gallium using EDX in JOEL 2010F TEM. The gallium Kα line shows up at 9.3eV. Copper peak is due to the TEM chip holder, not from the nanoribbon sample itself.

We could leave this gallium doped silicon nanoribbon into furnace to anneal at 750C for 2 hours with slow cooling for hours afterwards. [41, 105] Putting this annealed device back into the TEM we observe amorphous silicon being annealed into poly-crystalline silicon, and the diffraction pattern confirms the poly-crystalline silicon structure as shown in Fig. 5.8b,c. To test its electrical property, a precisely aligned electrodes are patterned by electron beam lithography and chrome-gold elec-

trode (3 nm of chrome for adhesion, and 50nm of gold) are evaporated on top of the nanoribbon as shown 5.10. The design of the electrodes is so that some of the contacts land on the nanoribbon, some land on the SiN_x membrane. We could then measure the difference between contacts that are connected by a silicon nanoribbon and compared to those are not. With 2-point measurement, these poly-crystalline silicon nanoribbon devices shows G-Ohm range of resistance, indicating proper back-gating or side-gating are required. Ways of increasing the conductivity of this device are required to make this nanoribbon an effective FET device, including introducing proper gating or increasing the silicon crystallinity. [77, 105]

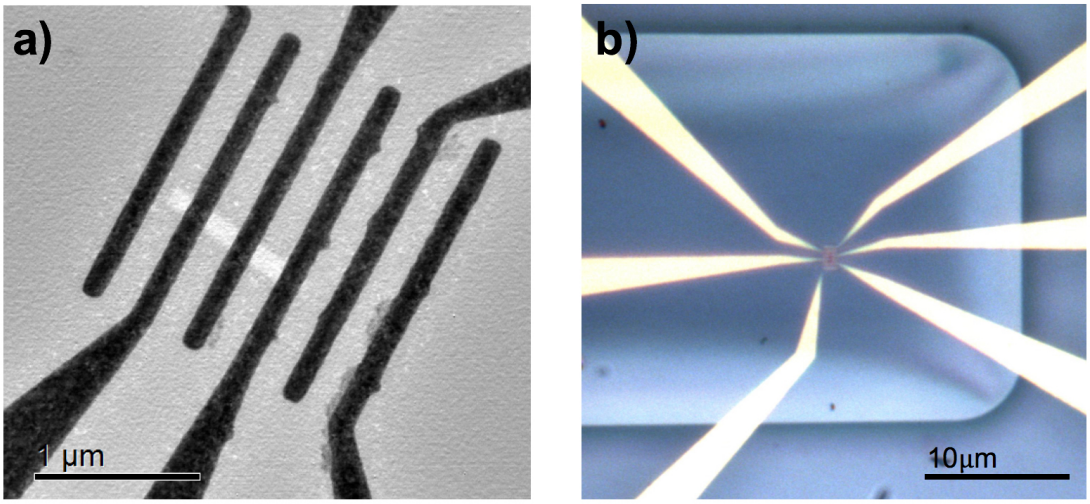

Figure 5.10: (a) Bright field TEM and (b) Optical image showing the electrodes sitting on top of the silicon nanoribbon.

Unlike graphene and other 2D materials nanoribbon-nanopore devices, which encounters issue of wetting and no translocation events occurring, this silicon based device and nanopore has an established protocol of wetting and DNA will pass through

these silicon based device without problems. This makes this type of silicon-based nanoribbon-nanopore FET device a promising direction to explore.

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