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Flexible, Photopatterned, Colloidal Cdse Semiconductor Nanocrystal Integrated Circuits

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Flexible, Photopatterned, Colloidal Cdse Semiconductor Nanocrystal Integrated Circuits

Abstract

As semiconductor manufacturing pushes towards smaller and faster transistors, a parallel goal exists to create transistors which are not nearly as small. These transistors are not intended to match the performance of traditional crystalline semiconductors; they are designed to be significantly lower in cost and manufactured using methods that can make them physically flexible for applications where form is more important than speed. One of the developing technologies for this application is semiconductor nanocrystals.

We first explore methods to develop CdSe nanocrystal semiconducting "inks" into large-scale, high-speed integrated circuits. We demonstrate photopatterned transistors with mobilities of 10 cm2/Vs on Kapton substrates. We develop new methods for vertical interconnect access holes to demonstrate multi-device integrated circuits including inverting amplifiers with ~7 kHz bandwidths, ring oscillators with <10 >µs stage delays, and NAND and NOR logic gates.

In order to produce higher performance and more consistent transistors, we develop a new hybrid procedure for processing the CdSe nanocrystals. This procedure produces transistors with repeatable performance exceeding 40 cm2/Vs when fabricated on silicon wafers and 16 cm2/vs when fabricated as part of photopatterned integrated circuits on Kapton substrates.

In order to demonstrate the full potential of these transistors, methods to create high-frequency oscillators were developed. These methods allow for transistors to operate at higher voltages as well as provide a means for wirebonding to the Kapton substrate, both of which are required for operating and probing high-frequency oscillators. Simulations of this system show the potential for operation at MHz frequencies. Demonstration of these transistors in this frequency range would open the door for development of CdSe integrated circuits for high-performance sensor, display, and audio applications.

To develop further applications of electronics on flexible substrates, procedures are developed for the integration of polychromatic displays on polyethylene terephthalate (PET) substrates and a commercial near field communication (NFC) link. The device draws its power from the NFC transmitter common on smartphones and eliminates the need for a fixed battery. This allows for the mass deployment of flexible, interactive displays on product packaging.

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First Advisor
Cherie R. Kagan

FLEXIBLE, PHOTOPATTERNED, COLLOIDAL CdSe

SEMICONDUCTOR NANOCRYSTAL INTEGRATED CIRCUITS

F. Scott Stinner

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in

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To my family, my friends, and all who supported me, especially cheese doodles

ABSTRACT

FLEXIBLE, PHOTOPATTERNED, COLLOIDAL CdSe

SEMICONDUCTOR NANOCRYSTAL INTEGRATED CIRCUITS

F. Scott Stinner

Cherie Kagan

As semiconductor manufacturing pushes towards smaller and faster transistors, a parallel goal exists to create transistors which are not nearly as small. These transistors are not intended to match the performance of traditional crystalline semiconductors; they are designed to be significantly lower in cost and manufactured using methods that can make them physically flexible for applications where form is more important than speed. One of the developing technologies for this application is semiconductor nanocrystals.

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Chapter 1 : Background

1-1 : Colloidal Semiconductor Nanocrystals

Nanocrystals are being broadly developed for a variety of applications, including sensors,[1] displays,[2] thermoelectric cells,[3] integrated circuits (IC)[4,5], and solar cells[6,7]. Their solution processability and low cost make them a desirable material for emerging technologies looking to exploit novel deposition techniques for unconventional applications, such as flexible electronics. Their tunable optical properties make them desirable for making photodetectors with a broad range of parameters as well as solar cells competitive with cells made from more expensive fabrication methods.

A wide variety of nanocrystals can be made in large quantities with monodisperse properties using chemical synthesis techniques. Changing parameters and materials in these syntheses can adjust properties of the product including size, shape, chemical composition, and surface chemistry.[8–10] These parameters allow the particles to be synthesized with properties matching their desired usage. Further processing after synthesis allows these properties to be changed as well as for the introduction of surface chemistries not compatible with the synthesis process.[11–13]

This work focuses on the use of cadmium selenide (CdSe) nanocrystals (NCs). They are formed using a hot injection synthesis process, as described in literature.[14] The size and surface chemistry of these particles can be tuned to fit their application. For the work described in this dissertation, we use NCs that are approximately 4 nm in diameter and are stabilized in solution using trioctylphosphine oxide (TOPO) ligands on their

surface. Following synthesis, the TOPO ligands are replaced in a chemical exchange process by thiocyanate (SCN). As SCN is a much shorter molecule than TOPO, this allows increased interparticle coupling and greater transport of electronic carriers through films formed from this material.

1-2 : Nanocrystal TFTs

In order to create a direct application of these materials, thin-film transistors (TFTs) can be formed using CdSe NC films with SCN ligands as the semiconducting layer. The simplest form of these TFTs uses a heavily doped silicon wafer coated with thermal oxide as the gate and oxide of the transistor. The semiconducting material is then deposited on this substrate and patterned metal contacts are added to create the source and drain. These types of TFTs have been demonstrated with multiple exchange procedures[15,16] with varying results.

These TFTs can also be doped using a variety of different techniques including chemical treatments[17–19] as well as the direct deposition of metals.[15,20–22,11] For this work, indium is used as a dopant as it can be easily deposited by thermal evaporation. It then diffuses into the NC film by annealing as it has very low melting point.[15]

Using these techniques, high performance TFTs have been demonstrated with mobilities exceeding 30 cm^2/Vs.[15] This performance, while not competitive with crystalline semiconductors, is competitive with other low-cost, solution processable semiconductors including $MoSe_2$ (50 cm^2/Vs[23]), carbon nanotube arrays (35 cm^2/Vs[24]),

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sol-gel metal oxides (14 cm^2/Vs[25]) and sol-gel IZO and IGZO (30 and 20 cm^2/Vs, respectively[26]) This performance is adequate for many low-speed applications including sensors and displays.

1- 3 : Low-Speed Flexible Nanocrystal Integrated Circuits

Single TFT devices, while interesting, have very few direct applications. In order to transition CdSe NC-TFTs from concept to applicable technology, multi-TFT integrated circuits (ICs) have to be demonstrated. Thus, our group previously developed multi-TFT ICs which utilize shadow mask patterning allowing simple fabrication.[4] This technique avoids air and chemical exposure of the NC films, both of which can cause significant damage. This allows simple demonstrations to be developed using procedures not drastically different than those used for the original single-TFT demonstrations.

When creating ICs, the most important structure is called the vertical interconnect access or VIA. This structure creates a vertical connection between different layers of metal in a circuit, such as between a layer used for gating and a layer used for contact to the source and drain of the TFTs, as was needed for CdSe NC-ICs. For these simple TFTs, a method was developed to exploit the chemical instability of oxides on gold.
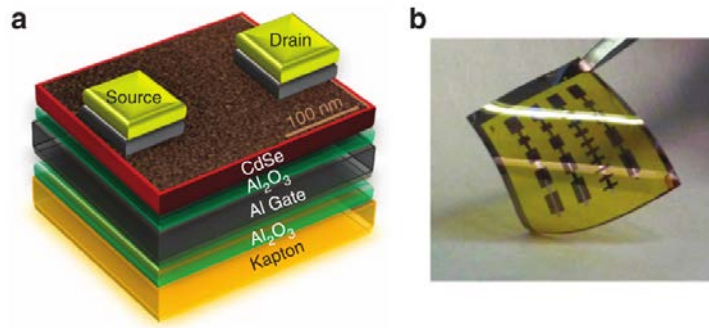
Figure 1-1 (A) Schematic of shadow mask patterned CdSe NC FET on Kapton substrate. (B) Photograph of shadow mask patterned CdSe TFTs. (Reproduced from Kim, D. *et al*, 2012)

The bottom layer of the transistor structure is the gating layer, shown schematically in Figure 1-1A. Aluminum is used due to its similar work function to that of doped CdSe NCs as well as its chemical compatibility with the high-k dielectric constant material alumina, which is used as the gate dielectric layer in these TFTs. A patterned gold layer can be deposited on top of this aluminum layer, creating a vertical pillar of gold used as the VIA. Following this gold deposition, a layer of alumina is deposited by atomic layer deposition (ALD) which is a chemical vapor deposition process. For thin layers of alumina, this process creates an unstable oxide top of the gold.

This unstable layer of oxide is believed to be removed during subsequent processing steps leaving an oxide on top of the aluminum gate sections and a bare gold surface where the VIAs are deposited creating a conductive vertical pathway.

This work also utilized a flexible substrate for fabricating these TFTs. The substrate used is polyimide film, which is purchased commercially and is commonly known under the DuPont trade name Kapton, shown in Figure 1-1B. This film has a high tensile strength, chemical resistance, and melting point allowing it to be easily incorporated into procedures common to semiconductor manufacturing.

The largest drawbacks to this material during fabrication are its inherent flexibility and high coefficient of thermal expansion. To remedy this issue, a thin layer of alumina is deposited on the Kapton film prior to the deposition of any other layers. This layer is thin enough to maintain the flexibility of the substrate but strong enough to prevent the Kapton film from significantly deforming in subsequent thermal processing steps. The flexibility of the substrate is managed during processing using a carrier wafer when a stable base capable of holding the Kapton flat is not provided by the tool. This method utilizes a soft polydimethylsiloxane (PDMS) adhesive film, purchased commercially under the trade name GelPak, mounted on a silicon wafer as a temporary carrier.

The TFTs produced from this worked showed modest performance. Single transistors were demonstrated with mobilities around 20 cm^2/Vs. While this does not

match the performance of single TFTs previously demonstrated this degradation was not unexpected. As the NC films are very chemically and situationally sensitive, some depletion in performance can be expected as the structure they are being incorporated within increases in complexity.

This work also demonstrated simple ICs based on the inverter structure including digital inverters, analog inverting amplifiers, and ring oscillators. As the CdSe NC transistors fabricated are solely n-type, these TFTs utilize a unipolar, saturated load design. Due to the limitations of shadow mask patterning, these TFTs were unfortunately very large. For two TFTs, as needed to demonstrate the inverter, the total pattering area was around 1 cm^2 (Figure 1-2A). This greatly limited their performance in the frequency domain due to large intrinsic capacitances and also makes them impractical for applications. These constraints limited the TFTs to a measured 3dB bandwidth of only 900 Hz (Figure 1-2C).
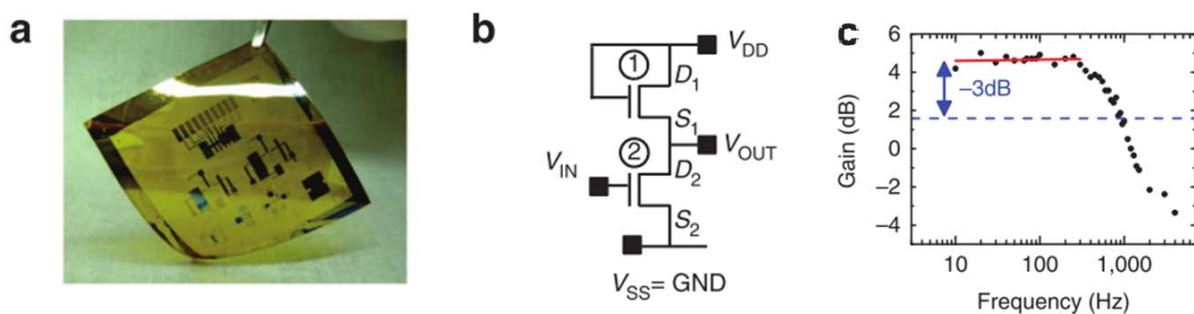
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Extending the development of the inverter, 5 stage ring oscillators were also fabricated. These TFTs were again limited by their large sizes. The measured results showed ring oscillators with 150 Hz oscillation frequencies. While the speed of these devices is limited, this work marked the first demonstrations of CdSe NC-ICs and provides much of the basic methods needed to further develop CdSe NC TFTs into faster and more complex ICs.

1-4: Air Stable CdSe NC TFTs

In order to scale down the device dimensions, a procedure must be developed which allows sub-10 µm patterning and alignment of metal electrodes. One route to fabricate TFTs on these length scales is the development of photolithographic processes. However, these processes will expose the TFTs to air and solvents not present when patterning with shadow masks. Like many solution processable semiconductors, CdSe NCs must be handled inside of a nitrogen glovebox to avoid exposure to oxygen and water which can greatly degrade their performance. This air sensitivity significantly limits their potential applications as their performance is diminished in atmosphere. The desire to mitigate these limitations led to the development of methods to make CdSe NC TFTs recoverable after exposure to air and solvents as well as being stable long-term outside of an inert atmosphere.[20]
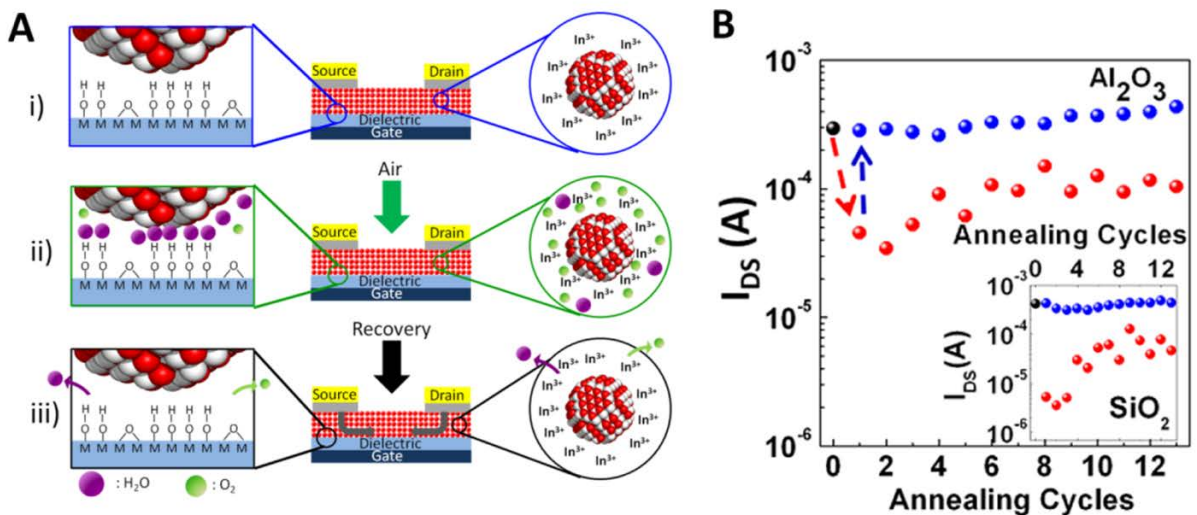
Figure 1-3 (A) Schematic representation of indium-driven CdSe recovery. (B) Plot of maximum drain current after exposure to atmosphere (red) and subsequent recovery annealing (blue). (Reproduced from Choi, J. *et al*, 2013)

The use of indium as a dopant for CdSe is widely accepted in both polycrystalline and NC TFT applications.[15,20–22,11] Given its low meting point, indium can be easily deposited by thermal evaporation and subsequently melted by annealing to drive diffusion of the material into the semiconducting film, acting an n-type dopant. As it would turn out, the annealing process also causes the desorption of oxygen from CdSe NC films (Figure 1-3A). Oxidation is the biggest cause of degradation in performance of CdSe NC films following exposure to atmosphere. Oxygen adsorbed into a CdSe NC film acts as a carrier trap, greatly reducing the number of available carriers and the conductivity of the film.[27] This causes a drastic reduction in current. Annealing the CdSe

NC films in the presence of indium causes this oxygen to be desorbed and/or gettered and provides additional indium dopant to the NC surface (Figure 1-3B).[20]
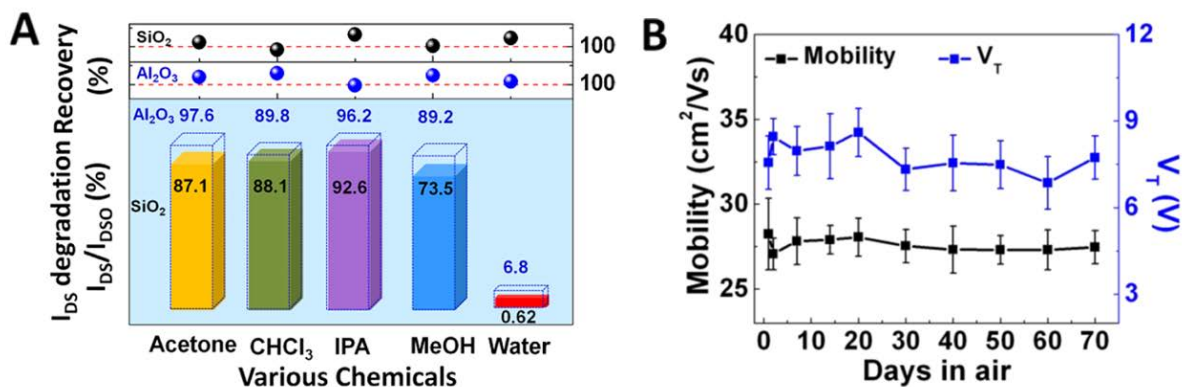
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This concept allows recovery of the TFTs from exposure to atmosphere as well as a wide variety of solvents, as shown in Figure 1-4A. This also allowed for the creation of a procedure for encapsulation the TFTs. Conformal metals and oxides are completely impermeable to gasses. As metals are conductive, this is not an option for creating the needed impermeable barrier. Therefore, an oxide was required. Using atomic layer deposition, a thin, impermeable, conformal layer of aluminum oxide can be deposited onto the CdSe NC TFTs. As it would turn out, this layer acted not only as a barrier to exposure, but also reduced the observed hysteresis of the TFTs, making them more stable for IC applications.[20]

This development opens the door for developing these materials into large-area, photolithographically patterned ICs. By being able to recover the material from chemical and atmospheric exposure, we can reverse the effects of photolithographic processing techniques, almost all of which are performed in atmosphere and utilize harsh chemicals.

1-5 : Flexible, Photopatterned CdSe Nanocrystal Integrated Circuits

In this thesis, we demonstrate photopatterned CdSe-TFT ICs. This includes the demonstration of procedures to produce low-voltage, photopatterned ICs on Kapton substrates. It is extended by the demonstration of chemical processing procedures which improve the performance of CdSe NC-TFTs. We further the evolution of CdSe NC-ICs with the development of procedures which allow for the demonstration of high-frequency NC-TFT oscillators on Kapton substrates. We extend the development of low-power, flexible substrate electronics with the demonstration of flexible electrochromic displays which can be powered with a near field communication (NFC) receiver.

The work in Chapter 2 develops and demonstrates the procedures used for fabricating photolithographically patterned CdSe-TFT ICs on Kapton substrates. These ICs include the demonstration of TFTs with motilities of 10 cm^2/Vs , high-speed inverting amplifiers with 6.7 kHz bandwidths, 5-stage ring oscillators with 65 kHz oscillating frequencies, as well as multi input logic including NAND and NOR gates. This shows the viability of fabricating CdSe NC-TFT ICs with photolithographic techniques.

Chapter 3 introduces a hybrid procedure for exchange, incorporating both a solution as well as a solid state thiocyanate ligand exchange process. This process demonstrates CdSe NC- TFTs with mobilities up to 40 cm^2/Vs on silicon with shadow mask patterns and 17 cm^2/Vs with photolithographic IC patterns on Kapton, besting the values previously reported for thiocyanate capped CdSe.

Chapter 4 develops methods by which CdSe NC-TFTs fabricated on Kapton substrates can be formed into simple cross-coupled oscillators and wirebonded directly on to a printed circuit board. These methods show the potential for CdSe-TFTs to be demonstrated and probed at MHz frequencies. This will not only demonstrate the full potential of CdSe-NC TFTs without being limited by transistor sizing, but may also provide insight into the movement of carriers in the NC film.

Chapter 5 furthers the development of low-power electronics on flexible electronics with a demonstration of flexible electrochromic displays which can be powered using an NFC link. These displays are demonstrated with large-area patterns activated and powered by a wireless NFC link available in most smartphones. This shows the potential for deploying small, low-power displays without the need for a battery.

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Chapter 2 : Flexible, High-Speed CdSe Nanocrystal Integrated Circuits

2-1 : Introduction

Solution and low-temperature processable semiconductors are being explored to realize low-cost, large-area, flexible electronics and to enable emerging mobile, wearable, and implantable devices. Applications including displays,[1,2] sensors,[3] integrated circuits (ICs),[4–8] and radio frequency identification (RFID) systems[9,10] have been demonstrated through the solution-based casting and printing of semiconducting organic molecules and polymers,[1,2,4,9,10] carbon nanotube arrays,[3,5,8] and sol-gel metal oxides.[7] Recently, colloidal nanocrystals (NCs) have emerged as a new member of this family of solution-processable semiconductors with demonstrations of high mobility (>10 cm^2/Vs) electronic transistors[11–16] and integrated circuits.[6,17]

Colloidal semiconductor NCs are typically synthesized with long-chain organic ligands on the NC surface allowing 1) the controlled growth of NC samples that are monodisperse and tunable in size and shape and 2) the dispersion of NCs in non-polar organic solvents, creating inks.[18–20] However, these long organic ligands serve as barriers to charge transport when NCs are assembled to form thin film solids. The introduction of compact ligand chemistries and processes to exchange these long ligands greatly enhances the electronic coupling between NCs in solids.[15,21,22] The combination of strong coupling through ligand exchange and of recently reported synthetic[23–25] and post-synthetic[11–15] methods to dope NC thin films are responsible for the dramatic increase of carrier mobility in colloidal NC-based thin films. Previously, our group exploited these

high mobility NC thin films in field-effect transistors to demonstrate solution-processable and flexible, low-voltage analog and digital integrated circuits (ICs).[6] However, in this first demonstration of nanocrystal integrated circuits (NCICs), the transistor wiring was defined by shadow masks which created large transistor sizes and electrode overlap and therefore introduced large parasitic capacitances that limited the bandwidth to ~900 Hz and switching speed to 600 µs for low-voltage analog and digital circuits, respectively.

In this chapter, we exploit methods we introduced for *in-situ* device repair that allows us to take these semiconducting NC materials, which are typically highly sensitive to their environment, out of the nitrogen glovebox and into the cleanroom, where they are exposed to the air and to the solvents commonly used in fabrication processes.[11] Here we use photolithography to pattern device electrodes enabling us to scale down device dimensions, drastically reducing parasitic capacitances from electrode overlap, and scale up fabrication across large 4 inch flexible Kapton substrates. We demonstrate NC field-effect transistors (NC-FETs) with channel lengths ranging from 5-40 μm and electron mobilities up to 10 cm^2/Vs. We integrate these NC-FETs using a newly developed process to fabricate vertical interconnect access (VIA) holes, which allows us to realize complex integrated circuits. These circuits include the fundamental building blocks for analog and digital circuits such as inverters and NAND and NOR gates. Taking advantage of reduced parasitic capacitances, we use these building blocks to realize amplifiers with ~7 kHz bandwidth and ring oscillators with a 7.7 μs delay per stage at a 2 V supply voltage. The delay per stage decreases with increasing supply voltage, reaching

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1.5 μs at a 5 V supply voltage. To the best of our knowledge, these NCIC ring oscillators are the fastest solution-processable, semiconductor-based ring oscillators fabricated on a flexible substrate and operating at low voltages.

2-2 : Methods

We use contact photolithographic techniques to pattern the gate, VIA holes and source/drain layers to realize flexible, wafer-scale CdSe NCICs. First, a 4 inch diameter, 50 μm thick, Kapton film is encapsulated in a 20 nm layer of alumina (Al_2O_3) grown by atomic layer deposition (ALD). This process preshrinks the Kapton and prevents the deformation of the plastic during following thermal processing steps, which can otherwise cause the delamination of subsequently deposited layers. Next, a photolithographically-defined and thermal (Al) and e-beam (Ti, Au) evaporated metal stack of Ti/Au/Ti/Al is fabricated to form gate electrodes. Aluminum, rather than gold, is required as the top layer of this stack in order to grow a stable, conformal oxide on top of the gate electrodes. The gate electrodes are oxidized by an oxygen reactive ion etching (RIE) process in order to promote further oxide growth. A 20 nm, high-k, Al_2O_3 layer is then grown by ALD on top of the RIE-oxidized gate electrodes to form a high quality, high unit capacitance (220 nF/cm^2) gate dielectric layer. Holes in the insulating Al_2O_3 layer are defined by photolithography and created by a chlorine RIE process. Chlorine etching of the Al_2O_3 layer is very aggressive and not only etches the Al_2O_3 dielectric layer, but also etches the underlying aluminum.[26] The gold layer in the stack is introduced to provide a robust etch stop and to maintain conductivity between the gate

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layer and the subsequently deposited VIA. The VIA holes are filled by e-beam evaporation of gold. The VIA is essential as it creates vertical connections between different metal electrode layers through the insulating Al_2O_3 layer, required to develop complex, IC topologies. To test VIA conductivity, we measure a test structure composed of many VIAs of identical size. The VIAs show Ohmic contact to the gate layer with a resistance of 60 ± 15 Ω for each VIA hole [Appendix 2-2]. This robust VIA process may be generally useful for devices fabricated from different solution-processable semiconductors as it desirably allows the use of Al_2O_3 as a gate dielectric layer for low-voltage, low-hysteresis flexible devices.

To fabricate the CdSe NC active layer, 4 nm CdSe NCs are prepared, following literature procedures.[27] The long-chain organic ligands introduced during synthesis are exchanged in solution with the compact ligand thiocyanate (SCN). These SCN-exchanged CdSe NCs are dispersed in dimethylformamide (DMF) at a concentration of 19.6 mg/mL, as estimated from the optical density at the first excitonic peak,[28] and deposited by spincoating to form 40 nm thin film, CdSe NC semiconducting channel layers, as previously reported.[14] Following spincasting, the CdSe NC thin films are annealed at 200 ^{o}C for 10 minutes to promote their adhesion to the substrate. To further prevent NC thin film delamination during processing, an ultrathin, 1 nm ALD Al_2O_3 layer is deposited. Source and drain electrodes composed of a metal stack of indium and gold are defined by photolithography and deposited by thermal evaporation to complete bottom-gate, top-contact NC-FETs and NCICs. The devices are annealed at 300 ^{o}C for 30

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min in order to drive indium diffusion from the source and drain electrodes through the 40 nm thickness of the CdSe NC thin film, heavily doping the contact region, and into and across the 5-40 μm long CdSe NC thin film active area, lightly doping the channel [Appendix 2-6]. In order to better control doping at the contacts and in the channel and realize high mobility and current modulation in devices as we scale down the channel length in comparison to our previous work, we deposit an additional 5 Å layer of indium by thermal evaporation across the entire NC film and then anneal the devices at 300 $^{\circ}$C for 10 min, an approach used previously to dope poly-crystalline CdSe transistors.[29] Next, devices are encapsulated in an additional 50 nm ALD Al_2O_3 layer to passivate the CdSe NC thin film surface and reduce device hysteresis.[11] Finally, the devices are annealed at 300 $^{\circ}$C for 10 min to complete the doping of the channel from the added indium as well as to repair the CdSe NC thin film after oxygen and solvent exposure during photolithographic patterning and ALD encapsulation. Detailed methods are discussed in Appendix 2-1.
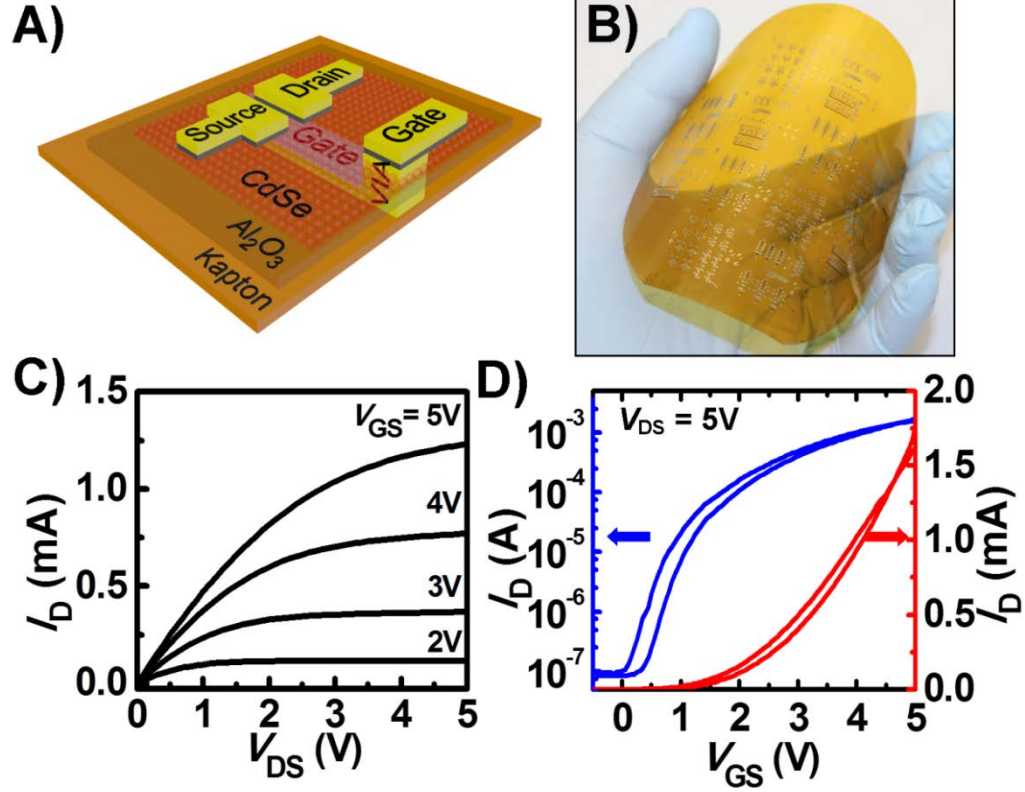
Figure 2-1 (A) Schematic of a CdSe NC-FET and a VIA used as building blocks to construct NCICs. (B) Photograph of an array of CdSe NCICs fabricated on a 4 inch, flexible, Kapton substrate. (C) Output I_D-V_{DS} and (D) transfer I_D-V_{GS} characteristics of a flexible CdSe NC-FET with photolithographically-patterned electrodes defining a channel length L= 10 μm and width W= 1000 μm.

Figure 2-1A details a schematic of a completed CdSe NC FET and a VIA defined

to realize NCICs. We successfully fabricate many individual transistors, inverters,

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voltage amplifiers, NOR and NAND gates and ring oscillators on a single 4 inch, wafer-sized, flexible Kapton substrate [Figure 2-1B]. Figure 2-1C, D shows representative NC-FET device output (I_D-V_{DS}) and transfer (I_D-V_{GS}) characteristics used as the building blocks to construct the NCICs. The NC-FETs show well-behaved, n-type characteristics at low operating voltages, seen by the linear increase and then saturation of the drain current (I_D) with increasing drain bias (V_{DS}) and the increase in drain current (I_D) with increasing gate bias (V_{GS}), as electrons are accumulated at low fields in the channel across the high unit capacitance, Al_2O_3 gate dielectric layer. Averaged over 30 measured NC-FETs with channel lengths ranging from 5 to 40 μm, in the saturation regime [Figure 2-1D] the electron field-effect mobility (μ_e) is 10.1 $\pm$ 0.28 cm^2/Vs with a threshold voltage (V_T) of 1.07 $\pm$ 0.03 V and a low hysteresis (ΔV_T) of 0.22 $\pm$ 0.02 V. In the linear regime [Appendix 2-6] μ_e is 6.2 $\pm$ 0.15 cm^2/Vs with a V_T of 0.84 $\pm$ 0.073 V and a ΔV_T of 0.32 $\pm$ 0.02 V. The drain current on/off ratio is greater than 10^4, with an average subthreshold swing of 350 $\pm$ 9 mV per decade. The calculated semiconductor-dielectric interface trap density is 7.14 $\pm$ 0.05 x 10^{12} cm^{-2}, similar to our previous reports on high-performance CdSe NC-FETs.[6,14] The metal-semiconductor contact resistance is probed using the transmission line method [Appendix 2-7] and is consistent with the formation of low-resistance, Ohmic contacts.[30]

Figure 2

A)

B)

C)

500 μm

D) Voltage transfer characteristics V_{out} (V) vs V_{IN}

5V, 4V, 3V, 2V

E) Gain (V/V)

F) V_{out} (V)

G) Current (A)

V_{IN} (V)

H)

V_{DD} = 2 V

Voltage (mV) vs Time (ms)

I)

Gain (dB)

V_{DD} = 2 V

Frequency (Hz)
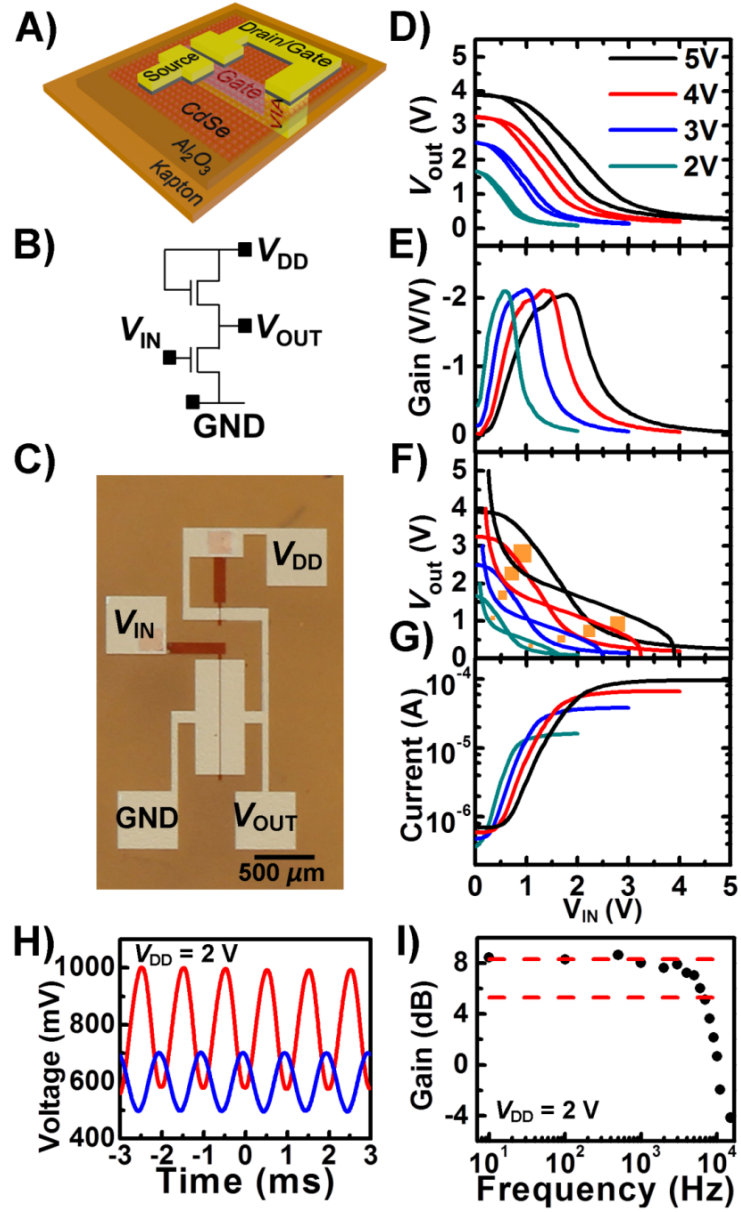
Figure 2-2 (A) Schematic of the load transistor used to construct the NCIC inverter. (B) Circuit diagram and (C) photograph of a flexible, CdSe NCIC inverter. The output voltage (V_{OUT}) is measured as a function of the input voltage (V_{IN}) for different supply voltages (V_{DD}) applied with respect to ground (GND). (D) Voltage transfer characteristics (V_{OUT}-V_{IN}), (E) voltage gain, (F) noise margin (orange squares), and (G) drain current for a CdSe NCIC inverter as a function of the supply voltage V_{DD}. (H)

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Output waveform (red) of a NCIC voltage amplifier in response to a 1 kHz, 200 mV sinusoidal input on a 600 mV DC input bias (blue). (I) Frequency response (Bode Plot) of a NCIC voltage amplifier (black circles). A linear fit (red dashed line, top) shows a 8.3 dB voltage gain at low frequency, which is used to find the 3 dB bandwidth (red dashed line, bottom).

Since our NC-FETs are n-type and have a positive V_T, we implement an enhancement-load design to form NCIC inverters. This topology uses two NC-FETs operating in unison where one FET serves as the driver and the other as the load [Figure 2-2B]. The load, shown schematically in Figure 2-2A, is built by connecting the drain and gate of the NC-FET through a VIA and operates as a two terminal, linear resistor. Figure 2-2C shows a photograph of a fabricated NCIC enhancement-load inverter.

Figure 2-2D-G show the inverter voltage transfer characteristics (VTCs), voltage gain, noise margin, and drain current for different supply voltages (V_{DD}). The circuit shows the expected VTCs, inverting a low voltage input (V_{IN}) to yield a high voltage output (V_{OUT}) and *vice versa* [Figure 2-2D]. The voltage swing in the VTCs for all supply voltages remains constant at 78 +/- 1 % of V_{DD}. This is in agreement with the ideal V_{DD}-V_T voltage swing for an enhancement-load inverter as V_T depends on the applied voltage, consistent with a gate bias dependent mobility common to amorphous semiconductor transistors.[31,32]

The voltage gain, defined as the slope of the VTCs, shows a maximum gain of -2.1 V/V for all input voltages and a wide region where the output voltage gain is greater than unity. For an enhancement-load inverter, the theoretical maximum gain is defined

as $\text{Gain} = \dfrac{g_{m_{\text{Driver}}}}{g_{m_{\text{Load}}} + g_{ds_{\text{load}}} + g_{ds_{\text{driver}}}}$. For an ideal device, the values of drain-to-source

conductance (g_{ds}) for the driver and load are several orders of magnitude smaller than the

transconductance (g_m) of the load which for this device g_m is 14.4 μS. However, g_{ds} is 1.7

μS, as seen by the residual slope in the saturation regime of the NC-FET output curves

[Figure 2-1C], and is too large to be neglected. This effectively reduces the gain, yielding

a calculated gain of 2.18 in strong agreement with our measured value [Appendix 2-3].

The noise margin is the measure of the ability of one device to switch another,

thus allowing multi-stage digital circuit operation. It is determined by calculating the

difference between the output voltage swing when the gain is greater than unity and the

input voltage swing over the same range.[33] It can be shown visually by overlaying the

inverter VTCs and its inverse at each V_{DD}, as highlighted by the orange rectangles in

Figure 2-2F. The noise margin increases from 450 mV at $V_{DD} = 2$ V to 1130 mV at $V_{DD} =$

5 V [Appendix 2-5].

The NCIC inverter gain opens the door for use of these devices in analog circuit

applications, such as voltage amplifiers. As an example, we drive an inverter with a V_{DD}

= 2 V and a V_{IN} composed of a 200 mV, 1 kHz peak-to-peak sinusoidal input

superimposed on a 600 mV DC offset [Figure 2-2H]. The DC offset is chosen to operate

the inverter at its point of maximum gain, as shown in Figure 2-2E. The output

waveform is amplified with a gain of approximately -2V/V and is offset at 780 mV,

consistent with the inverter VTCs, and it shows a 180 degree phase shift, originating from

the negative gain of the inverter. The frequency response of the voltage amplifier is measured by taking a series of these measurements at varying frequency and recording the amplitude of the input and output signals to find the voltage gain in decibels (dB). The results of these measurements are summarized in a Bode Plot in Figure 2-2I. The bandwidth, defined as the point where the gain has been reduced by 3 dB from that at low frequency, is estimated from the plot to be 6.8 kHz. Amplification remains above unity, or 0 dB, for frequencies of up to 10 kHz. Approximating the resistances and capacitances in the inverter as a single time constant network, we calculate a theoretical bandwidth of 9.8 kHz, in strong agreement with the measured result [Appendix 2-4]. This measured 3 dB bandwidth is almost 8 times larger than our previous voltage amplifiers and is primarily attributed to the smaller device features sizes realized here, which greatly reduce the parasitic capacitances from the gate to source/drain overlap from 277 pF [Ref. 6] to 36 pF.

Figure 3
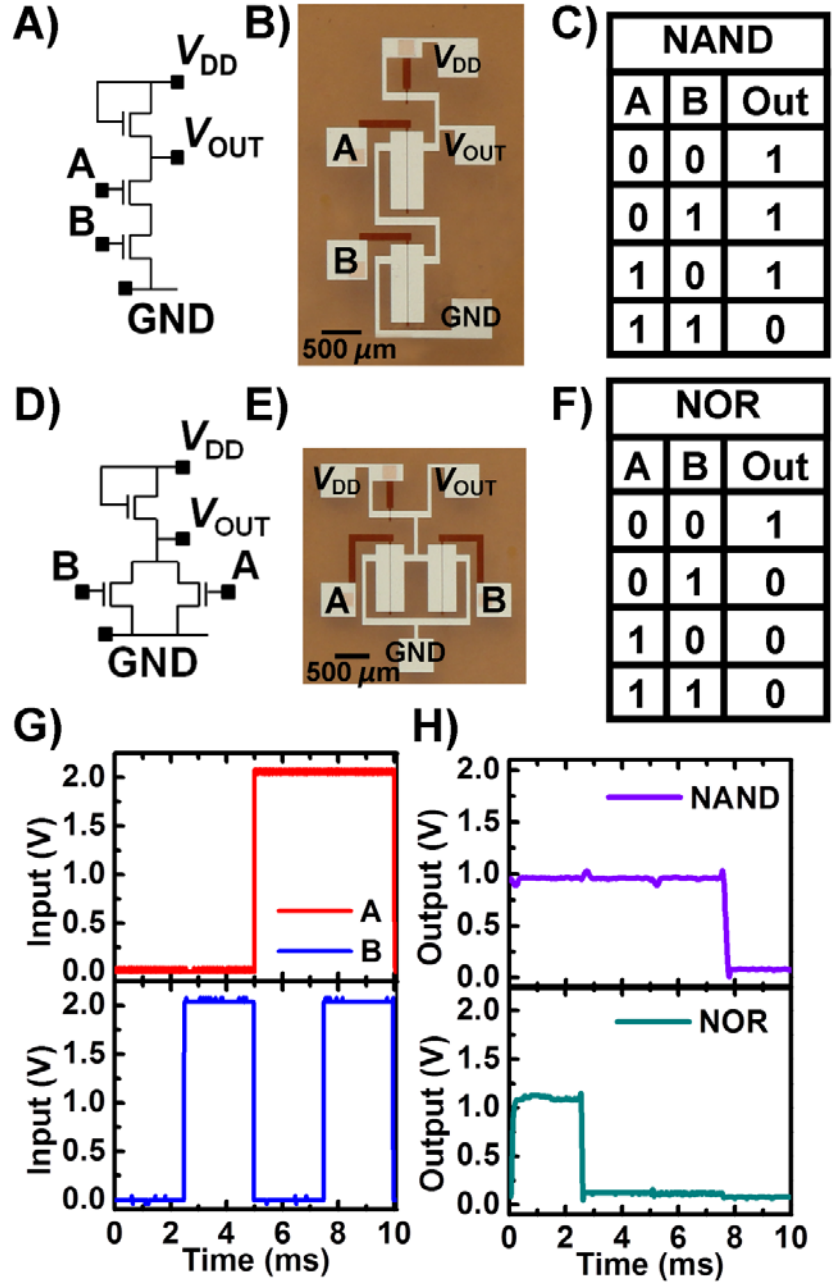
A)

B)

C)

NAND		
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

D)

E)

F)

NOR		
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

G)

H)

Figure 2-3 Circuit diagrams, photographs, and truth tables of flexible, CdSe NCIC (A, B, C) NAND and (D, E, F) NOR logic gates. (G) Waveforms for input voltages (V_{IN}) on the A (red) and B (blue) driver NC-FETs, which are switched at 100 Hz and 200 Hz,

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respectively. (H) Output waveforms (V_{OUT}) for NCIC NAND (purple) and NOR (green) logic gates with $V_{DD} = 2$ V.

Figure 2-3 shows circuit diagrams, photographs, and truth tables for flexible CdSe NCIC NAND and NOR logic gates. The logic gates are each constructed from three NC-FETs. The NAND gate uses two driver NC-FETs connected in series [Figure 2-3A]. Both NC-FETs must be on (state "1") to switch the output off (state "0"), as described by the truth table in Figure 2-3C. The NOR gate uses two driver NC-FETs in parallel [Figure 2-3D] allowing either to be switched on (state "1") to switch the output off (state "0"), as shown in the truth table Figure 2-3F. In order to test the function of these gates, we simulate the input conditions by connecting the gates of the A and B driver NC-FETs to two function generators. The function generators are setup to produce 0 to 2 V square wave voltages, switching at 100 Hz for the A NC-FET and at 200 Hz for the B NC-FET as shown in Figure 2-3G. The output waveform of each logic gate is captured on an oscilloscope and is shown in Figure 2-3H. The results are consistent with the NAND and NOR truth tables, where an output from each device close to 0 V corresponds to a "0" and an output of >1 V corresponds to a "1". The two distinct potentials at the "0" state output from the NOR gate correspond to a higher drain current achieved when both driver transistors are active. If only one driver transistor is turned on, the device current is halved, giving rise to slightly higher "0". This difference, however, is only ~50 mV which is a negligible difference for digital circuit applications as it is well below the

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noise margin. The demonstration of robust NCIC NAND and NOR gates shows promise for applications in complex digital circuitry.

Figure 2-4 (A) Circuit diagram, (B) photograph, and output characteristics at (C) 2 V and (D) 5 V supply voltages (V_{DD}) for a five-stage CdSe NCIC ring oscillator with a sixth stage buffer. (E) Delay per stage *versus* supply voltage (V_{DD}) for a CdSe NCIC ring oscillator. (F) Comparison of the delay per stage *versus* supply voltage (V_{DD}) for solution-processable, semiconducting (green) organic, (blue) carbon nanotube array, (red) sol-gel metal oxide, and (black) colloidal nanocrystal channel layers. Circuits are

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fabricated on (filled symbols) rigid substrates and (open symbols) flexible substrates. The flexible, CdSe NCICs reported here are highlighted as yellow-filled, black stars.

To further probe the switching speed of our NCICs and highlight the larger scale device uniformity, 5-stage ring oscillators are fabricated [Figure 2-4A]. A 6th stage is used as a buffer to isolate the output probe from the ring oscillators. Figure 2-4B is a photograph of a 5-stage ring oscillator built from the NCIC inverters shown in Figure 2-2. The output waveforms under V_{DD} = 2 V and 5 V are shown in Figure 2-4C,D. At V_{DD} = 2V, there is a 400 mV output swing oscillating at 13 kHz, equal to a 7.7 µs delay per stage (τ) calculated from $\tau = \frac{1}{2 \times N \times f}$, where N is the number of stages and f is the oscillation frequency. This delay per stage is two orders of magnitude smaller than the first NCIC based ring oscillator (τ = 600 µs), demonstrated at a 2 V V_{DD}.[6] At V_{DD} = 5V, there is a 1.2 V output swing oscillating at ~65 kHz, yielding a 1.5 µs delay per stage. Figure 2-4E shows the relationship between stage delay and V_{DD} between 2 V and 5 V. Faster switching speed is seen at higher V_{DD} as more current [see Figure 2-2G] passes through the devices allowing them to more quickly charge and discharge the capacitive loads.

Figure 2-4F compares the supply voltage dependent switching speed from ring oscillators constructed using our solution-deposited colloidal NCICs[6] and solution-processable organic semiconductors,[34–40] carbon nanotube arrays,[5,41,42] and sol-gel metal-oxides.[7] The primary challenge in creating a ring oscillator for all of these materials is

integrating them into IC fabrication processes. The secondary challenge is realizing devices which operate at less than 5 V, crucial for applications in portable electronics and sensors powered by batteries or inductive charging. In many other solution-processable materials, surface defects, high contact resistances, thick oxides, and large channel lengths limit their applications to higher operating voltages. The switching speed of our NCICs [Figure 2-4F (yellow-filled, black stars)] outperforms other solution-processable materials on flexible substrates at low voltages. As we have also developed processes to make NCICs compatible with conventional photolithography, NCICs can be adapted to currently available large-area fabrication equipment and techniques, boosting its development toward lost-cost, large-area electronics.

2-4 : Conclusions

In summary, we use photolithography to scale down device dimensions and reduce parasitic capacitance and scale up device fabrication to demonstrate large-area and flexible, solution-processable CdSe NCICs that operate at high bandwidth and high-speed for analog and digital electronics. We demonstrate the first NCIC NOR and NAND logic gates and report voltage amplifiers with a 6.8 kHz bandwidth at 2 V and ring oscillators with a 1.5 μs switching speed at 5 V. The higher bandwidth and higher speed of NCICs shows the promise of colloidal NCs as a materials class for large-area, flexible, high-speed circuits.

Appendix 2-1 : Detailed Methods

CdSe NC Synthesis, Ligand Exchange, and Deposition

4 nm CdSe NCs capped with trioctylphosphine oxide (TOPO) are synthesized using a modified version of methods found in Ref. 27. The selenium precursor for NC synthesis is created by combining 100 mL 97% tributylphosphine (Aldrich) and 9.9 g 99.99% selenium shot (Strem) under nitrogen and stirring them overnight to form tributylphosphine selenide. The cadmium precursor for NC synthesis, cadmium stearate, is created by combining 55 g 97% stearic acid (Acros), 10 g 99% CdO (Strem), and 50 mL 90% octadecene (Aldrich) and heating it under nitrogen to 280 ˚C. The solution is held at temperature until bubbling ceases. The reaction is allowed to cool, and then the mixture is precipitated with acetone, vortexed at high speed until sufficiently mixed to a uniform color, and centrifuged at the highest speed available in order to recover as much precursor as possible. The supernatant is discarded. The acetone precipitation, vortexing, and centrifuging process is repeated, and the supernatant is again discarded. The precipitant is then dried in a vacuum oven at 50 ˚C. Once dry, the cadmium stearate is pulverized in a mortar and pestle. The washing, vortexing, precipitation, drying, and pulverization procedure is repeated twice with methanol and then twice with acetone in order to insure the precursor is sufficiently clean.

CdSe NCs are synthesized by mixing 40 g of 90% TOPO (Aldrich), 40g of 90% octadecylamine (Acros), and 4.2 g of cadmium stearate (prepared as described above). The solution is heated to 135 ˚C and degassed under vacuum. The mixture is then heated under nitrogen to 320 ˚C. 20 mL of tributylphosphine selenide is then quickly injected to nucleate the NCs. Growth is continued at 290 ˚C for 15 min. The reaction is stopped by adding 50 mL of anhydrous toluene. The solution is transferred into a nitrogen glovebox. Anhydrous methanol is added to the solution until precipitation of the particles is observed. The mixture is then centrifuged at the highest speed available in order to recover as many NCs as possible. The supernatant is discarded. 16 mL of anhydrous hexanes are used to redisperse the precipitant. The resulting solution is then centrifuged and the supernatant is retained. The NCs are then redispersed in 16 mL anhydrous hexanes. Anhydrous ethanol is then added until precipitation of particles is observed. This mixture is vortexed until the mixture is a uniform color, and then centrifuged at the highest speed available and the supernatant is discarded. The process of redispersion in 16 mL of hexane, adding anti-solvent until precipitation is observed, vortexing,

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centrifuging, and discarding the supernatant is repeated with anhydrous acetone and anhydrous isopropanol. The final precipitant is then dispersed in 16 mL of anhydrous hexane for storage until use.

Ligand exchange with ammonium thiocyanate (NH_4SCN) is performed in an inert environment using the recipe found in Ref. 14, scaled proportionately to create a 450 μL dispersion of SCN-capped CdSe NCs in dimethylformamide (DMF) at an optical density (OD) of 40. This is performed by starting with 2.4 mL of TOPO-capped, CdSe NCs at an OD of 20 and combining it in a centrifuge tube with 3.6 mL of hexane and 3.2 mL of NH_4SCN in acetone at a concentration of 10 mg/mL. This mixture is vortexed at 3000 rpm for 2 min, centrifuged at 2000g for 1 min, and then the supernatant is discarded. 4.8 mL of tetrahydrofuran is added to the precipitated NCs and this mixture is vortexed at 3000 rpm for 2 min, centrifuged at 2000g for 1 min, and the supernatant is discarded. 4.8 mL of toluene is then added to the precipitated NCs and this mixture is vortexed for 1 min at 3000 rpm, centrifuged at 2000g for 1 min, and the supernatant is discarded. The precipitated NCs are then dispersed into 400 μL of DMF.

Thin films are deposited in an inert atmosphere by passing the resulting NC dispersion through a 1 inch diameter, 0.2 μm pore polytetrafluorethylene filter onto the substrate, then spinning the sample at 500 rpm for 15 s, ramping to 800 rpm over 15 s, and then holding at 800 rpm for an additional 30 sec.

Device Fabrication

CdSe NCICs are fabricated on 50 μm DuPont Kapton substrates. These substrates are encapsulated by 20 nm of Al_2O_3 deposited at 280°C in a Cambridge Nanotech Savannah 200 ALD system using trimethylaluminium and water precursors. Photolithographic patterns are defined in a bilayer of photoresists, MicroChem LOR3A and MicroChem S1813, deposited by spincoating at 3000 rpm for 45 s and 4000 rpm for 25 s, respectively, then baked at 180 °C for 105 s and 115 °C for 60 s, respectively. For the VIA and source/drain layer only S1813 is used. Patterns are exposed by contact photolithography using a Nanonex NX2600 system for a time of 6.3 s at 14.3 mW/cm^2. Exposed patterns are developed in Microposit MF-CD-26 for 60 s. Metal layers are deposited in a Kurt Lesker PVD75 system by thermal (Al) and e-beam (Ti, Au) methods at a deposition rate of 0.5 Å/s. For the gate metal, a stack of 2 nm Ti, 20 nm Au, 2 nm Ti, and 40 nm Al is used. MicroChem Remover PG heated to 70 °C in an ultrasonic bath is used for lift-off. The gate layer is oxidized by an Oxford 80 Plus RIE system with a 150 sccm flow of O_2 for 10 min at an RF power of 150 W. The gate dielectric layer is 20 nm

of Al_2O_3, deposited by the same ALD method described above. VIAs are defined by photolithographic methods (as above) and etched using a Trion Phantom III RIE/ICP system with a 50 sccm flow of BCl_3 gas for 35 s at an RF power of 300 W. VIAs are refilled using a stack of 2 nm Ti and 80 nm Au. CdSe NCs are exchanged as previously described and then deposited using a Specialty Coating Systems G3P spincoater installed inside of a nitrogen glovebox. The sample is heated on a Torrey Pines HP40 hotplate in an inert environment for 10 min at 200 °C to promote CdSe NC thin film adhesion. 1 nm Al_2O_3 is deposited by ALD at 150° C to protect the CdSe NC layer. The source/drain layer is defined by photolithography and consists of a stack of 40 nm In/50 nm Au, deposited at 0.5 Å/s in a custom Angstrom Engineering thermal evaporator installed inside a nitrogen glovebox. Following liftoff of the source/drain layer, the sample is heated at 300 °C in an inert atmosphere for 30 min. 5 Å of In is deposited at 0.05 Å/s by thermal evaporation in an inert atmosphere to further control the channel doping. To complete the channel doping, the sample is annealed at 300 °C for 10 min in an inert atmosphere. A 50 nm Al_2O_3 encapsulation layer is deposited by ALD at 150 °C. To complete recovery from air exposure for encapsulation, the sample is annealed at 300 °C for 10 min in an inert atmosphere.

NCIC Measurement

Devices are probed with a Suss MicroTec PM5 probe system enclosed in a nitrogen glovebox. Current and VTC measurements are performed using an Agilent 4156C semiconductor parameter analyzer. AC inverter measurements, NAND and NOR measurements, as well as ring oscillator output characteristics are collected using a Tektronix TDS 2014B oscilloscope buffered by a TI TL074CN operational amplifier chip setup on a custom printed circuit board as a unity gain buffer. Inputs for these measurements are provided by HP 33120A function generators. Unit capacitance is measured by an HP 4192A impedance analyzer.

Appendix 2-2 : VIA resistance

The VIA resistance is probed by applying 1 V across an even number of VIAs of equal size connected in a serpentine structure and measuring the current. Figure A2A shows a photograph of a 10 VIA structure and Figure A2B a schematic of a 6 VIA structure. The resistance is calculated using Ohm's Law and is shown as a function of increasing number of VIAs in Figure A2C. The resulting fit line gives us a resistance of 60 Ω per VIA and a probe contact resistance of 200 Ω.

A)

B)

C)
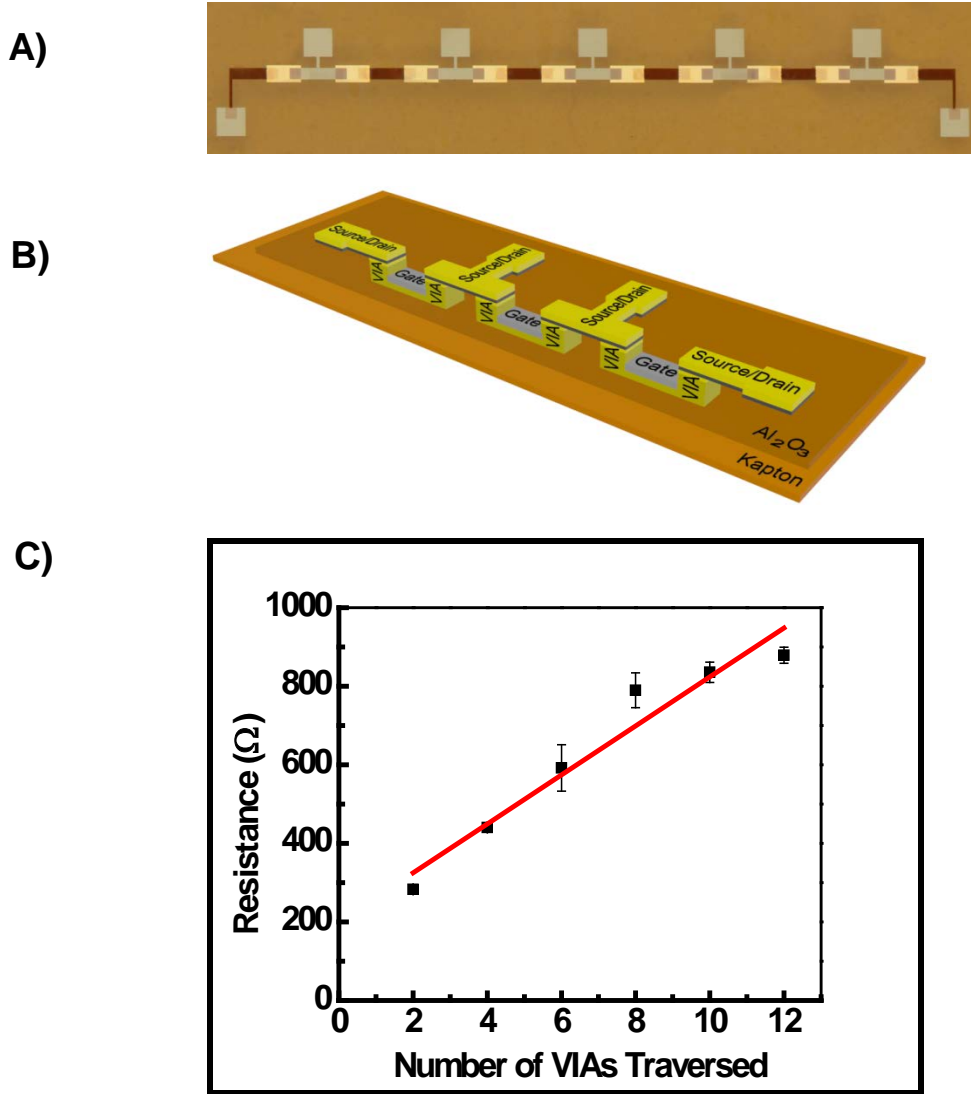
Figure A2-2 (A) Photograph of 10 fabricated VIAs and (B) schematic showing only 6 VIAs in the serpentine structure used to probe VIA resistance. (C) Plot of resistance versus number of VIAs traversed.

Appendix 2-3 : Inverter Gain

The gain for an enhancement load inverter is defined as: $\text{Gain} = \dfrac{g_{m_{Driver}}}{g_{m_{Load}} + g_{ds_{load}} + g_{ds_{driver}}}$

The parameters are defined and calculated in Appendix 2-4.

$g_{m_{load}} = 14.4 \ \mu S$

$g_{m_{driver}} = 35.2 \ \mu S$

$g_{ds_{driver}} = 1.7 \ \mu S$

$g_{ds_{load}} \sim 10^{-2} \ \mu S$

Using these parameters, we see a result of: $\text{Gain} = 2.18 \dfrac{V}{V}$

Appendix 2-4 : Single-time Constant Network Analysis of Amplifier Bandwidth

In order to determine the theoretical bandwidth, we used the approximation of a single time constant network. This defines the bandwidth as $f_{3dB} = \frac{1}{2\pi*\tau}$, where $\tau = R_{tot} * C_{tot}$. The total resistance (R_{tot}) can be approximated in this structure as the inverse of the sum of the conductance of the driver and load transistors (g_{ds}) and the transconductance (g_m) of the load transistor. The total capacitance at the node is the sum of the gate-to-source overlap capacitance of the load, the decoupled Miller drain-to-source overlap capacitance of the driver, and the cables used to connect the amplifier to the buffer and isolate the measurement from the large load capacitance of the oscilloscope. The capacitance of the cables is approximated from the capacitance per unit length of an RG-58 BNC cable (93 pF/m) and the length of two 4 ft. sections of cable required for electrical connection. We also used mobility and threshold voltage for the measured devices, which is 8 cm^2/Vs and 0.4 V, respectively. We used the same biasing conditions as described in the paper of 600 mV and 780 mV DC input and output bias, respectively.

$C_{ds_{driver}} = 22$ pF

$C_{gs_{load}} = C_{Overlap} + C_{channel} = 3.7$ pF

$Gain = 2.1$

$C_{miller_{driver}} = C_{ds_{driver}} \left(1 + \frac{1}{Gain}\right) = 32.5$ pF

$C_{node} = C_{gs_{load}} + C_{miller_{driver}} = 36.2$ pF

$C_{cables} = L_{cable} * C/L_{RG58} = 223.2$ pF

$C_{tot} = C_{node} + C_{cables} = 259.4$ pF

$g_{m_{load}} = \mu \, C_{ox} \frac{W}{L} \left(V_{gs} - V_t\right) = 14.4$ µS

$g_{ds_{driver}} = 1.7$ µS (Calculated from slope of the V_{ds} curves)

$g_{ds_{load}} \sim 10^{-2}$ µS

$R_{tot} = \dfrac{1}{g_{m_{load}} + g_{ds_{driver}} + g_{ds_{load}}} = 62.1$ kΩ

$$f_{3dB} = \frac{1}{2\pi \ R_{tot}C_{tot}} = 9.8 \text{ kHz}$$

If we perform this calculation after eliminating the cable capacitance, we see:

$$f_{3dB_{proj}} = \frac{1}{2\pi \ R_{tot}C_{node}} = 70.1 \text{ kHz}$$

Appendix 2-5 : Noise Margin

The noise margin of an inverter is defined by the difference between the output voltage range and the input voltage range when the gain is greater than 1.

$$\text{Noise Margin} = (V_{O_H} - V_{O_L}) - (V_{I_H} - V_{I_L})$$

This is illustrated for a CdSe NC inverter with a 5 V supply voltage in Figure A2-5A.
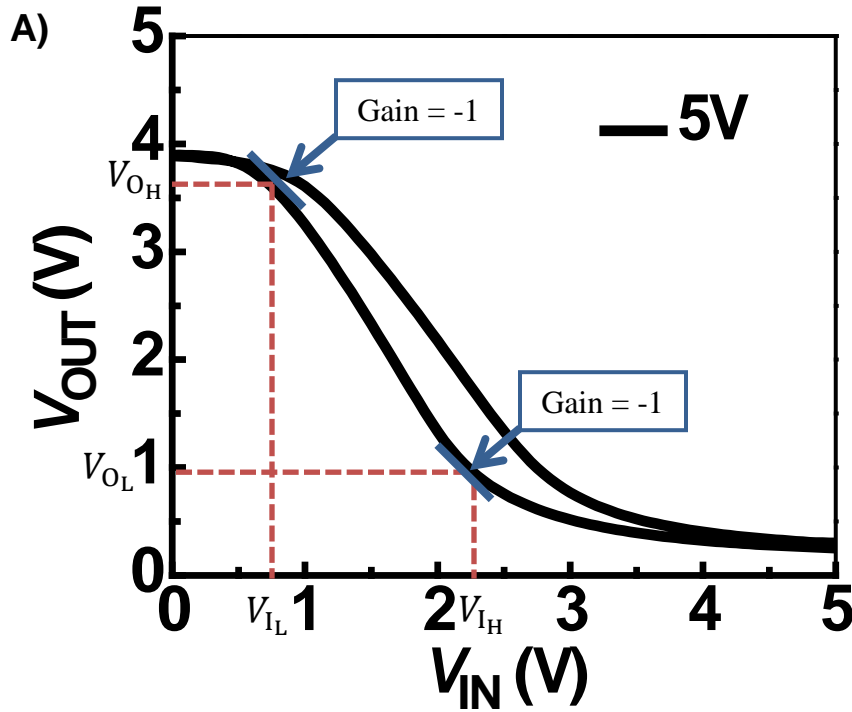
B)

Noise Margin	
2 V	450 mV
3 V	740 mV
4 V	950 mV
5 V	1130 mV

Figure A2-5 (A) Illustration of the noise margin calculation from VTCs collected with a 5V V_{DD}. (B) Table of noise margin values.

A)

B)
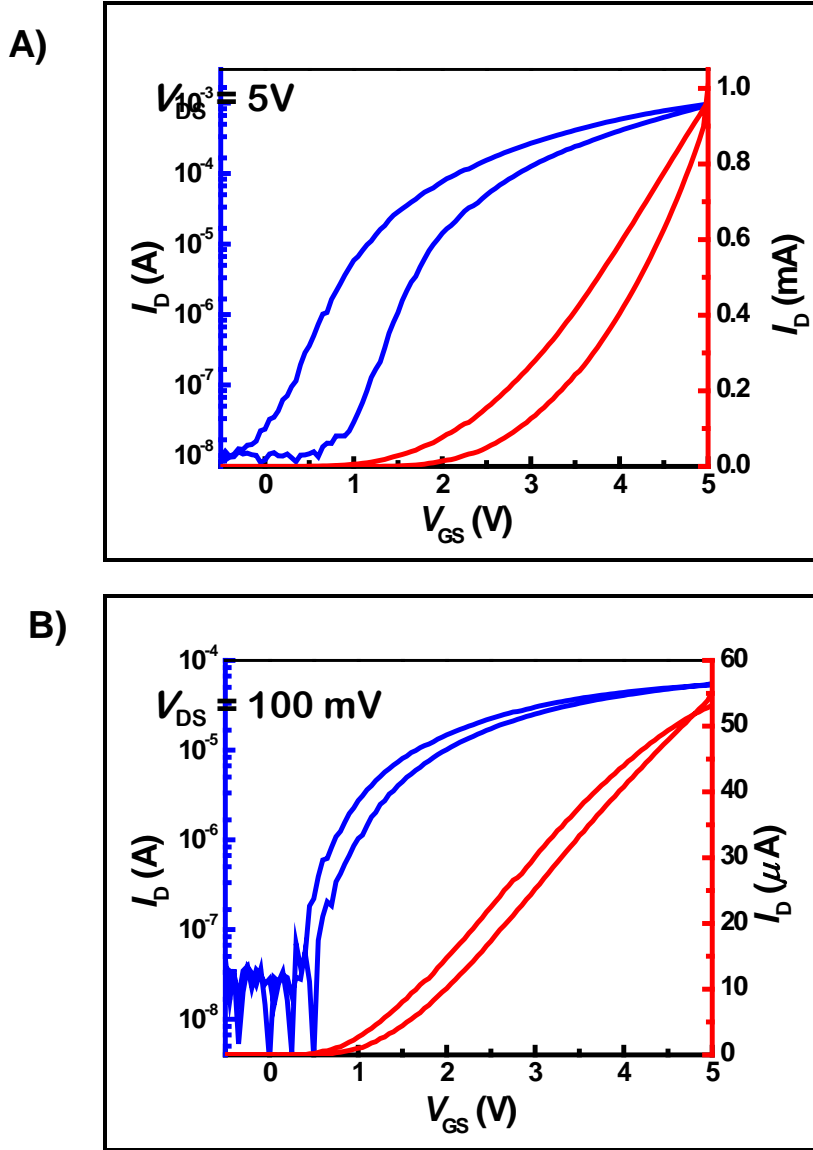
Figure A2-6 (A) Transfer (I_D-V_{GS}) characteristics of a flexible CdSe NC-FET prior to channel doping. The device has an electron field-effect mobility (μ_e) of 8.6 cm^2/Vs with a threshold voltage (V_T) of 1.9 V. (B) 3 Transfer (I_D-V_{GS}) characteristics of a flexible CdSe NC-FET in the linear regime.

Appendix 2-7 : Contact Resistance

A)
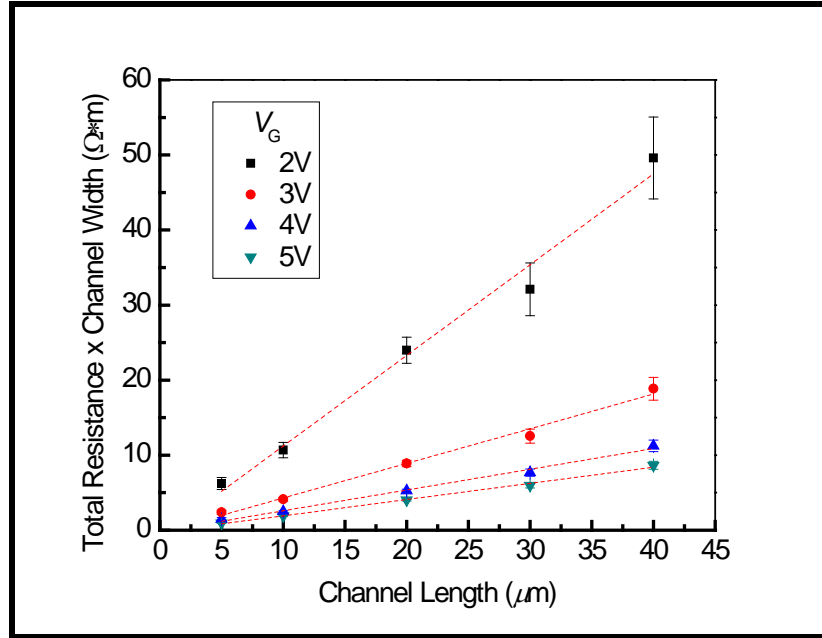
B)

Gate Voltage	Channel Resistance (Ω*m/μm)	Contact Resistance (Ω*m)
2 V	1.20764	-0.84074
3 V	0.46184	-0.33599
4 V	0.27629	-0.17863
5 V	0.21618	-0.24037

C)

Gate Voltage	Channel Resistance (Ω)	Contact Resistance (Ω)
2 V	80.5×10^3	-2.8×10^3
3 V	30.8×10^3	-1.1×10^3
4 V	18.4×10^3	-0.59×10^3
5 V	14.4×10^3	-0.80×10^3

Figure A2-7 (A) Total transistor resistance scaled by channel width *vs.* channel length used to extract the Channel Resistance (slope) and Contact Resistance (y-intercept). (C) Example resistance values are calculated for each voltage using a transistor with a channel length of 20 μm and a channel width of 300 µm.

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Chapter 3 : The Hybrid Exchange Procedure

3-1: Background and Motivation

Colloidal semiconductor nanocrystals (NC) are being developed for a wide variety of applications, including sensors,[1] displays,[2] thermoelectric cells,[3] integrated circuits (IC)[4,5], and solar cells[6,7] from a variety of materials. These NCs can be dispersed in solvent to make "inks" making them compatible with low-cost deposition techniques, like spincoating,[8–11] dip coating,[12,13] and inkjet printing.[2] When formed into solid films, the mobilities of semiconducting NC-TFTs are not currently comparable with traditional crystalline semiconductors, however their low-cost and ability to be deposited on a variety of substrates[4,14] makes them attractive for low-speed and flexible applications.

Colloidal NC semiconductor inks are typically synthesized with long chain organic ligands on their surface.[8,15–17] These ligands serve to stabilize and control the synthesis reaction in solution as well as allow them to be dispersed in non-polar solvents. However, these long ligands impede charge transport when the NCs are formed into solid semiconducting films. Therefore exchange processes have been developed for removing these long-chain surface ligands and replacing them with compact surface ligands allowing greater interparticle coupling and charge transport.[9,12,18,19]

Two different procedures have been broadly developed for the exchange of the surface ligands of colloidal NCs. The first being the solution-based exchange which replaces these ligands in solution, prior to the deposition of the material.[8,9] This is done by adding a solution of the compact ligands to the dispersion of NCs. For colloidal NC

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materials synthesized in research laboratories, the procedure needs to be tuned for each batch of material to obtain high-performance TFTs. This is believed to be due to the small batch synthesis procedure, where personal technique and timing can impact the output, as well as variability of the residual contaminants in synthesis precursors. Thus, when performing the exchange, if not enough of the compact ligand solution is added, too much of the insulating ligands remain and poor device performance is observed; if too much is added, the NCs often aggregate when redispersed in solvent for deposition. This makes the particles difficult to deposit, creating non-uniform films. For example, for the compact ligand thiocyanate, we believe thiocyanate does not replace all ligands on the NC surface, leaving less ligand on the surface after a more rigorous solution exchange. This creates more unbound surface sites on the NCs and a loss of ligands to stabilize dispersions. This effect may also be accelerated by the choice of solvent. We hypothesize that decomposition of dimethylformamide (DMF), creating formic acid,[20] may cause acid catalyzed ligand stripping, further increasing the number of open surface sites. While the NC dispersion may be optimized via iterative trials, this is a labor intensive and time consuming procedure. This limits further commercial development of these materials using this process, as a more robust procedure is needed for mass production.

The second type of exchange is a solid-state exchange, where the ligands are replaced after the NCs have been deposited into a film and the dispersing solvent has evaporated. Solid-state exchange procedures have been developed to exchange a wide array of NC compositions.[21–23] The procedure involves immersing a deposited film of

NCs with organic ligands introduced in synthesis in a bath of the compact ligand solution. This procedure is more straightforward in that solution concentration, solvent, and treatment times can be easily adjusted and the processes tend to be more robust to slight parameter changes. It also allows the NCs to be more completely stripped of the insulating ligands, compared to the solution exchange which often leaves some remnant organic ligand to prevent aggregation in solution, allowing improved interparticle coupling. The drawback to this approach is that there is significant volume loss from the removal/replacement of the long ligands. This subsequently requires that the procedure be done in a series of many thin layers in order to refill cracks and voids formed from the loss in volume. The resulting film often retains remnant defects and irregularities stemming from this process.

In this chapter we introduce the hybrid exchange; a procedure which combines both a solution-state and a solid-state exchange. With this procedure, an initial solution-exchange procedure is carried out on the NCs using a moderate amount of compact ligand solution. Alone, this would create TFTs with mediocre performance. However, the film is then further processed using a solid-state exchange procedure. This removes/replaces almost all of the remnant insulating ligands allowing greater charge transport between the NCs, as is desirable from the solid exchange. However, as much of the long, insulating ligands have already been removed in solution, the volume loss usually associated with the solid exchange is greatly reduced. This is believed to reduce the number of remnant cracks and irregularities in the film.

3-2: Methods

For this work, 4 nm TOPO-capped CdSe NCs are prepared using literature procedures[8] described in detail in Appendix 2-1 and dispersed in hexane. This material is then exchanged using a procedure similar to literature procedures for a solution thiocyanate exchange.[9] In this procedure, however, a constant recipe is used in order to standardize the procedure; previous work allowed this recipe to vary for optimization of the procedure. The standardized recipe begins with 1.8 mL of TOPO-capped CdSe NCs in a centrifuge tube diluted to an optical density (OD) of 5 in hexanes. 1.2 mL of NH_4SCN in acetone at a concentration of 10 mg/mL is added to the NC dispersion. This amount of NH_4SCN solution was chosen to be on the lower end of the range for optimized procedures which used the equivalent of approximately 1-2.5 mL of this solution for this volume of OD5 NC dispersion. The mixture is vortexed at 3000 rpm for 2 minutes, centrifuged at 2000g for 1 minute, and the supernatant is discarded. 2.5 mL of tetrahydrofuran is then added and this mixture is vortexed at 3000 rpm for 2 minutes, centrifuged at 2000g for 1 minute, and the supernatant is discarded. 2.5 mL of toluene is then added and this mixture is vortexed at 3000 rpm for 1 minute, centrifuged at 2000g for 1 minute, and the supernatant is discarded. The resulting precipitate is then dispersed in either 0.2 mL of dimethylformamide, to deposit NC films in a single layer, or 0.4 mL, to build up films from multiple layers.

The films are then deposited in an inert atmosphere glovebox by passing the dispersion through a 0.2 µm pore polytetrafluorethylene filter onto heavily doped silicon

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wafers coated with approximately 250 nm of thermally grown silicon oxide and 20 nm of aluminum oxide grown by atomic layer deposition (ALD). Before deposition, the substrates are cleaned by 150W oxygen plasma for 10 minutes as well as an *in-situ* UV-Ozone for 30 minutes. The partially, NH_4SCN-exchanged NC dispersion is then spun onto substrates at 500 rpm for 15 sec, ramped to 800 rpm over 15 sec, and then held at 800 rpm for an additional 30 seconds.

Solid-state exchange is done in a similar manner to published procedures. The samples are soaked in a bath of saturated (>200 mg/mL) NH_4SCN in acetonitrile large enough to fully submerge the sample for 1 minute followed by a 1 minute soak in pure acetonitrile to remove excess ligands from the surface. Acetonitrile was chosen after experiments showed significantly lower TFT mobilities and delamination using other solvents commonly employed for the procedure, including acetone and methanol.

For the two layer procedure, the samples are annealed following the spincoating of the first layer at 200 °C for 5 minutes in order to decompose most of the thiocyanate on the surface, as described in literature[8], making the NCs insoluble in dimethylformamide. This allows a second layer to be deposited without damaging the first layer. A second layer is then added using the same deposition and spinning procedure as the first. This is followed by an additional solid-state exchange treatment.

Following the ligand exchange, 40 nm of indium and 50 nm of gold are deposited to form source and drain contacts using an *in-situ* thermal evaporator with a pattern

defined by a shadow mask. The samples remain under nitrogen or vacuum for the duration of processing. This shadow mask pattern defines source and drain electrodes to construct TFT channels with a fixed W/L ratio of 15 and channel lengths varying from 30-200 µm. The samples are then annealed under nitrogen for 30 minutes at 300°C. TFT characterization is performed by using the heavily doped silicon substrate as a gate, making contact to the structure with a probestation mounted inside a nitrogen glovebox, and taking current measurements with an HP 4156 semiconductor parameter analyzer. Mobility is extracted by fitting the transfer characteristics using oxide parameters extracted from spectroscopic ellipsometry measurements.

For optical measurements, two samples are produced in parallel with the electrical sample; high-resistivity (1-10 Ω-cm) double-side polished silicon wafer and silica glass. These samples are taken through the same cleaning, deposition, and exchange procedures. Contacts are not deposited on these samples. Fourier transform infrared spectroscopy (FTIR) measurements are taken using the silicon wafer sample, taking an average of 256 scans from 1500-3750 cm^{-1}. UV-Visible spectrophotometry (UV-Vis) measurements are taken using the silica glass sample by taking a reverse scan from 850-400 nm.

3-3: Results

The initial development of these TFTs used a single layer procedure. In order to gain insight into the surface chemistry of the exchanged particles during the process, we used FTIR measurements. The curves (Figure 3-1A) show two peaks corresponding to

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the characteristic stretching of the carbon-nitrogen bond and the carbon-hydrogen bond. The former gives insight into the amount of thiocyanate introduced to the surface of the NCs, the latter gives insight into the amount of organic ligands remaining on the surface. Using the vibrational fingerprints to report on NC surface chemistry, it can be inferred that the additional thiocyanate treatment almost completely strips the remnant long insulating ligands from the surface of the NCs, as a control sample treated in pure acetonitrile without thiocyanate yielded no discernable change in peak level. Removal of long ligands is consistent with reducing the interparticle spacing and increases coupling between the NCs enabling greater transport.[9] This procedure yields TFTs with electron mobilities exceeding 30 cm^2/Vs with no optimization. These TFTs showed the viability of the procedure as it demonstrates similar electron mobilities as those found from an optimized solution exchange.[9,14] A comparison of the performance of these TFTs is shown in Figure 3-1A. However, these films tended to be relatively thick (~40 nm). Due to the volume loss incurred during the solid-state exchange procedure, these films would frequently form cracks and even partially or completely delaminate during processing.
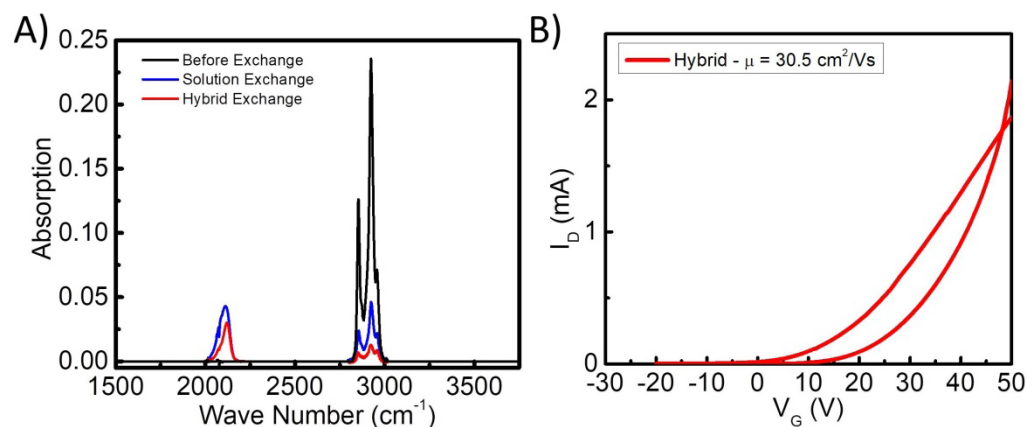
Figure 3-1 (A) Comparison of FTIR measurements of NC films formed from as-synthesized particles as well as following solution and hybrid exchange. (B) Transfer characteristics (I_D-V_{GS}) of hybrid exchanged CdSe NC-TFT with channel length L=50 µm and channel width W=750 µm.

This delamination issue is common for thick films using the solid-state exchange procedure. One hypothesis is that delamination may be due to the aggressive exchange of the top layers by the saturated solution causing contraction at the upper surface of the film, pulling lower layers away from the substrate before they can be exchanged while still adhered to the surface. This hypothesis could be tested by using a lower concentration solution for solid-state exchange and longer exchange times, however during this work fabricating TFTs with lower concentration solutions resulted in lower mobilities. Thus, a multi-step procedure is developed to remedy this issue. This procedure utilizes multiple, thinner layers, providing additional layers which can refill any cracks or voids that can formed during the first solid-state exchange treatment, while doing so with a much smaller volume loss than a complete solid-state procedure. This is

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evident from the fact that integration of integration of peaks in the single-layer FTIR measurements show a decrease in organic ligand of 75% (reduction from 11.7 to 2.9) during the solution exchange and a 93% decrease overall (reduction from 11.7 to 0.87) following the hybrid exchange. Even though there is thiocyanate added, it is much shorter than the original TOPO ligands, allowing the particles to be more closely packed. In the case of a solid-state exchange, this ligand replacement will happen in one step, leading to a much greater volume loss, making the film more prone to larger cracks and voids. A photograph showing the step-by-step addition to construct multiple layer films is shown in Figure 3-2A. This procedure showed a marked improvement over a single layer process in terms of eliminating the issue of delamination. However, beginning with the third layer of CdSe NCs, the mobility began to decrease, as shown in Figure 3-2B. This is partially due to increased off-current resulting from the larger cross section of the film, but the on-currents also decreased. It is believed that this may be an effect of doping as an increase in film thickness can decrease the relative amount of indium available to dope the film. Thus, it was determined that a procedure with only two steps would be optimal. With some procedural optimization, including reducing soak times from two minutes to one minute and increasing the inter-layer annealing temperature from 150°C to 200°C as well as following literature procedures for device encapsulation, mobilities of two layer TFTs reached 41 ± 3 cm^2/Vs, as shown in Figure 3-2C, besting the highest mobility previously reported for CdSe NC transistors exchanged with thiocyanate ligands.
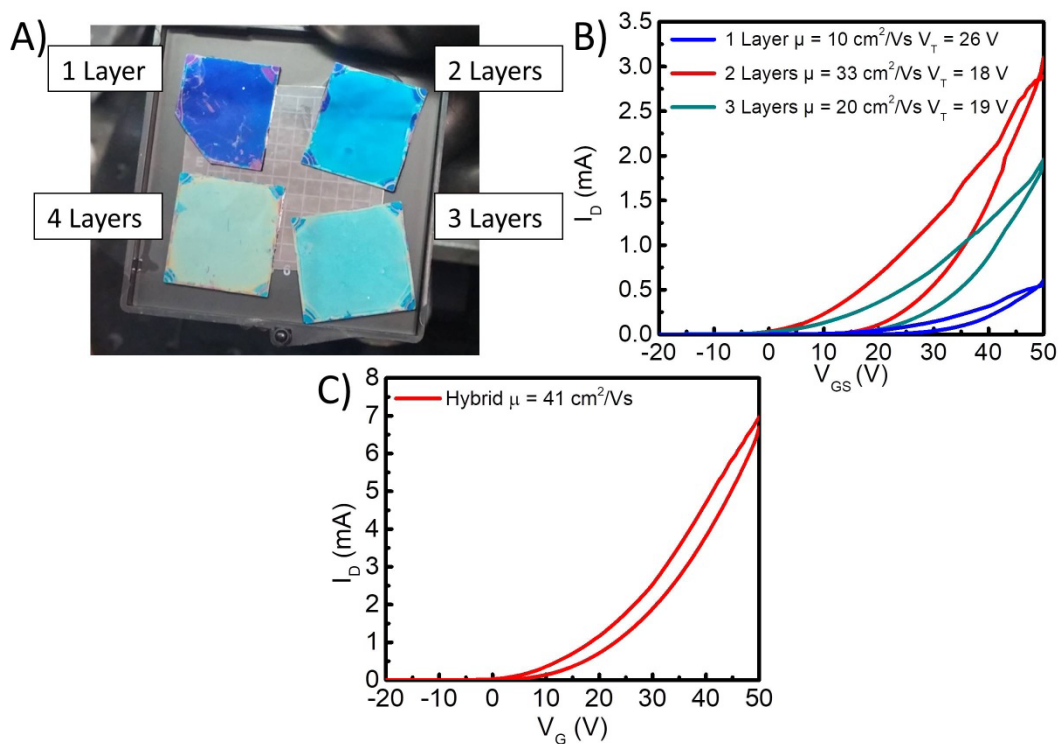
Figure 3-2 (A) Photograph of a step-by-step addition of layers of a hybrid exchanged CdSe NC film deposited on SiO_2 coated silicon wafer. (B) Comparison of transfer characteristics (I_D-V_{GS}) of multiple layers of hybrid exchanged CdSe NC-TFTs with channel length L=50 µm and channel width W=750 µm. The 4 layer result is omitted due to the lack of current modulation. (C) Transfer characteristic of optimized 2-layer hybrid device.

Further characterization of the two layer TFTs is performed in an attempt to understand the origin of improved device performance. UV-Vis and FTIR measurements are collected for each step of a two layer process and is shown in Figure 3-3. The peak broadening and red-shift in the UV-Vis plots shown in Figure 3-3A is consistent with increased interparticle coupling.[8] While this loss of quantum confinement is undesirable

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for optoelectronic applications, it is believed to be advantageous for transistor performance. As the NCs move closer together, the wave functions of the individual NCs become more greatly coupled, allowing the electrons to move more freely and improve transport.

Further characterization by FTIR gives insight into the surface chemistry. The curves (Figure 3-3B) show that after each subsequent deposition of solution-exchanged CdSe NCs, two strong peaks associated with thiocyanate and the organic ligands emerge. The organic ligand stretching peak is greatly depleted by each solid-state exchange treatment, decreasing the integrated area of the peak by ~70% during each treatment, consistent with prior reports,[8,21] suggesting significant removal of the organic ligand. There is some reduction of the thiocyanate during the hybrid exchange, as well. We believe that this is due to the high solubility of thiocyanate in acetonitrile which may be causing the loss of thiocyanate from the surface. The thiocyanate peak is further reduced upon 200°C annealing, as expected, since annealing will decompose the thiocyanate to sulfur eliminating the bond that this measurement can detect, as shown by Fafarman *et al.*[8]
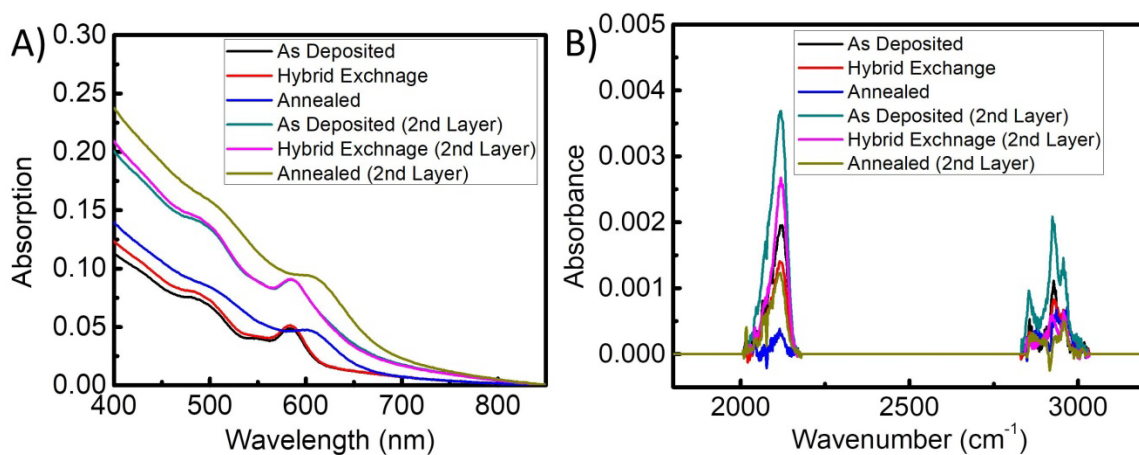
Figure 3-3 (A) UV-Vis and (B) FTIR measurements comparing each step in the process of depositing 2 layers of hybrid exchanged CdSe NCs.

This procedure proved to be able to make high performance TFTs from a new batch without additional optimization, as compared to solution exchange alone. Figure 3-4A shows mobility results from solution-exchanged NC TFTs during an optimization procedure. This procedure is time consuming and the best mobility achieved is around 25 cm^2/Vs. Figure 3-4B shows mobility results from hybrid-exchanged NC TFTs without any batch optimization thus demonstrating the robust nature of this procedure.
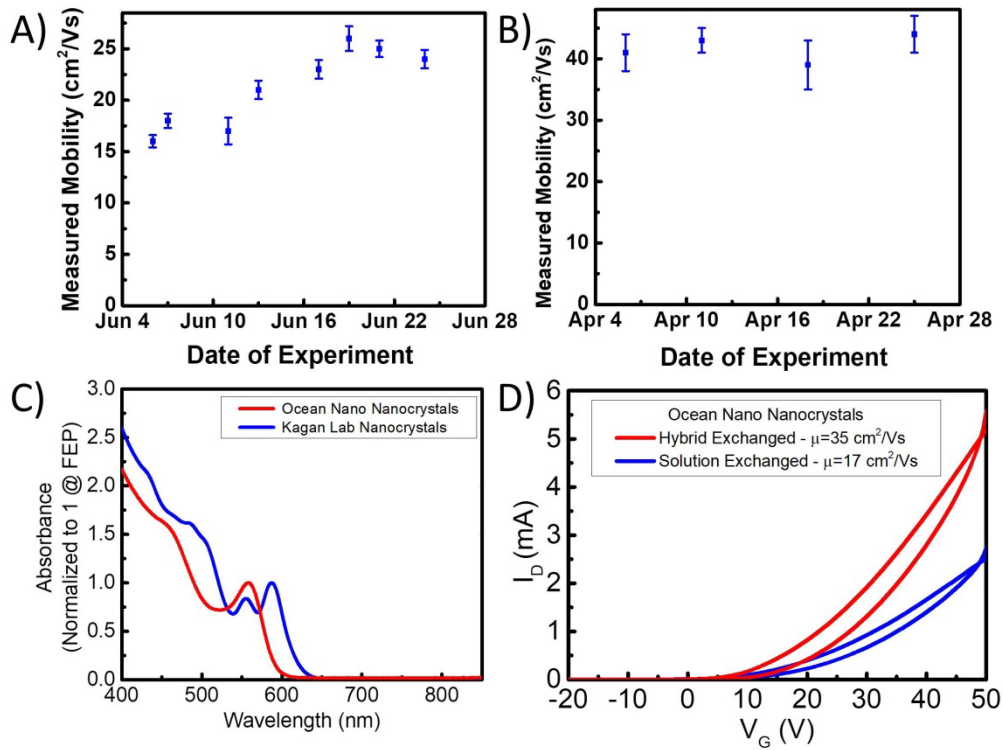
Figure 3-4 Average mobility as calculated from a fit of the transfer characteristics over time for (A) solution and (B) hybrid exchnaged NC TFTs. Each data point represents two CdSe thin films on silicon with Al_2O_3/SiO_2 dielectric stack ,measuring 6-8 TFTs measured on each, depending on yield. (C) Comparison of UV-Vis measurments of CdSe NCs made in the Kagan Lab and by Ocean Nanotechnology. (D) Comparison of transfer characteristics (I_D-V_{GS}) of hybrid and solution exchanged CdSe NC-TFTs made from Ocean Nanotechnology NCs with channel length L=50 µm and channel width W=750 µm.

As an extension to show the robustness and flexibility of this procedure, commercial CdSe NCs are purchased from Ocean Nanotech. This removes the control over synthesis that could be relied upon when the NCs are made in the labs at Penn. These commercial NCs are TOPO-capped with a specified first excitation peak (FEP) of

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around 580 nm. When received, the FEP is measured to be 567 nm, which is similar, but notably smaller than those made by the Kagan Lab, as shown in Figure 3-4C. After some optimization, TFTs fabricated from solution exchanged NCs only had a mobility of 17 cm^2/Vs. Without any batch-specific process optimization, the first TFTs fabricated with a hybrid exchanged NC film had a mobility of up to 34 cm^2/Vs. (Figure 3-4D)

These TFTs are also demonstrated using the photolithographic device fabrication procedures from Chapter 2 on Kapton substrates, as shown in Figure 3-5A. TFTs are produced with mobilities of 16±1 cm^2/Vs and threshold voltages of 1.1±0.1 V averaged across 12 TFTs. A representative device is shown in Figure 3-5B. While this does not match the performance of the TFTs produced with shadow mask patterning on silicon or Kapton, this result is not surprising. Using previous solution only exchange procedures, the photolithographically patterned circuits from Chapter 2 were demonstrated with mobilities of only 10 cm^2/Vs, well below the best demonstrated values on silicon of 30 cm^2/Vs. This reduction is believed to be an effect of the extensive chemical exposure during the photolithographic processes. While it has been shown that indium doping and annealing can be used to recover the NC film from chemical and air exposure,[14] that work did not account for exposure to alkaline developers as well as aggressive physical agitation during sonication.
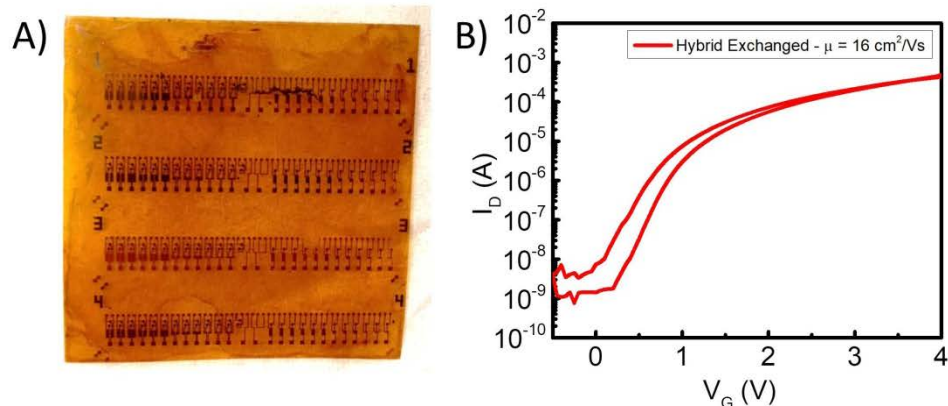
Figure 3-5 (A) Photograph of sample with hybrid exchanged CdSe NC-TFTs with photopatterned electrodes. (B) Transfer characteristics (I_D-V_{GS}) of hybrid exchanged NC-TFT with photopatterned electrodes with channel length L=40 µm and channel width W=1000 µm.

3-4: Conclusions

We demonstrate a hybrid method for ligand exchange of CdSe NCs for thin-film transistor applications. This method combines the solution and solid-state exchange procedures and demonstrates the best mobility for CdSe NC transistors capped with thiocyanate ligands. Infrared spectroscopy measurements confirm the removal of long chain organic ligands used in synthesis. Spectrophotometry measurements confirm the desired reduced interparticle spacing and increased coupling of the NCs following exchange and annealing. Further device measurements show the flexibility of this procedure to be used with commercially produced NCs as well as within procedures for fabricating integrated circuits. While this procedure focuses on CdSe NCs, other NC chemistries use similar procedures as those developed for CdSe NCs. The demonstration

of a process to combine these two procedures and take advantage of the benefits of each

makes this a valuable procedure for the continued development of NC TFTs.

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4-1: Introduction

Semiconductor devices which can operate at higher frequencies are applicable in a wide variety of fields including audio amplification, radio frequency communication, data transmission, computation, and analog signal processing. These applications are typically filled with traditional crystalline semiconductors, like silicon, germanium, and gallium arsenide. However, these traditional crystalline semiconductors are limited in their application as they are rigid and brittle and therefore cannot be used in applications where flexibility is required. Therefore, a new class of low-cost, solution-processable semiconducting materials is being developed as an option for modular deposition onto flexible substrates.[1–9]

Within this class of solution-processable semiconducting materials, semiconductor nanocrystals (NC) are emerging as a viable option.[10–17] NCs can be easily synthesized with controllable size and surface chemistries from several different materials.[18–20] However, the surface of as-synthesized particles is typically terminated with long-chain organic ligands. These ligands impede charge transport and hinder semiconducting performance of solid films. Therefore, ligand exchange procedures have been developed to remove these long-chain ligands and replace them with short ligands,[14,15,21–23] allowing greater interparticle coupling and charge transport.

CdSe NCs exchanged with thiocyanate ligands has emerged as a viable semiconductor NC ink for high performance thin film transistor (TFT) applications. Prior

work from our group showed a thiocyanate solution-exchange procedure, demonstrating TFTs with mobilities up to 30 cm^2/Vs.[11,14] A hybrid exchange procedure, presented in Chapter 3, improved this mobility up to 40 cm^2/Vs. This performance is comparable to many other solution processable semiconductors including MoSe$_2$ (50 cm^2/Vs[24]), carbon nanotube arrays (35 cm^2/Vs[5]), sol-gel metal oxides (14 cm^2/Vs[6]) and sol-gel InZnO and InGaZnO (30 and 20 cm^2/Vs, respectively[25]).

High-mobility, solution-exchanged, CdSe NC thin films are coupled with the development of photopatterning procedures in Chapter 2 to create high-speed CdSe NC-ICs. This work demonstrated the possibility for the use of NC-TFTs in high-frequency applications, including amplifiers and oscillators which could operate at 6.8 kHz and 65 kHz, respectively. However, the frequencies measured in Chapter 2 are greatly limited by the geometric capacitances of the devices themselves as well as the probing methods used for measurement. The geometric capacitances are the direct result of the practical limits of the contact photolithographic methods used for fabrication; the measurement method is limited by contact probing techniques, which have large intrinsic capacitances which create a significant capacitive load on the circuit.
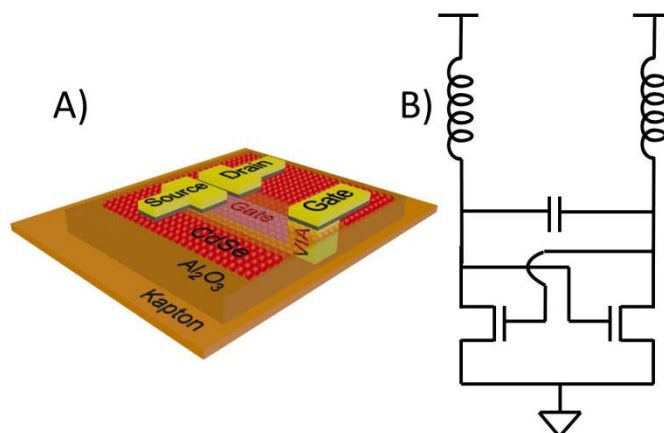
Figure 4-1 (A) Schematic of a CdSe NC-TFT. (B) Circuit diagram of simple oscillator structure.

In this chapter, we demonstrate the methods required to create simple, tunable, two-device cross-coupled oscillators (Figure 4-1) in order to fully characterize the high-frequency capabilities of CdSe NC-ICs and probe the fundamental transport of carriers within the film. This work focuses on developing an oscillator structure on a Kapton substrate that is able to be wirebonded directly to a printed circuit board (PCB), drastically reducing the loading effects of the probes and interconnecting cables. The structure also integrates external inductive elements which allow us to compensate for the geometric capacitances and increase the frequency of oscillation. The results of such a project would show the true performance of colloidal NC materials in devices, while reducing the loading effects of measurement and compensating for the geometric capacitances.

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In contrast to the prior work where oscillation is limited purely by device performance and geometric capacitances, the oscillation frequency of the cross-coupled oscillator structure developed in this chapter has multiple components. The oscillation frequency can be approximated as $f = \frac{1}{\sqrt{L \cdot C}}$, where L is the discrete inductor attached externally to the oscillator and C is a fixed value determined by a combination of the geometric capacitances of the TFTs and the coupling capacitance shown in Figure 4-1A. By reducing the value of the external inductors, the oscillation frequency can be increased and a limit can be found where the TFTs can no longer drive the oscillation. This point would represent a more accurate high-frequency limit of the NC TFTs which would not only demonstrate the potential abilities of NC TFTs, but may also give us some insight into the fundamental transport of carriers in the NC film.

We believe this frequency limit represents the dielectric relaxation frequency of the NC film. This frequency is defined as $f_d = \frac{\sigma}{\varepsilon_r \varepsilon_0}$ where σ is the conductivity of the semiconducting film, ε_r is the relative dielectric constant of the film, and ε_0 is the permittivity of free space. This can be approximated theoretically using known parameters. The high-frequency (>1 MHz) relative dielectric constant, as measured in a similar system by Suresh[26], is estimated to be 20 and the conductivity of an un-gated film is estimated from TFT measurements to be 45μS. Using these values, we estimate the cut-off frequency to be 25 MHz, well above previous values for NC oscillators. If this value can be determined within this topology, this measurement would provide a valuable

figure of merit for semiconductor NCs as well as a variety of unconventional semiconducting materials.

While the fabrication of the CdSe NC-TFT ICs is similar to Chapter 2 and Ref. 10, a few new procedures are used to fabricate these oscillators. First, the hybrid ligand exchange procedure developed in Chapter 3 is utilized. This procedure offers improved device performance as compared to the solution exchange, as is used in Chapter 2. Second, the contact structure needs to be updated to accommodate wirebonding. The wirebonding process requires the device contacts to be more robust than those previously used for direct probing. Finally, the metal layering procedures need to be updated in order to bring them in-line with modern semiconductor manufacturing techniques by insetting metal layers into layers of oxide of equal thickness, creating a smooth surface for each layer; the work in Chapter 2 simply added layers under the assumption that they are thin enough as compared to the horizontal dimensions to ignore the roughness. This updated procedure allows us to build devices with higher breakdown voltages.

4-2: Methods

To fabricate NC-TFT oscillators (Figure 4-1B), 2.5 inch square, 50 µm thick Kapton films are encapsulated in a 100 nm thick layer of Al_2O_3 deposited by atomic layer deposition (ALD) at 300ºC. This process acts to fix the size of the Kapton at the maximum thermal processing temperature to prevent further deformation which can cause delamination of subsequently deposited films. This layer is thicker than that used

previously in Chapter 2 and Ref. 10 in order to provide a media which can be etched to inset the gate electrodes.
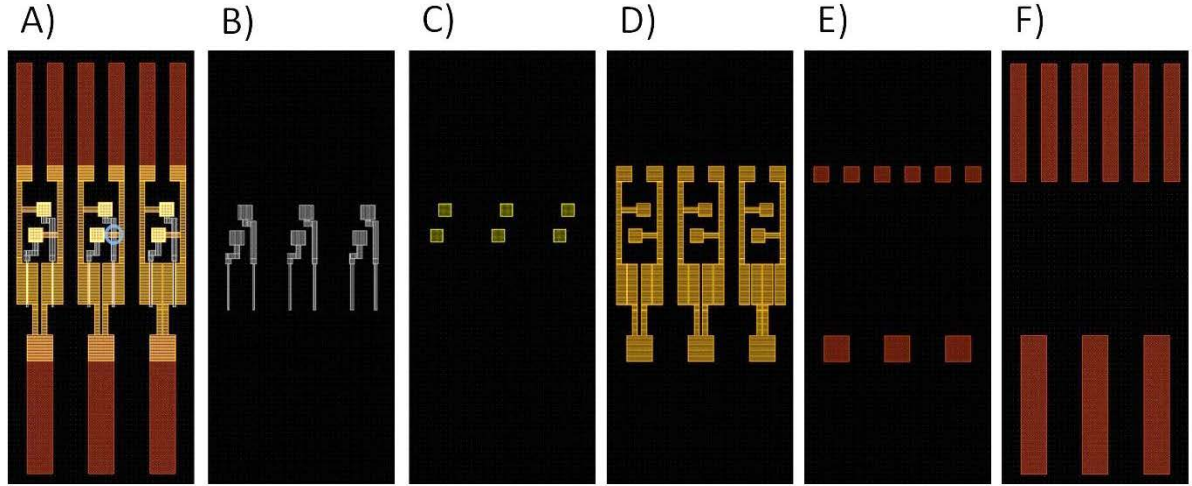
Figure 4-2 A small section of the photomask designs for NC oscillators with TFT channel width W=800 µm and channel length L=10, 20, 40 µm including (A) all layers overlaid, (B) the gate, (C) VIA, (D) source and drain electrodes, (E) contact pad wirebonding electrodes, and (F) extended wirebonding electrode patterns, respectively. The source of the overlap capacitance is indicated in the overlaid image by the blue circle, resulting from an overlap of the gate and source and drain electrode layers.

Next, a pattern for gate electrodes (Figure 4-2B) is defined by photolithography using positive photoresist and contact photolithographic methods. Each photolithographic patterning step in this procedure utilizes a 1.3 µm layer of S1813 photo resist and is exposed using a Suss MA6 mask alignment system with a 200 mJ/cm^2 exposure. This pattern is used in conjunction with a chlorine inductively coupled plasma (ICP) reactive ion etching (RIE) process (RF: 40 W, ICP: 400 W, BCl$_3$: 50 sccm, Pressure: 6 mTorr) for

90 seconds in order to form 55 nm deep trenches to inset the gate electrodes. The gate electrodes are then deposited in the defined trenches as a stack of thermally deposited aluminum and e-beam deposited titanium and gold in a 2nm/15nm/2nm/40nm stack of Ti/Au/Ti/Al, respectively. Aluminum is used at the top of the electrode stack in order to promote high quality Al_2O_3 growth on top of the electrodes for the gate oxide. Gold is used as a bottom layer to act as an etch stop during subsequent etch processes.

The resulting patterned, inset electrodes are then cleaned and oxidized by an oxygen RIE process (RF: 150 W, O_2: 100 sccm, Pressure: 15 mTorr) for 10 minutes in order to ensure complete removal of resist products and promote further oxide growth. 20 nm Al_2O_3 is then deposited by ALD at 300°C to form the gate oxide. Vertical interconnect access (VIA) holes through the insulating Al_2O_3 layer are then defined by photolithography (Figure 4-2C) and etched with a chlorine ICP RIE process, using the same conditions as above, for 50 seconds. The VIA holes are then refilled with an e-beam deposited stack of Ti/Au with thicknesses 2nm/80nm, respectively.

Next, a pattern for wirebonding electrodes is defined by photolithography (Figure 4-2F) and filled with a stack of e-beam deposited Ti and Au with thicknesses 100 nm and 600 nm, respectively. This thickness is required to form thick, robust contacts for wirebonding. This thick evaporation procedure is required as the gate oxide is etched by the gold electroplating solution which is normally used to build-up wirebonded contacts.

The CdSe NC semiconducting layer, consisting of 4 nm CdSe NCs synthesized following literature procedures[23], is then deposited and exchanged using a two-layer hybrid exchange procedure, combining both solution and solid state exchange steps, as outlined in Chapter 3. This process removes long chain ligands introduced during synthesis and replaces them with the compact ligand thiocyanate (SCN). Following this procedure, the films are annealed at 200ºC for 10 minutes to promote adhesion to the substrate. To further protect the CdSe NC film and prevent its delamination during subsequent processing, a 1 nm Al_2O_3 layer is deposited by ALD at 150ºC.

Next, photolithographically patterned source and drain electrodes (Figure 4-2D) are added on top of this structure. They are formed by a stack of thermally deposited indium and gold in a 40nm/50nm stack, respectively. Further channel doping, as needed in photopatterned circuits outlined in Chapter 2, is not needed for CdSe NC films deposited using the hybrid exchange procedure as it is observed to raise off-currents without increasing mobility. The devices are then annealed for 30 minutes at 300ºC and initial electrical testing is performed to verify high-performing devices. The devices are then encapsulated in 100 nm Al_2O_3 deposited by ALD at 200ºC in order to encapsulate the thin film surface, reduce hysteresis, and make the device stable in air.[11] During this encapsulation procedure, the wirebonding contacts are masked with adhesive Kapton tape to prevent oxide deposition onto the contacts. The devices are then annealed again at 300ºC for 30 minutes to repair the NC film from air and chemical exposure resulting

from the encapsulation procedure. Finally, the devices are mounted to the PCB using Kapton tape and wirebonded using gold bonding wire.

4-3: Discussion and Results

The oscillators are built from previously studied CdSe NC-TFTs, shown schematically in Figure 4-1A, using similar procedures as those used to develop the CdSe NC-ICs. However, modifications to this procedure are required to accommodate the operating voltages of the oscillators as well as wirebonding. The oscillator is formed using a simple structure of two cross coupled CdSe NC-TFTs, as shown in Figure 4-1B. The inductors in the circuit are discrete devices added externally and the coupling capacitor is an overlap capacitance between the gate and source/drain layers intrinsic in the final mask design (Figure 4-2A).

SPICE simulations of this system are performed using a custom first-order model of the CdSe NC-TFT with parameters extracted from device measurements and ideal discrete SPICE components (Appendix 4-1). The results of this simulation show that devices may need to operate at voltages up to 8V, as shown in Figure 4-3, with an input voltage of only 3V. The results also show the potential for 5-50MHz frequency oscillations, tunable by adjusting the external discrete inductors from 10µH to 100nH. Given the estimated dielectric relaxation frequency cut-off of 25 MHz, probing in this range will allow us to test these devices against our theoretical prediction.
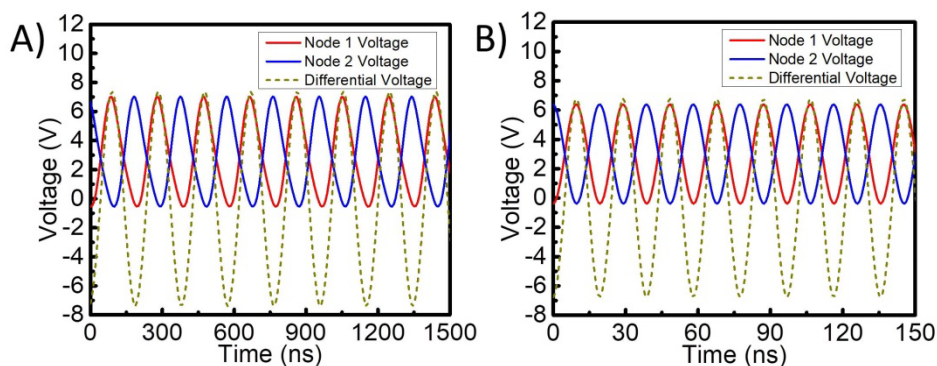
Figure 4-3 Output of simulation of oscillator circuit using (A) 10 µH (~5 MHz) and (B) 100 nH (~50 MHz) external inductors.

Prior IC development outlined in Chapter 2 studied these transistors at voltages up to 5V, but did not explore higher voltage operation. When higher voltages are applied in a scan starting at 6V to devices fabricated using those methods, breakdown is observed, as shown in Figure 4-4C. This is troubling given that breakdown of a 20 nm Al_2O_3 ALD film should be approximately 10-12V, depending on the quality of the film. It is believed that this limited operational window may be due to the method in which the IC structure is formed. Prior work simply built the layers on top of each other without much regard for the smoothness of the structure, shown schematically in Figure 4-4A. This method worked for the fabrication as the Al_2O_3 layer is conformal and was able to mold itself to the structure. However, this likely leads to parts of the oxide under the contacts being thinner than expected, giving rise to a lower breakdown potential than expected. This issue is resolved by etching a trench into the encapsulation oxide and in-setting the gate metal into this trench, shown schematically in Figure 4-4B. Embedding the gate electrode

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in underlying oxide created transistors which operate without breakdown up to 12V, as shown in Figure 4-4D. There is a drastic increase in off-current observed at source-drain voltages exceeding 10V, but this is believed to be due to nonlinear effects in the CdSe NC semiconducting film and not a result of the breakdown as the change was reversible.
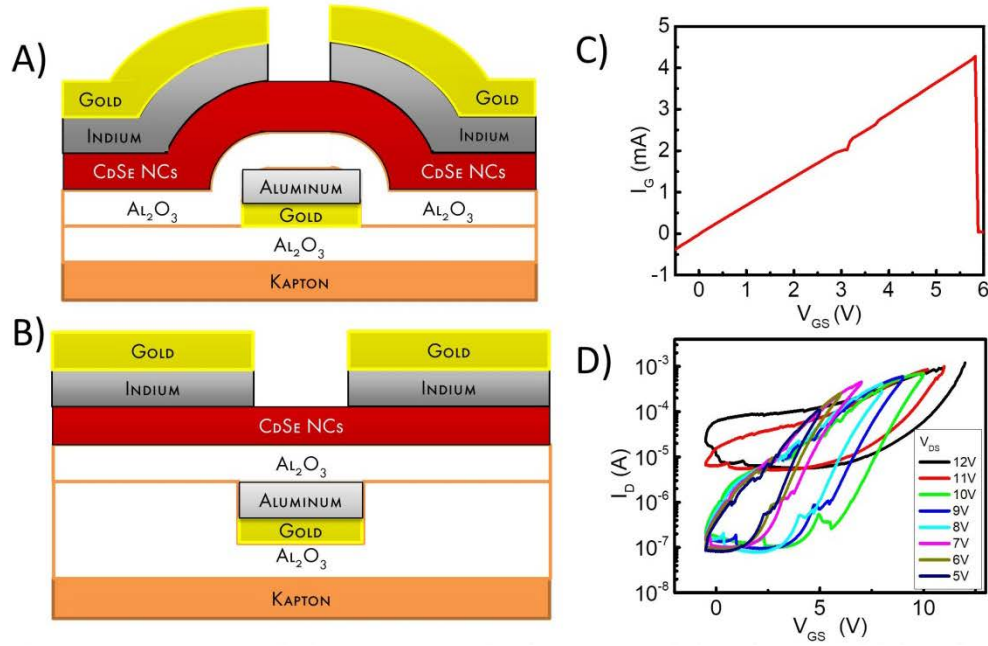
Figure 4-4 Diagram of a CdSe NC-TFT (A) without and (B) with gate electrodes inset into an oxide foundation. (C) Gate current measurement (I_G-V_{GS}) of device oxide breaking down at $V_{GS} > 5V$. (D) Transfer characteristics (I_D-V_{GS}) of a CdSe NC-TFT with gate inset into the oxide foundation.

In order to be able to make a wirebond connection to the oscillators, it was found that the contacts needed to be made significantly thicker and more robust than contacts used in prior IC development for direct probing. Thick layers of metal are required for wirebonding and this is usually achieved by electroplating the contacts. Unfortunately,

the electroplating process will etch the gate oxide. Therefore, contacts are developed

using thick (~500-1000 nm) layers of gold deposited by e-beam evaporation. Initially,

these contacts are deposited in a post-process step placing them on top of the structure

using the source and drain pattern with all but the contact pads physically masked (Figure

4-2E), as shown schematically in Figure 4-5A. Unfortunately, these contacts did not

adhere well enough to withstand the wirebonding process and they easily delaminated.

Thus, the process order was changed to use the same pattern but place a thick stack of

titanium and gold directly on the gate oxide, as shown schematically in Figure 4-5B. This

structure proved robust enough for successful wirebonds to be created, as shown in

Figure 4-5C.
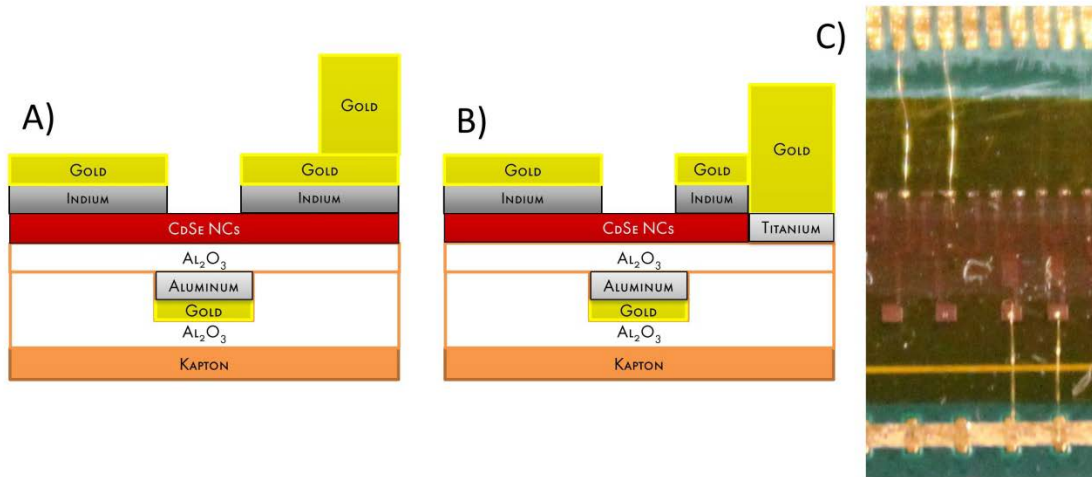
Figure 4-5 (A) Diagram of CdSe NC-TFT with wirebond contact on top of source and drain contacts and (B) with wirebond contacts directly placed on gate oxide. (C) Photograph of successfully wirebonded contacts.

Following the development of the updated fabrication methods, devices are fabricated to attempt to measure the oscillators. Figure 4-6A shows the PCB used to measure the individual devices. Design and schematics are shown in Appendix 4-2. External contacts are made using BNC cables. Power and ground is supplied from an HP 4156A semiconductor parameter analyzer. The load from the external probing is alleviated using an LM6172 100 MHz operational amplifier configured as a unity gain buffer. Output measurements are collected with a Tektronix TDS 2024B oscilloscope. Detailed diagram of measurement included in Appendix 4-3. Figure 4-5B shows completed devices with successful wirebonds to the board. The final design of the wirebond contact used large, extended sections of the titanium/gold stack in order to more easily allow the physical masking of the contact during the encapsulation procedure.

Unfortunately, the CdSe NC devices are found to be of very poor performance following the wirebonding procedure. This can be seen in Figure 4-6C where the capacitors and inductors in the oscillator slowly charge and momentarily oscillate. However, the CdSe NC-TFTs did not begin to drive the oscillation. The devices had degraded to mobilities of ~1 cm^2/Vs, despite being encapsulated. As the conductivity of the film is directly proportional to mobility, the dielectric relaxation frequency is therefore also directly proportional to mobility, assuming the other parameters remain constant. This would imply a theoretical cutoff frequency of ~1.5 MHz, well below the theoretically predicted oscillation of ~15MHz for a 1µH external inductor. The

degradation issue has multiple possible sources. It is possible that aggressive handing while mounting the substrate on the PCB compromised the encapsulation layer. It is also possible that this thickness of Al_2O_3 is not adequate to create an impermeable layer on Kapton on top of the IC structure. More careful handling of the sample as well as the use of thicker and potentially more robust encapsulation, such as an additional polymer layer on top of the alumina layer to further protect from devices from exposure and place the devices in a neutral strain axis, make it likely that future iterations of these devices will be successful.
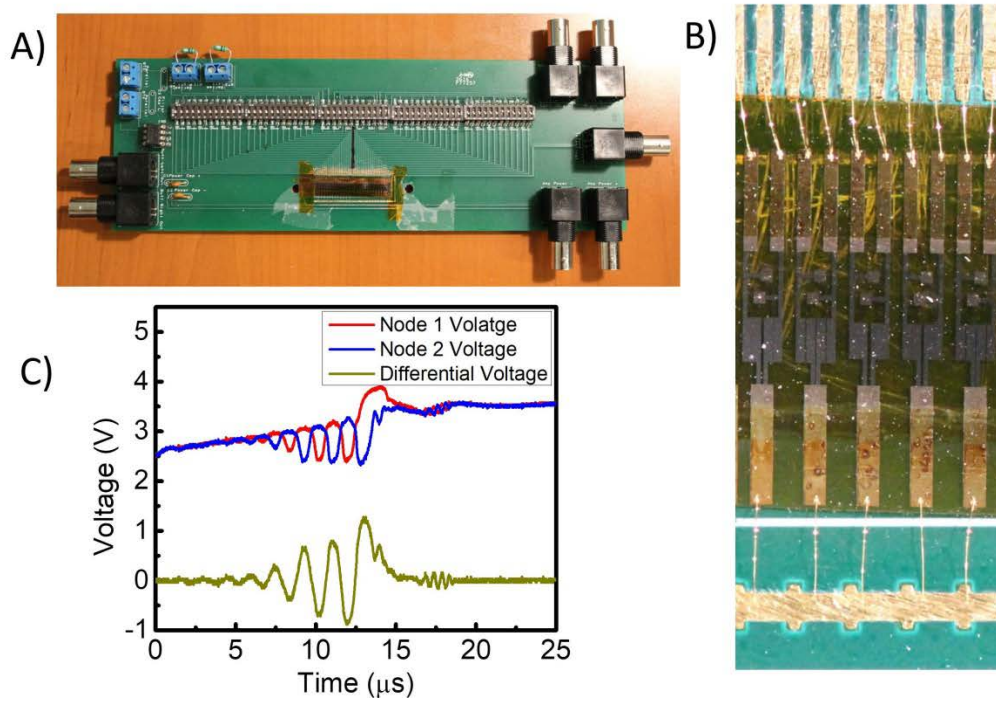
Figure 4-6 (A) Photograph of complete printed circuit board used for probing CdSe NC-TFT oscillators with sample mounted (lower middle) for wirebonding. (B) Photograph of complete devices wirebonded to the PCB. (C) Oscilloscope readout of measured oscillator with a 1 µH inductor and CdSe NC TFTs with channel length L=10 µm and channel width W=800 µm.

4-4: Conclusions

We demonstrate methods to fabricate CdSe NC oscillators targeting MHz frequency operation on a flexible substrate. These methods include the development of inset gate electrodes allowing for transistors operable at higher voltages as well as the development of contacts which allow a wirebond contact on a Kapton substrate. Simulations of this structure indicate the probability of MHz frequency oscillation. Future

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work will continue to pursue functional devices to show this operation in practice. Successful measurements will allow us to develop methodologies for directly probing the dielectric relaxation frequency; applicable not only on CdSe NC thin films, but also for probing transport in other unconventional semiconducting materials. In addition, successfully demonstrated CdSe TFTs in this frequency range will also open the door for the development of CdSe NC-ICs for high-performance sensors, displays, and audio applications.

Appendix 4-1: PSpice Layouts for CdSe device and oscillator circuit simulation.

Simulation of a custom first-order model for CdSe NC TFTs in a cross-coupled oscillator structure. Parameters used for simulation extracted from measurements of a sample of CdSe transistors with photopatterned electrodes on a Kapton substrate.
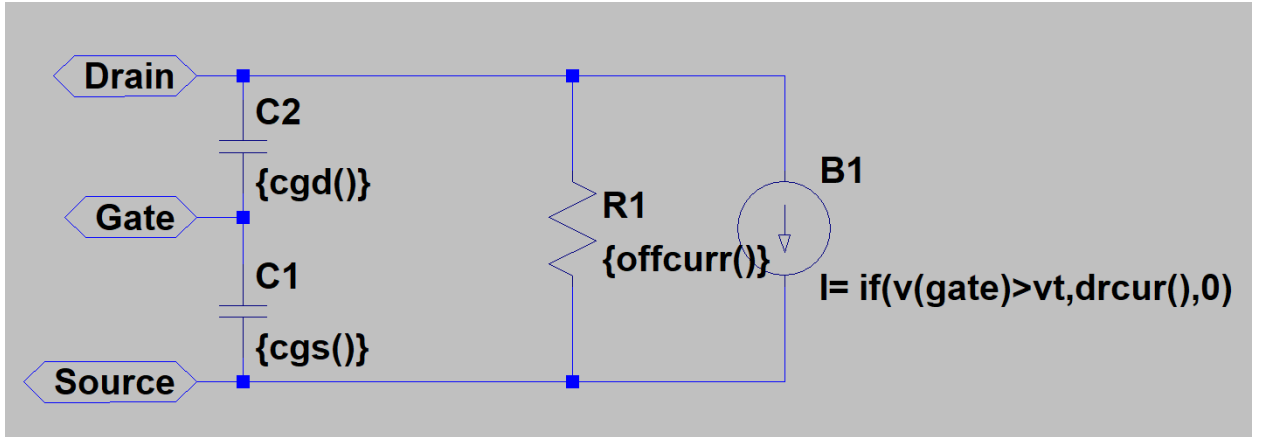

```
.param vt= .5
.param mus = 12
.param mul = 12
.param cox = 220n
.param wol = 40
.param lov = 10E-4
.param ltran = 10E-4
.param wtran = 400E-4
.param l1 = 0.06
.func leak() = {750E6/wol}
.func offcurr() = {leak()*10}
.func cov() = {wtran*lov*cox}
.func cgs() = {2/3*wtran*ltran*cox+cov()}
.func cgd() = {cov()}
.func drcur() = {if(v(drain) > v(gate)-vt,drcurs(),drcurl())}
.func drcurs() = {(mus*cox/2)*wol*square(v(gate,source)-vt)*(1+l1*v(drain,source)) }
.func drcurl() = {mul*cox*wol*((v(gate,source)-vt)*v(drain,source)-square(v(drain,source))/2)*(1+l1*v(drain,source)) }
```

.tran 0 50m 0 1n
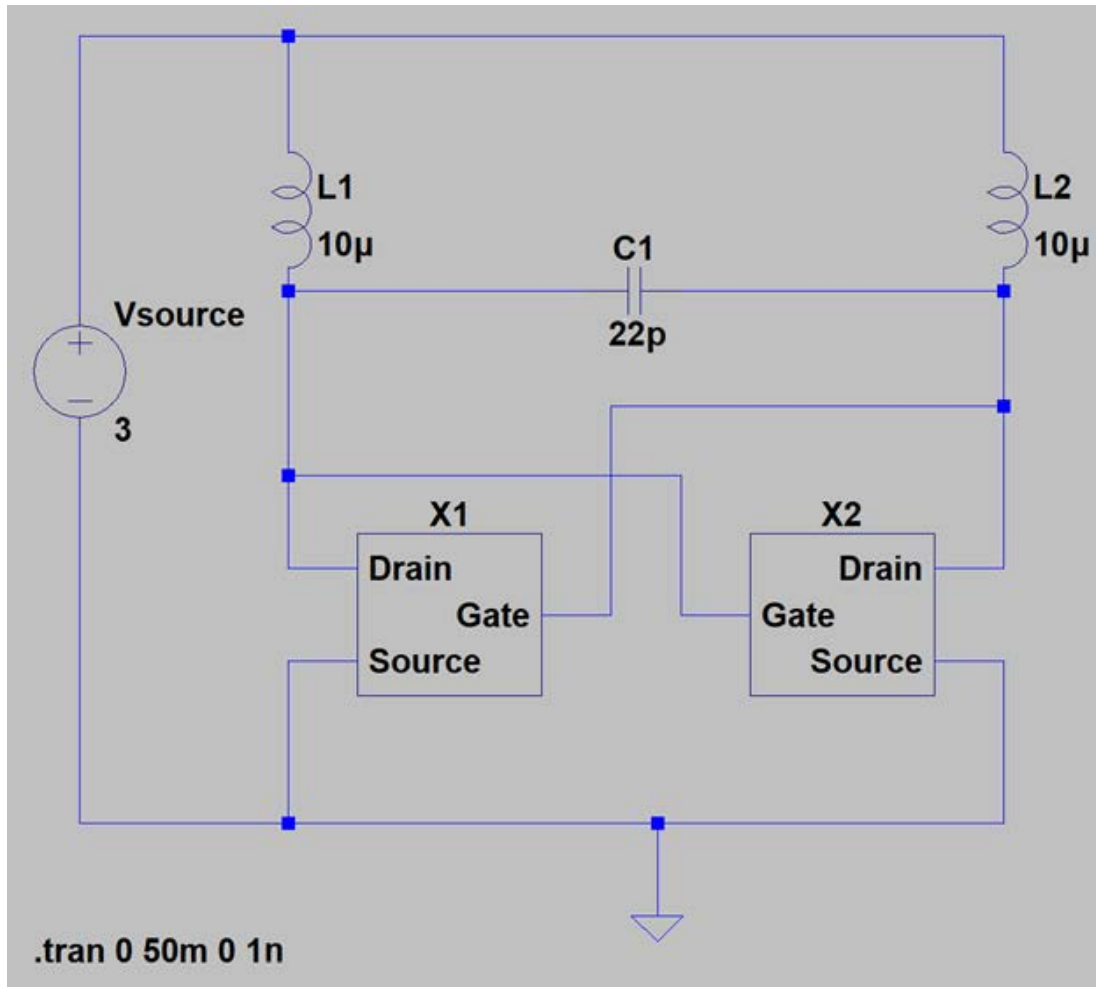
Appendix 4-2: Circuit schematic and layout of measurement PCB

Each oscillator and TFT is independently selectable using switches on the board in order to allow each one to be probed individually.
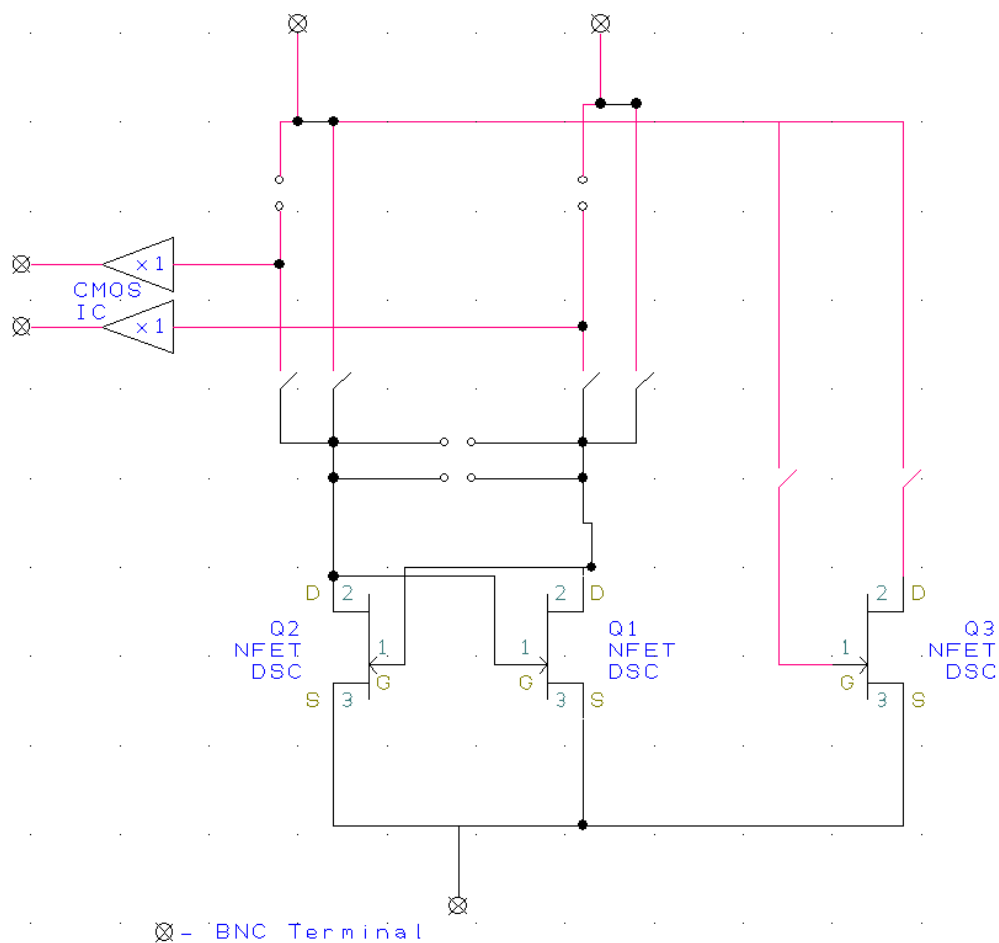
⊗ – BNC Terminal

○
○ – Screw Terminal for R/L/C

Transistor structure repated 12X for W/L = (In microns)
1000/10, 1000/20, 1000/40
800/10, 800/20, 800/40
400/10, 400/20, 400/40
200/10, 200/20, 200/40

Red lines represent traces on the top layer of the PCB. Light blue background is a ground plane on the bottom layer of the PCB for noise reduction.

Appendix 4-3 : Diagram of Oscillator Measurement
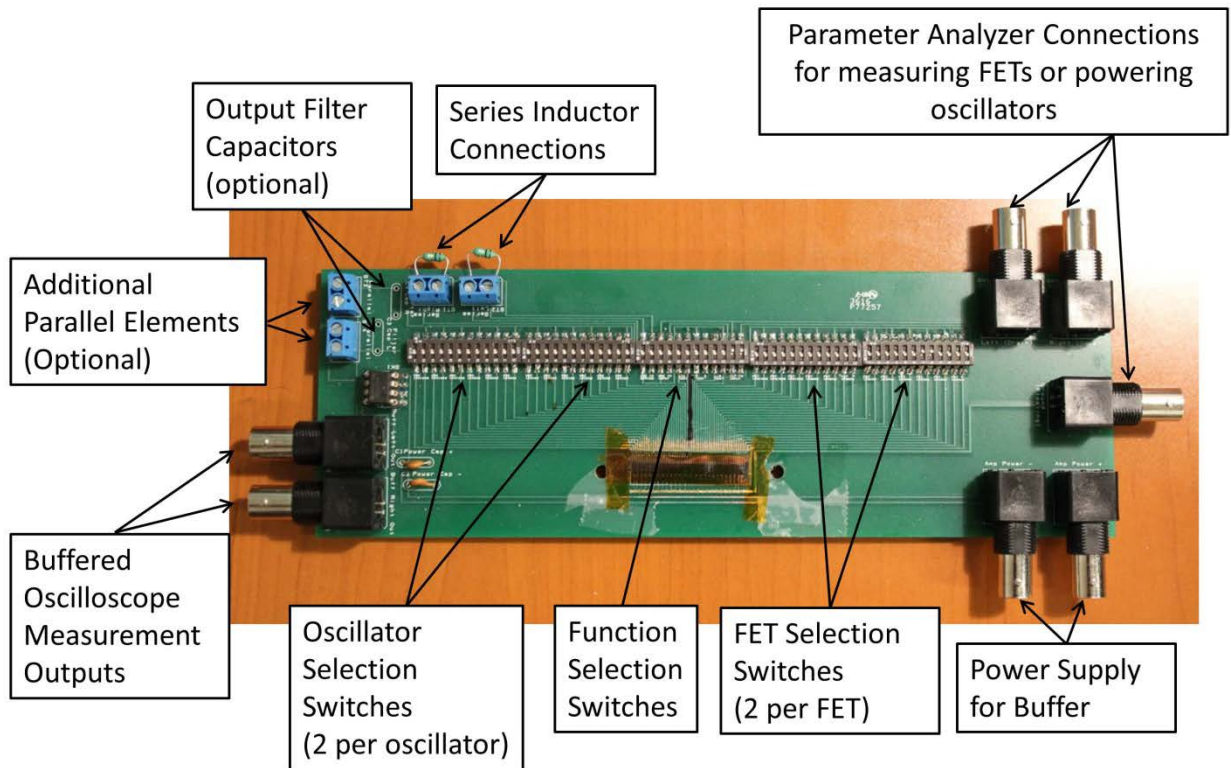
The top wirebond connections are provided with direct correlation to the location and number of devices. Bottom wirebond connection is a shared ground line.

For the selection switches, the two banks on the left and right are labeled as pairs for each FET or oscillator with width and length of the devices in microns. The center bank changes the function of the board. Starting from the left:

- **Osc to Series –** Connects the oscillator switch bank to the series inductances and output buffer inputs.

- **Osc to Input –** Connects the oscillator switch bank directly to the Left and Right terminals on the right of the PCB.

- **VIA Test** – Connects a VIA test structure directly to the Left and Right terminals on the right of the PCB. (Osc to Input switches must also be active)

- **R Test –** Connects a test structure shorting the right terminal to ground to the Right BNC terminal on the right of the PCB. (Osc to Input switches must also be active)

- **L Test –** Connects a test structure shorting the right terminal to ground to the Left BNC terminal on the right of the PCB. (Osc to Input switches must also be active)

- **L-R Test** - Connects a test structure shorting the right terminal to the right terminal to the Left and Right BNC terminals on the right of the PCB. (Osc to Input switches must also be active)

- **FET to Input –** Connects the FET switch bank to the Left and Right BNC terminals on the right of the PCB.

Three terminal connections to the parameter analyzer using the 3 top BNC connections on the right provide power for oscillators or measure FETs.

Positive and negative voltages >1V greater than anticipated output must be provided to the buffer for buffered output.

Output to the oscilloscope is probed directly on each end of the oscillator via independent buffers. Each output will be ~180º out of phase. Differential voltage must be calculated externally.

Screw terminals are provided for discrete inductor connection using though-hole parts.

Terminals are provided for adding additional coupling elements and filtering on the output. They are optional, but included for additional flexibility to tune or filter the oscillation.

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Chapter 5 : NFC Powered Flexible Electrochromic Displays

5-1: Introduction

When deploying electronic equipment, one of the primary concerns is how the device will receive power. When a small, portable package is desired, batteries can be cumbersome, expensive, and limited in their lifetime. Therefore it is preferable to have a permanent external supply or the ability to provide energy on-demand. Near Field Communication (NFC) has become a prime option for providing small amounts of on-demand power to a portable device.

NFC chips work by the principle of inductive power transmission. This is achieved by using two coils of wire in close proximity. The coil in the transmitter provides a focused radio frequency (RF) signal which can be received by a second coil of wire in close proximity. The electric signal in this second coil of wire can be rectified to produce a DC voltage adequate to power small devices. Data can be transmitted over this link by modulating the transmission frequency creating a simple link between two devices, where only one of which is directly powered. Applications for these devices are typically simple communication chips for radio frequency identification (RFID) tags, such as those found in access control tags and credit cards.

Here, we look to create an interactive experience on product packaging. Taking advantage of the NFC capabilities of many smartphones, we can harvest the power from the NFC link to activate a simple display. This allows the consumer a dynamic

experience with the product as well as the potential for the smartphone to interact with the product using the traditional NFC communication link.

For simplicity, a static display technology was chosen. The development of flexible display technology focuses on the ability to make a dynamic display capable of displaying arbitrary images.[1,2] However, simpler bimodal systems have also been developed with the capability to display only a single image. One of the simplest systems is an electrochromic display.[3] These are films which change color when an electric potential is applied to them and can only display one color. A simple pattern can be applied to show a single desired image. Given the space constraints and the desire to keep the cost of this system minimal, this was deemed the best option for this application.

Recent literature on electrochromic displays has shown the possibility to create flexible displays operable at low voltages with multiple colors.[3–5] These displays are produced with a simple structure and straightforward chemical procedures. Again, allowing a focus on the minimal cost of the devices. In addition, their physical flexibility allows for their placement in a larger variety of locations. This gives them the ability to be incorporated onto food packaging, which in many cases is a plastic bag. Coupling these flexible displays with commercially produced NFC products allowed for this demonstration of a simple display activated by a smart phone NFC transmitter.

5-2: Materials and Methods

All chemicals are purchased from Sigma-Aldrich. The electrochromic material is formed by a combination of an electrochromic dye, dimethyl ferrocene (DmFc), poly(vinylidene fluoride-co-hexafluoropropylene) (P(VDF-co-HFP)), and an ionic liquid (1-butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide) in a mass ratio of 3:1:12:60, respectively. For the blue color, methyl viologen hexaflourophosphate (MVHFP) is used as the electrochromic dye[3]; for red, diheptyl viologen hexaflorophosphate (DHVHFP) is used[4]. These chemicals are produced with a simple ion exchange reaction in DI H_2O. 100 mg of either methyl viologen dichloro hydrate[*] (blue, Figure 5-1A, B) or diheptyl viologen dibrobide[†] (red, Figure 5-1C) is dissolved in 5 mL of DI H_2O. Excess (>200 mg) ammonium hexaflourophosphate is dissolved separately in 5 mL of DI H_2O. The solutions are then combined into a single container. The desired material precipitates from this reaction and is filtered from the slurry, washed with DI H_2O, and placed under vacuum overnight to dry.

Differing from the literature procedure, these chemical are dispersed in acetone progressively. As the base form of P(VDF-co-HFP) is a pellet weighing approximately 40 mg, it is used as a discrete basis for the mixture. The solid polymer is very difficult and time consuming to dissolve in solvent when other materials are present, but can be easily dissolved when it is alone in the solvent. Therefore, the polymer is independently

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[*] IUPAC ID: 1,1′-Dimethyl-4,4′-bipyridinium dichloride
[†] IUPAC ID: 1,1′-Diheptyl-4,4′-bipyridinium dibromide

dissolved in 500 µL of acetone at 50°C. An exact weight of each pellet is recorded and used to determine the required amounts of the other chemicals based on the mass ratio specified above. The appropriate amount of DmFc and MVHFP or DHVHFP is then added to create an acetone mixture and vortexed briefly at room temperature. If MVHFP is being used as the dye, 100 µL of dimethylformamide (DMF) can then be added to the mixture to increase the polarity of the solvent. Finally, the appropriate amount of ionic liquid is added. It was found in experiment that if the DMF is not added to the MVHFP mixture, the addition of the ionic liquid will reduce the polarity of the solution to the point that the some of the MVHFP precipitates. DMF is unnecessary for DHVHFP dye.

As a substrate for the electrochromic material, an SU-8 pattern is created on the conductive side of an ITO-coated PET substrate. To create this layer, SU-8 2010 photoresist is spin coated directly onto ITO-coated PET pieces at 4000 rpm for 30 seconds creating an approximately 10 µm thick layer of SU-8. A piece of cut glass with soft polydimethylsulfoxide film (Trade name Gel-Pak) is used as a carrier to keep the PET stable on the spincoater. The substrates are then removed from the carrier and soft baked for 3 minutes at 95°C. The SU-8 is exposed using a Nanonex NX2600 mask aligner with an exposure of approximately 300 mJ/cm^2. The photomask used for the exposure is a Hershey corporate logo, a Hershey Kiss, or a Reese's cup logo pattern printed onto transparency film by a laser printer with a minimum dimension of 300 dpi (~90 µm) mounted by electrostatic forces to a blank piece of borosilicate glass. As the patterns are large, the precise dosing is not important and longer exposure times yields a

more robust cross-linked SU-8 product. The pieces are then baked for 4 minutes at 95°C. The substrates are then placed into a bath of SU-8 developer for 5 minutes while being periodically agitated. The substrates are then rinsed with isopropanol and dried with nitrogen. The remnant SU-8 which is exposed and cured during this process represents the area of the screen which will not change color when the electric field is applied. Even though this will be part of the final product, the residual SU-8 is not hard baked, as recommended by the manufacturer, as this makes the SU-8 hydrophobic. This hydrophobicity causes bubbling and wrinkles in the electrochromic film as it repels the electrochromic ink from the surface during deposition and curing.

This electrochromic ink is then deposited on the conductive side of ITO-coated PET (5 mil thickness, 60 Ω/sq) with an SU-8 pattern affixed with polyimide tape to a hot plate at room temperature. If DMF is not added to the MVHFP solution, the precipitated MVHFP is simply filtered from the solution with a 0.2 µm pore nylon syringe filter prior to deposition. It is important for the initial deposition to be done at room temperature as rapid evaporation of the dispersing solvent causes non-uniformities in the film. Immediately following deposition, the hot plate is turned on to 50°C and the sample is cured for 30 minutes in order to evaporate all residual solvent. While this extended curing time is not desirable, it was found that increased temperatures caused the formation of bubbles in the solvent which cause imperfections in the final film. If DMF is added to the solution to prevent precipitation of MVHFP, this curing time must be increased to 60 minutes to fully evaporate the solvent.

Following deposition of the electrochromic material on the patterned substrate, a second piece of ITO-coated PET is placed on top of the electrochromic material with the conductive side in contact with the electrochromic material to form the final structure (Figure 5-1A). Either Scotch double sided tape or Permatex 66B silicone RTV sealant applied by cotton swab was used to adhere the two layers together. As the electrochromic layer has very weak adhesion, this additional adhesive provided stability to the structure.
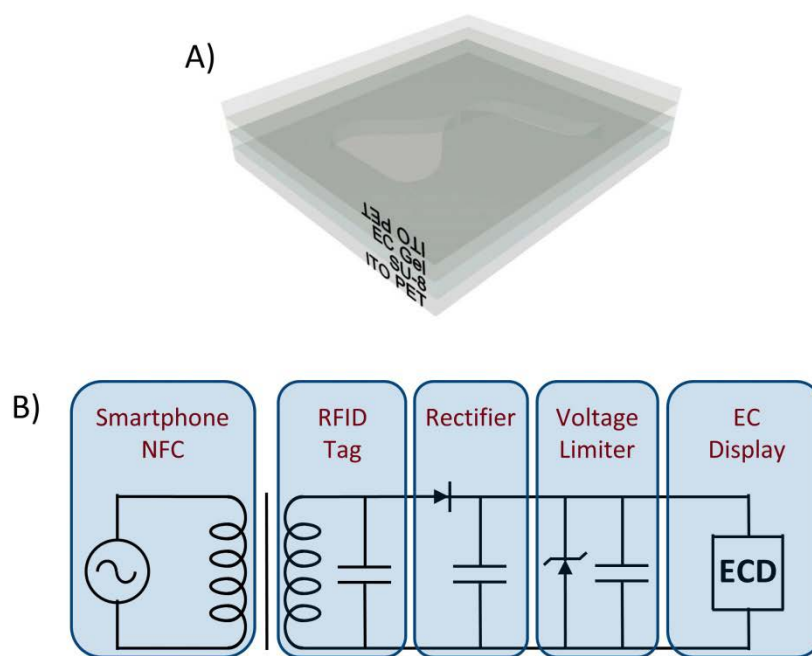

Figure 5-1 (A) Schematic of the electrochromic display structure. (B) Circuit diagram of NFC power harvesting circuit connected to electrochromic display.

The NFC circuit which powers the display consists of three stages, as shown in Figure 5-1B. The first is an NFC-enabled smartphone and a KKMoon radio frequency

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identification (RFID) key-tag providing the power source. The second stage is a simple diode rectifier and filter capacitor. The third stage is a reverse biased Zener diode acting as a voltage regulator and an additional filter capacitor. Connection between this circuit and the display was provided using alligator clips or zero insertion force (ZIF) connectors.

5-3: Results

Initial displays were successful for both blue (Figure 5-2A,B) and red (Figure 5-2C) dyes. The optional DMF added to the blue dye allowed more of the MVHFP to remain in solution and created a darker resultant display. For further demonstrations of this work, the optional DMF is not used as shorter annealing times are preferred.

Figure 5-2 Photographs of electrochromic displays with (A) MVHFP dye, (B) MVHFP dye with added DMF, and (C) DHVHFP dye.

The displays are tested at applied voltages of 2.5V to 5V. Initial testing is done at 5V using a USB charger or computer USB port as the power source. This would

frequently cause a burn-in effect in smaller displays, where a residual brown image is left after the screen is activated and the display will fail to change color when this bias is applied. (Figure 5-3A) This is the result of an electrochemical breakdown of the ionic liquid. 2.5V commercial voltage regulators are used during initial testing to bring the voltages down to a level which did not cause this effect. However, the lower applied field extended the time required to complete the electrochemical reaction. This led to slower turn-on transients. (Figure 5-3C,D) These turn-on transients could be reduced by using more dispersing solvent in the ink thereby reducing the thickness of the screen. (Figure 5-3 B) The procedure outlined here reflects this increase in solvent to keep turn-on times minimal.
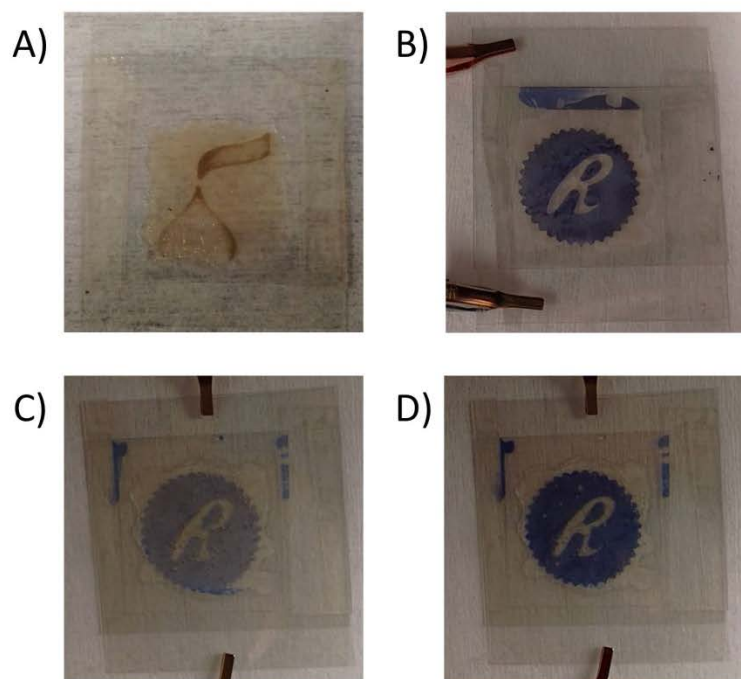
Figure 5-3 (A) Photograph of electrochromic display with burned-in image. (B) Photograph of thin MVHFP dye display after 5 seconds active. Photograph of thick MVHFP dye display after (C) 5 seconds and (D) 10 seconds active.

When the switch was made to testing with the NFC link, the regulator output failed to activate larger displays. The display was drawing more current than the voltage regulator could provide from the NFC link without depleting the output voltage due to the source resistance of the rectified signal as well as the regulator's own internal losses. These effects led to the switch to a Zener diode regulator structure when using the NFC link. This allows the maximum available power to be drawn directly from the link and the diode to simply act as a safety measure in case of a large input signal.

The resulting NFC-powered monochromatic displays were successful, as shown in Figure 5-4A. The displays turned on over the course of several seconds and bleached over the course of several minutes. The extended bleaching time can actually be desirable in an application as the display will not need to remain powered to keep the image visible. As this is an electrochemical reaction, it was found that the bleaching time could be moderately shortened by shorting the two contacts of the display. This may be possible in more complex active circuitry or by using a rectifying diode with a higher reverse bias current in a fully developed product.
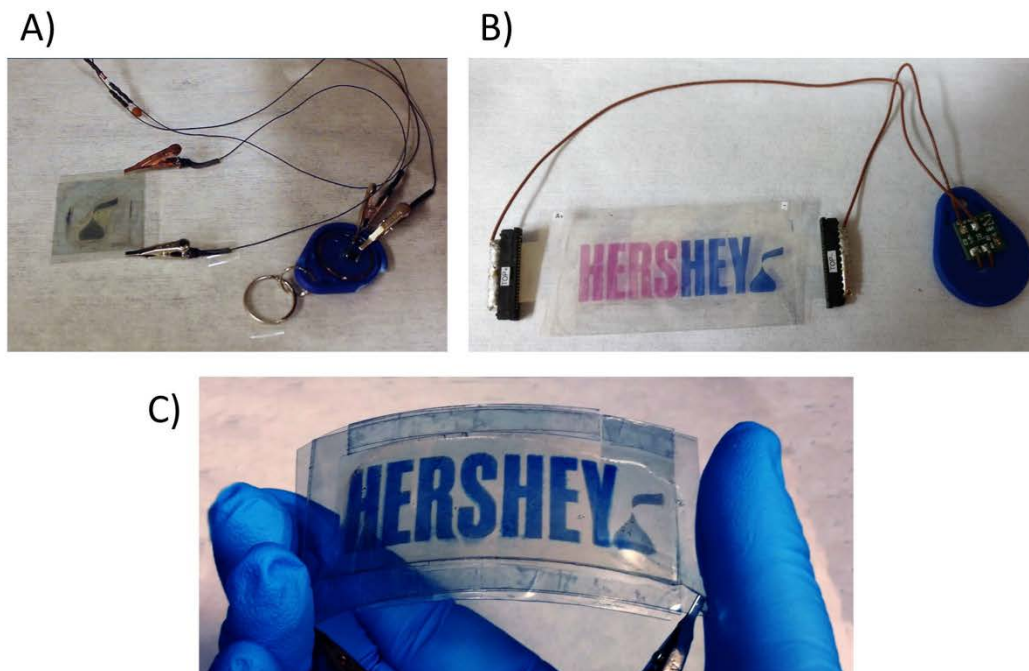
Figure 5-4 Photograph of (A) monochromatic and (B) polychromatic electrochromic display after being activated by the NFC link. (C) Photograph of monochromatic display being bent.

As an extension of the project, polychromatic devices were made which had both red and blue electrochromic material on a single substrate. (Figure 5-4B) The separation of the red and blue material was accomplished by careful manual deposition of the electrochromic materials into separate sections of the SU-8 pattern. This demonstration shows the viability of creating displays with many different colors within the same display. We also tested the functionality of displays under bending. As is shown in Figure 5-4C, the display was able to be activated when manually bent, thus displaying the viability of these displays to be placed on product packaging where flexibility is required.

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5-4: Conclusions

We demonstrate flexible, electrochromic displays with SU-8 patterns in multiple different colors. We integrate these patterned devices with an NFC device which can power them remotely without the use of a battery. This would allow for the display to be placed on packaging and used without concern for battery lifetime. We also show how timing can be controlled by modulating the thickness of the devices, allowing the potential for time-variant applications. We further demonstrate devices with multiple colors on a single substrate, allowing for polychromatic images to be displayed. These developments could be coupled with patterned or printed electrodes and more advanced active circuitry, opening the door for the development of mass producible displays on a flexible substrate, providing a dynamic, interactive user experience.

5-5 : References

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Chapter 6 : Future Directions

6-1: Nanocrystal Oscillators

Unfortunately, the CdSe nanocrystal (NC) oscillators, described in Chapter 4, were not successfully measured. A successful measurement is crucial for demonstrating the potential high-frequency applications of CdSe NC integrated circuits (IC) as well as probing the motion of carriers in the film. In order to create successful NC oscillators, there are two hurdles which remain: improved air stability and a reliable method for affixing the Kapton sample to the PCB. Both of these issues can be remedied without too much additional development.
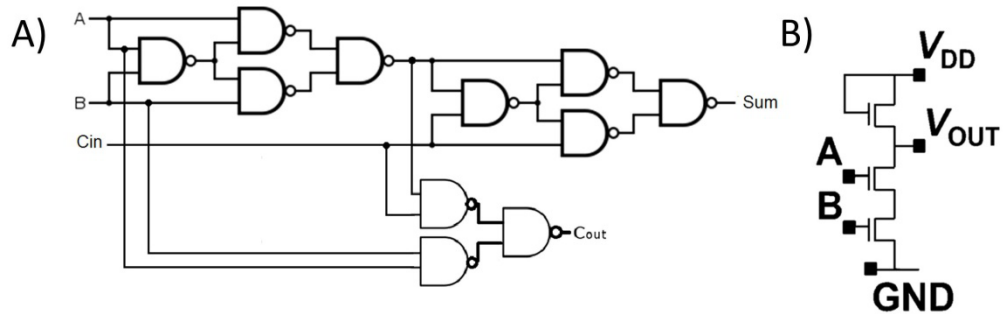
Due to extraneous factors, the devices which were wirebonded to the printed circuit board (PCB) spent many days in atmosphere. Based on the original work demonstrating air stable transistors, this should not be an issue as they should be stable in air for many days. However, it has been observed that the devices fabricated in the integrated circuit structure are not air stable; the devices degrade after only a couple days exposed to air. This is believed to be due to the increased surface roughness of the devices creating large steps that the aluminum oxide encapsulating media cannot cover, despite being conformal. Increased thicknesses of the encapsulating layer was attempted during this work, but was ultimately unsuccessful as of the writing of this dissertation. It is believed that the use of a thicker encapsulation layer and possibly an additional polymer layer, to provide additional device protection as well as reduce strain on the encapsulating film will solve this issue and yield successful results.

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The issue of substrate connection stems from the inherent flexibility of the Kapton and the nature of wirebonding. Initial testing used double-sided adhesive tape under the Kapton to attach it to the PCB. Unfortunately, this proved to be too soft for wirebonding as the wirebonding tip would not apply enough pressure to create a successful bond. Therefore, single-sided tape is used to attach the Kapton to the PCB. By having the Kapton directly on the PCB surface, this provided a hard enough surface for successful bonds to be made. However, it is very difficult to get the substrate perfectly flat on the PCB and the process of doing this bends and stretches the sample, potentially damaging the devices and encapsulating layer. The uneven surface that results from this procedure makes bonding of the full sample difficult, as the sample would move up and down during bonding when the needle presses on the surface. While this still allows the progressive testing of all devices, it is believed that leaving a larger blank section of the substrate at the edges to accommodate the tape, which was unfortunately trimmed earlier in the process, as well as more carful handing could remedy this issue.

6-2 : Multi-Stage Integrated Circuits

In order to further the applications of these devices for digital logic, they must be developed into more complex logic designs. One suggested configuration for this is the development of an adder. An adder is very important for the development of digital logic as it is one of the basic parts of an arithmetic logic unit, a central component of a microprocessor. This would involve the interconnection of many cascaded NAND gates, as shown in Figure 6-1. This would demonstrate the ability of one set of devices to switch

another, also referred to as noise margin. Cascaded logic gates were only demonstrated for inverters in Chapter 2. A further demonstration of cascaded multi-input devices is crucial to the future development of logic applications from nanocrystal integrated circuits.

Figure 6-1 (A) Logic diagram of a 1-bit full adder. (B) Circuit Diagram of a unipolar CdSe NAND logic gate.

6-3 : Non-Linear CdSe NC-TFT Modeling

In a traditional crystalline silicon semiconductor transistor, there are two well-defined regions of operation; linear and saturation. These regions can be modeled from theory using the following equations, usually referred to as the square-law model, with carrier mobility μ, oxide unit capacitance C_{ox}, threshold voltage V_T, and width and length of the active channel W and L, respectively:

$$I_D = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \text{ (Linear) } (0 > V_{DS} > V_{GS} - V_T)$$

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \text{ (Saturation) } (V_{DS} > V_{GS} - V_T)$$

These models hold true for most calculations. However, a correction, referred to as the Early Voltage (λ), is usually added in the saturation regime which accounts for a linear increase in drain current as drain-to-source voltage increases. This is most prominent in small channel devices (L<1µm) and is usually attributed to a modulation in effective channel length under high bias. This factor is added to the standard equation, as follows, with I_0 representing the uncorrected saturation drain current:

$$I_{D\lambda} = I_0(1 + \lambda \, V_{DS})$$

This model works well for modeling crystalline semiconductors. However, in many CdSe NC-TFTs, a non-linearity is observed in saturation. This non-linearity causes the drain current in the saturation regime not to flatten and increase linearly, but to curve and in some cases even decrease as the drain-to-source voltage is increased, as shown in Figure 6-2[1]. A physical explanation of this has not yet been found, but we believe it may have some basis in high-velocity lattice scattering as electron velocity increases with increased potential. In an attempt to characterize this effect, we developed a second-order model to fit the transistors.
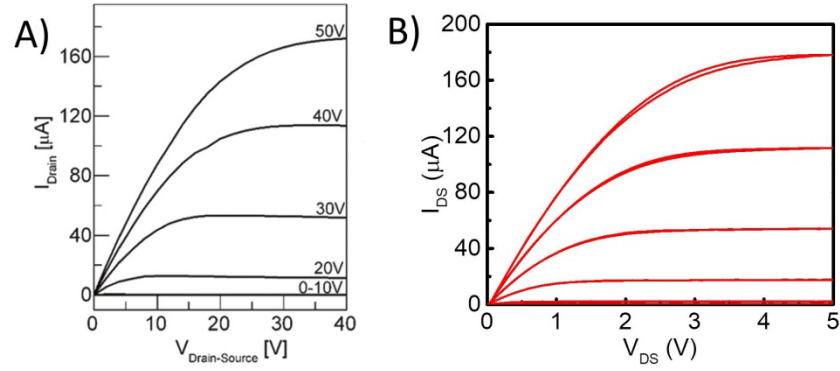
Figure 6-2 Output characteristics (I_{DS} vs. V_{DS}) for a CdSe TFT fabricated on (A) silicon wafer with SiO_2 dielectric and (B) Kapton with Al_2O_3 dielectric. (Figure A reproduced from Fafarman, A., *et al*, 2012)

The model we developed adds a second term to the channel modulation parameters in the saturation region of the square law model of transistor operation, as follows, with λ` representing the added second-order term:

$$I_{D\lambda`} = I_0(1 + \lambda\, V_{DS} + \lambda`V_{DS}^2)$$

The linear regime is assumed to be of the standard form without correction terms. In the linear model, the correction factors are found to have a discernable trend and raise the complexity of the model beyond a reasonable computation time for a least sum of squares fitting algorithm.

Using this model and a large set of data collected from an IC sample fabricated with the methods described in Chapter 2, we perform curve fitting of several devices in

MATLAB. The curve fitting algorithm used the assumption that there is a crossover point between the linear and saturation regimes where the value of each fit is equal. It then iteratively fits the data, assuming each point in the data to be the potential crossover, using the linear model to fit the data from V_{DS}=0 to the proposed crossover point and the saturation model for the data from the crossover point until V_{DS}=5V, the maximum voltage in the data being fitted. This process continues, saving each potential set of fitting parameters, until an inflection point is found where the difference between the fits of the two sections of the curve at the crossover point is closest to converging. The parameters extracted from this modeling are shown in Figure 6-3.
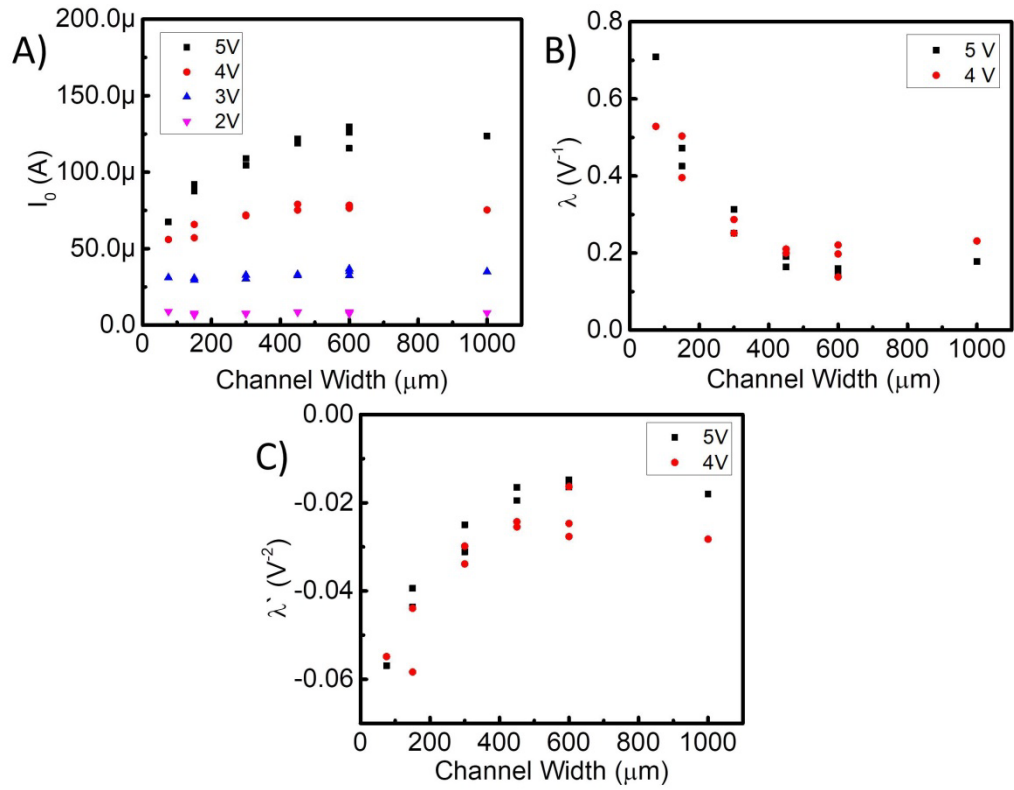
Figure 6-3 Plots of fitting results vs. channel length for different drain voltages for second order CdSe TFT model for (A) I0 (constant term), (B) Early Voltage (linear term), and (C) second-order correction term. Each point represents a fit of measurements from a single device. 2V and 3V are excluded from parameter results due to wide variation in results.

The results suggest a correlation between the channel width and the value of the fitted parameters. While the fitting parameters appear to show a trend, further exploration is needed. Testing on multiple samples from different fabrication and exchange techniques should be performed to characterize the variation in the parameters. For this data, there appears to be a correlation between channel sizing and fitted parameters. However, it is not yet known if this is a factor of purely the width or overall sizing and

the reasons for it. If this model can be explored and developed to accurately represent the devices, including this non-linearity, a better understanding of carrier movement may be obtained as well as the development of an advanced model giving us the ability to perform more accurate simulations of NC-TFT ICs in SPICE.

6-4 : CdSe Nanocrystal Photopatterning

One of the remaining limitations of CdSe NC-ICs in this work is that the NC thin film is not patterned. This means that the NC material covered the entire surface of the substrate and not just in the active regions. This has implications to device design as well as device performance. For design, the inability to pattern the materials limits us to unipolar ICs as we cannot deposit a p-type material for complimentary ICs. For performance, the existence of a contiguous film leads to undesirable coupling between devices. It also introduces parasitic transistors between the gate and source contacts as the gate metal travelling under the space between the contacts modulates the semiconducting material.

Patterning methods for this material have been previously developed in our group. The method is based on the discovery of the removal of CdSe NC films by tetramethyl ammonium hydroxide (TMAH) developer common in photolithographic processing. This can be coupled with a mask of photoresist to create a pattern in the CdSe NC thin film.

The process is done by placing photoresist directly onto a CdSe NC thin film without prior annealing. The pattern is then applied which exposes the resist in areas

where it is desired to remove the CdSe NC thin film. The developer is then used to selectively etch exposed positive photoresist and the underlying CdSe NC thin film by soaking the film in a bath of a TMAH developer for 3-5 minutes. This leaves behind a CdSe NC thin film pattern behind under unexposed photoresist. The unexposed resist can then be easily removed with a brief bath in acetone, which does not remove the CdSe NC thin film. Indium doping can then be used to recover the CdSe NC thin film from the chemical exposure. Representative samples are shown in Figure 6-4A,B.
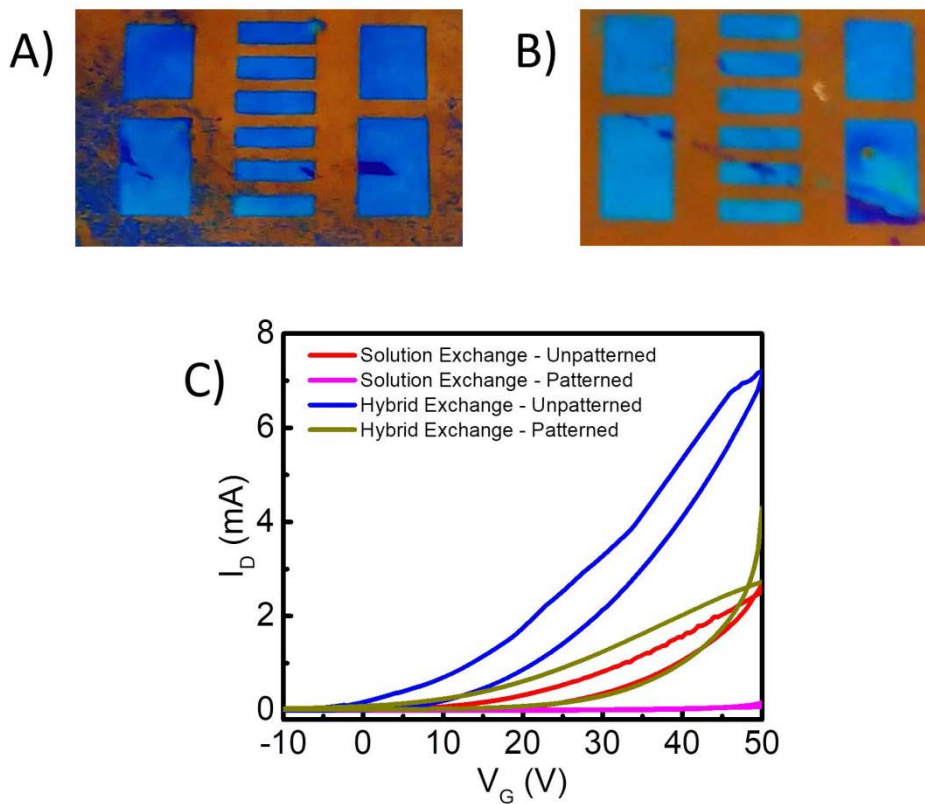
Figure 6-4 Photograph of patterned CdSe NC thin film on silicon wafer coated with a SiO_2/Al_2O_3 dielectric stack following (A) solution and (B) hybrid exchange. (C) Comparison of transfer characteristics (I_D-V_{GS}) of unpatterned and patterned samples form solution and hybrid exchanges.

While the method could produce patterned results, the performance of the recovered CdSe NC film is often degraded, as shown in Figure 6-3C. This reduction is mitigated to some extent by performing a hybrid exchange (Figure 6-4B) and a cleaner pattern is observed. However, depleted device performance is still observed. It is believed that the process, while leaving a film which looks visually acceptable, may damage the

film in other ways degrading the performance. In order to fully develop this procedure, this damage must be characterized and mitigated to restore high-performance CdSe NC-TFTs following pattering.

Other methods have been more recently developed by the Talapin Group which use photosensitive ligands to pattern the CdSe NC films[2]. The lift-off is then performed using polar solvents as developers rather than the TMAH developer. The resulting patterned films show only marginally degraded performance versus their prior reports. However, different ligand chemistries are used in this application which have not been fully explored and may not be compatible with the IC fabrication procedures on flexible substrates. Further development of these methods, either through incorporation of photosensitive ligands with thiocyanate ligands or development of IC fabrication procedures with these different ligand chemistries, may provide another route for patterned CdSe nanocrystals.

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