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Smart Sensor Networks For Sensor-Neural Interface

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Abstract
One in every fifty Americans suffers from paralysis, and approximately 23% of paralysis cases are caused by spinal cord injury. To help the spinal cord injured gain functionality of their paralyzed or lost body parts, a sensor-neural-actuator system is commonly used. The system includes: 1) sensor nodes, 2) a central control unit, 3) the neural-computer interface and 4) actuators. This thesis focuses on a sensor-neural interface and presents the research related to circuits for the sensor-neural interface.

In Chapter 2, three sensor designs are discussed, including a compressive sampling image sensor, an optical force sensor and a passive scattering force sensor. Chapter 3 discusses the design of the analog front-end circuit for the wireless sensor network system. A low-noise low-power analog front-end circuit in 0.5μm CMOS technology, a 12-bit 1MS/s successive approximation register (SAR) analog-to-digital converter (ADC) in 0.18μm CMOS process and a 6-bit asynchronous level-crossing ADC realized in 0.18μm CMOS process are presented. Chapter 4 shows the design of a low-power impulse-radio ultra-wide-band (IR-UWB) transceiver (TRx) that operates at a data rate of up to 10Mbps, with a power consumption of 4.9pJ/bit transmitted for the transmitter and 1.12nJ/bit received for the receiver. In Chapter 5, a wireless fully event-driven electrogoniometer is presented. The electrogoniometer is implemented using a pair of ultra-wide band (UWB) wireless smart sensor nodes interfacing with low power 3-axis accelerometers. The two smart sensor nodes are configured into a master node and a slave node, respectively. An experimental scenario data analysis shows higher than 90% reduction of the total data throughput using the proposed fully event-driven electrogoniometer to measure joint angle movements when compared with a synchronous Nyquist-rate sampling system.

The main contribution of this thesis includes: 1) the sensor designs that emphasize power efficiency and data throughput efficiency; 2) the fully event-driven wireless sensor network system design that minimizes data throughput and optimizes power consumption.

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ABSTRACT

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Nader Engheta

One in every fifty Americans suffers from paralysis, and approximately 23% of paralysis cases are caused by spinal cord injury [1]. To help the spinal cord injured gain functionality of their paralyzed or lost body parts, a sensor-neural-actuator system is commonly used. The system includes: 1) sensor nodes, 2) a central control unit, 3) the neural-computer interface and 4) actuators. This thesis focuses on a sensor-neural interface and presents the research related to circuits for the sensor-neural interface.

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(ADC) in 0.18μm CMOS process and a 6-bit asynchronous level-crossing ADC realized in 0.18μm CMOS process are presented. Chapter 4 shows the design of a low-power impulse-radio ultra-wide-band (IR-UWB) transceiver (TRx) that operates at a data rate of up to 10Mbps, with a power consumption of 4.9pJ/bit transmitted for the transmitter and 1.12nJ/bit received for the receiver. In Chapter 5, a wireless fully event-driven electrogoniometer is presented. The electrogoniometer is implemented using a pair of ultra-wide band (UWB) wireless smart sensor nodes interfacing with low power 3-axis accelerometers. The two smart sensor nodes are configured into a master node and a slave node, respectively. An experimental scenario data analysis shows higher than 90% reduction of the total data throughput using the proposed fully event-driven electrogoniometer to measure joint angle movements when compared with a synchronous Nyquist-rate sampling system.

The main contribution of this thesis includes: 1) the sensor designs that emphasize power efficiency and data throughput efficiency; 2) the fully event-driven wireless sensor network system design that minimizes data throughput and optimizes power consumption.

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Chapter 1

Motivation and Background

Paralysis has been one of the major illnesses that affect large populations both worldwide and in the United States of America. According to a study conducted by the Christopher & Dana Reeve Foundation in 2009, approximately 1.9% of American population (5.6 million) suffer from paralysis, either transient or permanent [1]. The study also listed the top causes of paralysis, including stroke, spinal cord injury (SCI) and multiple sclerosis. Spinal cord injury, as the second leading cause, was responsible for 23% of the 5.6 million paralysis cases in the U.S.

The study [1] showed that families with SCI patients were generally concentrated towards the lower annual household income bracketsAssociated with paralysis, the loss of productivity of paralyzed patients coupled with the expensive medical bills usually cause a decline in quality of life for the whole family. According to the 2016 Annual Statistical Report [9] by the National Spinal Cord Injury Statistical Center

(NSCISC) at the University of Alabama at Birmingham, 58.1% of SCI patients were employed at the time of the injury, but only 12.4% were able to be employed one year after the injury. The Report [9] also pointed out that the estimated lifetime costs directly due to SCI is around 4.7 million dollars (discounted at 2%) if the patient acquires high tetraplegia at 25 years old [10, 11, 12, 13]. The annual costs of a patient indirectly due to SCI, including losses in wages, fringe benefits and productivity, have an average of 72 thousand dollars per year [9].

To help paralyzed subjects, extensive research work has been conducted in the fields of Neural-Computer Interface (NCI)[14, 15, 16, 17, 18, 19], prosthesis [20, 21, 3, 22, 23, 24, 2] and wearable sensor network [25, 26, 6, 7, 27, 28]. A typical sensor-neural-actuator (SNA) system includes: 1) sensor nodes, 2) a central control unit (CCU), 3) the NCI and 4) actuators. Fig. 1.1 illustrates the blocks of a typical system and the information flow among the blocks.

Sensor nodes consist of sensors and signal processing circuits. Sensors are used to capture the physical interactions between the individual subject and the environment and to convert the interactions into electrical signals [29, 30, 31, 32, 33, 34, 35, 36]. With the advancement of material science, fabrication processes as well as information technology, low-power and miniaturized sensors are emerging rapidly. Accelerometers are usually used in sensing positions, gestures and angles [29, 30]. Gyroscopes are commonly used to sense movements and rotations [31, 32]. Strain gauges are widely used to sense forces and deformations [34, 35, 36]. Photodiodes and

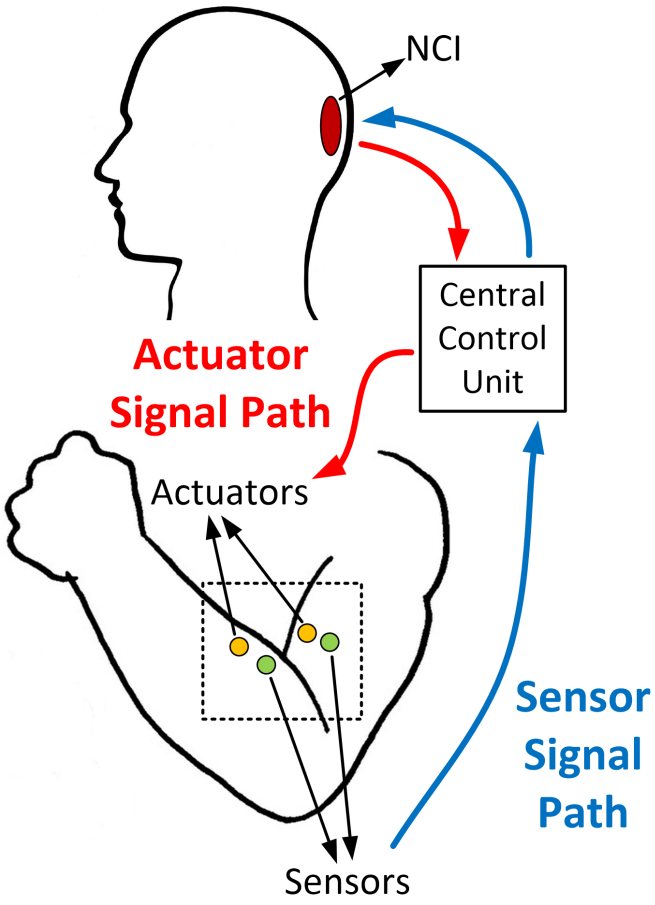

Figure 1.1: An illustration of the key functional blocks in a typical sensor-neural-actuator system.

image sensors are mostly used to sense ambient lighting, environment and motion [37, 38, 39]. The signal processing circuits interface with the sensors and condition (amplify, filter, digitize and digitally process) the electrical signals from the sensors [40, 41, 42, 43, 44, 45]. The signal processing circuits can be built with off-the-shelf components [40, 41] for low budget and short turnaround time, or they can be built with customized integrated circuits (IC) [43, 44, 45] for optimized functionality, low power consumption and miniaturized size.

The central control unit (CCU) acts as a relay of the sensory data from the sensor nodes as well as the neural activity information from the central nervous system [22, 5]. More extensively, it works collaboratively with the central nervous system [46, 47]. The CCU processes the data from the sensor nodes and encodes it into "neural language" by controlling the neural stimulator in the NCI to stimulate the central nervous system, which helps recreate the feeling of sensation [47, 48, 49, 4]. At the same time, the CCU takes the neural signals and decodes them into control signals to drive the actuators [5, 46, 50].

The neural-computer interface is the interface between the central nervous system and the central control unit. It delivers stimulations, either electrical [47, 50, 51, 52] or optical [53, 54, 55], to the central nervous system. Depending on the region where the stimulations are applied, sensations or body movements could be created [48, 49, 4, 52, 56]. Meanwhile, the NCI also gathers and records the electrical signals from the central nervous system [57, 58, 59, 60]. The signals are passed to the CCU

for analysis and further actions in the system.

Actuators convert electrical control signals into physical quantities [61, 62, 63], such as movements. Common actuators include but are not limited to: limb prosthesis [20, 21, 3, 22] to help amputated individuals gain mobility and muscle stimulations [21, 64, 65] to help individuals to gain control of the muscles whose functionalities were compromised by injury to the corresponding nerves. The sensors and the actuators can be integrated at the same site to form a bi-directional sensor-neural-actuator closed loop [48, 49, 4].

Depending on the applications, a combination of some or all of the blocks in the sensor-neural-actuator system can be implemented to help subjects compensate for the loss of physiological functions caused by paralysis.

J. He, et al., reviewed the neural prosthetics "for rehablitation of lower limb function spinal cord injured" in [2]. As shown in Fig. 1.2, SCI rehabilitation involves both and "assessments" and "therapies." For a sensor-neural-actuator system, the sensor signal path (blue path in Fig. 1.1) realizes the "assessments," while the actuator signal path (red path in Fig. 1.1) implements the "therapies."

K. D. Katyal, et al., introduced a hybrid brain-computer interface (BCI) system which "combines elements of autonomous robotic manipulation with neural decoding algorithms" to control a prosthetic hand [3]. As illustrated in Fig. 1.3, the hybrid BCI provides a good example of the implementation of a sensor-neural-actuator loop in Fig. 1.1. In-vivo experiments on a spinal cord injury patient have demonstrated

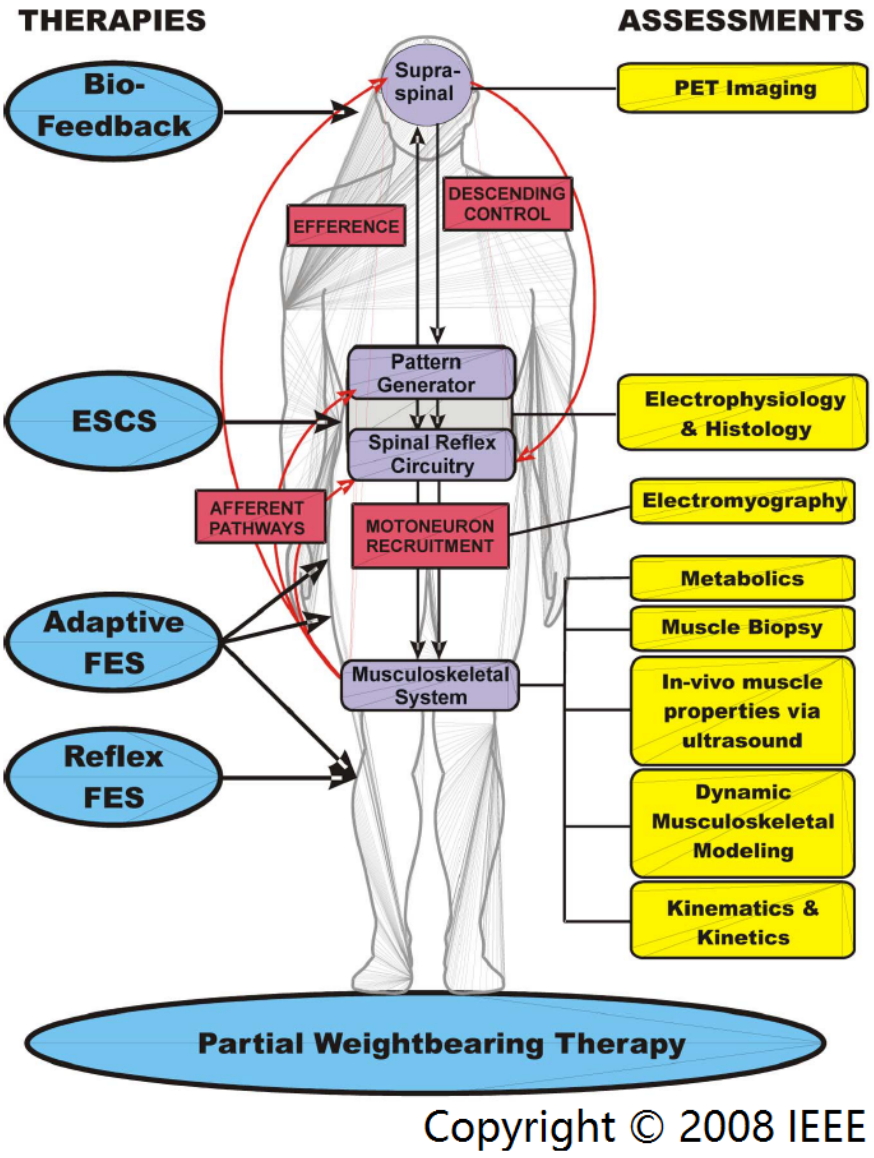

Figure 1.2: The schematics of a comprehensive system for SCI rehabilitation. It combines physiological system modeling, biosensors, medical therapy, advanced adaptive control, and neural interface technology in central and peripheral levels for improved understanding and treatment of neural motor disorders due to spinal cord injury. [2]

a 97.6% success rate for the patient to "grasp a known spherical object and place it at a desired location on a table" [3].

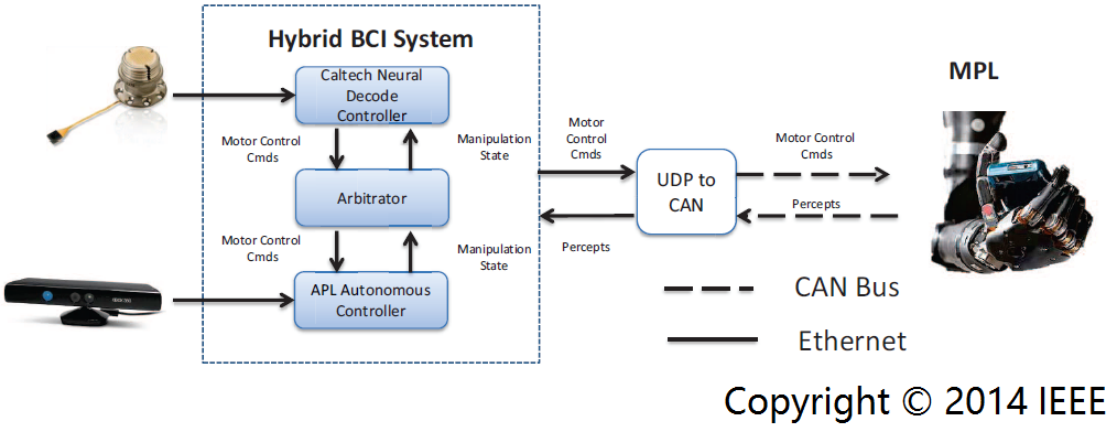

Figure 1.3: High-level block diagram presenting an overview of the hybrid BCI system [3].

In [4], X. Liu, et al., presented "a sensory feedback system for a prosthetic hand" including the sensor nodes, a partial CCU and a partial neural-computer interface blocks (actuator (blue) signal path in Fig. 1.1) in order to help upper limb amputated subjects recreate tactile sensation, as illustrated in Fig. 1.4. Tactile sensors are placed on the tips of the prosthetic fingers to sense the pressure on each finger tip. The pressure information is converted into "invoked tactile sensation at the stump skin of residual limb" in the form of transcutaneous electrical nerve stimulation (TENS). In-vivo tests have shown promising results.

G. R. Müller-Putz, et al., proposed a neural-actuator system that utilizes steady-state visual evoked potentials (SSVEPs) to control a two-axis electrical prosthetic

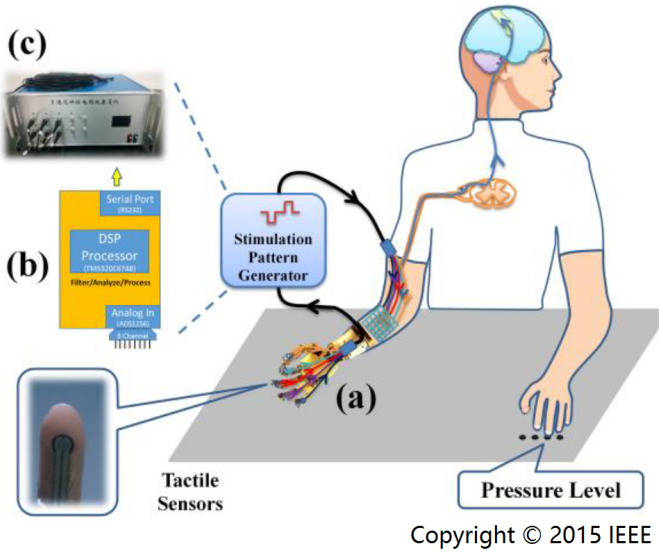

Figure 1.4: The structural diagram of the sensory feedback system: (a) the front module; (b) the signal processing module; (c) the electrical stimulator module. [4]

hand [5], as shown in Fig. 1.5, to implement a partial neural-computer interface, a partial CCU and actuators (sensor (red) signal path in Fig. 1.1). An up to 88% online classification accuracy has been achieved in experiments on four trained human test subjects.

A sensor network for mobile health (M-Health) applications is presented by F. Hu, et al., in [6]. A wireless sensor node implementation is depicted in Fig. 1.6. Biomedical signals such as electrocardiogram (ECG), electroencephalogram (EEG) and blood oxygen saturation ($SpO2$) are captured by the sensing chips. A microcontroller (MCU) processes the signals at each sensor motenode and sends the data out by a radio transceiver. A aggregation sensor (PDA), acting as a CCU (in

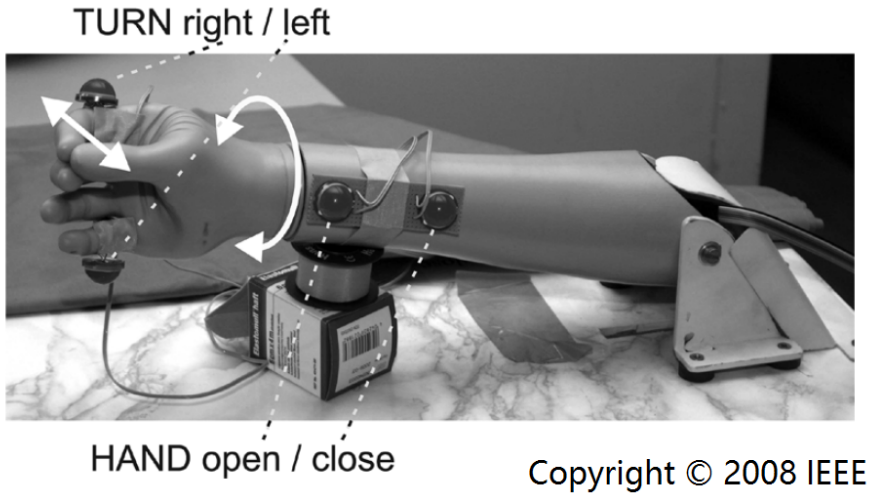

Figure 1.5: Hand prosthesis with mounted lights. It is attached at the fingers (the index finger to turn right, and the fifth finger to turn left) and at the forearm (the first light to open the hand, and the second one to close it) [5].

Fig. 1.1), gathers data from the sensor nodes and relays them to M-Health network, as shown in Fig. 1.6.

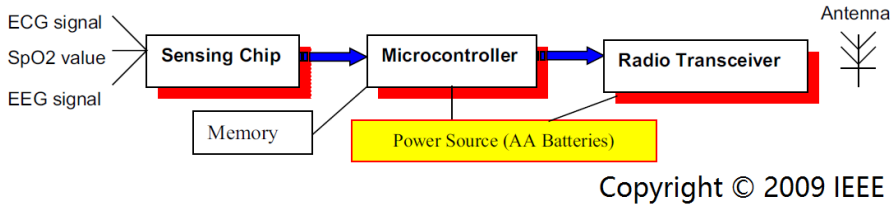

Figure 1.6: Medical sensor network (MSN) sensor node components. [6].

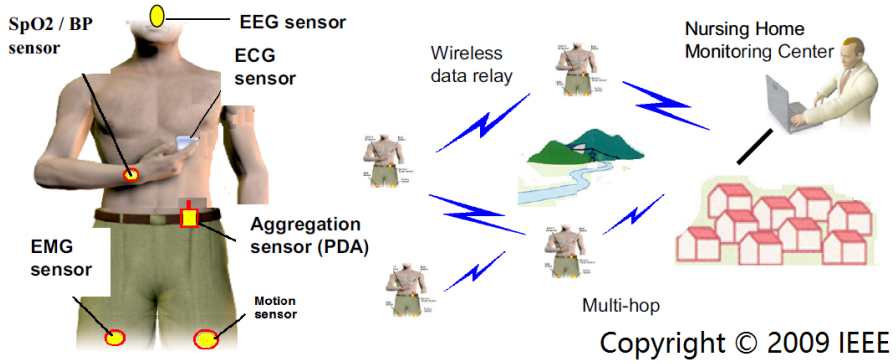

Figure 1.7: Wireless sensor networks (WSNs) for mobile health (M-Health). [6].

C. Gavriel, et al., showed a low-cost wireless body sensor network implemented with off-the-shelf components [7]. As shown in Fig. 1.8, the battery-powered wireless sensor node features a nine-axis motion-tracking sensor, an Arduino MCU and a wireless transceiver module in a coin-sized package. Real-time body motion (natural joint kinematics) streaming and recording are achieved with high accuracy.

A battery-free wireless smart glove is proposed by R. V. Aroca, et al., in [8], as "an assessment technology in stroke rehabilitation." The smart glove, as shown in

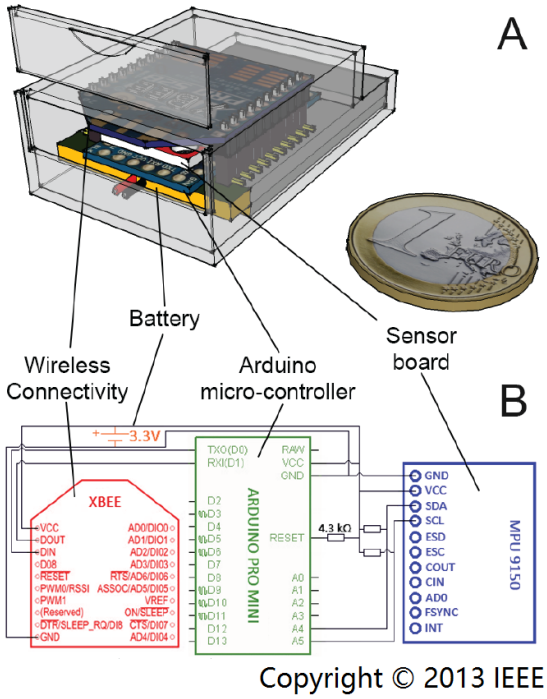

Figure 1.8: A) CAD drawing of the internal components of the wireless body sensor node, showing one possible packaging option. B) A schematic of the 4 main internal sensor components and their in-between connection paths. [7].

Fig. 1.9, is capable of measuring finger bending events utilizing a sensor node with ultra-high-frequency (UHF) radio-frequency identification (RFID) technology. The sensor node harvests energy from RF signals and uses the harvested energy to drive the strain gauge "Flex" sensor as well as to power an integrated analog-to-digital converter (ADC). The digitized sensor data is "backscattered" to the RFID reader by modulating the RFID antenna load at the sensor node.

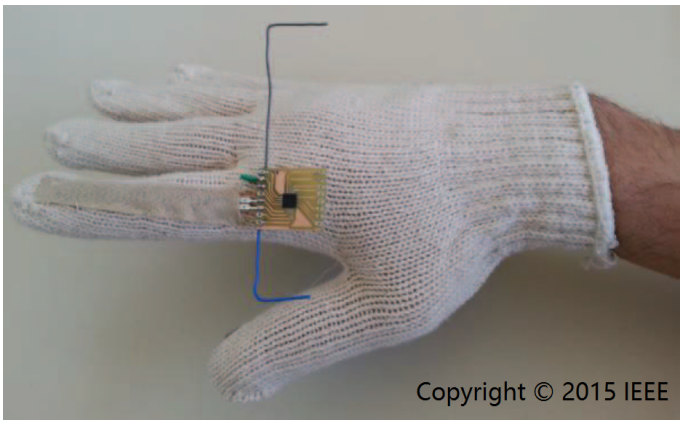

Figure 1.9: Glove with the Flex Sensor sewed on and the battery-free wireless smart sensor node attached. [8].

Despite encouraging state-of-the-art research, a fully operational sensor-neural-actuator system, with which the paralyzed individual is able to manipulate a prosthesis as his or her own body part, has not been extensively studied. One of the major challenges in such a system is absence of somatosensory feedback [66]. Even healthy individuals can experience difficulty in performing simple manual tasks without proper touch, posture and movement sensations [67]. Therefore, the research of this thesis focuses on the sensor-neural interface in the sensor-neural-actuator

system as shown in Fig. 1.1. Power efficiency and data-throughput efficiency of the sensor nodes are emphasized. As illustrated in Fig. 1.10, a pair of typical wireless sensor nodes for tactile sensation restoration application consists of a slave sensor on the finger tip and a master sensor on the wrist. Each sensor node has sensors, analog sensor interface circuits, power management circuits and wireless transceiver circuits. At the master sensor node, digital signal processing could also be implemented.

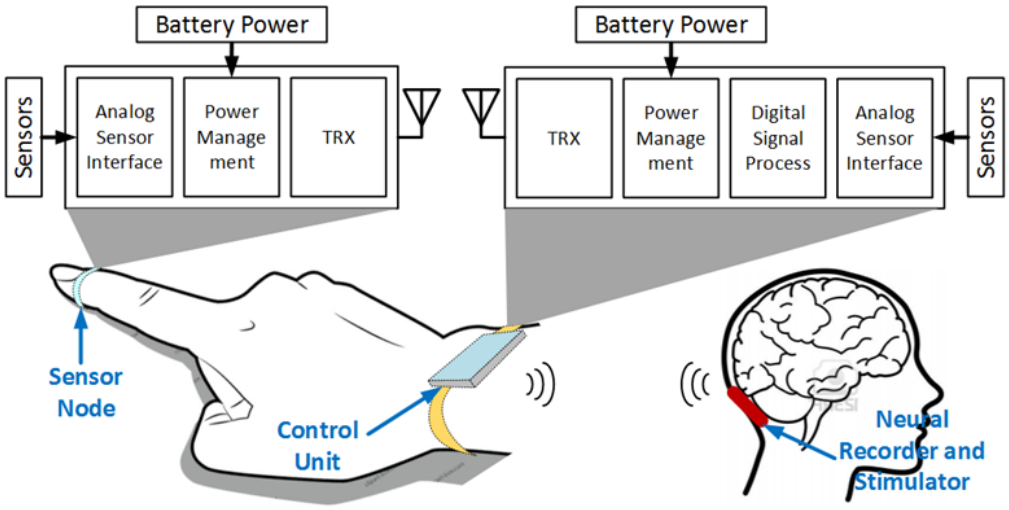

Figure 1.10: A pair of typical wireless sensor nodes for tactile sensation restoration application.

This thesis is organized as follows. Chapter 2 discusses the sensor design, including a compressive sampling image sensor, a standard-CMOS compatible optical force sensor and a passive scattering force sensor. Analog front-end circuit design is presented in Chapter 3, including a low-noise low-power analog front-end amplifier, 2 successive approximation register (SAR) ADCs and an asynchronous level-crossing ADC. Wireless circuit design is shown in Chapter 4. An impulse-radio ultra-wide-

band (IR-UWB) transceiver (TRx) is discussed. Chapter 5 shows a wireless fully event-driven electrogoniometer, as a system integration application of the wireless sensor network built with all the circuit blocks presented in this thesis. Chapter 6 concludes the thesis.

The main contribution of this thesis includes: 1) the sensor designs that emphasize power efficiency and data throughput efficiency; 2) the fully event-driven wireless sensor network system design that minimizes data throughput and optimizes power consumption.

Chapter 2

Sensors Design

Sensors, as the most front-end components in most modern sensor network systems, convert physical quantities into electrical signals. The research in sensor designs presented in this chapter provides sensors for the realization of smart sensor networks for sensor-brain interface. The research process also provides a good understanding of the properties and limitations of sensors, which as a result helps determine the specifications for the electrical circuit designs in the following chapters.

As the media between the physical world and the electric signals, several parameters play important roles in the sensor design. These parameters include sensitivity, range, power consumption, physical dimension and manufacturability.

Sensitivity reflects the sensor's accuracy to convert the physical quantity into electricity. Sensitivity is usually limited by the sensing mechanism, the sensing material and the sensor structure.

Range defines the extreme levels of the physical quantities that the sensor is able to handle in operation. Range, commonly known as the dynamic range of an image sensor, is mostly limited by the pixel design as well as the readout circuit design. The range of mechanical-to-electricity sensors is usually determined by the amount of mechanical deformation of the sensing material.

Power consumption reflects the sensor's efficiency of converting the physical quantity into electricity. It is mostly determined by the sensing mechanism. In addition, other factors such as the signal readout method, the sensing material and the fabrication process also affect the power consumption of the sensor.

The physical dimension of a sensor is determined by the sensor's applications. Miniaturized sensors are commonly used in, but not limited to, medical applications, since the artificial devices are expected to have minimal impact on physiology. On the other hand, large-scale sensors have been used as part of the structural materials in applications in robotics, architecture and civil engineering, etc.

Manufacturability is related to the difficulty in fabricating the sensor. It is also directly related to the cost and yield in the fabrication of the sensor as well as the sensor's ability to be integrated with the rest of the system, such as signal analysis and processing units. The less complicated the fabrication process of the sensor is, the better the yield and the easier the system integration are.

In the process of the sensor design, tradeoffs among the important parameters are necessary. For every sensor, the tradeoff between sensitivity and range is always

essential. This is mainly due to the properties and physical limitations of the sensing materials. The tradeoff between sensitivity and power consumption is usually the key factor in determining the sensing mechanism. A good sensor design takes a reasonable compromise of the parameters to meet the design specifications.

In this chapter, three sensor designs are presented, including a compressive sampling image sensor, an optical force sensor and a passive scattering force sensor. The compressive sampling image sensor is optimized for its low power consumption. The optical force sensor is optimized for its sensitivity as well as its ease of manufacture. The passive scattering force/stretch sensor is optimized for its power consumption, physical dimension and manufacturability.

2.1 Compressive Sampling Image Sensor

The content in the Compressive Sampling Image Sensor section was originally published in [68] ©2016 IEEE. Reprinted, with permission, from H. Zhu, M. Zhang, Y. Suo, T. D. Tran and J. Van der Spiegel, "Design of a Digital Address-Event Triggered Compressive Acquisition Image Sensor," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 2, pp. 191-199, Feb. 2016.

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2.1.1 Introduction

CMOS image sensors have experienced a rapid development in the past two decades. Its compatibility with the highly scaled modern CMOS technology enables a rapid increase of the image resolution, frame rate, and digital signal processing abilities. The recently reported commercial CMOS image sensors features higher than 20 mega pixels (MP) resolution with a frame rate of up to 90 frames per second (fps) for still image capture, or more than 4K resolution with up to 120fps for video recording [69, 70]. This fast growing requirement of image resolution and frame rate places an increased burden in terms of power consumption and readout rate. Image sensors that implement various on-chip, off-array image compression algorithms effectively reduce the throughput of the entire sensor, but cannot reduce the frame rate, or the amount of analog-to-digital conversion processing, which are typically the most power hungry functional units in an image sensor [71]. The concept of compressive acquisition realizes image compression during the image capture phase, which provides an alternative solution to on-chip image compression algorithm implementation.

Compressive sensing enables signal sampling at a rate lower than the Nyquist rate

without greatly sacrificing the quality of the original signal [72, 73, 74, 75]. Image sensors that implement on-chip compressive sensing algorithms have been reported in the literature [76, 77, 78, 79]. E.g. in [76], an analog compressive sensing processing unit is integrated at the focal plane. However, it suffers from poor linearity and large noise. Authors of [79] proposed a $\Delta\Sigma$-based single-shot compressive sensing image sensor, which divides the array into 4×4 pixel blocks. Power reduction is realized by doing an analog-to-digital conversion of only one randomly selected pixel from each block.

Time-to-first-spike image sensors that usually employ address-event representation (AER) as readout method, encode light intensity to time, which completely eliminates the A/D converter, and significantly reduces the readout data rate [80, 81, 82, 83, 84, 85, 86, 87, 88, 89]. In [81, 82, 80], the authors introduced three versions of time-to-first-spike image sensor designs, in which the each pixel is capable of generating a request when a photodiode is exposed to a certain intensity level, and requests are arbitrated for compressive AER readout. In [80], an arbitration time-to-first spike imager with on-chip histogram equalization was discussed. The design suffers from timing errors since it acknowledges pixel requests on a one-by-one basis instead of globally. Paper [83] and [84] proposed an image sensor enabling lossless compressive video acquisition as well as motion detection. AER is used to record the scene information captured by the imager, such as temporal contrast and grey scale. Paper [85] presented an image sensor using asynchronous time-based

image sensor (ATIS) with a real-time compressive sensing image reconstruction block implemented with a field-programmable gate array (FPGA). Images from the real-time reconstruction are shown to be comparable in quality to the images from state-of-the-art offline reconstruction. The authors of [88, 89] presented a time-to-first-spike imager for high dynamic range video recording. Paper [86] introduced an arbitration AER digital imager, which queues and arbitrates the read out sequence of the addresses of the exposed pixels. However, designs in [88, 89, 86] did not employ compressive sensing, therefore the amount of readout data is not reduced. [87] presented an imager with hybrid pixels implementing asynchronous dynamic event sensing and synchronous intensity sensing in the same pixel. However, the complicated structure of the hybrid pixel results in large pixel area and low fill factor.

In this chapter, an all-digital address-event triggered compressive acquisition image sensor, which combines the advantages of compressive sensing and AER, is presented. The imager is implemented in IBM 0.18μm standard CMOS technology, featuring an array of 48×72 22-transistor pixels, occupying a silicon area of $15\times15\mu m^2$ with a fill factor of 32.4%. After a global reset phase, each pixel raises a request when the integration voltage drops below a pre-set threshold of the pixel-level comparator. Requests are scanned, recorded and cleared in each request search cycle. A self-lock circuit is integrated in each pixel to make sure that one pixel only generates a single request in a frame capture phase. The all-digital nature of the proposed pixel design

guarantees its scalability in size with future CMOS technologies.

2.1.2 Design of the Image Sensor Array

Architecture and circuits of the pixel

Fig. 2.1 shows the architecture of the image sensor, consisting of a 48×72 array of all-digital image pixels with row and column control and address-event triggered readout circuitry. Each pixel consists of an inverter-based tunable-threshold-voltage comparator and a focal plane request logic unit. Fig. 2.2 illustrates the timing of a single pixel. The processing of each single pixel begins from a global reset phase, during which both the photodiode and the focal plane logic unit are reset (by "RST_{PIX}") and cleared (by "RST_{LGC}"), respectively, in each pixel. After the reset phase, the voltage of the photodiode, V_{PD}, drops proportionally to the illumination intensity. A "logic high" request signal, S_{REQ}, will be fired in the focal plane logic unit once the voltage of the photodiode is lower than a preset threshold voltage, V_{th}, of the pixel-level comparator. Readout circuitry records the address of the selected requesting pixels; subsequently a clear signal, CLR, is triggered to clear all the request signals in the fired pixels. A self-lock circuit is integrated in the focal plane logic unit to make sure that one pixel only generates a single request in the same frame capture phase. The "locked" status will be cleared during the next global reset phase by the focal plane logic reset signal, RST_{LGC}. If the darkest pixel is not fired by the end of the last loop, the readout logic will not wait any longer, but will

assign a value 0 to represent all the intensities that are smaller than the detectable threshold.

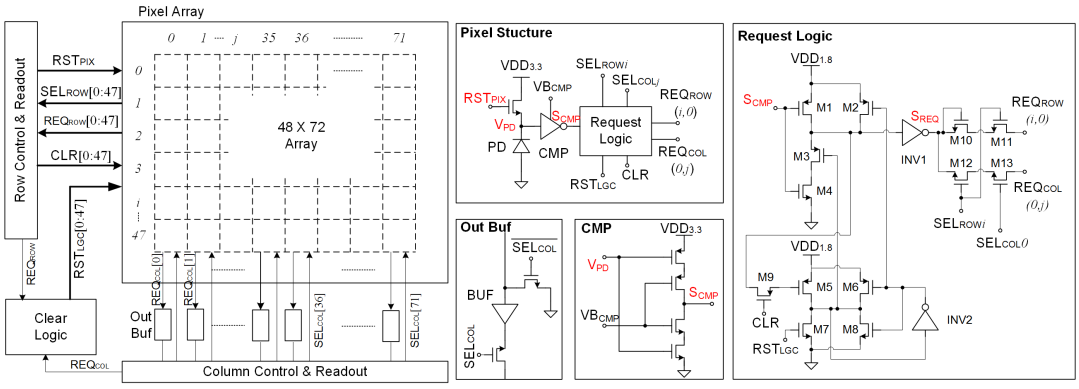


Figure 2.1: Architecture of the 48×72 all-digital address event image sensor array. Each pixel includes a reset transistor, a photodiode, a inverter-based tunable-threshold-voltage comparator, and an all-digital 17-transistor focal plane request logic unit. Column-level output buffers are employed for the readout of the requests generated in each pixel.

An inverter-based comparator, as illustrated in Fig. 2.1, is used to compare the voltage of the photodiode, V_{PD}, and a preset threshold. The threshold voltage V_{th} of the comparator is tunable between 1.0V to 2.0V which enables high tuning range for the pixel without occupying a large area. The simulated performance of the inverter-based comparator is close to a typical regenerative latch comparator which occupies at least twice as much of silicon area. Pre-amplifiers with offset cancellation are usually employed to reduce the offset of the comparators. However, they are not suitable for use in-pixel due to the area limitation and its complicated

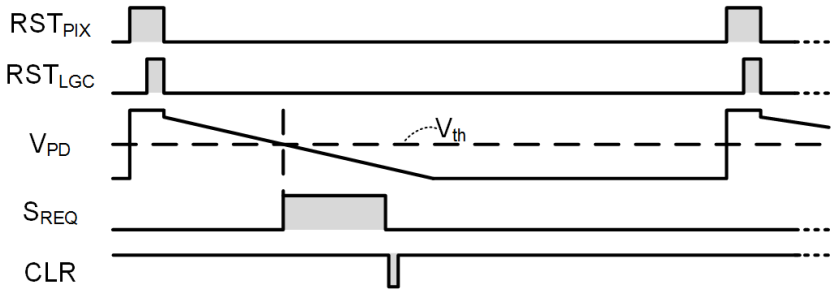


Figure 2.2: Timing of a single address event driven pixel. Both the photodiode and the focal plane logic unit are reset by RST_{PIX} and RST_{LGC} during the reset phase, respectively. After the reset phase, the voltage of the photodiode, V_{PD}, drops proportionally to the illumination intensity. A request, S_{REQ}, will be generated when V_{PD} is lower than a preset threshold voltage V_{th}. CLR will clear the request signal and lock the request logic until the next RST_{LGC}.

timing controls. To ensure a sufficient fill factor of the pixel, the mismatch of the comparators is traded off with comparator input gate area. Monte Carlo simulations of the comparator show that the standard deviation of the threshold voltage due to device mismatch and process variation is smaller than 30mV. The mismatch of the comparators contributes to the standard deviation of the fixed pattern noise (FPN) in dark, which is $30mV/(3.3V\text{-}0.7V\text{-}1.2V) = 2.14\%$, where $3.3V$ is the pixel reset supply voltage, $0.7V$ is the threshold voltage of the pixel reset NMOS switch, and $1.2V$ is the comparator threshold voltage.

The circuit of the focal plane logic unit is integrated in an all digital circuit with 17 transistors, as illustrated on the right of Fig. 2.1. The transistors M_{1-3} (with sizes of $0.5\mu m/0.32\mu m$ (thick oxide device), $0.4\mu m/0.18\mu m$ and $0.4\mu m/0.18\mu m$, respectively) and INV_1 ($2.4\mu m/0.18\mu m$ for PMOS and $0.4\mu m/0.18\mu m$ for NMOS for driving the row and column data buses) generate a pixel-level request, S_{REQ}, when the voltage of the photodiode is lower than the comparator threshold V_{th}. A pixel with a request generated is denoted as a "fired" pixel. M_5 and M_9 clear the request after it has been recorded. The W/L ratio of transistor M_5 ($3\mu m/0.18\mu m$) is much larger than that of M_8 ($0.22\mu m/2\mu m$), making sure the common drain node of M_5 and M_8 is pulled up during the clear period. The self-lock logic consists of $M_{4,6,8}$ (with sizes of $0.5\mu m/0.32\mu m$ (thick oxide device), $0.5\mu m/0.18\mu m$ and $0.22\mu m/2\mu m$, respectively) and INV_2, which lock the pixel output. All the $REQ_{ROW}(i,j)$ signals generated in a same row are connected to the row request bus. SEL_{ROW} signal

selects the row to be readout. The request of the selected row is transferred to the REQ_{ROW} output. The $REQ_{COL}(i, j)$ signal can only be read when a corresponding row is selected. In the row and column readout circuitry, buffers are added for an effective readout. The 72 columns are divided into two equal halves to double the processing speed of the triggered requests.

Timing and readout control logic

There are two different modes enabled in this design: i) video capture mode, and ii) compressive acquisition mode. Under video capture mode, the address of all the fired pixels will be readout, while under compressive acquisition mode, only the address of selected fired pixels will be readout. The value of the discarded pixels will be restored during the image reconstruction phase off-line, which will be detailed in the next section.

Fig. 2.3 illustrates the timing control of the readout process of the designed image sensor array under video capture mode. As mentioned in the previous subsection, for each pixel, after the reset phase, a request signal, S_{REQ}, will be generated once the photodiode voltage drops below V_{th}. A shift-register chain is included in both the row and column periphery circuits enabling a continuous scanning of the entire array. Take the i^{th} row for example. During one iteration, when the i^{th} row is selected ($SEL_{ROW}[i]$ is enabled), an active REQ_{ROW} (logic high) will be detected if one or more uncleared fired pixel(s) can be detected in the i^{th} row. A column scanning will

be triggered to readout the addresses of all the uncleared fired pixels. As mentioned earlier, there are two sets of column control and readout circuits for each half of the array. Fired pixels located in each half will be readout correspondingly. A clear signal, CLR, will be enabled to clear all the fired pixels by the end of current scanning iteration. No column scanning will be triggered if a low REQ_{ROW} is detected, in order to speed up the readout process. Pixels readout in the same iteration loop will be encoded to the same digitized gray level. The gray level is increased by one for each iteration. The digitized image will be further scaled up into the full range of a gray color map during image reconstruction.

Under compressive acquisition mode, the address(es) of only one or several fired pixels will be readout during one scanning iteration. The clear logic block enables: 1) one-pixel-one-iteration readout, which records address of the first detected fired pixel for each iteration. 2) N-continuous-pixel-one-iteration readout, which records the first N addresses of the detected fired pixels for each iteration. The value of N can be assigned from two configuration pins. The time span of each loop is controlled by a counter as part of the logic. The counter increases by one during each clock cycle. Once it counts to a preset threshold, one iteration is done. The value of the threshold can be preset through the two configuration pins as well. No matter which readout method is used, the start location of each scanning iteration is randomly assigned.

Fig. 2.4 (A) illustrates the state machine of the readout logic for the compressive

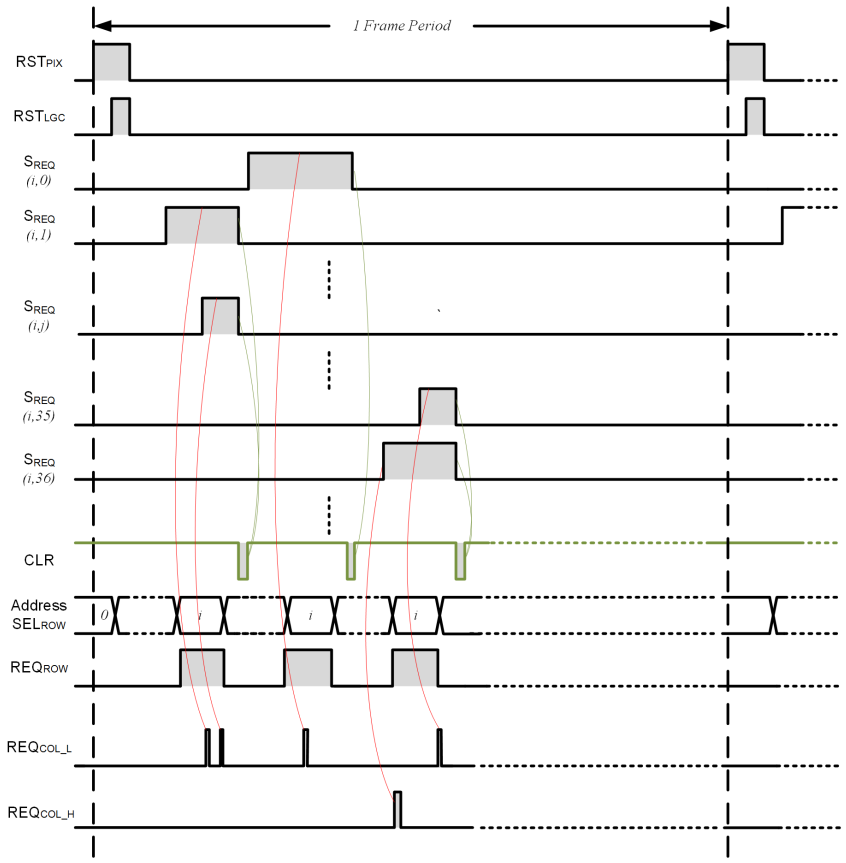


Figure 2.3: Timing control of the readout process of the proposed image sensor array under video capture mode. The i^{th} row is taken as an example. Once the i^{th} row is selected by $SEL_{ROW}[i]$, if an active ROW_{REQ} is detected due to the existence of one or more uncleared fired pixel(s) in the current row, a column scanning will be triggered to readout all the addresses of all the unclear fired pixels. A clear signal, CLR, will be enabled to clear all the fired pixels by the end of current scanning iteration.

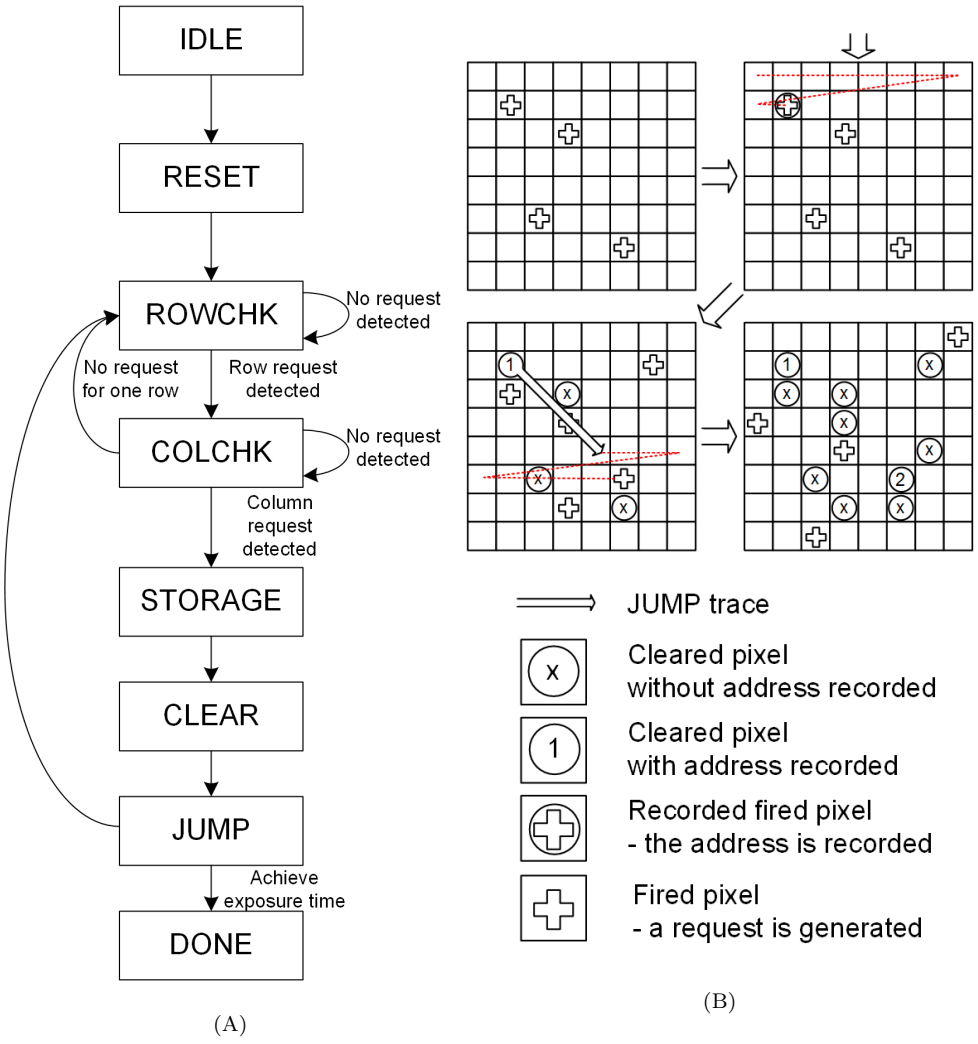


Figure 2.4: (A) State machine of the readout logic for the compressive acquisition mode with one-pixel-one-iteration readout. (B) A demonstration of the "Winner-takes-all" readout strategy.

acquisition mode with one-pixel-one-iteration readout. After the global reset of the photodiode as well as of the request of the logic circuit, the voltage of the photodiode from the overall array will drop proportionally to the light intensity. The system shifts the state from RESET to ROWCHK. In the ROWCHK state, the off array vertical control logic keeps scanning row by row. The row request from the selected row is taken as an input to the state machine during the ROWCHK state. One active row request input will shift the state to COLCHK. The column readout will then be triggered by scanning the requested row column by column until one pixel request is readout. Since the entire array is divided into two halves, the first half is denoted as the higher priority half in case two pixels requests are detected at the same time by the column readout circuit. The address of the request pixel will be recorded. There is a chance that a glitch may cause a false row request input. In order to increase the robustness of the system, a protection is applied in the COLCHK state, that if no column request is detected after scanning of the entire row, the state machine will be pulled back to ROWCHK state. A "Winner-take-all" strategy is applied to the compressive readout procedure, a clear signal, CLR, is triggered to clear all the request signals in the fired pixels, once one pixel is selected under one-pixel-one-iteration readout mode, or N pixels are selected under N-continuous-pixel-one-iteration readout mode. Only the address of the selected pixel/pixel-pair (if a column request is detected for both halves) is recorded, while all the unrecorded requests will be cleared together with the recorded one/ones. The

nature of the address event driven pixel design causes an uneven requests workload during the readout process. More pixels may be fired at some gray levels. The delay may mess up the relative histogram between pixels. The compressive acquisition readout method discards the majority of the pixels for each gray level, reducing the readout delay. The state machine enters a JUMP state to relocate to the next "start pixel" and then jump back to the ROWCHK state for the next scanning loop. An exposure time is preset for the control of the termination of the readout procedure. A graphic demonstration of the readout procedure is illustrated in Fig. 2.4 (B). An 8x8 array is taken as an example. The scanning begins from location [0,0], from the top left figure to top right one. It takes 10 clock cycles to scan to location [1,1], which is the second pixel on the second row. A off-chip field-programmable gate array (FPGA) pseudo random number generater is used in the JUMP state. A random number of clocks will be pushed into the horizontal and vertical control chain to shift the readout circuit from the currently selected pixel to another randomly selected pixel. As in this example, it takes 7 clock cycles to jump from [1,1] to [5,5]. If no pixel is readout before the counter achieves the threshold, only [1,1] and [5,5] will be readout, while all the other fired pixels are cleared. The bottom right array shows after a CLR signal is triggered, what the array looks like. It shows the readout pixels from the previous loop, the discarded pixels and newly fired pixels.

2.1.3 Image Reconstruction and Simulation

Algorithm for Image Reconstruction

The Algorithm presented in this section was provided by Dr. Yuanming Suo and Dr. Trac D. Tran from the Department of Electrical and Computer Engineering at Johns Hopkins University.

For the image acquisition method presented in the previous section, assume that the scene to be detected can be represented by an N-bit resolution grayscale digital image using a matrix $\mathbf{X}$, in which the intensity value of each pixel is $\mathbf{X}_{i,j}$, where i and j correspond to the horizontal and vertical locations of each pixel, respectively. The histogram of the image can be divided into a group of non-overlapping sets Σ_k, which can be defined as

$$\Sigma_k = \{(i,j) \mid \mathbf{X}_{i,j} \in [I_k, I_{k+1})\}, \tag{2.1.1}$$

where the intensity level $I_k \in [0, 2^N)$ and $I_k < I_{k+1}$. Under compressive acquisition mode, selected pixels are readout during each scanning iteration. The pixels readout during the same iteration will be assigned the same digital number to present the grayscale. Thus, the selected pixels within each set could be used to form a new matrix $\mathbf{X}_{\Sigma_k}$, where

$$\mathbf{X}_{\Sigma_k} = \begin{cases} \mathbf{X}_{i,j} & if\ (i,j) \in \Sigma_k \\ 0 & if\ (i,j) \notin \Sigma_k \end{cases} \tag{2.1.2}$$

Compared with the original matrix $\mathbf{X}$, the new sample image $\mathbf{X}_{\Sigma_k}$ has the values of pixels that do not belong to the set Σ_k replaced by zero. In other words, the

non-readout pixels are set to zero for image reconstruction. This is equivalent to using compressive sensing (CS) with a binary matrix, where the row number is the same as the number of non-zero pixels and the column number is the total number of pixels. For every row, there is only one non-zero value being one and the location of the non-zero value corresponds to the location of non-zero pixel (after the image is stretched into a vector).

Recovering the original image matrix $\mathbf{X}$ from a partially observed sample image $\mathbf{X}_{\Sigma_k}$ is an image completion problem, for which we take a dictionary learning based approach. First, we learn a dictionary or basis of image patches $\mathbf{D}$ using K-SVD [90] such that each image patch $\mathbf{x}$ (in a vector format) could be modeled using a linear combination of a few dictionary atoms as below,

$$\mathbf{x} = \mathbf{D}\mathbf{a}^\star \quad s.t. \quad ||\mathbf{a}^\star||_0 < s, \tag{2.1.3}$$

where ℓ_0-norm counts the non-zero value in the ground-truth sparse coefficient $\mathbf{a}^\star$ and there will be less than s non-zero coefficient values. This model can be naturally extended to a partially sampled version as below,

$$\mathbf{x}_{\Sigma_k} = \mathbf{D}_{\Sigma_k}\mathbf{a}^\star \quad s.t. \quad ||\mathbf{a}^\star||_0 < s, \tag{2.1.4}$$

where $\mathbf{x}_{\Sigma_k}$ is the sub-vector formed by extracting values on the active supports within Σ_k and $\mathbf{D}_{\Sigma_k}$ is the sub-matrix formed by extracting active rows corresponding to Σ_k.

In this work, 69 images [91] are used for dictionary learning. The images are mainly natural scenes, including pictures of flowers, fruits and cars. The training

images are chosen not to be similar to the test images to verify the generality of the proposed approach. After learning such a dictionary $\mathbf{D}$ from some training images, we will reconstruct the full image $\mathbf{X}$ from its partial observation $\mathbf{X}_{\Sigma_k}$ by solving the ℓ_0-norm minimization problem using orthogonal matching pursuit (OMP) [92] or its ℓ_1-norm relaxation in the framework of Convex Optimization [93]. For each sampled patch $\mathbf{x}_{\Sigma_k}$, we solve for its optimal sparse coefficient $\mathbf{a}$ with following formulation,

$$\min_{\mathbf{a}} ||\mathbf{x}_{\Sigma_k} - \mathbf{D}_{\Sigma_k}\mathbf{a}|| \quad s.t. \quad ||\mathbf{a}||_0 < s. \tag{2.1.5}$$

Then each patch is approximated by $\widetilde{\mathbf{x}} = \mathbf{D}\mathbf{a}$. To measure the recovery performance, we adopt Peak signal-to-noise ratio (PSNR) as well as structural similarity index (SSIM) [94]. PSNR is most commonly used to measure the quality of reconstruction of lossy compression techniques while its result might be inconsistent with human eye perception. SSIM improves upon PSNR and captures the context structure in the image better.

Simulation Results

The simulation presented in this section was performed by Dr. Milin Zhang from Department of Electrical and Systems Engineering, University of Pennsylvania.

The compression ratio of the algorithm can be calculated from the total amount of members selected from each set. Take the Lena image for example. The resolution of the original image is 24-bit with an array size of 256×256, as shown in Fig. 2.5 (A). All the pixels are classified into 2^{13} equally divided grayscale sets. N-continuous-

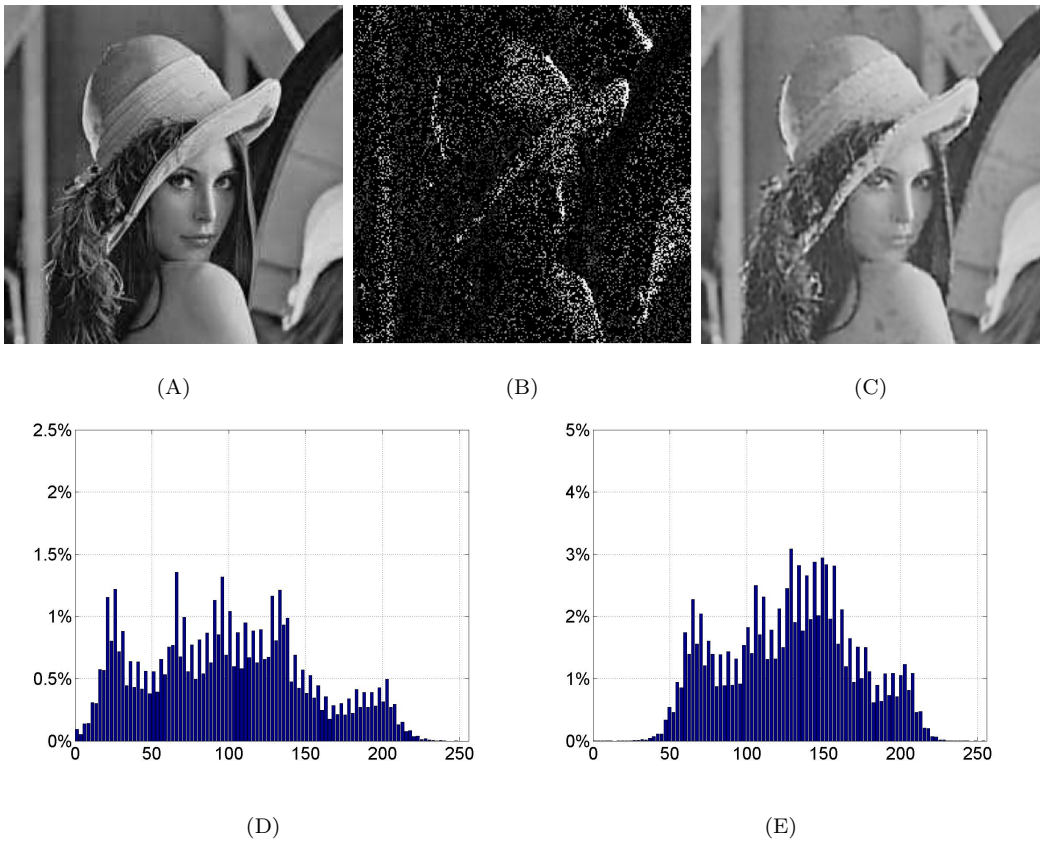


Figure 2.5: (A) A 24-bit 256×256 original sampled image is employed for the demonstration of the proposed image processing. The grayscale is equally divided into 2^{13} levels. N-continuous-pixel-one iteration readout method is used to form (B) the compressive sampled matrix $I_{smp}(i, j)$. (C) Reconstructed image from (B). A PSNR of 23dB and a SSIM of 0.835 is achieved. (D) and (E) show the histogram of the raw image and reconstructed image, respectively.

(A.1) 20.36:1
PSNR=19.4dB
SSIM=0.588

(B.1) 10.40:1
PSNR=22.7dB
SSIM=0.682

(C.1) 5.35:1
PSNR=23.0dB
SSIM=0.835

(A.2) 18.58:1
PSNR=14.9dB
SSIM=0.636

(B.2) 9.39:1
PSNR=19.3dB
SSIM=0.75

(C.2) 4.80:1
PSNR=20.8dB
SSIM=0.868

(A.3) 18.61:1
PSNR=13.7dB
SSIM=0.477

(B.3) 9.51:1
PSNR=16.5dB
SSIM=0.609

(C.3) 4.90:1
PSNR=19.6dB
SSIM=0.758

Figure 2.6: Reconstructed sample images with different compression ratios labelled underneath each figure.

pixel-one iteration readout method is used. The compressive sampled image is illustrated in Fig. 2.5 (B). A compression ratio of 5.35:1 is achieved. Compared with the original image, a peak signal-to-noise ratio (PSNR) of 23dB and a structural similarity (SSIM) of 0.835 is estimated from the reconstructed image in Fig. 2.5 (C). Fig. 2.5 (D) and (E) illustrate the histogram of the raw image and reconstructed image, respectively. The histogram of the image shifts after the reconstruction. Since the rescaling of the digitized pixel value does not directly represent the intensity level of the original scene, SSIM will be better to quantitatively evaluate the quality of the reconstructed image. Fig. 2.6 illustrates more reconstructed sample images with different compression ratios. In each sample image, with increased compression ratio, the PSNR and SSIM drops, which is also noticeable by the degradation of the level of details in the image. For the samples here, a compression ratio of 18 to 20 results in poor quality but recognizable images. With a compression ratio higher than 20, detail losses in the images are too significant so the objects in the images are not recognizable.

A simulation is also performed on the circuit level with a 16×16 array to verify the function of the system. 136 requests are captured and recorded as shown in Fig. 2.7 (A). The reconstructed image is illustrated in Fig. 2.7 (B). The compression ratio of this sample is around 2. The reconstructed image of the letter "A" is recognizable. Given the small size of the array in this simulation, a compression ratio greater than 2 are not likely to yield satisfactory results in the reconstructed image.

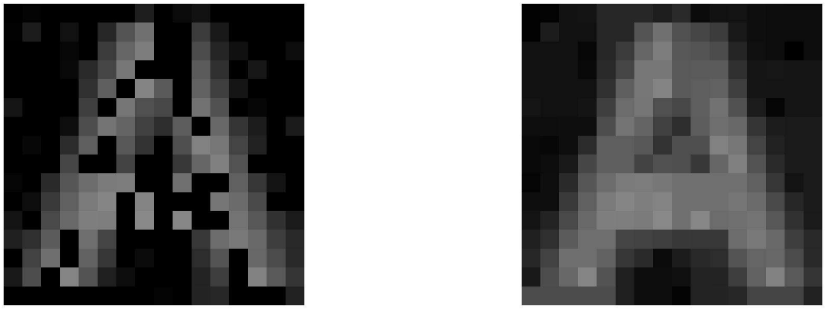


Figure 2.7: A simulation is performed on a 16×16 array. (A) 136 requests are captured and recorded. The value of unrecorded pixels are filled by zero. (B) Reconstructed image from the captured results.

2.1.4 Chip Fabrication and Experimental Results

Chip Fabrication

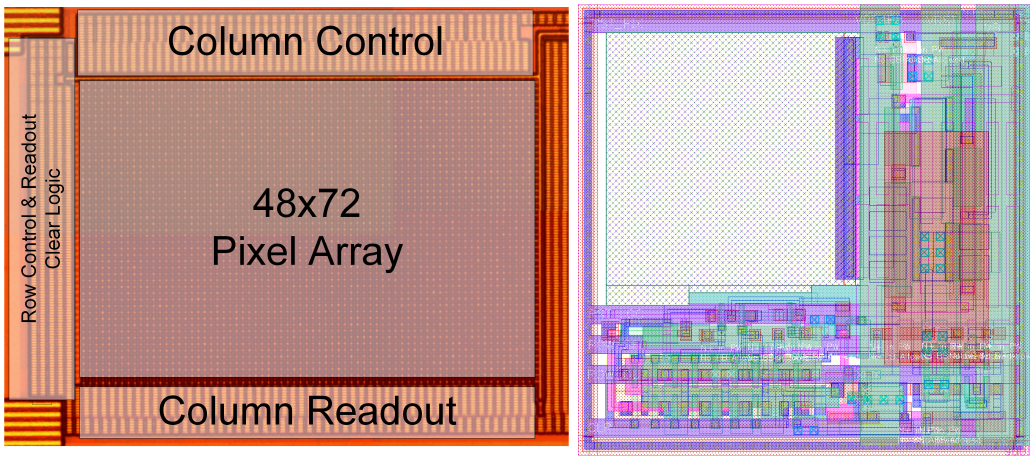
The image sensor that implements the compression scheme, consisting of an array of 48×72 pixels was fabricated using IBM 0.18μm standard CMOS process. The chip occupies an area of 1.125mm × 0.85mm. A microphotograph of the sensor array is shown in Fig. 5.8. Each pixel contains 22 transistors, which occupies 15×15μm^2 with a fill factor of 32.4%. Table 2.1 summarizes the characteristics of the proposed design.

Experimental Results

During the testing, a photograph slide is projected on the pixel array. Sample images captured in video mode without compressive sensing are shown in Fig. 2.9. In

Table 2.1: Summary of the measured performances

Process	0.18μm
Die Size	$1.125 \times 0.85\text{mm}^2$
Power supplies	3.3V/1.8V
Pixel Array	48×72
Pixel Size	15 $\mu m\times$ 15 μm
# of transistors	22/pixel
Fill Factor	32.4%
Pixel Dynamic Range	$>$ 100dB
Power Consumption	1.56mW @ 23fps
Compression Ratio	$>$ 10x
Frame Rate	up to 90fps

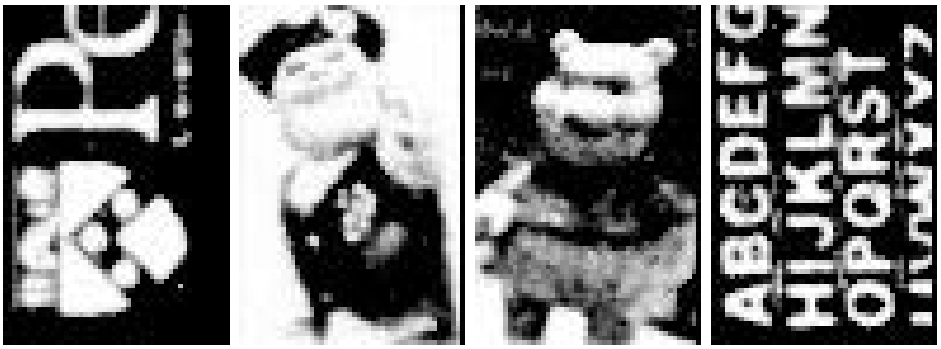


(A) (B)

Figure 2.8: (A) Chip photograph (size of 1.125mm × 0.85mm), and (B) pixel layout ($15\times15\mu m^2$).

video mode, the image sensor demonstrates the capability to capture images with complex shapes and fine details despite its small array size. Sample images captured with compressive sensing are illustrated in Fig. 2.10, where Fig. 2.10 (A) shows the raw compressed images and Fig. 2.10 (B) shows the reconstructed images from (A). The reconstruction of the image is performed off-line. Fig. 2.11 illustrates the captured compressed images and reconstructed images under a 10MHz system clock generated from an external FPGA for the readout timing control. 256 gray level image is captured under compressed acquisition mode for each sample. A frame rate of near 23fps can be achieved. A compression ratio is calculated according to the ratio between the total number of the pixels in the array and the total number of the sampled selected pixels. A compression ratio higher than 10x is achieved in the illustrated examples for views of a single character. More sampling points will help

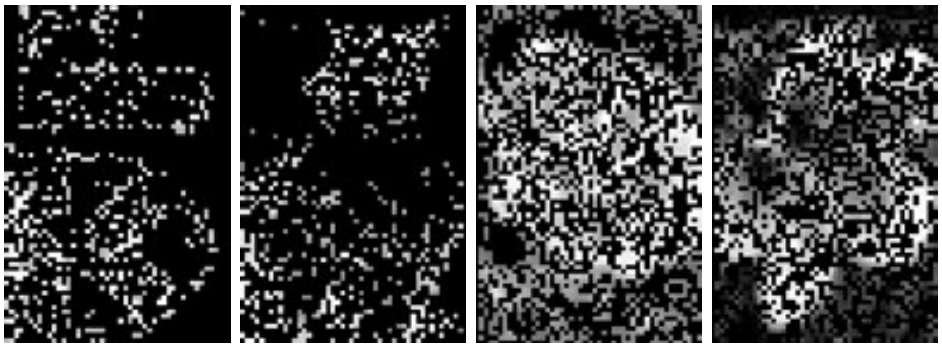
to improve the quality of the reconstructed images as shown in Fig. 2.12.



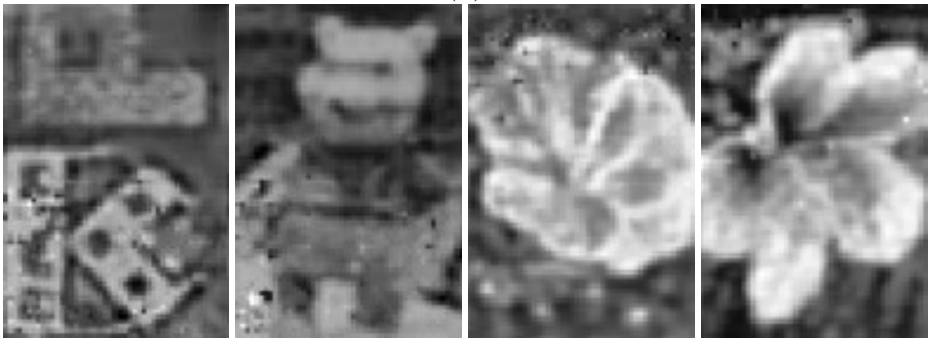
(A)

Figure 2.9: (A) Sample images captured without compressive sensing.

In order to evaluate the performance of the image sensor, an optical setup has been built as shown in Fig. 2.13, with help from Dr. Brian Edwards from Department of Electrical and Systems Engineering at University of Pennsylvania. A variable metallic Neutral Density (ND) filter is used to control the intensity of the incident light. A beamsplitter splits the incident beam of light into two. A fixed proportion of one of the two beams is applied to a powermeter for a quantitative evaluation of the incident light intensity. 100 pixels located in a 10×10 region are selected for this test. The image sensor is configured for single pixel mode. For this mode, the total number of clock cycles that one pixel takes to generate a request is recorded. For pixel performance measurements, a higher frequency system clock, 40MHz, is used during the testing. An average request time of all the 100 test pixels is calculated for each measured intensity, as illustrated in Fig. 2.14 (A). The incident power is normalized by the maximum power used during this test. In Fig. 2.14 (A), the

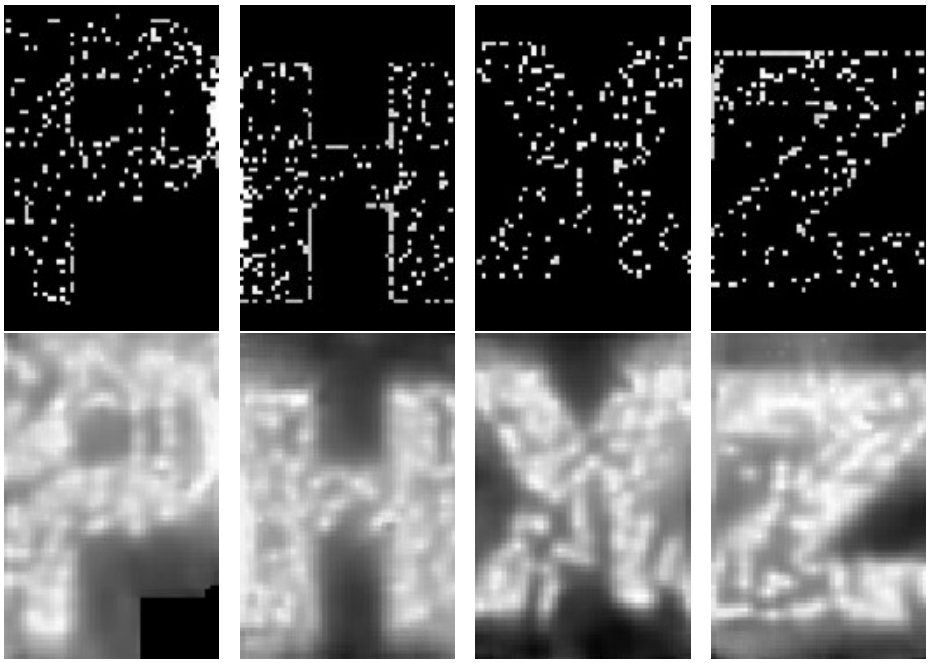


(A)



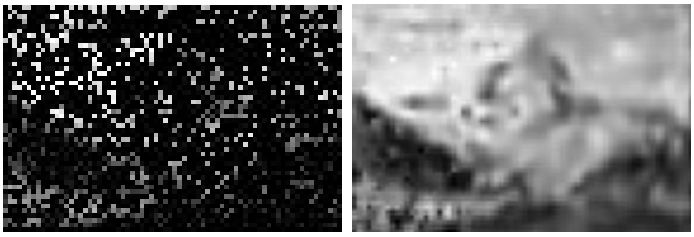
(B)

Figure 2.10: (A) Raw sample images captured with compressive sensing. (B) Sample images reconstructed from corresponding captured as shown in (A). N-continuous-pixel-one-iteration mode is used. And N is assigned to 7.

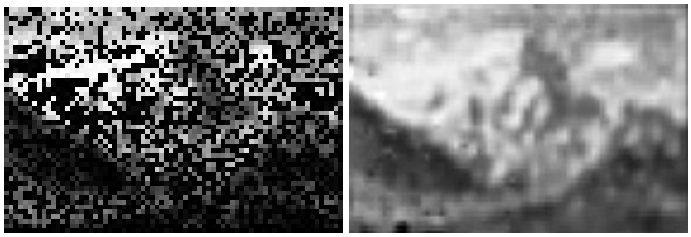


(A) 13.94:1 (C) 11.92:1 (B) 17.19:1 (D) 14.34:1

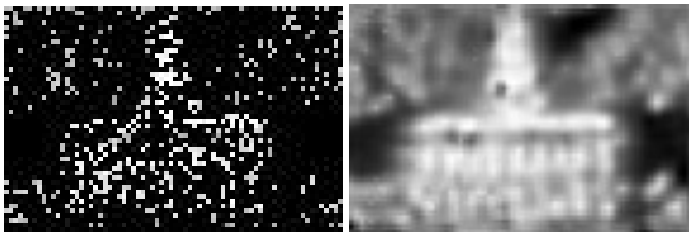
Figure 2.11: Sample images captured under compressive sensing mode, and the corresponding reconstructed results from the captured samples. The compression ratio is listed under the figures.



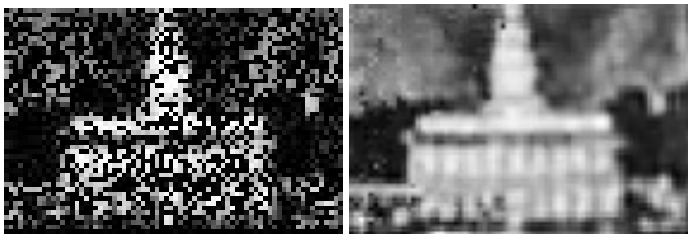
(A) 4.47:1



(B) 2.10:1



(C) 7.05:1



(B) 2.27:1

Figure 2.12: Reconstructed images with different compression ratios.

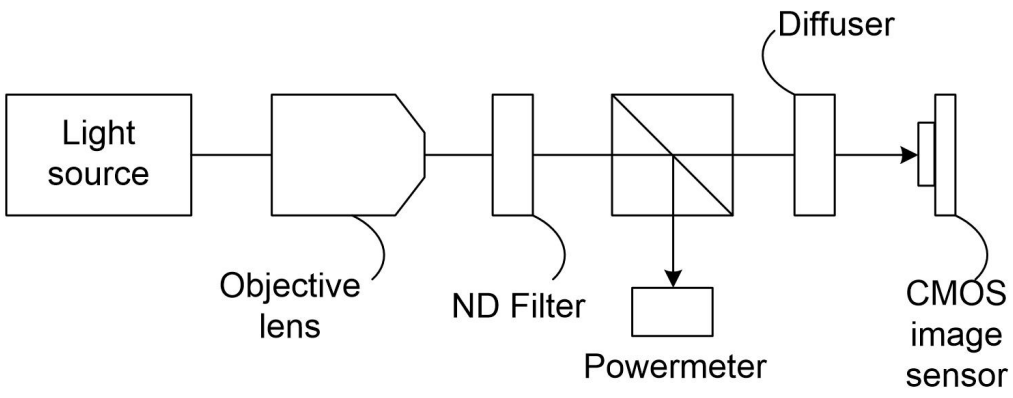
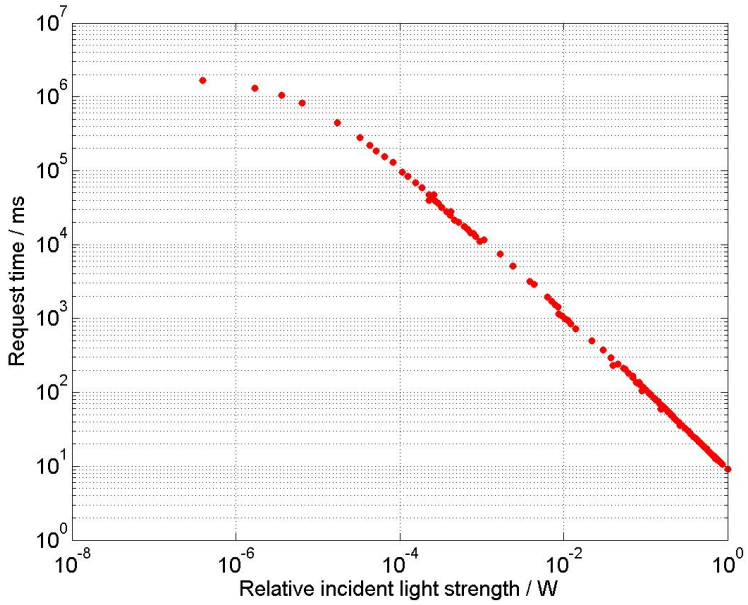


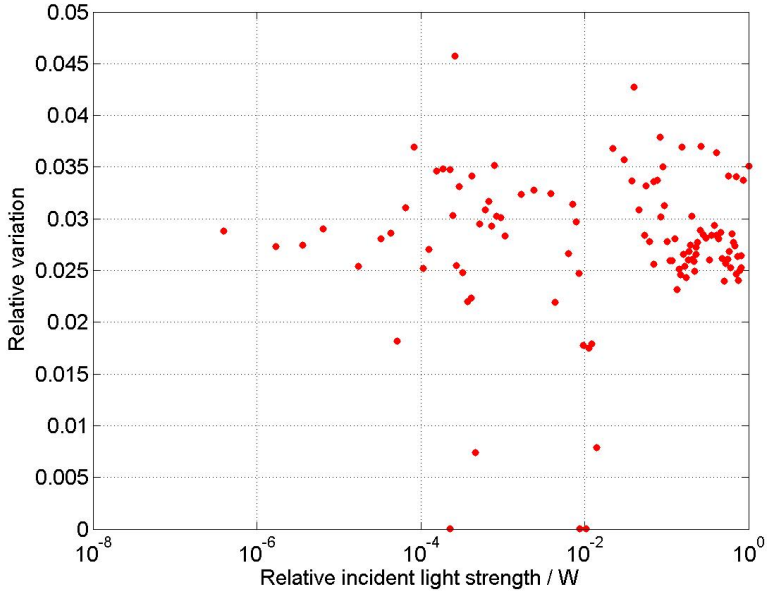
Figure 2.13: Optical test setup for the evaluation of the response of the image sensor to different incident light intensities. A beamsplitter is used to split the incident beam of light into two. A fixed proportion of one of the two beams is applied to a powermeter for a quantitative evaluation of the incident light intensity.

lowest tested relative incident light strength is below 10^{-6} W, where the request time is constant with indicent light strength. This shows the noise level of the pixels. From 10^{-6} W to 10^{-5} W, the curve is non-linear due to non-linearity response of the pixels and circuits. From 10^{-5} W to 10^{0} W, a linear relationship can be observed between the request time and the relative incident light strength. This defines the dynamic range of the pixels. A dynamic range of 100dB is achieved. According to the measurement, the fastest request is measured at 337th clock cycle after the reset of the pixel. A higher dynamic range can be achieved if brighter incident light can be applied to the image sensor.

A standard deviation of the recorded request times for all the pixels under the



(A)



(B)

Figure 2.14: (A) Average requests generating time, and (B) relative variation error of the test pixels while the strength of the incident light increases. The incident power is normalized by the maximum power used during this experiment.

same incident light intensity is calculated and normalized by the average request time of the test pixels, as shown in Fig. 2.14 (B). A variation of about 3% is derived from the analysis.

Statistical results on the distribution of the recorded requests are shown in Fig. 2.15 for different request times, which is corresponding to incident light intensities (according to Fig. 2.14 (A)). During each test round, the same incident intensity is applied to the entire array. Half of the image array is turned off. Only requests from the lower 48×36 pixels are taken into account. A histogram of the statistic of the request time generated from each pixel during each round is shown in Fig. 2.15. The fixed-pattern noise experiment results show that the standard deviation of FPN in dark is 3.5% with an average exposure time of 7.44×10^7 clock cycles.

2.1.5 Conclusion

A prototype imager is implemented and successfully tested, which combines the advantage of compressive sensing and AER image sensor into an all-digital address event triggered compressive acquisition image sensor. All the compressive processing is performed during the image capture phase, which eliminates the data converters and also reduces the workload of the readout circuits.

The image array can work under both video capture mode and compressive sensing mode. Under image acquisition mode, a higher than 100dB dynamic range is measured with a relative variation of around 3%. Under compressive sensing mode,

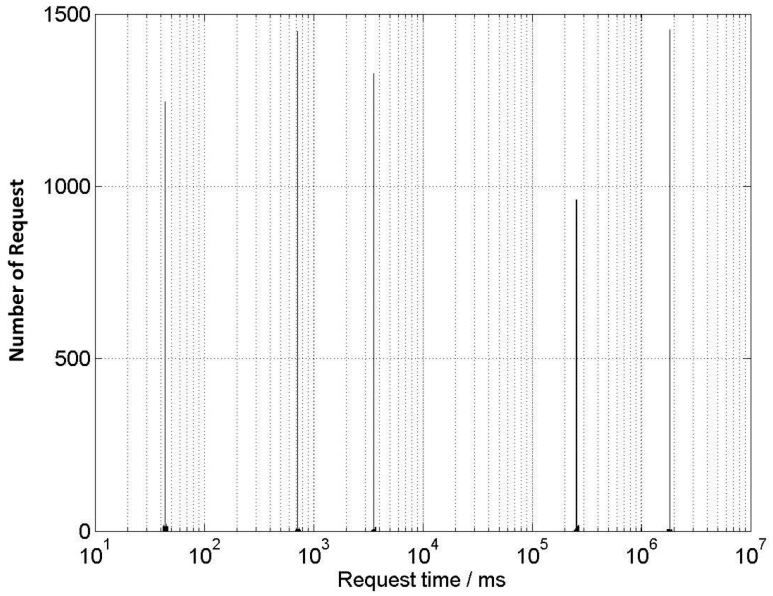


Figure 2.15: Histogram plot of the request time under different request times.

a "winner-take-all" strategy is applied to record requests from selected pixels; the image can be reconstructed off-line with a compression ratio higher than 10x. The 48×72 pixel image sensor was fabricated in 0.18um standard CMOS technology, featuring a 22-transistor all-digital pixel architecture with a size of $15\times15\mu m^2$ and a fill factor of 32.4%. It consumes 1.56mW at 23fps or 5.48mW at 90fps, both in compressive sensing mode. The all-digital nature of the proposed pixel design guarantees its scalability with future CMOS technologies that provides smaller size.

The proposed design has advantages in low data throughput rate over the traditional CMOS image sensors. It is more power efficient in applications with wireless transceivers in wireless sensor nodes for Internet of Things. The all-digital

nature of the proposed image sensor also allows easier transferability to more advanced CMOS fabrication technologies, in which power consumption will also be scaled.

2.2 Optical Force Sensor

2.2.1 Introduction

Force sensors with high sensitivity have gained great interest in recent years due to their potential applications in touch screens, electronic skins, and medical diagnostics, etc. [95][96][97]. Compact size, high precision, and low cost are needed in most applications.

Micro-Electro-Mechanical Systems (MEMS) are one of the most fast growing technologies in the miniaturized force sensor market in recent years [98][99]. However, MEMS sensors usually require using specialized micro-fabrication processes [100] [101] [102] [103] [104] [105] [106] [107], which have high cost and small scale. More and more MEMS sensors are designed based on standard CMOS technology to address the cost and scalability issues [108] [109] [110] [111] [112] [113], but post-CMOS-fabrication processing in a micro-fabrication facility is requested. The design of standard-CMOS technology compatible force sensors is challenging.

Polymer-based optical force sensors have advantages over other types of force sensors, including insensitivity to electronic noise and ease to scale. Elastomeric

polydimethylsiloxane (PDMS) is typically used as the compressible optical cavity or waveguide. In [114], the authors introduced the optical device combining two plastic optical fibers and PDMS showing good pressure sensing resolution of about 1kPa. The optical pressure sensor comprised of a PDMS waveguide integrated with polymer organic light emitting diodes (OLED) and a polymer organic photodiode as the light source and photodetectors [115] demonstrated very high sensitivity ($0.2kPa^{-1}$) and tolerance to bending.

Thanks to advancements in silicon light emitting devices (Si-LED) in standard CMOS technology [116] [117] [118] [119] [120] [121] [122] [123], an optical waveguide becomes feasible in standard CMOS technology. Combined with the advantages of the polymer-based optical force sensor, a standard-CMOS compatible optical force sensor has been designed and will be presented in this thesis. The force sensor consists of a piece of inverse-lenticular patterned PDMS material and a standard-CMOS optical waveguide which consists of an Si-LED, a silicon dioxide (SiO_2) optical waveguide channel and a photodiode (PD), as shown in Fig. 2.16. As demonstrated in Fig. 2.17, the optical channel has a CMOS LED on one end, a light-guide channel in the middle and a 3T-photodiode on the other end.

2.2.2 Design of the Optical Force Sensor

The PDMS material is made with a flat surface at the top side and inverse-lenticular structures at the bottom side. The PDMS (sylgard 184 kit, Dow Corning Co.) was

composed of a 1:10 mixing ratio of curing agent. The PDMS mixture was cast on a polystyrene lenticular lens board with a pitch of 20μm. After degassing for 30 minutes, the PDMS mixture and lenticular lenses molds were cured for 3 hours at 65°C. Finally, the PDMS membrane was carefully peeled off from the mold. The patterned PDMS material is fabricated with the help from Dr. Dengteng Ge, a Post Doctoral research fellow from Dr. Shu Yang's group in Material Science and Engineering Department at University of Pennsylvania.

In operation, the LED emits light into the SiO_2 optical waveguide channel on the CMOS chip. A certain amount of light is totally internally reflected at the top interface of the chip and reaches the photodiode on the other end of the waveguide. By placing the PDMS material on top of the SiO_2 with the inverse-lenticular structured surface facing the waveguide channel, little totally internally reflected light escapes from the channel, since the contact area between the PDMS and the SiO_2 is minimal with no force applied on the PDMS material. As illustrated in Fig. 2.18, when force is applied to the PDMS material, the inverse-lenticular structure deforms, and hence the contact area between the PDMS and the SiO_2 is increased. More light in the optical waveguide channel excapes from the channel. Therefore, less light reaches the photodiode and the exposure of the photodiode decreases. The amount of photodiode exposure and the deformation of the PDMS inverse-lenticular structure changes monotonically with applied force.

The CMOS chip consists of the optical waveguide and an SAR ADC, which is

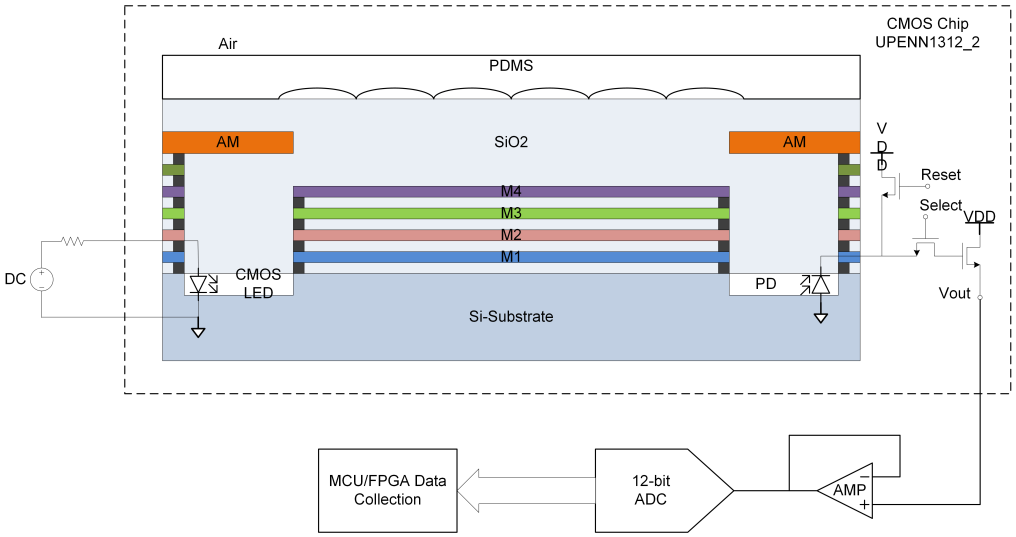


Figure 2.16: System view of the optical force sensor. (Layer Mi: metal layer i; layer AM: top metal layer.)

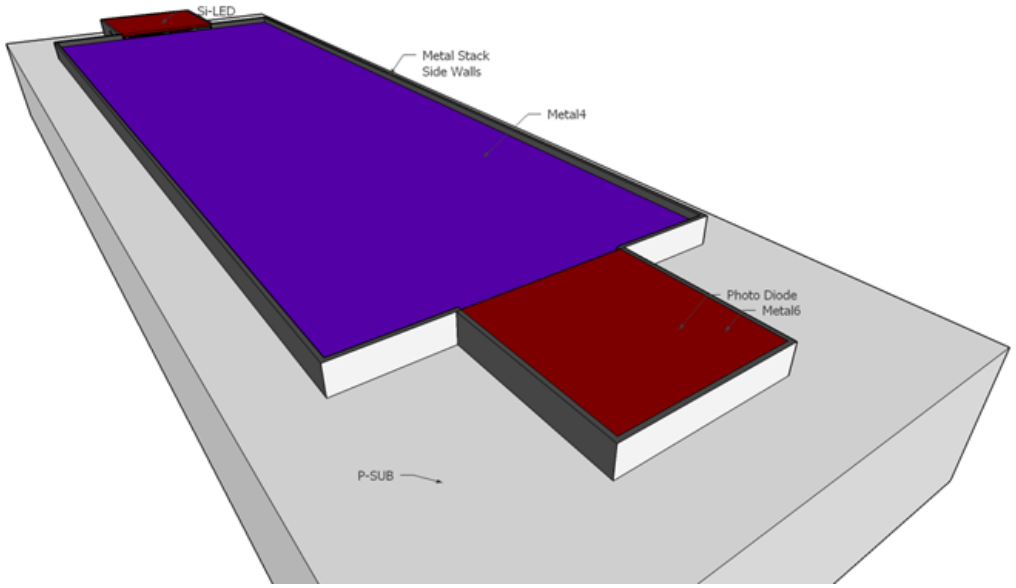


Figure 2.17: 3-dimension view of the optical channel

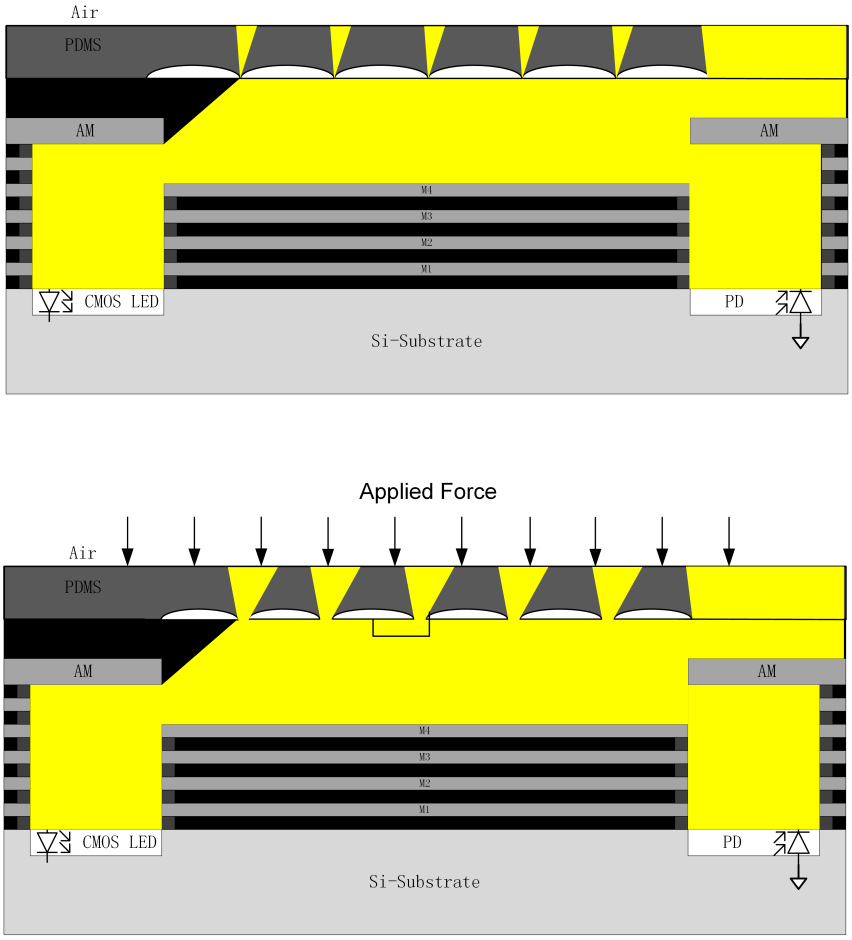


Figure 2.18: Operating mechanism of the optical force sensor. Geometry not drawn to scale.

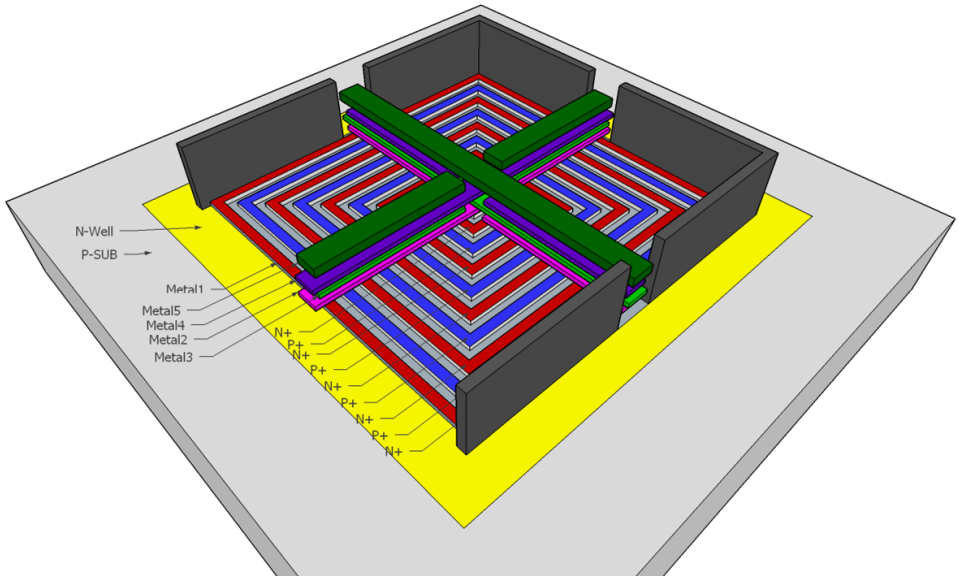


Figure 2.19: 3-dimension view of the silicon LED

implemented using the IBM 0.18μm 1P6M standard CMOS process. The silicon LED on one end of the optical waveguide has a size of 80μm by 80μm using interdigitated P+ N+ rings inside an N-well, as shown in Fig. 2.19. The photodiode on the other end of the optical waveguide also has a size of 80μm by 80μm. The photodiode is designed using a traditional 3-transistor pixel structure. The SiO_2 optical waveguide channel has a size of 200μm by 600μm. The sidewalls of the LED, the photodiode and the waveguide channel are shielded by stacked metal layers and vias for minimum light leakage through the sidewalls. The bottom side of the optical waveguide channel is elevated to metal 4 layer. This can effectively prevent the light from being absorbed by the silicon substrate under the channel. It also reduces the path length of totally internally reflected light traveling inside the channel by reducing

the thickness of the SiO_2 layer in the channel, which effectively reduces the light loss at reflections. The SAR ADC is designed to achieve a 12-bit resolution and a 1MS/s sampling rate. The details of the SAR ADC design is presented in Chapter 3 - Front-End Circuit Design. Fig. 2.20 shows the layout of the fabricated optical waveguide channel in the IBM 0.18μm 1P6M standard CMOS process.

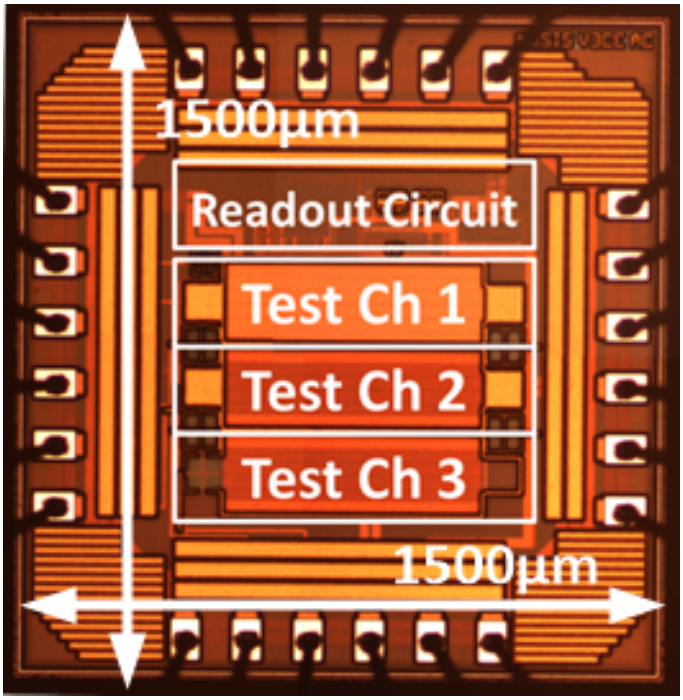


Figure 2.20: Layout of the optical force sensor chip

2.2.3 Experimental Results

The optical power and electric-to-optical conversion efficiency of the Si-LED is experimentally investigated. Fig. 2.21 shows the input electric power and output optical power of the Si-LED. The LED turns on by reverse-biasing the P+N+

junction to around 11V. The device has stable performance with the reverse-biasing voltage up to 18V. The electrical power is in the mW range while the optical power is in the nW range. Due to the indirect-band nature of silicon, most of the carrier recombination generates heat and only a small portion of the recombination generates photons. As shown in Fig. 2.22, the electrical-to-optical conversion efficiency of the Si-LED is at 10^{-7} to 10^{-8} level. Although the efficiency is low, the Si-LED does give out enough light to be visible to the naked eye in normal in-door lighting conditions. The intensity of the emitted light is also enough for the operation of the optical force sensor.

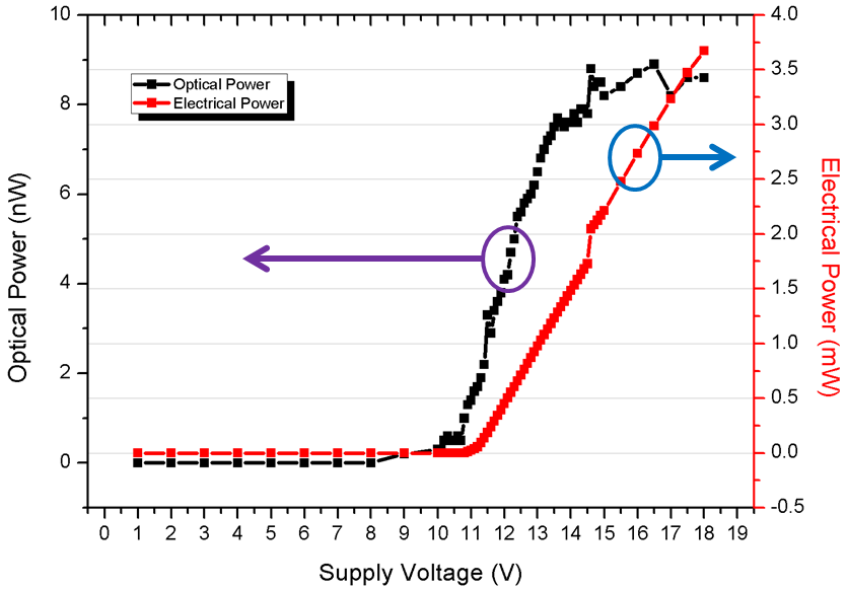


Figure 2.21: Electric and optical power of the silicon LED

Fig. 2.23 shows the performance test of the CMOS optical waveguide without the patterned PDMS material on top. With increasing light intensity from the Si-LED, the photodiode is discharged faster. The full sensor experiment results are

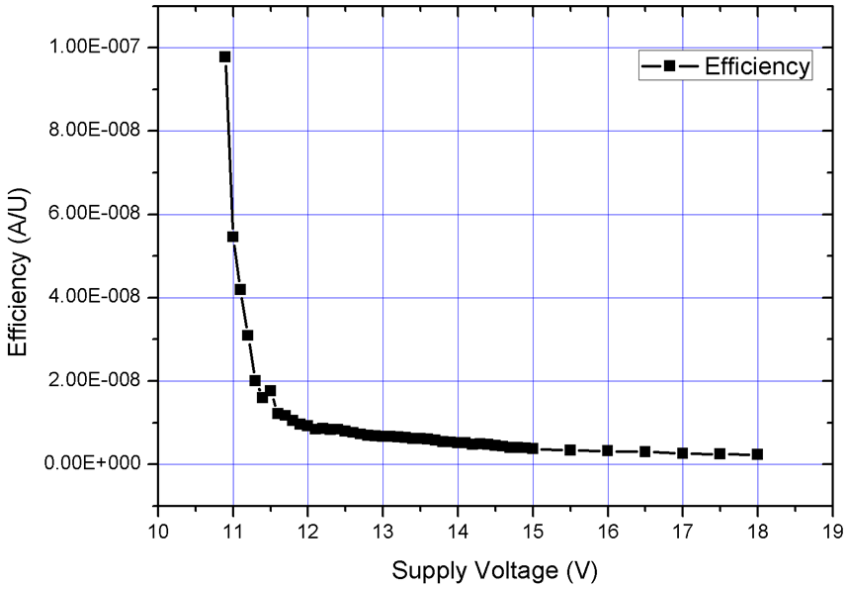


Figure 2.22: Electric-to-optical conversion efficiency of the silicon LED

presented in Fig. 2.24. The results show that the photodiode receives more light and discharges faster both when no PDMS material is placed on top of the waveguide and when no force is applied to the PDMS material on top of the waveguide. When force is applied to the PDMS material on top of the waveguide, the photodiode is exposed much more slowly, indicating more light is extracted by the PDMS from the waveguide.

Fig. 2.25 shows the response of the sensor with applied force ranging from 0N to 0.87N. The sensor shows monotonic and highly linear response to applied force in the range from 0.1N to 0.87N, which exhibits a linear regression R^2 value of 0.9892. The linearity of the sensor could be further improved by employing a lookup table (LUT) digital calibration. Given the 10.6 bits ENOB of the ADC, the sensitivity of the sensor is 0.00144N, corresponding to 2.25kPa with the 800μm $\times$ 800 μm PDMS

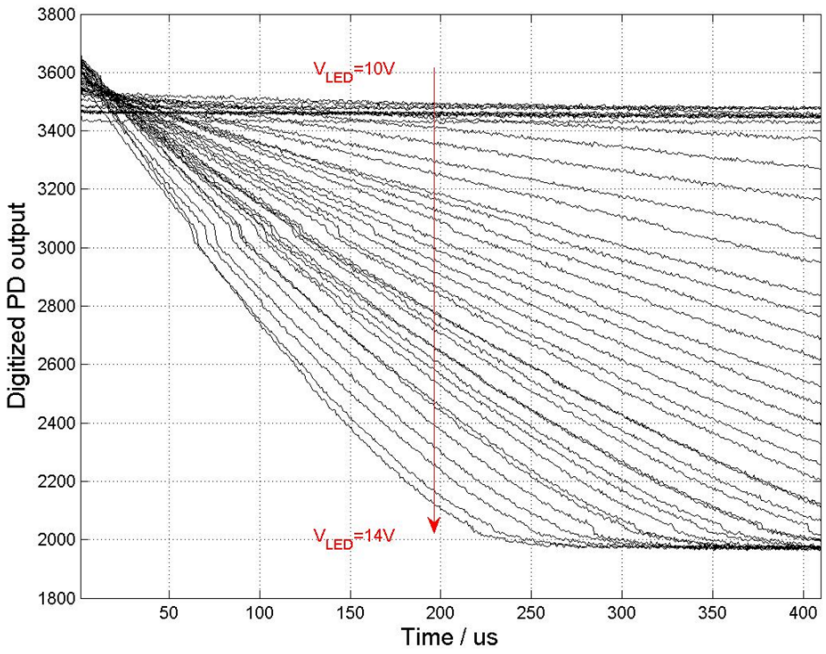


Figure 2.23: Experimental response of the optical channel for different reverse bias voltages of the SiLED.

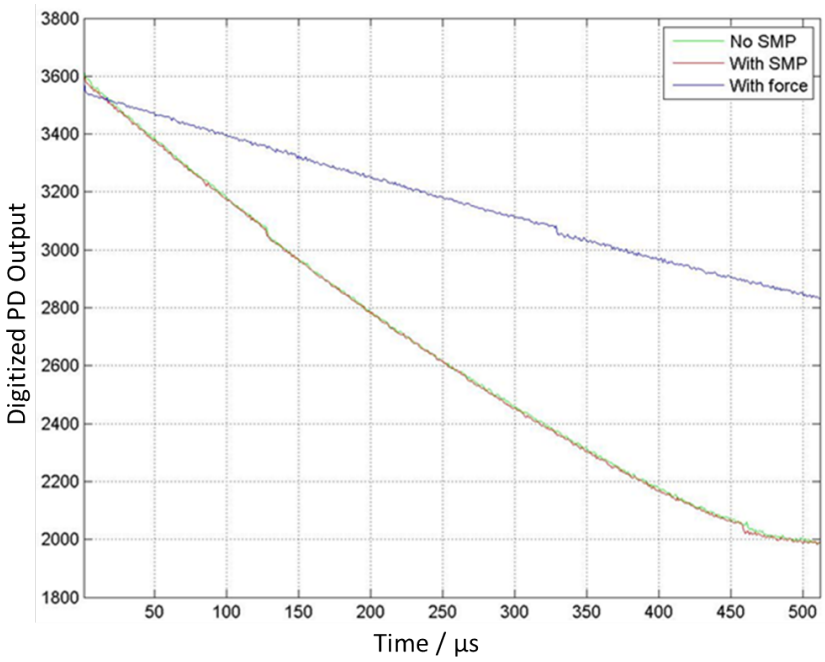


Figure 2.24: Measured sensor response: digitized photodiode voltage with respect to applied force. The photodiode discharges faster when no PDMS film sample (SMP) is present and when no force is applied to the PDMS SMP on top of the optical waveguide channel. The photodiode discharges much more slowly as a result of more light escaping from the waveguide when force is applied to PDMS SMP.

membrane area.

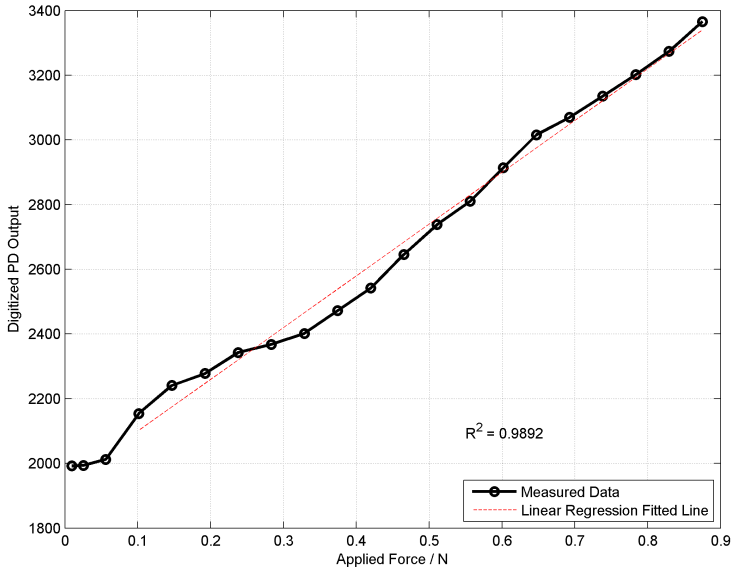


Figure 2.25: Measured sensor response: digitized photodiode voltage with respect to applied force. Linearity of the force sensor is given by the fitted regression line R-squared value of 0.9892 over an applied force range from 0.1N to 0.87N.

The optical force sensor is optimized for its sensitivity and its manufacturability. The sensitivity is mainly determined by the mechanical properties of the PDMS sample and the inverse-lenticular structure on it. It is worth noting that in mechanical stress simulation, the inverse-lenticular structure has the largest amount of deformation under the same applied force when compared with triangular strips, rectangular strips, as well as lenticular strips. The manufacturability and compatibility of the proposed optical force sensor are achieved by fabricating the device using standard

CMOS process. In addition to the CMOS chip, only a low-cost, simple-to-fabricate PDMS layer is required for the sensor. When compared with MEMS sensors, which require post-fabrication processes in a nano-fabrication facility, the proposed CMOS compatible sensor is clearly advantageous in terms of cost, yield, ease of use, and integrability with CMOS signal analysis and processing circuits into large systems.

2.2.4 Conclusion and Future Work

An optical pressure sensor using a piece of PDMS material on top of a standard-CMOS optical waveguide is presented. The optical waveguide has a Si-LED on one end, a SiO_2 optical waveguide channel in the middle and a 3T-photodiode on the other end. The force-induced deformation of the inverse-lenticular structure of the PDMS material extracts light out of the optical waveguide. Experimental results show that the exposure of the photodiode is inversely proportional to the force applied to the PDMS material.

Future work for the proposed optical force sensor includes detailed analysis of sensitivity by using different structures on the PDMS material and the effect of the pitch of the structures.

2.3 Passive Scattering Force Sensor

2.3.1 Introduction

Low-power sensors, wireless-powered sensors, and passive sensors have always been desired in the wireless sensor node and the wireless sensor network. Especially in biomedical applications where wireless sensor nodes are attached or implanted in animal or human subjects, low-power sensing significantly extends the battery life of the wireless sensor nodes, while wireless-powered and passive-responsive sensing offers unlimited operation time, enabling long term monitoring without changing batteries.

In recent years, passive radio-frequency back scattering tags have been successfully used in radio-frequency identification (RFID) technology [124] [125] [126] [127] [128]. The space-filling curve, thanks to its compact size and its narrow bandwidth of frequency response, is widely used in the design of passive scattering tags [129]. The peak scattering frequency of a space-filling-curve tag is very sensitive to the dimension of the tag. This makes the space-filling-curve tag a good candidate for a force or stretch sensor. With the recent advancements in liquid metal antenna research [130] [131] [132] [133], the implementation of a passive scattering force/stretch sensor is made possible by using a flexible liquid-metal-filled space-filling-curve tag.

In this section, a wireless passive scattering force sensor node is proposed, designed and tested. The sensor node takes advantage of the backscattering frequency response

of space-filling-curve tags. In each passive scattering sensor node, a 2nd-order Hilbert-curve tag [129] is used for sensor node identification, while another 2nd-order Hilbert-curve tag is used for force sensing. This sensor network is primarily designed for human finger tactile sensing as part of the paralyzed limb sensory restoration project. The proposed sensor node can also be adapted for other applications such as building structure monitoring.

2.3.2 Design of the Passive Scattering Force Sensor

The space-filling-curve tags, shown in Fig. 2.26, act as microwave backscattering objects. The major advantages are: 1) completely passive response by backscatter microwave energy; 2) compact size compared with other antennas at the same resonant frequency; 3) resonant frequency more sensitive to size change than that of dipole antennas.

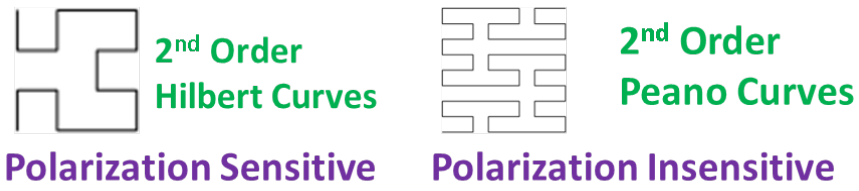


Figure 2.26: Space filling curves: (left)2nd-order Hilbert curve, (right) 2nd-order Peano curve

A 2nd-order Hilbert curve is used to implement the proposed wireless sensor node because of its simple geometry and ease of fabrication. As shown in Fig. 2.27, the

Hilbert-curve tag is sensitive to the polarization of the incident microwave because it is symmetrical about a line. When the incident electric-field polarization is along the axis of symmetry of the Hilbert curve, we define the position of the tag as in the polarization direction, also known as i-polarization. Similarly, when the incident electric-field polarization is perpendicular to the axis of symmetry of the Hilbert curve, we define the position of the tag as quadrature to the polarization direction, also know as q-polarization. The incident microwave induces current in the segments of the 2nd-order Hilbert-curve tag, which are laid along the polarization of the incident electric-field, as shown in Fig. 2.27. The longest path along which the induced current can pass defines the electrical lengths of the tag. The electrical length further determines the resonant frequency of the tag. For tags placed in the i-polarization position, the induced current is always 0 at the symmetry point, so the electrical length is half of the total trace length. On the other hand, for tags in the q-polarization position, the induced current does not have to be 0 except at the physical ends of the tag trace. Therefore, the electrical length is the full trace length. This also indicates that the resonant frequency of a 2nd-order Hilbert-curve tag in i-polarization should be about twice as high as that of a tag with the same size in q-polarization, as illustrated in Fig. 2.28.

In a wireless sensor network, there should be the capability for multiple sensor nodes. Since the passive backscattering tags only have changes in their frequency response, multiple access and spectrum reuse should be designed. In the proposed

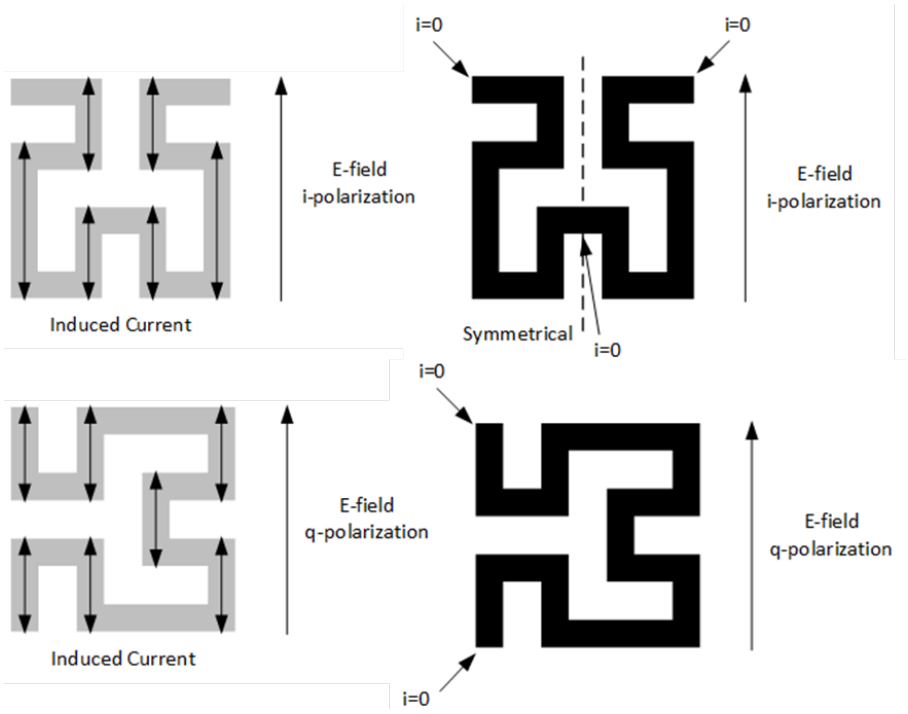


Figure 2.27: Resonance mechanism of a 2nd-order Hilbert curve

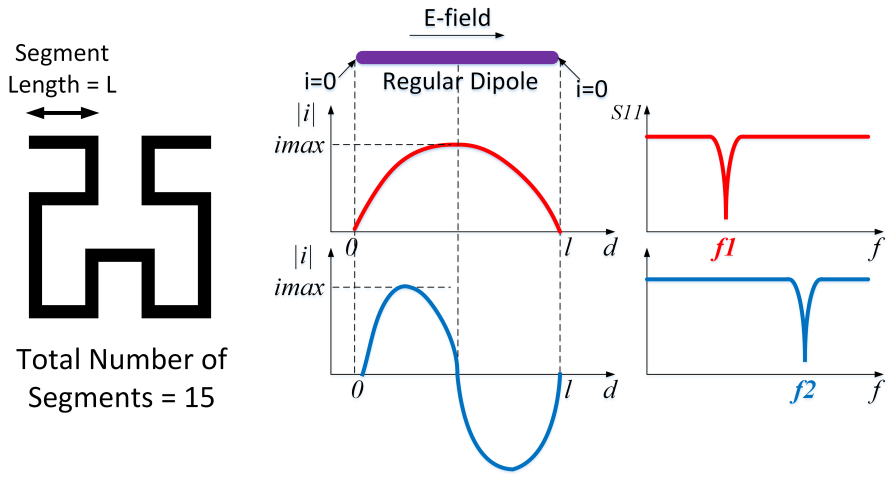


Figure 2.28: Resonance mechanism of a 2nd-order Hilbert curve

wireless sensor node design, a combination with time-division multiple access (TDMA) and frequency division-multiple access (FDMA) is used to expand the network capacity.

The spectrum allocation for the sensor node is shown in Fig. 2.29. In each sensor node, there is a fixed-shape ID tag implemented with a 2nd-order Hilbert-curve tag. The ID tag has its unique resonant frequency. Each sensor node has a different ID tag with a different size, so the resonance of the ID tags in the sensor nodes can be easily selected by radiating the corresponding resonant frequency onto the ID tags. As shown in Fig. 2.30, the ID tag is connected to a microwave-to-DC converter implemented with voltage multipliers. The microwave-to-DC converter turns the resonant current of the selected ID tag into a DC voltage to drive a low-power switch. The switch is connected at the mid-trace point of the sensing tag, which is implemented using a flexible 2nd-order Hilbert curve tag. When the switch is turned on, the resonant frequency of the sensing tag falls into the sensing spectrum. When the switch is turned off, the resonant frequency of the sensing tag goes to twice the frequency of the sensing spectrum. Each time only one sensor node is selected, so there will only be one sensing tag responsive in the sensing spectrum. A sweeping frequency stimulus in the sensing spectrum is radiated onto the sensing tag to determine its resonant frequency.

The microwave-to-DC converter, the switch and the sensing tags in every sensor node in the network are the same. This simplifies the fabrication of the wireless

sensor nodes, since the circuits and the sensing tags are more complicated to make than the ID tags. As shown in Fig. 2.29, the ID spectrum is allocated at a higher frequency range than the sensing spectrum. Such a spectrum allocation avoids the situation where the sweeping frequency stimulus at the sensing spectrum may accidentally turn on some ID tags by their high-order resonant frequencies if the ID spectrum is allocated at lower frequency than the sensing spectrum. Both the ID tag and the sensing tag are placed in q-polarization position so that, for the ID tag, at the mid-trace point the resonant current can reach its maximum in the ID tag for better RF-to-DC conversion efficiency, and for the sensing tag, at the mid-trace point the switch can control the resonant frequency. Fig. 2.31 shows the picture of a sample of the passive scattering wireless sensor node.

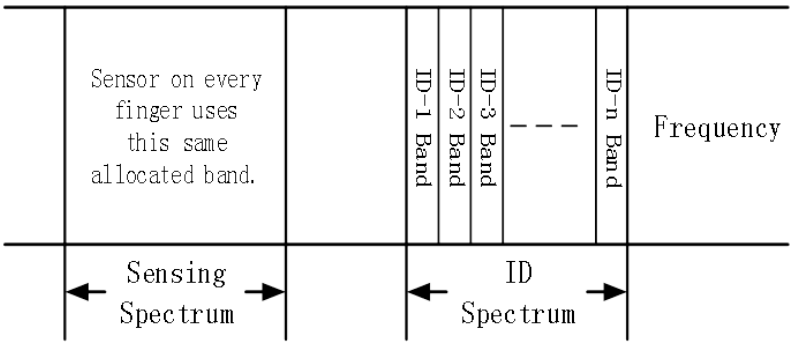


Figure 2.29: Spectrum allocation of the passive scattering wireless sensor node

The sensing tags should be made flexible so physical force applied to the sensing tag causes the dimension change of the tag and hence the resonant frequency change. The sensing tag in the proposed wireless passive scattering sensor node is designed

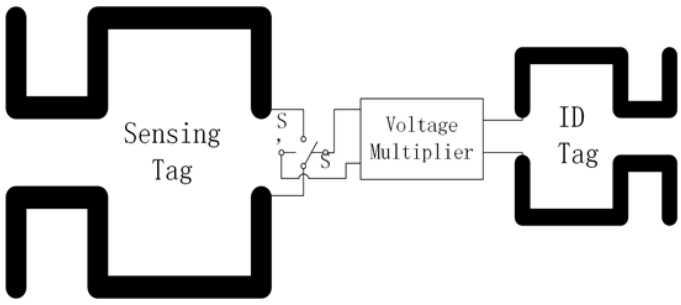


Figure 2.30: Schematic of the passive scattering wireless sensor node

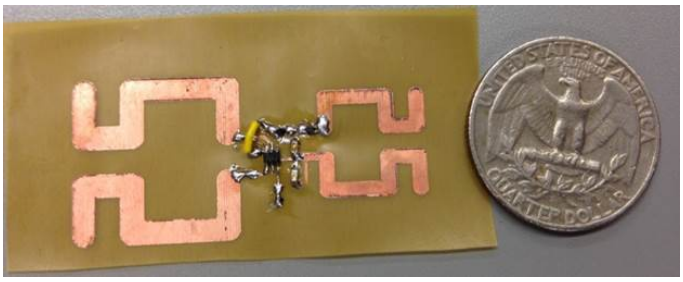


Figure 2.31: A picture of a sample of the passive scattering wireless sensor node

with the 2nd-order Hilbert-curve shape and is fabricated with GaIn liquid metal in flexible PDMS channels by Mr. Srihari Sritharan from Department of Neurosurgery, University of Pennsylvania. For force sensing, the Hilbert-curve shaped channel in the PDMS is pre-filled with the liquid metal. A force sensitive pump forces oil into one end of the channel when force is applied to the pump. The oil pushes the liquid metal in the channel to move towards a reservoir at the other end of the channel, effectively shortening the total length of the liquid metal trace.

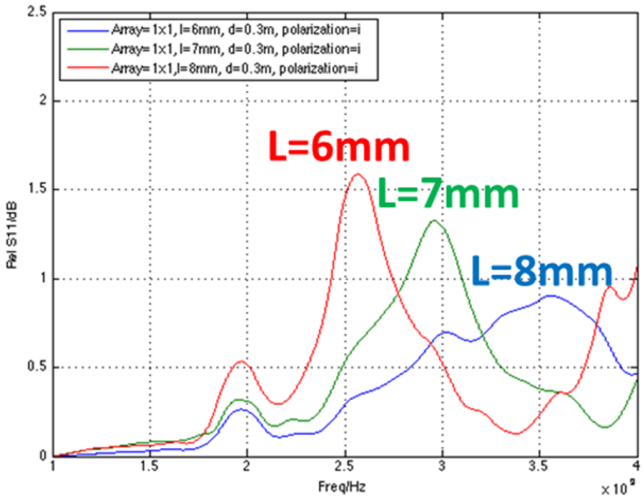
2.3.3 Simulation and Experiment Results

The simulation results presented in this section were obtained with the help from Dr. Milin Zhang, a Post Doctoral research fellow from the Department of Electrical and Systems Engineering at University of Pennsylvania. The experiments were done inside the anechoic chamber of the Antenna Research Lab at Villanova University, with the help from Dr. Christopher Thajudeen and Dr. Ahmad Hoorfar from Villanova University.

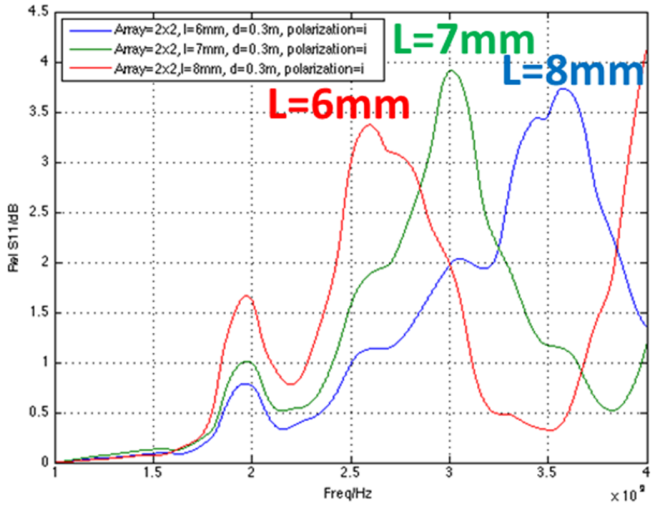
Fig. 2.32 shows the measured frequency responses of the 2nd-order Hilbert-curve tags with segment lengths (L) equal to 6mm, 7mm, and 8mm, respectively, at a distance of 0.3m away from a horn antenna, which is used to radiate the incident waves to the tags and to pick up the reflected waves. The experiments were conducted in a microwave anechoic chamber. In the top plot, the reflection frequency response peaks at 2.6GHz for the tag with L=8mm, at 3.0GHz for the

tag with L=7mm, and at 3.5GHz for the tag with L=6mm. The bottom plot in Fig. 2.32 shows the responses of 2 by 2 arrays with the 2nd-order Hilbert-curve tags where in each array the 4 tags have the same size. It is clear that the array shows stronger response in magnitude than a single tag, but the resonant frequency of each tag and its corresponding array with the same segment length stays the same. The figure also shows that the results with the single 2nd-order Hilbert-curve tags exhibit a signal-to-noise ratio large enough to distinguish the reflected frequency response of each tag. Therefore, it is feasible to use the 2nd-order Hilbert-curve tags to design and build passive backscattering wireless sensor nodes.

Fig. 2.33 shows the simulation results of the selection of the passive scattering wireless sensor node. The simulations were done in the Computer Simulation Technology (CST) Microwave Studios simulation software. In the simulation setup, a sensing tag with the mid-trace point connected is used to simulate the "switch on" scenario, while a sensing tag with the mid-trace point disconnected is used to simulate the "switch off" scenario. From the plots in Fig. 2.33, it is clear that when the switch is turned on, the resonant frequency of the sensing tag is at 1.5GHz, and when the switch is turned off, the frequency range of interest, also as know as the sensing spectrum, is free of resonant frequency of the sensing tag. Fig. 2.34 gives the measured results of the selection of the passive scattering sensor node by using the device shown in Fig. 2.31. When the switch is turned on, the resonant frequency of the sensing tag is at 1.5GHz, which agrees with the simulation results. When the



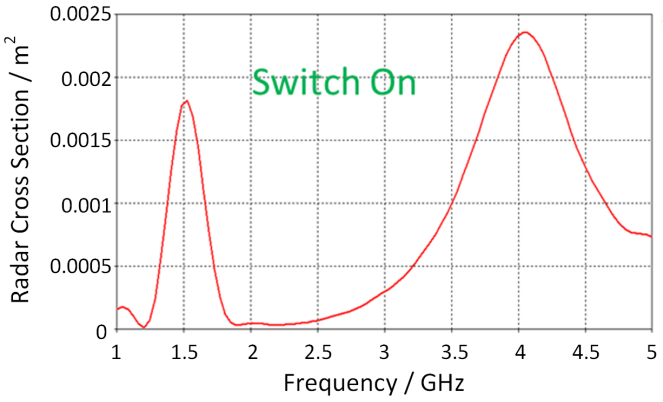
(A)



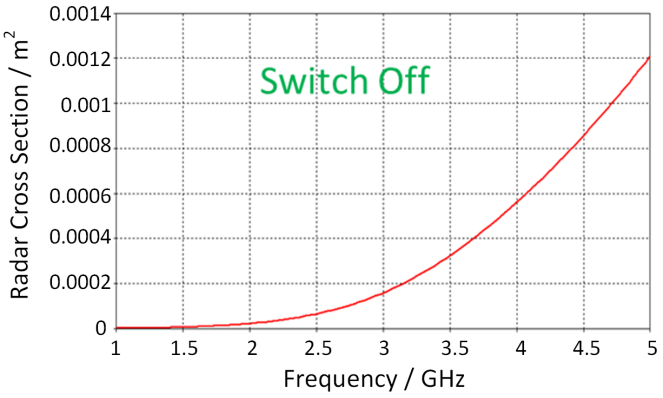
(B)

Figure 2.32: (A) Measured responses of single 2nd-order Hilbert-curve tags with different sizes. (B) Measured responses of 2×2 arrays of 2nd-order Hilbert-curve tags with different sizes.

switch is turned off, the resonant frequency is moved to 3GHz, which is twice as high as the "switch on" resonant frequency, as predicted. The left plot in Fig. 2.34 shows both the frequency response of the sensing tag when "switch on" and when "switch off". The right plot in Fig. 2.34 shows the difference between the "switch on" and "switch off" frequency responses of the sensing tag.

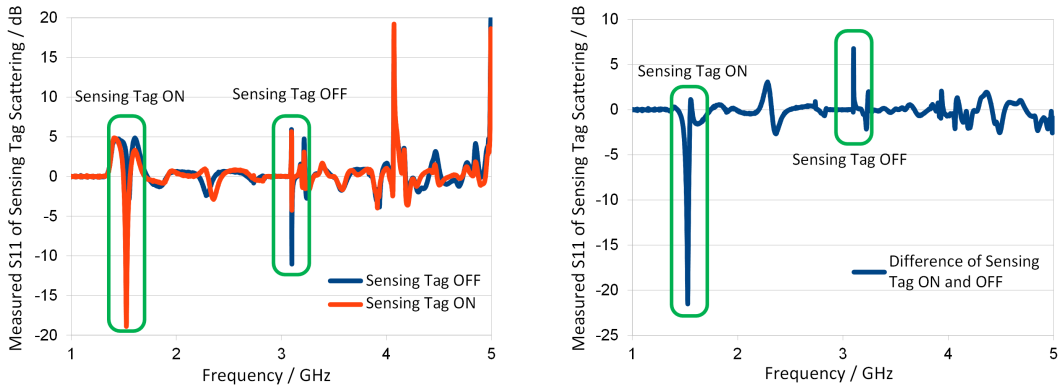


(A)



(B)

Figure 2.33: (A) Simulated radar cross section (RCS) response of the sensing tag when switched on. (B) Simulated RCS response of the sensing tag when switched off.



(A) (B)

Figure 2.34: Experimental results of the selection of the passive scattering wireless sensor node. (A) Measured S11 of Sensing tag scattering response when turned on and off. (B) The difference in the S11 response between sensing tag turned on and off.

As shown in Fig. 2.35, frequency responses are measured with sensing tags made with the liquid metal placed in q-polarization position. When 1 segment of the liquid metal is suppressed into the channel, the resonant frequency of the sensing tag is at 2.9GHz. When 2 segments of the liquid metal is suppressed in to the channel, the resonant frequency of the sensing tag is at 3.2GHz. When 3 segments of the liquid metal is suppressed in to the channel, the resonant frequency of the sensing tag is at 3.5GHz. These results prove the change of the length of the liquid metal trace results in the resonant frequency change of the sensing tag.

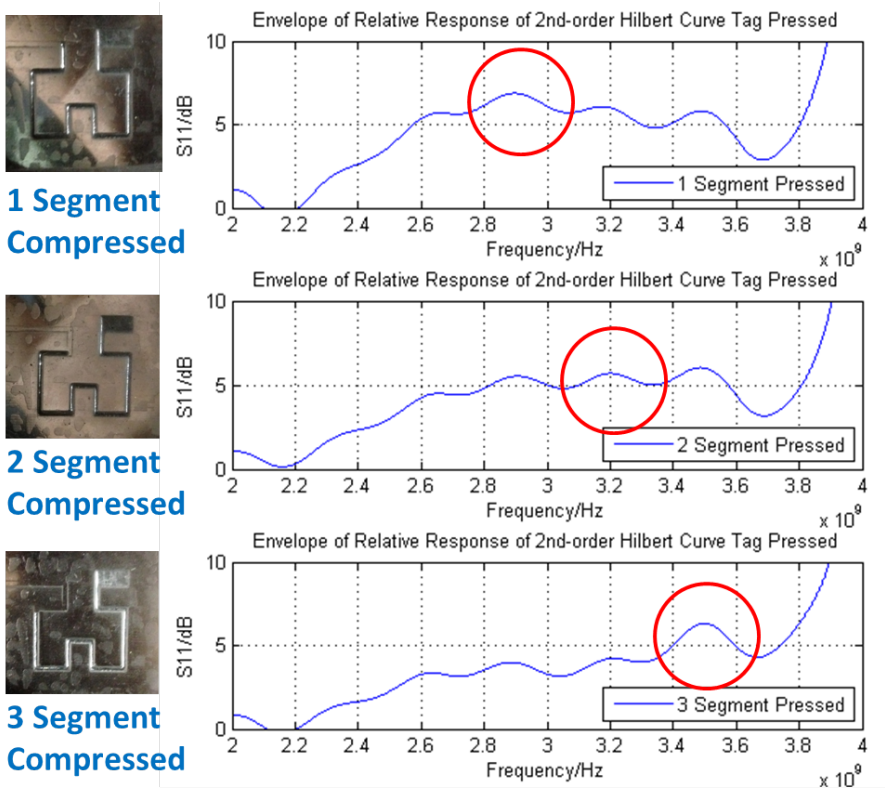


Figure 2.35: Measured responses of the 2nd-order Hilbert-curve force sensor made of GaIn liquid metal

2.3.4 Conclusion and Future Work

A wireless passive scattering force sensor node is described and tested. The sensor node takes advantage of the back-scattering frequency response of the space-filling-curve tags. In each sensor node, a 2nd-order Hilbert-curve tag is used for sensor node identification, while another 2nd-order Hilbert-curve tag is used for force sensing. Experimental results successfully demonstrated the feasibility to wirelessly and selectively turn on a sensor node by radiating the corresponding resonant frequency of its ID tag. The resonant frequency of the sensing tag on the selected sensor node is detected by a frequency sweep within the sensing spectrum. The resonant frequency of the sensing tag is then matched to the amount of force applied.

The future work on the passive scattering wireless sensor node design includes 1) complete wireless sensor node and wireless sensor network experiments; 2) further optimization of the geometry; 3) detailed characterization.

Chapter 3

Front-End Circuit Design

In a sensor network, sensors convert physical quantities into electrical signals, while front-end circuits filter, amplify and digitize the electrical signals for further processing or wireless transmission. The front-end circuits, as the first stage in the electrical signal processing chain, play an essential role in determining the noise level, bandwidth, swing and distortion of the system.

In this chapter, the design of the front-end circuit for the wireless sensor network system is presented. First, a low-noise, low-power analog front-end circuit implemented in $0.5\mu m$ CMOS technology is shown. This circuit was designed with intracranial neural signal recording in mind, as well as applications for general-purpose small signal detection. Next, a 12-bit 1MS/s successive approximation register (SAR) analog-to-digital converter (ADC) is presented. The ADC is designed for general purpose signal digitization in front-end circuits of the sensor network and is imple-

mented in $0.18\mu m$ CMOS process. Lastly, a 6-bit asynchronous level-crossing ADC implemented in $0.18\mu m$ CMOS process is presented, designed specifically for a fully event-driven wireless sensor network system.

3.1 A Low-Noise Low-Power Analog Front-End Circuit

3.1.1 Introduction

Analog front-end circuits, as the first stage in most sensor network systems, are usually desired to have low noise, low power consumption, and adequate gain. Similar features are shared with neural recording front-end circuits in brain-computer interface applications [134, 57, 135, 60, 58, 59]. For intracranial extracellular neural recording, the action potential (AP) signals range from $5\mu V$ to $500\mu V$ in a band from 100 Hz to 6kHz, while local field potential (LFP) signals can be as high as $5mV$ in sub-Hertz frequency [135, 136, 57, 137]. Therefore, the analog front-end amplifier should have input-referred noise lower than the smallest input signal of $5\mu V$. Also, the amplifier should block DC voltages to prevent output saturation by large input voltage drifts at low frequencies. A voltage gain that maximizes the signal swing at the amplifier's output is also desired to utilize the full input range of the ADC.

For the ADC, as the input signal has a dynamic range of 60dB ($5\mu V$ to $5mV$), a

minimum of 10-bit resolution is needed. By Nyquist sampling theorem, a sampling rate of at least 20k Sample/s (S/s) is needed to capture the 10kHz signal band without aliasing. As a result, the SAR ADC architecture is selected to balance the resolution, speed, and power consumption of the ADC [138].

In this section, the design of a low-noise, low-power analog front-end chip is presented. The chip integrates four channels of amplifiers and a 12-bit 1MSample/s SAR ADC. The front-end chip was fabricated using ON Semiconductor 0.5μm standard CMOS technology.

3.1.2 Low-Noise Low-Power Amplifier Circuit Design

The architecture of the amplifier design is illustrated in Fig. 3.1, which consists of a band-pass, low-noise, low-power input stage amplifier and a low-pass second stage amplifier. In order to maximize the signal swing fed to the ADC input, the overall voltage gain of the amplifier is chosen to be 54dB (500×), which gives a maximum output swing of $5mV_{pp} \times 500 = 2.5V_{pp}$. The first stage low-noise amplifier provides 40dB voltage gain to guarantee low input-referred noise and the second stage contributes 14dB voltage gain. The mid-band gain of the first stage amplifier is determined by the capacitance ratio between the input capacitor and the feedback capacitor as $\frac{C1}{C2}$. The gain of the second-stage amplifier is determined by the resistance ratio of the feedback resistors as $\frac{R_1+R_2}{R_1}$.

The design of the first stage amplifier is adopted from the neural amplifier by R.

Harrison [57]. The low-frequency cut-off ω_L can be calculated as

$$\omega_L = \frac{1}{2r_{inc}C_2} \tag{3.1.1}$$

where r_{inc} is the incremental resistance of the pseudo resistors, realized by diode connected PMOS transistors. When C_1, $C_{L1} >> C_2$, the high-frequency cut-off ω_H can be estimated as follows

$$\omega_H \approx \frac{g_{m1}}{A_1 C_{L1}} \tag{3.1.2}$$

where A_1 is the closed-loop voltage gain of the first-stage amplifier, g_{m1} is the transconductance of the first-stage operational transconductance amplifier (OTA) and C_{L1} is the load capacitance at the output of the first stage which is is implemented by a MOS capacitor to limit the bandwidth. The second stage amplifier is implemented with a resistive feedback op-amp to further enhance the gain.

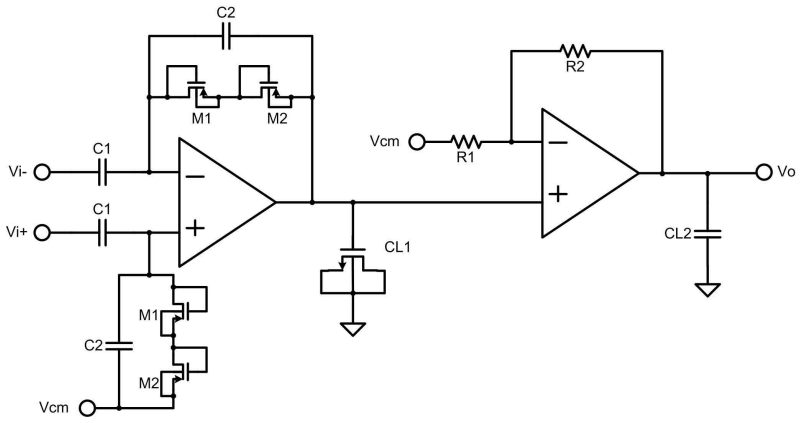


Figure 3.1: Architecture of the low-noise low-power high-sensitivity amplifier.

In the proposed design, both the silicon area limitation and the input impedance

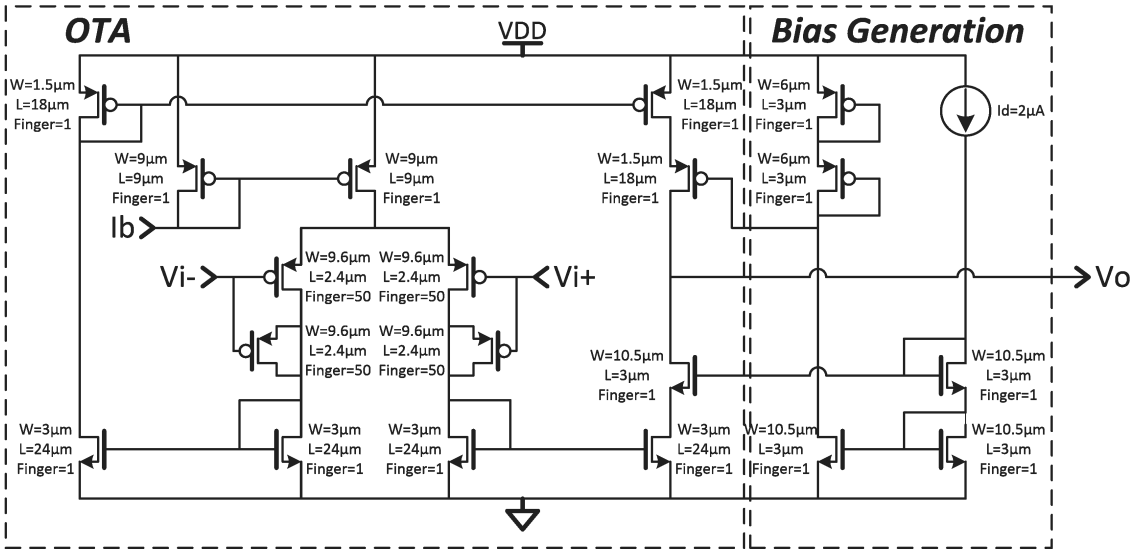


Figure 3.2: Schematic of the first-stage operational transconductance amplifier (OTA) of front-end amplifier

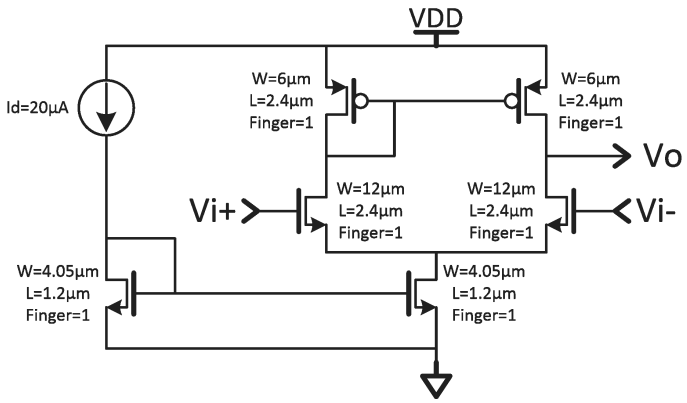


Figure 3.3: Schematic of the second-stage operational amplifier (OpAmp) of front-end amplifier

requirement of the amplifier are taken in consideration. The capacitors, C_1 and C_2, are implemented with double-layer poly capacitors and are carefully matched during layout. The size of the diode-connected transistors M1 and M2 is $18\mu m/18\mu m$, showing a simulated small-signal incremental resistance around 1.5TΩ. Therefore, the low-frequency cut-off, ω_L, is 0.5Hz. The high-frequency cut-off, ω_H, of the first stage is set to 10kHz by tuning g_{m1} and C_{L1}.

At the frequency range of interest, the major source of noise in this circuit is flicker (1/f) noise. The 1/f noise level is inversely proportional to the gate area, especially the input gate areas of the OTA. As presented in [57], the overall input-referred noise of the first stage amplifier can be expressed in terms of the input referred noise of the OTA as,

$$\overline{v_{ni,amp}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \overline{v_{ni,OTA}^2} \tag{3.1.3}$$

where $\overline{v_{ni,OTA}^2}$ is the input-referred noise of the OTA. A larger input gate area can help reduce the input-referred noise of the OTA, $\overline{v_{ni,OTA}^2}$, by reducing the 1/f noise of the OTA [139]. However, the input gate area cannot be made too large, otherwise the overall input-referred noise of the first-stage amplifier, $\overline{v_{ni,amp}^2}$, will increase [57, 140]. In this design, PMOS input gates are used in the first-stage OTA, as shown in Fig. 3.2, because PMOS transistors show 1 to 2 orders of magnitude lower flicker noise than NMOS transistors when biased at the subthreshold operating region [57, 141, 142]. The gate size of the input PMOS transistors in the OTA is chosen to be $480\mu m/2.4\mu m$ for optimized input-referred noise performance of the

first-stage amplifier.

The second-stage amplifier is implemented with a single-stage differential common source operational amplifier (Op-Amp), as shown in Fig. 3.3. The open loop voltage gain of the Op-Amp is 45dB in simulation. Resistive feedback is used to achieve the 14dB closed-loop voltage gain of the second-stage amplifier. Non-inverting negative feedback is chosen to minimize the loading to the first-stage amplifier.

3.1.3 A 12-bit 1MS/s SAR ADC Circuit Design in 0.5μm CMOS Process

The on-chip ADC as shown in Fig. 3.4 features 12-bit resolution and up to 1MS/s conversion rate. A two-stage digital-to-analog converter (DAC) is employed for the successive-approximation-register ADC circuit. The coarse conversion part of the DAC is implemented with a binary-weighted capacitor array, and it generates the first 9 most significant bits (MSBs). The capacitors are implemented with double-poly capacitors. The unit capacitor, C_0, is 204fF and has the size of 15μm by 15 μm, which ensures that the linearity of the DAC is higher than 12 bits. The capacitor array is laid out in a center-symmetric manner for the best matching of each capacitor in the array. The fine conversion part of the DAC is realized by a resistor string of 8 resistors, each of which has a resistance of 2kΩ, guaranteeing that the settling time of the DAC is fast enough for 1MS/s operations. The voltage input range of the SAR ADC is from 1.2V to 3.8V. The simulated DNL and INL

are both less than 0.5LSB.

The SAR logic is developed based on the schematic of the combinational logic successive approximation registers products DM2502, DM2503, DM2504 from National Semiconductor [143].

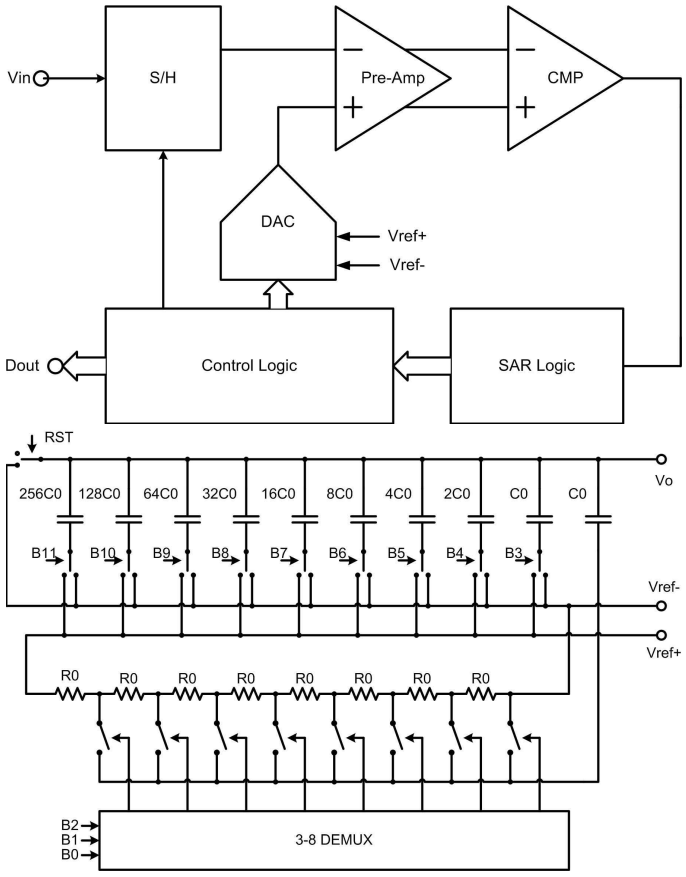


Figure 3.4: Architecture of the 12-bit resolution 1M samples/s on-chip successive-approximation-register ADC.

3.1.4 Experimental Results and Discussion

Fig.3.5 shows the microphotograph of the analog front-end that was fabricated using $0.5\mu m$ 2P3M standard CMOS process, occupying an area of $1.5mm \times 1.5mm$.

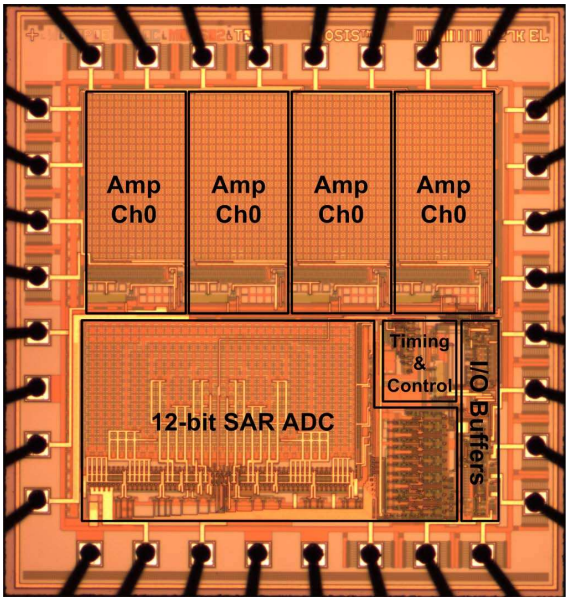


Figure 3.5: A microphotograph of the analog front-end. The size of chip is 1500μm by 1500μm.

The amplifier gain is measured with an Agilent 33521A function generator as input source and an Agilent MSO7034B oscilloscope to capture the output signals. As shown in Fig. 3.6, the measured mid-band gain of the low-power, low-noise amplifier is 54.24dB, which is very close to the simulated voltage gain of 53.92dB. The measured bandwidth is from 3.27Hz to 11kHz, which differs from the simulated bandwidth from 0.56Hz to 8.38kHz. The deviation of the measured low-frequency cut-off ω_L from the simulated result is due to the inaccuracy of the simulation model

for extremely large incremental resistance of diode-connected transistors, which is usually in the order of TΩ. The deviation on the high frequency cut-off, ω_H, is most likely due to the fabrication process corner variation of the test die. By adjusting the bias current of the amplifier, the high frequency cut-off can be further tuned. The output-referred noise is measured using an Agilent N9320B spectrum analyzer with the input of the amplifier shorted to ground. The input-referred noise is converted from the measured output-referred noise by dividing the mid-band voltage gain of the amplifier. The input-referred noise is $3.11\mu V_{rms}$, which is slightly higher than the simulated $2.42\mu V_{rms}$, due to i) the coupled power line noise at 60Hz and other environmentally coupled noise around 1kHz; and ii) the noise from the spectrum analyzer, which has a noise floor of -90dBm at its minimum resolution bandwidth of 10Hz.

The static performance (DNL, INL) of the SAR ADC has been tested with a 10Hz, 1.2V-3.8V triangular wave input signal generated with an Agilent 33120A function generator. The digital output data were recorded using a Tektronix TLA6204 logic analyzer. The dynamic performance of the SAR ADC has been tested with a 486.8164kHz 1.2V-3.8V sine wave input signal generated also with the Agilent 33120A function generator. The ADC was clocked at 1MS/s. The digital output data were recorded using an Agilent MSO7034B Mixed Signal Oscilloscope. The digital data were processed using Matlab. The testing result of the on-chip SAR ADC shows a differential nonlinearity (DNL) smaller than +1.7LSB/-1LSB, and an

integral nonlinearity (INL) smaller than +1.5LSB/-1.1LSB, as shown in Fig. 3.8. The effective number of bits (ENOB) of the ADC is 10.2 under 1MS/s sampling rate at the 486.8164kHz input (Fig. 3.9). The measured results show degraded DNL and INL performance when compared with the simulated results.

Table 3.1 and Table 3.2 summarize and compare the simulated results and measured performance of the front-end amplifier and the SAR ADC.

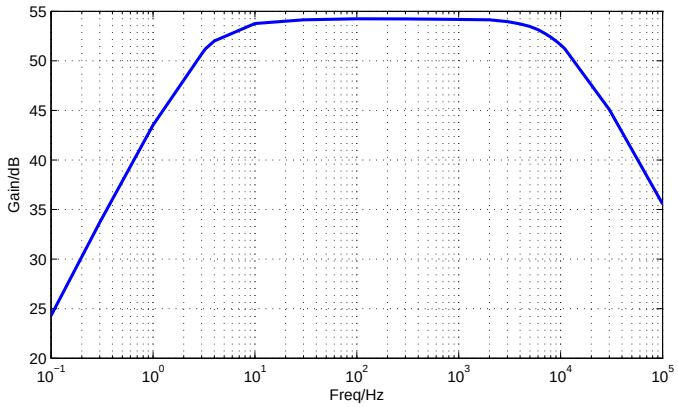


Figure 3.6: The measured AC gain of the low-power low-noise amplifier

3.2 A 12-bit 1MS/s SAR ADC in 0.18μm CMOS Process

Based on the SAR ADC design presented in the previous section, a 12-bit 1MS/s SAR ADC has been implemented in IBM 0.18μm standard CMOS technology. This SAR ADC is designed for general-purpose uses in systems like wireless sensor networks and image sensors. Therefore, the design goals are to minimize power

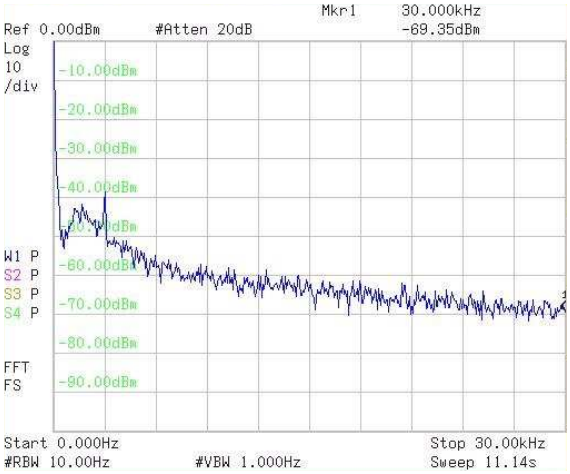
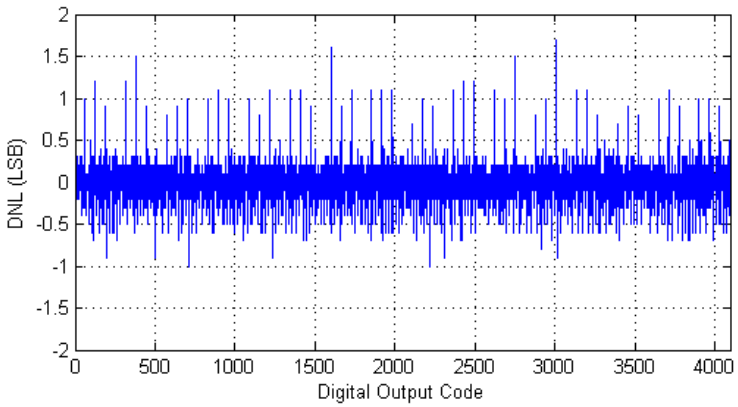


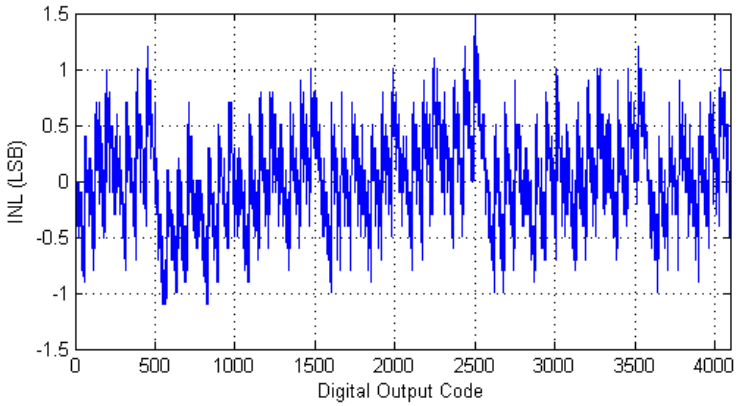
Figure 3.7: The output-referred noise spectrum of the low-noise low-power low-noise amplifier

Table 3.1: Front-End Amplifier Performance Summary

Design Parameter	Simulated Results	Measured Results
Supply Voltage	5V	5V
Supply Current	$24\mu A$	$24\mu A$
Mid-Band Gain	53.92dB	54.24dB
Bandwidth	0.56Hz-8.38kHz	3.27Hz-11kHz
Input-Referred Noise	$2.42\mu V_{rms}$	$3.11\mu V_{rms}$
THD & N @ 1kHz	45.2dB	37.9dB
CMRR	83.9dB	66.8dB
Channel Isolation @ 1kHz	N/A	57.4dB



(A)



(B)

Figure 3.8: Measured (A) DNL and (B) INL of the SAR ADC in 0.5μm CMOS process.

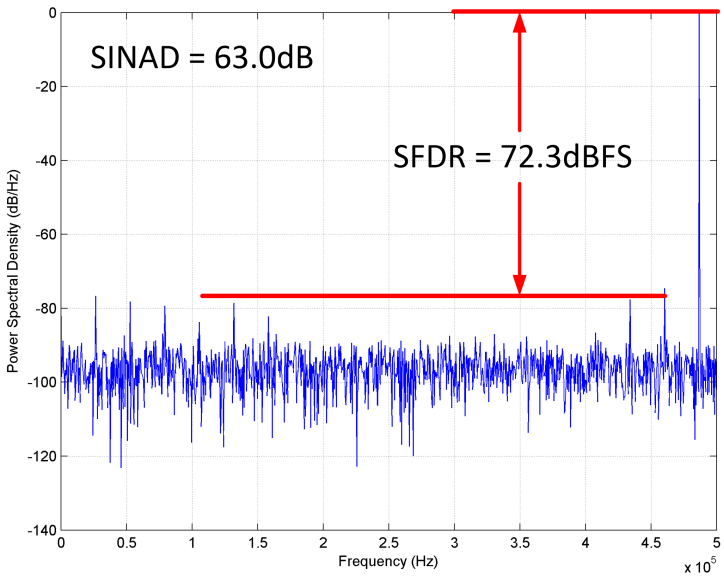


Figure 3.9: Measured spectrum of the SAR ADC in 0.5μm CMOS process.

Table 3.2: Amplifier Performance Summary

Design Parameter	Simulated Results	Measured Results
Supply Voltage	5V	5V
Power Consumption	3.86mW	3.69mW
Input Voltage Range	1.2V-3.8V	1.2V-3.8V
DNL	<0.5 LSB	<+1.7/-1.0 LSB
INL	<0.5LSB	<+1.5/-1.1LSB
ENOB	N/A	10.2bits
FOM	N/A	2.93pJ/conv

consumption, to maximize input signal range and to accommodate a wide voltage supply range. Different layout versions of this SAR ADC have been used in multiple projects, including i) a wireless fully event-driven electrogoniometer (presented in Chapter 5 - System Integration), ii) a video compression image sensor.

3.2.1 Circuit Design

The architecture of the SAR ADC is shown in Fig. 3.10. A capacitive charge sharing digital-to-analog converter (DAC) is employed. The DAC is divided into two parts to reduce the total capacitor area and the power consumption. The 6 most significant bits (MSB) of the DAC are implemented with a 6-bit binary-weighted capacitor array. The 6 least significant bits (LSB) of the DAC are implemented with C-2C capacitor array. The capacitors in the DAC are realized using dual layer metal-insulator-metal (MIM) capacitors.

According to simulations, the DAC achieves a linearity higher than 72dB. The sample-and-hold processing is implemented together with the capacitor array DAC, thus, no additional sampling capacitor is required. The DAC outputs the subtraction result of the input voltage and the weighted reference voltage. The comparator compares the DAC output with a constant common mode voltage, $V_{ref}/2$. This design reduces the circuit complexity since no wide common-mode input range comparator is needed. Fig. 3.11 shows the schematic of the comparator used in this SAR ADC.

No Sample/Hold Amplifier (SHA) is implemented in the ADC for the wireless fully event-driven electrogoniometer application. This is because the ADC is taking buffered full swing voltage signals from the accelerometer. The output buffer in the accelerometer provides sufficient current to drive the input load of the capacitor array in the ADC. For the video compression image sensor application, a PMOS source follower SHA is implemented to compensate for the DC level shift caused by the NMOS source follower used in the image sensor's analog voltage readout circuit. The schematic of the SHA is shown in Fig. 3.12.

The SAR logic is developed based on the schematic of the combinational logic successive approximation registers products DM2502, DM2503, DM2504 from National Semiconductor [143].

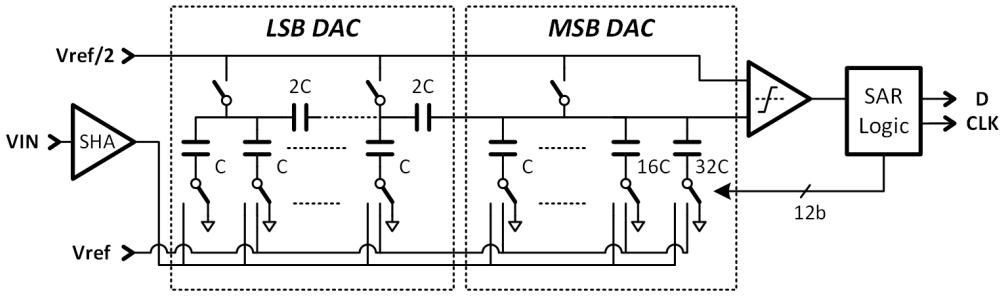


Figure 3.10: Architecture of the of 12-bit resolution successive approximation register (SAR) analog-to-digital converter (ADC).

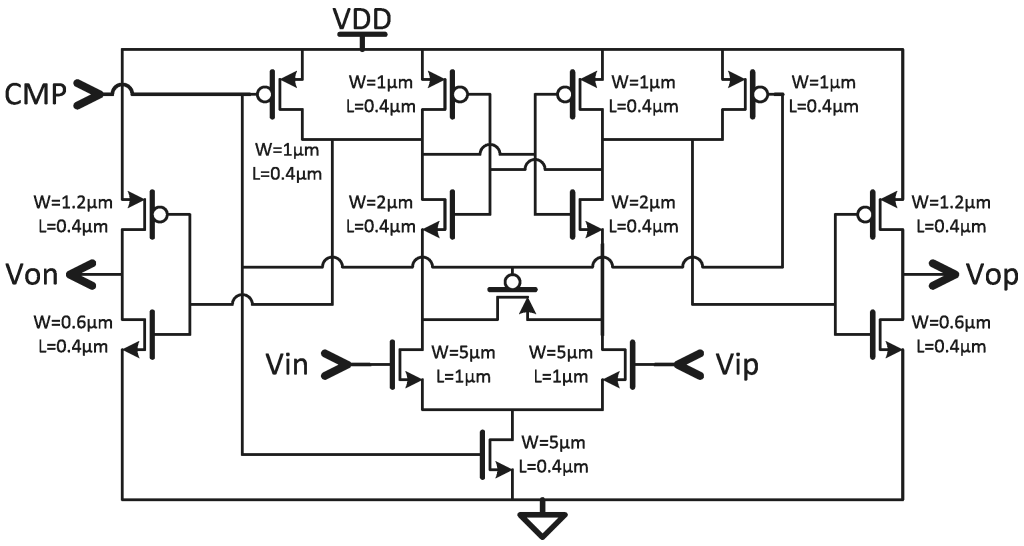


Figure 3.11: Schematic of the comparator in the SAR ADC.

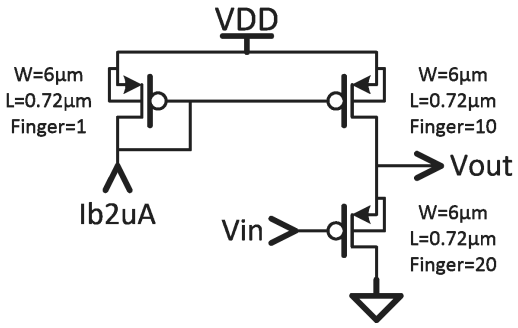


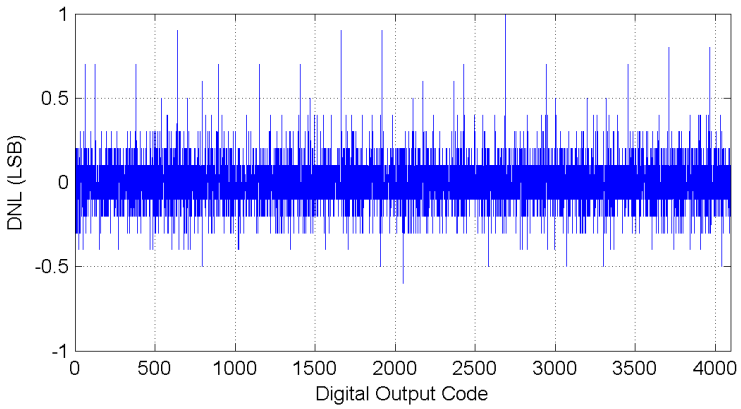
Figure 3.12: Schematic of the Sample/Hold Amplifier (SHA) in the SAR ADC for the image sensor column level ADC version.

3.2.2 Measurement Results

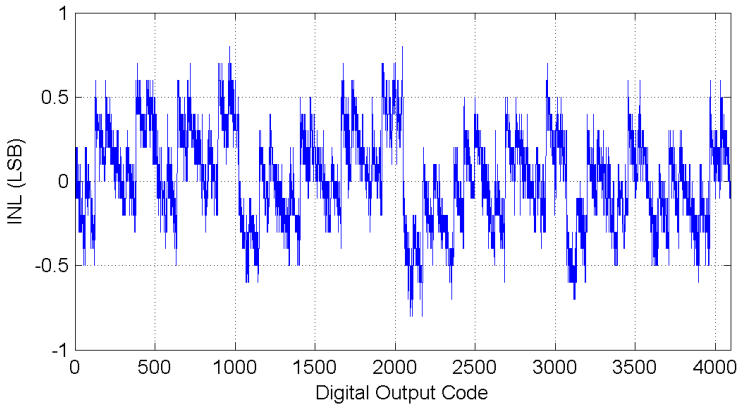
The SAR ADC can work under a supply voltage ranging from 1.8V to 3.3V. The static performance (DNL, INL) of the SAR ADC has been tested with a 10Hz, 0V-1.8V triangular wave input signal generated with an Agilent 33120A function generator. The digital output data were recorded using a Tektronix TLA6204 logic analyzer. The dynamic performance of the SAR ADC has been tested with a 486.8164kHz 0V-1.8V sine wave input signal generated with the same Agilent 33120A function generator. The digital output data were recorded using an Agilent MSO7034B Mixed Signal Oscilloscope. The SAR ADC was connected to 1.8V supply voltage and was clocked at 1MS/s. The measured differential non-linearity (DNL) is less than 1.0LSB while integral non-linearity is less than 0.8LSB at 1MS/s conversion rate, as shown in Fig. 3.13. The ENOB is 10.6 bits with the 486.8164kHz sinusoidal input signal, as illustrated in Fig. 3.14. The power consumption is as low as 195fJ/conversion with 302.5uW at 1MS/s under 1.8V supply voltage. Table 3.3 summarizes the performance of the SAR ADC.

3.3 An Asynchronous Level-Crossing ADC

Part of the content in the section, An Asynchronous Level-Crossing ADC, was originally published in [144]



(A)



(B)

Figure 3.13: Measured (A) DNL and (B) INL of the SAR ADC in 0.18μm CMOS process.

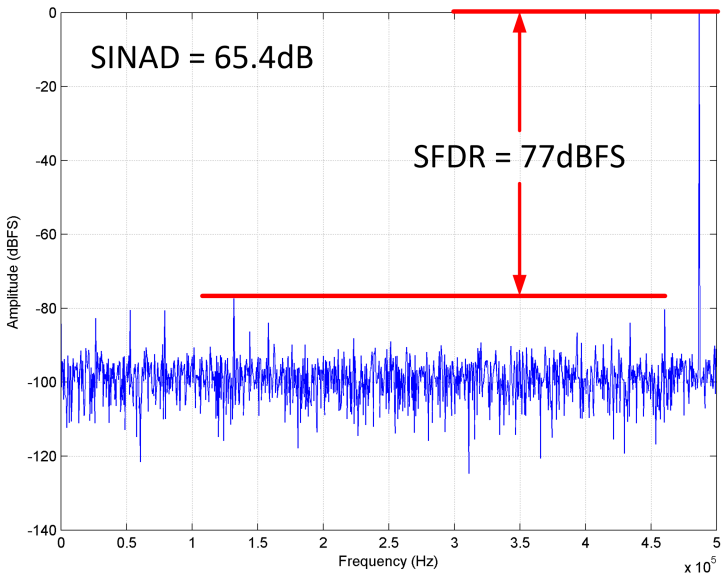


Figure 3.14: Measured spectrum of the SAR ADC in 0.18μm CMOS process.

Table 3.3: Measured performance summary of the SAR ADC

Supply Voltage	1.8V - 3.3V
Input Voltage Range	0V to Supply Voltage
ADC Resolution	12 bits
Max Sampling Rate	1MS/s
Power Consumption	302.5μW @ 1.8V_{dd}
FOM	195fJ/conv
ENOB	10.6 bits

2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 770-773.

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3.3.1 Introduction

Asynchronous continuous sampling event-driven ADCs have been introduced in ultra-low power analog front-end systems in recent years [145, 146, 147, 148]. The major advantages include its relatively low average output data rate and signal dependent power consumption [149, 150, 151, 152, 153, 154]. [145] proposed a fixed-window level-crossing ADC integrated with low-noise amplifiers for bio-potential recording applications. However, the power consumption due to the reset procedure of the feedback capacitor in each comparison cannot be reduced. [146] described an event-driven ADC, featuring a 200nW power consumption for wearable ECG sensing applications, under a 300mV power supply, which significantly limits the dynamic range and signal-to-noise ratio of the input signal. The maximum input

frequency is also limited to 1kHz because of the large ADC loop delay. Adaptive resolution asynchronous ADCs were proposed in [147, 152] to improve the data rate and power consumption efficiency, but at the cost of increased complexity and power consumption of the entire design.

Here, a low-power high-speed asynchronous event-driven level-crossing ADC is presented, featuring 6-bit resolution, 0.8-2.0V wide supply range, 1MS/s sampling rate, 5.01kHz input signal bandwidth, with a power consumption as low as 5μW. Gated low power digital circuits are used to optimize the power consumption. A self-controlled delay loop is integrated to increase the robustness of the level-crossing ADC. In a case study for body movement measurements (presented in Chapter V - System Integration), the asynchronous level-crossing ADC produces 90% less output data when compared with the synchronous sampling ADCs to capture the same signal with the same accuracy.

3.3.2 Circuit Design

The asynchronous level-crossing ADC enables continuous-time data sampling for completely event-driven operations. Fig. 3.15 illustrates the block diagram of the asynchronous continuous-time level-crossing ADC. The architecture of the ADC is adopted from the 2008 paper by B.Schell and Y. Tsividis [151]. It tracks the changes of the input signal by comparing it with a set of hysteresis reference voltage pair, $V_{ref}+$ and $V_{ref}-$, using a pair of comparators. The low-power, wide-common-

mode-range comparator pair, adopted from [151], as shown in Fig. 3.16, enables the level-crossing ADC to operate in a wide supply range from 0.8V to 2.0V. The input stage of the comparator is biased at $2\mu A$, balancing both the requirements of power consumption and conversion speed.

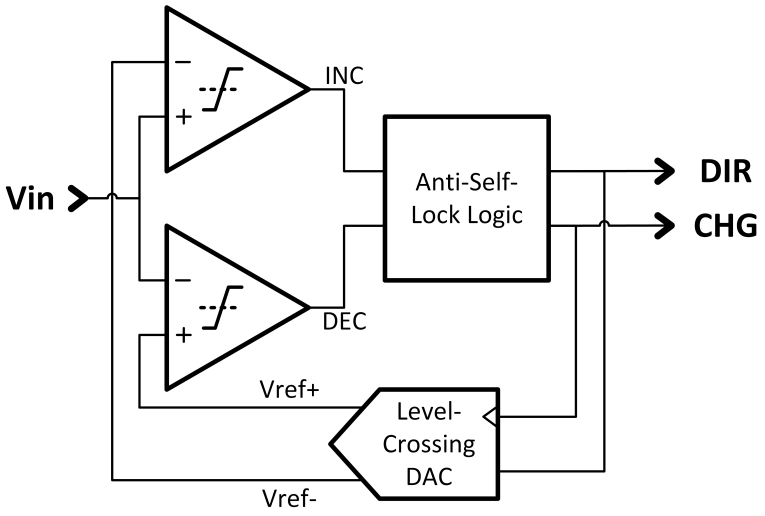


Figure 3.15: Block Diagram of the Asynchronous Level-Crossing ADC, integrating a pair of comparators, an anti-self-locking logic, and a level-crossing DAC.

A 64-level DAC, adopted from [151], is implemented with a resistive ladder to generate 64 pairs of reference voltages. In each ADC conversion cycle, a pair of reference voltages, $V_{ref}+$ and $V_{ref}-$, are selected from the reference voltage generator. The comparator pair generates an "increase" (INC) or a "decrease" (DEC) output signal when the input voltage crosses above $V_{ref}+$ or below $V_{ref}-$, respectively. Fig. 3.17 illustrated the operation principles of a simplified (8-level) version of the

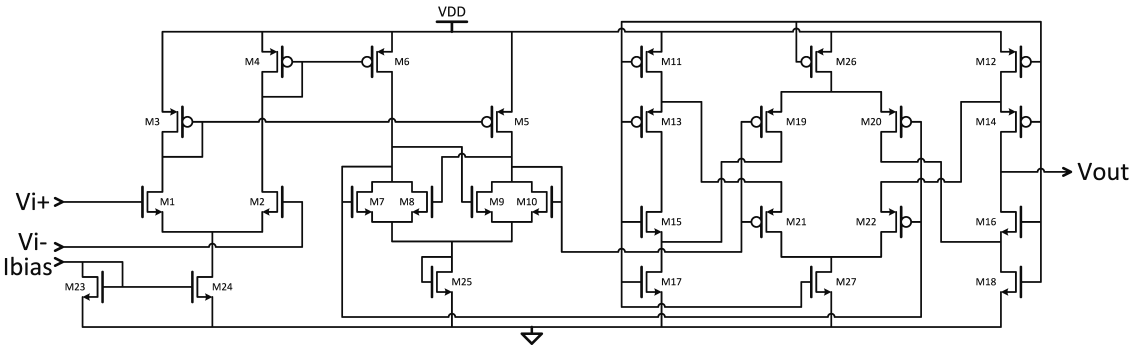


Figure 3.16: Schematic of the low-power, wide-common-mode-range comparator in the level-crossing ADC.

asynchronous level-crossing ADC. $V_{ref}+$ and $V_{ref}-$ are combined into a single "ADC Reference Voltage" line in Fig. 3.17 for the simplicity of the demonstration. For each set of the reference voltage pair, the $V_{ref}+$ is slightly higher than the $V_{ref}-$ of the upper next set of reference voltages, as shown in Fig. 3.18, which makes the ADC robust against noise and overshoot of reference voltages when a new set of reference voltages are selected.

The INC and DEC outputs from the pair of comparators are converted to a "direction" (DIR) signal and a "change" (CHG) signal by the digital logic. The DIR and CHG signals are fed to a shift register to control the selection of the reference voltage pair in the asynchronous DAC, where the DIR signal controls the shifting direction of the shift register while the CHG signal clocks the shift register. The shift register, as illustrated in Fig. 3.19, is implemented with low-power clock-gating D-flip-flops (DFFs). The input clock of the DFF is gated by a combination logic of the input and output signals to reduce switching power consumption on the

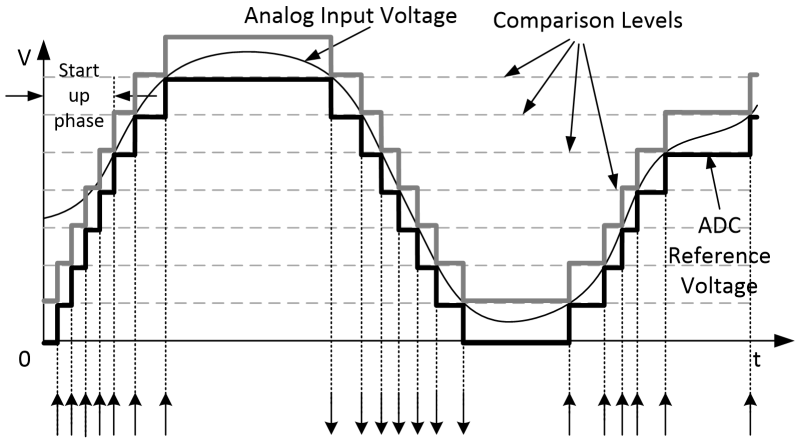


Figure 3.17: Operation principles of an 8-level asynchronous level-crossing ADC. ↑ and ↓ represent an "increase" (INC) or "decrease" (DEC) output of the ADC, respectively.

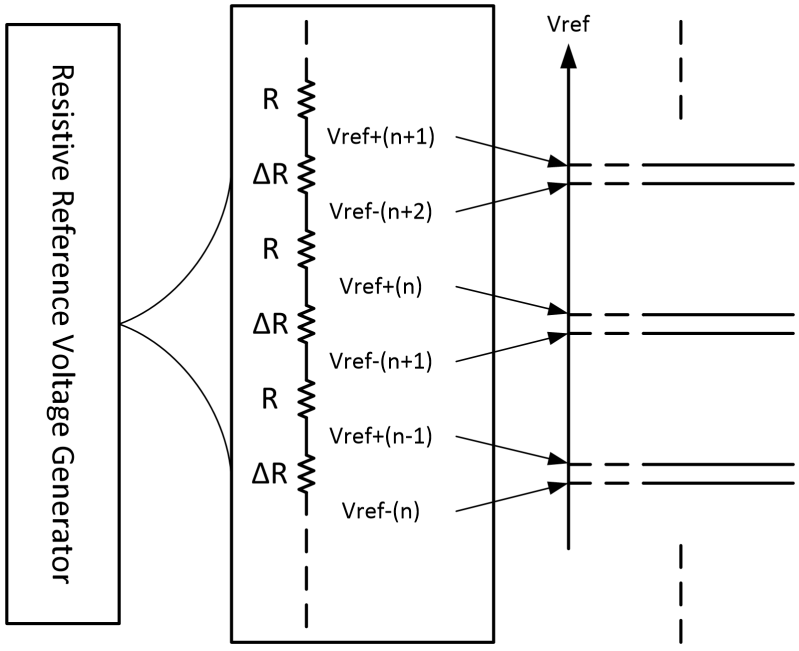


Figure 3.18: Schematic of the hysteresis resistive reference voltage generator.

parasitic capacitance of the input gates in the DFF during unnecessary clock cycles. Simulation results show a 83.3% decrease of power consumption at 500kHz under 1.8V supply voltage, as compared to standard DFF design without clock-gating.

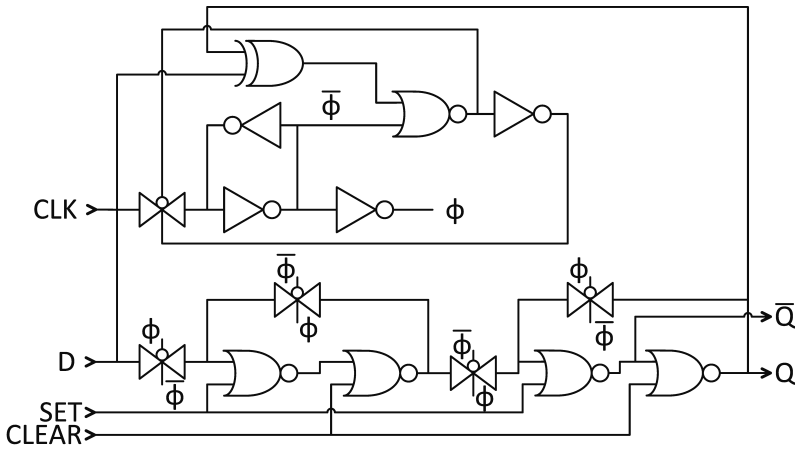


Figure 3.19: Schematic of the low-power clock-gating D-flip-flop (DFF).

An asynchronous reset function is implemented in the ADC. During reset phase, the shift register clears its current selection of the reference voltage pair and selects the lowest set of reference voltage pair. After the reset is released, the ADC starts to change the selection of the reference voltage pair at its fastest speed to catch up with the input signal. The continuous-time sampling operation of the ADC resumes once the reference voltage pair catches up with the input signal. The reset function improves the system robustness.

One critical issue of the level crossing ADC is the self-locking of the circuit. It originates from the edge-detection nature of the D-flip-flops used in the shift register. Self-locking occurs when the reference voltage pair, selected by the shift register,

loses the capability to continuously track the analog input voltage. Self-locking happens a) during circuit startup phase, b) during circuit (shift register) reset phase, c) during conversion error, or d) when input signal changes faster than the circuit can respond. Fig. 3.20 demonstrates how self-locking happens under different scenarios in a simplified 8-level asynchronous level-crossing ADC. When the ADC enters the self-locking state, either the INC or the DEC signal stays high. No rising edge in CHG signal is generated to clock the shift register. The selection of the reference voltage pair for the comparator pair is frozen at the same level and the tracking of the input signal is lost. Once the self-locking state is entered, the level-crossing ADC can only exit the self-locking state by itself when the input signal returns between the selected reference voltage pair that is able to start to track the input signal again.

In order to release the ADC from a self-locking state, an anti-self-locking CHG signal generation logic circuit is used, as shown in Fig. 3.21. The INC and DEC signals are encoded into CHG and DIR signals with a digital encoder circuit. The DIR signal is generated RS-flip-flop logic, as shown in Fig. 3.21 (A), to control the shifting direction of the shift register. A self-controlled delay loop, as shown in Fig. 3.21 (B), will reset the CHG signal if the tracking of the input signal is lost. Fig. 3.22 demonstrates the timing of this control logic. Either the INC or DEC signal discharges node B and pulls up node A. The comparator, which is biased with 30nA current, will delay the logic change from node A and node B to the

comparator output node by $0.5\mu s$. A CHG signal is associated with the output of the comparator. The logic low signal at node C will evoke the recharge of node B and discharge of node A, and hence the output of the comparator will be delayed again by another $0.5\mu s$ before node C turns logic high. As shown in Fig. 3.21 (B), the logic low signal at node C turns on the PMOS transistor controlled by node C and the bottom NMOS transistor controlled also by node C cuts off the sink current, so the recharge of node B is guaranteed even when INC and DEC signals are high during the process. If either the INC or the DEC signal is high at the moment when node C is recharged, node B will be discharged again and the loop will then generate another pulse for the CHG signal. If the INC and DEC signals are low after node B is recharged, the PMOS transistor controlled by node A is turned on to keep node B high. With the anti-self-locking logic, the proposed level-crossing ADC will be immune to self-locking, as demonstrated in Fig. 3.20. Hence, the proposed level-crossing ADC features better robustness and makes an asynchronous reset function possible. The fastest response speed of the level-crossing ADC is $1\mu s$, which is determined by the delay of the self-controlled delay loop in the anti-self-locking logic. In order to avoid overshooting conversions of the ADC, the delay of the self-controlled delay loop is designed to be longer than the conversion time of the input signal comparators.

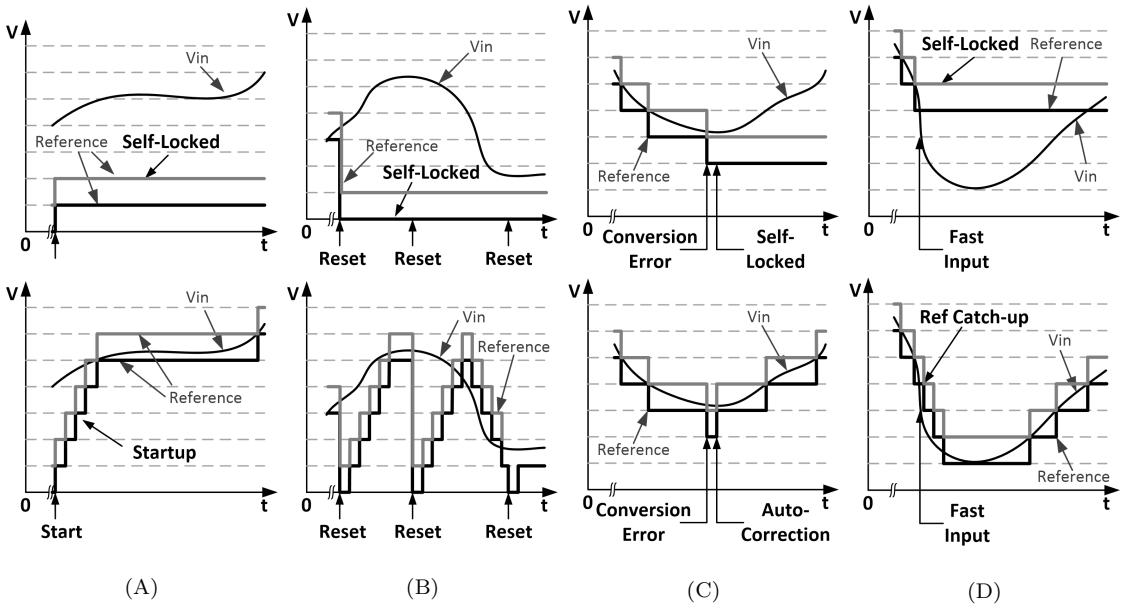
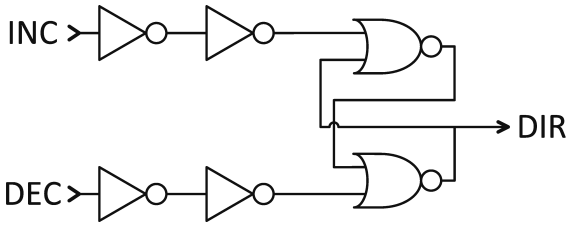
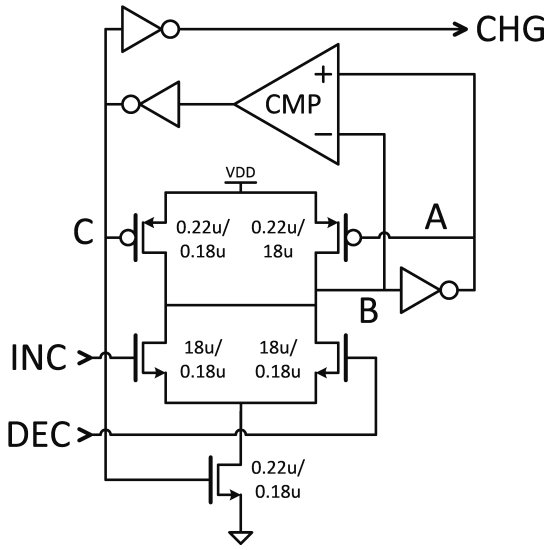


Figure 3.20: Self-locking state of the level-crossing ADC (upper row) and non-self-locking of the ADC with the proposed anti-self-locking "CHG" signal generation circuit (lower row) (a) during ADC startup, (b) during asynchronous resets, (c) during conversion error, and (d) when the input signal changing faster than the fastest ADC response speed.



(A)



(B)

Figure 3.21: Schematic of (A) "Change" and (B) "Direction" circuit.

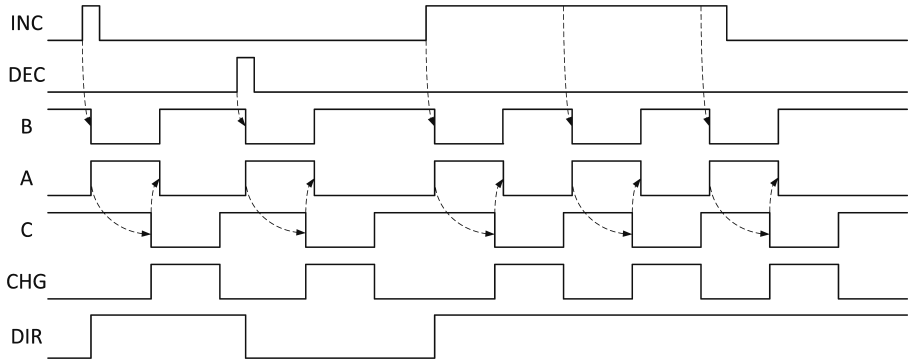


Figure 3.22: Timing diagram of the CHG signal generation circuit.

3.3.3 Measurement Results

The level-crossing ADC can work under 0.8V to 2.0V supply voltage. The input voltage range is from 0.2V to V_{DD} - 0.15V. The maximum input signal slew rate that the ADC can follow is 0.026V/μs at 2.0V supply voltage, so the maximum input signal bandwidth of the ADC is from DC to 5.01 kHz. The power consumption of the ADC can be as low as $5\mu W$ at 0.8V supply voltage with 1 kHz sinusoidal input signal. Fig. 3.23 shows the waveforms of the input and output signals of the asynchronous level-crossing ADC. The reconstructed ADC data is calculated by integrating the Direction signal at the rising edges of the Change signal. The spectrum of the reconstructed ADC output, as shown in Fig. 3.24, demonstrates the SNDR of the level-crossing ADC is 46.2dB at 1.8V supply and 5kHz sinusoidal input. Table 3.4 summarizes the performance of the level-crossing ADC.

3.4 Conclusion

Being at the very first stage of the electrical signal processing chain in a sensor network system, the design of the front-end circuits is essential to the noise level, bandwidth, swing and distortion performances of the system. Three front-end circuit designs for the wireless sensor network systems are presented in this Chapter.

A low-noise, low-power analog front-end circuit implemented in ON Semiconductor 0.5μm standard CMOS technology is designed for intracranial neural signal

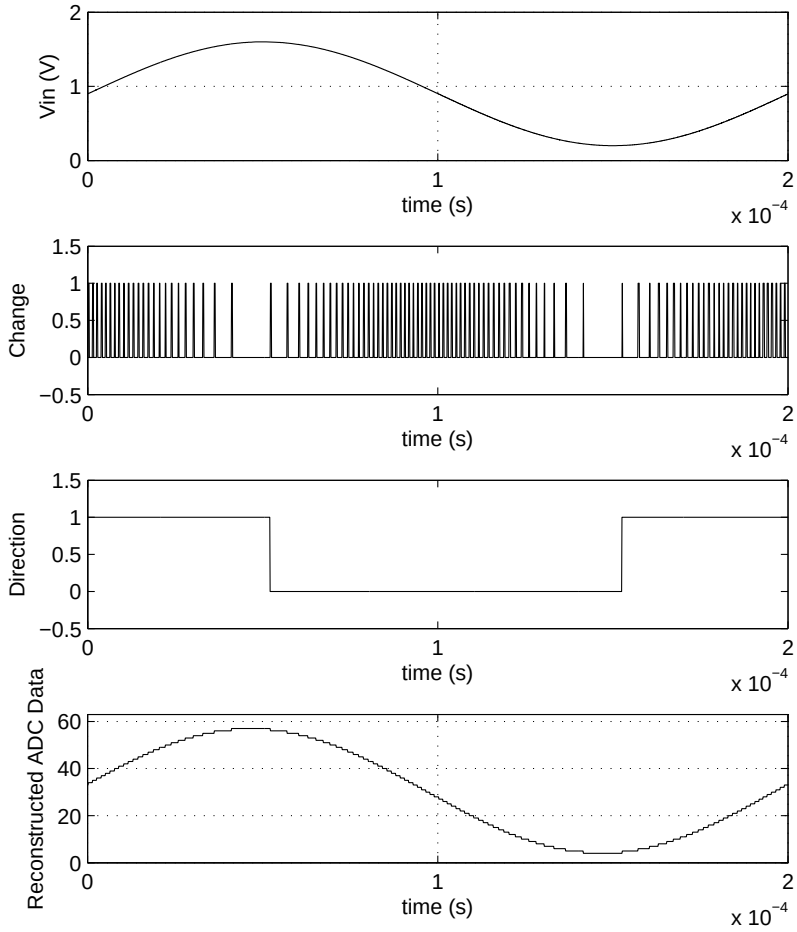


Figure 3.23: The spectrum of the level-crossing ADC output data.

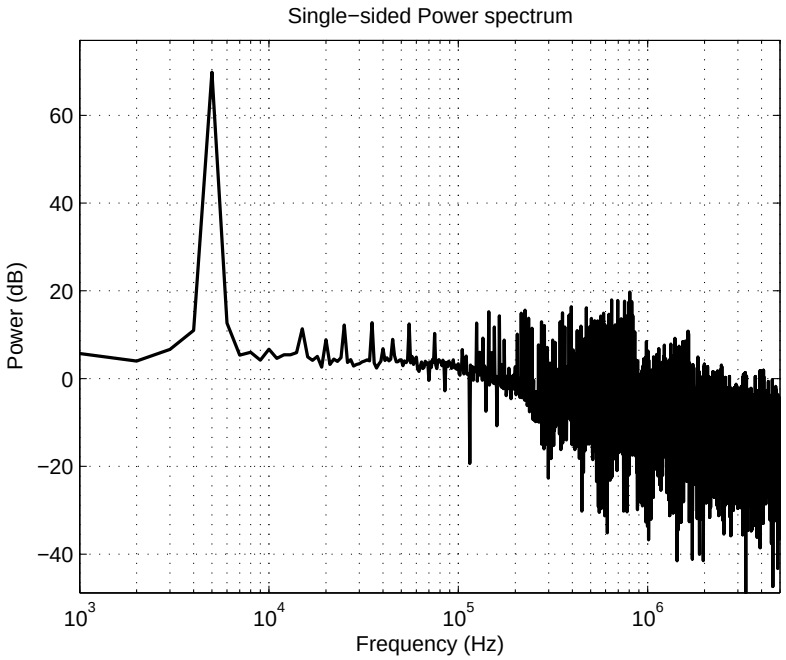


Figure 3.24: The spectrum of the level-crossing ADC output data.

Table 3.4: Measured performance summary of the level-crossing ADC

Supply voltage	0.8V to 2.0V
Input voltage range	0.2V to (supply voltage - 0.15V)
Input capacitance	<0.2pF
Maximum input signal slew rate	0.026V/μs @ 2.0V
Input signal bandwidth	DC to 5.01 kHz @ 2.0V
Power consumption	80μW @ 2.0V 5μW @ 0.8V
SNDR	46.2dB

recording as well as for general-purpose small signal detection. Ultra low noise of the front-end amplifier provides a low noise figure for the system. Sub-Hz to 10kHz bandwidth makes it suitable not only for biomedical signal recording, but also for interfacing to many other types of sensors. 54dB AC gain and 12-bit ADC resolution provide sufficient accuracy of the digitized signal for further signal processing. The low-power consumption makes this analog front-end suitable for power critical applications, such as battery/wireless-powered implanted devices as well as wireless sensor networks.

A 12-bit 1MS/s SAR ADC implemented in IBM 0.18μm standard CMOS process is designed for general purpose signal digitization in front-end circuits of the sensor network. A coarse-fine two-stage capacitive DAC structure is implemented for small silicon area and low power consumption. Bottom-plate sampling is used to achieve full-swing input signal range while relaxing the design requirement of the comparator. Thick oxide devices are used to accommodate a wide supply voltage range (1.8V-3.3V). This SAR ADC has an ENOB of 10.6 bits and FOM of 195fJ/conversion. It has been used in a wireless fully event-driven electrogoniometer system, as presented in Chpater 5 of this thesis. The ADC has also been used in a video compression image sensor in a collaboration with Jie Zhang, et al., from Johns Hopkins University.

A 6-bit asynchronous level-crossing ADC implemented in IBM 0.18μm standard CMOS process is designed specifically for a fully event-driven wireless sensor network system. The event-driven nature of the asynchronous level-crossing ADC makes it

the perfect candidate for digitizing sparse signals, such as neural action potentials and body movements, in a fully event-driven system. The ADC is able to operate with 0.8V to 2.0V supply voltage. The power consumption could be as low as $5\mu W$. Measured SNDR of the ADC is 46.2dB. This ADC is implemented in a wireless fully event-driven electrogoniometer system, as presented in Chpater 5 of this thesis.

Chapter 4

Wireless Circuit Design

4.1 Impulse-Radio Ultra-Wide Band Transceiver

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4.1.1 Transeiver Design

Impulse-Radio Ultra-Wide-Band (IR-UWB) communication is widely used in near-range, power-sensitive applications, especially biomedical systems [**?**, 155, 156, 157, 158], due to its simple circuit structure of the transceiver design, low power consumption, and high data rate.

In this design, three parallel, asynchronous and independent channels are implemented in the transmitter, as shown in Fig. 4.1. The transmitter architecture is adopted from W. Tang and E. Culurciello's 2011 paper [159]. Each channel includes a baseband generator (Fig. 4.2 (A)), an Radio Frequency (RF) pulse generator (Fig. 4.2 (B)), and two power amplifiers. The baseband generator converts digital input data into short pulses with different formats. The pulse width of the short pulses is tunable from 10ns to 250ns for different transmission duty cycles under different data rates. The baseband short pulses modulate an RF signal in the RF pulse generator. The RF pulse generators are implemented with ring oscillators with a total number of stages of 3, 5 and 7 for the three different channels. According to simulations the frequency generated by each channel is in the range of 2.8GHz-3.3GHz, 1.9GHz-2.4GHz, and 800MHz-1.3GHz, respectively. The oscillation frequency of each of the ring oscillators is tunable over 500MHz by an analog tuning voltage. The outputs

of the RF pulse generators are amplified by RF power amplifiers and fed into the transmitting antennas. In each channel, a low-power amplifier and a high-power amplifier are implemented for applications that require different RF output power levels. Both power amplifiers are realized by scaled inverters. The operation timing diagram of the transmitter is given in Fig. 4.3. Logic "0" is encoded into one short pulse in a baseband clock cycle, while logic "1" is encoded into two short pulses in a baseband clock cycle. An output of three continuous short pulses in a baseband clock cycle represents a global reset signal of the entire circuit.

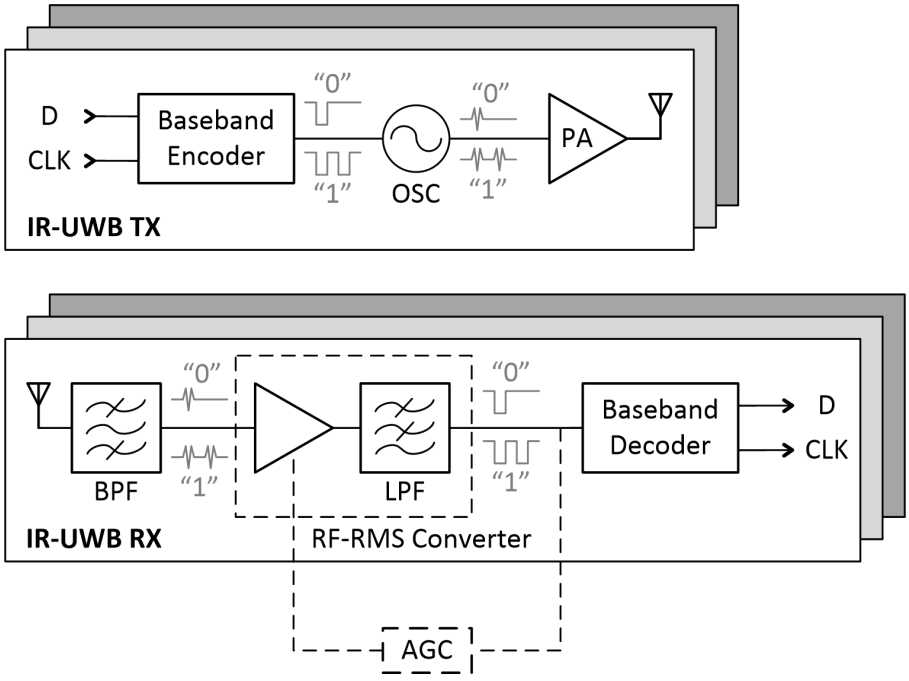
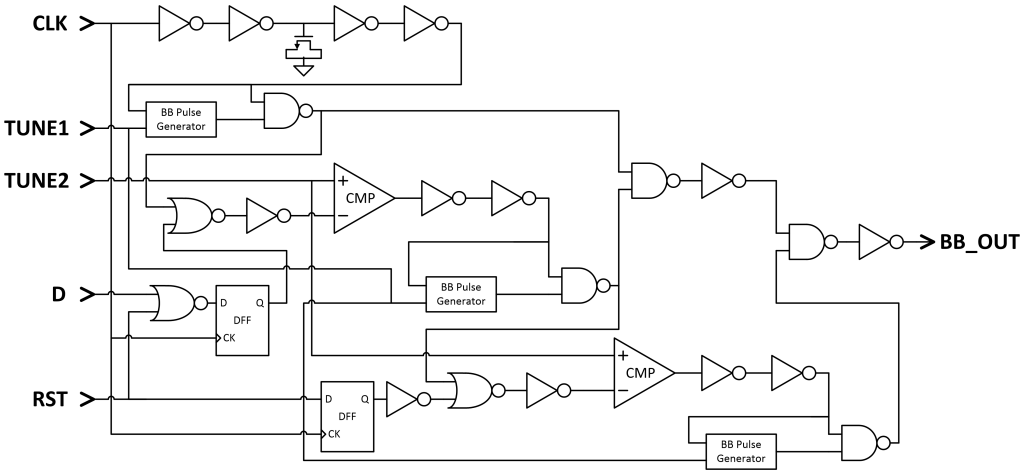
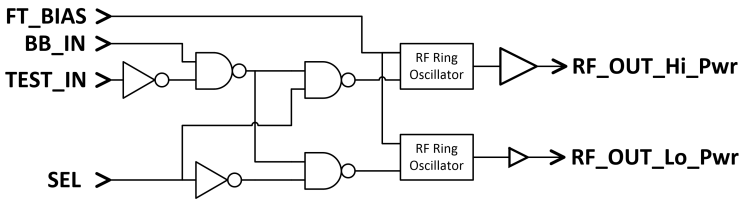


Figure 4.1: Block diagram of the IR-UWB transceivers. Three parallel, asynchronous and independent channels are implemented.

A tri-channel IR-UWB receiver is also implemented, as shown in Fig. 4.1. Within each channel, the RF signal is picked up by the receiving antenna at its corresponding



(A)



(B)

Figure 4.2: Architecture of (A) the baseband generator of the transmitter, which converts digital data input into short pulses with a tunable width from 10ns to 250ns, and (B) the RF pulse generator of the transmitter, which modulates the short pulses output of the baseband generator to RF frequencies.

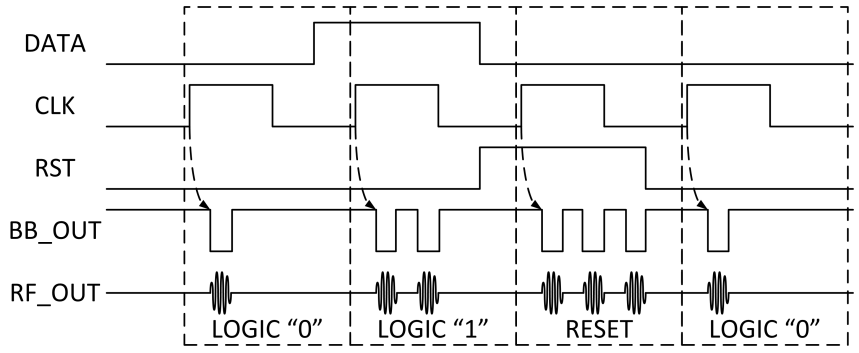


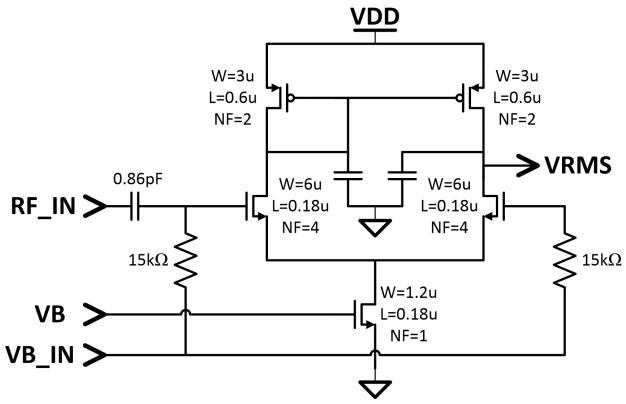
Figure 4.3: Timing diagram of the IR-UWB transmitter. Logic "0" is encoded into one short pulse in a baseband clock cycle, while logic "1" is encoded into two short pulses in a baseband clock cycle. An output of three continuous short pulses in a baseband clock cycle represents a global reset signal of the entire circuit.

operating frequency. A high-order band-pass filter extracts the in-band signal. The output of the bandpass filter is first amplified by a low-noise amplifier (LNA), and then fed into an RF power to root-mean-square voltage (RF-RMS) converter shown in Fig. 4.4 (A). A comparator (Fig. 4.4 (B)), synchronized to a fast sampling clock, compares the output of the RF-RMS converter with a reference voltage. The output of the comparator is encoded as logic high or low. A digital baseband decoder logic circuit is implemented, with the help of Dr. Milin Zhang from Department of Electrical and Systems Engineering at University of Pennsylvania, using a pattern-recognition logic to decode the comparator outputs into the format of received data (RX_DOUT), received clock (RX_CLKOUT) and received reset (TX_RSTOUT). The timing diagram is demonstrated in Fig. 4.5. The clock for the comparator sampling

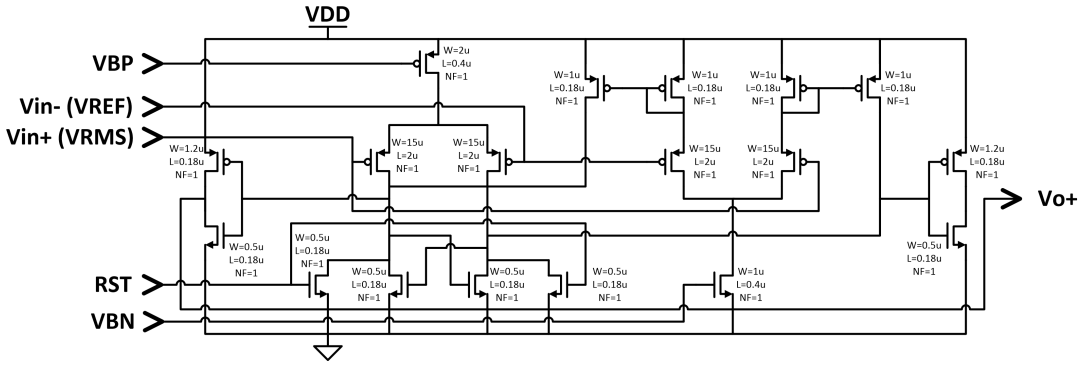
as well as the decoder logic runs at least eight times as fast as the received clock (RX_CLKOUT). The decoder has a running window to recognize the pattern of the data in the window. Within the running window, a string of continuous logic "1"s followed by a logic "0" is decoded as a logic "1" output. Similarly, a string of logic "0"s followed by a logic "1" is decoded as a logic "0" output. Subsequently, the decoded logic "1"s and "0"s within the running window are recognized and decoded to the received data, received clock and received reset signals. The size of detection window is configurable between 8 clock cycles and 16 clock cycles for different transmission data rates and transmission duty cycles.

4.1.2 Measurement Results

The transmitter circuit can operate over a wide supply voltage range from 1.2V to 2.0V. The continuous RF output power is measured by setting the RF ring oscillators and power amplifiers continuously on. The RF output power is measured with an Agilent N9320B spectrum analyzer. The output power of each channel is -13dBm with the high power RF power amplifier turned on, and -33dBm with the low power amplifier on. The oscillation frequencies are 1.6-1.7GHz, 0.9-1.0GHz and 0.6-0.7GHz, respectively for channel 0, channel 1 and channel 2. The drop in oscillation frequency between the simulated results and the measured results are due to the extra loading of the parasitic capacitance and the package of the test chip. Fig. 4.6 shows the waveforms of the baseband short pulses of the transmitter operating at 0.5Mbps data



(A)



(B)

Figure 4.4: Architecture of the (A) RF-RMS converter and (B) the comparator used in the RF-RMS detector, which compares the output of the RF-RMS converter with a reference voltage.

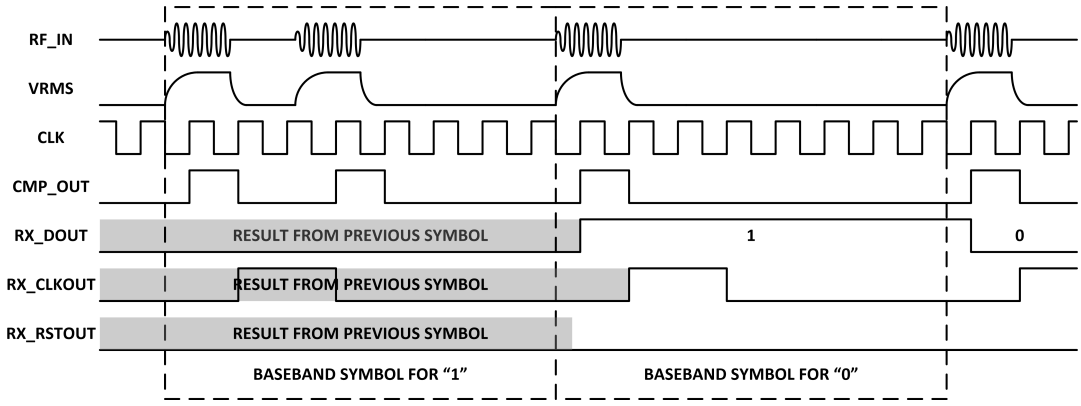


Figure 4.5: Timing diagram of the IR-UWB receiver. The output of the RF-RMS is decoded in a digital pattern-recognition logic circuit with the output in the format of received data (RX_DOUT), received clock (RX_CLKOUT) or received reset (TX_RSTOUT).

rate, captured using an Agilent MSO7034B oscilloscope. The power consumption is measured by using a Keithley 195 system digital multimeter to monitor the average DC current and voltage of the power supply to the transmitter block. The measured power consumption of the transmitter can be as low as 4.6pJ/bit, at 10Mbps data rate and 1.2V supply voltage. The measured performance of the IR-UWB transmitter is listed in Table 4.1.

The IR-UWB receiver also works over a wide supply voltage range from 1.2V to 2.0V. The clock frequency of the comparator and decoder logic can vary from 800kHz to 80MHz, which makes the receiver able to receive data from 50kbps up to 10Mbps. Fig. 4.7 shows the waveforms of both transmitter and receiver operating at 0.5Mbps data rate, captured using an Agilent MSO7034B oscilloscope. The power

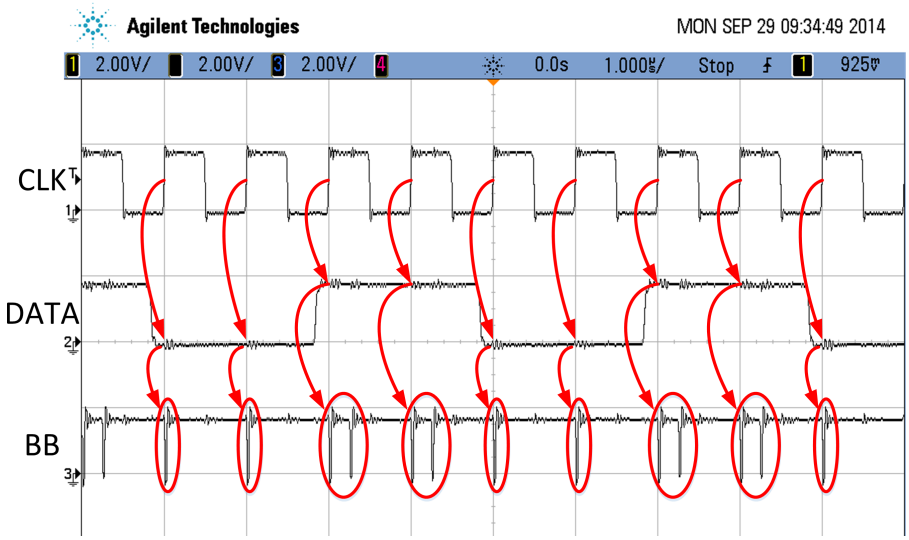


Figure 4.6: Waveforms of the output pulses of the transmitter. "DATA" and "CLK" are the input data and clock to the transmitter, respectively. "BB" is the baseband short pulses of the transmitter. A clock frequency of 0.5Mbps is used in this measurement.

Table 4.1: Summary of the measured performance of the IR-UWB transmitter

Supply voltage	1.2V to 2.0V
Output power	-13dBm under high power mode -33dBm under low power mode
Output frequency	1.6-1.7GHz for channel 0 0.9-1.0GHz for channel 1 0.6-0.7GHz for channel 2
Maximum data rate	20Mbps/channel
Power consumption (High power mode)	34.1pJ/bit @ 10Mbps, 1.2V 225pJ/bit @ 100kbps, 1.2V
Power consumption (Low power mode)	4.6pJ/bit @ 10Mbps, 1.2V 118pJ/bit @ 100kbps, 1.2V

consumption is measured by using a Keithley 195 system digital multimeter to monitor the average DC current and voltage of the power supply to the receiver block. The receiver power consumption can be as low as 1.12nJ/bit 1Mbps data rate and 1.2V supply voltage. The measured results for the IR-UWB receiver are summarized in Table 4.2.

The IR-UWB receiver could successfully pick up data wirelessly within 20cm distance from the transmitter, using a pair of monopole antennas. Longer communi-

cation distances are achievable by adding LNA stages at the receiver end.

Table 4.2: Measured performance summary of the IR-UWB receiver

Supply voltage	1.2V to 2.0V
Input frequency	300MHz - 4GHz
Maximum data rate	10Mbps/channel
Power consumption	1.12nJ/bit @ 1Mbps

4.2 Conclusion

In this chapter, the design of the wireless circuit for the sensor network system is presented. A low-power impulse-radio ultra-wide-band (IR-UWB) transceiver (TRx) is designed for wireless data communication between the sensor nodes. The TRx can operate at a data rate of up to 10Mbps, with a power consumption of 4.9pJ/bit transmitted for the transmitter and 1.12nJ/bit received for the receiver.

Future improvements of the transceiver include: 1) on-chip integration of an low-noise amplifier (LNA) in the receiver; 2) on-chip channel selection RF filter; 3) automatic gain control (AGC) feedback loop for the receiver.

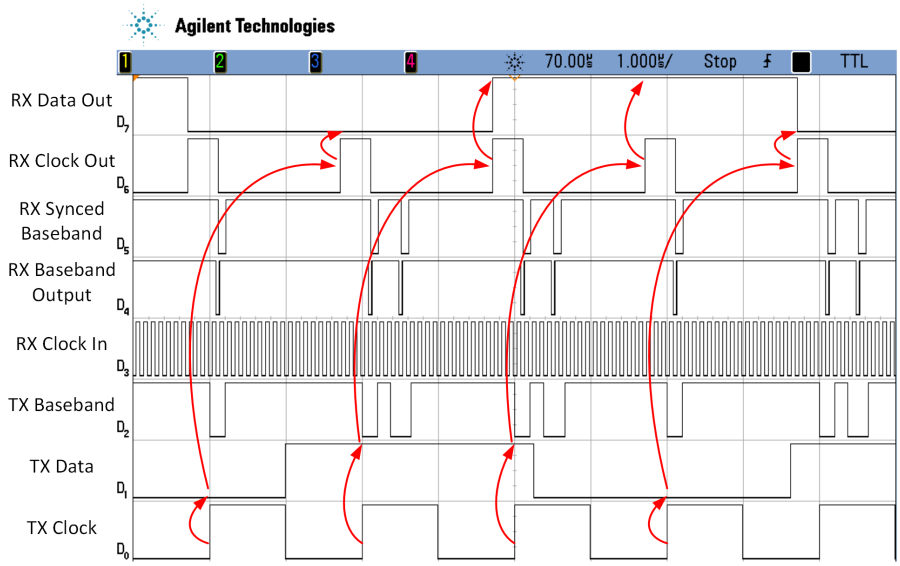


Figure 4.7: Measured waveforms of the transceiver signals. A clock frequency of 0.5Mbps is used in this measurement. "TX Data" and "TX Clock" are the transmitted data and clock signals at the UWB transmitter. "TX Baseband" is the baseband short pulses at the transmitter. "RX Clock In" is the digital sampling clock for the comparator and pattern recognition logic at the receiver. "RX Baseband Output" and "RX Synced Baseband" are the comparator instantaneous output and the synchronised output at the receiver. "RX Data Out" and "RX Clock Out" are the received data and clock at the receiver, respectively. "BB" is the baseband short pulses of the transmitter.

Chapter 5

System Integration

5.1 A Wireless Fully Event-Driven Electrogoniometer

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5.1.1 Introduction

Significant resources have been devoted over the past decade to the development of brain-machine interfaces (BMIs). These devices allow neurologically-impaired individuals to interact with the world by decoding motor intent from neural signals. Despite encouraging results [160, 161], the goal of liberating paralyzed limbs has not materialized. Foremost among the critical barriers to wide-spread implementation of BMI technologies is the absence of somatosensory feedback [162]. Touch, posture, and movement sensations are critical to normal motor function, but their transmission to the brain is interrupted by paralysis.

To restore the somatosensory pathway, sensory signals can be detected with artificial transducers and subsequently encoded to provide electrical microstimulation in the brain [163]. Microstimulation of somatosensory brain areas has been shown to yield discriminable percepts [164] and guide movements [165, 56, 166]. Most prior work has assumed that the sensors driving brain stimulation will be mounted on a prosthetic limb used by the subject [167, 168].

A recent advance in BMI technology consists of reanimating a person's own paralyzed limb using brain-controlled muscle stimulation rather than relying on a

prosthetic limb [52, 51]. This new strategy of restoring motor control presents new challenges for sensory feedback. In particular, since the sensors are worn directly on the body, they should have a minimal physical presence, free of the constraints of gloves or wires. This places greater demands on the specifications of the sensor and associated electronics, such as power consumption and size.

The wireless fully event-driven electrogoniometer is designed as part of a brain-machine-interface to study the relationship between the neural activities and body movement. A wearable sensor is required for this application to quantitatively evaluate body movement. The sensor has a minimal physical presence and is free of the constraints of gloves or wires. The system integrates i) a multi-channel neural signal recording device, ii) a wireless fully event-driven electrogoniometer, and iii) a PC interface. An electrogoniometer is a device used to measure joint angles. It typically employs sensors with relatively high power consumption, such as potentiometers or strain gauges [169, 170, 171]. The low power electrogoniometer described here is designed using a pair of Impulse-Radio Ultra-Wide Band (IR-UWB) wireless smart sensor nodes interfacing with low-power 3-axis accelerometers. The three analog outputs of the accelerometer are digitized by three individual asynchronous continuous-sampling level-crossing ADCs, which are presented in Chapter 3 - Front-End Circuit Design.

A tri-channel IR-UWB transceiver, as presented in Chapter 4 - Wireless Circuit Design, is implemented in the sensor node for data communication, connecting to

the three digitized outputs of the 3-axis accelerometer. The three channels work independently at three different frequencies. The transmitter sends out short pulses of radio frequency (RF) waves, which are generated by the RF pulse generators and modulated by the baseband generators. The receiver picks up the signals from a corresponding channel and decodes the received signal into digital data. A high resolution successive approximation register (SAR) ADC, as presented in Chapter 3 - Front-End Circuit Design, is also integrated for data conversion of the accelerometers at the receiver end. A real time data processing unit performs on-chip joint angle calculation using the measurements from the two sets of accelerometers at the transmitter site and receiver site, respectively.

5.1.2 Architecture of the Entire System

Fig. 5.1 illustrates a block diagram of the entire system, which integrates i) a neural signal acquisition device, ii) a wireless electrogoniometer consisting of a pair of smart sensor nodes, and iii) a PC interface. A deep brain neural signal is captured and recorded, while the joint angle is measured from a dual-sensor-node system. The relationship between the neural data and sensory data is studied off-line.

The neural signal acquisition device has a size of $43mm \times 16mm \times 15mm$ if battery powered, and a size of $43mm \times 32mm \times 15mm$ if powered by wireless inductive coupling. The neural signal acquisition device, as shown in Fig. 5.2 is developed using off-the-shelf components. It integrates a four-channel analog front

end, a microcontroller, and a 2.4GHz wireless transceiver. The analog front-end integrates four channels of low-noise instrumentation amplifiers followed by a high-precision sigma-delta analog-to-digital converter in each channel. Each channel of the analog front-end has a gain of 45.6dB, a sampling rate of 20kS/s with 8-bit resolution. It has 1.33μVrms per channel input-referred noise, and an 1.2mW per channel power consumption. The digitized data is serially fed through SPI interface to the wireless transceiver by a Nodic Semiconductor nRF24LE1 microcontroller (MCU). The wireless transceiver encodes and transmits the data with an over-the-air data rate of 2Mbps. The receiver device decodes and feeds the data to a PC through a USB port. The neural signal acquisition device is powered by an inductive coupled wireless power receiver module connected to an inductive receiving coil. The Texas Instrument BQ51013B wireless power receiver, which is compatible with the WPC1.1 wireless charging protocol, can be paired with any commercial inductive wireless charging pad. According to its datasheet, the wireless power receiver has a peak AC-DC conversion efficiency of 93% and an overall power transmission efficiency about 70% from the building AC power line to the DC output if placed on top of the charging pad. The maximum output DC power can be as high as 7.5W, which is much higher than the demand from the neural signal acquisition device.

The electrogoniometer is implemented using a pair of wireless smart sensor nodes interfacing to accelerometers for the measurement of the joint angle. The wireless smart sensor node is a customized integrated circuit (IC) which includes

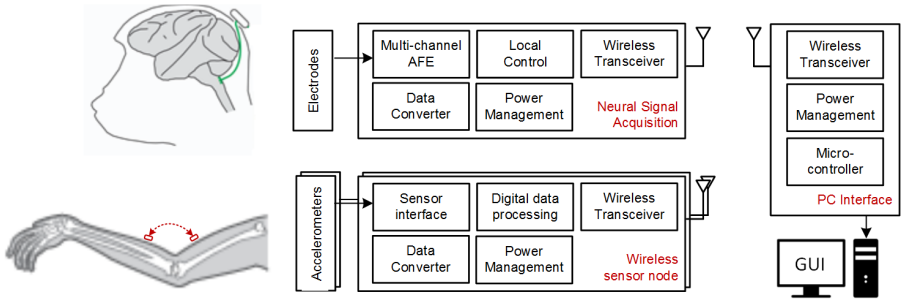
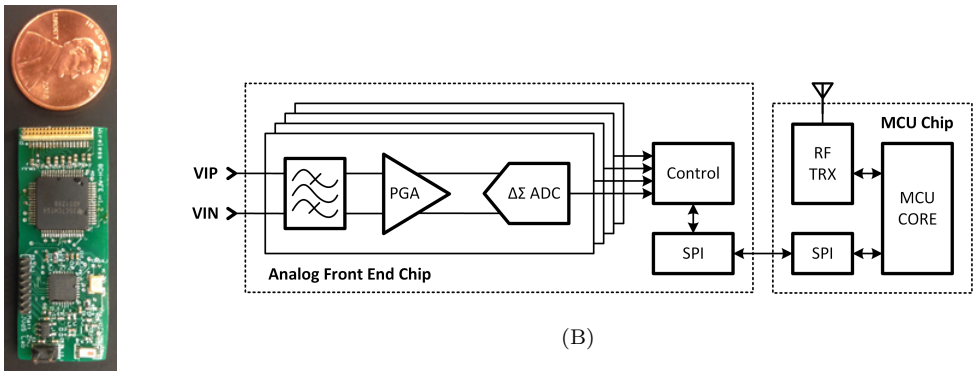


Figure 5.1: Block diagram of the entire electrogoniometer system, consisting of i) a neural signal acquisition device, ii) a wireless electrogoniometer, and iii) a PC interface.



(A)

(B)

Figure 5.2: (A) Photo of the neural signal acquisition device. (B) Block diagram of the neural signal acquisition, consisting of a four channel analog front end, a microcontroller, and a 2.4GHz wireless transceiver.

the asynchronous level-crossing ADC, the SAR ADC and the IR-UWB wireless transceiver, presented in Chapter 3 and Chapter 4, respectively, of this thesis. A sensor interface is integrated as the analog front end in the sensor node. There are two data converters integrated in the sensor node, one of which is a 6-bit asynchronous level-crossing ADC, and the other of which is a 12-bit successive approximation register (SAR) ADC. Different ADCs are used for operations under different working modes. The digitized data can be either sent out through a tri-channel ultra-wide band transmitter, or be read out through a data cable.

5.1.3 Configuration of the Electrogoniometer

The wireless electrogoniometer can be configured to work under different modes, including:

i) High resolution data acquisition mode, as illustrated in Fig. 5.3, which records digitized sensory data from the SAR ADC through a data cable. In this mode, both sensor nodes are powered by external batteries and the wireless transceiver module and digital data processing module are turned off. The sensory data are packaged in an 8-bit MCU. The MCU is configured with one Universal Asynchronous Receiver/Transmitter (UART) serial port for data communication with the PC.

ii) Low power data acquisition mode, as illustrated in Fig. 5.4. Under this low power data acquisition mode, the asynchronous level-crossing ADC is used

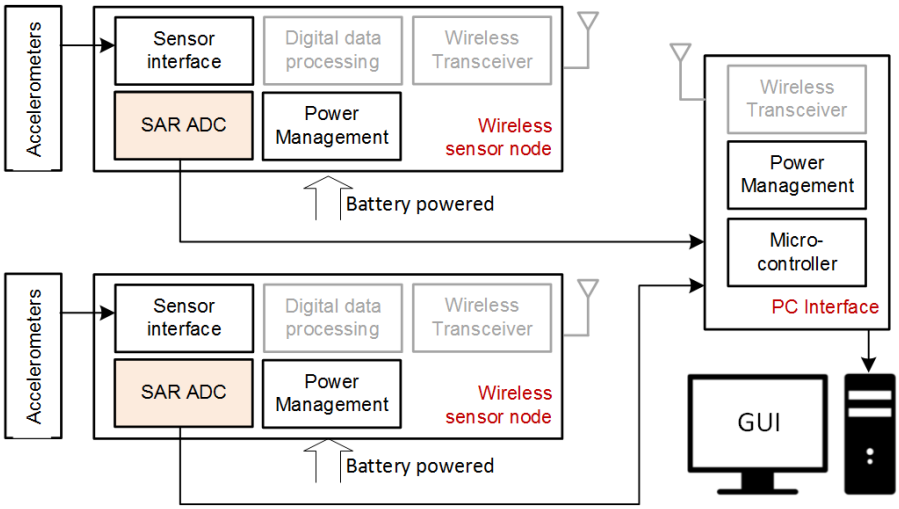


Figure 5.3: Block diagram of the entire system under high resolution data acquisition mode. Digitized sensory data read from the SAR ADC are sent back to the PC through the PC interface board.

for data conversion. The digitized sensory data are wirelessly sent to the PC interface board. The sensor node is powered by a small battery.

iii) The angle measurement mode, as illustrated in Fig. 5.5, in which one of the sensor nodes is configured as a master node, and the other is configured as a slave node. The slave node transfers the sensory data to the master node. An on-chip processing unit performs joint angle calculation using both the sensory data received from the master node and the local sensory data. The calculated results can be either shown on local display or wirelessly transmitted to the PC end. Both the master sensor node and the slave sensor node are battery-powered.

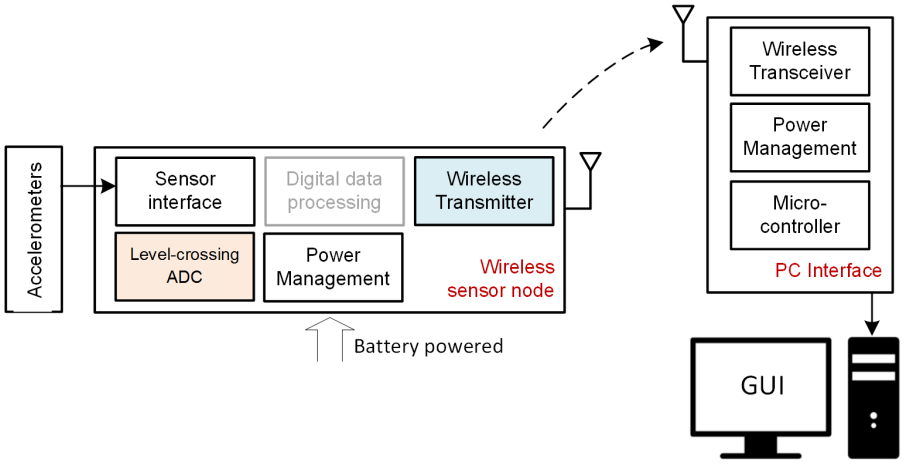


Figure 5.4: Block diagram of the entire system under low power data acquisition mode. The sensory data are digitized using a level-crossing ADC and wirelessly sent to the PC interface board.

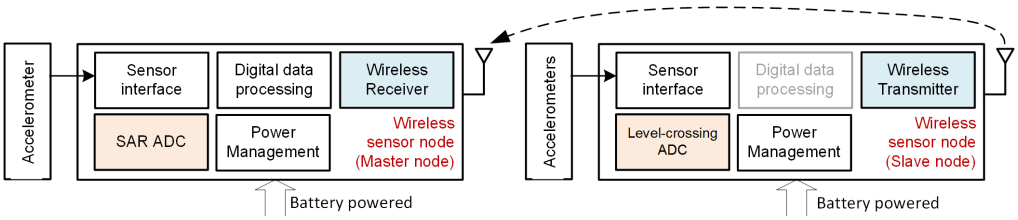


Figure 5.5: Block diagram of the entire system under angle measurement mode. Both sensor nodes are powered by batteries. The joint angle is calculated in the on-chip digital data processing unit.

5.1.4 Static Body Joint Angle Measurement

Fig. 5.6 shows the experimental setup of the dual-accelerometer system for the static angle measurement of a joint between two rigid body segments, S_1 and S_2. Two low power, complete 3-axis accelerometers with signal conditioned outputs are mounted on the two segments.

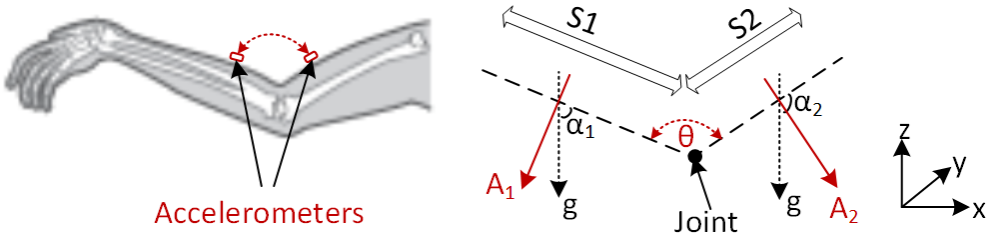


Figure 5.6: Experimental setup of the dual accelerometers system for joint angle measurement. The measured joint connects two rigid body segments, S_1 and S_2.

Define $\widehat{n}_g$ as a unit normal vector to gravity. The measured accelerometer vector is defined as $\vec{A_1}$, $\vec{A_2} \in \mathbb{R}^3$, with respect to the local coordinate system. The cosine of the joint angle, θ, can be written as

$$cos\theta = \frac{\vec{A_1} \cdot \vec{A_2}}{||\vec{A_1}||||\vec{A_2}||} \tag{5.1.1}$$

The calculation of the division is not hardware friendly. In order to make it easier for hardware implementation, comparison between the calculation of

$$\Gamma_1 = \left[\frac{\vec{A_1} \cdot \vec{A_2}}{cos\theta}\right]^2 \tag{5.1.2}$$

and

$$\Gamma_2 = \left[||\vec{A_1}||||\vec{A_2}||\right]^2 \tag{5.1.3}$$

is illustrated in Fig. 5.7. For angle measurements, the accelerometer vector recovered from the receiver, $\vec{A_1}$, and the digitized accelerometer vector output from the local SAR ADC, $\vec{A_2}$, are sent into the digital processing unit through two input buffers. Three dot product calculation units are needed. Since the resolution of the level-crossing ADC used in the slave node is 6-bit, only the 6-bit MSB of the local SAR ADC is used. The resolution of the dot product calculation units are all 6-bit. Sixteen comparisons are implemented digitally, realizing an output resolution of 4-bit of the joint angle. An output stage encodes the calculation result in serial data stream. In order to reduce on-chip workload, uneven level division of θ is applied. The digital signal processing circuit implementation was done by Dr. Milin Zhang from Department of Electrical and Systems Engineering at University of Pennsylvania.

5.1.5 Chip Design

The wireless electrogoniometer is implemented in IBM 0.18um standard CMOS technology. The test chip has a size of $4.5mm \times 1.5mm$, as shown in Fig. 5.8. The active circuits occupies a total silicon area of $0.5mm^2$.

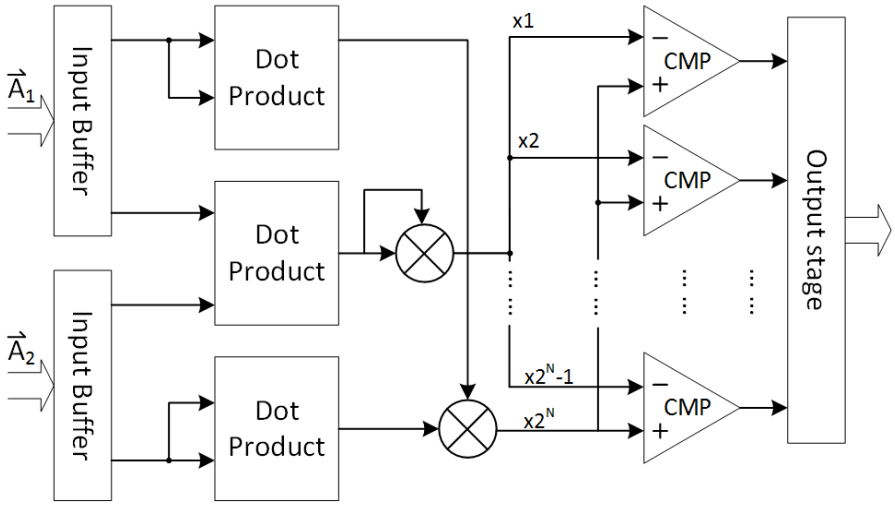


Figure 5.7: Architecture of the real-time joint angle calculation digital processing unit.

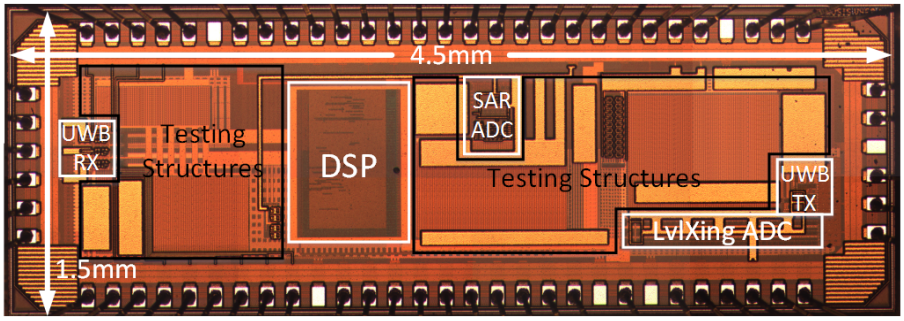


Figure 5.8: Microphotograph of the proposed design.

5.1.6 Data Analysis

The electrogoniometer is designed to quantitatively evaluate the angle between two segments. Two 3-axis accelerometers are used. Due to the sparse yet rapidly changing nature of body movements, the bandwidths of the accelerometer output signals are wide-band and up to kHz range. In this case, a traditional Nyquist sampling rate ADC, such as an SAR ADC, should run at a constant sampling rate of at least twice the maximum signal bandwidth. Data with redundant information are generated when the signal changes much slower than the maximum signal bandwidth. On the other hand, an event-driven level-crossing ADC only generates output data when the input signal changes. Therefore, the data rate will be variable and proportional to the rate of the input signal change. A Matlab simulation has demonstrated that with a 10Hz-5kHz frequency sweeping input signal, as shown in Fig. 5.9, the data throughput generated by the event-driven level-crossing ADC is less than 10% of the data throughput by a Nyquist sampling rate ADC with the same resolution. A scenario study on the data throughput is presented in the next section with in-vivo measured data of body joint movements.

5.1.7 Scenario Data Analysis

Data throughput generated by the asynchronous level-crossing ADC in specific daily scenarios is studied. Two 3-axis ADXL327 accelerometers are each connected to the asynchronous level-crossing ADCs on two sensor nodes. The slave sensor node

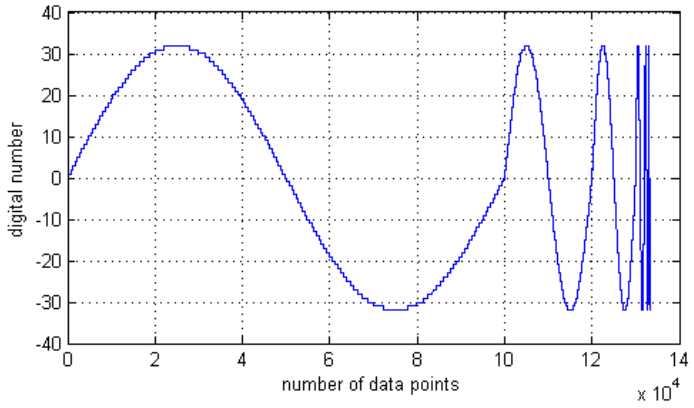
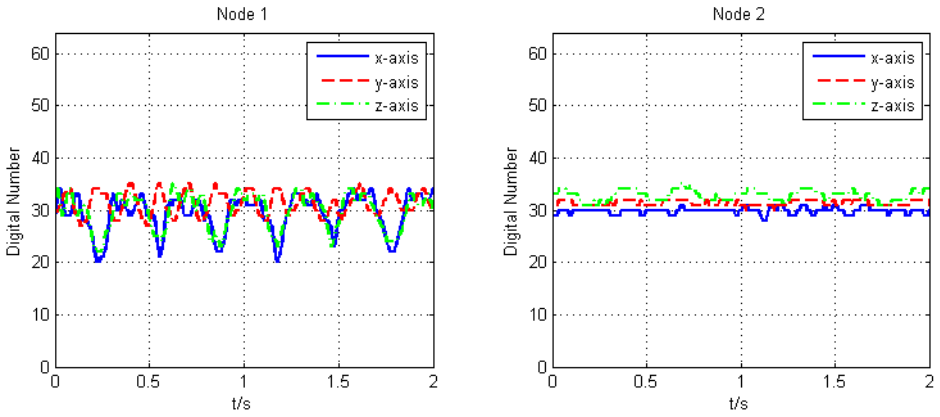


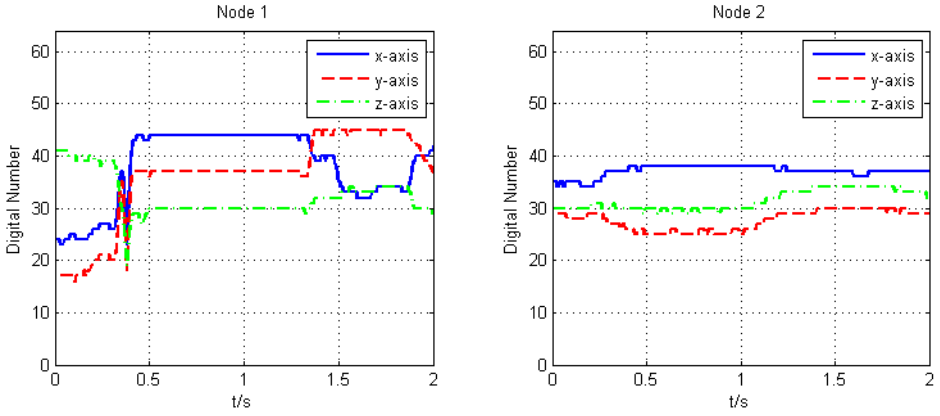
Figure 5.9: 10Hz-5kHZ frequency sweep input signal.

is attached to the chest of a human subject while the master node is attached to the upper arm of the subject. The wireless transmitters on the slave node are connected to the receivers on the master node through RF co-axial cables due to the absence of proper UWB antennas and filters for wireless data transmissions. Since the level-crossing ADC has a tracking speed of up to 1 step change per μs, the measured data is synchronously recorded with a 1MHz sampling clock for storage, digital signal processing, and plotting. Recorded results are plotted in Fig. 5.10. Digitized accelerometer readings are demonstrated for the scenario of (A) walking at a normal pace (Fig. 5.10 (A)), (B) sitting at a table (Fig. 5.10 (B)), and (C) intense indoor movements including jumping and running (Fig. 5.10 (C)).

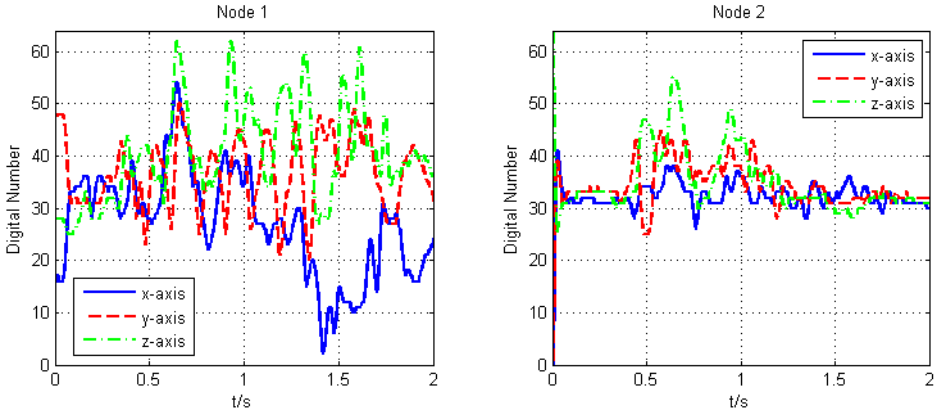
The data throughput generated during a 2s period in each scenario (A), (B) and (C) are 650 bits, 299 bits and 1788 bits, respectively. For comparison, a Nyquist sampling rate ADC with resolution of 6-bit, which is equivalent to the asynchronous level-crossing ADC, needs to be sampled at 10.02kHz to match the input signal



(A)



(B)



(C)

Figure 5.10: Measured results of scenarios of (A) walking at a normal pace, (B) sitting at a browsing the Internet, and (C) intense indoor movements.

bandwidth of the level-crossing ADC. The data throughput of 6 Nyquist rate ADC for all scenarios of (A), (B) and (C) is 721.44kbits. Therefore, in real-life joint-angle and movement measurements, the data throughput generated by the asynchronous level-crossing ADC is significantly lower than the data throughput generated by a Nyquist rate ADC with similar performance. The power consumption of the wireless sensor node system employing the level-crossing ADC can also be much more competitive since the power-hungry wireless transceiver has lower workload.

5.1.8 Conclusion

A wireless fully event-driven electrogoniometer is presented using a pair of ultra-wide band (UWB) wireless smart sensor nodes interfacing with low power 3-axis accelerometers. The two smart sensor nodes are configured into a master node and a slave node, respectively. Low-power asynchronous level-crossing ADCs and an SAR ADC are integrated for the digitization of the analog signal of the accelerometers under different operation modes. An asynchronous digital signal processing (DSP) unit is included on the master node, performing the computation of the joint angle based on local sensory information as well as the information wirelessly recieved from the slave node. A tri-channel UWB transceiver is designed particularly for the data transmission of the 3-axis accelerometers. Experimental scenario data analysis shows higher than 90% reduction of the total data throughput using the proposed fully event-driven electrogoniometer to measure joint angle movements

when compared with a synchronous Nyquist-rate sampling system.

Chapter 6

Conclusions and Outlook

One in every fifty Americans suffers from paralysis, and approximately 23% of the paralysis cases are caused by spinal cord injury [1]. To help the spinal cord injured gain functionality of their paralyzed or lost body parts, a sensor-neural-actuator system is commonly used. The system includes: 1) sensor nodes, 2) a central control unit, 3) the neural-computer interface and 4) actuators. Depending on the applications, a combination of some or all of the blocks in the sensor-neural-actuator system are implemented to compensate for the loss of body functions.

This thesis has focused on a sensor-neural interface and has presented the research related to circuits for the sensor-neural interface. Sensor design, analog front-end circuit design and wireless circuit design are discussed in Chapter 2, Chapter 3 and Chapter 4, respectively. A system integration of the circuit blocks is illustrated in Chapter 5.

The main contribution of this thesis includes: 1) the sensor designs that emphasize power efficiency and data throughput efficiency; 2) the fully event-driven wireless sensor network system design that minimizes data throughput and optimizes power consumption.

In Chapter 2, three sensor designs are discussed, including a compressive sampling image sensor, an optical force sensor and a passive scattering force sensor. The compressive sampling image sensor is optimized for its low data throughput and low power consumption. The optical force sensor is optimized for its sensitivity as well as its ease of manufacture. The passive scattering force/stretch sensor is optimized for its power consumption, physical dimension and manufacturability.

The compressive sampling image sensor combines the advantage of compressive sensing and address-event representation (AER) image sensor into an all-digital address event triggered compressive acquisition image sensor. All the compressive processing is performed during the image capture phase, which eliminates the data converters and also reduces the workload of the readout circuits. The image sensor has advantages in low data throughput rate over the traditional CMOS image sensors. It is more power efficient for applications such as wireless sensor network and Internet of Things. The all-digital nature of the proposed image sensor also allows easier transferability to more advanced CMOS fabrication technologies, in which power consumption will also be scaled.

The optical pressure sensor uses a thin film of PDMS membrane on top of an

optical waveguide that is built in $0.18\mu m$ standard CMOS technology. The optical waveguide has a Si-LED on one end, a SiO_2 optical waveguide channel in the middle and a 3T-photodiode on the other end. The force-induced deformation of the inverse-lenticular structure of the PDMS membrane causes light to escape from the optical waveguide. Experimental results show that the exposure of the photodiode is inversely proportional to the force applied to the PDMS material. Future work for the optical force sensor includes detailed analysis of sensitivity by using different structures on the PDMS material, the effect of the pitch of the structures and the repeatability over time.

The wireless passive scattering force sensor node takes advantage of the back-scattering frequency response of the space-filling-curve tags. In each sensor node, a 2nd-order Hilbert-curve tag (ID tag) is used for sensor node identification, while another 2nd-order Hilbert-curve tag (sensing tag) is used for force sensing. Experimental results successfully demonstrated the feasibility to wirelessly and selectively turn on a sensor node by radiating the corresponding resonant frequency of its ID tag. The resonant frequency of the sensing tag on the selected sensor node is detected by a frequency sweep within the sensing spectrum. The resonant frequency of the sensing tag is then matched to the amount of force applied. Future work on the passive scattering wireless sensor node design includes: 1) complete wireless sensor node and wireless sensor network experiments; 2) further optimization of the gometry; 3) detailed characterization.

Chapter 3 discusses the design of the analog front-end circuit for the wireless sensor network system. First, a low-noise low-power analog front-end circuit implemented in $0.5\mu m$ CMOS technology is shown. This circuit was designed with intracranial neural signal recording in mind, as well as applications for general-purpose small signal detection. Next, a 12-bit 1MS/s successive approximation register (SAR) analog-to-digital converter (ADC) is presented. The ADC is designed for general purpose signal digitization in front-end circuits of the sensor network and is implemented in $0.18\mu m$ CMOS process. Lastly, a 6-bit asynchronous level-crossing ADC realized in $0.18\mu m$ CMOS process is presented, designed specifically for a fully event-driven wireless sensor network system.

The low-noise, low-power analog front-end circuit implemented in ON Semiconductor $0.5\mu m$ standard CMOS technology is designed for intracranial neural signal recording as well as for general-purpose small signal detection. Ultra low noise of the front-end amplifier provides a low noise figure for the system. Sub-Hz to 10kHz bandwidth makes it suitable not only for biomedical signal recording, but also for interfacing to many other types of sensors. 54dB AC gain and 12-bit ADC resolution provide sufficient accuracy of the digitized signal for further signal processing. The low-power consumption makes this analog front-end suitable for power critical applications, such as battery/wireless-powered implanted devices as well as wireless sensor networks.

The 12-bit 1MS/s SAR ADC implemented in IBM $0.18\mu m$ standard CMOS

process is designed for general purpose signal digitization in front-end circuits of the sensor network. A coarse-fine two-stage capacitive DAC structure is realized for small silicon area and low power consumption. Bottom-plate sampling is used to achieve full-swing input signal range while relaxing the design requirement of the comparator. Thick oxide devices are used to accommodate a wide supply voltage range (1.8V-3.3V). This SAR ADC has an ENOB of 10.6 bits and FOM of 195fJ/conversion. It has been used in a wireless fully event-driven electrogoniometer system, as presented in Chpater 5 of this thesis. The ADC has also been used in a video compression image sensor in a collaboration with Jie Zhang, et al., from Johns Hopkins University.

The 6-bit asynchronous level-crossing ADC implemented in IBM 0.18μm standard CMOS process is designed specifically for a fully event-driven wireless sensor network system. The event-driven nature of the asynchronous level-crossing ADC makes it the perfect candidate for digitizing sparse signals, such as neural action potentials and body movements, in a fully event-driven system. The ADC is able to operate with 0.8V to 2.0V supply voltage. The power consumption could be as low as 5μW. Measured SNDR of the ADC is 46.2dB. This ADC is implemented in a wireless fully event-driven electrogoniometer system.

Chapter 4 shows the design of the wireless circuit for the sensor network system. A low-power impulse-radio ultra-wide-band (IR-UWB) transceiver (TRx) is designed for wireless data communication between the sensor nodes. The TRx can operate at

a data rate of up to 10Mbps, with a power consumption of 4.9pJ/bit transmitted for the transmitter and 1.12nJ/bit received for the receiver.

Finally, a wireless fully event-driven electrogoniometer is presented in Chapter 5. The electrogoniometer is implemented using a pair of ultra-wide band (UWB) wireless smart sensor nodes interfacing with low power 3-axis accelerometers. The two smart sensor nodes are configured into a master node and a slave node, respectively. Low-power asynchronous level-crossing ADCs and an SAR ADC are used for the digitization of the analog signal of the accelerometers under different operation modes. An asynchronous digital signal processing (DSP) unit is included on the master node, performing the computation of the joint angle based on local sensory information and information wirelessly recieved from the slave node. A tri-channel UWB transceiver is designed particularly for the data transmission of the 3-axis accelerometers. An experimental scenario data analysis shows higher than 90% reduction of the total data throughput using the proposed fully event-driven electrogoniometer to measure joint angle movements when compared with a synchronous Nyquist-rate sampling system.

The proposed sensor-neural interface in this thesis could be easily adapted to other wireless sensor network systems besides the electrogoniometer. For example, a smart skin sensor network to help recreate finger sensations could be realized by simply placing the wireless sensor nodes on fingers and interfacing the sensor nodes with force sensors. Future wireless sensor node studies should focus on low-

power sensors and circuits, high-efficiency wireless power transfer, as well as the expandability of the sensor network. The recent focus on Internet of Things from the semiconductor industry also provides a great platform for further wireless sensor node developments.

Future studies in neural stimulations will help improve the restoration of different sensations in the central nervous system. Eventually, prosthetics that feel like one's own body parts will emerge. With the rapid growth of the trillion-dollar global healthcare market [172] as well as the advancement in engineering, neurology and medicine, a complete sensor-neural-actuator system will be made clinically available to help patients with paralysis in the foreseeable future.

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