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System and Circuit Level Design and Analysis of a 16-Bit Sigma-Delta ADC for a TETRA-2 Network Mobile Station Application

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Abstract: - This paper outlines a comprehensive design evaluation for development of a 16-bit Sigma-Delta (Σ - Δ) Analog-to-Digital Converter (ADC) for TETRA-2 Network Mobile Station (MS). A step-by-step design approach is described commencing from system-level evaluation leading to the circuit design, which would serve as a useful reference to designers involved with development of ADCs for wireless equipment.

I. INTRODUCTION

Terrestrial Trunked Radio (TETRA) [1] is a digital trunked mobile standard developed by the European Telecommunications Standards Institute (ETSI). The purpose of the TETRA is to meet the traditional Professional Mobile Radio (PMR) user organizations and Public Access Mobile Radio (PAMR) applications e.g. public safety (fire, ambulance and rescue services), transportation, utilities (water and electricity) and government (police, border control and military). Like GSM moving to GPRS, EDGE and UMTS/3G, due to increasing user demand for new services and facilities, the end of 2005 saw new standards being finalized as part of TETRA Release 2 [1]. The Mobile Station (MS) for the TETRA-2 applications is a Time Division Multiple Access (TDMA) based OFDM system, capable of supporting channel bandwidths of 25 kHz, 50 kHz, 100 kHz and 150 kHz [1]. A single ADC design solution therefore must be able to support a channel bandwidth of at least 150 kHz. The modulation schemes supported are $\pi/4$ DQPSK, $\pi/8$ D8PSK, 4 QAM, 16 QAM and 64 QAM.

This paper pertains to a systematic design evaluation for development of a 16-bit Σ - Δ ADC for baseband processing of TETRA-2 MS. Various Σ - Δ ADC designs have been developed to-date for GSM, CDMA and DECT applications, however the design evaluation for the TETRA-2 MS is novel as the TETRA-2 specifications are still in the process of being finalized by ETSI and to the best knowledge of the authors there is no publication on this in the open literature to date.

This paper will therefore provide a valuable reference for designers involved with the development of TETRA-2 radio equipment. A step-by-step design approach is described commencing from system-level evaluation all the way to the circuit design, which is verified by lengthy

HSPICE simulations. Section II describes the Radio Frequency (RF) Front-End (FE) assumed for the receiver. In section-III the system design is analyzed with the circuit non-idealities and nonlinear stability analysis. This is followed by simulation results in section-IV and conclusions are enumerated in section-V.

II. RECEIVER ARCHITECTURE

The receiver designs implemented for wireless applications are the superhetrodyne, low-IF or the zero-IF type [2]. The receiver assumed in this study is a conventional superhetrodyne design [2] as seen in Figure 1. The FE consists of the first-RF filter, Low Noise Amplifier (LNA), second-RF filter (II-RF ϕ) and a mixer. The IF and baseband consist of the IF filter, the Automatic Gain Control (AGC) amplifier with a variable gain and the Quadrature Demodulator that give the In-phase and Quadrature-phase channel inputs to the respective ADCs. The Σ - Δ modulator outputs the digital samples to the SLINK filters [3], [4]. SLINK filters offer considerable advantages in terms of VLSI/hardware implementation for high sample rates [3], [4], [5]. A single-stage down-conversion from the SLINK filter, to the Root Raised Cosine (RRC) filter is employed to offer sufficient attenuation to the adjacent channel interference.

III. ADC ARCHITECTURE

The Σ - Δ ADC architecture is detailed and developed in this section. System level evaluation is undertaken for the design of the Noise Transfer Function (NTF), circuit non-idealities and nonlinear stability analysis. This is followed by the circuit design of the Σ - Δ modulator.

A. Channel Bandwidth and System Design.

The channel bandwidth requirements for the receiver determine what Dynamic Range (DR) and Effective Number of Bits (E_{NOB}) are achieved for various clock frequencies/Oversampling Ratio (OSR). The DR and the E_{NOB} are given by [6]:

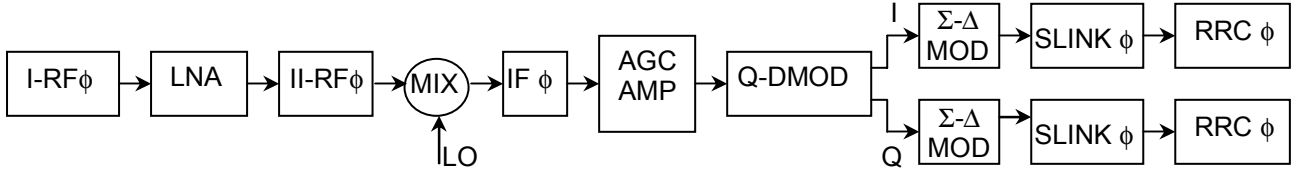


Figure 1. TETRA-2 Receiver

$$DR = 10 \log \frac{3}{2} [2^B - 1]^2 \frac{(2L+1)OSR^{2L+1}}{\pi^{2L}} \quad (1)$$

$$E_{NOB} = \frac{DR - 1.76}{6.02} \quad (2)$$

The minimum required E_{NOB} is dictated by the hardware options available in the DSP/FPGA/ASIC for the system and the RF-FE. The parameters in (1) viz., quantizer bits (B), modulator order (L) and OSR (i.e. the clock frequency) can be changed to achieve the required DR for the minimum E_{NOB} . For TETRA2 the receiver bandwidth f_B is given by (3) [1] where β is the bandwidth expansion factor having a value of 1.125, with $S_B R$ being the symbol rate of 2400 Hz, and N_{sc} the number of the sub-carriers. From (3) the bandwidths obtained are given in Table 1.

$$f_B = \beta \times S_B R \times N_{sc} \quad (3)$$

Parameters	Channel Bandwidth			
	25 kHz	50 kHz	100 kHz	150 kHz
N_{sc}	8	16	32	48
f_B (kHz)	21.6	43.2	86.4	128.6

Table 1. TETRA-2 Channel Bandwidth

Assuming a minimum required resolution of 16-bits, a 3rd-order Σ - Δ modulator would require a clock rate of 8.294 MHz, which is feasible to design and implement. The structure of a 3rd-order Σ - Δ modulator meeting the above requirements along with the coefficient values are shown in Figure 2. The single-loop 3rd-order structure is chosen since it offers a straightforward simple configuration for evaluation and implementation. The Σ - Δ modulator is designed with a lowpass NTF using the 'Cookbook' methodology [7]. The required coefficients are obtained after the desired signal scaling.

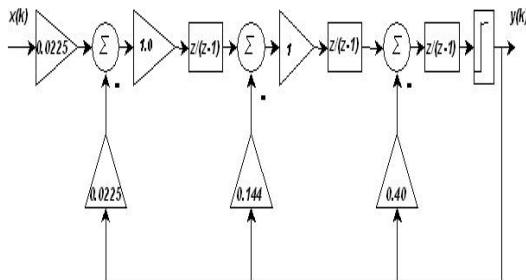


Figure 2. 3rd-order single-loop Σ - Δ modulator

B. Circuit Non-Idealities.

Incorporating the non-ideal blocks and undertaking system level simulations quantify the degradation in the Signal-to-Noise Distortion (SNDR) as a result of the circuit non-idealities. The various nonideal blocks developed in Simulink/Matlab are used for analysis [8], [9]. As a result of the non-idealities, the net reduction in the SNDR is given in Table 2.

Sl.	Parameter	Reduction in SNDR
I.	Sampling Jitter: 15 ns	1.70 dB
II.	Switch thermal Noise	0.62 dB
III.	Input-referred op-amp noise: $30 \mu V_{rms}$	1.75 dB
IV.	GBW: 11.5 MHz 100 kHz	0.00 dB 28.0 dB
V.	Slew Rate (SR): $4 V/\mu s$ $: 1 V/\mu s$	0.00 dB 28.0 dB
VI.	All non-idealities combined	4.50 dB

Table 2. Net reduction in SNDR

The resultant reduction in the SNDR due to all of the non-idealities considered together is 4.5 dB. Therefore the required clock frequency of the Σ - Δ modulator increases to 10.24 MHz from (1) and (2), to account for this reduction in SNDR for a minimum of 16-bit resolution in the baseband, providing us with a safety margin of 5 dB at the same time.

C. Nonlinear Stability Analyses

The NTF of the Σ - Δ modulator is given by [7]:

$$H(z) = \frac{1 - 3z^{-1} + 3z^{-2} - z^{-3}}{1 - 2.2z^{-1} + 1.688z^{-2} - 0.443z^{-3}} \quad (4)$$

The stability analysis is undertaken using the Noise Amplification Curve ($A(K)$) proposed in [10] and established for various Σ - Δ modulators in [11]. The $A(K)$ curve for the Σ - Δ modulator is plotted in Figure 3. The Σ - Δ modulator becomes unstable as $A(K)$ approaches the global minimum value of the curve which is 0.9 [10]. This instability sets in when the equivalent quantizer gain K has a value of 0.75. The stable amplitude limits can therefore be predicted for the NTF for DC, sinusoidal and dual-sinusoidal inputs from the quantizer gain values and the noise amplification curves as explained in [11], for which the values obtained for this Σ - Δ modulator are given in section IV.

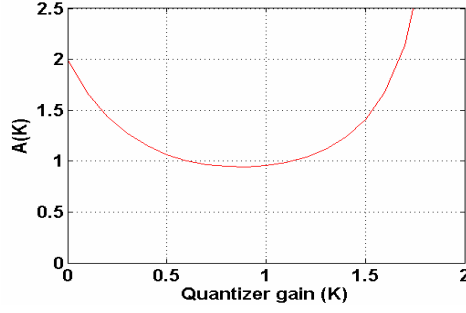


Figure 3. A(K) Curve

D. Sigma-Delta Modulator Circuit Design

The circuit of the 3rd-order Σ - Δ modulator was modelled in HSPICE deploying a 0.35 μm CMOS process in a differential configuration is shown in Figure 4. ϕ_1 and ϕ_2 are the complimentary clocks operating at the OSR clock frequency. The op-amp is a single-stage folded-cascode configuration as shown in Figure 5. One bias I_{ss} provides the drain current of both the input transistors $M1$, $M2$ and the cascade devices $M3$ and $M4$. The two-stage gain boosting is implemented at the transistors $M3$ and $M4$, which increases the output impedance of the differential op-amp. The output impedance in this way can be 'boosted' substantially without stacking more cascade devices on top of $M1$ and $M2$.

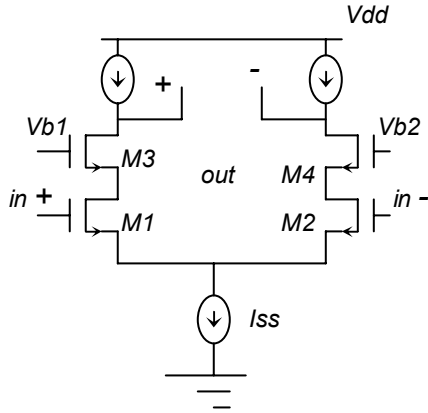


Figure 5. Folded-cascode op-amp

The comparator is designed to be fast and a simple differential amplifier as circuit shown in Figure 6 fulfils this requirement. The integrator settling speed is the only limiting factor for the sampling rate of the Σ - Δ modulator. The Σ - Δ modulator performance is relatively insensitive to the comparator offsets and hysteresis, because these are attenuated by the noise shaping structure of the Σ - Δ modulator.

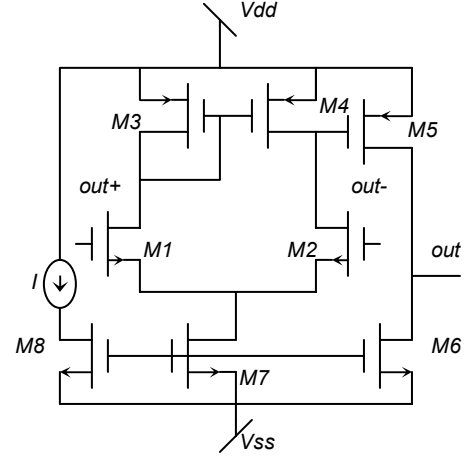


Figure 6. Differential Comparator Circuit

IV. SIMULATION RESULTS

A TETRA-2 OFDM based system has been modeled in SIMULINK for simulations with a RRC filter having a roll-off factor of 0.2 [1]. The 25 kHz channel signal for QAM-4 modulation produced an Error Vector Magnitude (EVM) of 2.5 % without the Σ - Δ ADC, which increased to 4.7 % with the Σ - Δ ADC and is plotted in Figure 7. Since the system is TDMA, in order to obtain the EVM perfect synchronization is required between the transmitter and the receiver. This along with the OSR increases the simulation time considerably. Therefore for the other channel bandwidths (50 kHz, 100 kHz & 150 kHz) the RRC output spectrum was measured and was found to be as per the TETRA -2 specifications.

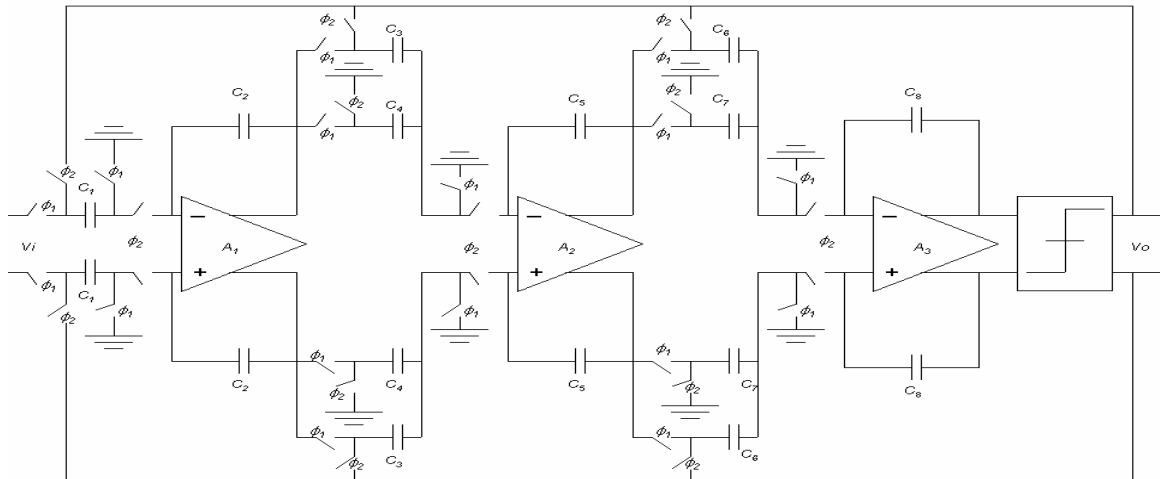


Figure 4. Sigma-Delta Differential Circuit

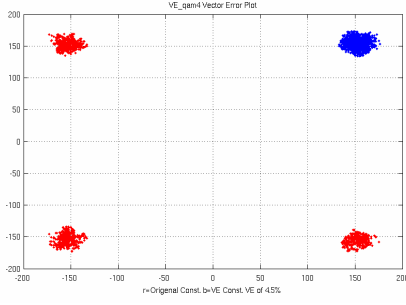


Figure 7. QAM-4 constellation.

For QAM-16 modulation the EVM is plotted in Figure 8. The % EVM is well below the specified 10% limit for TETRA-2 [1].

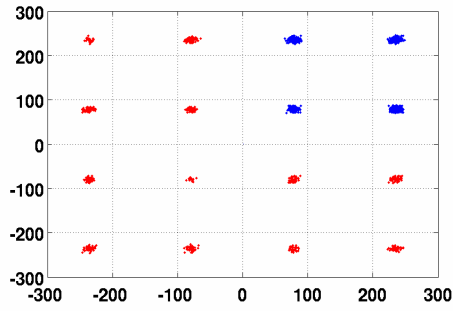


Figure 8. QAM-16 Constellation.

As observed accurate mappings are produced as a result of the correct parameter selection in Table 2. The parameters can be varied in order to observe the effects of degradation, but the same has not been quantified as is considered beyond the scope of this paper.

HSPICE transient analyses were undertaken at a clock frequency of 10.24 MHz. It was observed that the predicted non-ideal SNDR response matches very closely to the SNDR response obtained from HSPICE simulations as shown in Figure 9.

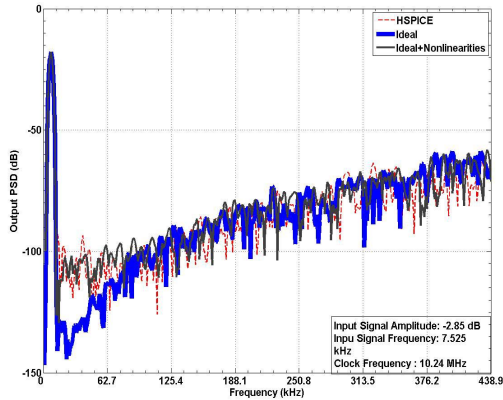


Figure 9. Non-ideal Σ - Δ Modulator Response

To obtain the maximum stable input amplitude limits, simulations were undertaken at 10.24 MHz for which the values obtained are shown in Table 3.

SI	Input Signal	Stable Amplitude Limit	
		Estimated	Actual
I.	DC	0.60	0.63
II.	Sinusoidal	0.80	0.75
III.	Dual-Sine	0.35	0.36

Table 3. Stable Amplitude Limits

The stable amplitude limit obtained by HSPICE simulations for the sinusoidal signal at 7.525 kHz is plotted in Figure 10.

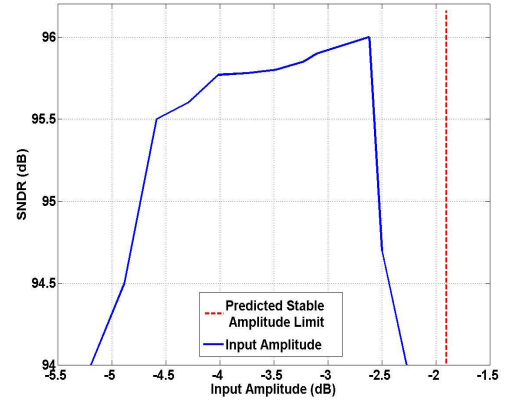


Figure 10. Stable Input Amplitude: Sinusoidal Signal

The step-by step approach for the design analysis in this section is given in Figure 11. Although tonal analysis has been included in the methodology, it has not been explained since the application considered is for wireless. The tonal analysis is applicable for audio applications. The tonal analysis is described in details in [12].

V. CONCLUSIONS

A comprehensive design methodology and performance evaluation of a 16-bit Σ - Δ ADC for TETRA-2 MS is presented and is validated by system and circuit level simulations. The design approach reported here would provide a valuable reference for designers involved with design of Σ - Δ ADCs for TETRA-2 receivers.

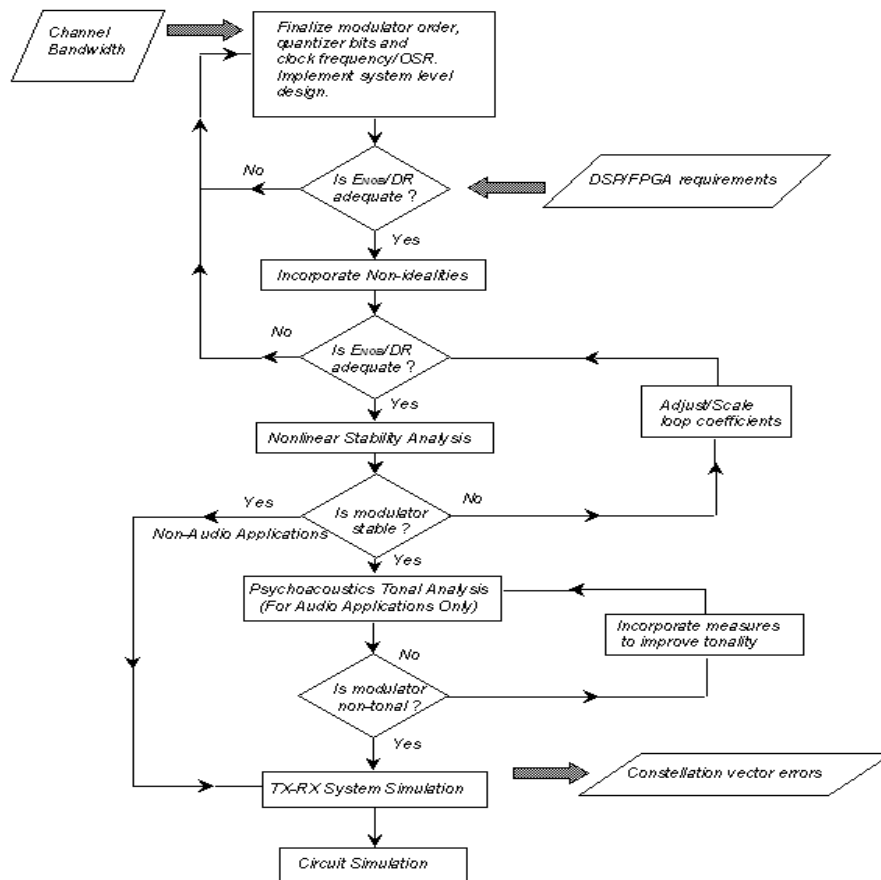


Figure 11. Steps in Design Methodology

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