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Sub-ns Shaping of Switching Transients in GaN HEMT Bridge-legs

Sub-ns Shaping of Switching Transients in GaN HEMT Bridge-legs

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Abstract

The thesis that follows this abstract describes the development of a high bandwidth active gate driving testbed and the investigation of effects that multi-GHz bandwidth gate signals have on the switching of 650 V GaN HEMT power devices. It covers the development of the support hardware required to drive a proto-type active gate driver capable of updating its output impedance every 100 ps to deliver between ± 10 A of gate current. The challenges caused by 150 V/ns and 10 A/ns slew rates on the support circuitry are investigated to select DC-DC converters and digital signal isolators which allow the testbed to be self-immune to the transitions it can produce.

A GUI, in MATLAB, and embedded software, in C and VHDL, are developed to aid creation of resistance sequences for the prototype gate driver, automate double pulse testing and data collection.

Measurement techniques suitable for GaN HEMT devices and optimised power circuits are explored and evaluated. Considerations on the impact of a measurement technique on circuit layout and the parasitic inductance present are explored as this impacts the viability of power circuit current measurement methods.

The testbed developed is used to verify the output of the prototype gate driver and show that the packaging parasitics do not compromise the high bandwidth waveforms. High bandwidth active gate driving is used to demonstrate beneficial control via the gate of <5 KW scale transitions during double pulse tests with 650 V normally-off GaN HEMTs. Reductions in drain oscillation of up to 10% and switch node voltage spectra by 9 dB above 125 MHz were observed depending on the load configuration.

The impact of environmental and electrical operating parameters on the robustness of demonstrated improvements is investigated and discussed. For load current variations of ± 3 A a resistance sequence is shown to keep drain current peak spectral content within 10 dB of the minimum achieved with a fixed gate resistance sequence. Finally, a method is proposed that allows the established resistance sequence to be compensated for changing load current and keep peak spectral content within 5 dB of minimum for a new optimised point.

Dedication

This thesis is dedicated to my partner and significant other, Sam, my family and my friends. They have all supported me in ways they do and don't realise throughout the process of researching and writing this thesis.

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I would like to thank Prof Bernard Stark, Dr Neville ONiell and Dr David Drury for their role as supervisors and all the guidance and support imparted.

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I am grateful to Electrical Energy Management Group at the University of Bristol for being such a supportive environment within which this work was conducted. Particular thanks are extended to Dr Sam Williamson, Dr Jason Yon, Dr Niall Oswald, Dr Philip Anthony, Mr Sam Walder, Mr Dominic North for the encouragement and reassurance given in numerous long conversations.

Author’s Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

Signed:

Date:

Memorandum

This memorandum accompanies the thesis, "Sub-ns Shaping of Switching Transients in GaN HEMT Bridge-legs" and is derived from work carried out by the author and those explicitly stated as contributors where appropriate within the Electrical Energy Management Group in the Department of Electronic and Electrical Engineering at the University of Bristol. The main contributions claimed by this work are the following:

- Investigation into suitable probing and measurement techniques for use with current generation commercially available data acquisition equipment.
- A research testbed capable of investigating the application of 10 GHz effective bandwidth gate signal to 650 V rated GaN HEMT power devices.
- Demonstration of the controllability of GaN HEMTs via the gate connection.
- Demonstration of beneficial switching waveform shaping via the gate connection.
- Demonstration of, given a known good high bandwidth active gate driving resistance sequence, a simple method to adapt it to a change in load current.

Publications

First Author Publications

- J. J. O. Dalton, J. Wang, H. C. P. Dymond, D. Liu, D. Pamunuwa, B. H. Stark, N. McNeill and S. J. Hollis, 'Shaping switching waveforms in a 650 V GaN FET bridge-leg using 6.7 GHz active gate drivers', in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, Florida, USA, 2017.
- J. J. O. Dalton, H. C. P. Dymond, J. Wang, M. H. Hedayati, D. Liu, D. Drury and B. H. Stark, 'Stretching in Time of GaN Active Gate Driving Profiles to Adapt to Changing Load Current', in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, Oregon, USA, 2018.

Co-authored Publications

Journal Publications

- H. C. P. Dymond, J. Wang, D. Liu, J. J. O. Dalton, N. McNeill, D. Pamunuwa, S. J. Hollis and B. H. Stark, 'A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI', *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 581–594, Jan. 2018.

Conference Publications

- H. C. P. Dymond, J. Wang, D. Liu, J. J. O. Dalton, N. McNeill, D. Pamunuwa, S. J. Hollis and B. H. Stark, 'Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns', in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, Wisconsin, USA, 2016.
- J. Wang, D. Liu, H. C. P. Dymond, J. J. O. Dalton, and B. H. Stark, 'Crosstalk suppression in a 650-V GaN FET bridge-leg converter using 6.7-GHz active gate driver', in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, Ohio, USA, 2017.
- J. Wang, M. H. Hedayati, D. Liu, S. Adami, H. C. P. Dymond, J. J. O. Dalton and B. H. Stark, 'Infinity Sensor: Temperature Sensing in GaN Power Devices using Peak di/dt', in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, Oregon, USA, 2018.
- H. C. P. Dymond, D. Liu, J. Wang, J. J. O. Dalton, and B. H. Stark, 'Multi-level active gate driver for SiC MOSFETs', in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, Ohio, USA, 2017.
- S. Walder, X. Yuan, I. Laird, and J. J. O. Dalton, 'Identification of the temporal source of frequency domain characteristics of SiC MOSFET based power converter waveforms', in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, Wisconsin, USA, 2016.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

AGD	*Active Gate Driving*
CMRR	*Common Mode Rejection Ratio*
CMTI	*`Common Mode Transient Immunity*
CSP	*Current Surface Probe*
DAC	*Digital to Analogue Converter*
EMI	*Electromagnetic Interference*
ESL	*Equivalent Series Inductance*
ESR	*Equivalent Series Resistance*
FFT	*Fast Fourier Transform*
FPGA	*Field Programmable Gate Array*
GaN	*Gallium Nitride*
HEMT	*High Electron Mobility Transistor*
LiDAR	*Light Detection and Ranging*
LVDS	*Low Voltage Differential Signalling*
PCB	*Printed Circuit Board*
PGD	*Prototype Gate Driver*
PoL	*Point of Load*
RF	*Radio Frequency*
SiC	*Silicon Carbide (4H-SiC)*
SPI	*Serial Peripheral Interface*
UoB	*University of Bristol*
USB	*Universal Serial Bus*

WBG	*Wide Band Gap*

List of Accepted Terms

Driver Clock Period	*Period of the prototype gate driver VCO*
Fine Drivers	*Asynchronous drivers within the PGD*
Main Drivers	*Synchronous drivers within the PGD*
Resistance Sequence	*Programmed settings for 'main' and 'fine' drivers stored in the PGD*
Switch Node	*The node between two power devices in a single bridge-leg. The output of a bridge-leg.*
Mains Voltage	*Referring DC-link voltages of approximately 400 V*

1. Introduction

1.1. Direction of Modern Power Electronics

The design of modern power electronics, from point-of-load (PoL) converters in computer systems to the motor drives in electric vehicles, is being driven by power density. Greater power is required to be delivered in the same physical dimensions, for the volume they occupy to be reduced to meet packaging constraints, or improved efficiency to reduce the need for active cooling. This requirement feeds into a desire for tighter integration of the power electronics, making products and systems smaller, less costly and potentially have a lower component count. The desire for increased power density is also pushing the limits of what is possible with advanced Silicon power devices; in terms of their electrical and physical properties.

High Switching Losses - Silicon, as a power semiconductor, has a low band gap and critical electric field. Therefore, to block a large voltage, a thick device must be constructed. The thickness required to block high voltage causes high resistance and therefore conduction loss.

Poor High Frequency Switching Performance – To combat the high resistance caused by designing devices to block large voltages, the die areas must also be large to manage conduction losses. Large die areas for low conduction losses cause large gate structure areas which in turn cause large gate-source capacitance. High gate-source capacitance gives high gate charge which means large gate current peaks and which cause losses in the power device and gate driver when switching at high frequency. Large gate structures will also cause large gate-drain capacitance (or reverse transfer capacitance) through which current can be injected into the gate and have a serious impact on performance.

Poor High Temperature Performance – Device leakage currents are high at elevated temperatures due to high intrinsic carrier concentration, which comes about from the lower band gap that Silicon possesses.

Large Output Capacitance - The output (or drain-source) capacitance, caused by the large die areas required to reduce on state resistance, is high. This means, particularly as converter input voltages rise, there is the potential for large amounts of energy to be stored in it. For the device status to transition from a blocking to conducting state the energy must be discharged which can cause high switching losses in the device changing state. The energy must also be sourced or sunk to other parts of the circuit; commonly through a complimentary device where additional losses are incurred or necessitating auxiliary circuitry when used with certain circuit topologies to prevent the device from

failing. This is a problem, for example in silicon super-junction devices which require current injection [1] or diode deactivation [2] circuitry when used in voltage source topologies.

Poor Packaging for High Frequency Switching - The packages traditionally used for silicon power devices are bulky and not optimised for high frequency operation. Large amounts of parasitic inductance in them mean that, even if the device die they contain can switch quickly, the package will not permit this without potentially damaging voltage transients occurring. The large physical size of the combined device and packaging then limits the degree of integration which can be achieved in the wider power electronic system.

If the goal is to increase power density then a promising avenue is raising the switching frequency of power converters. This allows for, independently of the topology employed, bulky passive components such as capacitors, inductors and magnetic cores to be reduced in size and potentially in number too [3]–[5].

Raising the switching frequency and maintaining the desired levels of efficiency requires a new type of semiconductor power device. Wide band-gap (WBG) semiconductors such as Gallium Nitride (GaN) and Silicon-Carbide (SiC) offer solutions to the problems highlighted with Silicon power devices. Just as the low band-gap and critical electric field strength are the source of the limitations in Si, they are the core reason WBG devices offer greatly increased performance.

Table 1 - Semiconductor material properties[1].

Material Property	**Si**	**4H-SiC**	**GaN**
Band Gap (eV)	1.1	3.2	3.4
Critical Field Strength (MV/cm)	0.3	3	3.5
Electron Mobility ($cm^2/V \cdot s$)	1450	900	2000
Electron Saturation Velocity ($10^6 cm/s$)	10	22	25
Thermal Conductivity ($W/cm^2 \cdot K$)	1.5	5	1.3
Intrinsic Carrier Concentration (n_i)	1.9 $x10^{10}$	8.2 $x10^{-9}$	1.5 $x10^{-10}$
Minority Carrier Lifetime (τ s)	$1x10^{-3}$– $1x10^{-9}$	~0.7$x10^{-6}$	~1$x10^{-9}$

Both GaN and SiC both have ~3x greater band gap energies of Si and offer at least and order of magnitude greater critical electric field strength. Therefore, when comparing like-for-like devices a WBG power device will be thinner, have a smaller die area and lower on-state resistance than a similarly rated Si device. This allows for the potential to have low switching losses even at high

[1] All units and quantities are accurate at time of writing and referenced to Si units prior to the redefinition of the kilogram.

switching frequency. WBG semiconductors offer greatly improved high temperature performance up to the limit of Silicon, ~125 °C, and beyond due to low intrinsic carrier concentrations.

The use of emerging power devices addresses almost all of the barriers to progress in modern power electronics in tackling these challenges.

GaN High Electron Mobility Transistor (HEMT) power devices have benefitted from the new packaging methods employed by manufacturers such as Efficient Power Conversion (EPC), who supply package-less passivated dies [6]–[8], and GaN Systems who have developed the GaNPX package [9]. These kinds of low parasitic inductance optimised packaging methods have been key to leveraging the possible performance of GaN but similar fundamental packaging redesigns have not yet been applied to SiC.

Combined with the increased electron mobility and greater saturation electron velocity compared to SiC, shown in Table 1, these packages make GaN HEMTs ideal for increasing speed and high switching frequency applications.

GaN is also promising at lower frequencies and power levels as it allows for more compact layouts that comparable silicon parts. GaN should in time become cheaper than both Si and SiC as GaN can be grown on Si substrates, processed using current Si power device manufacturing equipment (unlike SiC) and will use less wafer area to give the same device ratings as a comparable Si part.

1.2. GaN HEMTs as Power Devices

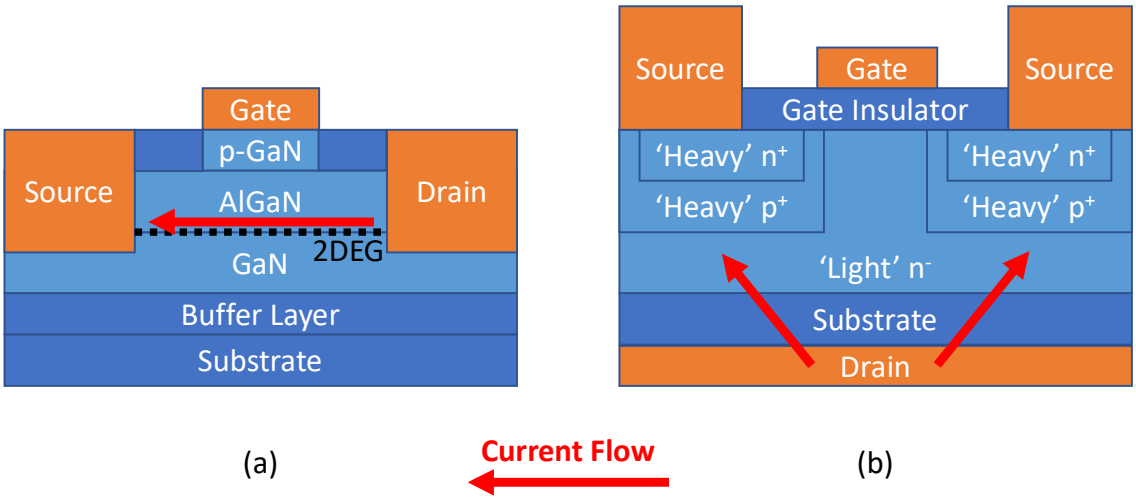

Figure 1 - Diagrams of typical power devices structures for (a) the lateral GaN HEMTs used in this work and (b) conventional vertical Si & SiC MOSFETs.

Unique to GaN is that conduction happens in a small band at the GaN to AlGaN interface where a heterojunction is present, a 2D electron gas (2DEG) formed which is shown in Figure 1(a), and the high electron mobility detailed in Table 1 achieved. Since conduction only happens at the interface

between the materials this means that they are inherently lateral devices as opposed to Si and SiC which are vertical devices when used in power applications. Lateral devices are good for high frequency operation as they can transition from blocking to conducting rapidly due to low vertical thickness giving them small parasitic capacitances.

The GaN HEMTs used in this work are non-cascode normally-***off*** devices as this is desirable for power electronics however HEMTs are intrinsically normally-***on*** devices. Several solutions exist to attaining normally-off HEMTs but both the GaN Systems GS66508P 650 V [10] (See Appendix A) and EPC EPC2015 40 V [11] (See Appendix B) parts in this work use the following approach. p-GaN material, indicated in Figure 3(a), is placed in a trench etched into an insulation layer below the gate contact and above the AlGaN layer. This causes the AlGaN/GaN HEMT to become normally-off and have a positive (gate to source) threshold voltage. The position of the gate structure relative to the source and drain terminals allows the threshold voltage and reverse voltage drop during reverse conduction to be controlled at time of design.

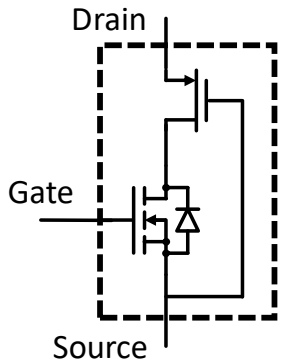

Figure 2 – Representative internal structure of a typical normally-off cascode GaN HEMT showing the upper depletion mode HEMT and lower enhancement mode Si MOSFET.

Another approach, used by manufacturers such as Transphorm, to turn a normally-on GaN HEMT into a normally-off device with positive threshold voltage is to use a cascode structure. A low-voltage Si MOSFET is placed in series with the GaN HEMT as shown in Figure 2 to form a single switch. The MOSFET needs to match the current rating of the GaN HEMT but will only experience the voltages required to turn the HEMT on and off. This allows the cascode structure to have low losses and be a viable solution to creating a normally-off power device.

The cascode structure gives the robustness of a traditional Si MOSFET gate which is tolerant of large gate voltage ranges, approximately ±15 V, that are like SiC MOSFETs too. This is at the expense of a more complex and physically larger power device that is potentially limited by the Si MOSFET performance. The p-GaN gate removes this upper limit but presents an electrically delicate gate

terminal with a typical voltage range of 0-6 V [10], [11] and maximum acceptable limits of approximately -10-7 V. Brief sub-microsecond voltage transients outside of these limits can be acceptable but are manufacturer specific like the specific voltage range which the gate can tolerate.

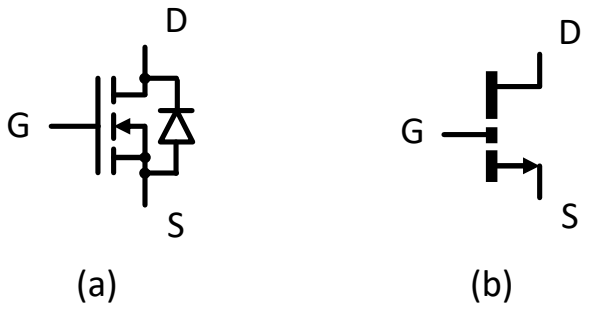

Figure 3 - Symbols for functionally similar normally-off power devices which block positive drain-source voltage, turn-on due to a positive gate-source voltage and exhibit diode-like off-state reverse conduction. (a) is a depletion mode n-channel MOSFET and (b) is the symbol used by GaN Systems and this work to denote a GaN HEMT.

Both Si and SiC MOSFETs possess a parasitic anti-parallel diode, seen in Figure 3(a), which acts as a reverse conduction path when the device is turned off. Devices are available with discrete co-packaged diodes to reduce the losses of the parasitic diode structure. HEMTs like those used in this work, shown in Figure 3(b), lack the intrinsic diode and so are drawn without one. They do, however, have a reverse conduction mechanism that results in 'lossy' high voltage drop diode like behaviour. Reverse biasing the drain-source terminals, to approximately 1.5-2 V for EPC and GaN Systems HEMTs, causes the channel to turn on and conduct. If a negative off-state gate-source voltage is applied to help prevent accidental turn-on it will add to the reverse voltage drop across the device during diode-like behaviour. This makes the use of negative off-state bias undesirable for non-cascode GaN HEMTs.

GaN HEMT power devices, from EPC, were initially introduced at low, ~100 V, ratings to capture the PoL converter [12]–[14], market where power density is the primary driving factor. During this work mains voltage 650 V rated parts were introduced by GaN Systems in ~2015 which enabled the work in Chapters 3 and 4 of this thesis to be conducted. It is expected that GaN power devices in non-cascode configurations will reach 900 V above which SiC will take over as the WBG semiconductor material of choice for power devices. This is due to it being expected that a ≥900 V GaN HEMT would require a change to a vertical device structure which is under active investigation but not yet as mature as current lateral devices [15].

1.2.1. Non-Power Applications

Application areas such as LiDAR and solid-state LiDAR have made widespread use of < 100V GaN HEMTs. The small size and low R_{ds-on} makes them ideal candidates for the high-power pulse

generators required. RF applications where very high switching frequencies are required are another popular use of GaN HEMTs. The fast switching and small parasitics make it useful for generating the bursts of GHz range RF bursts like those in pulsed Radar or creating the switching supplies for envelope tracking RF power amplifiers.

All these areas harness low voltage GaN HEMTs or application optimised RF GaN power devices, high voltage normally-off GaN HEMTs have not yet seen wide adoption. The ability to control the devices at switching speeds well above the speeds required for mains voltage, 400 V DC link, power electronics has then been well demonstrated [16], [17]. However, comparable transition durations over greater amplitude causes vastly increased slew rates for voltage and current waveforms in the order of 2-3x. This complicates several areas related to reliable implementation of power GaN HEMTs as well as performing in-circuit measurements.

1.3. Switching Trajectory Management & Active Gate Driving

EMI production and the non-ideal switching features which cause it such as overshoots and oscillation have been addressed in the past for Silicon power device based converters in a number of ways. The most prevalent of these are auxiliary networks such as dissipative snubbers in the power circuit or voltage clamps in the gate conduction loop [18]–[22]. Such networks use passive and active components to regulate the shape of the device gate waveforms or power circuit switching waveforms.

These more traditional forms of auxiliary networks are outside the scope of this work and their impact on wide band gap power electronics is not covered in this thesis. A promising alternative solution in literature is active gate driving (AGD). Active gate driving can mean a broad spectrum of techniques, but widely involves adjusting the gate voltage or current to the gate of the power device to control the switching action during turn-on or turn-off transitions more precisely.

Ways of achieving this can be broadly grouped into analogue, digital or hybrid methods with open-loop and closed-loop implementations lying within. Irrespective of the implementation method, the impact they aim to have on the connected power circuit generally falls into one or more of the following categories:

dv/dt and di/dt control – managing the switching trajectory of the power device

Current and Voltage sharing – in parallel or series combinations of power devices there is a need to ensure all devices switch at the same time to prevent damaging individual devices or causing cascade failures.

Loss Management – Such as thermal balancing between power modules. Due to their location within a converter cooling system at high load they may not all be cooled equally. As power devices age the switching performance can drop too which may cause unequal heating amongst devices or modules.

Electrical stress reduction – Voltage and current overshoots are common in switch mode power conversion, but left unchecked they can cause device failure and premature aging due to thermal transients which leads to failure [23]. Overshoots also contribute towards the EMI generated by the converter in operation as they inevitably result in periods of high waveform slew rate.

Oscillation control – oscillations in the power waveforms are a major contributor to the EMI produced by a converter. At the switching and ringing frequencies present in GaN based converters conventional methods developed for silicon using passive filter networks are no longer sufficiently effective. Even in cases where their deployment is effective, they introduce another source of loss and increase the volume of the converter, decreasing power density and efficiency.

These five main areas are the same areas which snubbers and auxiliary gate networks have been used to control. However, AGD aims to accomplish one or more of them simultaneously without the need for extra components or as great of a loss in maximum achievable efficiency.

1.4. Challenges posed by GaN HEMT power devices

Many of the problems previously described in this introductory chapter are becoming exacerbated, and new ones introduced when using GaN HEMT power devices, as described below.

Increasing switching frequency and slew rates: The move to GaN HEMT power devices brings increased switching frequency and significantly increased slew rates compared to Silicon. These together exacerbate issues relating to overshoots and oscillation of parasitic circuit elements. The problem of unwanted oscillation is further complicated by the spectral content of the waveforms shifting further up the frequency range where emitted and conducted EMI limits are stricter.

The requirement to address power circuit waveforms: Since the power circuit waveforms contain more energy and have traces long enough to act as antennae for the frequencies they are conducting, they should be addressed in preference to the gate circuit waveforms. This can be to make the circuit self-immune (i.e. it doesn't interfere with itself and cause problems such as crosstalk) or to control radiated electromagnetic interference (EMI) The techniques mentioned for controlling power circuit waveforms typically fall into either dissipative or regenerative (also known as resonant) types [18].

Dissipative and regenerative snubbing techniques are no longer wholly appropriate: Dissipative techniques will absorb the energy contained in the parts of the waveforms to be suppressed to

dissipate them as heat. Regenerative types will allow a portion of the energy in overshoots and oscillation being suppressed to be recovered; usually to the DC link or held within itself to be supplied during the next switching cycle. For future power electronic systems dissipative types need to be discarded completely as they occupy large amounts of space to be able to dissipate energy as heat. Additionally, since they can only waste energy from suppressed features, they limit maximum efficiency more than regenerative snubbers.

At the very least regenerative techniques should be used but they suffer from the same problems as dissipative methods. The current generation of passive components such as capacitors, inductors and ferromagnetic cores, become lossy at the frequencies expected with GaN HEMT based power conversion.

1.5. The ideal solution for GaN devices

If a converter could be ideally controlled, it would not generate the non-ideal waveform features which are to be suppressed. This could be more efficient than generating and suppressing them in a lossy way. Even if no overall boost in efficiency is gained, power density can be increased as fewer components take up less area and PCB layouts can be optimised further.

Therefore, the best solution would be to prevent the generation of non-ideal ideal switching features in the first place. Active gate driving, if applied to GaN successfully, could be the answer to allowing this; this thesis explores this possibility.

2. Literature Review

2.1. High Bandwidth Measurement Methods for Power Electronics

Active gate driving for GaN HEMT devices will be required to counteract undesirable device behaviour multiple times during a switching transient, or even multiple times within a single unwanted feature of a transient, such as a cycle of a 500 MHz oscillation. Therefore, in theory, sample rates and bandwidths that far exceed 10 GHz are necessary to visualise active gate interactions and resulting power waveforms perfectly. As the measurement requirements also include high dynamic range and common mode rejection, off-the-shelf measurement has important limitations, and various reported methods have been adopted to maximise measurement capability for research on GaN and other fast power technologies [24]–[26].

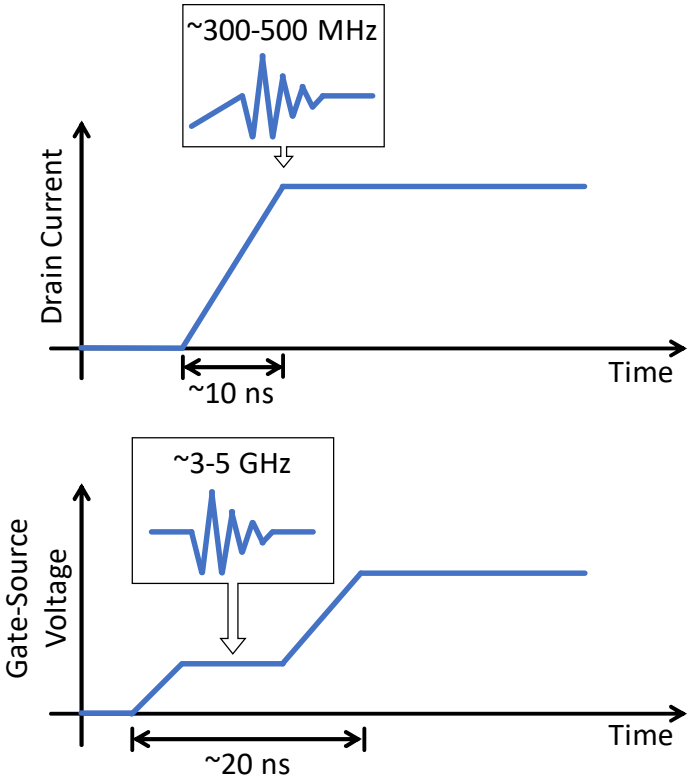

Figure 4 - Idealised drain current and gate voltage waveforms representative of a GaN HEMT turn-on transition with areas of high frequency content highlighted.

Figure 4 illustrates the core problem being faced in measurement of modern power electronics operating under the influence of high bandwidth active gate driving. Not shown, but also important, is the idealised drain-source voltage waveform which has similar time scales and features to the drain current. If power circuit ringing in hundreds of MHz is to be corrected it can be assumed that control must be exerted at an order of magnitude faster in the low GHz range.

The primary method for monitoring activity within a power converter is voltage and current waveform capture. The bandwidth of the measurement systems, measurement loop inductance and probe tip capacitance are highlighted as factors which must be considered in [26]. It asserts that even the highest bandwidth passive voltage probe, a 1GHz Tektronix TPP 1000, available at the time and today has insufficient bandwidth to capture accurately all the desired waveform features. The voltage probe's limitation depends upon circuit configuration and nature of oscillations and transients present. However, amplitude accuracy of waveforms captured must be considered in the context of the frequency content during experimentation for even state-of-the-art conventional measurement techniques.

Covered in [26] is the impact of probe-to-PCB impact, particularly that a large current loop area caused by poor ground connection has the potential to reduce a probe's useful bandwidth by as much as 80%. Even when a 'good' ground connection technique is used, a reduction of 20% of useable bandwidth is reported for the same TPP 1000 1GHz probe thus highlighting the importance of this for any measurement system.

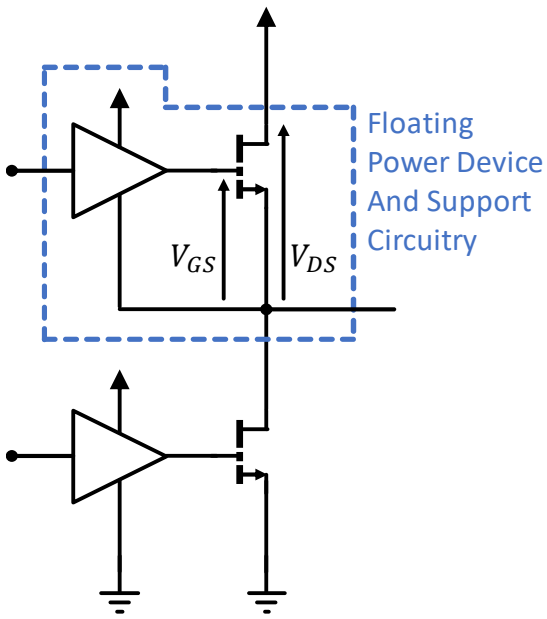

Figure 5 - Illustration of a bridge-leg switching cell, from which converters can be built, indicating the floating region and power device voltages referenced to the switch-node.

Power converters typically have isolated 'floating' regions, seen in Figure 5, which require measurements to be taken under the influence of large common mode signal components. The shortcomings of a possible pseudo-differential solution involving two single ended measurements are laid out in [26] and the Common Mode Rejection Ratio (CMRR) requirements of an isolated differential measurement discussed. The state-of-the-art 1 GHz Tektronix IsoVu TTVM1 differential probe is

compared against a traditional 200MHz active differential probe and shown to have ~2000x lower error due to limited CMRR at full bandwidth. The ability to make high bandwidth floating measurements allows for the first time, insight to be gained into the behaviour of floating regions of GaN based switch mode power electronics. However, as highlighted previously in [26], even 1 GHz of useable voltage waveform measurement bandwidth is insufficient for capturing the full dynamic range of waveforms which can exist.

Untouched upon in [26] is the need to measure current in the main conduction loop or gate loop of a WBG bridge leg. The high bandwidth requirements for voltage measurements carries over to current with power circuit waveforms requiring high bandwidths in the order of 1-2 GHz [27] for current generation GaN HEMTs. A shunt or hall effect current probe are conventional methods for measuring current but must be inserted into the current conduction path resulting in large insertion impedance which can significantly impact the switching performance as shown in [28].

Co-axial current shunts can be used to minimise this effect by being designed with minimal additional current loop area but still introduce multiple nH [27], [28] of insertion impedance. Though small this can be as much loop inductance as an optimised power loop design has naturally[29], [30] and consitutes. Custom made co-axial current shunts that are designed to be electromagnetically small such as those in [31] have outperformed commercially available parts such as the state-of-the-art one available from T&M Research. Rise times 8-30x faster than the 10 mΩ commercial shunt used in [31] were achieved which allowed for far higher fidelity measurement of the GaN HEMT bridge-leg output current.

High-fidelity measurements with current shunts are limited to ground referenced measurements unless a differential probe with high bandwidth and CMRR such as the TTVM1 discussed in [26] is used in conjunction with them. Even then they still introduce large insertion impedance, layout impact and have limited power rating therefore, alternative methods such as current surface probes (CSPs) [32], [33] or Rogowski coils [25], [27], [32], [34] are attractive. Both offer very low, potentially sub-nH, insertion impedance with the lowest reported at 0.2 nH for the differential planar Rogowski coil used in this work. They can be fully PCB integrated [27] or designed to be removable [25], [32], [34]; the removeable probe featured in [25] and used in this work requires only a 4 mm x 3 mm section of outer layer trace and has a useable bandwidth of ~225 MHz. That bandwidth is limited by the loading effect of the passive voltage probe attached to its output but is 2-4x higher than reported for techniques with similar insertion impedance.

Both CSPs and Rogowski coils provide only AC information which is less useful in the characterisation stage of converter design as it requires processing intensive integration to reconstruct DC information. This process also makes the measurements susceptible to DC offset error where the output of the sensor, as recorded by the data capture system in use, is not zero when there is no AC current present. DC error at the input of an integration over time will cause a cumulative error at the output which is normally characterised by a ramp of positive or negative gradient superimposed on any desired signal resent.

Band-pass filtering of signals being measured to block out-of-band components combined with large numbers of time domain averages have been shown to extend the useable bandwidth of a measurement system [24].

This work intends to examine hard switched GaN Switching transients which have not been artificially slowed down, in line with literature it is expected a switching transient can occur in 10-25 ns [12], [35], [36]. To be able to place at least 10 sample points on a fast transition would then require at least 500 MHz bandwidth and 500 MSa/s. This however would be 500 MHz to the -3dB point of the oscilloscope's response, which means amplitude accuracy over the range is compromised. Exceeding this by 2-5x gives a reasonable over-specification of the bandwidth resulting in 1-2.5 GHz and, by giving 10 sample points at maximum bandwidth, 10-20 GSa/s sampling rate.

Table 2 - State of the art oscilloscopes within the scope of this work.

Oscilloscope	Bandwidth (50Ω)	Sample Rate	Channels	ADC Bits / ENOB	Rise/Fall TIme (50Ω)
Rohde and Schwarz RTO 2064	6 GHz (2 chan) 4 GHz (4 chan)	> 20 Gsa/s (2 chan) >10 Gsa/s (4 chan)	4	8 / 7.0	76 ps
Rohde and Schwarz RTO 2044	4 GHz	> 20 Gsa/s (2 chan) >10 Gsa/s (4 chan)	4	8 / 7.0	100 ps
Tektronix MSO64	8 GHz (4 chan)	> 25 GSa/s	4	12 / 5.9 (4 GHz)	50 ps
Keysight Infinium MSO S-804A	8 GHz	> 20 Gsa/s (2 chan) >10 Gsa/s (4 chan)	4	10 / 6.4	53.8 ps
Keysight Infinium MSO S-604A	6 GHz	> 20 Gsa/s (2 chan) >10 Gsa/s (4 chan)	4	10 / 6.8	71.7 ps
Teledyne LeCroy HDO9404	4 GHz	> 40 Gsa/s (2 chan) >20 Gsa/s (4 chan)	4	10 / 6.8	100 ps

Considering the derived specification informed by the literature reviewed, the state of the art for oscilloscopes which satisfy these criteria can be summarised by Table 2. The Rhode and Schwarz RTO 2000 Series, Tektronix MSO 6 series, Keysight Infinium S-series and Teledyne LeCroy HDO9000 series oscilloscope are comparable pieces of equipment at broadly similar price points.

The oscilloscopes used for this work, a Rhode and Schwarz RTO 1024 and 1044, are like the RTO 2044 listed in Table 2 with the RTO 1024 having reduced bandwidth of 2 GHz.

2.2. Gate controllability of GaN HEMT Power Devices

Active gate driving uses more complex gate signals than conventional switching, and therefore, places significantly higher requirements on responsiveness of the device to gate signals. To some extent, the responsiveness of GaN HEMTs has been tested in several areas of research (e.g. LiDAR, Radar and Envelope Tracking).

LiDAR (Light Detection And Ranging) is a prime target area for the application of GaN HEMT power devices. The pulse generators and light sources used in LiDAR typically operate at low voltages which allows for mature <100 V rated non-cascode GaN HEMTs to be used which were the first to be widely available. The use of wide band gap power electronics has allowed for increased maximum and decreased minimum ranges along with improved distance resolution [37].

Compared to the silicon devices previously used in LiDAR applications, GaN HEMTs allow the pulses to be shorter and more precisely defined; this allows for better minimum sensing distance and distance resolution respectively. For a given size PCB footprint GaN HEMTs allow larger current pulses which give more intense pulses of light. The pulses can then travel further and remain detectable upon their return which gives increased maximum range [37].

Typical pulses generated in emitter drive circuits for LiDAR have the following characteristics; switching transitions last < 2 ns and have an on duration of < 10 ns. They are typically < 100 V in magnitude and driving the LED or laser emitters with current pulses of < 100 A. The GaN devices are typically switched between blocking and fully enhanced states, with linear operation only occurring transiently, to generate < 50 V/ns and < 15 A/ns slew rates [16], [17], [37]. This must all be done whilst driving the delicate gate of the GaN HEMT in such a way as to not damage it. Application notes from one of the leading manufacturers of normally-off GaN HEMTs, EPC, stress the importance of the gate driver and PCB design to protect the delicate gate structure of the devices [38], [39].

LiDAR applications have been able to drive GaN HEMTs with conventional gate drive because the slew rates experienced are relatively low compared to 400 V DC GaN power circuits which exhibit slew rates

of 100-150 V/ns and 10 A/ns. In LiDAR applications high bandwidth active gate driving has not been required to harness the benefits of GaN HEMTs, but this thesis intends to explore its application at high voltage.

Pulsed radar is another high-speed application of GaN and is similar to LiDAR and other Time-of-Flight ranging systems from an operational point of view. GaN HEMTs are being used in the high-power radio frequency (RF) generators to produce the bursts of RF as replacements for Gallium Arsenide (GaAs) and other older device technologies. Both GaN and SiC wide band gap power semiconductors are promising replacements for older Si (Silicon) and GaAs power devices in high frequency operation required for radar. GaN for radar applications performs better than SiC [40] because current flows in a 2D electron gas (2DEG) which is an un-doped region of semiconductor. This means HEMTs not only change from blocking to conducting, and vice versa, rapidly but have very low R_{DS-ON} due high electron mobility within the 2DEG. SiC devices, on the other hand, conduct current in a doped region of the device which means there is lower electron mobility and therefore makes them exhibit low gain at RF frequencies. The lower electron mobility of SiC also gives higher on-state resistance which leads to low efficiency in RF amplification [40]. The gain of the devices at high frequency is related to the drift region velocity in the saturated operating mode. In GaN this velocity is higher and therefore it has the potential to have higher gain at RF frequencies.

For high power there is a desire to bias RF GaN devices up to 150 V, however, there are limited devices capable of supporting this [40]. As a result GaN for RF applications is limited to 100 V in comparison to GaN HEMT power devices which have reached and exceeded ratings of 650 V due to them being optimised for their respective applications [40]. They have been reported for use in UHF to K band radar systems operating from 0.5 – 27 GHz at powers ranging from tens of watts to kilowatt scale with the potential demonstrated for multi-kilowatt GaN based power amplifiers [40]–[47]. The growing of GaN HEMTs on diamond substrate has shown that breakdown voltages can be lifted to 165 V for a device capable of 770 mA/mm current density [48]. The use of such a substrate allows for higher thermal conductivity compared with Si or SiC with the device reported in [48] achieving 1.5 $K \cdot mm/W$.

For pulsed radar applications high power sinusoidal bursts are produced at the designed frequency of the system. The burst durations and PRFs (Pulse Repetition Frequencies) vary depending on the maximum unambiguous range the system is designed to operate at; the order of hundreds of kilohertz is typical (e.g 100 – 400 KHz) [49].

Envelope tracking is a method for improving efficiency of RF power amplifiers for modulation schemes which encode information in the amplitude of the output signal. It involves continuous variation of the supply voltage of the RF power amplifier to within a small margin of the minimum required to transmit a given input signal. This means the power amplifier operates in saturation rather than the linear region where it will have to dissipate large amount of power. High data rate modulation schemes used in 4G/5G with high peak to average power ratio and wide modulation bandwidth would cause the power amplifier to spend a long time at high back off. Therefore, envelope tracking power amplifier supplies are required to maintain efficiency.

Both the fast switching speed and smaller size of GaN HEMTs have allowed the improvements demonstrated with its application to envelope tracking RF PAs. The inherent ability of GaN HEMTs to switch quickly means they can track the envelope of the signal to be amplified more closely and over a greater bandwidth. The smaller size of GaN devices allow the power density to be increased and circuit parasitics, which influence the modulation bandwidth, to be minimised.

GaN HEMTs in envelope tracking supplies have been reported to switch at up to 200 MHz [50]. They are then modulated to provide envelope tracking bandwidths up to 80 MHz [51]. Operating voltages are typically <100 V with 24 V to 50 V being a common range [50], [52]–[54]. Slew rates as high as 152 V/ns have been reported for a 50 V transition [52].

The GaN HEMTs used in envelope tracking power supplies are typically used in switched mode, changing between the cut-off and saturation region rapidly, to maximise supply efficiency. Single or multi-phase buck converter and switched capacitor converter topologies have been reported as viable options for envelope tracking supplies [50], [51], [54], [55].

These applications show that it is possible to control the switching transition of GaN HEMTs reliably at the slew rates and frequencies required to not artificially limit performance in kilowatt scale switch mode power conversion. The ability to switch safely further suggests that R_{DS-ON} optimised GaN HEMTs, for power conversion applications, may be controllable with gate signals of sufficiently enough bandwidth. This requires a step up in the test bed design approach and techniques for using GaN at high speed in power electronics. A further step up will then be required to apply active gate driving at mains voltage and the associated slew rates.

2.3. Achievements in High-Bandwidth Gate Driving

The required bandwidth for active gate driving of GaN devices, and their delicate gate structure, make analogue and digital control methods challenging to implement. A number of high-speed, complex gate driving methods have been reported, to achieve an impressive range of benefits. Notable

amongst them are electrical stress reduction, loss management, slew rate control, oscillation reduction and current and voltage sharing amongst series and parallel devices.

The focus of this work is on GaN HEMTs and as such the review covers work directly related to or applicable to GaN and other fast switching device technologies (e.g. SiC).

2.3.1. Electrical stress reduction

GaN devices have no ability to support overvoltage scenarios and avalanche like traditional Silicon MOSFETs [7]. Due to their construction a process, surface breakdown, like dielectric breakdown occurs and they catastrophically fail with even a small over-voltage condition across their drain-source and gate-source terminals [56], [57]. Therefore, whilst driving them as quickly as possible, it is critical that voltage stresses to be controlled and reduced so that transient conditions don't immediately cause device failure. Current stresses, for example transient current pulses at device turn-on, can cause thermal transients that, for a material like GaN which has low thermal conductivity (1.3 $W/cm^2 \cdot K$), is problematic [23], [58]. Thermal transients could cause immediate junction over-temperature conditions or prematurely age novel composite packages made of materials with differing thermal expansion coefficients.

Work conducted with a sub-type of GaN based power devices, gate injection transistors, has shown that they are very robust to short circuit induced current pulses [59]. Devices were shown in that work/reference to withstand pulses more than 80% of their rated voltage for tens of microseconds. This must however be designed into the gate driver network but can be done without sacrificing switching performance and, for the 600 V devices investigated, makes GaN more promising compared to SiC in application.

Therefore, active gate driving specifically targeting the limitation of current and voltage overshoots is popular.

High bandwidth active gate driving with digitally controlled active drivers connected to one bridge-leg of a full-bridge 1700 V 150 A Si IGBT based inverter can dramatically reduce voltage overshoots under PWM operating mode [60]. During continuous switching the active driving method and pattern tuning method proposed was able to suppress V_{ce} overshoot by as much as 64% to within 10% of input voltage [60]. More specifically, when operating in boost mode with current flowing into the switch node and the lower switch is turning on, the lower switch overshoot was reduced by 44% and the upper switch by 64%.

dv/dt control of 600 V GaN HEMTs with an active gate driver allowed independent control of the peak gate voltage experienced during turn-on or turn-off to prevent damage to the power device [61]. The turn-on gate voltage could be held in the range 7.2 - 8.8 V over the full turn-on dv/dt range and 7.36 V across the entire turn-off dv/dt range.

These dv/dt ranges are however still slow for the GaN HEMTs used which are capable of 100-150 V/ns transitions under active gate driving and in a layout optimised power circuit.

2.3.2. Automatic Profile Generation for Digital Methods

For digitally controlled active gate driving methods, where a processing system controls the gate drive profile in a closed-loop or iterative way, a method for generating the next profile to try is required. Previously cycle by cycle control with Si power devices has been possible due to the low switching frequencies and relatively slow device transitions.

However, using a digital approach with current technology introduces an inherent latency that forces a different approach to be taken. Online sequential optimisation to provide a pseudo-closed-loop active gate driving system has been shown to be effective in [62], [63]. Removing the constraint of sensing and responding cycle to cycle allows for greater analysis of the data for a single transition. An entire switching cycle can be captured and post-processed to calculate quantities such as switching loss and waveform spectral content which cannot be sensed directly.

Particle swarm optimisation has been shown to be an effective approach to online automatic profile generation [64].

Simulated annealing has also been shown to be effective with SiC MOSFETs and applied to a driver similar to the one used in this work but functioning at least an order of magnitude slower [65]. With a minimum time step of 40 ns and 63 levels of output drive capability a reduction in current overshoot of 25% and switching loss of 38% at turn-on was possible with a Si IGBT after manual tuning. The simulated annealing algorithm was then able to reduce this further by 26% and 18% respectively. This is promising as an online optimisation method as it does not rely on a family of possible solutions to be evaluated to move towards a new solution.

Applying these techniques to wide band gap circuits, GaN particularly, has been noted to be difficult because of the in-circuit sensing requirements [66].

2.3.3. Loss Management

In multi-phase or interleaved power converters it is common for some power devices to interact with the cooling system differently and thus be at different temperatures. The new device packages

associated with GaN HEMTs and the low thermal conductivity of GaN are prone to damage over time with repeated thermal cycling.

An active gate driving strategy which aimed to reduce converter efficiency at light load to stabilise power device temperature thermally at an elevated level proved effective in [67]. A three step gate driver with adjustable mid-level voltage and mid-level activation delay time was developed to dynamically control switching loss on a cycle by cycle basis. At low load levels in a scenario representative of a DC-DC converter it was possible to use the 2-step driver to increase control switch losses by 1.5-2x, maintain a raised case temperature, and reduce the degree of thermal cycling.

Similarly, active gate current control with GaN gate injection transistors has allowed for losses during switching, conduction and gate driver losses to be controlled individually. This allows for an extra degree of freedom when balancing losses, EMI and switching waveforms quality [68].

Management of the lossy reverse conduction mode of GaN HEMTs is another promising area in which active gate driving with a high effective bandwidth has helped. After fine tuning an active negative voltage clamp circuit, gate driver losses increase from 70 mW to 140 mW compared to conventional gate driving. However, the overall efficiency of the soft switching LLC converter it is implemented in was raised by 0.5% between 300 W and 700 W [69].

2.3.4. dv/dt and di/dt control

The direct control of dv/dt and di/dt during a transition within a power converter is key to controlling the EMI produced by and the switching losses of a converter. It is typically part of a strategy which may implement oscillation control or loss management, but they can be targeted separately.

The primary challenge with in-transition control of GaN is, as suggested in the measurement section of this literature review, the bandwidth of the signals that are required and furthermore the control loop delay. A gate driver with an integrated analogue dv/dt control loop has been reported to give < 200 ps response time to a connected, but not co-packaged, GaN HEMT [70]. Furthermore, the implementation separates out control of di/dt and dv/dt during a transition. A fixed gate resistor value regulates di/dt whilst the quoted fast control loop regulates dv/dt. This method was reported to drastically reduce EMI associated with fast GaN HEMT turn-on transitions.

dv/dt control of 600 V GaN HEMTs with a digital active gate driver allowed turn-on and turn-off voltage slew rates to be varied between 9 – 27 V/ns and 7.5 – 35 V/ns respectively in [61]. In this instance it is used to effectively control oscillations and electrical stresses at the gate connection of the power device caused by the power loop coupling into the gate loop during switching.

dv/dt and di/dt control has been used with SiC MOSFETs in a 200 V DC Link, 100 KHz switching frequency power converter [71]. The proposed non-integrated gate driver was able to reduce voltage and current overshoots by ~30% for turn-on and turn-off edges whilst also reducing switching losses by 57% compared to conventional gate driving. This is also reported to lead to an improvement in drain current waveform spectra at 5.7 MHz of ~10 dBµA.

The reported works highlight the benefit of slew rate control as a goal for active gate driving techniques. Control of power circuit waveform slew rates has been shown to be possible with GaN HEMTs at reduced switching speeds. The implementation of di/dt control is hampered by the difficulties associated with current sensing within an optimised GaN HEMT based power circuit.

Therefore, this thesis investigates the application of dv/dt and di/dt control to GaN HEMTs operating at high slew rates.

2.3.5. Oscillation control

Oscillation of parasitic circuit elements and feedback-based oscillation via power device parasitic capacitances are some of the main sources of EMI in a power converter. In extreme cases it can lead to premature aging of the power device through contact degradation, its mounting due dendrite growth between pads and damage due to internal stresses as GaN is a highly piezoelectric material. The process of accounting for the presence of the oscillations influences the degree to which components may be over specified for an application (e.g. 650 V power device for a 400 V DC link, 600 V rated capacitors for a 400 V DC link converter). Typically, component ratings will be over specified by 25-50%; active gate driving could allow this margin to be reduced by preventing resonant interactions between circuit parasitics. This could then lead to system level savings and boosted power density and therefore active gate driving has targeted these benefits.

The move to wide band gap power devices complicates the application because of the high control bandwidth required to influence them during short transitions without artificially slowing them down to make them controllable. The lack of drivers suitable for GaN HEMTs that have high enough effective bandwidth or fast enough output update rate has limited work in this area. A small number of drivers exist that operate approximately 10-20x slower than is required for GaN.

The resulting dearth of literature and desirability of the possible benefits of oscillation control with GaN HEMTs make it promising area of work to explore.

2.3.6. Device Current and Voltage sharing

Using series or parallel combinations of power devices is common for increasing the voltage or current handling capability where a single power device with sufficient ratings does not yet exist. With discrete or co-packaged devices in all semiconductor technologies, the faster the intended transition is, the more troublesome it becomes to ensure all devices switch at the same time. If, during a fast transition, current or voltage are not shared equally it can cause a single or multiple device to fail and cause a cascade failure of the remaining parallel or series devices.

Reported work has shown the ability to effectively parallel GaN HEMTs without the need for advanced gate driving techniques with both discrete and integrated power devices [72]–[77]. Careful characterisation and modelling of the parasitic circuit elements, particularly the inductance, in each parallel branch has been shown to be key [72], [74], [77]. In these cases it was possible to parallel 4 GaN HEMTs, one of which resulted in a 650 V 240 A rated bridge-leg that was successfully operated at 400 V and 240 A for double pulse tests [72]. Providing a close degree of impedance matching is maintained GaN HEMTs operate well in parallel as they have a positive resistance coefficient with temperature. If a single device conducts more current, it gets hotter and its R_{ds} rises which causes current to divert amongst other parallel devices [73]–[75].

References to series stacking of GaN HEMTs in the literature, in order to increase their combined voltage rating, is limited due to the highlighted challenges brought about by their fast switching action. A pair of two device series stacks with 650 V 60 A GaN HEMTs has been demonstrated with a “quasi-active” gate driver to simulate and implement a 330 V input bi-directional boost converter [78]. The “quasi-active” gate driver is a passive approach with auxiliary gate networks to provide separate turn-on and turn-off paths, static voltage balancing and the ability to adjust the dynamic voltage balancing during switching.

Previously IGBTs have been popular choices for combining in series and parallel for high-voltage applications high-power. With single devices capable of blocking > 3kV series stacks allow operation at MV and HV with a minimum number of individual devices in the stacks. Parallel combinations of single devices rated for >600 A allow for hundreds of kilowatts scale bridge-legs to be constructed with ease.

As with GaN HEMTs, transient voltage imbalance with IGBTs during switching transitions remains a problem even at reduced speed. Digital active gate driving methods have proven effective at minimising static and dynamic voltage sharing in series stacks of up to 3 devices at each switching position [79]–[82]. This has allowed for 4.5 kV rated IGBTs used in series pairs to form a single switch

to implement a 6.6 kV DC link voltage converter [80]. The detailed FPGA based non-integrated digital adaptive active gate driving strategy was able to improve static and dynamic voltage sharing delta between devices by 18% to below 2% after 10 switching transitions.

Similar active gate driving methods have been applied to parallel combinations of IGBTs with a view to improving the balance of static and dynamic current [82]–[86]. Constraining the reported work to digital adaptive gate controlled methods, it has been shown that 4 devices connected as 2 parallel pairs in series can operate effectively as part of an extensible combined voltage and current balancing scheme [82]. Transiently a single IGBT of the 4 supported almost the full 10 A load current during double pulse tests; the method detailed was able to reduce this with within 20 %, 1 A, under all conditions. The method presented was intended to be extensible up to combinations of 10 IGBTs to form a single voltage and current balanced switching module.

This shows active gate driving methods have been effective for parallel and series connection of IGBTs after path inductance has been controlled as is highlighted to be important for doing the same with GaN HEMTs. However, the increase in control bandwidth required to drive GaN HEMTs similarly is a barrier to investigating if there are further benefits beyond careful control of circuit parasitics.

2.4. Scope of this Thesis

The ability of the devices to be switched rapidly and reliably suggests that high bandwidth active gate driving of GaN is a promising area of work with several different benefits that could be pursued. The areas of electrical stress reduction and oscillation control, previously referred to in sections [2.3.1] and [2.3.5] respectively appear to be the most promising as they directly address problems with the wider adoption of GaN.

Oscillation control contributes to reducing EMI which cannot be otherwise controlled with current generation passive components due to high frequency effects or power circuit layout optimisation. Electrical stress reduction in addition to oscillation control could then contribute towards maximising GaN HEMT operational life in application.

One of the core benefits of using GaN HEMTs is their fast switching action and high maximum switching frequency, therefore work conducted should aim to maximise switching slew rates, targeting greater than 50 V/ns and attaining or surpassing 10 A/ns.

Literature has also shown the possible benefits and approaches to optimising or continuously adapting an active gate driving strategy to changing power converter operating conditions.

To conduct this work a suitable testbed and experimental apparatus are required that surpass the capabilities of those reported to at the time of writing. The core questions this thesis will be addressing are as follows:

- Is the switching transition of a current generation GaN on Si HEMT power device controllable via the gate?
- Can benefits, such power circuit oscillation reduction and electrical stress reduction be demonstrated with GaN HEMTs, without artificially slowing switching transitions?
- What are the limitations of any benefits which can be demonstrated?

3. Creating a Testbed for Sub-Nanosecond Shaping of Switching Transients

3.1. Acknowledgement and Attribution

Section 3.3, 3.5 and 3.6 enabled the work in the following publications where the author of this thesis is the first author:

- "Shaping switching waveforms in a 650 V GaN FET bridge-leg using 6.7 GHz active gate drivers" [87]
- "Stretching in Time of GaN Active Gate Driving Profiles to Adapt to Changing Load Current" [88]

Furthermore, it enabled the work in the following co-authored conference publications:

- "Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns" [89]
- "Crosstalk suppression in a 650-V GaN FET bridge-leg converter using 6.7-GHz active gate driver" [90]

Section 3.4 additionally enabled the co-authored paper "Multi-level active gate driver for SiC MOSFETs" [91] originally published at the 2017 IEEE Energy Conversion Congress and Exposition.

3.2. Aims

The goal of this work is to beneficially shape switching waveforms by sub-nanosecond manipulation of the GaN HEMT gate. To be able to do this, the development of experimental hardware and techniques capable of generating the high bandwidth gate signal and capturing the resultant high bandwidth waveforms is required. The developed testbed must function reliably in proximity to the EMI generated by slew rates in excess of 100 V/ns and 1 A/ns common in mains voltage wideband-gap bridge-legs.

To achieve this goal the following core questions in their respective sections will be addressed throughout this technical chapter:

- Is it possible to develop intuitive programming methods for complex active gate driving profiles?
- How do we create robust programming hardware for an existing active gate driver that can survive the high EMI environment of a wide band-gap power converter?

- How do we design a converter around an existing sub-nanosecond active gate driver and supporting microelectronics so that the high EMI from the GaN HEMT bridge-leg does not affect it? (i.e. It is self-immune)

3.3. The Sub-Nanosecond Gate Driver

3.3.1. Introduction

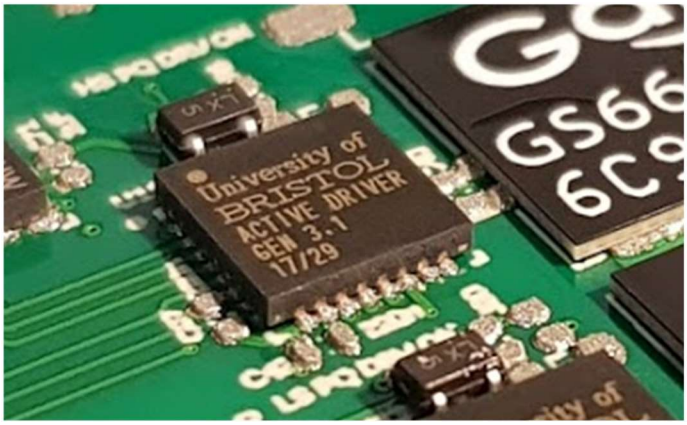

Figure 6 - A photo of the latest generation sub-ns gate driver prior to re-flow soldering.

Developed by previous work and made available to this work is a pre-existing active gate driver for GaN HEMTs. The driver has the output voltage range, 0-5 V, current drive capability, +/- 10 A and fine time resolution, 150-100 ps[2], required to test the hypothesis of this research. A full explanation of the driver, its design and capabilities can be found in [92]. For the purposes of this and subsequent chapters the salient features of the internal architecture will be discussed and a brief introduction to the driver given.

3.3.2. Operational Description

With the drivers used throughout this work the desired gate driver parameters, such as clock frequency, and resistance profile must be determined and programmed off-line. Once programmed the driver operates without intervention until changes to its configuration are desired whereby switching must cease to ensure a safe state while programming occurs[3].

The playback of the resistance sequence stored by the gate driver is triggered by the arrival and sampling of a rising or falling edge at the gate signal input pin. Separate sequences are stored for the

[2] This work spans the first three generations of the active gate driver. Generations one and two have 150 ps time resolution. Improvements to the internal design of the driver allowed for 100 ps in the most recent generation used in this work.
[3] This is subject to change but valid within the scope of this work.

pull-up and pull-down transitions and comprise the desired output resistances, polarities and timing information.

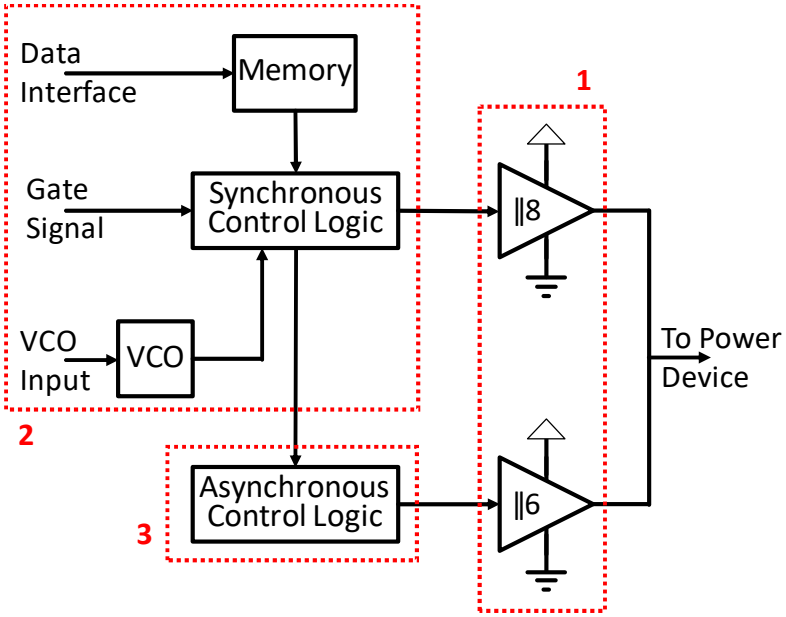

Figure 7 - Internal structure diagram of the prototype gate driver.

Internally the gate driver consists of 3 main sub-systems:

1. A two-part output stage comprising a 'main' driver that is synchronous to the internal clock and an asynchronous 'fine' driver triggered by the stack of each internal clock period. The 'main' driver has 2^8 resistance levels offering an output range between 0.14 Ω and 36 Ω. The time resolution of the 'main' driver is 1.6 – 2.4 ns in accordance with the operating range of the driver's internal clock. The 'fine' driver has 2^6 discrete output resistances between 1 Ω and 64 Ω with a duration and triggering delay time resolution of 100 ps. All parts of both drivers can be placed in a high impedance state during a transition if so desired. The 'main' driver can only pull in the same direction as the edge that caused sequence playback to occur (i.e. pull-up on an incoming rising edge and pull-down for an incoming falling edge). Conversely, each 'fine' driver can pull-up or pull-down on both edges on a clock period by clock period basis.
2. A synchronous memory and control logic block that runs at the same speed as the main system clock. It controls sequence playback and is triggered by the incoming gate signal. The programming of the memory is performed by an external system.
3. An asynchronous control block that is responsible for using the data loaded from memory by the synchronous part to generate the required sub-ns signals for the 'fine' driver.

The pull-up, PMOS, and pull-down, NMOS, networks in the main and fine drivers are only capable of supporting 5 V across themselves. Each individual driver in each half is constructed from a 2.7 V rated transistor, sized to give the desired nominal impedance, and a 1.8 V transistor sized to give the update speed required. For the GaN HEMTs used in this work, where the threshold voltage is approximately 2 V, this means the sub-nanosecond gate driver is broadly capable of fully enhancing the devices at turn-on. GaN Systems recommends the use of 6 V for their 650 V rated power devices but datasheets for the parts used suggest the difference to be measurable but small [10]. The use of +5 V allows greater head room for gate voltage overshoot before encountering the +7 V upper limit (+10 V transiently for <1 μs).

3.3.3. Sub-Nanosecond Resistance Sequences

To understand both the capability and limitations of the resistance sequences further, their structure will be discussed in more depth. The methods developed for graphically defining and representing them will also be introduced due to their importance to this work.

Each gate driver stores two resistance sequences; one for a turn-on transition of the connected device and one for a turn-off transition. A single resistance sequence defines the behaviour of the active gate drive for eight clock cycles after a transition has been sampled at the gate signal input. Eight clock cycles is chosen as a function of a number of manufacturing process limitations, such as maximum supported clock frequency, and a binary coded decimal power of 2 that doesn't result in a large silicon area after layout. A large layout would make meeting timing constraints within the control logic and memory challenging.

The internal voltage-controlled oscillator (VCO) that drives the memory, control logic and synchronous 'main' driver has a usable frequency range of between 400 MHz and 625 MHz. 400 MHz is the lower limit of what the VCO can produce and above 625 MHz the synchronous control logic behaves unpredictably before failing to function entirely until the VCO is slowed again.

This means that the span of time covered by eight times the chosen VCO clock period is important as it is the maximum span of time over which control with the 'main' drivers can be exerted upon the connected power device.

Additionally, the asynchronous 'fine' drivers have a limited number of group triggering delay elements and individual triggering delay elements for positioning them. If a long clock period is chosen, then it is not possible to activate the 'fine' drivers towards the end of each period.

Table 3 - All the settings available during a single clock period for turn-on and turn-off transitions of the sub-nanosecond gate driver.

	Main Driver	**32 Ω Fine Driver**	**16 Ω Fine Driver**	**8 Ω Fine Driver**	**4 Ω Fine Driver**	**2 Ω Fine Driver**
Polarity	Determined by trigger edge direction	Pull-Up or Pull-Down	Pull-Up or Pull-Down	Pull-Up or Pull-Down	Pull-Up or Pull-Down	Pull-Up or Pull-Down
Strength	High-Z or 0.14 Ω - 36 Ω	High-Z or 32 Ω	High-Z or 16 Ω	High-Z or 8 Ω	High-Z or 4 Ω	High-Z or 2 Ω
Duration	Internal clock period	1, 2, 4, 6 x 100 ps	1, 2, 4, 6 x 100 ps	1, 2, 4, 6 x 100 ps	1, 2, 4, 6 x 100 ps	1, 2, 4, 6 x 100 ps
Individual Triggering Delay	None	0 – 6 x 100 ps	0 – 6 x 100 ps	0 – 6 x 100 ps	0 – 6 x 100 ps	0 – 6 x 100 ps
Group Triggering Delay	None	0 – 6 x 100 ps				

Table 3 above indicates all the settings available to the user within one clock cycle on one of the two resistance sequences a gate driver can store. Each low-to-high and high-to-low transition then comprises 8 instances of Table 3. At the start of each of the eight internal clock cycles following a PWM edge the main driver is set to the desired resistance for the duration of the clock cycle. In parallel, the fine drivers are configured, and a triggering pulse sent to the sub-nanosecond timing system. Each fine driver can, once per clock cycle, be delayed from triggering up to 600 ps in 100 ps increments and as a group all the fine drivers can be delayed up to another 600 ps in 100 ps increments. Once triggered the fine driver pulse duration can be selected to last 1, 2, 4 or 6 x 100ps.

3.3.3.1. The Effect of Clock Period Variation on the Asynchronous Drivers

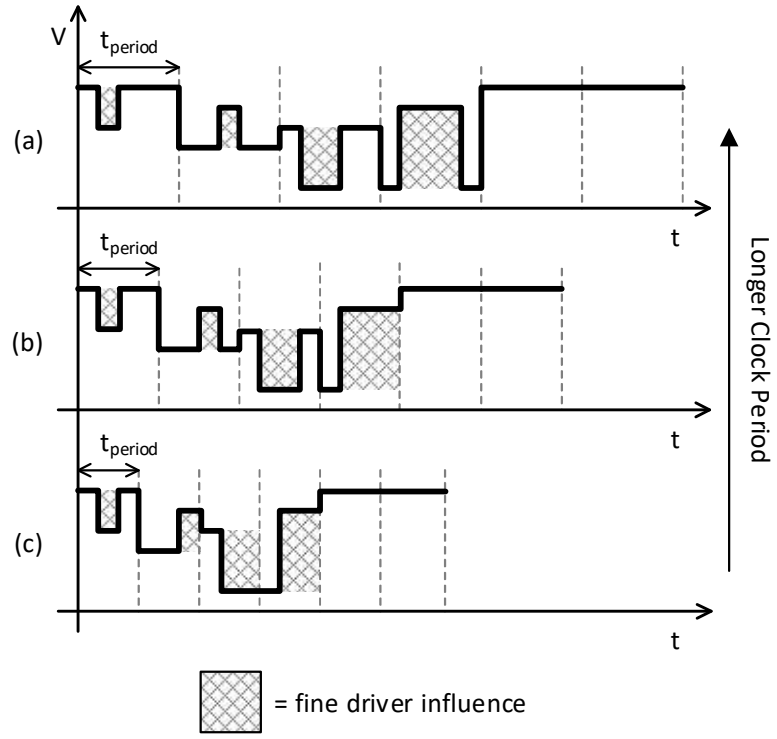

Figure 8 - The impact of gate driver clock frequency on a fixed resistance sequence utilising the fine drivers. The action of the fine drivers in is indicated by the shaded areas.

Figure 8 demonstrates an important but non-obvious implication of the combined synchronous and asynchronous architecture of the gate driver. The sub-nanosecond control system that co-ordinates the fine drivers is triggered by a pulse generated at the start of each clock cycle. After this pulse a pre-configured system of analogue elements, which govern triggering delays and durations, runs to completion or until the clock period ends. This is seen in Figure 8(c) where the final fine driver pulse has been shortened by the clock period ending before it's configured duration has elapsed.

Therefore, if the clock period changes, the fine driver delays and durations are still relative to the start of a clock period and are not scaled to maintain relative position and size. This makes the speed of the VCO as critical to the behaviour of the driver as the sequences themselves.

3.3.3.2. Output Resistance Dependence on Output Voltage

The next most important aspect of the operation of the driver to be considered when designing and reviewing resistance sequences is the variation in output resistance in relation to output voltage.

The active gate driver does not use parallel combinations of discrete resistances to provide the output resistance ranges stated in Table 3. Instead, the FETs in the parallel output stages of both the 'main' and 'fine' drivers are sized to give an on-state resistance of a specific value. This approach means that

this nominal design value is only valid for when there is 5 V, the maximum output voltage, across an NMOS or PMOS branch of a main or fine driver.

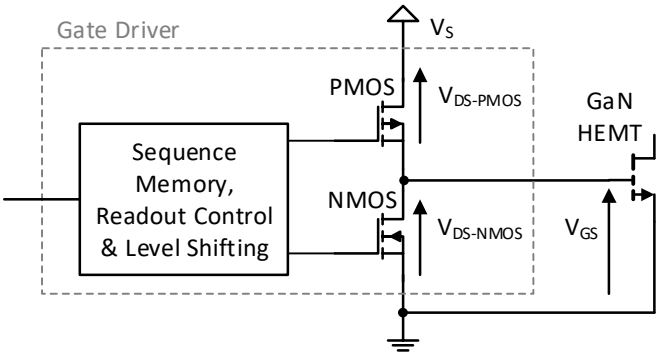

Figure 9 - An example output driver indicating the relationship between drain-source voltages in the output driver and the gate-source voltage of the connected power device.

Figure 9 shows how the voltage across the PMOS and NMOS branches of the output drivers relate to the supply voltage, V_S , and the connected power device gate voltage, V_{GS}. Therefore, the voltages across branches of the output drivers, $V_{DS-NMOS}$ and $V_{DS-PMOS}$, can be defined as the following:

$$V_{DS-PM} = V_S - V_{GS}$$

$$V_{DS-NMOS} = V_{GS}$$

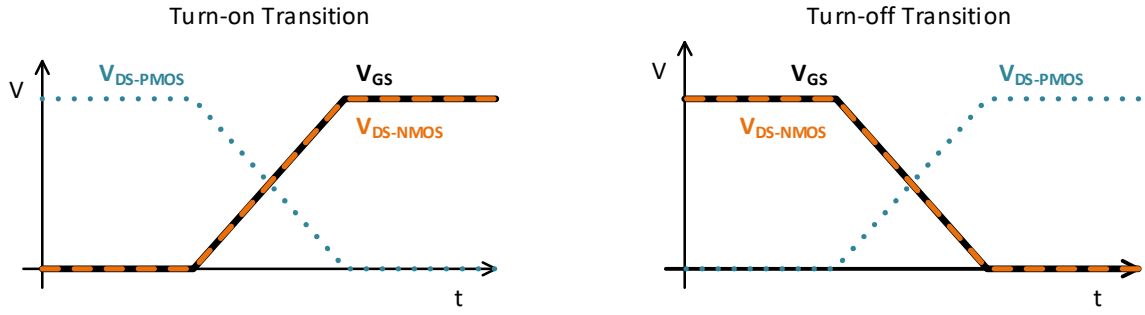

Figure 10 - Representative turn-on and turn-off transition waveforms indicating the change in voltage across the output driver branches.

FET type devices such as the ones in the output drivers have two distinct operating regions which they move between as the voltage across them changes. Figure 10 illustrates how the voltage across the output driver branches changes in relation to each other during turn-on and turn-off transitions of the connected power device.

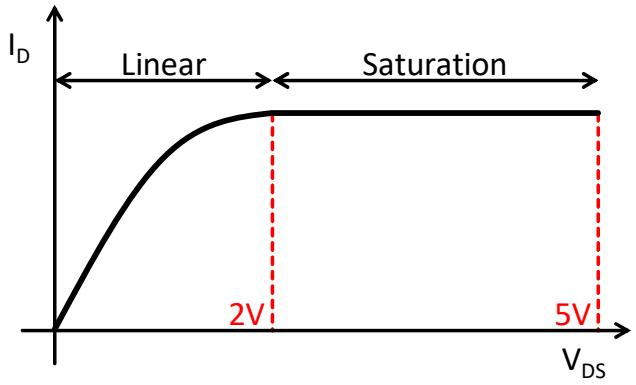

Figure 11 – Representative I-V curve for the output drivers in both PMOS and NMOS networks of the AGD output stage. A single curve is shown as the output drivers are only ever driven at their maximum gate voltage.

In the case of the gate driver used for this work, shown in Figure 11, when V_{ds} is between 5 V and 2 V the output branches are in saturation and behave like current sources. Below this, between 2 V and 0 V, they enter the linear region where they behave more like a voltage source with series resistance.

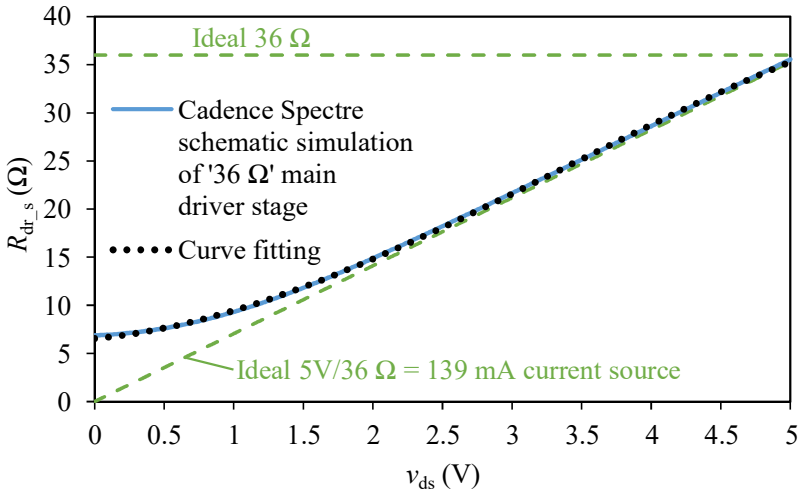

Figure 12 - Simulated output characteristics of a single pull-down NMOS transistor in the main driver showing how it's effective output resistance varies over a transition compared to a fixed 36 Ω resistor and the effective output resistance of a comparable 139 mA current source. Copied from Figure 4 originally published in [92].

Figure 12 shows how the simulated on-state resistance of an individual NMOS, pull-down, main driver varies over the course of a transition. During a transition the voltage across these branches will vary due to the charging or discharging of the connected power devices gate capacitance. This means, for a turn-off transition, the effective output resistance of the active NMOS drivers falls causing the pull-down strength and voltage fall rate to increase as the transition progresses.

The output drivers will be susceptible to changes in temperature that effect their nominal output resistance whether they come from the environment, near-by components or from internal losses. For the purposes of this work the period over which a transition occurs, < 25 ns, is considered short

enough for internal losses to not cause a significant rise in temperature. Whilst the peak current capability of the driver is ±10 A this is rarely used in practice when driving a single GaN HEMT.

3.3.3.3. *Voltage Sources and Current Source in High Speed Active Gate Driving*

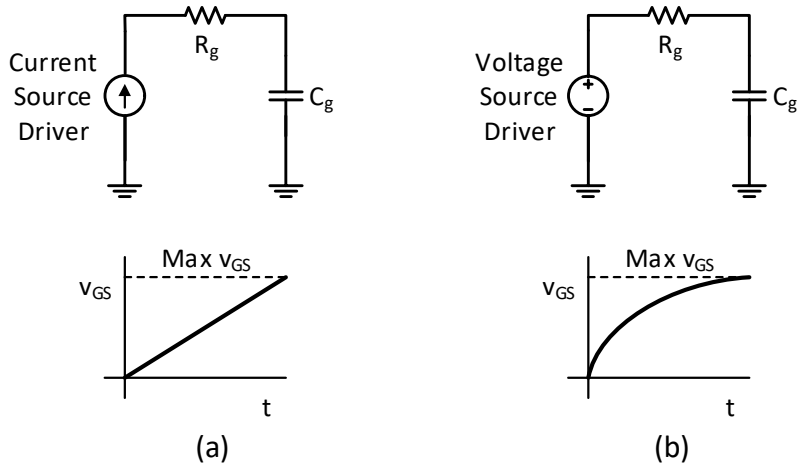

Figure 13 - Illustrative waveforms of charging an R-C load representative of a power device gate from a current source(a) and a voltage source(b).

Conventional gate drivers behave as voltage sources applying a voltage step function to the gate of a power device via a fixed resistance. In Figure 13.b this situation is shown and accordingly gives an exponential rise in V_{GS} towards the amplitude of the step function applied across the R-C load the device gate forms. If the duration of the rise is too long, then a larger voltage step function must be applied which risks damage to power device gate; particularly in the case of GaN HEMTs which do not have explicitly isolated gate structures.

If a current source is used instead, Figure 13.a, then the duration of the rise can be controlled more easily to give a linear rise. However, inductance in the gate loop makes this arrangement susceptible to over voltage caused by di/dt.

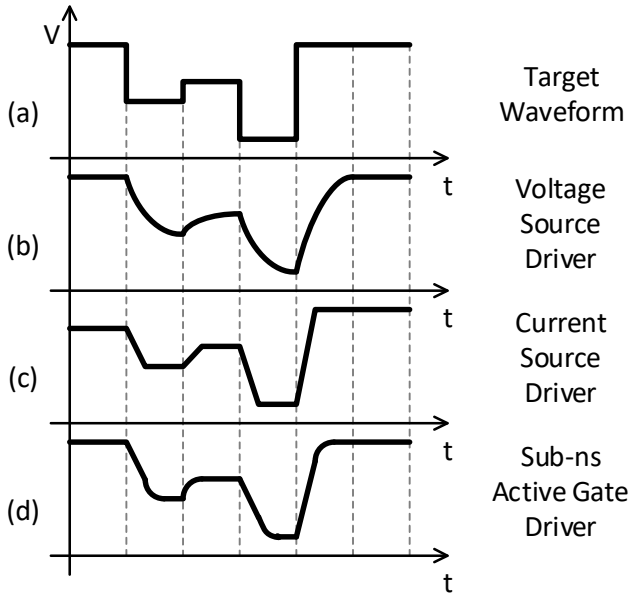

Figure 14 - Comparison of different gate driver sources to the tracking of a defined, fast target waveform comparable to that used in sub-nanosecond active gate driving.

Taking into account Figure 12 and Figure 13; Figure 14 illustrates the practical impact of the different kind of sources that could be used to control a power device in a high bandwidth active gate driver. Due to the exponential nature of the rise the voltage source driver, shown in Figure 14.b, is not able to accurately replicate the target waveform in Figure 14.a.

The current source driver, Figure 14.c, can better replicate the target waveform but due to the sharp changes in di/dt at the end of a change in target waveform overshoots are likely. Figure 14.d represents both a representative response of the sub-nanosecond gate driver used in this work and also a middle ground between Figure 14.b and Figure 14.c. The portion where it behaves as a current source allows it to better track the target waveform while the voltage source action provides a smooth di/dt ramp.

3.3.4. Representing Resistance Sequences

To simplify the construction and comparison of sub-nanosecond resistance sequences a clear method of representing them is needed. Its main purpose is to show relative changes in driving strength and their timing versus the impact they have on the various important power device waveforms.

For a single driver there are two edges for which profiles may need to be represented; each of these edges can then be broken down into a pull-up and pull-down profile over time. Even when using nominal values displaying the settings during each clock period a diagram that states this would be too complex to be useful for intended purposes. This indicates one of three methods as most suitable for displaying the result of these settings for each turn-on or turn-off transition:

1) Two separate diagrams are used for each resistance sequence. One axis represents the pull-up settings and another the pull-down settings over time on a 0 Ω to High-Z (driver inactive) axis. An example is shown in Figure 15. This is good for simple sequences where the pull-up or pull-down network alone is used but consumes a large amount of space for the information it communicates.

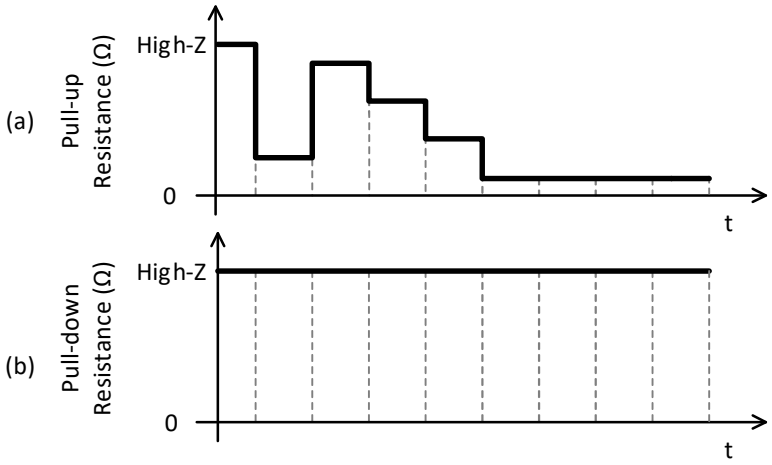

Figure 15 - An example turn-on resistance sequence shown using two separate diagrams.

2) A combined diagram for each resistance sequence showing the nominal output resistance from both the pull-up and pull-down networks from 0 Ω to High-Z (inactive) [87], [89]–[92]. This method will be used in places throughout this work as it is compact and fits in well with stacked arrangements of important circuit operating waveforms. An example is shown in Figure 16.

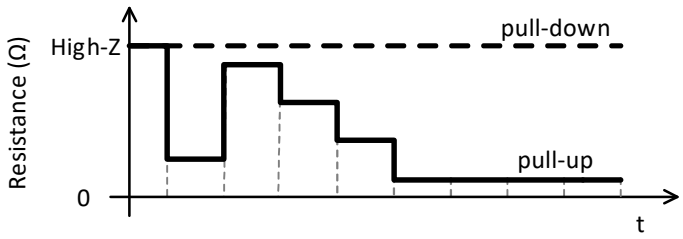

Figure 16 - Combined diagram form used in software and space at a premium situation. This gets cluttered when complex patterns are employed however.

3) A hybrid of approach 1 and 2 which can be seen in Figure 17 below. Two separate diagrams sharing a common horizontal axis and origin value. In this case High-Z (driver inactive) would mark the centre of the combined diagram [88]. The pull-up output resistance extends upward towards 0 Ω such that the further up in this half of the diagram the 'stronger' the pull-up network. Similarly, the pull-down resistance extends downward toward 0 Ω and the further

down in the lower half of the diagram the ‘stronger’ the pull-down network is set. Though space consuming, it is good for complex resistance sequences where both pull-up and pull-down drivers are active on a single transition. Another benefit is that ‘at a glance’ the trend of a sequence can be determined more easily that the combined diagram in Figure 16.

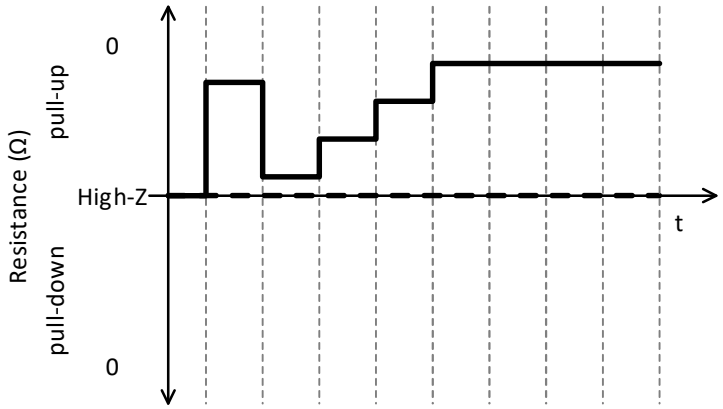

Figure 17 - Hybrid diagram form used in presentations.

All three diagrams are intended to be displayed alongside voltage and current waveforms, ideally stacked so that the time axis is easily correlated. Approach 3 is the preferred method although approach 2 will also be used in places as previous work that is drawn upon has used this approach, it is the most compact and it may not always be possible to update to the newer style.

3.4. A UI for Designing Sub-Nanosecond Impedance Profiles

3.4.1. Introduction

The capabilities of the driver in use for this work and the structure of the sequences it gets programmed with has been discussed. Table 3 shows all the settings in a single, of eight, clock cycles for one, of two, transitions. This work concentrates on a bridge-leg or half-bridge power circuit comprising two power devices and two sub-nanosecond gate drivers.

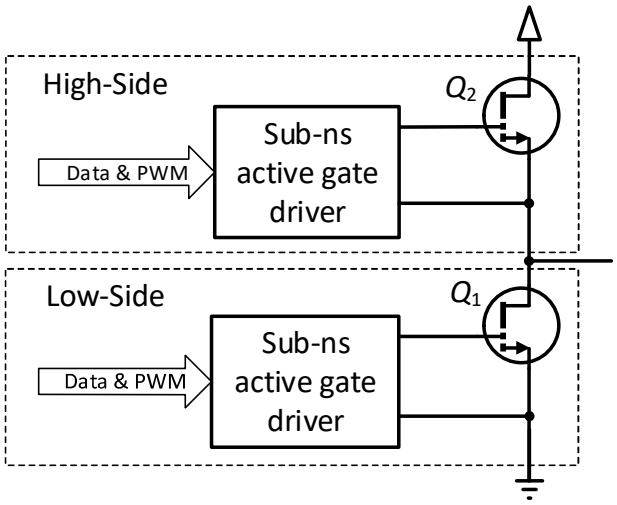

Figure 18 - Diagram of a GaN HEMT bridge leg with two active gate drivers. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

A single complete resistance sequence is one quarter of the data required to fully configure the gate drivers in a bridge leg. Therefore, an intuitive user interface for designing and testing the resistance sequences that allows rapid perturb-and-observe testing cycles is required. The specification for such a user interface in this case was as follows:

- Give a representation of the resistance sequence as designed considering the programmed clock speed
- Provide methods for saving and restoring resistance sequences
- Present at least all settings for a single active gate driver in a single clock period at once
- Provide a means for configuring test equipment other than the active gate drivers if desired
- Provides a means for recording all important data automatically

The structure of the test bed hardware, where a host PC co-ordinates test equipment and communicates with the Xilinx Zynq SoC which programs the gate drivers, gives two options for the resistance sequence creation interface; a text-based user interface or a graphical one.

3.4.2. Text-based vs Graphical

Early versions of the sub-nanosecond gate driver were programmed with a text-based user interface and showed that simple resistance sequences could take a substantial quantity of experimental cycles to optimise. This process of optimising gate resistance sequences can be split into two distinct time periods within an experimental cycle each with their own typical durations:

1) The time taken for a set of waveforms to be inspected and new sequences designed. This is mostly determined by the design of the user interface and can take up to a minute.

2) The time taken to update settings on the test bed equipment and perform a double pulse test. This process typically takes 3 seconds and varies by hundreds of milliseconds.

Table 4 - Comparison of user interface paradigms for creating resistance sequences.

Feature	Text Based Interface	Graphical Interface
Design Time	Low ✓	High
Prototyping Time	Low ✓	High
Feature Addition Complexity	Low ✓	High
Speed of Use	Low	Very High ✓
Ease of Navigation	Low	Very High ✓
Resources	Low ✓	High
Remote Operation Complexity	Low ✓	High
Ease of Multitasking	Low	High ✓
Strain After Long Term Use	High	Low ✓

Table 4 suggests that a text-based interface is the correct choice for this task due to its short development time requirement, high extendibility and low host system resource consumption.

However, the time spent interacting with the user interface is the biggest single contributor to the experimental cycle duration. If the number of cycles required to optimise a resistance sequence cannot be controlled, then the speed of a single cycle must be prioritised.

```
-> PQ Live Pattern Editing Program
|-> PWM Mode
(q)uit or (return) to continue.

Edit pattern options:
        Print current main drivers pattern by entering 'p'
        Print full patterns by entering 'pf'
        Select next menu level by pressing return without entering any text
        Change VCO level by entering 'vnnn' where nnn is desired level in hex (min=0x0, max=0x2AA, current=0x2AA)
        Exit menu by entering 'e'
        Quit test by entering 'q'
Select slot to edit by entering number 0 to 7 followed by 'h' or 'l' for high side or low side (e.g. '5h').
        Currently selected slot is: low side slot 0
To change the main driver strength for all slots, type 'a<side><pull direction><strength>' where:
                                <side> is 'h', 'l', or 'b' for high side, low side, or both
                                <pull direction> is 'u', 'd', or 'b' for pull up, pull down, or both
                                <strength> is driver strength in hex, entered as two digits (no leading 0x required)
```

Figure 19 - The top of three levels in the text-based user interface for resistance sequence development during a continuous switching experiment. This is written in C, running on a single ARM core of the Zynq 7000 FPGA and presented over USB serial port.

Figure 19 shows a small part of the multi-tiered text-based user interface. Large amounts of text make it slow to read and the combinations of characters needed to form a command cause mistakes to be common. This leads to additional time correcting mistakes and spotting mis-configuration which further slow the sequence development and optimisation process.

Visualising the current resistance sequences and determining the next change to make to it is difficult with the text-based interface. To visualise a resistance sequence, it must be exported to MATLAB where a pre-existing script constructs a graphical representation of it.

Therefore, despite the suggestion of Table 4, this makes a graphical user interface a more suitable choice for the problem of designing resistance sequences. Interacting with a graphical user interface is faster, more intuitive and can show the current resistance sequence in a clear way as adjustments are made.

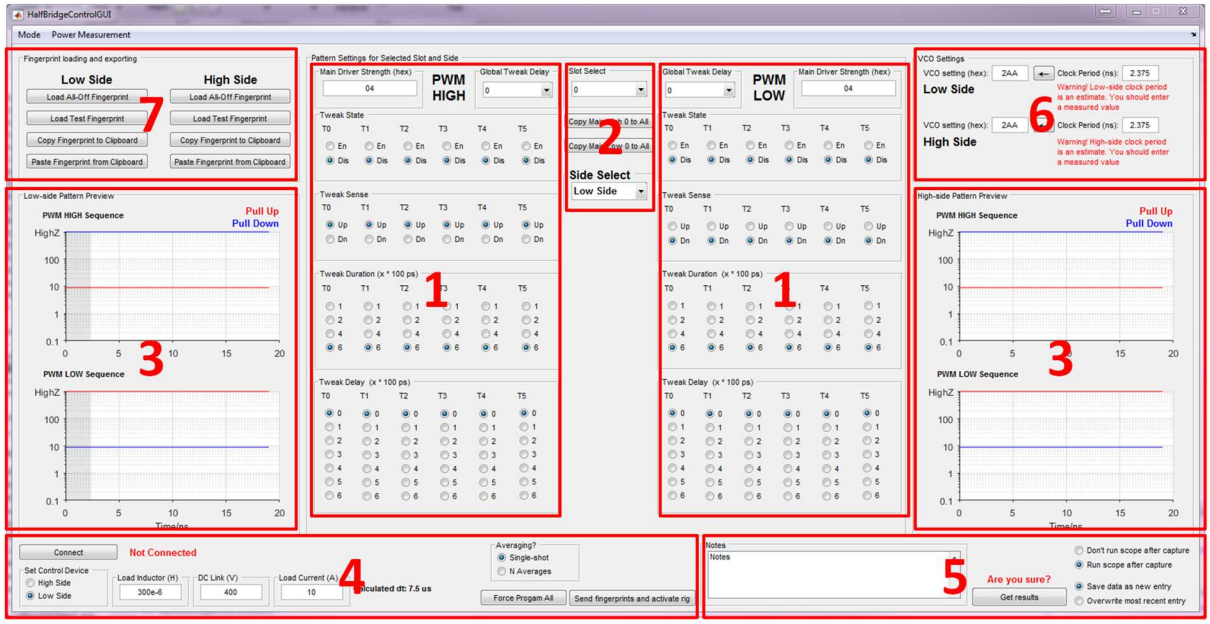

Figure 20 - The graphical user interface developed in MATLAB for use with the C software running on the Zynq 7000 FPGA and testbed hardware to replace the text-based user interface in Figure 19.

Figure 20 shows the developed graphical user interface. The interface is split into seven main sections which can be broken down in the following way:

1) The full main and fine driver settings for the currently selected clock period and gate driver.

2) The gate driver and clock period selection controls.

3) The sequence preview windows

4) The double pulse test configuration and triggering controls

5) The result and notes capture controls

6) Sub-nanosecond gate driver clock frequency controls

7) Quick sequence loading and saving controls

The aim of the interface is to make developing a resistance sequence for a single transition as fast as possible. Experience with the text-based interface suggested that co-development of resistance sequences for multiple edges was unnecessary due to the complexity of developing a single sequence and instrumentation limitations. Because of this the selection controls in Figure 20.2 allow the user the select an individual clock period within one of two gate drivers. This is then highlighted by the grey shaded area of the resistance sequence previews in Figure 20.3. Once a driver and clock period has been selected, the full settings for both turn-on and turn-off transitions can then be manipulated in Figure 20.1 with the sequence previews being updated in real-time. Figure 20.6 allows the clock frequency of both the gate drivers to be adjusted. It is set in terms of the value programmed into the SPI digital-to-analogue converter (DAC) so the resulting frequency must be measured, the clock period computed manually and entered back into this area. This then adjusts the time axis of the sequence preview figures for the effected driver to suit the new clock period.

Once a resistance sequence is ready to be tested Figure 20.4 allows the important parameters of the double pulse test to be configured and a test sequence triggered. This updates the support equipment for the test bed and programmes the gate drivers in a safe way before triggering the function generator.

The controls within Figure 20.5 allows for the results, current configuration and environmental parameters to be captured automatically into a cell array within MATLAB.

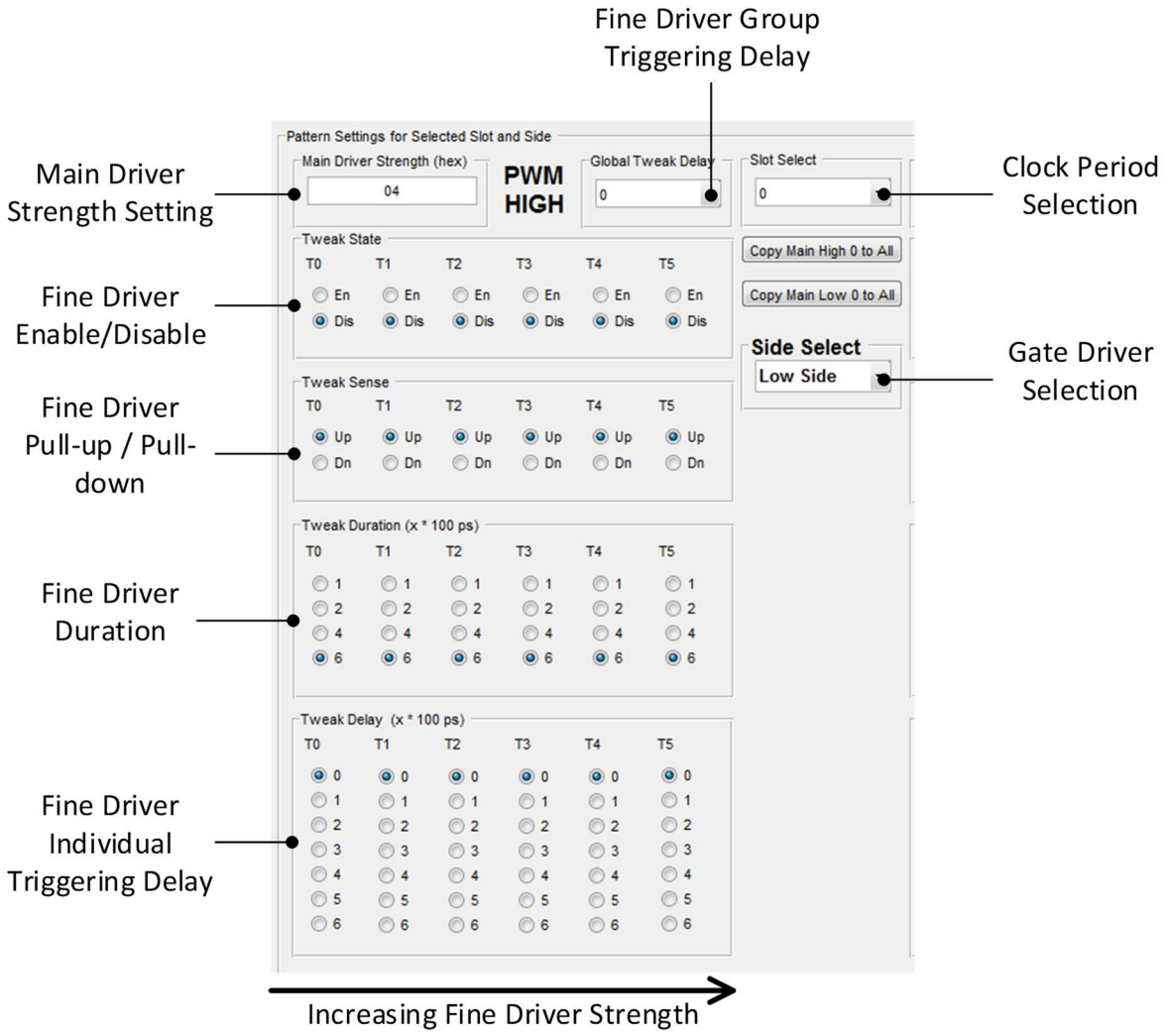

Figure 21 - All of the available controls for a single clock period in one transition.

Figure 21 highlights the controls required for developing a resistance sequence for a single transition, in this case the low-to-high turn-on transition. Despite appearing complex, it lays out the esoteric settings, detailed in Table 3, available within a single clock cycle without the need for sub-menus. This is desirable as they would obscure subtle information which can be gleaned by scanning over the array of radio buttons. The user can easily see the relative difference in settings between fine drivers and the degree of adjustability remaining in a driver such as for the individual triggering delay. This makes it easier to determine if the desired adjustment can be made in the current clock period or if a different one is needed.

3.5. Low Voltage Signalling in a High Slew Rate Environment

3.5.1. Introduction

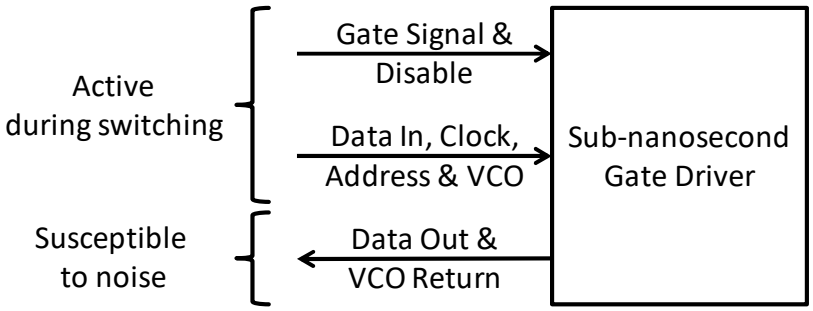

Figure 22 - Illustration of the sub-nanosecond gate driver control and programming interface.

Figure 22 illustrates the main features of the sub-nanosecond gate driver's electrical interface to the programming and support hardware. The inputs and outputs are always active and susceptible to spurious transitions causing unwanted behaviour of the driver. For example, a spurious transition on the data clock input during switching will cause the data in on-board memory to become invalid and the output behaviour unpredictable until re-programmed. The return signals will not be utilised during switching but need to be prevented from carrying switching noise into other parts of the test bed.

Therefore, for the sub-nanosecond gate driver to be useful the support and programming hardware needs to:

1) Control the driver by transferring gate and output disable signals reliably to the driver whilst switching is occurring. As in Figure 22 the low-voltage logic interface to the drivers is always active which makes it susceptible to cross-talk and EMI cause by power device switching. The low 1.8 V logic level means that relatively small disturbances are required for a false reading from any given input pin.

2) Program the driver by transferring the desired sub-nanosecond resistance sequences from the user interface to the gate drivers. This will only occur when there is no switching activity due to each driver only storing a single resistance sequence for each transition, but the DC link may still be energised.

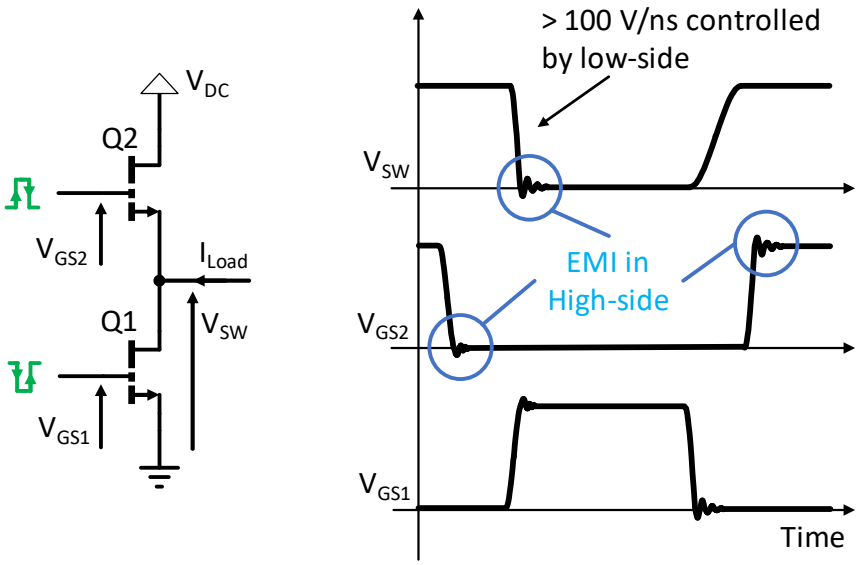

Figure 23 - A bridge leg showing the important reference potentials.

Figure 23 shows a bridge leg layout and indicates the changes in potential throughout a switching cycle. The high-side power device, Q2, and associated drive circuitry must float as they are referenced to the switch node waveform V_{SW}. This means they must change potential at slew rates at up to 100 V/ns and withstand significant EMI. This EMI will primarily come from oscillations in the power stage but also from the output of the gate driver too. The wide resistance range and sub-nanosecond drive capability allow for significant high frequency content generation at the gate drive output.

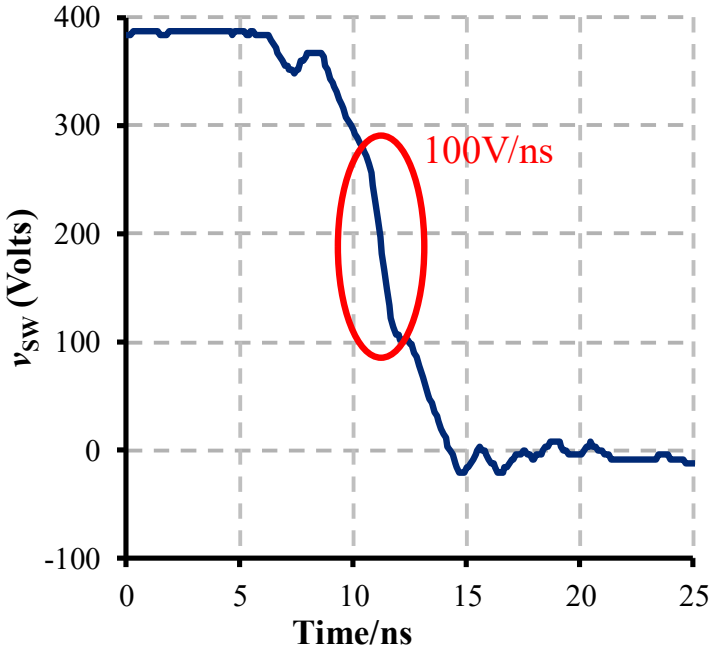

Figure 24 - Experimental data captured at the switch node of the bridge leg showing a slew rate of 100 V/ns.

Figure 24 shows experimental waveforms and highlights the extreme slew rates a GaN HEMT bridge leg can produce. From knowledge of the slew rates and changes in reference potentials within the bridge-leg throughout a switching cycle the requirements for the gate driver support and programming hardware can be determined. They must have the following:

1) High immunity to radiated EMI. GaN HEMT based bridge legs can oscillate at frequencies in the order of hundreds of megahertz [88] due to the small value of parasitic circuit elements present. Therefore, short PCB traces and small copper areas, such as those present in a high-performance PCB design, can effectively couple and radiate in EMI.

2) High common mode transient immunity (CMTI). This is the ability for the hardware to resist the ground reference for parts of it slewing between different potentials at high rates and frequencies. This is comprised of several main factors, the capacitance across the isolation boundary, the capacitance of the isolated region to earth and the inherent CMTI of any components used due to their internal structure.

This means that these two requirements depend upon the components selected and the design of the PCB they reside upon. This will be discussed separately in the following parts of this section.

3.5.2. Test-bed Programming Hardware Structure

The previous section highlighted that the support hardware must fulfil two main purposes; to program the provided gate driver and to control it reliably. Figure 22 gave an overview of the gate drivers electrical interface; it requires three separate power supplies, one analogue signal and numerous digital signals. In addition to the number of elements in the electrical interface is that the analogue and digital signals have a limited acceptable voltage range, 0-1.8 V and 1.8 V TTL logic respectively. This makes them susceptible to noise or false high and low conditions caused by EMI and cross-talk between nearby signals.

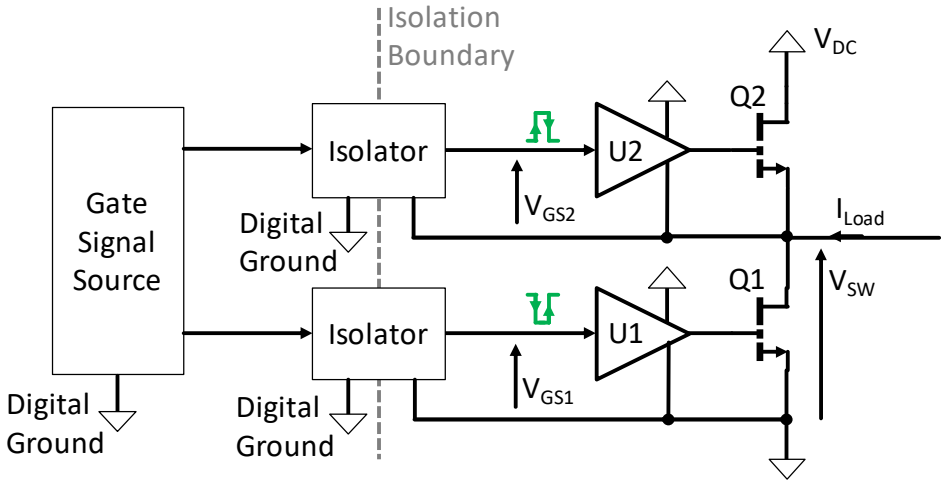

Figure 25 - Introduction of isolators in high and low side for required isolation and signal path matching.

The need for the high-side to float and withstand the EMI and high slew rates of the bridge-leg has been discussed. A digital signal, which allows the ground on one side of its isolation boundary to differ from the ground on the other isolator must be introduced. An isolator is also introduced in the low side as the propagation delay of the isolators is long and can be a significant portion of any desired dead-time. The additional isolator also further isolates the programming and support hardware from EMI generated by the bridge-leg being coupled into signals and power rails.

To assist in interfacing with the sub-nanosecond gate driver a Digilent ZedBoard, housing a Xilinx Zync 7000 Series SoC (System-on-Chip) was chosen. The Zync 7000 part in use provides 2 ARM CPU cores and Xilinx Spartan 6 class FPGA fabric. Only one of the ARM CPUs is used in this implementation to communicate with a host computer to provide a user interface and program the sub-nanosecond gate drivers. The FPGA fabric is used to implement peripherals that aid testing and programming of the drivers. One such peripheral allows the software running on the ARM CPU to intercept the gate signal connections to the drivers. This kind of interlock functionality is particularly useful when programming a new resistance sequence, a condition in which accidental triggering of a driver would have unpredictable results.

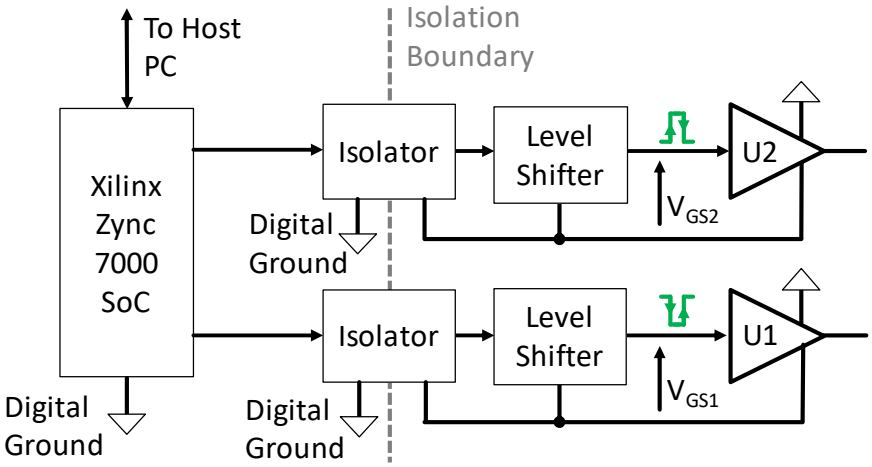

Figure 26 - A simplified view of the test bed hardware considering the requirements and constraints so far.

Figure 26 gives a simplified view of the resulting test bed structure once the desired capabilities and hardware specifications are considered. Level Shifters have been introduced so that the logic levels used by the signals to the gate drivers can be kept high right up to last point. This helps with immunity to switching noise and radiated EMI as only the last part of the signal path is particularly susceptible to false transitions being registered.

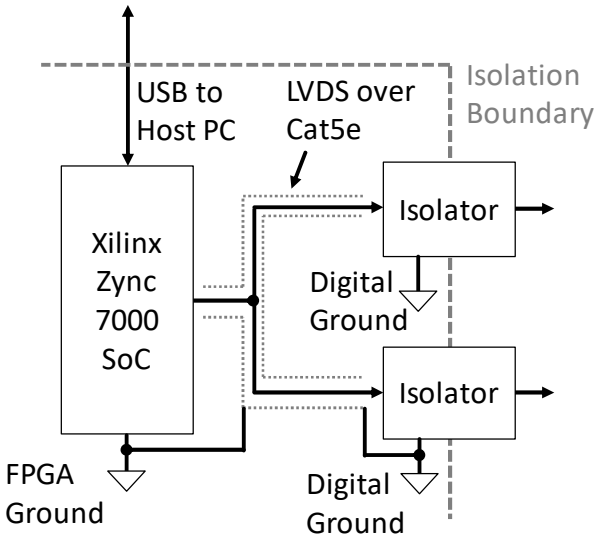

Figure 27 - An illustration of the changes made to accommodate long distance transmission of LVDS signals from the FPGA.

The final part of the test bed hardware structure allows the FPGA to be placed a distance away from the power stage; the main source of EMI. This is required because the development board that hosts the SoC is not designed with resistance to high EMI in mind. The development board also has indicator LEDs, buttons and switches which are used for user interaction prior to and during run-time.

To facilitate moving the FPGA to a safe distance for the user to interact with it the Low Voltage Differential Signalling (LVDS) transceivers built into its I/O blocks are used. All programming and control signals are routed via these and over Cat5e shielded twisted pair cable to a complimentary set of LVDS transceivers on the test bed. This allows up to 10m between the testbed and FPGA in accordance with the recommended maximum distance over Cat5 cable from the DS90LV032A datasheet.

Alongside the other additions to the final hardware structure shown in Figure 27 is another isolation boundary. A USB isolator is positioned close to the host PC on each of the two connections from the Zync 7000 SoC. This helps prevent conducted or radiated EMI causing erroneous disconnection events from the host PC and loss of control of the test bed.

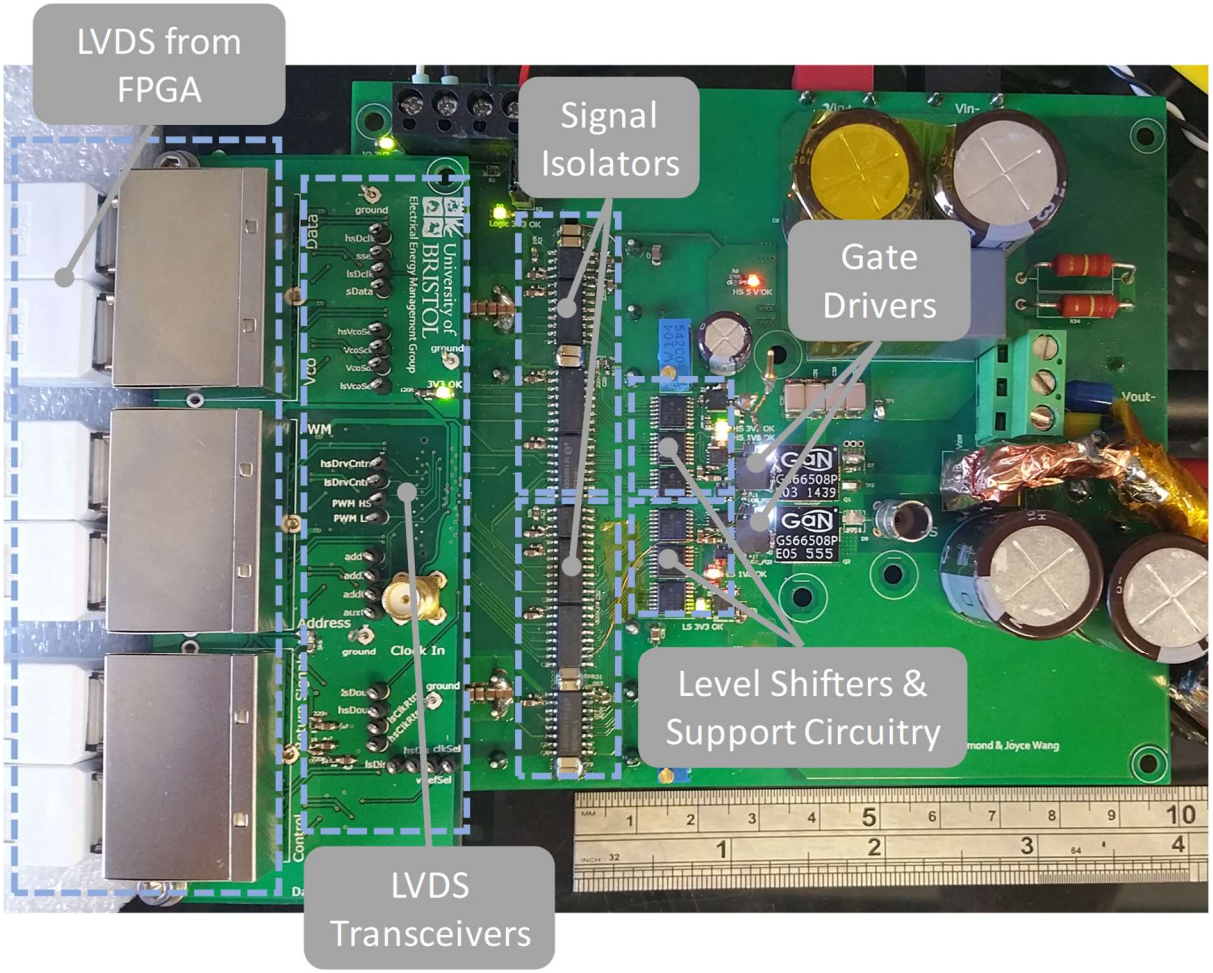

Figure 28 - Annotated picture of a power board highlighting areas important to the gate driver support hardware with a ruler provided for scale.

Figure 28 shows the implementation of the hardware structure discussed. Not shown are the Isolated DC-DC converters and LVDS transceivers which are mounted on the underside of the larger power

board and interface boards respectively. Components are spread between the front and rear of the PCBs to aid a compact layout.

The support circuitry comprises the +3.3 V and +1.8 V linear isolated regulators required for the level shifters and sub-nanosecond gate driver along with a 12-bit DAC for controlling the gate drivers internal VCO.

3.5.3. Selecting Digital Isolators and DC-DC Converters for a High Slew Rate Operating Environment

The high slew rate and high EMI operating environment of a wide band gap bridge leg means certain components must be chosen with care. The signal isolators and the isolated DC-DC converters bridge the isolation boundary between the floating parts of the test bed and those with a fixed ground potential. These two types components need to allow their input and output ground potentials to slew with respect to each other at the full rate determined by the bridge-leg power stage. High di/dt and, for example, current oscillation in the power loop combined with inductance in the GaN HEMT package can cause additional high frequency changes in the potential of the floating copper planes that the isolators and DC-DC converters must accommodate.

3.5.3.1. Digital Isolators

The work in later sections will almost exclusively draw on data produced using the Texas Instruments ISO784x series of isolators. Prior to their availability and experimental work with 650 V GaN Systems GS66508P devices the sub-nanosecond gate driver testbed had used Silicon Labs SI864x series parts.

In line with their minimum common mode transient immunity specification (CMTI) listed in Table 5 Silicon Labs SI864x cannot withstand the >100 V/ns transients experienced with the GS66508P devices and a 400 V DC link. During experimentation exceeding the limit to this degree manifests as three in every ten double pulse switching events causing shoot through which is often destructive to one or both power devices and their associated gate driver.

Table 5 - Comparison of digital isolators.

Part	CMTI (min)	Input Supply	Output Supply	Propagation delay (Min/typ/MAX)
Texas Instruments ISO784x	100 V/ ns (all channels)	2.25 - 5.5 V @ < 8.6 mA	2.25 – 5.5 V @ < 3.3 mA	6 / 11 / 16 ns
Silicon Labs SI864x	50 V/ns (all channels)	2.375 - 5.5 V @ < 9.2 mA	2.375 - 5.5 V @ < 4 mA	5 / 8 / 13 ns
Silicon Labs SI838x	200 V/ns (low speed channels)	Signal Powered	2.25 - 5.5 V @ < 7.6 mA	3.8 / 4.1 / 5.6 us

Texas Instruments ISO794x proved sufficient however experimental data suggests the power stage design used in this work generates up to 50% higher dv/dt than the specified minimum. It is conjecture why they do not malfunction in the same way as the SI864x parts they replaced. It is possible this CMTI rating of 100 V/ns is conservative or that the duration for which the spec is breached for is important to it continuing to operate as expected.

The minimisation of any floating copper plane areas and signal trace length can be influenced by the choice of digital isolators. Isolators which have mixed channel directions, such as the ISO784x series, allow for the number of integrated circuits to be reduced because the test bed relies on signals to and from the sub-nanosecond gate drivers for normal operation. This also reduces the electrical load on the isolated power rails.

At the time of writing, the Silicon Labs SI838x series of digital isolators could be a viable alternative as they claim 200 V/ns CMTI at the expense of significantly higher propagation delay and variation in propagation delay.

3.5.3.2. DC-DC Converters

The DC-DC converters have a similar requirement to the digital isolators; the capacitance coupling their input to their output needs to be as low as possible. The isolated side of the digital isolators, level shifters, DAC, gate driver and linear voltage regulators all require their power to come across the isolation boundary.

Due to the high component count the isolated regions in the testbed have a high power requirement of approximately 0.5 W (100 mA at 5 V on the non-isolated side). Using a typical conversion efficiency of 80% this means that statically, the power requirement on the isolated side is 0.4 W. Transiently, the power consumption can be much higher with the sub-nanosecond gate driver able to deliver up

to 10 A peak current into the GaN HEMT gate. To keep the requirements of the DC-DC converter low this kind of peak is delivered from de-coupling capacitance in the isolated region.

Table 6 shows two of the DC-DC converters which were used in version of the test bed comparing, particularly their output power and isolation capacitance.

Table 6 - Comparison of isolated DC-DC converters.

Part	**Isolation Capacitance (TYP)**	**External Components?**	**Ouput Power**	**Shieled Case?**
Traco Power THN 15-2411WI	1000 pF [1940 pF with external components]	Yes	15 W @ 5V	Yes
Murata NML0505SC	19 pF	No	2 W @ 5V	No

When developing the sub-nanosecond gate driver test bed for work at high voltages with the GaN Systems GS66508P 650 V power devices, the Traco Power THN 15-2411WI isolated DC-DC converters were chosen. The main specifications for which can be seen in Table 6. The shielded case surrounding the converter and high output power makes them attractive for operation under the influence of high EMI. The THN 15-2411WI however has significant isolation capacitance internally.

Experimentation at 400 V showed that transitions in the test bed typically cover 10-20 ns. If this is approximated to a 20-40 ns period sinusoid the resulting frequency range required to represent a smooth transition between the on and off state would be 250–500 MHz.

During operation, it is posited the presence of this much isolation capacitance causes ‘pumping’ of the supply rail on non-isolated side of the DC-DC converter. Within 32 double pulse events in succession, where 150 ms rest time between double pulse test cycles is given for full load current reset, the non-isolated supply rail had risen by 0.7 V.

Revising the testbed design to use the Murata NML0505SC DC-DC converters resulted in over two orders of magnitude lower isolation capacitance. The ‘pumping’ effect is eliminated suggesting the internal isolation capacitance and recommended external isolation capacitance were the path across the isolation boundary.

Table 7 shows that the internal isolation capacitance of the THN 15-2411WI alone would offer less than 1 Ω of impedance to any spectral content in the 250 – 500 MHz range. This would give a very high chance of pulses of current crossing the isolation boundary via the isolation capacitance on ever switching event in the power stage. Any additional undesired oscillations in the power stage due to

the use of no resistance sequence or a non-optimised resistance sequence would only add to the problem.

Table 7 – Comparison of DC-DC converter isolation capacitance reactance.

Part	Isolation Capacitance (TYP)	Reactance @ 250 MHz	Reactance @ 500 Mhz
Traco Power THN 15-2411WI	1000 pF [1940 pF]	0.637 Ω [0.328 Ω]	0.318 Ω [0.164 Ω]
Murata NML0505SC	19 pF	33.5 Ω	16.8 Ω

The manufacturers application note for the THN 15-2411WI suggests using additional capacitance to couple the DC-DC converter input and output together. This is to reduce the quantity of EMI at the output of the converter by shunting it to the input, however, it also crosses the isolation boundary and counts as part of the total isolation capacitance. The value in brackets in Table 7 reflects the implemented total isolation capacitance.

Comparing the implemented implication of both DC-DC converters; the NML0505SC offers almost 2 full orders of magnitude higher impedance across the frequency range of interest. This effectively limits the conducted EMI across the isolation boundary due to high slew rates in the power circuit and would reduce the 'pumping' effect.

3.5.4. PCB Design Considerations for Digital Signalling in a High Slew Rate Operating Environment

Figure 29 - Photo of a via cross-section showing the copper layers and diagram of PCB materials stack up.

Capacitive coupling between 'noisy' power planes caused by EMI or normal operation and signals can lead to undesirable behaviour. The versions of the test bed which produced result for this work utilised a 4 layer, 0.8mm finished thickness PCB. Figure 29 shows a diagram and accompanying cross-section

photo of the layer of the material stack up used to minimise this effect. Anywhere a signal lies over a plane or planes at different potentials overlap on two adjacent layers they can be approximated to a parallel plate capacitor. Use of the 0.8mm finished thickness PCB to keep the separation of the plates small and therefore minimise the capacitance but resulting in larger reactance too. Current pulses drawn by ICs as they operate and EMI from switching activity in the bridge-leg is present in the power rails and signal traces by way of cross-talk. Increasing the reactance then limits the ability for ringing, oscillations and switching noise to propagate about the PCB.

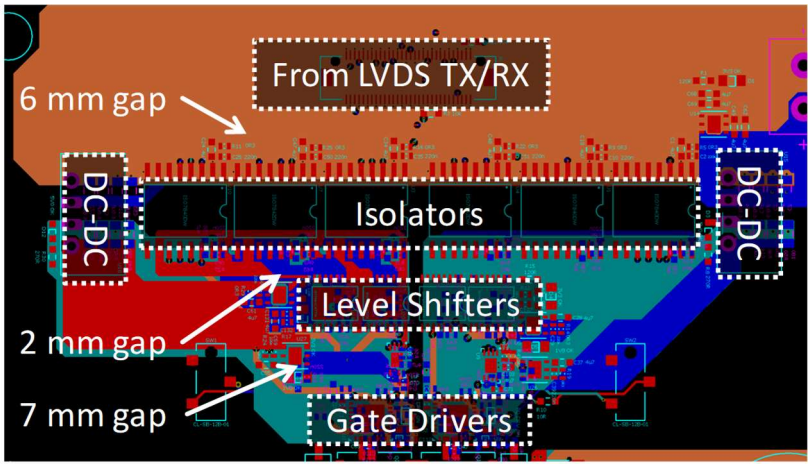

Figure 30 - The test bed PCB layout for the gate drive, programming and support hardware section.

In addition to the use of a 0.8 mm 4-layer PCB the lengths of trace carrying signals is minimised and sharp 90-degree corners eliminated. Trace lengths are kept small primarily by the placement of components close to each other as can be seen in Figure 30.

The length of traces contributes in two main ways to the system performance. As trace length increases so does the inductance of the trace to the value of approximately 1 nH per mm for a trace not above a ground plane, and traces act as either dipole or loop antennae.

In a high EMI environment with small signals, such as the test bed, the antenna effect is also considered. Specification of the DC-DC converters used 500 MHz as the upper frequency limit for emissions the bridge-leg generates through switching. This gives a ¼ wavelength of 150 mm up to which the efficiency of radiation and reception of EMI will increase. The longest traces on the layout in Figure 30 exist between the LVDS transceiver board-to-board connector and the digital isolators and are not longer than 35 mm. This is approximately five times shorter than the ¼ wavelength distance for 500 MHz and suggests the layout should not be susceptible to the antenna effect until ~2 GHz.

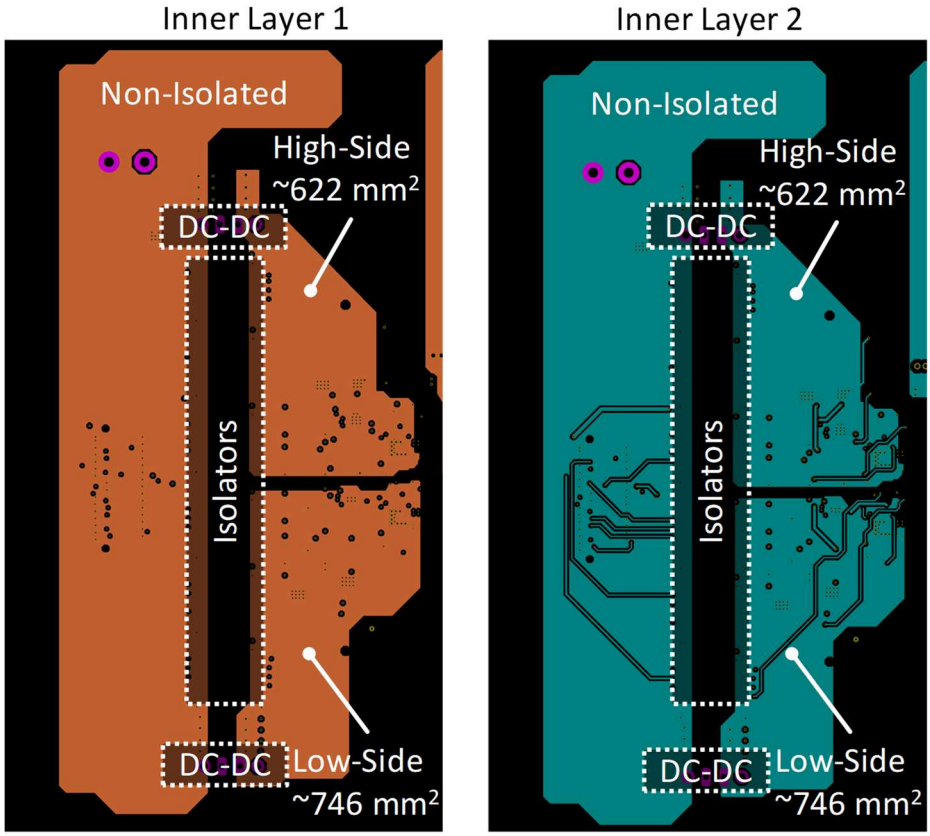

Figure 31 - The copper areas on the inner 2 layers of the test bed excluding the bridge-leg power stage.

Figure 30 showed all the copper layers of the PCB stacked on top of each other. If the two inner layers are isolated and separated the areas shown in Figure 31 are the result. In the sub-nanosecond gate driver test bed the inner layers are used to maximise signal integrity by having continuous ground planes beneath the two outer layers which signals are routed on.

This can be seen in Figure 31 where signal routing on these inner layers is used only as a last resort and it has been constrained to only one of the two. The only breaks in Inner 1 are due to vias at different potentials passing through the layer. Large ground planes like this are beneficial for high frequency performance where current takes the shortest route possible as its return path. Maintaining large continuous copper areas are used to ensure no signals are routed through 'open' space where they are not above a plane of their ground potential.

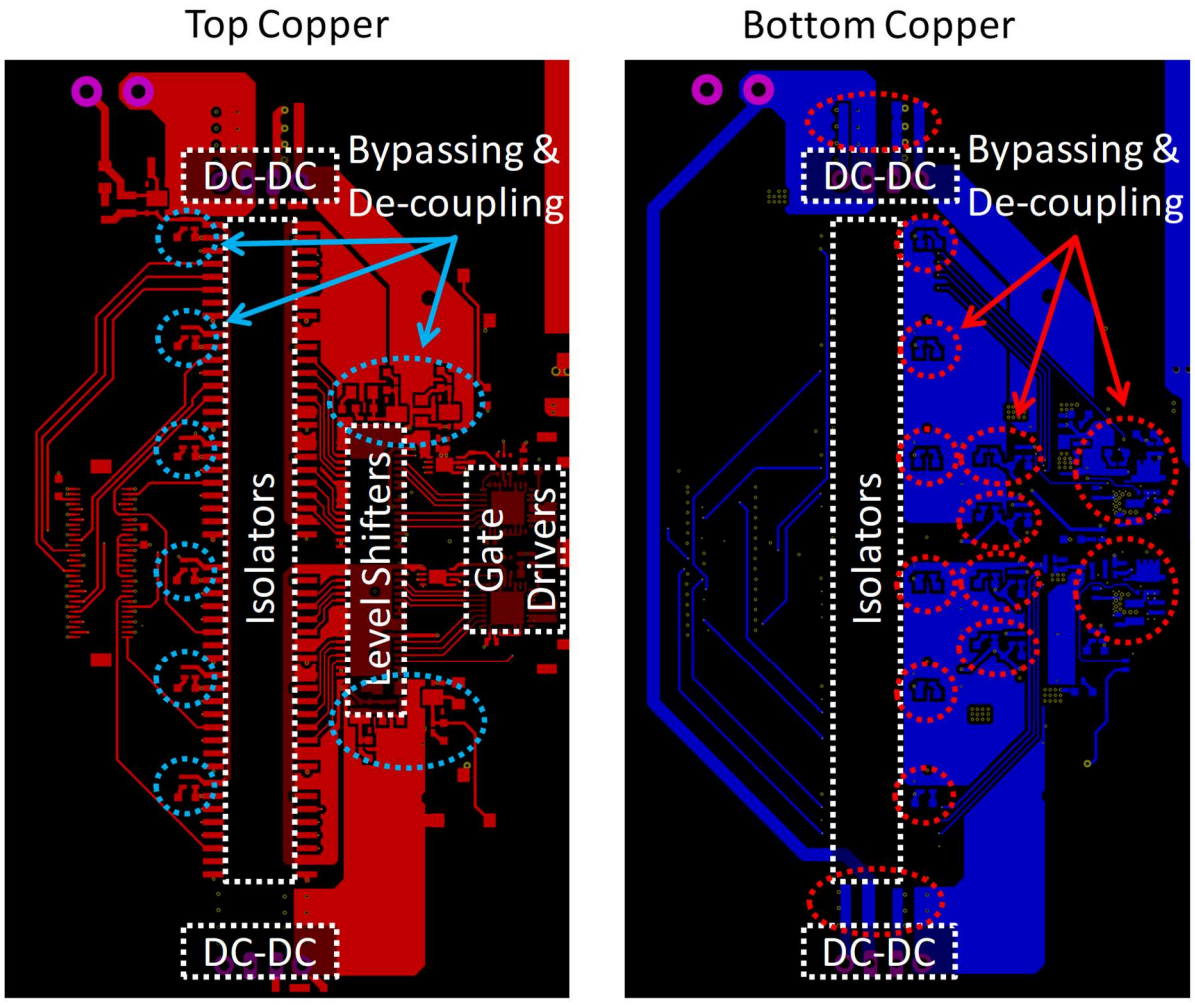

Figure 32 - The top (left) and bottom (right) copper layers indicating the individual de-coupling networks and their relation to the components they service.

Figure 32 demonstrates another aspect of the strategy adopted for placing components to that in Figure 30. All active components are concentrated on the front side of the PCB and positioned to minimise the number of vias required in the signal carrying traces. The parasitic capacitance and inductance of vias is approximated by the following equations. [93]

$$L \approx \frac{h}{5}\left(1 + \ln\left(\frac{4h}{d_I}\right)\right)$$

$$C \approx \frac{0.0555 * e_r * h * d_I}{d_O - d_I}$$

$$Z_0 = 31.6\sqrt{\frac{L}{C}}$$

Where d_I is the diameter of the via and d_O is the clearance hole diameter in a middle layer copper area. The use of a 0.8 mm PCB layout limits these parasitics but at high frequency (>100 MHz) signals or their harmonics could still interact with them. Vias also cause disruption to the return current path whose current density will try and follow that of the signal carrying trace. This causes problems as the return current path becomes hard to predict and design in a desirable way. Therefore, the number of signal-carrying vias is limited.

The digital side of the test bed is protected against RF energy and high frequency spectral content, not only in the signals but also in the power rails. Correct power de-coupling aims to isolate one component or section of the test bed circuitry from another and by-passing provides a low impedance path to shunt undesirable content to ground.

To maximise the effectiveness of the de-coupling and by-passing strategy used the following are considered in the system level design:

1) The networks are physically close to the component they are interacting with to minimise the current loop area between them and the active component [93]–[95]. This can be seen in Figure 32 where all the networks are highlighted for the front and rear of the PCB. Depending on the space allowance they are placed directly next to the active component, which is most desirable, or beneath the active component on the underside of the PCB.

2) The networks should not be separated from the active component by vias however this is traded off against the requirement to place them physically close [93]–[95]. Figure 32 shows that almost half of the de-coupling networks are placed on the underside of the PCB. This minimises de-coupling network loop area and allows for signal traces to not be routed through vias instead.

3) As RLC resonant networks formed of explicit components and parasitic elements individual networks have integrated damping resistance, they won't resonate at frequencies they will be exposed to.

4) They will form further RLC tuned networks with remote networks and are designed to not interact and resonate with them in combination with power distribution network parasitics.

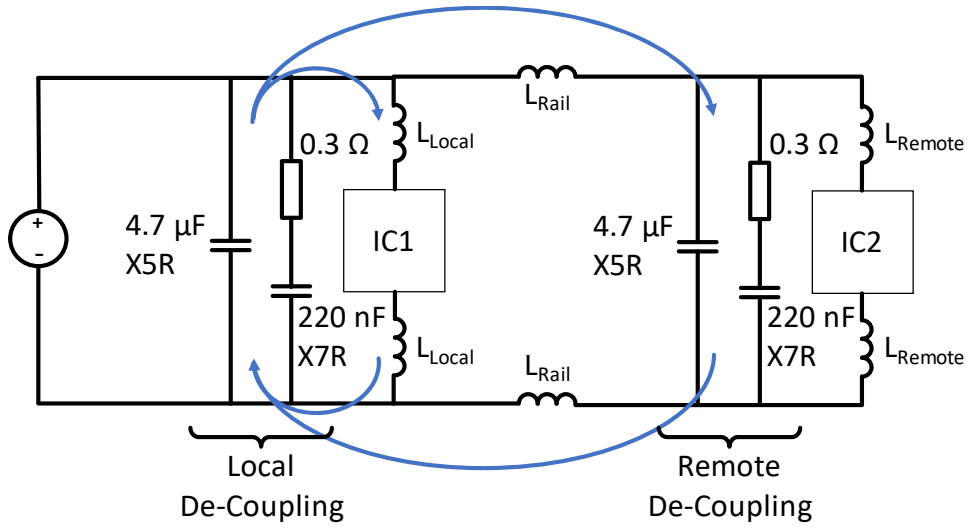

Figure 33 - Diagram of the designed damped de-coupling networks with an illustration of inter network interaction.

High performance ceramic capacitors are used to minimise the ESR and ESL in the de-coupling networks. The networks, shown in Figure 33, include a damping resistor for the smaller capacitor in the network which acts as the de-coupling element. This prevents the local network and the trace amounts of inductance between its components from forming an effective RLC resonant network and oscillating with itself. The damping resistance in each de-coupling network ensures that any local de-coupling network cannot oscillate with a remote one via the inductance of the power distribution network between them.

The larger 4.7 µF capacitor acts as the by-passing element with its reactance dropping below 1 Ω by 35 MHz Above 100 MHz, a single by-pass capacitor will present less than 400 µΩ of impedance and the parallel combination of all the networks will effectively shunt any EMI imposed on the power rails by the bridge-leg during switching to ground.

3.6. A GaN Bridge-leg with High Slew Rate Capability for Sub-Nanosecond Active Gate Driving

3.6.1. Introduction

The power stage of the test bed for the sub-nanosecond gate driver is a bridge-leg comprised of a pair of GaN Systems GaN HEMTs without external free-wheeling diodes. The sub-nanosecond gate driving this work focuses on is interested in the period of time where GaN HEMTs transition and shortly afterward. Therefore, the use of auxiliary commutation components like anti-parallel Silicon Carbide (SiC) Schottky diodes, which would reduce reverse conduction losses during dead time, is not needed.

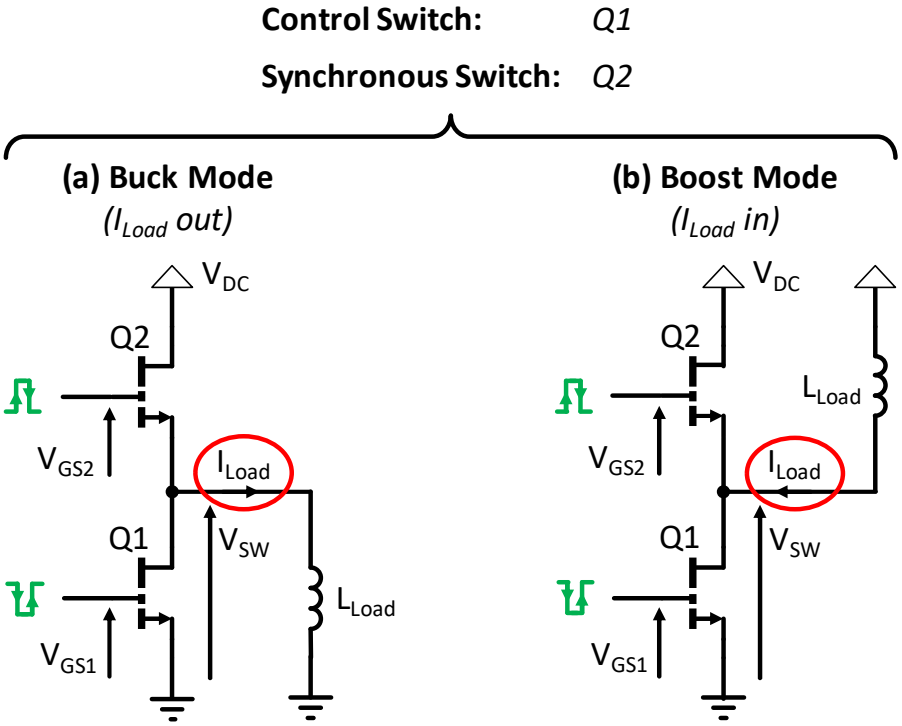

Figure 34 - Illustration to the current direction in and out of the switch0node with respect to the terms 'Buck' and 'Boost' Mode operation. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

The power stage can be configured for both buck and boost mode operation, either switch acts as the control switch and either the positive or negative DC link to be referenced to earth. For this work the operating mode of interest is boost mode with Q1 as the control switch, shown in Figure 34(b). This places Q1 in control of the load current, a transition under full load and a transition where it is blocking the full DC link voltage.

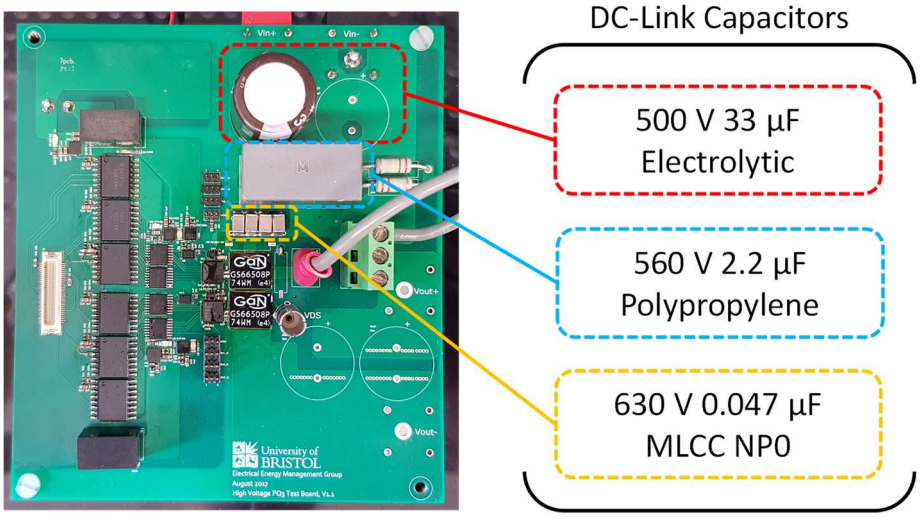

Figure 35 - A photo of a power stage with components populated for double pulse experiments highlighting the type and value of DC-link de-coupling capacitors.

The GaN Systems GS66508P has been used as the first available enhancement mode, non-cascode, 650 V rated power devices with low $R_{DS\text{-}ON}$ suitable for this work[4]. They are bottom side cooled devices which use the copper planes of the PCB as a thermal sink. This gives adequate cooling for experiments to be undertaken without an externally measurable change in device temperature occurring when large numbers of successive double pulse events are desired. The soldered thermal pad provides good thermal conductivity and allows double pulse experiments to be carried out without any supplementary cooling which could impede physical access to test points for instrumentation. This can be seen in Figure 35 where access to the, approximately 0402 component sized, pads between the gate drivers and power devices are the only place the gate voltage can be probed.

3.6.2. Designing a High-Performance Main Conduction Loop for GaN HEMTs

For the full potential of the sub-nanosecond gate driver to be realised the physical layout of the power stage is optimised such that it does not impede the performance of the GaN Systems GS66508P power devices. To do this the inductance of the main current conduction loop in the power stage is designed to be low. This is done at the expense of capacitance between adjacent layers. 3D modelling and parasitic extraction of the copper areas in the power stage suggest it to be 5 nH which was not the lowest figure reported[96] for a similar bridge-leg but enough for this work.

To minimise the main current loop inductance a vertical design, where current flows to and from a given point on an adjacent copper layer, is used. A vertical design has been reported [96], [97] to give significantly improved performance over a horizontal approach where the main current loop lies entirely on a single copper layer. This approach minimises the current loop area and therefore inductance because one dimension can be reduced to the distance between PCB copper layers.

Common source impedance in enhancement mode GaN HEMT bridge-legs has the potential to cause problems when combined with the low maximum gate voltage they possess. This is mitigated by the kelvin source connection on the GS66508P devices which allows the gate current loop to be almost completely separated from the main conduction loop. Peak di/dt observed during experimentation is over 1 A/ns meaning that even 1 nH of common source impedance between the gate drive and main loop would cause a 1 V shift in the ground potential of the gate drive circuit.

[4] Cascode 650V GaN HEMTs were available at the time from Transphorm in TO-247 packages. These were unsuitable as it places the driver in control of a Si MOSFET which in turn controls a d-mode GaN HEMT. Additionally, the TO-247 could make passing the effect of high bandwidth gate resistance sequences challenging.

3.6.3. Controlling High Frequency Current Paths in the Main Conduction Loop

High frequency current produced by the switching action of the bridge leg returns via the shortest path possible. In a vertical current loop design such as that used in the sub-nanosecond gate driver test bed means returning on the copper layer directly beneath the top copper to the low equivalent series resistance (ESR) and equivalent series inductance (ESL) ceramic DC-link capacitors. These are physically closest to the power devices and low impedance meaning they are electrically 'close' too compared with the plastic and electrolytic capacitors present on the DC link.

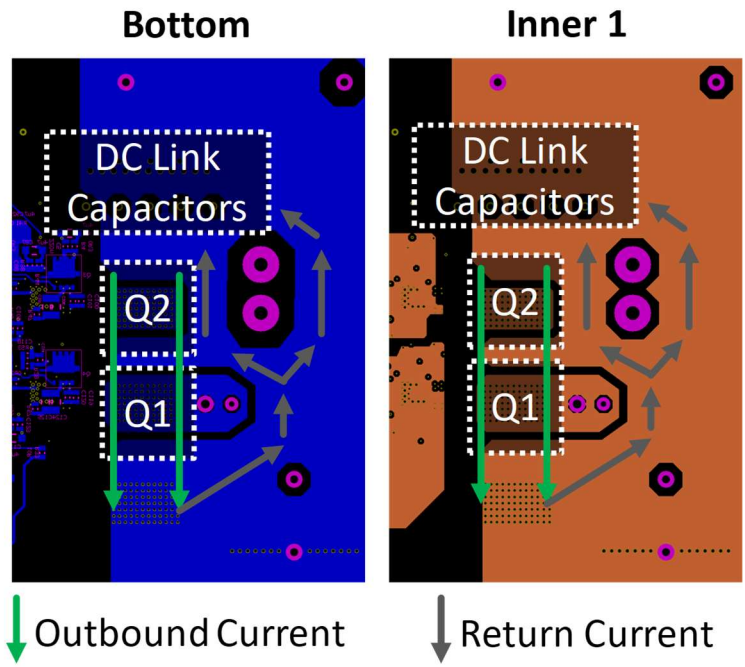

Figure 36 - Diagram of a non-working PCB design due to high power loop inductance.

Figure 36 shows the first inner copper layer and bottom copper layer of an unsuccessful PCB design, the parallel combination of these form the return current path for the main conduction loop. High power loop inductance and coupling to the isolated digital areas caused self-reinforcing oscillations for a load current of 2 A at 150 V.

The output capacitance of the GS66508P power devices change by a factor of 60x up to 400 V. Observation has suggested that this could be the cause of the self-sustained oscillation at 150 - 250 V, where the output capacitance is at its lowest, and that increasing the DC link voltage further causes the oscillation to disappear. In the case of the PCB layout from Figure 36 increasing the DC link voltage beyond 150 V caused the oscillations to grow in amplitude and multiple device failures due to shoot through after a single double pulse event.

Current from the DC link capacitors flows on the top copper layer where the power devices are mounted. Inner 1 and Bottom copper layers form the return current path to the DC-link capacitors but the majority of current flows through Inner 1 as it is physically closer and therefore has lower impedance. The presence of obstructions in the shortest current path cause expansion of the loop area and higher current density in certain areas, both of these effects lead to higher loop inductance than is desired.

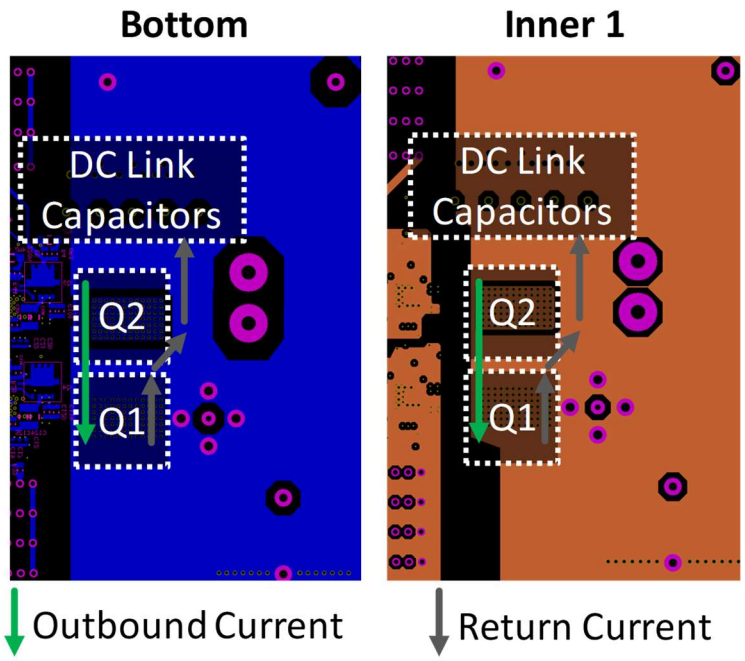

Figure 37 - Diagram of a working PCB design with difference highlighted.

Figure 37 presents the Inner 1 and bottom copper of an earlier design to that in Figure 36 used in the power stage that produced the high-voltage data used in this work. Current can flow through the thermal vias of Q1 and return more directly to the DC Link resulting in a smaller main conduction loop. The design from Figure 36 is an evolution of it which allows high bandwidth current sensing in the low-side power device source as well as the high-side drain.

An untested modification to correct the high loop inductance from Figure 36 is presented in Figure 38. The features highlighted in Figure 38 have made the following improvements:

1) Smaller creepage distance allowance. The copper areas should not be at a different potentials, since they are both connected to the source of the low-side device. The separation is only to force current flow underneath a current sensor positioned on the top copper layer. This gives a larger copper area on the bottom layer for current to flow which reduces current density and impedance. On Inner 1 the reduction has allowed an opening between the thermal vias

and through holes for the switch node voltage probe adaptor which gives another shorter route for high frequency current to return via.

2) RF PCB design inspired ‘guard’ rings intended, particularly for the high-side power device, where the thermal vias it surrounds are slewing at the same rate as the switch node. Therefore, it could help contain EMI that would otherwise couple into signals and planes in the isolated gate driver areas. These also form a short path for very high frequency current to return to the dc link capacitance that is more directly underneath current on the top copper layer.

3) Copper areas underneath the dc-link capacitors have been increased and with care taken to limit coupling into the high-side gate driver ground plane and intrude on creepage distance which is supporting the DC link voltage.

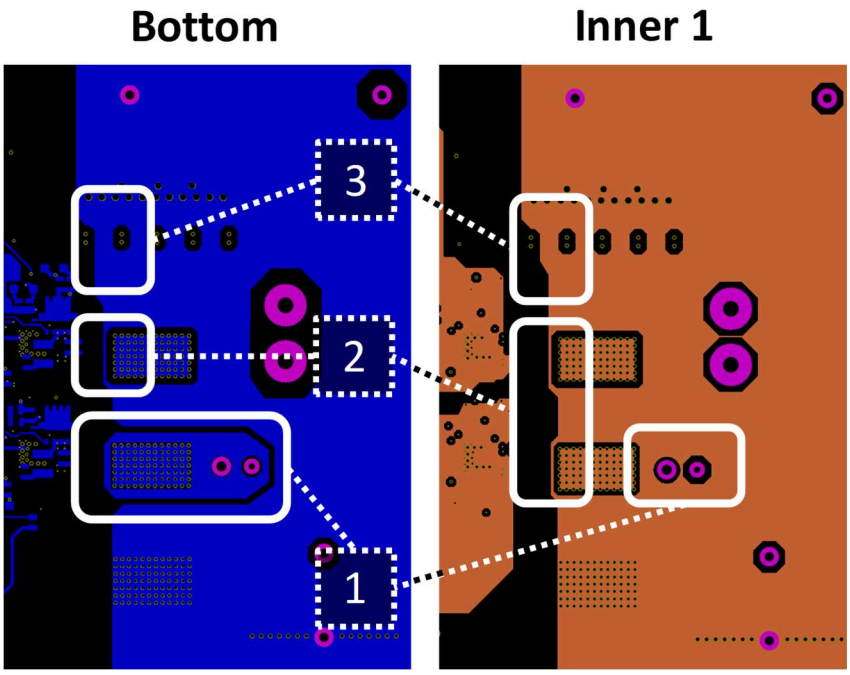

Figure 38 - Diagram of an untested design intended to correct the shortcomings of its predecessor.

3.7. Further Work & Limitations

Most of the time spent interacting with the GUI for configuring resistance sequences is spent performing only a few operations. Firstly, the ability to save and recall an entire GUI state including the double pulse experiment settings would decrease the time taken to begin experimenting after powering up the testbed. The next biggest time saving feature would be an easy way to move a configured fine driver pulse, including strength, delay and duration between clock periods. Currently this involves at least 6 operations to disable a fine driver, change clock period and then reconfigure

the pulse form memory. This leaves scope for mistakes to be made transcribing the settings and consumes large amounts of time as it is done numerous times during the development of a resistance sequence.

The latest version of the testbed hardware which is designed in this chapter and used for the work conducted in Technical Chapter 4 still involves significant interaction form the user during power-on and setup. At power-on and off the various power supplies used must be sequenced manually in conjunction with the C software running on the Xilinx SoC. This is to ensure hard-to-detect damage isn't caused to the LVDS transceivers on the test bed or to the output stage of the sub-nanosecond gate driver. This sequencing should be controlled in software to help minimise the risk of human error.

The problems presented by having many signals crossing the isolation boundary have been discussed, therefore reducing the number of signals is a prudent area of further work. It would reduce isolation capacitance further and reduce component count on the test bed boards. This could be accomplished by placing a microcontroller alongside the gate driver in the isolated regions and moving the data interface across the isolation boundary from a parallel one to a serial one. The digital isolators and their associated level-shifters are also the most power consuming components on the test bed, reducing the number of them could allow for smaller DC-DC converters with lower isolation capacitance to be used. A reduction in the component count would allow for faster and less complex debugging of assembly time problems or problems arising during operation after a power device failure.

The high count of fine pitch components leads to repair complications. Particularly where component footprints are defined by the solder mask alone repeated re-working of a PCB to repair it can cause the mask to fail. At best this makes it hard to then complete a repair and at worst it will make a PCB unusable any longer. Reducing active component counts will reduce the passive de-coupling networks associated with them and in-turn relieve this issue.

The digital isolators selected for use in the final version of the test bed are rated to 100 V/ns and slew rates greater than this have been measured in the power circuit of the test bed. Work should be conducted to verify the limit where they begin to function in an unexpected manner.

4. Sub-nanosecond Shaping of GaN HEMT Switching Transients

4.1. Acknowledgement and Attribution

Section 4.3 enabled the work in the following first author publications:

- “Shaping switching waveforms in a 650 V GaN FET bridge-leg using 6.7 GHz active gate drivers” [87]
- “Stretching in Time of GaN Active Gate Driving Profiles to Adapt to Changing Load Current” [88]

Furthermore, it enabled the work in the following co-authored publications:

- “Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns” [89]
- “A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI” [92]
- “Crosstalk suppression in a 650-V GaN FET bridge-leg converter using 6.7-GHz active gate driver” [90]

Section 4.4.2 is adapted from the co-authored publication “Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns” [89] originally presented at the 2016 IEEE Energy Conversion Congress and Exposition.

4.2. Aims

Now that a technical ability and the design of a testbed to implement it has been discussed, the measurement infrastructure around it is investigated.

High bandwidth probing of high voltage, ground referenced, and floating signals is challenging and existing tools for performing either have been developed around their suitability for Silicon power devices. At the voltages covered in this work, 0 – 400 V on the DC link, and above Silicon devices will be switching an order of magnitude slower than is the expected of comparable wide band-gap converters. Lower switching frequencies and lower slew rates mean that the probe-to-circuit interconnect, bandwidth and common mode requirements are not as strict as wide band gap circuits dictate.

This means that voltage probes without PCB scale co-axial interconnects and current measurements with shunts that add multiple nH of inductance are acceptable. This is no longer the case with increased switching speed and decreasing device parasitics such as output capacitance, and

comparable Super Junction Silicon MOSFETs have ~10x greater change in output capacitance compared to a similar GaN Device. Faster switching speed, smaller devices parasitics and smaller layout parasitics give rise to the need for care to be taken in setting up measurement systems around wide band gap power circuits.

The previous chapter established a test bed and the hardware requirements enabled to conduct work with a sub-nanosecond resolution active gate driver. This chapter will then focus on the following areas arising from a need to measure and verify the technical ability from the first technical chapter.

- What probing methods are effective for making the high bandwidth waveforms we expect to see visible?
- Can the high bandwidth signals generated by the sub-nanosecond gate driver be effectively transmitted to the gate of the power device without co-packaging them?
- Will a GaN HEMT respond to the high bandwidth gate signals that a sub-nanosecond active gate driver can produce during a switching transient or at all?

4.3. Investigation into Probing to make Sub-Nanosecond Driving Capability Visible

After establishing testbench hardware that should be capable of achieving sub-nanosecond active gate driving it needs to be verified. To be able to verify the operation and impact of the sub-nanosecond gate driver suitable probing arrangements that offer enough protection and bandwidth are required.

Being able to capture high fidelity waveforms that accurately represent the activity with the power device gate loop and main conduction loop allows for the development of resistance sequences and the calculation of performance metrics. To be able to observe signals at the frequencies and slew rates present in the bridge leg conventional power electronic probes and probing methods are not necessarily suitable.

Therefore, the available options must be weighed considering the practical limitations each has and the requirements of the signals which are going to be probed.

4.3.1. Voltage Measurement Analysis

Oscilloscope probes available for capturing voltage waveforms can typically be grouped into one of four categories:

1) **Single Ended Passive Probe** e.g. Rhode & Schwarz RT ZP-10, Tektronix TPP1000, PMK PHV 1000-RO
2) **Single Ended Transmission Line Probe** e.g. Rhode & Schwarz RT ZZ-80
3) **Electrically Coupled Active Differential Probe** e.g. Rhode & Schwarz RT ZD-30 + RT ZA-15 attenuator
4) **Optically Coupled Active Differential Probe** e.g. Tektronix TIVH08[5] + MMCX50X attenuator

Probes that fall into these categories, such as the examples listed, typically have advantages and disadvantages when used in the different measurement locations of Figure 39. They will be discussed after the next part of the selection process.

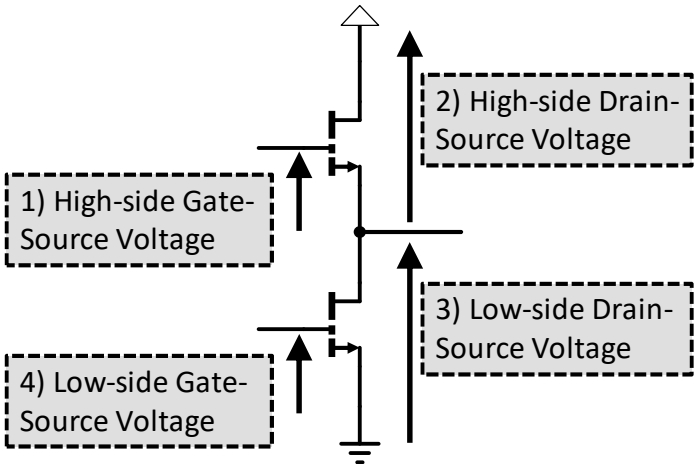

Figure 39 - Illustration of the locations where voltage is sensed in the testbed.

Figure 39 shows the most common measurement locations required for the development and testing of a bridge-leg. The most common circuit configuration for the testbed used in subsequent chapters has an earth referenced negative DC link and inductive load configured for boost mode operation. This makes the low-side power device as the control device and makes the voltages relating to the most desirable.

[5] This probe was released in 2018 after this work was conducted but is included for comparison purposes as it constitutes a new probe type which is noteworthy in this discussion.

Considering the probe specifications from Table 8 the various voltage measurements can be broken down. An assessment of the requirements and limitations of the probes can then be made along with a suitable choice.

Table 8 – The salient details of the specification for each of the probes considered for use in this work.

Probe / Technique	**R&S RT ZP-10**	**Tektronix TPP1000**	**PMK PHV 1000-RO**	**R&S RT ZZ-80**	**R&S RT ZD-30**	**Tektronix TIVH08**
Catergory	Single Ended Passive	Single Ended Passive	Single Ended Passive	Single Ended Transmission Line	Electrically Coupled Active Differential	Optically Coupled Active Differential
Bandwidth	500 MHz	1 GHz	400 MHz	8 GHz	3 GHz	800 MHz
Input Impedance	10 MΩ	10 MΩ	50 MΩ	500 Ω	1 M Ω	10 M Ω
Voltage	400 Vrms	300 Vrms	1000 Vrms (4000 Vrms transient)	20 Vrms	±60 V (differential mode) ± 22 V (common mode)	±25 V or ±50 V (differential mode) 60 kV (common mode)
Tip Capacitance	9.5 pF	3.5 pF	7.5 pF	0.3 pF	0.6 pF	3 pF
Rise Time	700 ps	Unknown	900 ps	Unknown	Unknown	450 ps
Floating	No	No	No	No	Yes	Yes

1) High-Side Gate-Source Voltage

Given the ~10ns duration [87], [89], [92] of a GaN HEMT gate transition the assumption is made that at least 1 GHz of effective bandwidth is required. The signal is nominally 0 - 5 V with transients up to 7 V and down to -2 V depending on the transition direction [87], [89], [92]. In the case of the high-side device it is with respect to a large common mode component in the form of the low-side drain-source voltage. This will be nominally 0 – 400 V with transients of up to 450 V and high frequency components. Given the ~10 ns duration [87], [89], [92] of a GaN HEMT gate transition the assumptions made that at least 1 GHz of effective bandwidth is required. The signal is nominally 0 - 5 V with transients up to 7 V and down to -2 V depending on the transition direction [87], [89], [92]. In the case of the high-side device it is with respect to a large common mode component in the form of the low-side drain-source voltage. This will be nominally 0 – 400 V with transients of up to 450 V and high frequency components.

The requirement for this to be a floating measurement, whilst the negative DC link is earth referenced, means that only the Tektronix TIVH08 can make the measurement but was not available when the test bed was designed, and this work conducted.

A battery powered oscilloscope and single ended voltage probe, such as the R&S RT ZP-10 or R&S RT ZZ-80, would not be suitable due to the significant capacitance to earth presented by the oscilloscope.

2) High-Side Drain-Source Voltage

Like the low-side drain-source voltage this is a 0 - 400 V high bandwidth waveform requiring at least 500 MHz bandwidth based on a 20-25 ns transition duration assumption [87]–[90], [92]. It has the same large common mode component as the high-side gate-source voltage. There are no failure modes that should cause voltages beyond these limits.

The most effective way to measure it is with a single differential voltage probe. The R&S RT ZD-30 could not be used as it has insufficient common mode voltage range and insufficient differential mode voltage range to make this measurement. The Tektronix TIVH08 with a different attenuator attachment is the most suitable candidate considered in this selection but was not available at the time the work was conducted.

This value could be measured directly with a probe such as the PMK PHV RO-1000 and a battery powered oscilloscope. However, the capacitance to earth would pose problems even at the limited 400 MHz bandwidth of the probe.

The final way for this quantity to be acquired is by calculation. The low-side drain-source voltage and DC link voltage can be subtracted to be left with the voltage across the high-side power device. This method however, is not desirable as it is susceptible to numerous sources of measurement error for such as DC offset error in either probe used and probe de-skewing error.

3) Low-Side Drain Source Voltage (a.k.a Switch Node Voltage)

Assuming normal circuit operation, the low-side drain source voltage has the same requirements as the high-side drain-source voltage and potential for failure modes.

The low-side drain-source voltage measurement is ground referenced which makes the PMK PHV 1000-RO the most suitable choice despite the bandwidth being below what is desirable. The high voltage rating will mean that repeated exposure to the switch node voltage will not damage it or the oscilloscope channel despite not being galvanically or optically isolated. The low tip capacitance is less important as it is small compared to the output capacitance of the low-side power device at all values of drain-source voltage.

4) Low-Side Gate-Source Voltage

This measurement is very similar to the high-side gate-source voltage except that it being ground referenced allows greater flexibility in probing arrangements.

The R&S RT ZZ-80 and R&S RT ZD-30 would both be good choices as they offer the best bandwidth and enough differential voltage range for the expected signal. The RT ZZ-80 however, has low input impedance which would cause it to have a significant loading effect on the output of the sub-nanosecond gate driver and could influence the effectiveness of the weakest output drivers. The 1 MΩ input impedance of the RT ZD-30 should keep leakage current to an acceptable level.

The structure of current GaN HEMTs means there is no isolation layer, as in MOSFETs, between the channel and gate structure. Therefore, it should be assumed that during device failure it is possible for the drain terminal to become connected to the gate terminal. This means the maximum voltage which could be experienced here in the testbed is as high as the full DC Link voltage with any inductance induced transients on top.

If a drain-source power device failure mode is then considered, both are eliminated as their maximum voltage limit is too low. Both probes would be damaged with the galvanic isolation of the RT ZD-30 giving the oscilloscope channel a good chance of survival. The RT ZZ-80 would likely fail along with the oscilloscope channel or the entire oscilloscope.

The R&S RT ZP-10 is the best choice for probing the gate to source voltage since it has the second highest bandwidth and second-best rise time of the remaining probes. The 2.5 mm diameter tip will give the best chance of a low inductance ground connection being possible too. With 10 MΩ of input impedance it should survive a gate-drain short failure of the power device long enough for the DC link to be de-energised even if the voltage exceeds its maximum rating. Even with high input impedance the high tip capacitance means that frequency components beyond the probe bandwidth in the gate signal could be bypassed to earth.

The Tektronix TPPP1000, like the R&S RT ZP-10, would be a suitable but the lower maximum voltage rating means that damage to the probe is more likely in the event of the drain-gate short and is then discounted.

The test bed circuit configuration used means that only the measurements surrounding the low-side power device are required. These can be performed with minimal risk to the measurement equipment and with enough bandwidth to provide useful insight.

4.3.2. Current Measurement Analysis

The techniques available for capturing current information from the main conduction loop can be grouped into one of five categories:

1) **Current Shunt + Passive Voltage Probe** e.g. Bourns CST0612-FC-R0005-E + Rhode & Schwarz RT ZP-10
2) **Current Shunt + Active Differential Probe** e.g. Bourns CST0612-FC-R0005-E + Rhode & Schwarz RT ZD-30
3) **Co-axial Current Shunt** e.g. T&M Research SSDN-05
4) **Hall Effect Active Current Probe** e.g. Keysight N2783B
5) **Field Probe Current Sensor** e.g. University of Bristol Infinity Sensor [25] + Rhode & Schwarz RT ZP-10

As with the voltage probe selection process the measurements that it is desirable to take must first be identified.

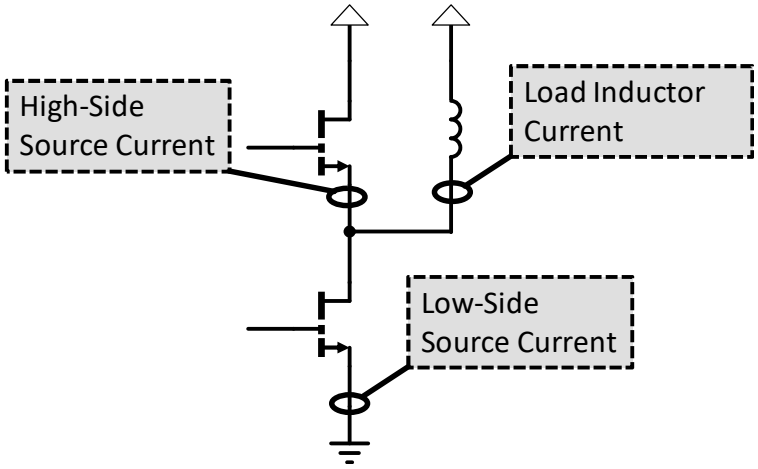

Figure 40 - Illustration of the ideal locations for current to be sensed in the testbed.

Figure 40 shows the ideal locations to capture current information from the main conduction loop. The source current in both power devices is preferred to the drain current as It is indicative of the current that has flowed through the power device. This means that any current capacitively coupled into the gate loop via the gate-drain capacitance is discounted. In devices where a separate source connection is provided for the gate driver, such as the Gan Systems GS66508P, the gate loop current is also removed when the measurement is taken at the source terminal.

Placing any sensors in the source of the power devices cause and accompanying changes to the PCB layout causes an unacceptable increase in main conduction loop inductance from the track length

introduced alone. If 1mm of outer layer trace introduces ~ 1 nH of inductance, then any addition to the < 10 nH main loop inductance is significant.

Figure 41 shows the revised locations for current sensing in the test bed which will be discussed in conjunction with the technique used to sense current there below.

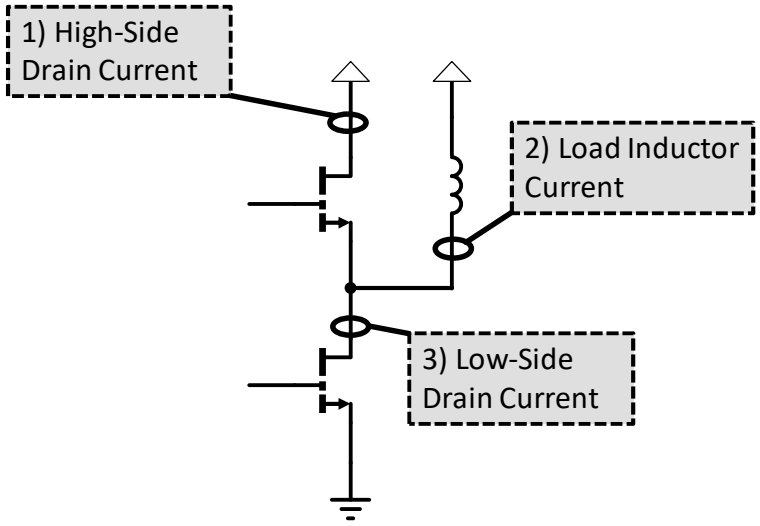

Figure 41 - Revised current sensing locations in the testbed considering the impact on PCB layout.

Considering the techniques from Table 9; the various current measurements shown in Figure 41 can be broken down. Then requirements and limitations of the techniques can then be assessed along with a suitable choice made.

Table 9 - Current measurement techniques and relevant performance criteria for selection from.

Probe / Technique	**Bourns CST0612-FC-R0005-E + R&S RT ZP-10**	**Bourns CST0612-FC-R0005-E + R&S RT ZD-30**	**T&M Research SSDN-05**	**Keysight N2783B**	**University of Bristol 'Infinity' Sensor + R&S RT ZP-10**
Category	Resistive Shunt + Passive Voltage Probe	Resistive Shunt + Active Differential Probe	Co-axial Resistive Shunt	Hall Effect Active Probe	Differential Rogowski Coil Field Probe
Bandwidth	~500 MHz	~1 GHz	400 MHz	100 MHz	~350 MHz
Rise time	~1 ns (limited by probe and connection)	~ 500 ps (limited by probe and connection)	1 ns	3.5 ns	~1 ns (limited by probe)
Insertion Impedance	~1 nH	~1 nH	<1 nH	N/A	~1 nH
Current Limit	10 A @ 400 V	10 A @ 400 V	20 A @ 400 V	30 A	Not Applicable
Power Limit	1 W (5 W short term)	1 W (5 W short term)	2 W	Not Applicable	Not Applicable
Floating	No	Yes	No	Yes	Yes
Impact on Main Loop Layout	High	High	Medium	Very High	Low

1) High-side Drain Current

Using the same justification as for the voltage probes; the expected current transition duration of the power devices is ~20-25 ns. This means that a minimum bandwidth of the probe is 400 - 500 MHz. The fast overcurrent transients resulting from device capacitances charging and discharging will increase this in practice if absolute amplitude accuracy is desired.

The two options involving the Bourns CST0612-FC-R0005-E current shunt will provide the highest fidelity measurements of all the options. However, the large increase in main conduction loop inductance due to the layout changes required to include them makes them unsuitable.

The next highest bandwidth technique, the T&M RESEARCH SSDN-05 co-axial current shunt, and similar part have been used in literature as an appropriate method for high bandwidth main conduction loop current measurement. In the testbed for this work it would introduce too much additional inductance and must be ground referenced or connected to a battery powered oscilloscope. Using a battery powered oscilloscope would have the same problems as voltage probe measurements with one and therefore the SSDN-05 is discounted.

Using a University of Bristol 'Infinity' sensor (See Appendix C for more details) in combination with an R&S RT ZP-10 passive voltage probe gives the highest fidelity possible for the lowest impact on

the main conduction loop. It only requires that, for the size of sensor available[6], a portion of the copper leading to the high-side drain is concentrated to a section of track directly under the sensor. The down side to this sensor is that the voltage it outputs is proportional to di/dt and so requires calibration and integration of the output over time to reconstruct the drain current waveforms which are shown in this work.

2) Load Inductor Current

The core purposes of this measurement in this work are two-fold. Firstly; to provide a check for the actual current during a double pulse event after a calculated inductor charge time has been executed. Secondly; it provides a DC calibration point for the integrated output of sensors like the UoB Infinity Sensor. For these purposes it is a low bandwidth (<100 MHz) moderate magnitude (<20A) signal.

There is the potential for there to be significant high frequency spectral content above the self-resonant frequency of the load inductor. This makes it desirable to be able to measure this current from DC to the GHz range as it is with the power device drain current but not essential.

It has no requirements for insertion impedance or for how invasive the measurement can be since it doesn't impact the main conduction loop. The load inductor is connected using short lengths of wire to terminals on the testbed.

The Bourns CST0612-FC-R0005-E current shunt options would also provide the highest fidelity measurements for the load inductor current. However, of the two options, only one allows for the measurement not to be ground referenced. Using the RT ZD-30 to measure the voltage across the shunt would require it to withstand switch node voltage swinging between 0 V and the positive DC link voltage, 400 V, with transients on top. It's limited common mode voltage range therefore means it is unsuitable for this option.

The T&M RESEARCH SSDN-05 co-axial current shunt, for the same reasons as the High-Side drain current isn't suitable for measuring the load inductor current and is discounted.

The Keysight N2783B can perform floating measurements and since it is a hall effect sensor that clamps around the lead to the load inductor, the common mode voltage range experienced will have no effect.

[6] Further work since the development of the sensor used in this testbed has shown that the matching of sensor size and trace is possible to reduce the need for reducing the trace as far as is done in this work.

3) Low-Side Drain Current

Based on the same assumptions as for the high-side drain current the low-side equivalent has the same specifications. Being in the drain of the low-side device means that it is still floating. Therefore, for the same reasons discussed for the high-side drain, only the UoB field probe sensor is a viable option. However, this would force the power devices to be moved further apart to make the required space for the sensor between the switch node and the drain of the low-side GaN HEMT.

Some knowledge of the current in the low-side GaN HEMT is required for the calculation of performance metrics like switching loss. The only remaining way is to infer the value using the measurements available. In the case of the test bed and the work in subsequent chapters this is the high-side drain current and load inductor current.

The main limitation of this method is that it assumes the high-side drain current and load inductor current measurements available have enough bandwidth to capture all the dynamic range available. With this assumption and the application of Kirchoff's Current Law at the switch node the following can be said to be true.

At turn-on of the low-side device the full load current is being conducted by the high-side device and the turn-on of the low-side device will control the turn-off of the high-side device. The current waveform of the high-side power device's output capacitance charging will be representative of the low-side device's current waveform as it turns-on; during turn-on it takes up load current from the high-side device. The assumption of enough bandwidth to capture the full dynamic range means that there has been no high frequency interaction with the load inductor and only the two power devices interact with each other.

Since the high-side drain current measurement is the integrated output of di/dt in the drain current it requires its gain to be calibrated. This is done by the assumption that the end value for the low-side drain current must be the full load current. Therefore, the output of the integration is linearly scaled to match the output of the Keysight N2783B probe.

With the limitations noted it is possible to attain the three current values from only two recorded values. The work to test the validity and impact of these assumptions is noted in the final section of this chapter.

4.3.3. Final Probe Selection

Collating the outcome from the previous two sections, down selecting probes and measurement locations, Table 10 can then be formed. In specific cases where probe details change, they will be stated, otherwise the probes used and their locations within the testbed will be as in Table 10 and Figure 42.

Table 10 - Probe models, details and their usage throughout this work.

Usage	**Probe Model**	**Customisations?**
Load Inductor Current	Keysight N2783B	None
High-Side Drain Current	UoB differential Rogowski 'Infinity' field probe current sensor + R&S RP-ZP10	PMK 2.5 mm PCB adapter & fine wire gauge twisted pair to infinity sensor
Low-Side Gate-Source Voltage	R&S RT-ZP10	Fine pitch spring pin ground suitable for 0402 SMT pads
Low-Side Drain-Source Voltage	PMK PML HV	PMK 5.0 mm PCB probe adapter

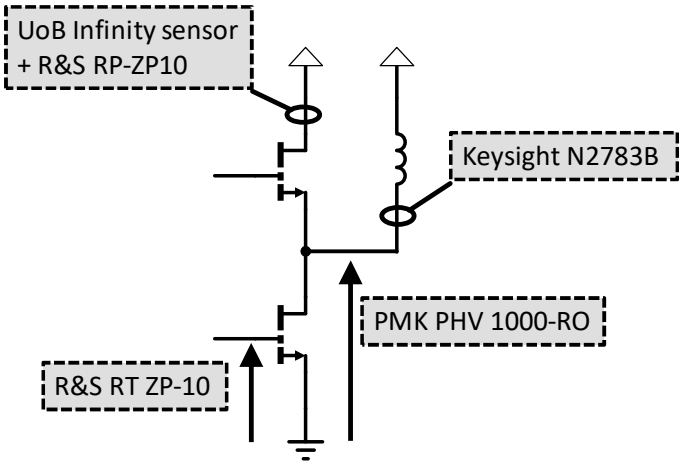

Figure 42 - Probe locations, probes in use and the quantities being measured in the test bed.

4.3.4. Probing Single Ended Voltages

Single ended passive voltage probes are the most susceptible to problems arising from poor probing technique or the effects of probe tip loading on the circuit under test. Poor ground connections with a large current loop area cause inductance which will impact the waveforms observed.

High input impedance passive voltage probes, such as those used in the testbed, typically have 3-6x the tip capacitance of similar active probes. This can mean 7-10 pF compared with 1-3 pF which loads and interacts with the circuit under test.

For example, the probe used for measuring the Low-Side Gate-Source voltage has 9.5 pF of tip capacitance and the sub-nanosecond gate driver is capable of outputting down to 100 ps pulses every 100 ps. These pulses will contain significant spectral content up into GHz however the reactance of the tip capacitance has fallen to below 10 Ω by 2 GHz and acts as a strong by-passing path for the high frequency content needed to for fast pulses to occur.

The sub-nanosecond gate driver has a peak source current capability of 10 A for the shortest fine driver pulses, so the impact of this pull-down effect is limited. However, for a conventional GaN gate driver such as the Texas Instruments LM5114 which can source 1.3 A, a strong pull-down path for high frequency content (caused by the probe measuring the gate-source voltage) will significantly impact the switching transition. This could then complicate the selection of a fixed gate resistance for conventional non-active drivers.

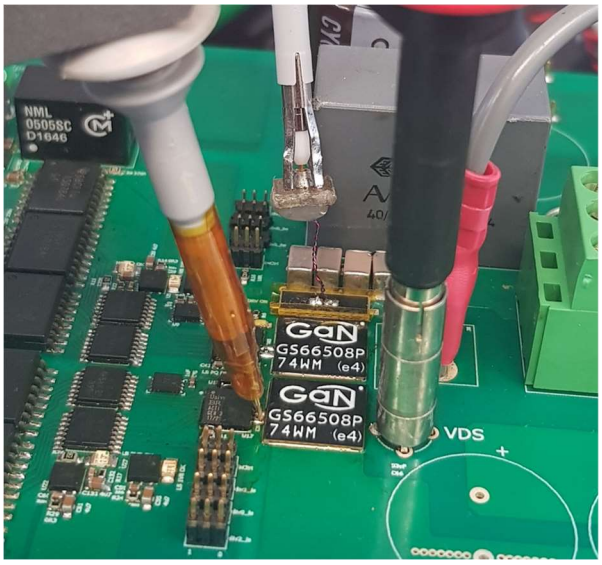

Figure 43 - The main measurement points, with probes in place, of the bridge-leg.

Figure 43 shows the proximity of the measurement locations and the limited space available for interconnection methods on the testbed. The performance of the main conduction loop is the primary concern and so the customisations made to probes are aimed at both measurement fidelity and making compact connections to the testbed.

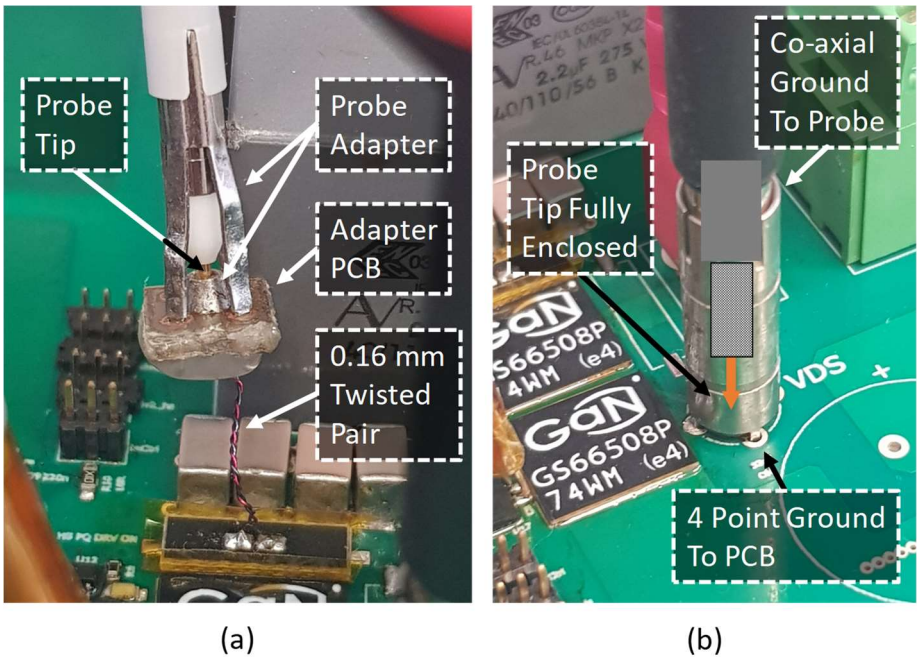

Figure 44 - PMK 2.5mm and 5.0mm PCB probe adapters used in the testbed.

PMK 2.5mm (Figure 44.a) and 5.0mm (Figure 44.b) PCB probe adapters provide a stable mechanical connection and favourable electrical connection to the test bed. Using co-axial PCB voltage probe adapters allows them to be integrated into the PCB design such as for the switch node voltage in Figure 44.b. They are also be used in a stand-alone manner for the UoB differential Rogowski 'Infinity' field probe current sensor . The 2.5mm co-axial adapter adapts the probe tip to a fine twisted pair in Figure 44.a and then to the sensor itself. The co-axial nature of the ground connection and enclosure of the probe tip means they have high immunity to the radiated EMI of the bridge-leg and minimal current loop area.

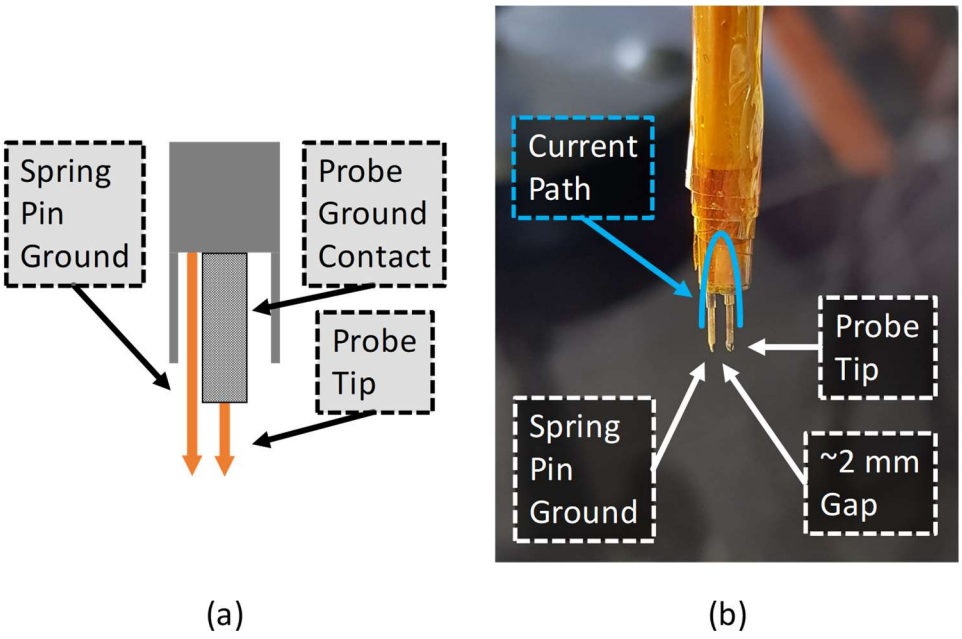

Figure 45 - Modified R&S RT ZP-10 voltage probe with low inductance ground connection for measuring gate voltages.

The gap between the gate driver and power device, visible in Figure 43 and approximately the width of a 0402 SMD component, is primarily for voltage isolation between the power circuit and isolated regions. The customisations made to the Rhode and Schwarz RT ZP-10 voltage probe allow the exposed pads in this narrow gap to be probed and to be done with a small current loop area.

The RT ZP-10 probe's construction allows for a spring pin, like the probe tip itself, to be inserted between a plastic shroud and the ground collar of the probe as shown in Figure 45.a. This is secured in place with Kapton tape resulting in an assembly like that in Figure 45.b. The gives a very small current loop area for the measurement when the spring pins are compressed and their length reduced which results in low inductance.

4.3.5. Current Measurement in the Main Conduction Loop

Observation of only the voltage waveforms in the power stage allows limited insight to be gained about the impact of sub-nanosecond gate driving on switching performance. The measurement of current at high frequency in the main conduction loop is needed to be able to calculate key performance parameters such as switching loss in power devices. Due to the presence of inductance in the conduction loop the voltage waveforms present are a result of the current waveform and so direct measurement of it also removes a level of disconnection between the resistance sequence used and the effect it has.

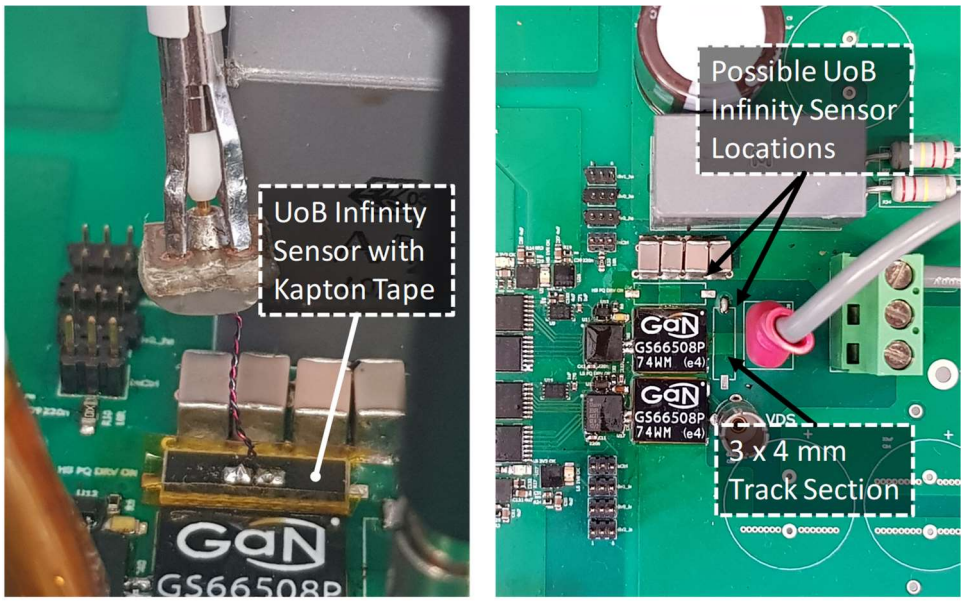

Figure 46 - Closeups of the UoB differential Rogowski 'Infinity' field probe current sensor and the impact it has on the layout for it to be included.

The low-side device being the control device for the work in subsequent chapters means that drain current of it is a desirable quantity. The field probe sensor used in this work allows for low impact on the loop inductance whilst still being able to acquire high bandwidth current measurements. In this case, shown in Figure 46.b, only a 4 mm length of 3 mm wide track is required to carry the current to be measured. It's inserted between the high-side power device drain and DC link decoupling capacitors where all of the current is flowing on the top copper layer already. The 'Infinity' field probe sensor, with a layer of Kapton tape for increased creepage protection, is then placed on top of the exposed track segment and the di/dt in that track segment sensed.

4.3.6. De-skewing Mixed Probes

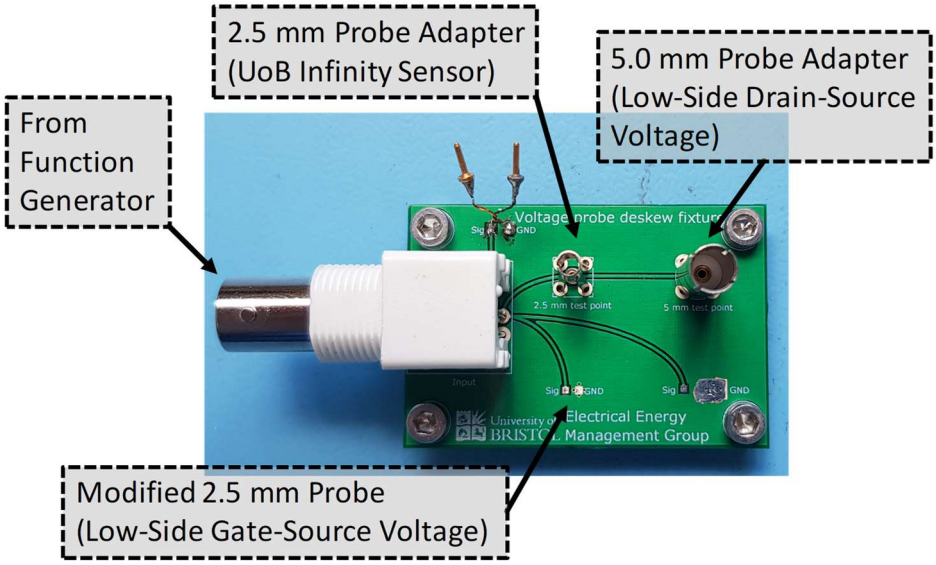

Figure 47 - The voltage probe de-skewing test fixture used for this work.

De-skewing of the voltage probes used for the low-side gate-source voltage, low-side drain-source voltage and infinity sensor were performed using the fixture shown in Figure 47. After allowing the oscilloscope, a Rhode & Schwarz RTO 1024 or RTO 1044, to thermally stabilise all probes are attached simultaneously and the fixture driven with a short rise time square pulse train from a Keysight 81150A. This allows compensation and de-skewing to be performed together whilst a Y-split of the signal from the function generator is fed to a separate oscilloscope channel for triggering and all voltage probes are then aligned to it.

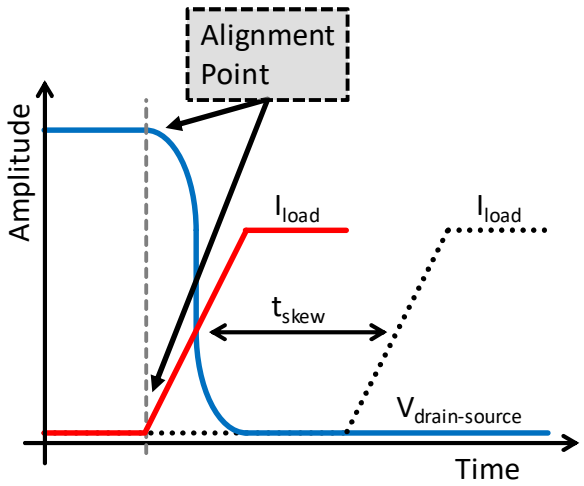

Figure 48 - Representative illustration of the alignment method used for the Keysight active current probe.

The Keysight N2783A active current probe used for measuring the load current is de-skewed separately as it has ~1 µs of signal delay and cannot be done in the same way. The testbed bridge-leg

is used, as it has low inductance in the main conduction loop, to generate a 'fast' current transition in a resistive load. The testbed circuit configuration is unchanged except for a resistor in place of the load inductor. The Keysight N2783A current waveform is then aligned on a transition edge to the PMK PHV 1000-RO probe switch node waveform and is treated as de-skewed. This is shown in Figure 48 where the start of the load current rise, caused by the low-side device turning on, is de-skewed until it aligns with the start of the fall in low-side drain-source voltage.

4.4. Getting Sub-Nanosecond Gate Signal Pulses to the Power Device Gate

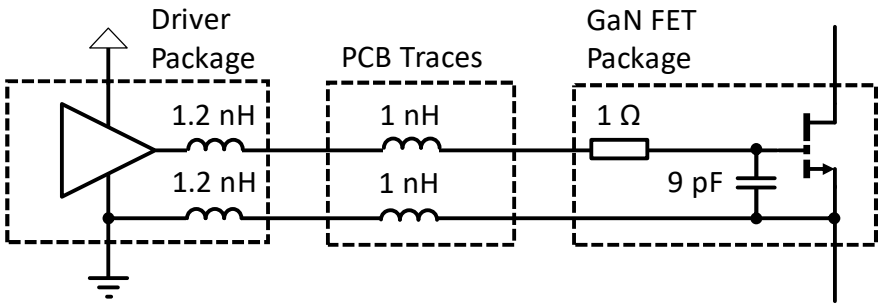

Figure 49 - A simplified representation of the dominant parasitic elements of the gate current loop which act to filter the gate drive waveform.

In Figure 49 the values for the simplified lumped parameter representation of the gate loop are determined using a variety of techniques. ANSYS Q3D Extractor provided parasitic extraction for the sub-nanosecond gate driver package whilst the PCB traces are estimated by a ~1nH per mm of microstrip rule-of-thumb and the GaN HEMT package by examination of the GaN Systems GS66508P SPICE model file. This method does not take account of mounting quality variation or manufacturing tolerance of parts, but they are assumed to be factors of negligible impact.

The parasitic elements in the gate conduction loop behave like a low pass filter for desirable high bandwidth content of the sub-nanosecond gate resistance sequences. The gate driver package alone presents approximately half of the gate loop inductance. Therefore, it must be verified that the high bandwidth signal can be transmitted out of the drive package effectively before connecting a power device which has additional parasitic capacitances coupling the gate loop into the main conduction loop.

4.4.1. Verifying Sub-Nanosecond Gate Drive Output

In addition to testing the impact of package parasitics on the desired gate waveform the timing of the synchronous elements to the internal VCO and the asynchronous delay elements needs to be tested.

The synchronous sub-system need testing to find the range of VCO frequencies for which they function as expected. The delay elements need their real values to be checked against the design values and

the mapping of DAC output setting to the resulting VCO frequency needs to be verified. These allow the functionality of the driver to be confirmed but also help accurately create representations of the programmed resistance sequences which depend upon the timing information.

To ensure the asynchronous sub-nanosecond timing capability of the gate driver used for this work a test is used that is immune to the jitter at the input to the gate driver and any variation in the internal VCO frequency. This step verified the function of the first generation of sub-nanosecond gate driver as the sequencing and timings elements of later generations are derived from the same design.

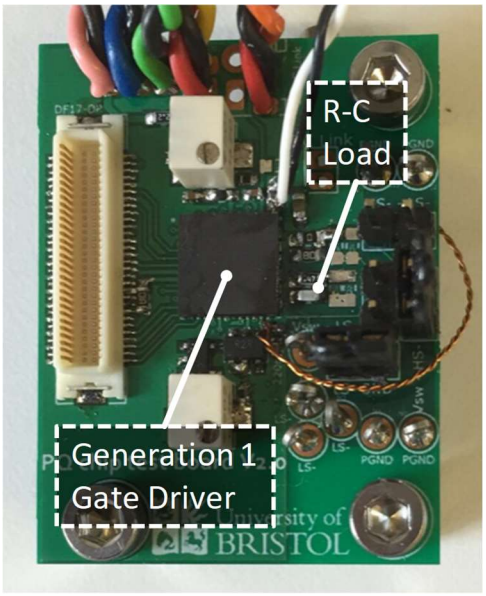

Figure 50 - Photo of the test board used for sub-nanosecond gate driver output testing.

GaN HEMTs, such as the GaN Systems GS66508P, have a delicate gate structure rated to a low maximum voltage (7 V[7]) which will then fail if exposed to small overvoltage transients. The 100 ps duration of the shortest gate driver output pulse and ~4 nH of gate loop inductance require only a modest strength driver before large inductive transients are generated. If damage occurred to the gate it could then skew results part way through an automated test run. Therefore, all testing and verification is performed with a passive load that is representative of the gate of a GS66508P power device. In this case a 10 pF load capacitor and 1 Ω load resistor are used.

Figure 50 shows the test board with Generation 1 sub-nanosecond gate driver and RC dummy load mounted for this testing stage. It mimics the gate loop layout as closely as possible for both the early low voltage EPC EPC2015 testbeds and the later GaN Systems GS66508P based high voltage testbeds.

[7] This has been revised several times during this work from an original 0 -> 5 V absolute maximum rating up to -2 –> 7 V.

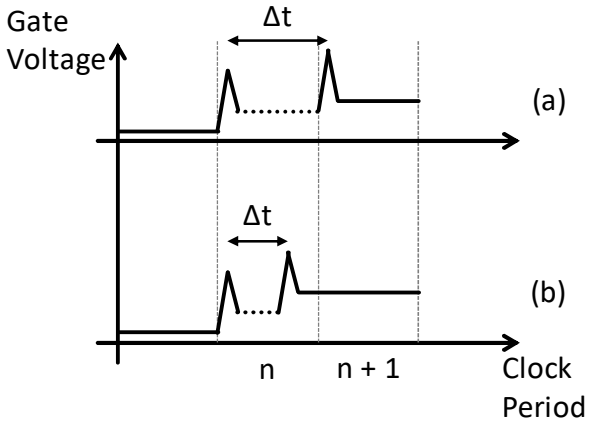

Figure 51 - Diagram of the methods used to verify sub-nanosecond driver synchronous and asynchronous timing capability.

Resistance sequences are generated and programmed into the gate driver to, on a pull-up edge, generate a short pull-up pulse at the beginning of the first gate driver clock period to trigger the oscilloscope in a consistent location. This step isolates measurements from the jitter introduced in sampling the gate signal input to the gate driver at the internal VCO frequency and propagation delay variation within the driver. The sequences generated have two main purposes and ways of achieving them:

1) To verify the synchronous part of the driver as shown in Figure 51.a; a pulse is generated at the start of one or more consecutive clock periods. The time difference between the pulses is checked to ensure it matches the programmed VCO period where a divided version is present at a pin on the driver package for measurement.

2) To verify the sub-nanosecond elements as shown in Figure 51.b; In the same clock period after the triggering pulse a later sub-nanosecond fine driver generates a second pull-up pulse with varying asynchronous delay relative to the first. The time difference is measured from oscilloscope data and the timings confirmed against the programmed value.

This test is automated to be able to check all aspects of the driver's functionality although only a small number of VCO settings are tested compared with the 10-bit resolution of the DAC used to set the VCO frequency.

4.4.2. Verifying Sub-Nanosecond Gate Drive Activity in the Main Conduction Loop with EPC EPC2015 40 V GaN HEMTs

Having verified the output of the sub-nanosecond gate driver by monitoring the gate voltage waveform it is assumed the high bandwidth waveforms are reaching the power device gate. The voltage waveform is the result of the gate driver charging the parasitic elements that make up the

gate capacitance. If the effects of the resistance sequence are seen in it, and the correct mounting of the power device has already been verified, then it is concluded that they have also reached the gate of the power device.

Performing a similar test to that detailed in the previous part of this section is complicated by the behaviour of the power device and how its characteristics change throughout a transition. In the boost mode, low-side control switch configuration the turn-off edge would not be more useful as the voltage across the power device during turn-off is controlled predominantly by the load current.

Due to this, a test focussed solely on mapping the programmed sequence to changes in individual main or fine driver changes wasn't performed. Their impact was instead assessed by using simple resistance sequences applied to power devices whilst monitoring power circuit waveforms.

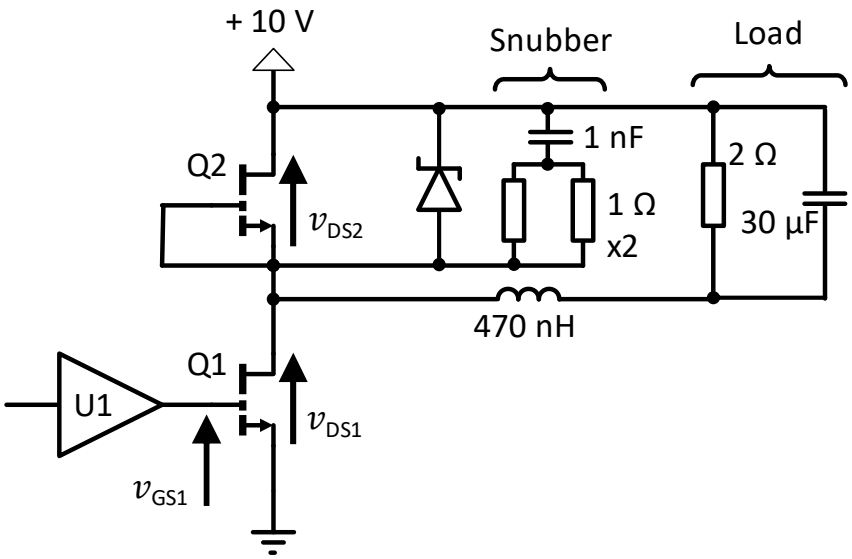

Figure 52 - The circuit configuration used for experimentation with generation 1 sub-nanosecond active gate drivers. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

The testbed circuit configuration used for initially assessing the impact of the sub-nanosecond active gate driving with a Generation 1 driver is depicted in Figure 52. The low voltage nature of the design allows for all points to be probed with the R&S RT ZD-30 active differential voltage probe if required but has no provision for current sensing in the main conduction loop[8].

The circuit is a high-side referenced buck converter intended for continuous switching which allows for power stages voltages to be kept low and the control device, $Q1$, to be ground referenced. The synchronous GaN power device is diode connected but due to concerns about losses during self-

[8] The University of Bristol Infinity Sensor was still being prototyped at the time this work was carried out in 2015 and 2016

commutated reverse conduction and anti-parallel free-wheeling Schottky diode is present. The added parasitic inductance and capacitance of the diode the freewheeling diode introduces across $Q2$ can cause oscillations during the turn-off of $Q2$ and so a snubber is introduced to combat it them.

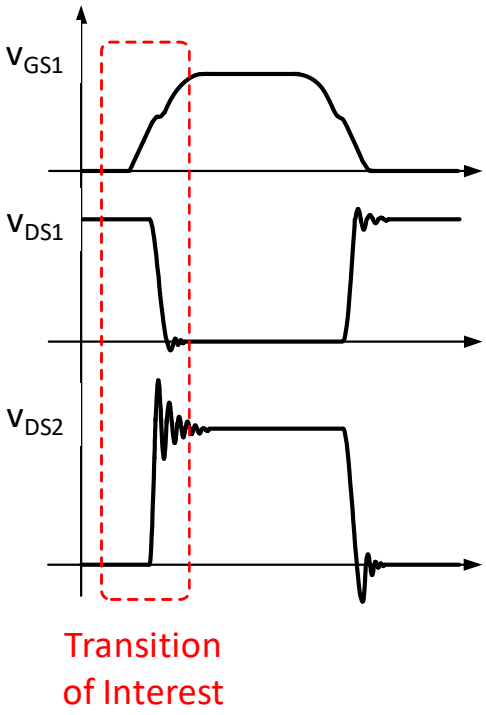

Figure 53 - Illustration of the transition which will be shaped during testing. Copied from Figure 4 originally presented in co-authored publication [89].

Figure 53 indicates the transition of interest during the first testing of the sub-nanosecond active gate driver on the low voltage testbed. This transition has the greatest potential to generate EMI as the currents that flow are only limited by parasitic circuit inductance. The low voltage testbed has an estimated 0.6 nH of main conduction loop inductance so this displacement current can be very high. This also means it is likely to excite any resonant circuits formed with other circuit parasitics and oscillate which in turn produce the EMI. The additional freewheeling diode, shown in Figure 52, could exacerbate this issue with additional capacitance and inductance in parallel to that of $Q2$.

In this configuration the drain-source voltage of $Q2$, v_{DS} , is the switch node voltage and so the voltage applied across the output terminals. Any oscillations that occur during the transition of interest in the waveform across $Q2$ can therefore be assumed to be present at the output. Frequency components of the oscillations above the self-resonant frequency of the filter inductor, where the inter-turn capacitance dominates the inductor behaviour, will pass to the filter capacitor and load. From here, the EMI can then be radiated from cables long enough to form antennae or conducted to other parts of the circuit.

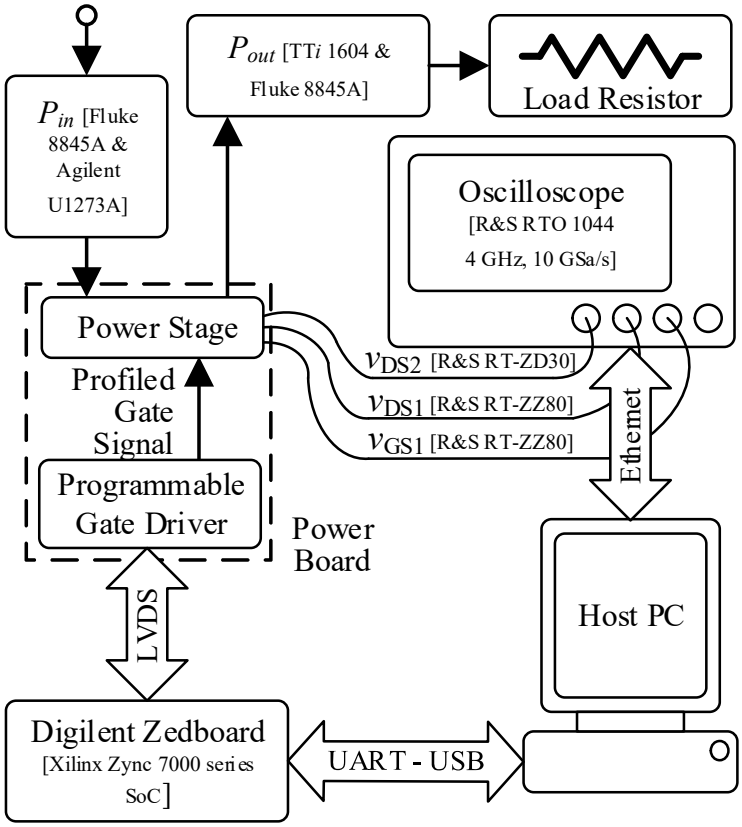

Figure 54 - Diagram of the experimental setup used in initial waveforms shaping with the Generation 1 gate driver. Copied from Figure 7 originally presented in co-authored publication [89].

The full experimental setup used in the work which this section draws from is shown in Figure 54. The low voltage nature of the circuit means the high bandwidth R&S RT ZZ-80 and R&S RT ZD-30 probes, discounted for the high-voltage GaN Systems GS66508P based testbed, are used to maximise measurement fidelity.

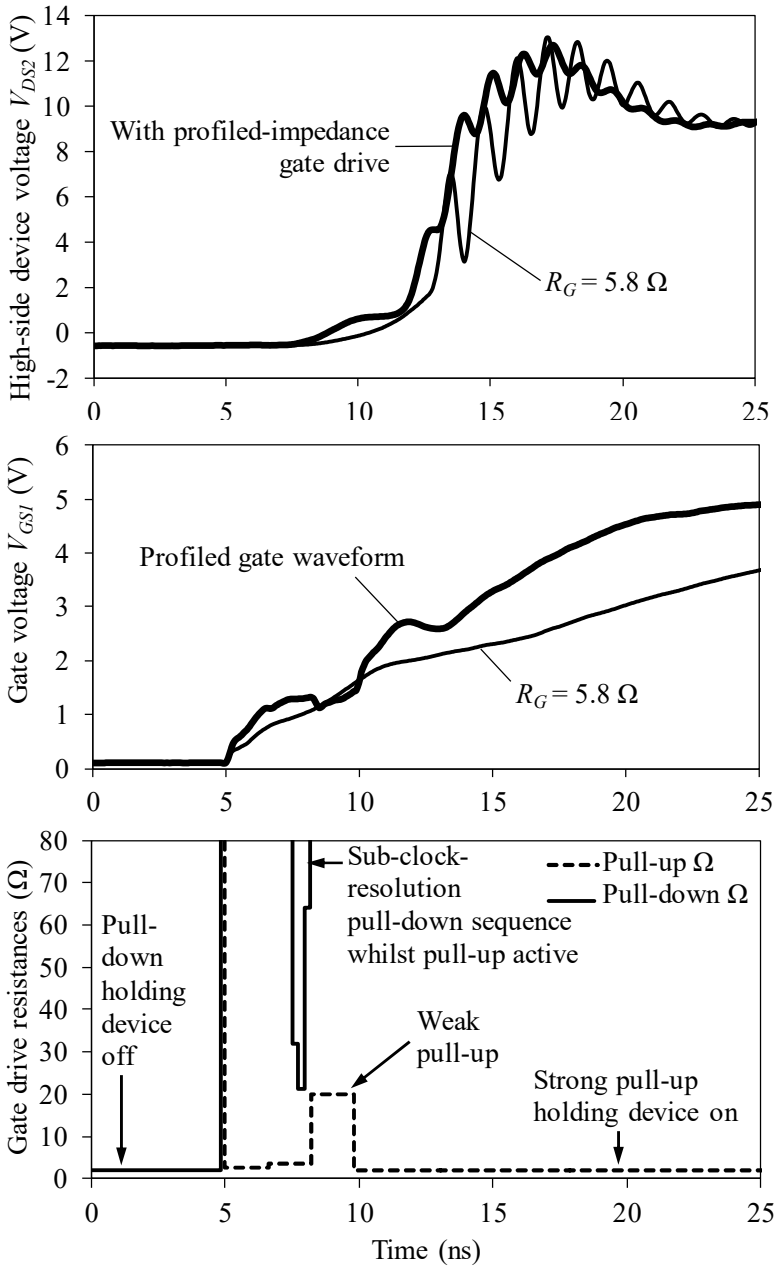

Figure 55 - V_{gs1} and the simple resistance sequence used to produce the gate waveform. Copied from Figure 8 originally presented in co-authored publication [89].

Figure 55 shows the a relatively simple sub-nanosecond resistance sequence (bottom), compared to the ability of the gate driver, used to produce the gate-source voltage waveform v_{GS1} (middle). For performance comparison the output of the sub-nanosecond gate driver configured to produce a nominal 5.8 Ω fixed gate resistance is also shown. This profiled gate waveform reaches fully enhances the power device by bringing its gate voltage to the maximum of 5 V in ~20 ns whereas the conventional gate driver strategy has only reached ~3.5 V in this time. Features of the resistance sequence can be directly related to the captured gate-source voltage where the increasing pull-up

resistance causes the voltage slew rate to decrease. A sub-nanosecond pull-down pulse is used to briefly bring the device below the threshold voltage, ~ 1.4 V, despite a pull-up main driver still being active before the gate-source voltage can rise again and continue towards 5 V.

Firstly, the 5.8 Ω fixed gate resistance seen to create significant high frequency (~ 800 MHz) oscillations in the v_{DS2} waveform which have been reduced with the profiled gate waveform. Secondly, the impact of the sub-nanosecond pull-down during turn-on can be seen in the v_{DS2} waveform at ~ 10 ns where the voltage across the device stops rising for ~ 1 ns. This suggests that v_{DS1} stopped falling at this time due to the dip below the threshold voltage v_{GS} caused by a sub-nanosecond gate driver fine driver pulse.

This is treated as evidence that, in this test bed using EPC EPC2015 GaN HEMT power devices, the impact of the sub-nanosecond gate driver outputting a high bandwidth gate drive waveform can be seen in the power circuit waveforms.

4.5. Conclusion

A down selection procedure based around a selection of high-performance probes and techniques useful for probing wide band gap circuits was conducted. The pros and cons for both voltage and current measurement methodologies was discussed along with their relative safety to the equipment involved.

Suitable voltage probes and interface techniques were chosen for the testbed developed in the first technical chapter and possible unavoidable limitations discussed. Despite offering ~500 MHz measurement bandwidth this could still obscure or at least effect the amplitude of spectral content above this frequency which would otherwise be of interest.

A floating current measurement technique based around an in-house field probe sensor was selected for measurement of the main conduction loop current waveforms. It's low insertion impedance and floating nature whilst also allowing ~300 MHz bandwidth with the sensor and probe combination used make it the best option of those explored. The assumptions surrounding the inference of device currents with the measurements available are discussed and assumed to be viable for the purposes of this work.

Using the probing methods discussed the process of de-skewing mixed probes to the tight time constraints required is detailed. This allows the output of the sub-nanosecond gate driver to be verified to determine if the device packaging presents a significant hinderance to the transmission of the desired high bandwidth waveforms.

Finally, a low voltage, ground referenced boost converter is used to demonstrate that simple sub-nanosecond resistance sequences can be used to influence the power waveforms of a GaN power devices.

4.6. Further Work & Limitations

In this chapter it is noted that the voltage probes selected could still have insufficient bandwidth for the potential waveforms. The probes selected also have the potential to significantly load the circuit under test in the case of the gate-source voltage measurement. Therefore, since higher bandwidth alternatives with smaller probe tip components are now available, an investigation how they compare to the chosen methods is prudent. It would give insight into the observation that ~500 MHz could be insufficient for the dynamic range of voltage waveforms likely to occur within a GaN power stage equipped with high bandwidth active gate drivers. For the work in this thesis no post processing of voltage probe data to compensate for probe response is conducted. This could be an effective way to extend the useful measurement range of the selected probing systems but would higher bandwidth probes to correlated compensated data against.

The current probing and measurement setup does not have a facility to measure the current in the gate conduction loop. It is directly indicative of the charge delivered to the gate irrespective of the parasitic elements in the loop. This means it could offer deeper insight and ease the development of resistance sequences used in active gate driving that is currently unavailable.

5. Improving 650 V GaN HEMT Switching Transients

5.1. Acknowledgement and Attribution

This chapter is based upon and adapted from the first author paper, “Shaping Switching Waveforms in a 650V GaN FET Bridge-Leg Using 6.7 GHz Active Gate Drivers” [87] originally presented at the 2017 IEEE Applied Power Electronics Conference and Exposition.

Section 3.4.3 is adapted from the aforementioned publication and the co-authored one, “Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns” [89]. This was originally presented at the 2016 IEEE Energy Conversion Congress and Exposition.

5.2. Aims

Wide band gap power devices have a broad spectrum of application within power electronics and outside it. Solid-state LiDAR has already benefitted from the application of GaN power devices and accompanying gate drivers. They have allowed for shorter pulses at high current to be generated with greater control over the pulse duration. These turn directly into increased resolution, increased maximum range and decreased minimum range.

The application of sub-nanosecond active gate driving in addition to GaN power devices could potentially extend these benefits even further. It could offer a better trade off between switching performance and speed without being limited to a single gate resistance and potentially allow even shorter pulses to be generated. In power electronics similar benefits exist, however, being able to reduce or influence the distribution of the EMI produced is a more promising problem active gate driving could allow to be addressed.

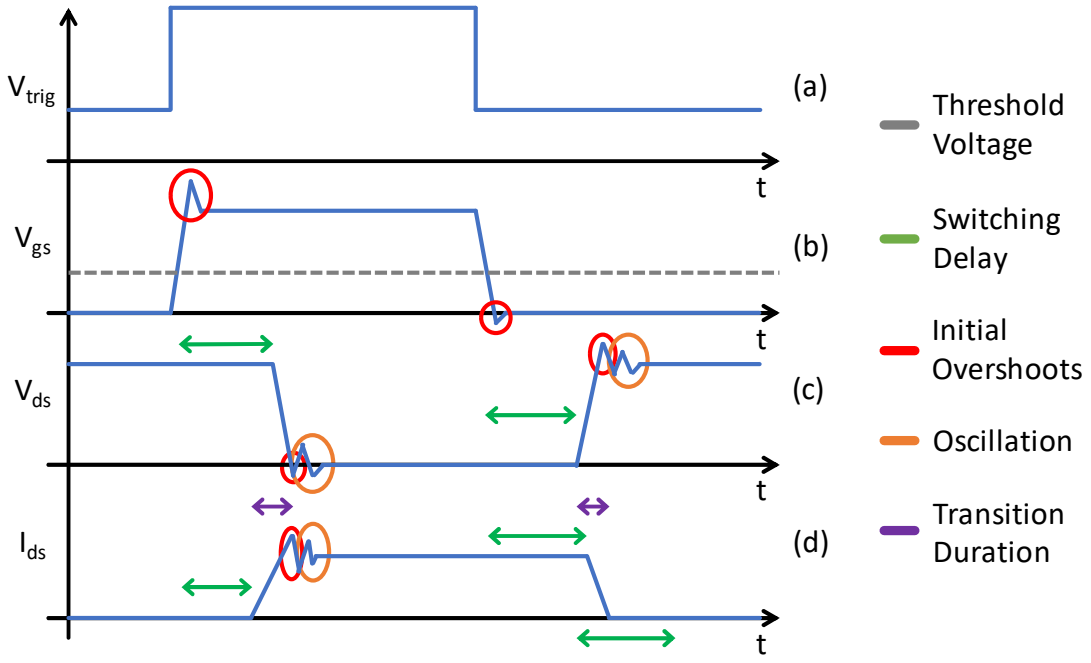

Figure 56 - Conceptual waveforms highlighting the non-ideal aspects of switching waveforms that active gate driving could address.

The highlighted areas of Figure 56 show some of the aspects of power waveforms which have been exacerbated by the increased switching speeds and slew rates offered by GaN HEMT power devices. Sub-nanosecond active gate driving could allow the better management of these areas which are detailed further in Table 11.

Table 11 - Further detail of the salient features highlighted in the conceptual waveforms of Figure 56.

Feature	Cause	Problem
Switching Delay (Figure 56.c & d)	• Power device gate capacitance • Gate drive impedance • Power circuit di/dt	• Limits the maximum switching frequency • Limits minimum safe deadtime
Transition Duration (Figure 56.c & d)	• High power device gate capacitance • Large gate drive resistance	• Direct positive relationship to switching loss
Initial Overshoots (Figure 56.b, c & d)	• Power circuit di/dt and dv/dt • Power circuit layout parasitics	• Increased switching loss • Increased device current and voltage stress • Increased device heating
Voltage and Current Oscillation (Figure 56.c & d)	• Power circuit di/dt and dv/dt • Power device parasitics • Power circuit component parasitics • Power circuit layout parasitics	• Increased switching loss • Increased device current and voltage stress • Increased EMI • Increased chance of crosstalk • Potential to cause positive feedback via C_{gd}

Focus will be on current oscillation in the active switch during turn-on and controlling it with sub-nanosecond active gate driving. It appears to be the easiest aspect of switching to impart a measurable effect upon, since it interacts with layout parasitics to contribute towards overshoot, undershoot and oscillations.

The tools used for performing and measuring sub-nanosecond low voltages have been proven, and this will now be scaled up to mains voltages and kilowatt scale switching transitions with 650 V GaN HEMTs. The aim is to ensure the power devices are placed under representative stresses during switching and respond accordingly to active gate driving.

The aims, therefore, are to address the following questions:

- Is active gate driving effective with GaN Systems GS66508P 650 V GaN HEMTs [10] operating at mains voltages for suppressing non-ideal switching features such as oscillation and overshoots?
- Is the degree of control offered over power circuit waveforms useful in different circuit configurations at fixed operating conditions (e.g. DC link voltage, load current and device temperature)? These will include buck and boost mode operation.
- Can the reductions in oscillation, overshoots and switching loss offered in the time domain be mapped onto corresponding measurable improvements in the frequency domain?

5.3. Introduction

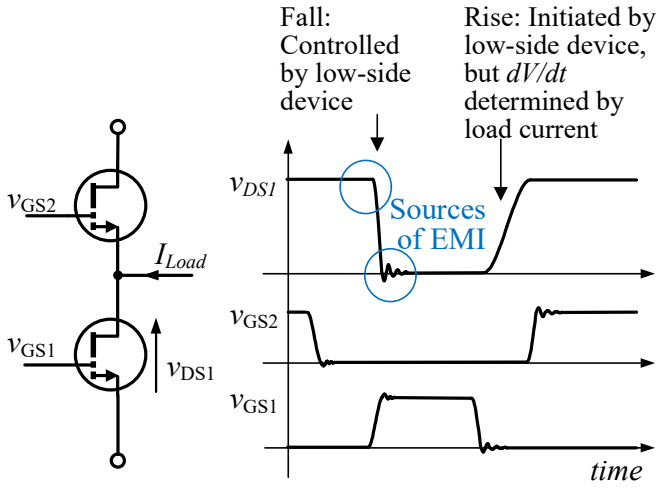

Figure 57 - Conceptual switch-node voltage transitions of a bridge-leg for current flowing into switch-node, with potential sources of EMI indicated, and the high- and low-side gate signals.

Observing the transient current in the bridge-leg helps with facilitating the development of active gate driving strategies. For example; at turn-on, the gate voltage (v_{GS1}) of the low-side control device directly influences this current. As the current in the low side device increases, and v_{DS1} falls, current diverts away from the synchronous device. This, in turn, is the cause of the rise in the drain-source voltage over the, high-side, synchronous device. This transient is conceptually illustrated in Figure 57 and highlights the voltage transient, with undesired oscillation, which controllability of the drain current transient could allow influence over.

As discussed previously; implementation of the sub-nanosecond active gate driver in a hard-switched 400 V DC link, 'mains voltage', bridge-leg presents additional challenges. Primarily that the driver for the high-side synchronous GaN HEMT needs to be level shifted with dv/dt exceeding 100 V/ns. However, it also means that both power device gates are now in control of the switch-node voltage; the control over each transient by a single driver/device is only partial; and the devices' respective roles depend on the polarity of the load current.

Figure 57 illustrates boost mode operation where the load current is flowing into the switch node. Here, the low-side power device controls the falling edge of the switch-node transient. Its rising edge, when the low-side device turns-off, is slower and determined by the load current charging the output capacitances. For current flowing out of the switch-node, buck mode operation, the situation is the reverse of this.

5.4. Test Setup and Experimental Procedure

5.4.1. Test Circuit

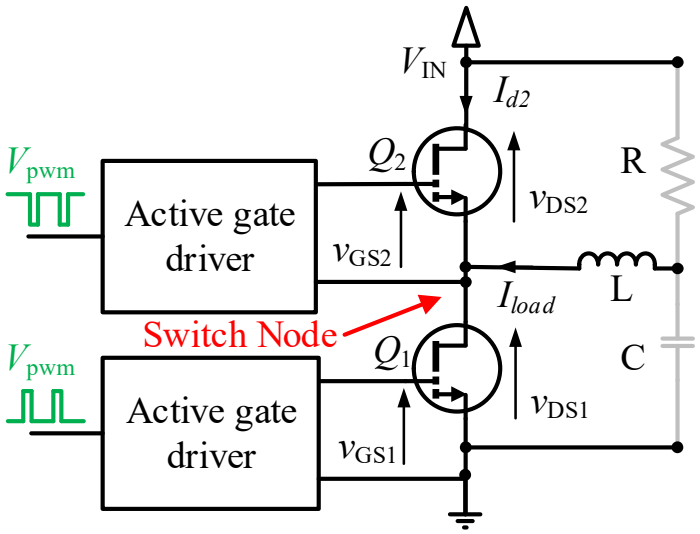

Figure 58 - Bridge leg arrangement and possible configurations of load components to cater for buck (current out of the switch node) or boost (current in to the switch node) mode and continuous or double-pulsed operation. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

The version of the testbed use for this work is like that detailed in Chapter 1, except that it uses an older version of the sub-nanosecond gate driver where the fine driver elements had more limited functionality.

Figure 58 shows a schematic of the experimental circuit, with the possible configurations of the load used for this chapter indicated. The circuit is designed to operate in both double-pulsed and continuous switching modes. In this chapter, double-pulse tests use purely inductive loads, and continuous switching use an R-L-C composite load. This layout is chosen because it can replicate the device interactions and hard-switched transitions in a synchronous boost converter (load current flows into the switch node) or buck converter (load current flows out of the switch node), depending on the configuration of the load.

For boost mode, the lower device in the bridge leg (Q_1) is the active switch and has its turn-on transition shaped by its associated gate driver. In this mode the active switch turn-off transition and both transitions of the synchronous switch (Q_2) are driven with a fixed drive strength. A load inductor alone is connected between the positive DC Link and the switch node so that the load current is always flowing into the switch node.

For the double-pulsed Buck mode of operation, Q_2 is now the active switch with its turn-on transition being shaped. As with the Boost mode configuration all other transitions occur with a fixed drive

strength. The load inductor is now connected between the switch node and the negative DC Link to ensure current always flows out of the switch node. For continuous operation an L-C filter using a different inductor and a capacitor to the negative DC link is employed, with a load resistor connected to the positive DC Link resulting in current always flowing into the switch node.

In all instances a dead-time of 100 ns was used to minimise the chance of shoot through caused by cross-talk or slow device switching whilst developing resistance sequences for the active gate driver. The inductor charge time was, at least, an order of magnitude larger than this and so the impact of a relatively long dead time period is considered negligible.

5.4.2. Test Setup

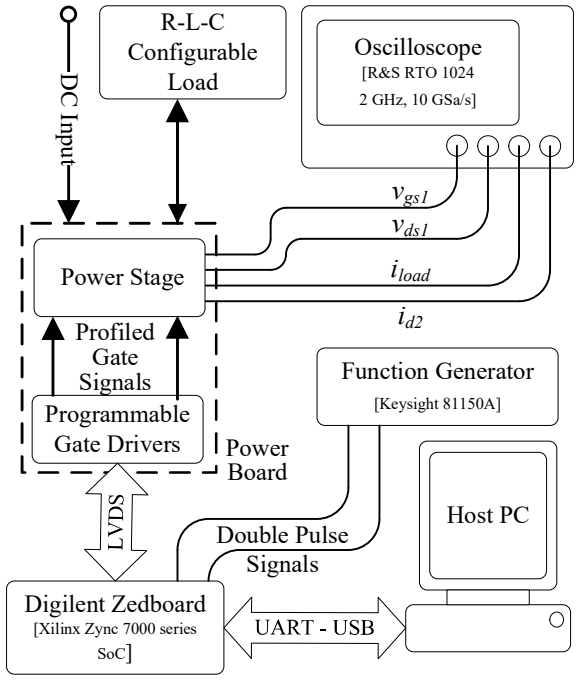

Figure 59 - Overview of the test system hardware layout and interconnects.

The configuration of the experimental hardware is illustrated in Figure 59. The Diligent Zedboard with a Xilinx Zynq 7000 series system-on-chip (SoC) discussed in Chapter 3 provides a remote-control interface to configure the gate drivers and program them. Prior to performing a double pulse or continuous test, the host computer sends the desired drive sequences to the Xilinx system, which in turn programs the gate drivers.

For a double-pulse experiment, the external Keysight 81150A function generator is configured with the desired double-pulse gate-driver control waveforms from MATLAB, and has its output passed through the Xilinx system to the gate drivers. For continuous switching tests, 100 kHz PWM signals are generated by a VHDL defined PWM generator block in the FPGA fabric of the Zynq SoC.

Experimental waveforms are captured and de-skewed on a Rhode & Schwarz RTO 1024 2 GHz 10 GSa/s oscilloscope. With the low-side as the active switch, data capture triggering occurs on the second rising edge of v_{GS1}. For the high-side as the active switch, the rising edge of v_{DS1} is used as neither v_{DS2} nor v_{GS} can be inspected directly.

As discussed in depth during the previous chapter; wideband floating high-voltage measurements and non-invasive high-bandwidth current measurements are problematic. Therefore, single ended ground-referenced voltage measurements are the primary data in this chapter. Voltages v_{DS1} and v_{GS1}, the low-side device drain-source and gate-source voltages, are measured with R&S RT-ZP10 10:1 500 MHz and PMK PHV 1000-RO 100:1 400 MHz passive voltage probes respectively.

In line with the discussion on probing arrangements in the previous chapter current information for both i_{D1} and i_{D2} is captured with a UoB differential Rogowski 'Infinity' field probe sensor [25] combined with another R&S RT ZP-10 voltage probe. This gives an insertion impedance of 0.2 nH at 1 GHz, and a bandwidth of ~300 MHz[9].

i_{D1} measurements are not taken directly. It is inferred from the measurement of the high-side device current. The charging of the high-side power device's output capacitance will be controlled by the low-side device's turn-on transition, as during turn-on it takes up load current from the high-side device. Therefore it is assumed the high-side device current will be representative of the low-sides devices current for the purposes of this chapter.

For continuous switching experiments, the oscilloscope is set to capture and average 8,192 consecutive waveforms to enhance the signal-to-noise ratio. The averaged data are transferred to the host PC for conversion into the frequency domain using MATLAB.

The main power board, shown in Figure 60 is of a similar but older design to the testbed developed in previous chapters. It contains two 2nd generation sub-nanosecond active gate drivers, and two early life cycle GaN Systems GS66508P 650 V 55 mΩ HEMTs [10]. The 2nd generation sub-nanosecond active gate drivers are functionally very similar to the 3rd generation described in Chapter 1. The salient differences are the sub-nanosecond time resolution is lower at 150 ps, instead of the 100 ps, and a limited number of the sub-nanosecond fine drivers function correctly.

[9] The figure is between 200 MHz and 300 MHz and mostly determined by the loading effect of the probe on the sensor

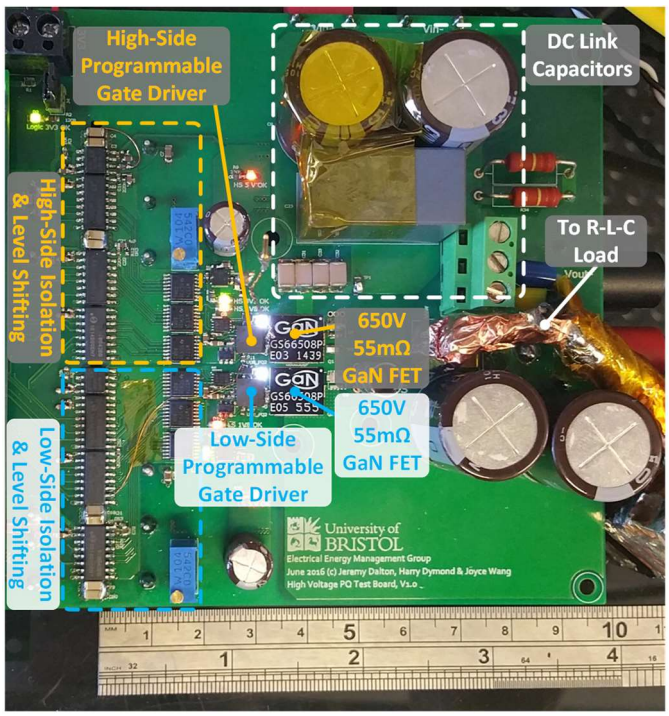

Figure 60 – The power board used in this chapter containing a bridge-leg of two GaN Systems GS66508P 650 V 55 mΩ HEMTs, each with its own programmable gate driver, isolated power supply, level shifting and isolation for control signals.

5.4.3. Switching Transitions Under Investigation and Shaping Strategy

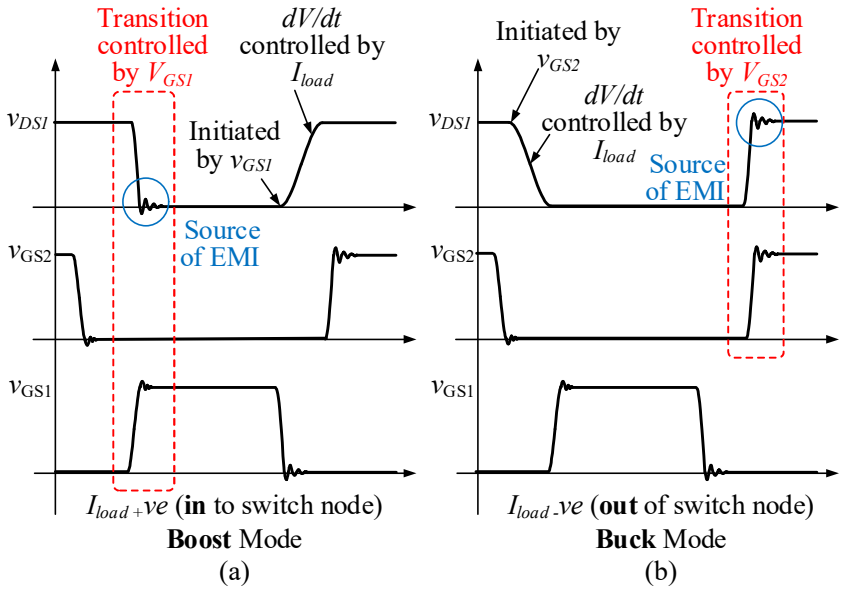

Figure 61 - The four switch-node voltage transitions which are possible in a bridge leg. Boost mode (a) where load current flows into the switch node. Buck mode (b) where load current flows out of the switch node.

In a bridge leg, there are four types of gate transitions per load current direction, as illustrated in Figure 61, where dead times have been exaggerated for clarity. With the current flow into the switch node and representing boost conversion, Figure 61.a, the low-side device is the control device. Its

turn-on transition controls the switching transient, however at turn-off, the load current determines its device voltage gradient dv_{DS}/dt as it charges the output capacitance of the device. Therefore, the turn-on transient (highlighted) is more controllable and used in Section 5.5 to demonstrate active gate driving. During buck conversion, with the load current flowing out of the switch node Figure 61.b, the high-side device is the control device. Turn-on (highlighted) is more controllable for the same reason, and is therefore demonstrated in Section 5.6.

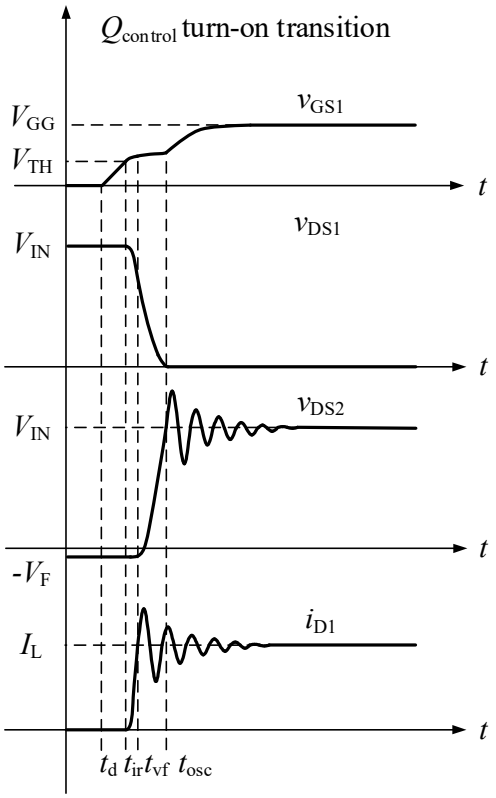

Figure 62 - Typical control switch turn-on waveforms for boost mode operation such as in Figure 61.a. Copied from Figure 5 originally presented in co-authored publication [89].

The objective of sub-nanosecond active gate driving, within the scope of this chapter, at the transition of interest is to reduce the drain current ringing resulting from the control device turning on. This transition, shown in Figure 62, can be divided into four consecutive stages: turn-on delay time t_d, current rise time t_{ir}, voltage fall time t_{vf} and oscillation time t_{osc}. In principle, a low gate driving resistance is needed for both the voltage fall and current rise intervals to reduce the switching loss. However, during the voltage fall, a low resistance increases the displacement current flowing through the synchronous device and thereby exacerbates oscillation in the final stage of the transition. This begins to illustrate the limitations of a constant strength driver in an analogous situation driving a GaN HEMT quickly.

In contrast, sub-nanosecond active gate driving allows the best resistance to be chosen for each of the phases with an aim to strike a better compromise between oscillation reduction and another chosen metric (e.g. switching loss). The gate driving strategy used for this work can described as follows.

- $\boldsymbol{t_d}$ Turn-on delay time: The control switch remains blocking in this stage and a low gate drive resistance is applied to pre-charge the gate and reduce turn-on delay time.
- $\boldsymbol{t_{ir}}$ Current rise time: A low gate resistance is employed initially to reduce the overlap loss. As the drain current slew rate determines the current overshoot and oscillation in the next stage, when drain current i_{D1} approaches load current I_L, the gate drive resistance is increased to reduce power circuit di/dt.
- $\boldsymbol{t_{vf}}$ Voltage fall time: A high gate resistance is applied at the beginning to reduce dv/dt and the resultant displacement current flowing through $Q_{control}$. In order not to greatly increase the overlap loss, the gate resistance is decreased when v_{DS1} approaches zero.
- $\boldsymbol{t_{osc}}$ Oscillation time: After v_{DS1} reaches steady-state, gate resistance should not affect the oscillation in i_{D1} and v_{DS2} and low gate resistance is applied to hold the device on.

The shaping strategy employed is similar to the strategy for low voltage GaN devices reported in the previous chapter and the paper it is based upon [89].

5.5. Double Pulsed Boost Operation

For double pulsed boost mode operation, where current is flowing in to the switch node, the circuit is configured with load component values for Figure 58 as shown in Table 12.

Table 12 - Circuit configuration for double-pulsed boost-mode operation.

Load Component	**Value**
R	Short Circuit
L	88 µH
C	Open Circuit

Figure 63 shows the circuit setup used given the test conditions outlined in Table 12.

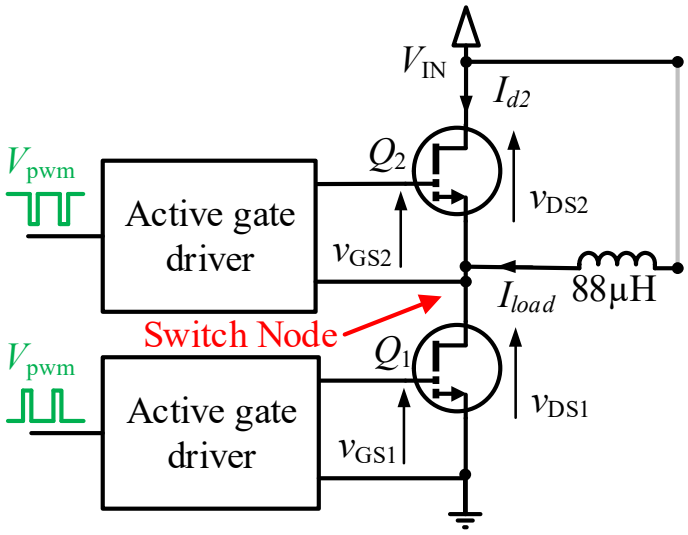

Figure 63 – Resultant circuit schematic, based on Figure 58, used for double pulsed boost mode experiments. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

Despite the lower DC link voltage of 200 Volts and the initial pulse charges the inductor current to 10 A to make the transitions representative of those within a kilowatt scale converter.

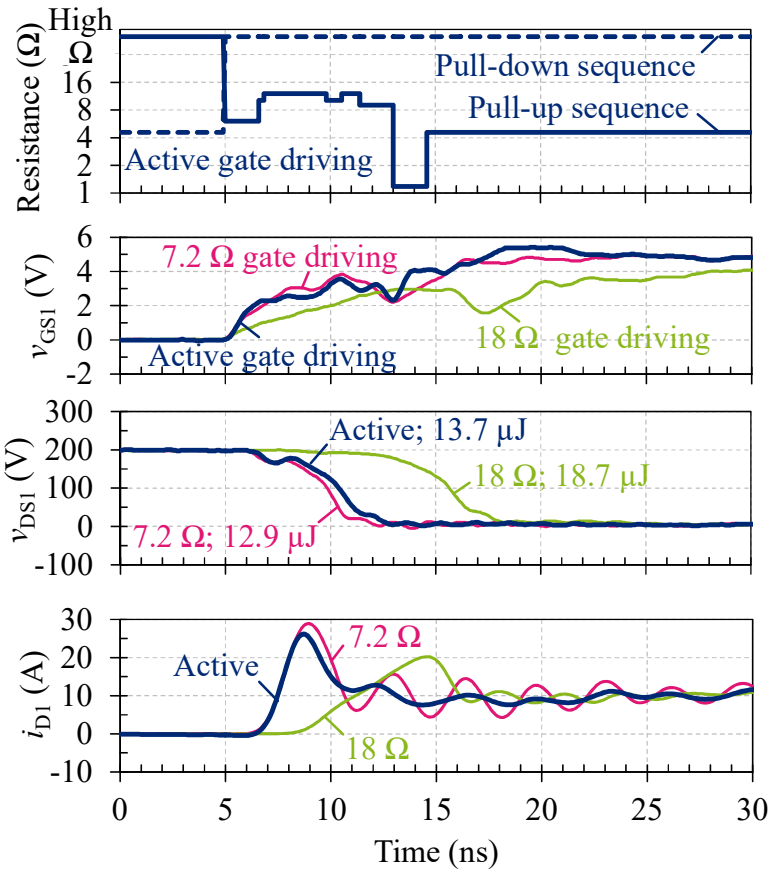

Figure 64 - Turn-on switching waveforms of the control device under boost-mode operation, with pseudo-constant-strength gate driving (7.2 Ω and 18 Ω), and active gate driving (gate resistance plots at top) aimed at reducing ringing in the drain current i_{D1} and switch-node voltage v_{DS} . The DC link voltage used was 200 V and nominal load current 10 A.

Figure 64 shows the measured turn-on switching waveforms of the control device for one active and two pseudo-constant-strength gate driving scenarios. The aim of the active gate driving sequence used here is to reduce current stress and current ringing in the bridge-leg.

Driving the control GaN HEMT with a fixed resistance of 7.2 Ω results in an 18.9 A current (i_{D1}) overshoot and ringing duration of more than 20 ns. Increasing the gate resistance to 18 Ω reduces the current overshoot to 10.2 A and damps the ringing by 73% but increases the switching loss and switching time by 45% and 50% respectively.

The control-device's turn-on switching loss for each scenario has been estimated using [98].

$$\mathrm{E_{SW}}_{on} = \int (i_{\mathrm{D1}} \times v_{\mathrm{DS1}})dt + \mathrm{E_{Coss}} \qquad (1)$$

and is provided in the line labels of the v_{DS1} graph in Figure 64. E_{Coss} is the energy that is stored in the output capacitance of the device in its off-state, and can be derived through simulation or using the datasheet [10]. For 200 V switching of GS66508P GaN devices, E_{Coss} is 2.9 µJ. This is a useful method

to assess the performance of similar time domain waveforms as it encapsulates the duration of the transition phases and the delays that position them relative to each other.

It is apparent that the resistance sequence used, shown in Figure 64, provides a reduction in current overshoot and ringing without a significant increase in switching loss. A low resistance is applied for the first 1.6 ns of the switching transition to reduce the turn-on delay time and the initial current rise time. A subsequent increase of the resistance suppresses i_{D1} overshoot and in-circuit ringing and maintains the current slew rate the same as 7.2 Ω gate drive strength. Momentary decreases in the resistance are used to optimize the switching waveforms and reduce the overlap loss. The final decrease of drive resistance provides a strong pull-up for the remaining on-state.

This strategy is seen to almost eliminate the ringing in the drain current and reduce its overshoot by 10%, however with no increase in switching time and an increase in switching loss by only 6%. This is a significantly better trade-off of current ringing against switching loss than the 18 Ω constant gate driving, which is one of the manufacturers recommended values for the turn-on gate resistance for this power device.

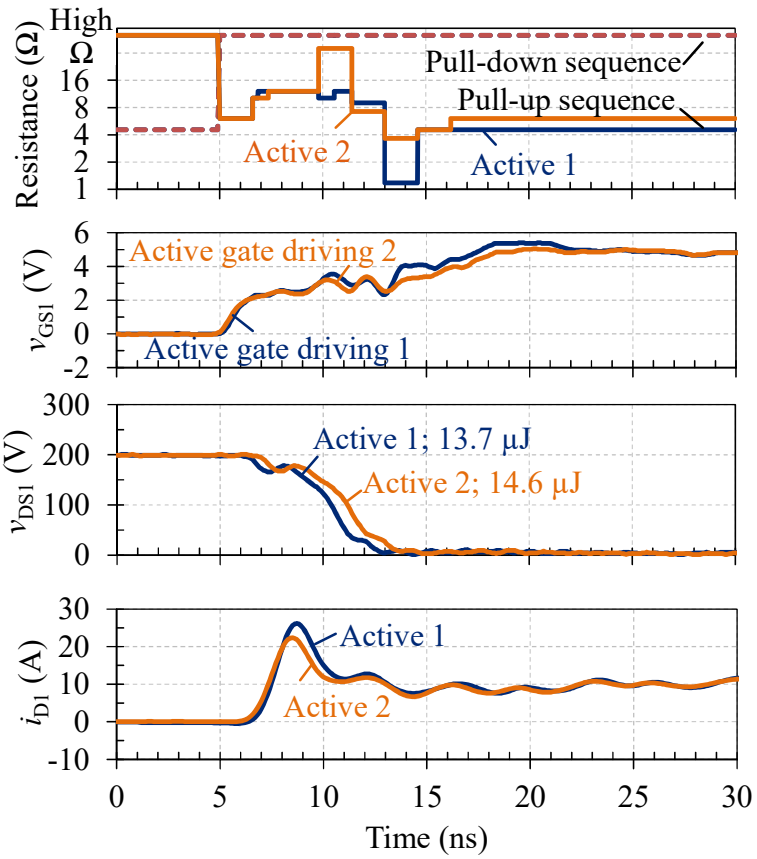

Figure 65 - Turn-on switching waveforms of the control device under boost conversion, with two active gate-driving scenarios (gate resistance sequence plots at top) aimed at reducing ringing in the drain current i_{D1} and switch-node voltage v_{DS1}.

Figure 65 compares another active gate driving sequence to that of Figure 64. The new sequence is seen to have the same damping effect on the drain current, but to further reduce the current overshoot to 12.4 A, and eliminate the overshoot in the gate-source voltage v_{GS1}. In exchange, the turn-on switching loss is increased by 7%. This illustrates a trade-off to be made when defining active gate driving resistance sequences.

5.6. Double Pulsed Buck Operation

For current flowing out of the switch-node, the circuit is configured with load component values as shown in Table 13. The DC link voltage remains at 200 V and the initial pulse charges the inductor current to 10 A as with boost-mode operation.

Table 13 - Circuit configuration for double-pulsed buck-mode operation.

Load Component	**Value**
R	Open Circuit
L	88 µH
C	Short Circuit

Figure 66 shows the circuit setup used given the test conditions outlined in Table 13.

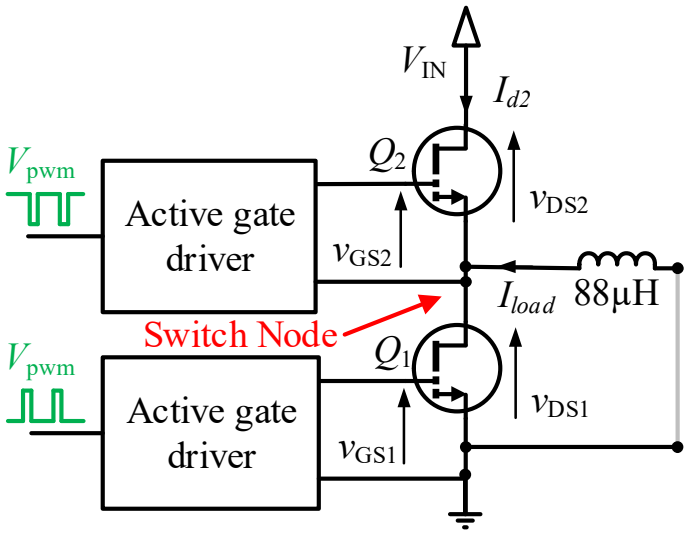

Figure 66 - Resultant circuit schematic, based on Figure 58, used for double pulsed buck mode experiments. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

A new gate resistance sequence is used for the high-side sub-nanosecond gate driver with the same goals as the sequence used for the boost mode operation. Re-using the same sequence from boost mode operation showed a partial improvement in switching waveform quality. Variation between gate drivers, power devices and component mounting mean that sequences must be optimised or developed again.

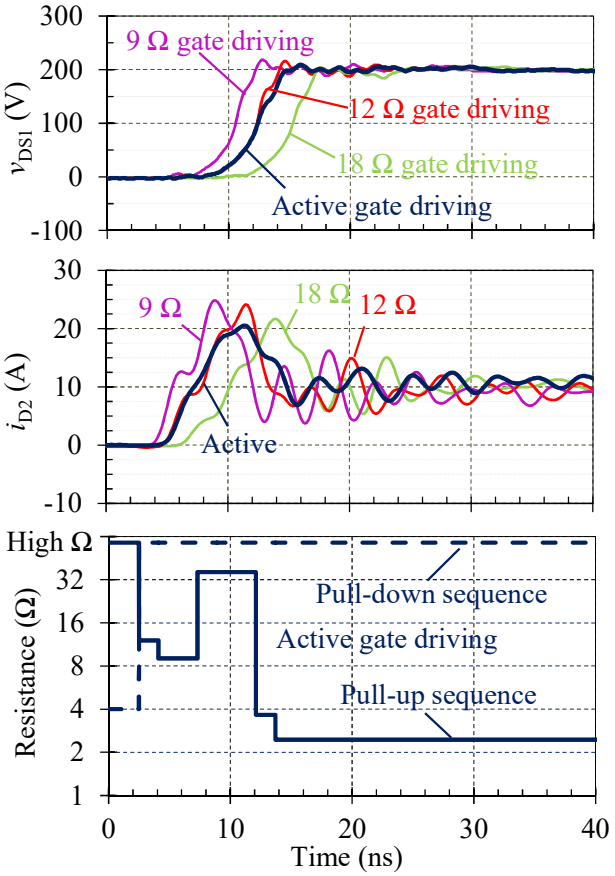

Figure 67 - Switching waveforms for the active switch current and synchronous switch voltage during active switch turn on under buck-mode operation. The gate resistance sequence used for the active switch under the active gate-driving scenario is shown at the bottom. Like boost mode operation; the DC link voltage used was 200 V and nominal load current 10 A.

Figure 67 shows an actively controlled transition compared against three transitions that use different pseudo-constant gate resistances (9 Ω, 12 Ω, and 18 Ω). As in the previous set of results, the current measurement represents the drain current of the control device taking up the load current out of the switch node. However, the control device is now the high-side device. The resistance sequence is based upon the 'Active 2' sequence used from Figure 65 with minor adjustments to account for the change in circuit configuration. v_{DS2} data isn't available due to the problems associated with capturing it detailed in Section 4.3.1.

The results show the following:

- **Switching delay.** As constant driver gate resistance increases and the time delays of i_{D2} and v_{DS} increase. In the active gate driving scenario the delay is identical to that of the constant 12 Ω scenario, as the active driving sequence is initially set to 12 Ω.
- **Current overshoot.** Compared with the three constant gate resistance scenarios, it is clear that the active resistance sequence used reduces the peak drain current i_{D2}.

- **Ringing and EMI.** Active gate driving delivers a smoother i_{D2} waveform which is monotonic during the current rise with lower oscillation once it has fallen back to the level of the load current. The damping of oscillation appears to be equivalent to that of the 18 Ω scenario. This smoother waveform will contain lower-magnitude high-frequency components and therefore can potentially generate less EMI [99], [100]. Active gate driving also reduces peak di/dt at the peak of i_{D2}thereby 'softening' it.

Considering these aspects, it can be concluded that sub-nanosecond active gate driving can control the profile of drain current i_{D2}, and provide a better trade-off, relative to fixed-resistance gate driving, between time delay, current overshoot, ringing and EMI.

5.7. Continuous Boost Operation

For continuous boost operation, the circuit shown in Figure 58 is configured with load component values as shown in Table 14.

Table 14 - Circuit configuration for continuous boost-mode operation.

Load Component	Value
R	5
L	44 µH
C	66 µF

Figure 68 shows the circuit setup used given the test conditions outlined in Table 13.

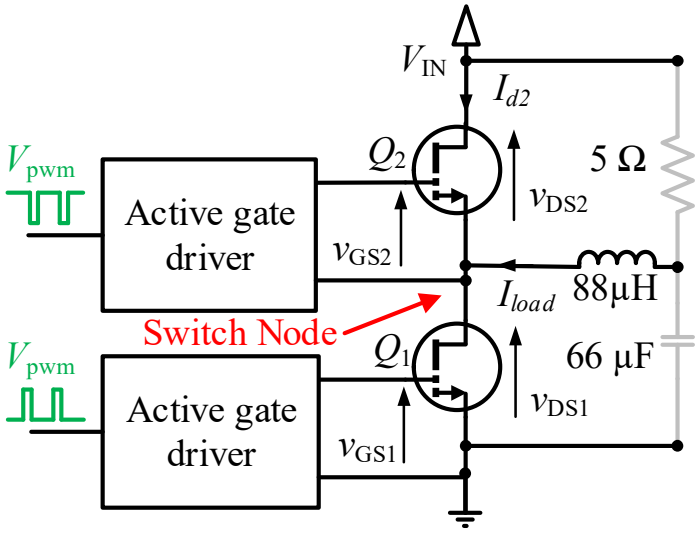

Figure 68 Resultant circuit schematic, based on Figure 58, used for continuous boost mode operation. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

The load components are actively cooled during testing to ensure the temperature is kept stable throughout the experiment so small variations in their value do not impact the results once averaging

has occurred. The DC link voltage is 100 V and the duty cycle of the 100 kHz PWM control signal is set to give 10 V at the output and a DC load current of 2 A.

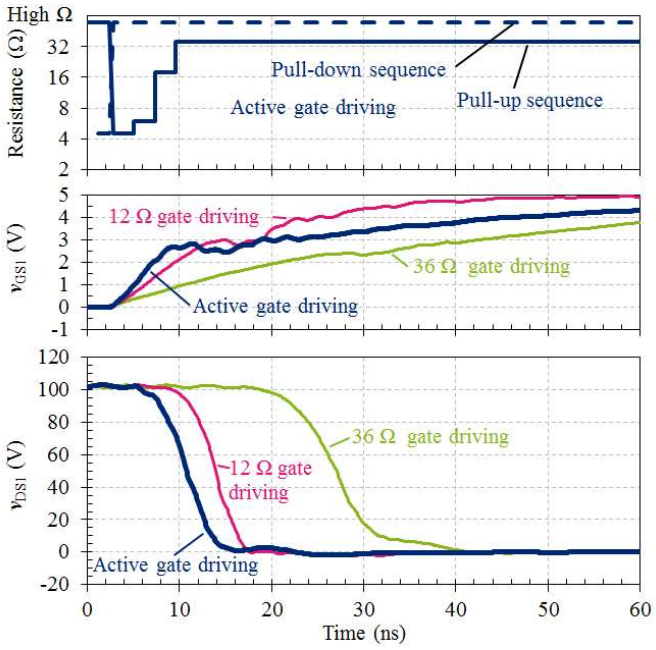

Figure 69 - Switch-node and low-side gate voltages, for fixed drive resistances of 12 Ω and 36 Ω, and for the active gate driving profile shown in the top graph. The active gate resistance used is seen to reduce switching delay. During continuous operation the DC link voltage and load current were further reduced to 100 V and 2 A respectively.

In this experiment, the aim is to turn on the control device as fast as when driven with a fixed 12 Ω gate resistance but to obtain EMI-generating spectral components that are typical of slower 36 Ω driving. i_{D1} and i_{D2} are not shown due the way in which data was captured, to be able to calculate the spectra desired averaging of time domain waveforms was carried out on the oscilloscope. To recover DC current information from the field probe current sensors integration of time domain waveforms is required which could not be done at the same time as averaging.

Figure 69 shows the measured switch-node voltage v_{DS1} and the low-side gate voltage v_{GS} under three different gate-drive scenarios: faster 12 Ω conventional driving, slower 36 Ω conventional driving, and active gate driving. The active driving scenario results in a 90 % to 10 % switch-node transition time of 5.6 ns, similar to the faster 12 Ω fixed drive. Delay is reduced by 3.3 ns with respect to the fast 36 Ω driving, due to the use of a lower initial gate-drive resistance to quickly ramp the device to its threshold voltage. Drive strength is then reduced during the transient in order to result in a less abrupt end to the switching transition.

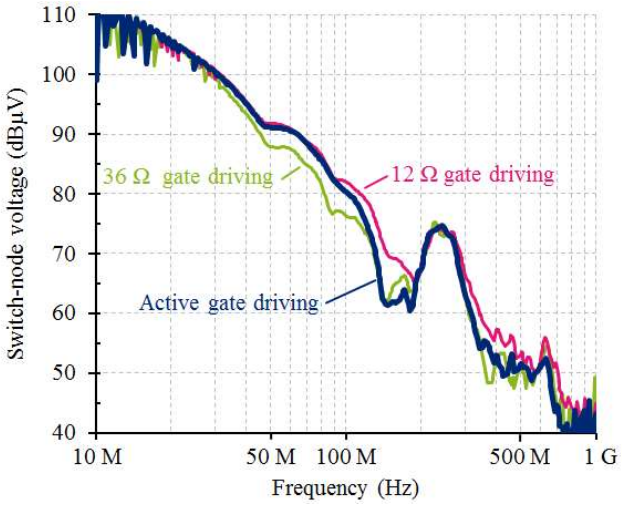

*Figure 70 - Spectral envelopes, **calculated** from measured time-domain data, of the switch-node voltage waveform for the three gate-driving methods of Figure 69.*

Figure 70 shows the influence of the different gate-drive scenarios on the spectrum of the switch-node voltage. The spectral envelopes are calculated from the time-domain data of a complete switching cycle and therefore include contributions from the low-to-high transition. The waveforms shown are intended to be representative of conducted and radiated emissions if they were measured. The assumption being that if the spectral content is present in the waveforms it has the potential to do either.

The nature of this edge is governed by the load current and is unaltered in all three scenarios. At frequencies above 125 MHz, the active gate driving results have switch-node, high-frequency content matching that achieved with slow 36 Ω driving, that is up to 9 dB lower than the 12 Ω case. Therefore, the calculated spectral content is like, and in places better than that given by using a large gate resistance value. Importantly this has been achieved without incurring higher switching losses normally associated with using a high gate resistance.

5.8. Continuous Buck Operation

Conducting a continuous switching buck mode experiment, aimed at improving the spectral content at across the control switch was not completed. In this configuration an insufficient number of measurements could be made.

Both the high-side, control switch, gate voltage, v_{GS2}, and drain-source voltage, v_{DS2}, are floating measurements which are not possible due to the limitations detailed in Section 4.3.1. i_{D1} and i_{D2}could not be measured due to the same integration and averaging problem from Section 5.7. This means that the quantities required for resistance sequence tuning and optimisation are both unavailable.

If an optimal resistance sequence could be found the remaining measurement, v_{DS} , the voltage over the synchronous switch could be used to calculate spectral envelopes and compare performance.

5.9. Conclusion

It has been shown that active gate driving of 650 V GaN HEMTs is effective for a number of objectives with the possibility to shape both the drain current and drain-source voltage of both power devices in a bridge leg in both buck- and boost-mode operation. It was found that using a 0.2 nH/300 MHz current sensor facilitated the improvement of both current and voltage waveforms in the bridge-leg. The sub-nanosecond timing capability of the active gate driver is shown to be essential to allowing waveforms to be shaped beneficially. The 150 ps resolution, and low driver impedance range (0.12 to 64 Ω) permit the optimisation of mains-voltage GaN HEMT waveforms without the integration of the driver and device into a single package.

When operated in double pulse mode at 200 V DC link and 10 A load current, a significant degree of control over the active-switch drain current and switch-node voltage is demonstrated, for both buck and boost mode operation. The current overshoot and ringing in the power waveforms due to circuit parasitics are actively reduced and the voltage oscillations in the DC link are damped. The timing of resistance sequences is shown to be critical to the success of active gate driving, thus justifying the 150 ps resolution of the driver.

Under continuous switching operation and at reduced ratings of 100 V and 2 A load current, the significant control of the switch node voltage and voltage spectra is also demonstrated. The switching delay is reduced, and parts of the spectrum are reduced by up to 9 dB equivalent to the effect of tripling the gate resistance but without any reduction in the overall switching speed.

5.10. Further Work & Limitations

While differences and effects are visible in the waveforms as presented, there is likely much higher frequency content that is not or has its amplitude skewed due to probe bandwidth limitations. The work reported in this chapter could also have been limited by the functionality of the driver generation since work with the 3rd generation has shown even greater time resolution to be useful.

Despite being multi-hundred-watt-scale transitions, it would be more useful if it had been conducted with a 400 V DC link to stress the devices properly as designed. This would ensure the high dv/dt and di/dt possible with such a bridge leg is reached. The digital isolators used in this version of the test bed were the limiting factor in this case as they could not withstand high slew rates.

Broadly, as load goes up then the EMI generated by a converter will too. Therefore, the continuous switching load current should be higher ideally the 2 A used is quite low for 30 A nominal devices. 10 – 15 A would be more appropriate but would require a layout comprising active cooling for the power devices, which this PCB doesn't allow.

The calculated spectral content of waveforms is a good indicator of the effectiveness of high bandwidth active gate driving. However, they do not consider the impact of the PCB layout and wider test bed arrangement on radiated and conducted emissions. A useful piece of further work would be to conduct far field electromagnetic radiation measurements. This type of measurement would be more representative of the benefits offered by high bandwidth active gate driving in application.

Switching losses given in this chapter do not include the energy contained in the ringing which can continue long after the power device has switched. Further analysis could be completed including this to determine if the benefit of active gate driving is greater than concluded.

6. Adapting Active Gate Driving Sequences to Changing Operating Point

6.1. Acknowledgement and Attribution

This chapter is based upon and adapted from the first author paper, “Stretching in Time of GaN Active Gate Driving Profiles to Adapt to Changing Load Current” [88] originally presented at the 2018 IEEE Energy Conversion Congress and Exposition.

6.2. Aims

The proven capability to impact both switching waveforms and spectral content of waveforms directly translates into benefits for power electronics designers. It has, however, only been done with a fixed set of operating conditions. In a power converter, such as an inverter, this is not the case and several operating parameters will impact the effectiveness of an optimised sub-nanosecond resistance sequence such as:

- **DC Link Voltage –** This should be relatively stable at switching frequency time scales while a converter is operating but will contribute towards the peak di/dt and dv/dt observable with the main conduction loop.
- **Load Current –** This has one of the biggest effects of device performance during switching as it impacts the charging rate of output capacitance and charge velocity in the depletion layer for the control device during turn-off. The load current doesn’t directly impact the turn-on of the control device but if a fast transition to a high load current is required to minimise switching losses then, indirectly, it has a significant impact. In short; for a given gate drive condition the power device will appear to switch faster with higher peak di/dt at high current and slower with lower peak di/dt at low current.
- **Power Device & Gate Driver Temperature –** The temperature of both components will impact nominal resistance in the gate conduction loop and in turn, the effective resistance sequence being used to control the power device.
- **Power Device & Gate Driver Health –** Transient and fault conditions within the converter have the potential to damage both components over time and they will age regardless with their performance degrading accordingly [23], [58], [59], [101], [102].
- **Component to PCB Interface Health –** The PCB scale packages of emerging wide band gap power devices pose new complications to initial mounting and interconnection health over

time [8]. High current densities and effects such as dendrite growth both contribute to contact performance degrading over time which could impact the effectiveness of a resistance sequence.

This chapter will focus on the impact of load current on the effectiveness of the previously proven benefits available.

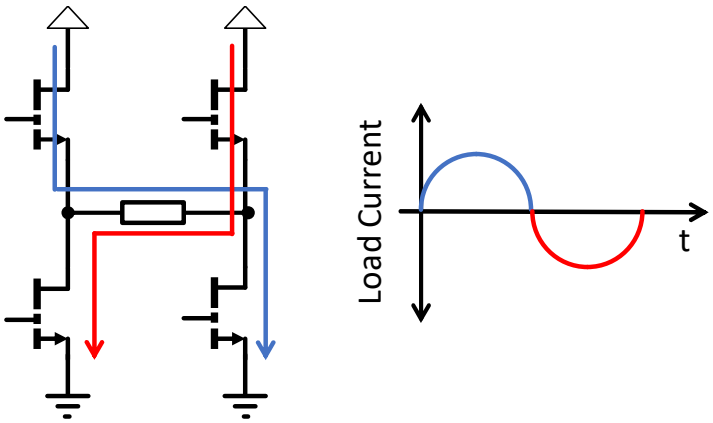

Figure 71 - Illustration of an H-bridge inverter to show the continuous change in output current magnitude and direction for a sinusoidal output.

In the given case of an inverter, this quantity is continuously changing during normal operation as shown in Figure 71, and even in DC-DC converters load current transitions will occur. Therefore, it is deemed the most interesting quantity to investigate the effect of as it presents a big barrier to the implementation of active gate driving outside of research. Focus will be on the turn-on transition of the control device, as with the previous chapter, due to this transition being controlled primarily the power device turning on rather than the amplitude of the load current.

In summary this chapter builds upon the proven high voltage GaN device controllability of the previous chapter to explore the following questions:

- To what degree does the load current, which impacts the speed of physical processes inside GaN HEMTs, impact the effectiveness of a fixed sub-nanosecond active gate driving resistance sequence?
- Can any effectiveness lost due to a change in load current be re-gained by stretching or compressing the fixed resistance sequence in time?
- To what extent can the performance of the fixed resistance sequence at it's designed load current and driver clock frequency be regained?

6.3. Introduction

Active gate driving with sub-nanosecond resistance sequences has been shown to reduce EMI, overshoot, and switching loss. Active gate drivers with the ability to profile at a 150 ps time resolution have opened up the possibility of actively driving mains voltage GaN devices. However, these drivers have only been demonstrated with pre-programmed gate profiles that have been optimized at certain operating conditions, whereas converters typically operate in a range of conditions.

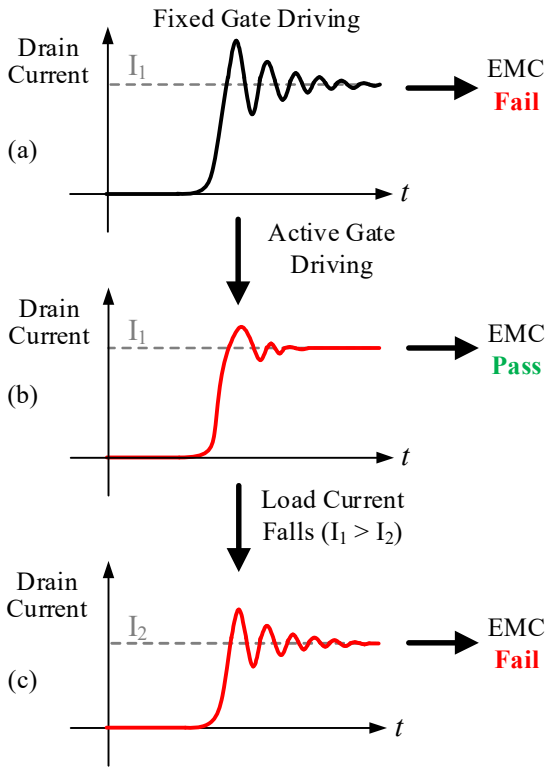

Figure 72 - Illustration of a typical conventional gate drive turn-on current pulse (a) compared to the benefit offered by open-loop active gate driving (b), and the impact operating point can have on power device drain current in the actively driven case.

Active gate drivers allow switching waveforms of a power electronic converter, e.g. the drain current of a power device, to be "shaped" via the gate signal during the switching transition. For example, turn-on drain current ringing under conventional gate driving, as illustrated in Figure 72.a., can be transformed into a waveform with the same switching speed but with less ringing, Figure 72.b., and therefore less EMI.

The gate signal profile can be set in advance of converter operation (open loop) or sensing mechanisms can be used in a closed loop feedback or adaptive configuration to allow the circuit to react continuously to variations in operating parameters, such as load current. Closed-loop and adaptive active gate driving is well documented for Silicon (Si) power devices. However, due to the

short switching time and high slew rates of a GaN HEMT power device, during kilowatt scale power circuit switching transitions, closed-loop or adaptive active gate driving [64] is more challenging.

Active gate driving of GaN HEMTs can be categorised by the capabilities of the driver. Single-step closed-loop drivers for GaN have been demonstrated that are able to help combat EMI [103], [104]. Drivers capable of three or more steps have also been shown to be capable of further reducing EMI and targeting overshoot in switching waveforms [105], [106]. A profiling flexibility with even greater time resolution during the switching transition has been shown to enable the reduction of crosstalk and oscillations [90], in addition to overshoot and EMI [87], [89], [90], [92]. However, reported drivers with this very high time resolution, are currently open-loop with pre-programmed gate driving profiles. These profiles are optimised under specific operation conditions (e.g. fixed current, temperature, and DC voltage levels) and therefore they may not be optimal or even safe at other operating points, as illustrated in Figure 72(c).

Therefore, this open-loop, high-resolution category of drivers under changing load current are to be investigated. The aim is to find out when the effect of active gate profiles become measurably degraded and need to be updated, and whether there are computationally viable means of doing so. That is, are there any methods significantly faster than designing a new profile for re-gaining performance from a known good profile. This is a critical step towards being able to deploy active gate driving in real-world GaN converters that operate effectively under varying operating conditions.

Using established methodology and equipment a fixed active gate driving resistance sequence is developed to minimise drain current ringing and spectral content. The gate profiles in a 650 V GaN HEMT bridge‑leg operating from a 400 V DC-link are optimized to minimize current ringing at turn-on for a given load current. Then, the load current is varied, showing that the gate signal profile remains close to optimal for ±20% changes in current. Also, over a larger range of at least ±35%, the profiled waveform performs better than a non-profiled gate waveform. It is then demonstrated that by slightly increasing the driver's internal clock frequency with decreasing load current, the profile is re-optimized for new load currents.

6.4. Method and Test Setup

6.4.1. Method

Figure 73 shows the method used in this work to investigate sensitivity to changes in nominal load current. Trends are determined based upon the ringing introduced by the imposed changes to the operating point.

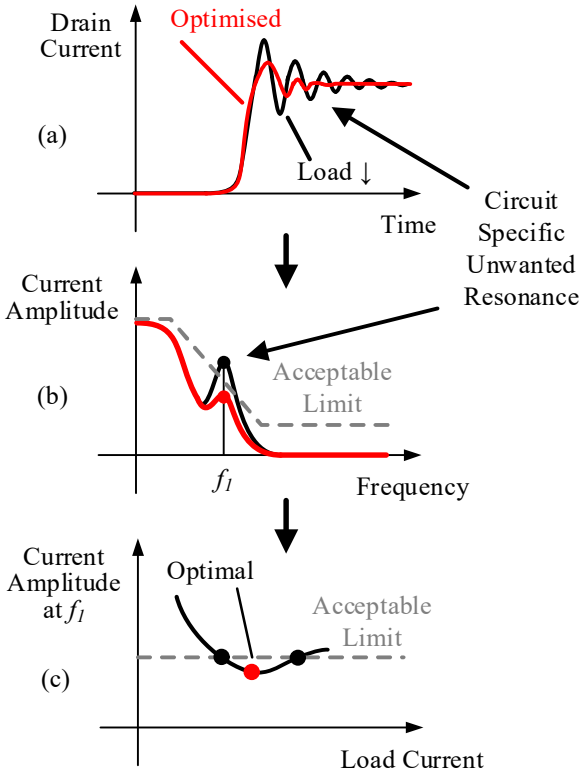

Figure 73 - Example drain-current switching waveforms in the time (a) and frequency (b) domains. Open-loop active driving is able to reduce the ringing in (a) to within a pre-defined acceptable limit in the frequency domain (b). Load current variations in (c), and the resulting change in GaN HEMT switching characteristic, cause ringing to once again breach and acceptable level.

The GaN HEMT bridge leg, comprising a pair of GaN Systems GS66508P 650 V GaN HEMTs, used for this work is configured as shown in Figure 74. It is configured for boost mode operation where load current flows into the switch node. The bridge leg is driven with double-pulse waveforms according to the desired nominal load current flowing in the load inductor, L_o (300 µH). The DC Link, V_{IN}, is maintained at 400 V and switching was optimised at a load current, i_L, of 10 A, about which it is then varied.

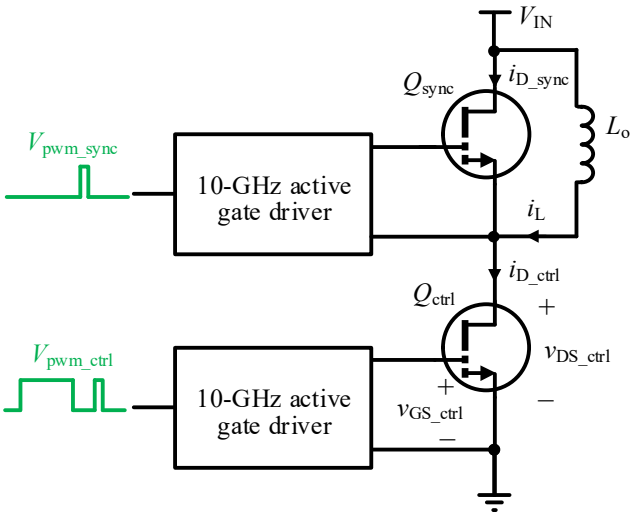

Figure 74 - Diagram of the power circuit configuration used for this work. Anti-parallel diodes are omitted due to the diode like behaviour inherent to GaN HEMTs. See section 1.2 for more details.

Both power devices are driven with active gate drivers (in open loop mode) although the driver for the upper device, Q_{sync}, is not performing any profiling and the output of the driver is set to a constant drive strength for turn-on and turn-off transients (i.e. it is acting as a conventional driver).

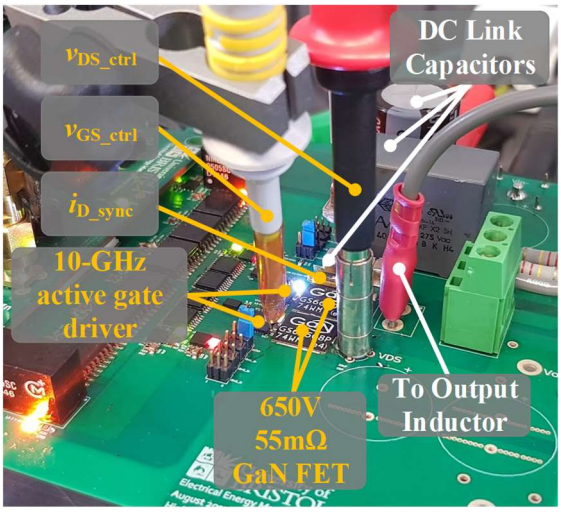

Figure 75 - Photograph of power circuit used for this work indicating major components and probe locations.

Figure 75 illustrates the major components of the experimental hardware as shown in Figure 74 and their relative proximity to each other. This compact layout is critical for realising the high performance offered by GaN power devices and allowing sub-ns active gate profiling to be as effective as possible.

6.4.2. Test Setup

Figure 76 shows a schematic of the experimental setup detailing specific instrumentation and equipment used where appropriate. The power circuit current and voltage waveforms are captured by a Rhode & Schwarz RTO1044 4 GHz 10 GSa/s oscilloscope. The chosen operating mode allows for

voltage measurements to be ground-referenced, as capturing floating reference measurements of high voltages at the bandwidth required is particularly challenging. As indicated in Figure 76, the gate-source voltage, v_{GS_ctrl}, of the low side GaN HEMT, Q_{ctrl}, is probed directly by a Rhode and Schwarz RT-ZP10 10:1 500 MHz probe with spring tips for both signal and ground directly probing the gate and source terminals. The drain-source voltage, v_{DS_ctrl}, is measured by a PMK HV1000 100:1 400 MHz passive voltage probe connecting through a coaxial PCB-mounted probe adapter to the drain and source terminals of the low-side device. These connection techniques ensure that any loop inductance, loading effects, and noise paths introduced are minimized, which is essential for making high bandwidth measurements.

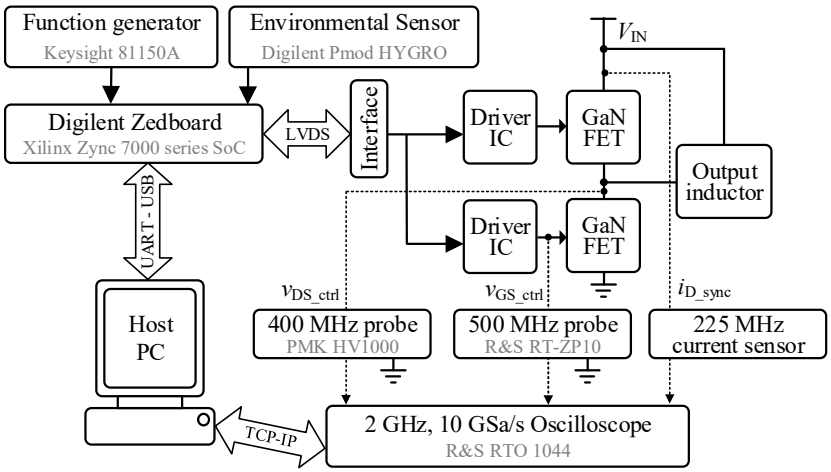

Figure 76 - Top level configuration diagram of the experimental hardware and support equipment.

The drain current of the high-side GaN HEMT, iD_{sync}, is measured by a non-invasive and floating current sensor with a bandwidth of 225 MHz. The load inductor capacitance has been measured to be small and so the load current during a switching transient is assumed to be constant. This allows the low-side device current, iD_{ctrl}, to be inferred and introduces low insertion inductance (0.2 nH); a feature that is particularly important so that it has the least influence on the inductance-sensitive GaN switching transient. The GaN Systems GS66508P power devices possess a kelvin source connection meaning the gate loop current is already excluded from the measurement and doesn't have to be accounted for in post-processing.

The raw data for each test is a single-shot capture of a double-pulse event long after the dc-link has been energised to prevent the effect of current collapse impacting the results. After a test sequence is complete, an automated MATLAB script on the host computer collects the captured data from the oscilloscope, together with ambient temperature and humidity data from the Xilinx system shown in Figure 75. Results for all data sets were also collected on the same day once equipment had reached stable operating temperatures, to minimise the impact of the memory effect [107] that enhancement

mode GaN HEMTs display, and to minimise the small day-to-day variation in the asynchronous timing circuits of the active gate driver.

6.5. Optimised Gate Driving at a Single Load Point

For all results presented, the same active driving profile was used. The optimisation goal of this profile is to reduce the current oscillations and overshoot peak, whilst minimising transition time, at a nominal load current of 9 A. The profile is shown in Figure 77, and its effect on the power-circuit current is shown in Figure 78.

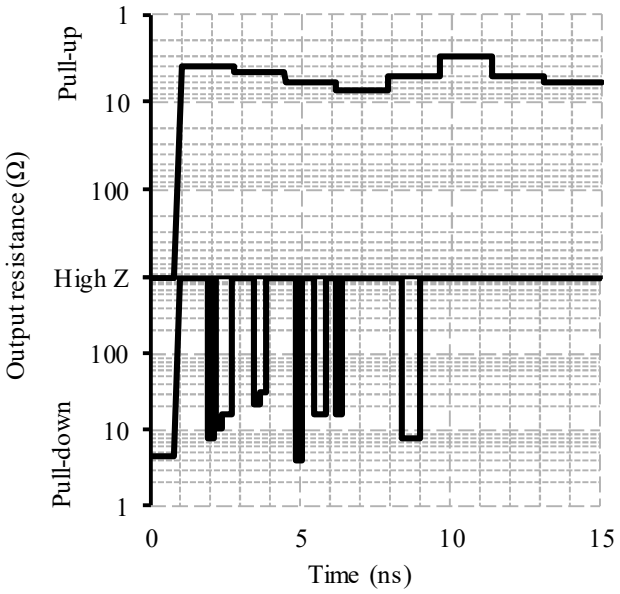

Figure 77 - The gate impedance profile used throughout this chapter. The thicker lines represent the application of very short time duration 'tweaks' where the thickness of the line obfuscates the area inside the line.

The profile employs a generally strong pull-up, as is expected of a turn-on transition, varying between 9 Ω and 3 Ω with an average of ~6 Ω across the transition. The very high time resolution of the driver used in this work is then used to apply 100-400 ps pull-down 'tweaks' at hand-tuned points in time to eliminate the source of ringing in the power waveforms, by preventing the aspects of the transition which excite circuit-specific resonances in the power circuit from being generated.

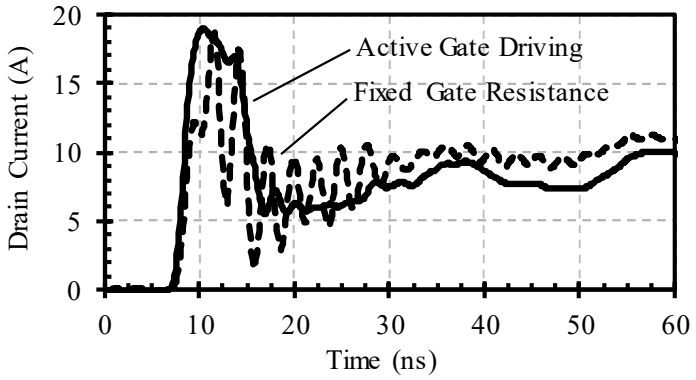

Figure 78 - A comparison between the active gate driving profile used in this work and a comparable fixed gate resistance.

Figure 78 shows the improvement to the Q_{ctrl} drain current surge and current oscillation that the active gate driving profile used in this work delivers. With the steady-state load current fixed at 9 A, the lowest fixed gate resistance capable of less than 20 A peak current overshoot is chosen, and its drain current transition shown for comparison.

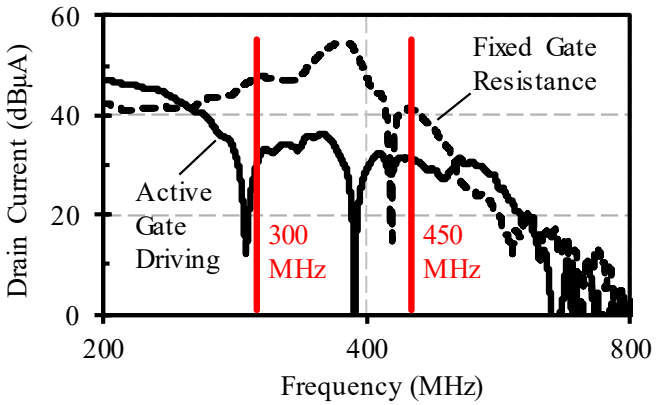

Figure 79 - The calculated spectra of the drain current waveforms shown in Figure 78.

The use of high time-resolution active gate driving profile removes a significant amount of high frequency content in the initial pulse by broadening the peak and eliminating most of the ringing superimposed upon the pulse, whilst offering a slightly higher peak $di\ /\ dt$. The active driving profile then almost eliminates continued high frequency (~400 MHz) ringing after the initial current pulse.

This suggests the presence of this undesirable oscillation could be used as a metric by which to judge the effectiveness of the active gate driving profile.

6.6. Impact of Changing Load Current

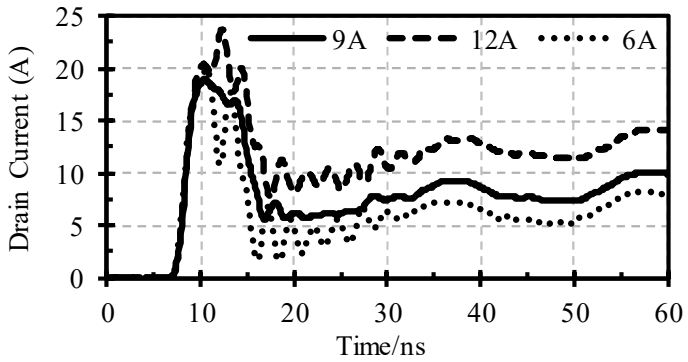

Figure 80 - Drain current switching waveforms for open-loop active gate driving at various load currents, where the gate profile has been optimised for the 9 A case.

Figure 80 shows in the time domain the impact of changing the steady-state current away from point at which has been optimised. It is varied around 9 A by ±3 A. Both 6 A and 12 A traces show the return of the ~400 MHz oscillation seen in Figure 79. Lowering the steady-state current has resulted in larger peak-peak oscillations in the drain current waveform due to 'de-tuning' of the optimised gate resistance sequence.

In both cases, the active gate driving profile has become less effective, but decreasing the steady-state current has had a more pronounced effect. It is therefore expected that the frequency spectra of the three waveforms would reflect this and allow the relative impact of a change in steady-state current to be quantified.

The load current range chosen comes about because of several factors. The nominal maximum drain current for the GS66508P GaN HEMTs in use is 30 A [10] therefore a nominal value, 9 A, that keeps the peak current overshoot, ~20 A, below this was required for both conventional and active gate driving. To be able to generate a range of load currents a values a nominal level above this, 12 A, had to also be safe reaching a maximum overshoot of ~24 A. ±3 A was then chosen as a significant deviation away from 9 A, ~±30%, where any difference caused by the load change would be obvious. Additionally, it made provision for a second overlapping load range sweep to be performed at lower current if one were needed.

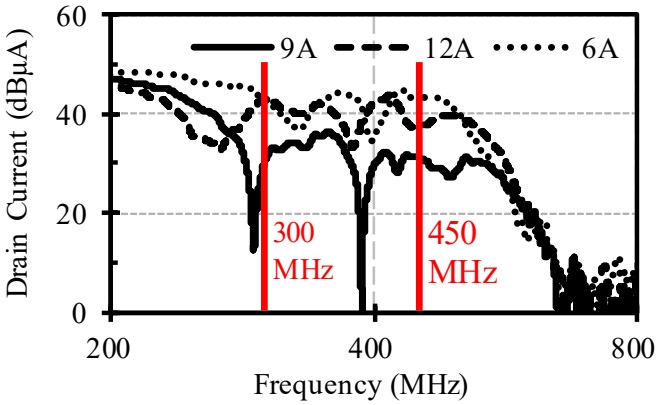

Figure 81 - Calculated spectra of the current switching waveform for 6 A, 9 A and 12 A steady-state loads highlighting the frequency band where this work concentrates (around 400 MHz).

The time-domain data used to produce Figure 80, which is not a continuous pulse train, is used to calculate the spectral content by padding the data to an effective 100 kHz switching frequency and applying a Tukey (tapered cosine) window with taper factor of 0.25 before performing an FFT.

It is shown that between 300 MHz and 450 MHz, there is significant variation between the three envelopes. In this highlighted 150 MHz band, the 6 A and 12 A traces have an increase of approximately 25%, when the deep minima in the 9 A spectrum is excluded. The 6 A spectrum however has higher peaks in this band and shallower lows suggesting it overall has more spectral content contained in this band. This reinforces the qualitative observation from Figure 80 that a decrease in steady-state current has more of an impact than an increase does.

This increase to either side of an optimal point indicates that a U-shaped curve-of-effectiveness exists about the point at which an active gate driving profile is optimised, as illustrated in Figure 82.

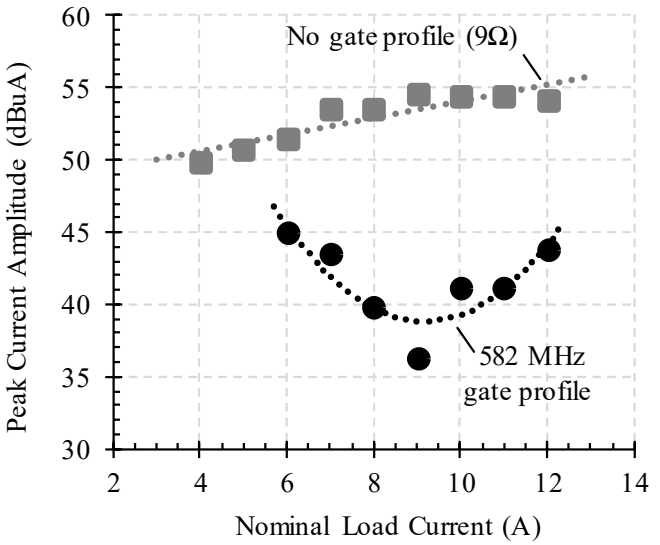

Figure 82 - Peak current magnitude between 300 MHz and 450 MHz plotted against steady state load current.9Ω is used for comparison as it produces similar drain current overshoot and peak $di\ /\ dt$ as seen in Figure 78.

6.7. Time Scaling Concept

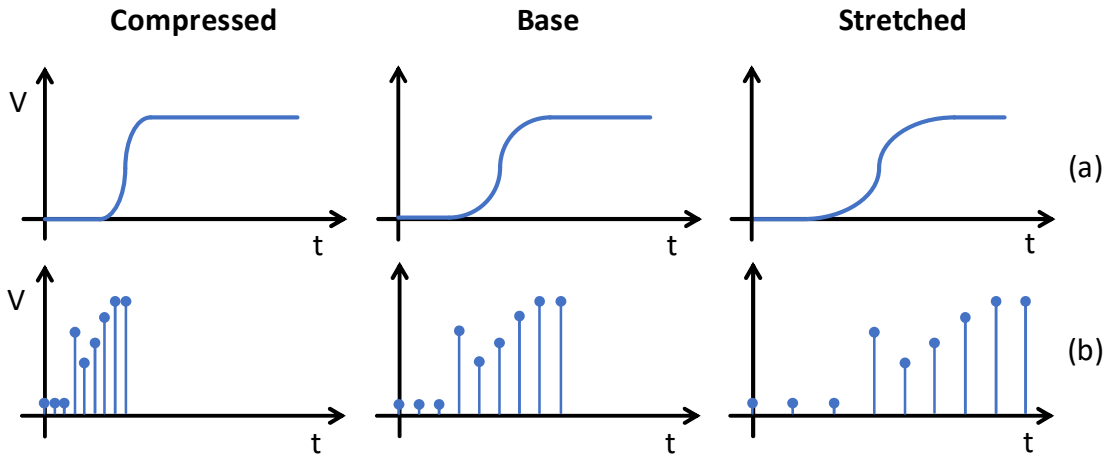

Figure 83 - Representative waveforms of ideal waveform scaling time for the continuous time (a) and discrete time (b) cases.

The most ideal form of time scaling operates in the same way as depicted in Figure 83. In both the continuous time (analogue) and discrete time (clocked digital) cases the entire waveform is stretched or compressed equally at all points. This maintains the relative positions of all points in the waveforms with respect to the starting point as the waveforms are stretched and compressed to make it last a greater or shorter amount of time respectively.

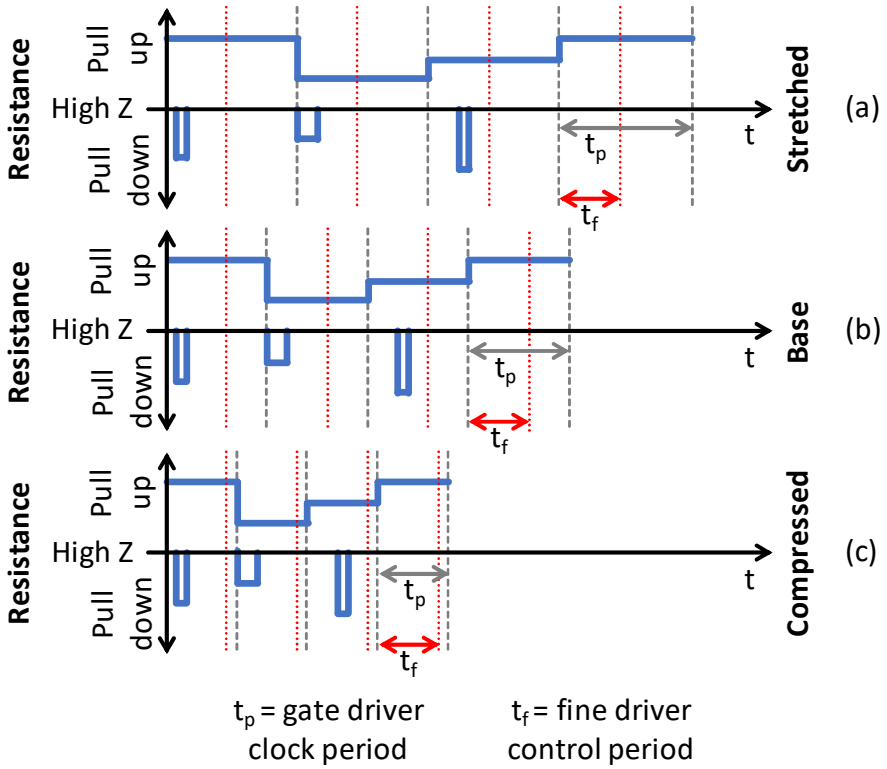

Figure 84 - Representative time scaling waveforms for the driver used in this work during the first half of a low-to-high turn-on transition. For more information about the prototype active gate driver refer to section 3.3.

In contrast to the ideal time scaling situation shown in Figure 83, the sub-nanosecond gate driver used in this work has a limitation which has been alluded to in the first technical chapter.

Figure 84 illustrates this limitation. In Figure 84.b, a resistance sequence is designed for a fixed set of operating conditions. The synchronous main drivers, that change with the internal clock period, provide the varying pull-up and the asynchronous parts, which are triggered by the start of each clock period, provide carefully crafted pull-down events.

In all parts of Figure 84, t_p shows the duration of the driver's internal clock period and t_f shows the fixed maximum delay period for the asynchronous drivers. The asynchronous nature of the fine drivers and fixed maximum delay are the limitation to scaling of the resistance sequences in time.

If the resistance sequence is fixed whilst the gate drivers' internal clock is adjusted the fine driver activations stay in the same place for the same duration relative to the start of each clock period. However, this means they are not in the same relative position or of the same relative duration within a clock cycle as is demonstrated in Figure 84.a and Figure 84.b. This leads to distortion of the intended resistance sequence in time which has an unknown impact on its effectiveness.

Alteration of the VCO clock frequency is the only method to alter the duration of the 'main' drivers and perform the stretching or compression of their resistance sequence. The limited resolution, available delay and available duration settings for the 'fine' drivers mean it is not easily possibly to synthesize a stretched or compressed base sequence with them. If this were possible it would still undesirable as it makes the stretching and compression process complicated and, in some cases, not possible.

6.8. Scaling Time to Track Load Current

The process for developing an optimized waveform, like that used in this work for the objectives stated, is concerned with manipulating the gate of the GaN HEMT at very specific points in its switching transition. The switching characteristics of GaN HEMTs, which active gate driving hopes to precisely control, is dependent upon the load current too. This requires the gate driver to compress or stretch the time over which the active gate driving profile is applied to maintain or track performance.

As shown in Figure 85, the indicated U-shape performance curve exists not only at the load current and clock frequency for which the active gate profile was developed, but that the same gate profile could be re-optimised by tuning the clock frequency at which it is reproduced. Giving rise to another such U-shaped curve, the 607 MHz gate profile, which could be formed about another optimal point.

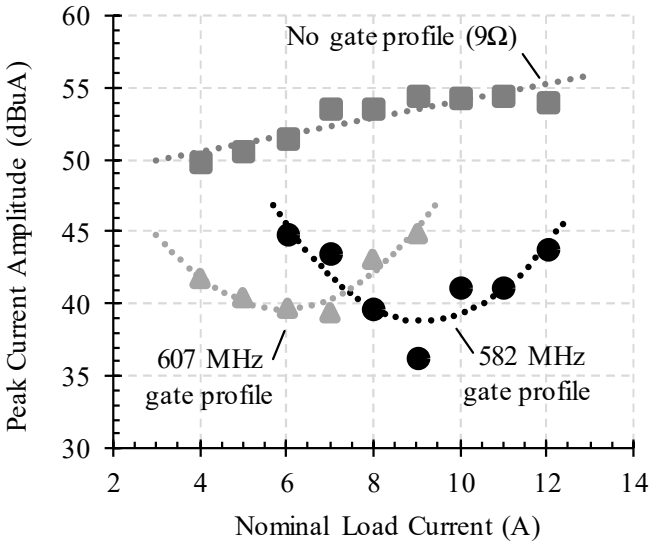

Figure 85 - Peak current magnitude between 300 MHz and 450 MHz plotted against steady state load current with the active drive sequence at two different playback frequencies.

This suggests that, for a given active gate driving profile, performance can be maintained across a much broader load current range than previously thought, without the need to change to an entirely new gate profile.

Furthermore, the results shown in Figure 85 suggest that even de-tuned by shifting load current, the active gate driving profile still performs significantly better than a comparable fixed gate resistance at the same load current. 9Ω is used for comparison as it produces similar drain current overshoot and peak $di\ /\ dt$ as seen in Figure 78.

6.9. Discussion and Conclusions

Active gate driving gate profiles have been developed to suppress current ringing in the 300-450 MHz band. The gate signal profiles used in this work remain close to optimal for $\pm$20% changes in current, and over a larger range of at least $\pm$35% the profiled waveforms perform better than a non-profiled gate waveform. Furthermore, it is shown that a gate drive profile which is becoming non-optimal as the load current changes, can to some extent, be re-optimised by stretching or compressing the gate profile in time, for example by changing the clock frequency of the active gate driver. Using this method, the problem of maintaining switching performance across a broad operating area becomes a single-parameter optimisation, which is simpler than optimising all the degrees of freedom of a complex driving pulse such as that of Figure 77.

In conclusion, currently reported open-loop high time resolution active gate driving profiles allow the potential of GaN HEMTs to be exploited more fully than conventional fixed gate resistance drivers. However, the open loop nature makes their impact on performance dependent upon current operating point versus the operating point at which they were optimised. A single parameter adaptation measure is shown to permit a fixed active gate driving profile to operate correctly over a wide load current range.

6.10. Further Work & Limitations

Further work directly following on from the findings of this chapter should focus verifying the re-optimisation at more load points. It has already been shown that re-optimisation at a load current below the design point is possible so the same should be repeated for a load current above the design point in the first instance. This should start to define any limits there may be to the degree of re-optimisation that is available using the time scaling technique.

As noted in the introduction, there are many other factors which can be called an operating parameter of the converter or that contribute to its current operating point. Therefore, the next most prudent parameters to vary and attempt to adapt with the time scaling concept are DC link voltage and power device temperature. Like load current, they contribute to the speed at which GaN HEMTs switch and can be sensed online and at high fidelity. Firstly, the impact of them to a fixed sub-nanosecond resistance sequence should be investigated to assess if adaptation to changes in them is needed. If it is and if adaptation to compensate for changes in them is possible then it addresses another challenge in the application of active gate driving.

It appears from experimentation that the suppression of circuit-specific resonances is achieved primarily by repeated rapid pull-down gate pulses (Figure 77) during a more gradual pulling-up of the gate. The intention of this work was to stretch or compress the gate profile in time, to compensate for changes in operating conditions. With the driver used in this work, however, the timings of these fast pull-down pulses are not perfectly scaled with the driver's clock frequency, as they are formed in part by asynchronous circuitry that permits pulses to be created that are shorter than the clock period. The resulting profile distortion may therefore be influencing the results.

7. Conclusion

7.1. Test Bed

This thesis covers the development of a high bandwidth active gate driving testbed and the investigation of how to use multi-GHz bandwidth gate signals to impact the switching of high voltage GaN HEMT power devices.

It covers the development of the support hardware required to drive a proto-type active gate driver capable of changing its output impedance every 100 ps to deliver between ± 10 A of gate current. Highlighted, in Chapter 1, are the challenges caused by high slew rates on the floating portions of the gate drive and support circuitry which are referenced to the switch-node of the bridge-leg. Careful selection of DC-DC converters and digital signal isolators are key to the test bed being self-immune to the 150 V/ns and 10 A/ns transitions it can produce. A GUI is developed along with embedded software to speed up visualisation and development of resistance sequences for the prototype gate driver, automate double pulse testing and data collection. This works in tandem with the support hardware to allow the testbed to function as an effective research tool.

Measurement techniques suitable for use with GaN HEMT devices and optimised power circuits featuring them are explored and evaluated. The effects of probe tip loading and the ground loop inductance are highlighted as having a big impact on the effective bandwidth of the measurement system. Considerations on the impact of a measurement technique on circuit layout and the parasitic inductance present are explored as this impacts the viability of certain power circuit current measurement methods. An example of this is the adaptations made to voltage probes to minimise ground loop inductance with spring pins and co-axial probe adaptors.

The testbed developed is used to verify the output of the prototype gate driver and show that the packaging parasitics do not compromise the high bandwidth waveforms as far as the measurement technique used allows. Then the gate driver is connected to a low-voltage GaN HEMT and the functionality re-verified. It is shown that, in this test case, the impact of the high-bandwidth gate drive waveform is visible in the power circuit waveforms; and that therefore, beneficial shaping of the waveforms could also be possible.

7.2. Results

Using the active gate driving test bed developed this thesis demonstrates results in the following key areas that contribute towards the original aims of this research at the end of the literature review.

"Is the switching transition of a current generation GaN on Si HEMT power device controllable via the gate?"

Chapters 2 and 3 deal with addressing this question. Firstly, it is shown that the impact of any kind of high bandwidth active gate driving applied to the gate of a GaN HEMT can be seen in the power circuit waveforms of a <100 V GaN HEMT.

The same capability is applied to mains voltage 650 V GaN HEMTs and shown to be useful for several objectives. It is possible to beneficially control both the drain current and drain-source voltage of both power devices in a bridge leg in both buck- and boost-mode operation. The sub-nanosecond timing capability of the custom active gate driver appears to be essential to allowing waveforms to be shaped and suggests that there may exist a trade-off between switching loss and ringing frequency and amplitude. It was found that using a 0.2 nH insertion impedance, ~225 MHz bandwidth current sensor facilitated the improvement of both current and voltage waveforms in the bridge-leg. The 150 ps resolution and wide active gate driver impedance range (0.12 to 64 Ω) permit the optimisation of 650 V GaN HEMT waveforms without the integration of the driver and power device into a single package.

"Can benefits, such as power circuit oscillation reduction and electrical stress reduction, be demonstrated with GaN HEMTs without artificially slowing switching transitions?"

In Chapter 3 several different improvements in multiple different operating configurations are shown. The first configuration tested is double pulsed boost mode operation. Power device drain current overshoots are reduced by ~10% without slowing down the switching transition compared to a 'fast' fixed resistance or increasing switching loss by >1 µJ compared to a 'slow' fixed resistance.

Double pulsed buck mode operation showed similar improvements with drain current oscillations effectively damped similarly to using a large gate resistance and peak current overshoot reduced by ~5 A. Switching delay, though not the smallest observed in the experiment, was comparable with that of a small fixed gate resistance which has greater drain current oscillation and overshoot.

The final operating mode tested in Chapter 3 is continuous boost mode operation. In this the goal is to turn on the control switch as quickly as when driven with a fixed 12 Ω gate resistance. However, the active gate driving sequence used is designed to obtain EMI-generating spectral components that are typical of slower 36 Ω driving. Above 125 MHz, active gate drive gives switch-node voltage waveform spectral content like that of slow 36 Ω driving, which is up to 9 dB lower than the 12 Ω fixed gate resistance case. In summary AGD allows spectral content like, and in places better than, that given by using a large gate resistance value without incurring the large switching loss normally associated with this situation.

Chapter 4 demonstrates control of power circuit waveform spectral content again. This time targeting the drain current waveform spectral content in the 300-450 MHz frequency band which is asserted to represent the characteristic resonance of the test bed. Compared to the fixed gate resistance used for comparison in the experiment an improvement of almost 20 dB is possible at the load current for which the resistance sequence was designed. This links to the final question which this thesis intends to address.

"What are the limitations of any benefits which can be demonstrated?"

Chapter 4 continues to explore how the benefit offered with active gate driving varies about the load point, 8 A, at which the resistance sequence is designed. Varying of the load current between ± 3 A of the design point degrades the time domain waveforms. However, performance is still >5 dB better than the fast, fixed gate resistance. This applies to all load points in the range to form a U-shaped curve of peak load current spectra amplitude observed in the frequency range of interest about the design point.

The experiment is extended to investigate a simple method for re-optimising the performance of the initial resistance sequence for a new load current. In this case it is re-optimised for a load current of 6 A; compressing the sequence in time by increasing the gate driver's clock frequency allowed a second U-shaped curve to be found. At 6 A it was 10 dB better than the fixed resistance sequence and across the same ± 3 A range the compressed sequence remained >5 dB better than the fixed resistance sequence.

In line with the original question about finding limitations of benefits demonstrated by AGD this indicates the useful load current range of a fixed resistance sequence when the goal is to supress spectral content associated with the characteristic circuit resonance.

8. Further Work

8.1. Generating new Knowledge

8.1.1. Dynamic R_{ds-o}

A reported, but not well investigated in the context of active gate driving, aspect of normally-off GaN HEMTs is the dynamic R_{ds-} they display [107], that is, the on-state resistance of a conducting device varies over time. The effect is dependent upon how long the device has been blocking a given potential before switching. This could impact the effectiveness of AGD for GaN HEMTs when switching continuously vs double pulsing. Therefore, this should be investigated to determine, if any, the impact it has on an established high bandwidth gate resistance sequences aimed at reducing non-ideal switching aspects such as those shown in this thesis.

8.1.2. Performance Tracking with Operating Conditions

The results and subsequent simple performance tracking method proposed in Chapter 4 are concerned only with load current. Many other parameters make up the operating point and operating conditions of a converter and could impact the switching performance of the GaN HEMTs. Therefore, testing the same situation and proposed tracking method with electrically slow parameters such as DC link voltage and physically slow parameters like power device temperature should be undertaken. This would help link the effectiveness of the method directly to the circuit parameters which effect how quickly GaN HEMTs switch. The data gathered could then inform a more comprehensive method of stretching and compressing in time to adapt to multiple different condition changes simultaneously.

8.1.3. Resistance Sequence Generation

To extend this work directly without further development of the prototype gate driver, investigation of automated methods for finding resistance sequences for a chosen goal should be pursued. This could take the form of a process that is only executed once or an iterative / adaptive process which happens continuously over successive or many switching events.

Due to the size of the problem space presented by a gate driver with many possible settings, the methods presented in the literature review which have been used to solve similar problems are not suitable. A more intelligent search method must be used such as a genetic algorithm or artificial neural network which can explore problem spaces with no prior knowledge is the most logical approach. Any approach used could benefit from manual minimisation of the problem space before being employed, for example, all constant output settings or average output resistance ranges could be defined for turn-on and turn-off edges.

This could then feed into designing a gate driver with an on-board CPU to make simple adaptations to the resistance sequence at run time such as that outlined in Chapter 4. Similarly, if the driver could be modified to include multiple memories and store several pre-configured resistance sequences with different objectives and an on-board CPU could select between them. The CPU could be used to adapt the stored sequences in accordance with operating parameters similarly to the method described in Chapter 4 to maintain effectiveness for their design objective. More complicated dedicated hardware for executing a trained neural network might be able to perform the entire resistance sequence optimisation process when given an objective.

8.1.4. Driving GaN Power Modules

The literature review supporting this work showed that multi-die power modules with GaN HEMTs have been possible at small scales with careful design of packaging parasitics. The work presented does not investigate the impact of driving multiple GaN HEMTs in parallel or HEMTs by more than two manufacturers. It is therefore unknown how well the findings translate and scale across a broader range of GaN HEMTs.

This gives rise to several ways the capabilities of high bandwidth active gate driving to influence the switching action of GaN HEMTs demonstrated in this work could be utilised.

Building larger modules – There could be a limit to the number of dies which can be successfully combined in series or parallel by a careful design alone. A large module (e.g. >4-6 GaN HEMT dies) driven by one or more high bandwidth active gate drivers could overcome the limitations of careful design alone.

Combining modules in series and parallel – Similarly to building larger modules; one or more high bandwidth active gate drivers could be used to safely combine several independently functional GaN HEMT power modules.

Improved switching action – The prototype gate driver presented in this work has significant gate drive current capability which is unused when driving a load with the characteristics of a single GaN HEMT gate. A layout optimised power module, comprising many GaN power devices, which can function when used with a conventional gate driver could be driven with the prototype driver to explore the demonstrated improvements with a power module.

8.2. Improving Presented Knowledge

8.2.1. Re-evaluating Probes and Probing Methods

New probes with greater performance have become available throughout the course of this work. Where possible they should be evaluated back to back with the probing methods presented in this work to test the assertion that waveform content well beyond the bandwidth of the probes used in this work is present and of interest.

If the high frequency content does exist, then repetition of experiments to compare results and conclusions back to back would be useful. In this work it is hypothesised that spectral content into multiple GHz is present and being generated but is undetectable with the probes available. It is possible that it would be detectable as radiated emissions but, due to the lab environment available, it would introduce hard to control quantities which would impact the repeatability of experiments.

Being able to capture this high frequency detail would allow for any subtler interactions and waveform differences due to high bandwidth active gate driving to be investigated.

Compensating for the response of the probes and measurement techniques used could help extend the useable bandwidth beyond manufacturer rated bandwidths. This might be possible by characterising probe response in conjunction with the adaptations used to allow in circuit probing (e.g. co-axial PCB adaptors) and then post-processing recorded data.

The ability sense current slew rate in the gate conduction loop using a field effect current probe like the one presented in Chapter 2 or capacitive coupling could be beneficial. Since the gate transients are only short, integration of di/dt data to gather DC information should be possible. For both turn-on and turn-off transients the initial DC level can be assumed to be approximately zero, though a small amount of leakage current will exist at the start of turn-off. Integrating over a short period of time limits the accumulation of DC error due to the measurement system too. Being charge controlled devices the switching action of the GaN HEMTs will be directly related to the current flowing into and out of the gate. This could help in the design of fixed resistance sequences or provide a useful control signal for closing the loop.

8.2.2. Root Cause of Characteristic Resonance

Investigation as to the source of the characteristic resonance shown and successfully suppressed in Chapter 4 could help inform the design of future power circuits. It is hypothesised that the source and the cause of the frequency range observed is the power circuit conduction loop inductance resonating with the output capacitance of the GaN HEMTs.

8.2.3. Use of Top-side Cooled Power Devices for Reduced Package Inductance

Investigation into the use of top-side cooled power devices from GaN Systems. Due to the way in which current flows with the GaNPX package of a bottom side cooled device it is asserted that a bottom side cooled device could offer reduced packaging inductance.

For a bottom side cooled device in a GaNPX package the current flows from the bottom of the package to the top and then down again to the power device die. This is mirrored for the current flowing out of the power device die since GaN HEMTs are lateral devices. In a top-side cooled GaNPX packaged device the die is the other way up meaning that current does not have to be routed from the bottom to the top of package before reaching the die.

This may produce a measurable improvement by further reducing the power loop inductance of an already optimised design and for double pulsing purposes the cooling requirement can be mostly ignored.

8.3. Addressing Test Bed Usability Limitations

For a direct continuation of this work to occur there are several refinements and improvements to the test bed and experimental methods which should be explored. They are aimed at increasing the reliability and repeatability of any given experiment or measurement.

Further automation of the testbed hardware would allow the embedded software and MATLAB to perform sequencing of the various power supplies during start-up and shut-down. Refinement of the GUI used to control the testbed and design resistance sequences could dramatically reduce the time taken to re-commence testing after a shutdown. It would also reduce the possibility of human error when transcribing experiment settings from results to re-run a specific experimental variation.

Re-design of the prototype gate driver support hardware to reduce the number of signals crossing the isolation boundary would help reduce the isolation capacitance and overall component count. This should give improved dv/dt immunity and would make assembly of new testbed PCBs faster.

The field effect current probes used are prone to errors caused by mis-alignment of the sensors to the track they are sensing the current in. While this can be compensated for a single situation a <1 mm lateral shift can cause significant change in sensor gain. Therefore, completing a family of experiments can be problematic and repeating any number, with the same sensor compensation, after the testbed has been disturbed is almost impossible. A mounting method to mechanically stabilise the sensor to the PCB would aid in setting up the testbed and reduce variation within a single experiment. An alternate solution would be to co-design and build the sensor structure into the PCB however this

causes problems for layer-to-layer insulation and increases the possibility of damaging the probe or oscilloscope.

9. Final Word

High bandwidth active gate driving can and should be applied to GaN HEMTs to control their switching action at high power levels and high slew rates. This thesis presents high bandwidth active gate driving for GaN HEMTs as a functional alternative to traditional switching aids. Demonstrating its ability to reduce current and voltage stresses without increasing switching loss and influence the spectra of associated waveforms.

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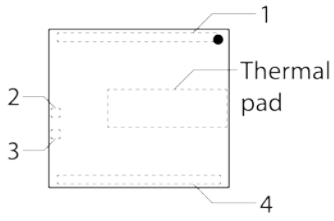
Appendix A: GaN Systems GS66508P Datasheet

GS66508P
Bottom-side cooled 650 V E-mode GaN transistor
Preliminary Datasheet

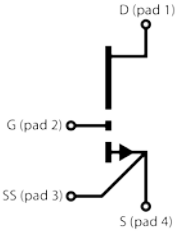
Features

- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 50 mΩ
- $I_{DS(max)}$ = 30 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 10.0 x 8.7 mm² PCB footprint
- Source Sense (SS) pin for optimized gate drive
- RoHS 6 compliant

Package Outline



Circuit Symbol



The thermal pad must be connected to Source, S (pad 4), for best performance

Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- Class D Audio amplifiers
- 400 V input DC-DC converters
- On Board Battery Chargers
- Traction Drive

Description

The GS66508P is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS66508P is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Submit datasheet feedback

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	30	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	25	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	72	A

(1) Pulse ≤ 1 µs

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.5	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	7.0	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	24	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS66508P-TR	GaN*PX*® Bottom-Side Cooled	Tape-and-Reel	2000	13" (330mm)	24mm
GS66508P-MR	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	7" (180mm)	24mm

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		50	63	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 9 A
Drain-to-Source On Resistance	$R_{DS(on)}$		129		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 9 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 7 mA
Gate-to-Source Current	I_{GS}		160		µA	V_{GS} = 6 V, V_{DS} = 0 V
Reverse Gate Leakage Current	I_{RGL}		10		nA	V_{GS} = -10 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V, I_{DS} = 30 A
Drain-to-Source Leakage Current	I_{DSS}		2	50	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		400		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		1.3		Ω	f = 25 MHz, open drain
Input Capacitance	C_{ISS}		260		pF	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		65		pF	
Reverse Transfer Capacitance	C_{RSS}		2		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		88		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		142		pF	
Total Gate Charge	Q_G		5.8		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		2.2		nC	
Gate-to-Drain Charge	Q_{GD}		1.8		nC	
Output Charge	Q_{OSS}		57		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics continued (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.1		ns	V_{DD} = 400 V, V_{GS} = 0-6 V I_{DS} = 16 A, $R_{G(ext)}$ = 5 Ω T_J = 25 °C (note 5)
Rise Time	t_R		3.7		ns	
Turn-Off Delay	$t_{D(off)}$		8		ns	
Fall Time	t_F		5.2		ns	
Turn-On Delay	$t_{D(on)}$		4.3		ns	V_{DD} = 400 V, V_{GS} = 0-6 V I_{DS} = 16 A, $R_{G(ext)}$ = 5 Ω T_J =125 °C (note 6)
Rise Time	t_R		4.9		ns	
Turn-Off Delay	$t_{D(off)}$		8.2		ns	
Fall Time	t_F		3.4		ns	
Output Capacitance Stored Energy	E_{OSS}		7		µJ	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz
Switching Energy during turn-on	E_{on}		47.5		µJ	V_{DS} = 400 V, I_{DS} = 15 A V_{GS} = 0 - 6 V, $R_{G(on)}$ = 10 Ω $R_{G(off)}$ = 1 Ω, L = 40 µH L_P = 10 nH (notes 7, 8)
Switching Energy during turn-off	E_{off}		7.5		µJ	

(6) See Figure 12 for timing test circuit diagram and definition waveforms

(7) L_P = parasitic inductance

(8) See Figure 13 for switching test circuit

Electrical Performance Graphs

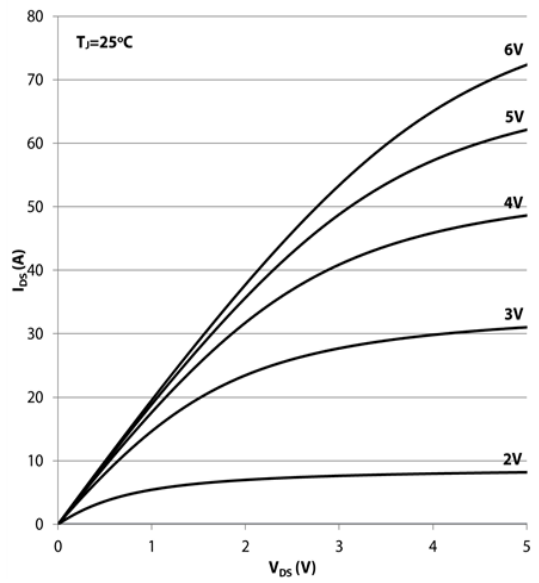


Figure 1 : Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

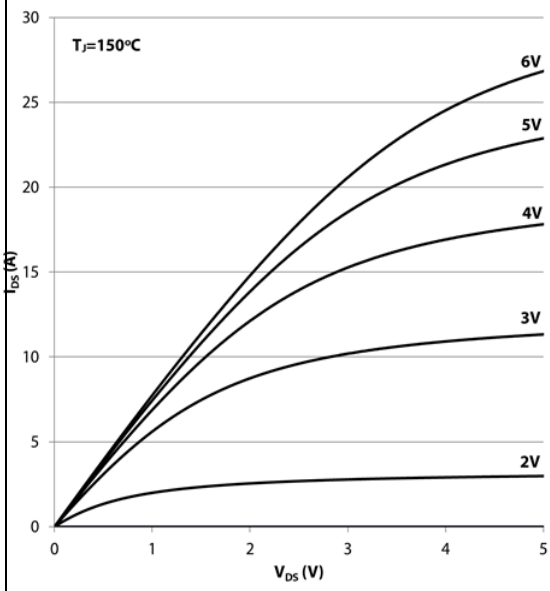


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

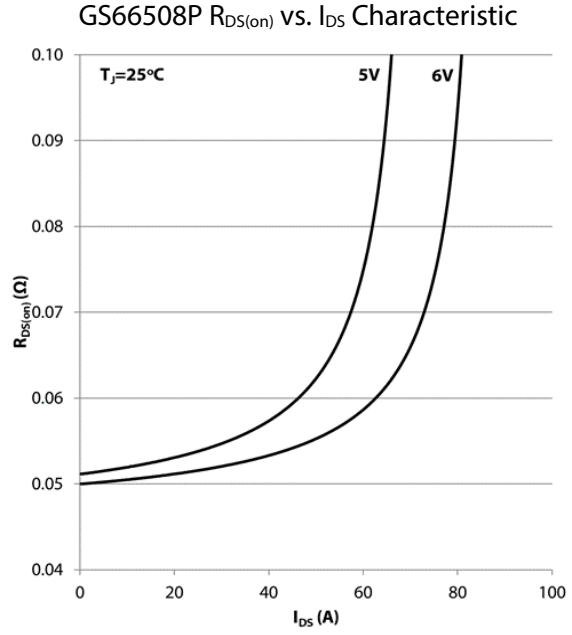


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

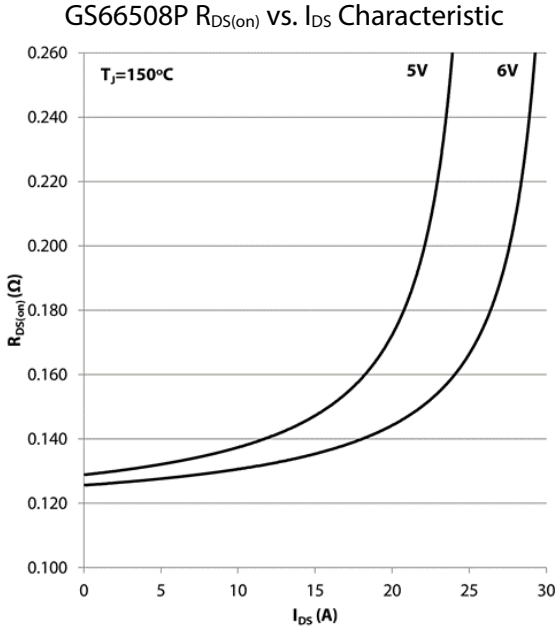


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

GS66508P I_{DS} vs. V_{DS}, T_J dependence

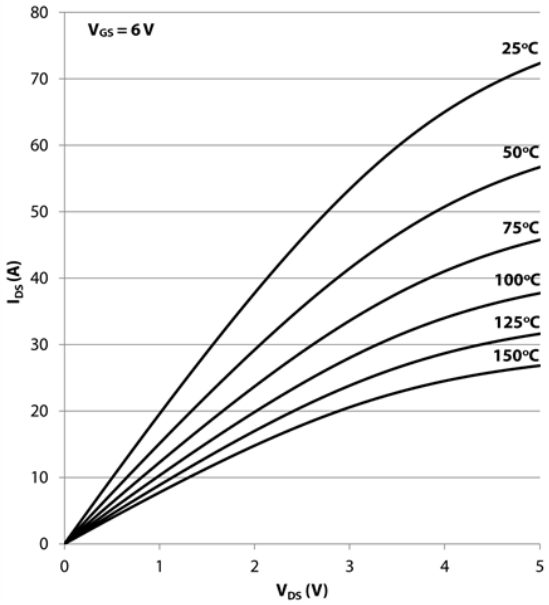


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

GS66508P Gate Charge, Q_G Characteristic

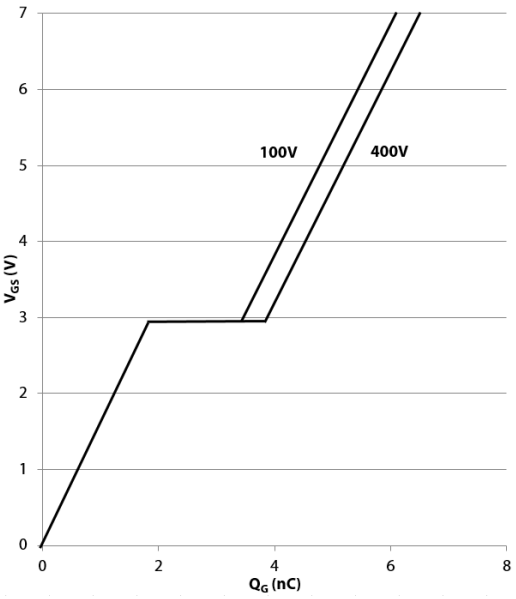


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

GS66508P Capacitance Characteristics

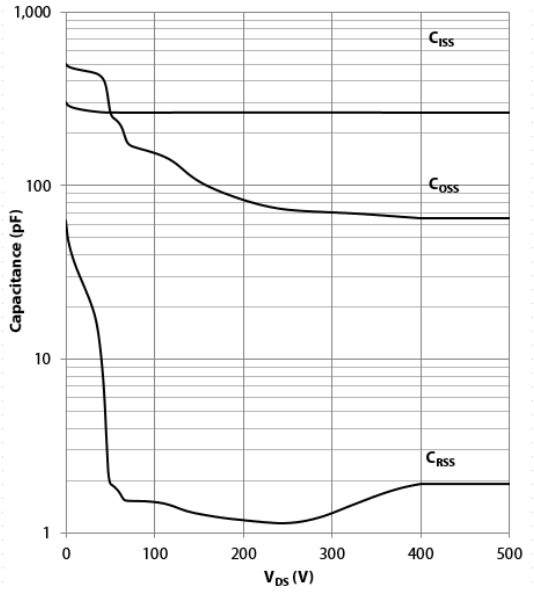


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS66508P Stored Energy Characteristic

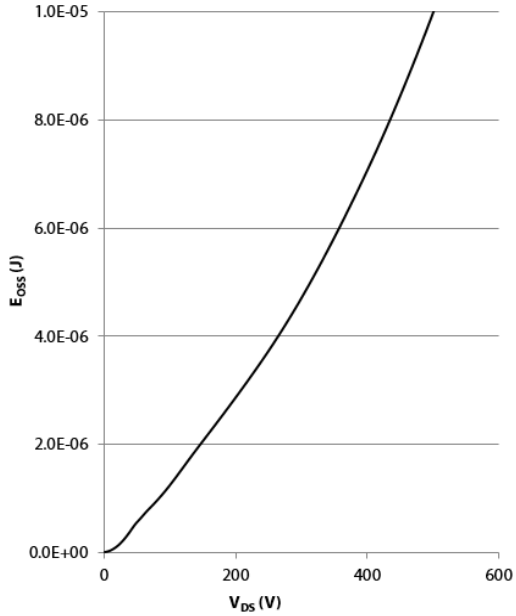


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

GS66508P Reverse Conduction Characteristics

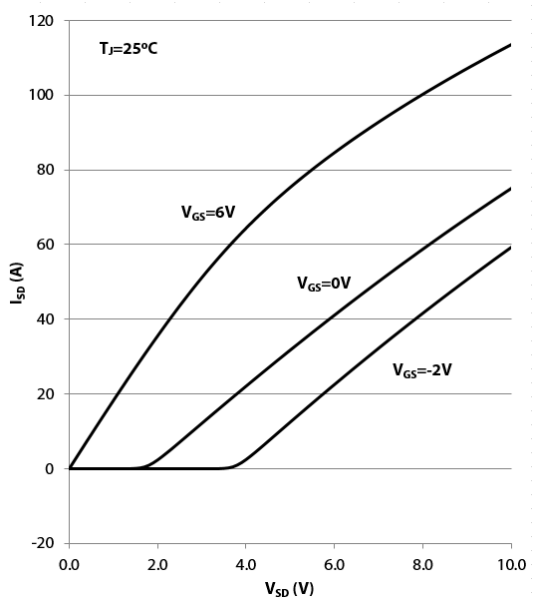


Figure 9: Typical I_{SD} vs. V_{SD}

GS66508P I_{DS} vs. V_{GS} Characteristic

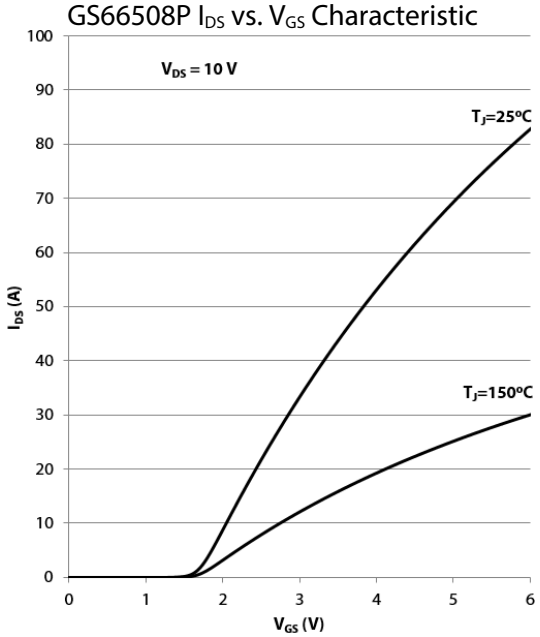


Figure 10: Typical I_{DS} vs. V_{GS}

GS66508P $R_{DS(on)}$ Temperature Dependence

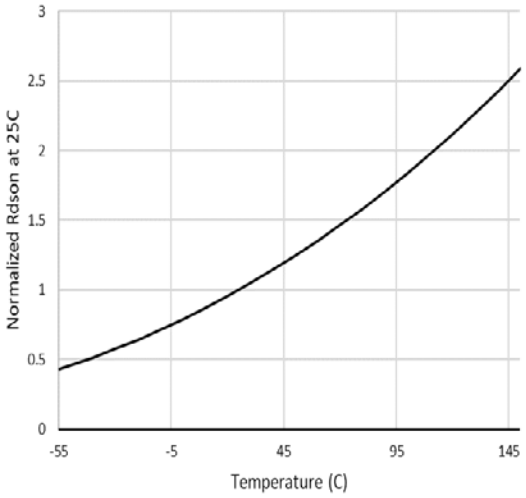


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

GS66508P I_{DS} - V_{DS} SOA

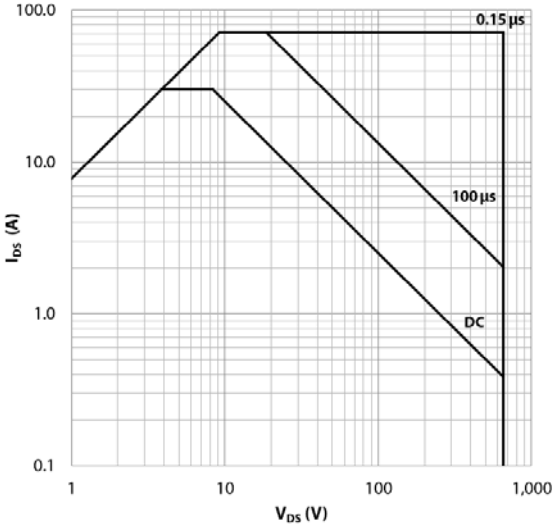


Figure 12: Safe Operating Area @ T_{case} = 25 °C

Thermal Performance Graphs

GS66508P Power Dissipation Temperature Derating

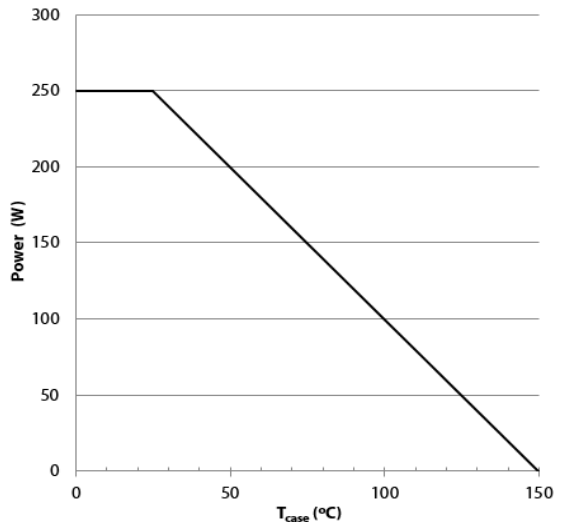


Figure 13: Power Derating vs. T_{case}

GS66508P Transient $R_{\theta JC}$

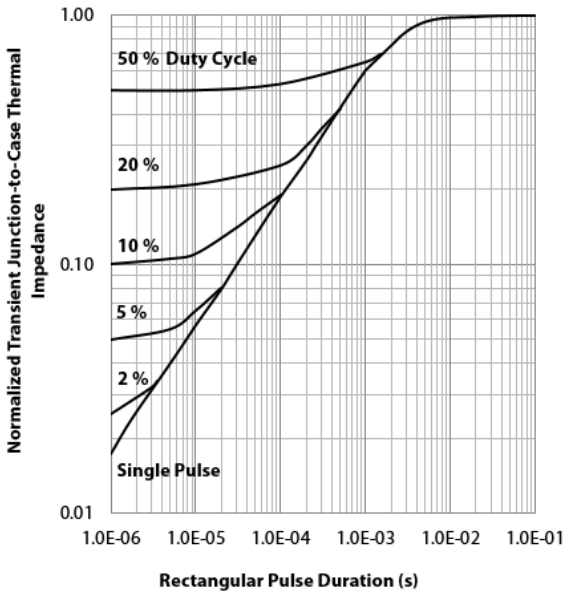


Figure 14: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

Test Circuits

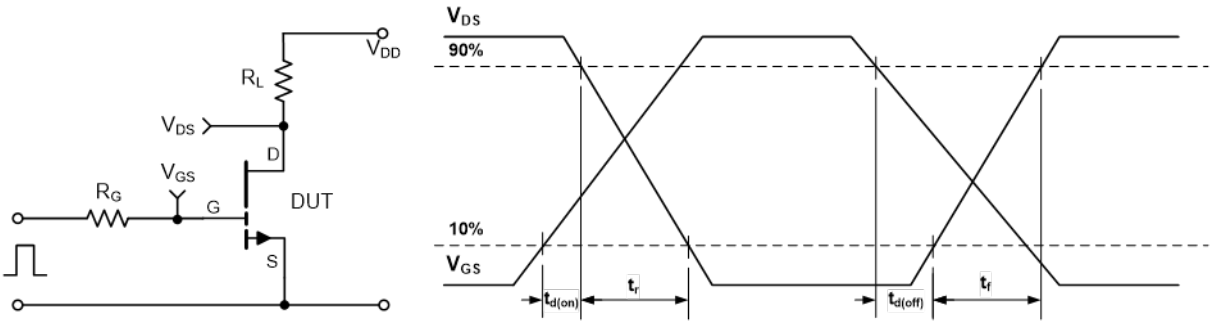


Figure 15: GS66508P switching time test circuit and waveforms

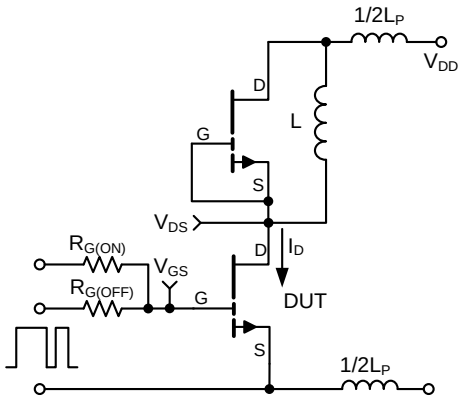


Figure 16: GS66508P Switching Loss Test Circuit

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 at www.gansystems.com.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note GN001 for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note GN001 for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The GS66508P has a dedicated source sense pin. The GaN*PX*® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad on the GS66508P and returning from the source sense pad on the GS66508P to the driver ground reference.

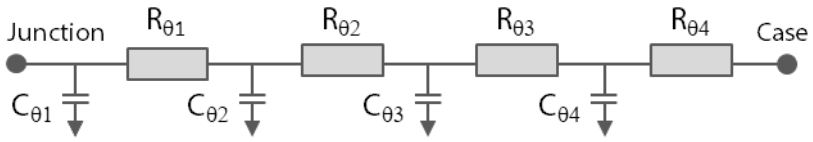
Thermal

The substrate is internally connected to the thermal pad on the bottom-side of the GS66508P. The source pad must be electrically connected to the thermal pad for optimal performance. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under the Drain pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

GS66508P RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.015	$C_{\theta 1}$ = 8.0E-05
$R_{\theta 2}$ = 0.23	$C_{\theta 2}$ = 7.4E-04
$R_{\theta 3}$ = 0.24	$C_{\theta 3}$ = 6.5E-03
$R_{\theta 4}$ = 0.015	$C_{\theta 4}$ = 2.0E-03

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending

on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage
The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering
The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66508P device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

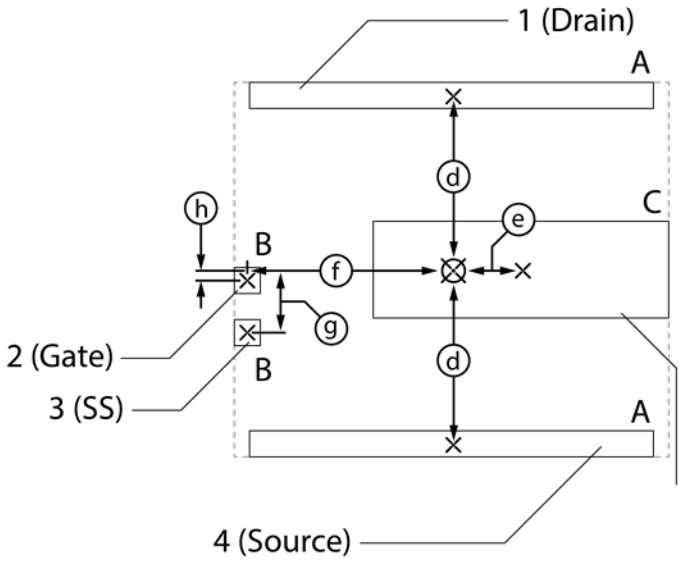
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues.

Recommended PCB Footprint for GS66508P



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	9.30	0.60	0.366	0.024
B	0.60	0.60	0.024	0.024
C	6.80	2.23	0.268	0.088

Dimensions

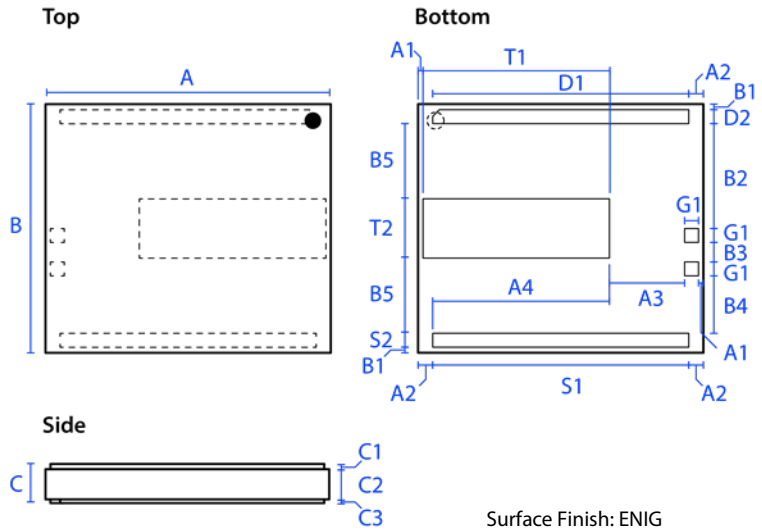
	mm	Inches
d	4.02	0.158
e	1.60	0.063
f	4.70	0.185
g	1.45	0.057
h	0.25	0.010

PCB pad openings

Package outline

NOTE: Thermal pad must be connected to Source (pad 4) for best performance

Package Dimensions

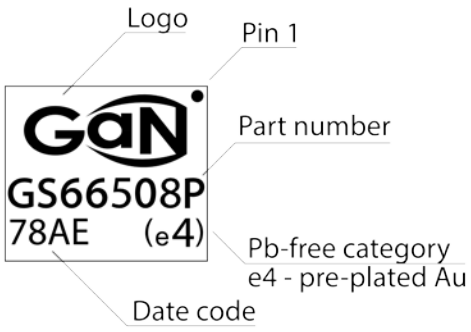


	mm	Inches	
A	10.05	0.396	± 0.10 mm (0.004″)
A1	0.075	0.003	± 0.05 mm (0.002″)
A2	0.425	0.017	± 0.05 mm (0.002″)
A3	2.70	0.106	
A4	6.35	0.250	
B	8.68	0.342	± 0.10 mm (0.004″)
B1	0.075	0.003	± 0.05 mm (0.002″)
B2	3.77	0.148	
B3	0.70	0.028	
B4	2.06	0.081	
B5	2.70	0.106	
C	0.51	0.0201	± 0.05 mm (0.002″)
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	9.20	0.362	
D2	0.50	0.020	
G1	0.50	0.020	
S1	9.20	0.362	
S2	0.50	0.020	
T1	6.70	0.264	
T2	2.13	0.084	

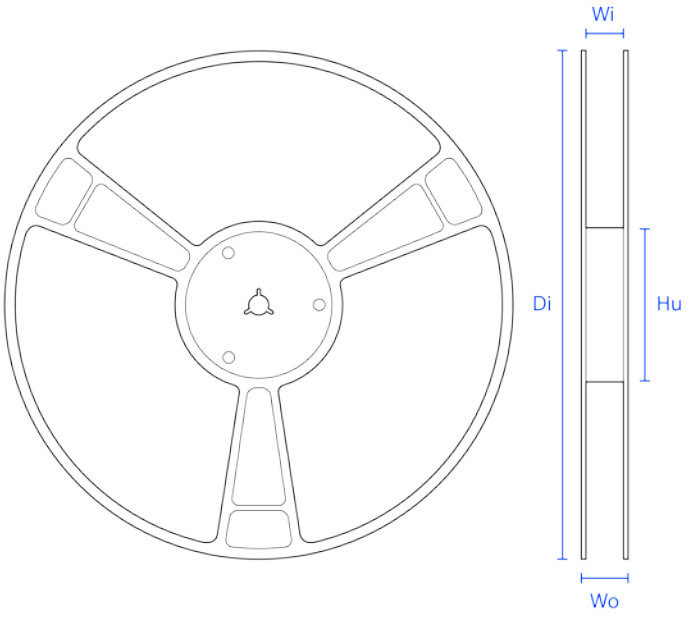
Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

Note: Inch measurements are approximate values

GaN*PX*® Part Marking

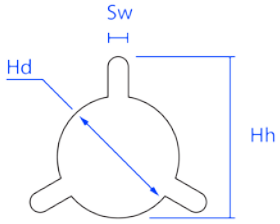


GS660508P GaN*PX*® Tape and Reel Information

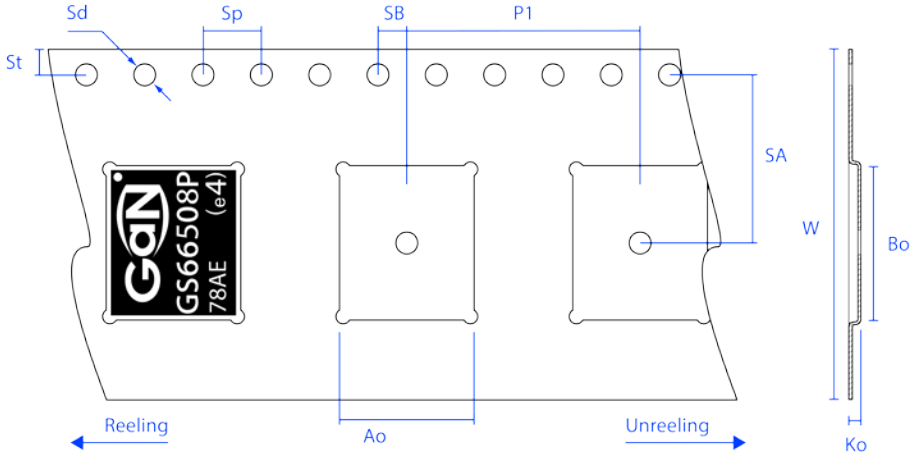


Dimensions (mm)

	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	178.0	+ 1.0 / - 0.0
Wo	30.4	MAX	27.7	+/-1.0
Wi	24.4	+ 2.0 / - 0.0	25.0	+ 1.0 / - 0.0
Hu	100.0	+/- 1.5	60.0	+ 1.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.5
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.0	+/- 0.2



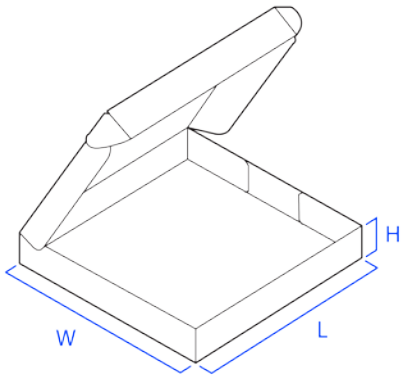
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	16.00	+/- 0.1
W	24.00	+/- 0.3
Ko	0.84	+/- 0.1
Ao	9.23	+/- 0.1
Bo	10.58	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	11.5	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



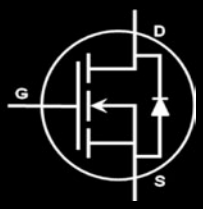
Outside dimensions (mm)		
	7″ mini-reel	13″ tape-reel
W	197	342
L	204	355
H	32	53

Appendix B: EPC EPC2015 Datasheet

EPC2015 – Enhancement Mode Power Transistor

V_{DSS}, 40 V
$R_{DS(ON)}$, 4 mΩ
I_D, 33 A

NEW PRODUCT



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 125° C)	48	V
I_D	Continuous (T_A = 25°C, θ_{JA} = 13)	33	A
	Pulsed (25°C, Tpulse = 300 µs)	150	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-5	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

EPC2015 eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics (T_J= 25°C unless otherwise stated)						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 500 µA	40			V
I_{DSS}	Drain Source Leakage	V_{DS} = 32 V, V_{GS} = 0 V		200	400	µA
I_{GSS}	Gate-Source Forward Leakage	V_{GS} = 5 V		1.5	7	mA
	Gate-Source Reverse Leakage	V_{GS} = -5 V		0.3	1.5	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 9 mA	0.7	1.4	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 33 A		3.2	4	mΩ
Source-Drain Characteristics (T_J= 25°C unless otherwise stated)						
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V, T = 25°C		1.75		V
		I_S = 0.5 A, V_{GS} = 0 V, T = 150°C		1.8		

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	15	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	54	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V		1100	1200	pF
C_{OSS}	Output Capacitance			575	750	
C_{RSS}	Reverse Transfer Capacitance			60	70	
Q_G	Total Gate Charge (V_{GS} = 5 V)	V_{DS} = 20 V, I_D = 33 A		10.5	11.6	nC
Q_{GD}	Gate to Drain Charge			2.2	2.7	
Q_{GS}	Gate to Source Charge			3	3.5	
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		18.5	22	
Q_{RR}	Source-Drain Recovery Charge			0	0	

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics

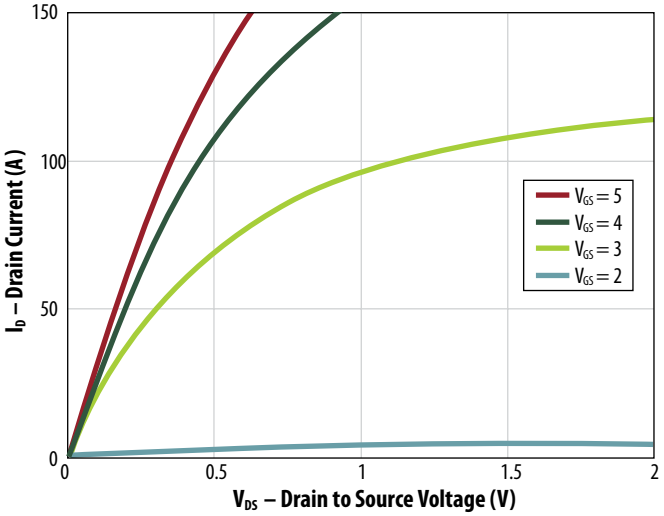


Figure 2: Transfer Characteristics

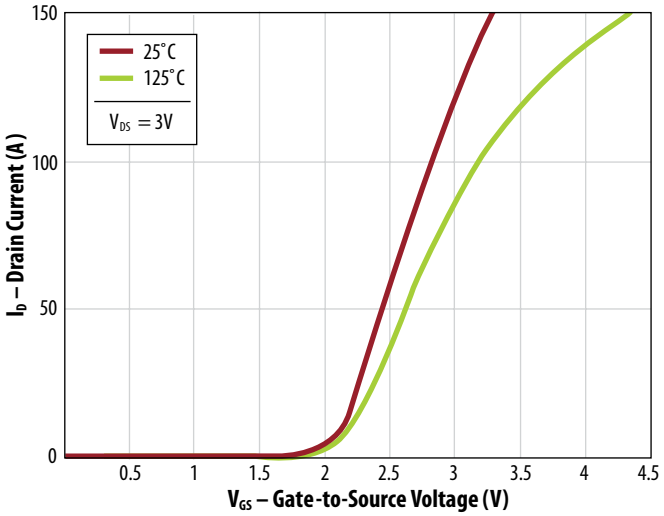


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Current

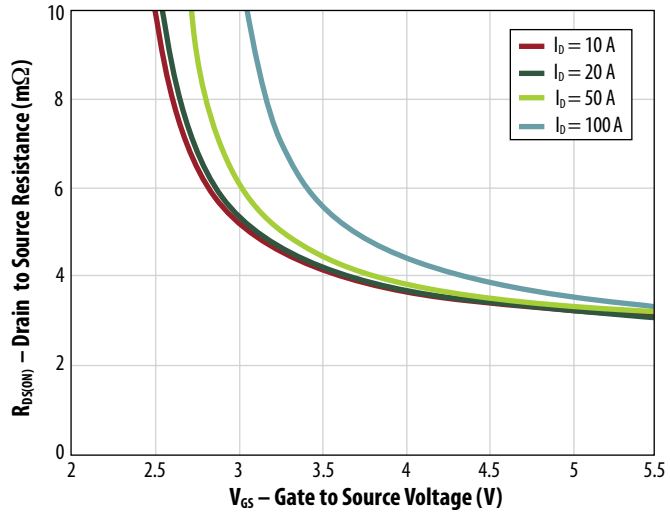


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperature

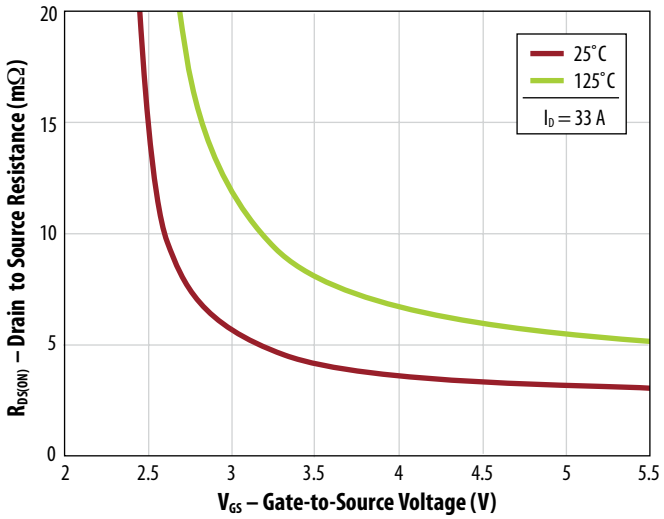


Figure 5: Capacitance

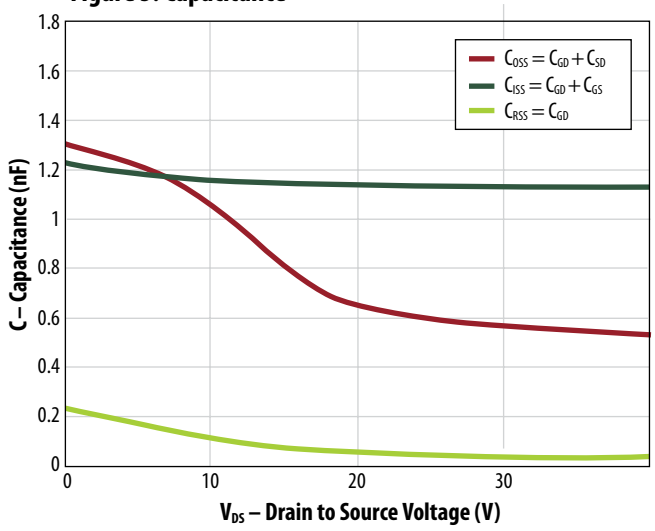


Figure 6: Gate Charge

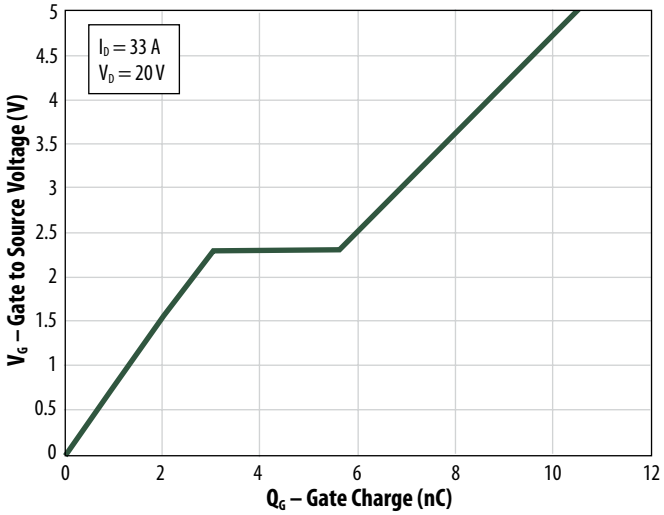


Figure 7: Reverse Drain-Source Characteristics

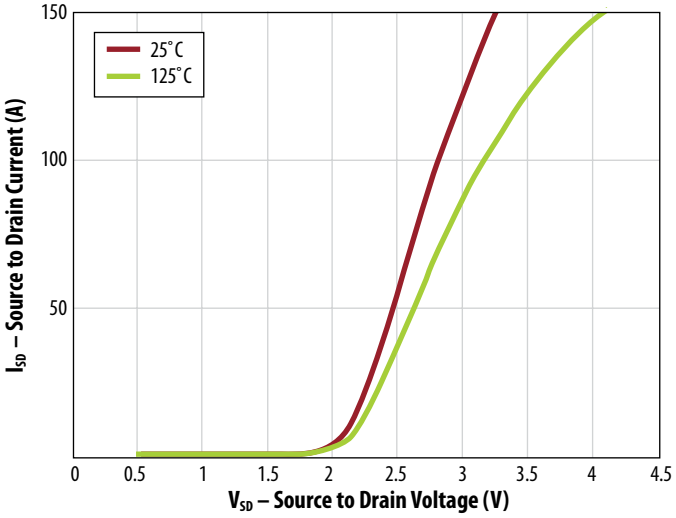


Figure 8: Normalized On Resistance Vs Temperature

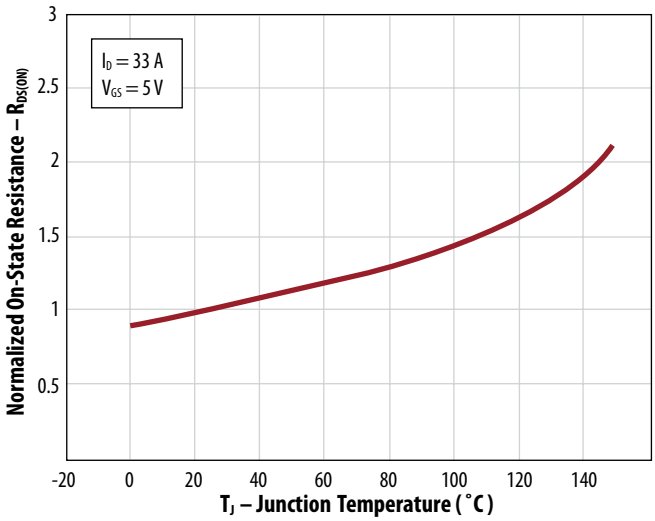


Figure 9: Normalized Threshold Voltage vs. Temperature

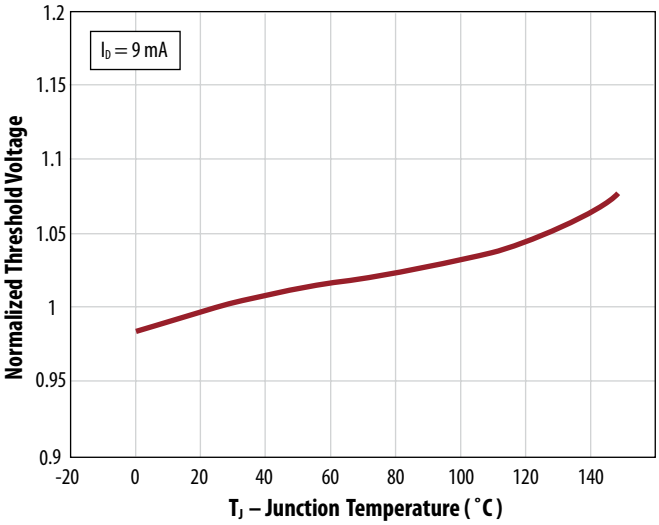
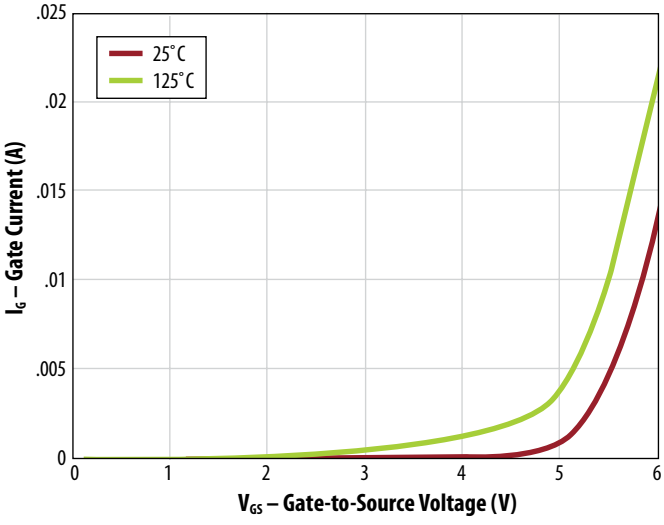
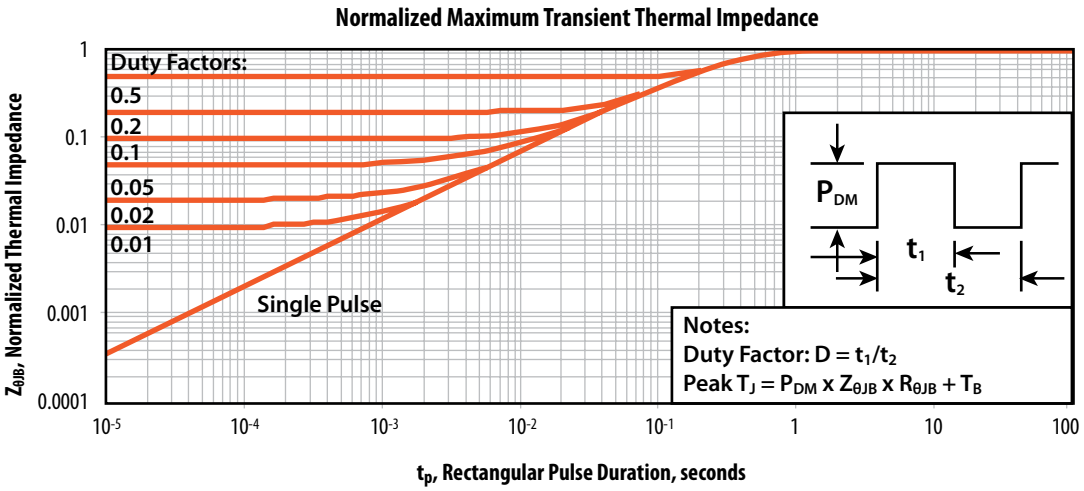


Figure 10: Gate Current



All measurements were done with substrate shortened to source.

Figure 11: Transient Thermal Response Curves



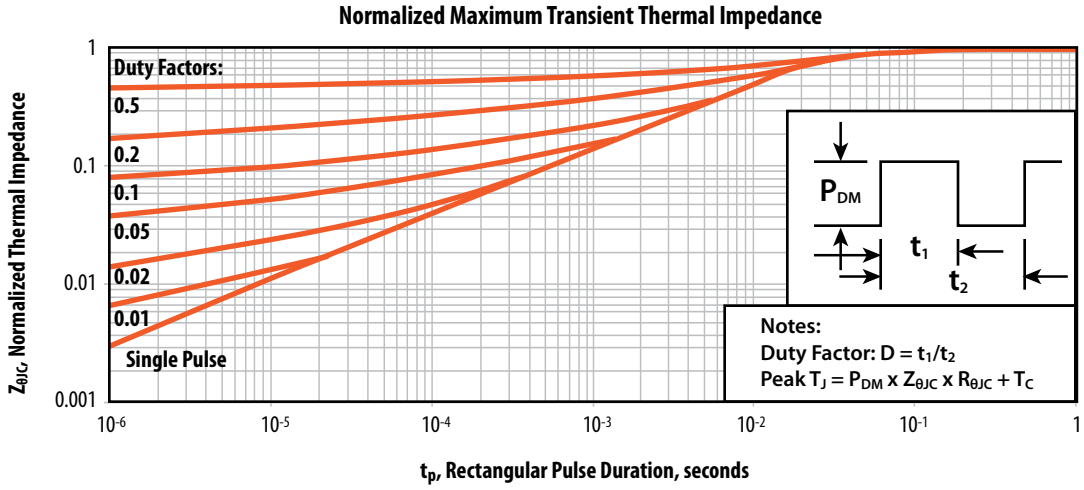
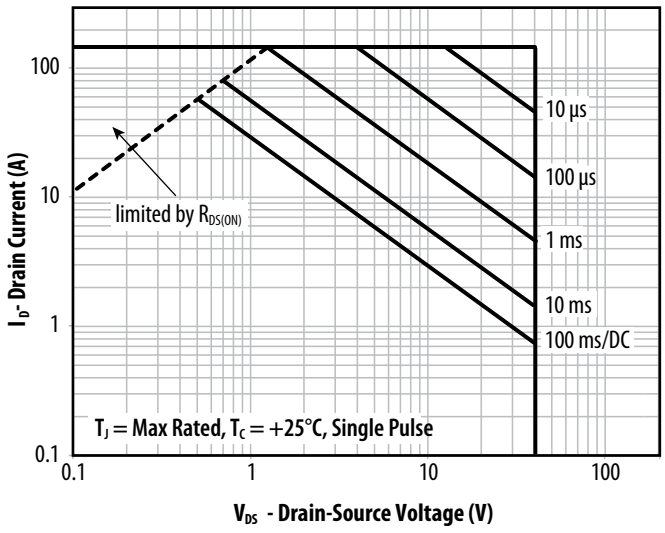
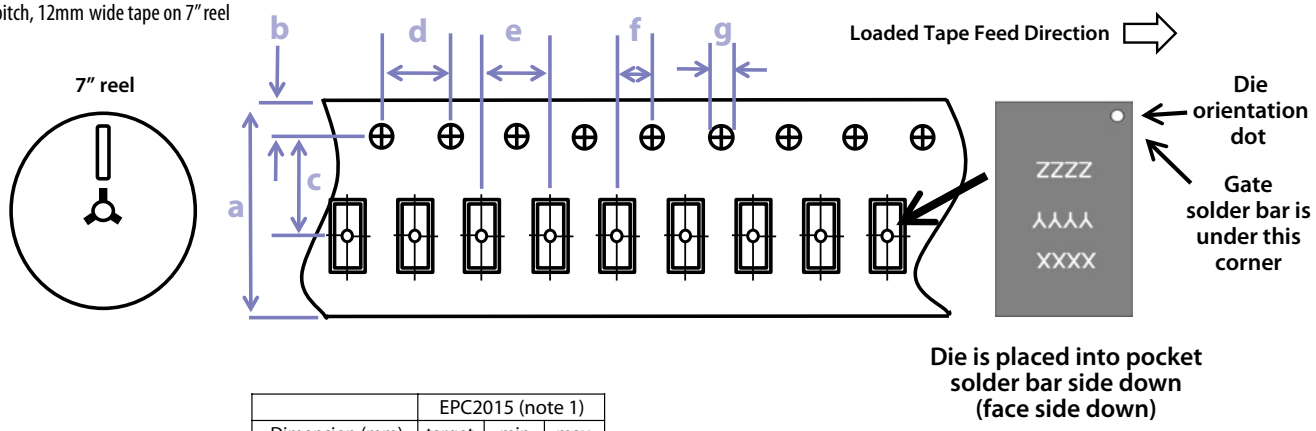


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

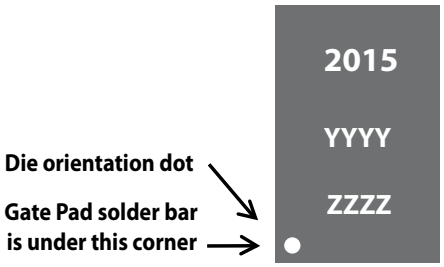
4mm pitch, 12mm wide tape on 7" reel



	EPC2015 (note 1)		
Dimension (mm)	target	min	max
a	12.0	11.7	12.3
b	1.75	1.65	1.85
c (note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

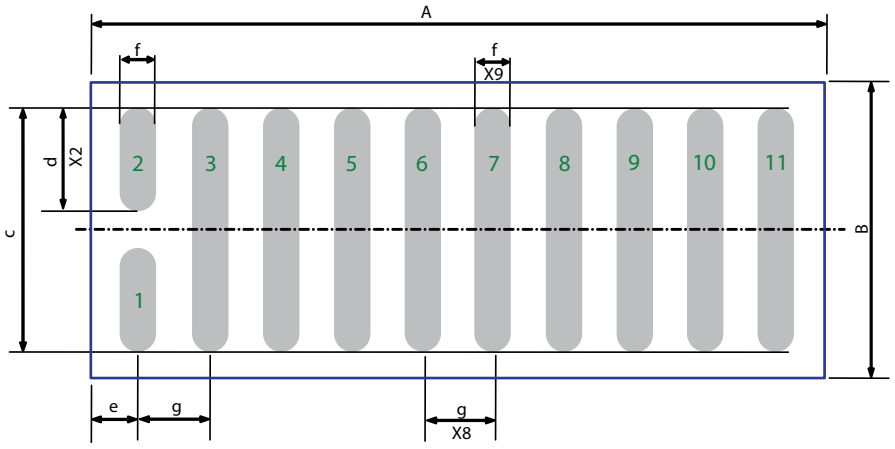
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2015	2015	YYYY	ZZZZ

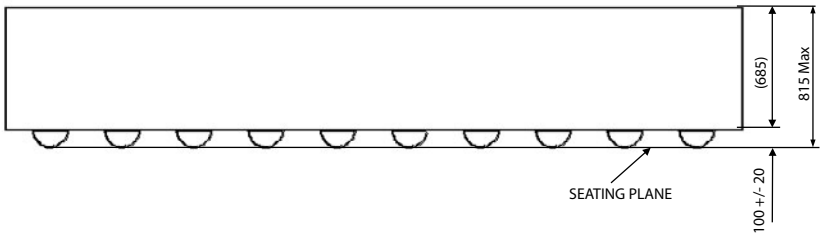
DIE OUTLINE

Solder Bar View



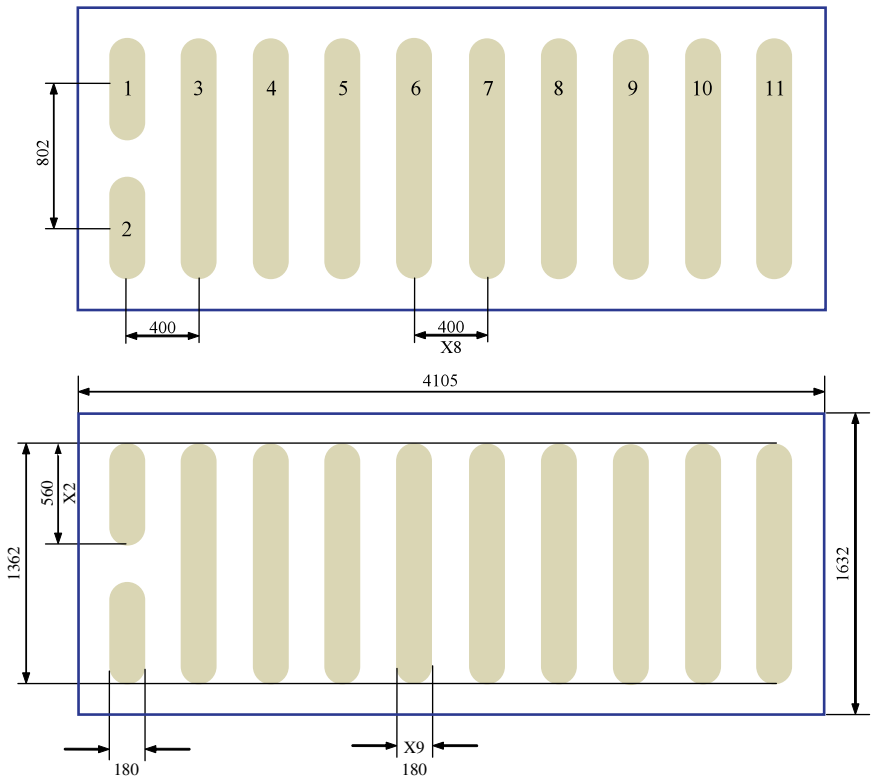
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Side View



RECOMMENDED LAND PATTERN
(units in µm)

The land pattern is solder mask defined.



Pad no. 1 is Gate;

Pads no. 3, 5, 7, 9, 11 are Drain;

Pads no. 4, 6, 8, 10 are Source;

Pad no. 2 is Substrate.

Appendix C: UoB Differential Rogowski ‘Infinity’ Field Probe Current Sensor Datasheet

Applications

- Measuring current waveforms for power semiconductor devices
- Measuring pulse current
- Measuring ac current superimposed on dc current
- Measuring high-frequency sinusoidal current

Features

- Non-intrusive and low insertion inductance, loading the circuit under test by 0.2 nH (at 1 GHz) or less, depending on the current slew rate
- Galvanic isolation and floating measurement
- 300 MHz bandwidth when using with a standard 500 MHz voltage probe
- Intrinsic noise cancellation
- Minimum changes to the PCB design

1. Basics

The basic design concept of the current sensor is illustrated in Fig. 1. It consists of one planar coil on each side of the orange PCB trace carrying the current to be measured. The current sensor detects magnetic field changes as the current flowing through the PCB trace changes. It induces a voltage in the two planar coils. These two coils are connected in series so that the current in the trace directly under the sensor provide two signal components of the same polarity, thus providing a voltage signal v_{out} that is proportional to *di/dt* and expressed as

$$v_{out} = M\frac{di}{dt} \quad (1)$$

where M is the mutual inductance between the current sensor and the power loop which the trace carrying the current is part of. The current can thereby be derived as

$$i = \int \frac{v_{out}}{M} dt \quad (2).$$

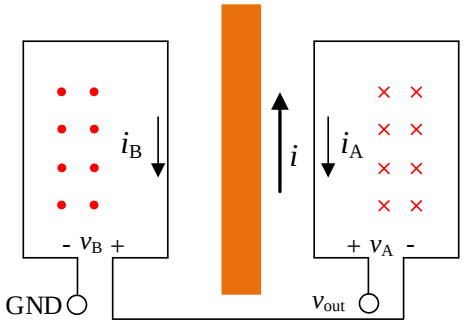


Fig. 1. The proposed current sensor.

Currents in the traces outside of the sensor footprint induce opposing signals in the two coils that cancel out with each other, thus providing high noise immunity. The concept is

similar to a planar subset of a Rogowski coil, with the coils moved up to the trace to optimise noise immunity. The current sensor sits on the circuit board and right above the trace to be measured as illustrated in Fig. 2. The ground plane does not need to be altered, which leads to this sensor having an almost negligible effect on switching performance.

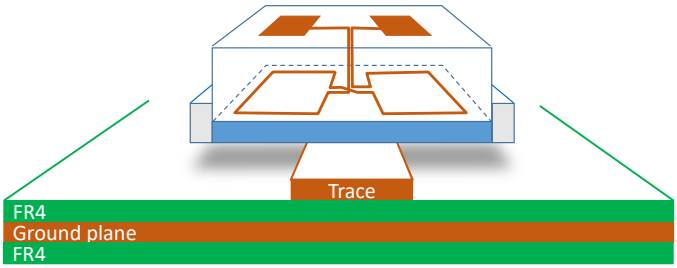


Fig. 2. The current sensor sitting on the circuit board and right above the trace to be measured.

2. Insulation

Although there is an insulation layer on the coil side, **from the safety perspective, it is important that the sensor be treated as without any insulation**. One method to enhance insulation is to coat the coil side with insulation tape. This would slightly reduce the mutual inductance between the sensor and the current-carrying trace, and reduce or increase the coupling capacitance between them, depending on the thickness and dielectric constant of the insulation material.

3. How to use

A 3mm (or less) trace carrying the current to be measured is required. To reduce common mode noise, avoid measuring on traces with high dv/dt.

As shown in Fig. 2, to use the sensor to measure current, place it right above the trace with the coil side facing downward and the trace right in between two coils; use twisted pair to connect the output of the sensor to the oscilloscope through a probe. The bandwidth of the oscilloscope and probe determines the measurement bandwidth.

The current can be calculated according to eqn. (2). The coefficient M is dependent on the relative position of the sensor coils and the trace, among other things. If a transient current with known steady-state value is measured, M can be deduced from the ratio between the steady-state value of the integration of the sensor output over time and that of the current.

4. An example

Current sensors of two different sizes are shown in Fig. 3. The smaller one is generally used to measure current with higher di/dt.

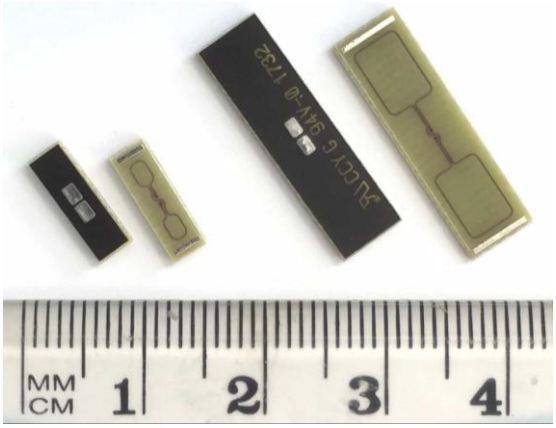
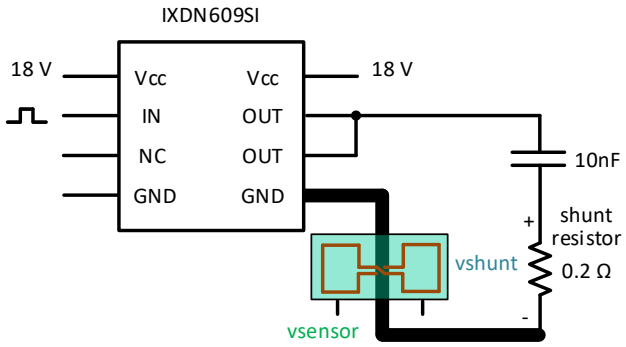
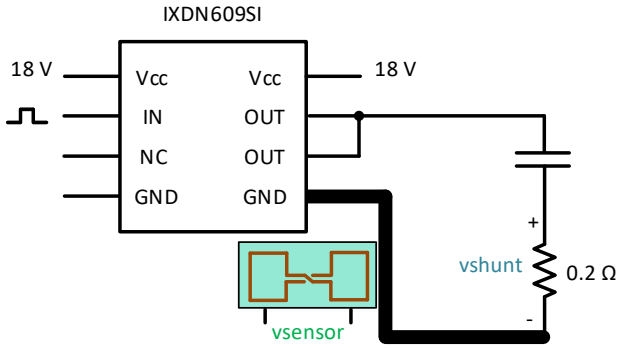


Fig. 3. Photo of current sensors of two different sizes.

A simple circuit as shown in Fig. 4 is built up to test the smaller current sensor. The output of the gate driver is connected to an RC network to create a high-speed current pulse. The sensor is placed at two difference positions: one right on the trace, the other right on the edge of the trace, as shown in Fig. 4(a) and (b) respectively.



(a) Current sensor at position 1.

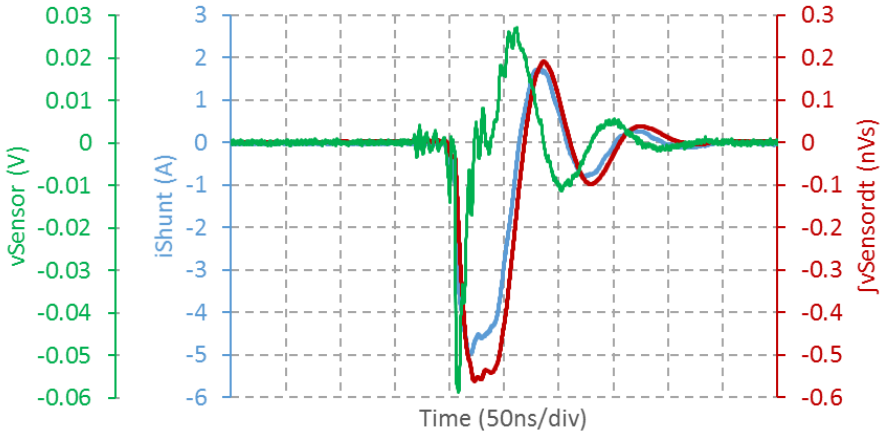


(b) Current sensor at position 2.

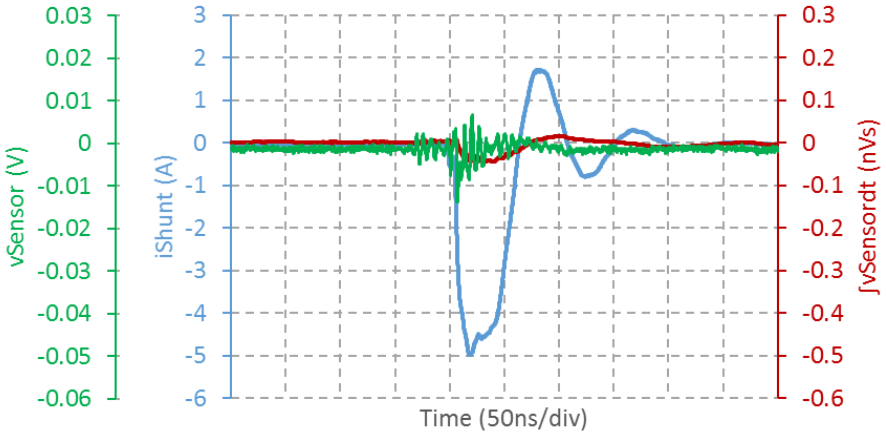
Fig. 4. Test circuit.

The test results shown in Fig. 5 are taken at gate driver pull-down. It is demonstrated that when the sensor is placed right on the trace with the trace in the middle of the two coils, the measurement agrees well with that by the shunt resistor. The mutual inductance (i.e., the

coefficient *M* in eqn. (2)) in this case is 0.112 nH. When the sensor is placed on the edge of the trace, unwanted current in immediate proximity is attenuated by 90%.



(a) Current sensor at position 1.



(b) Current sensor at position 2.

Fig. 5 Test results at gate driver pull-down.