A Neutral-Point Diode-Clamped Converter with Inherent Voltage-Boosting for a Four-Phase SRM Drive

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Abstract - **This paper proposes a new asymmetric neutral-point diode-clamped (NPC) multilevel converter for a four-phase switched reluctance motor drive. The inbuilt NPC clamping capacitors are used for both voltage level clamping and also as dc rail voltage-boosting capacitors to increase the output power of the motor, particularly for high-speed electric vehicle applications. The new converter allows regenerative energy to be recovered back to the dc supply for rapid machine braking, thus increasing overall drive efficiency. Analysis of the different modes of converter operation, along with design equations for sizing the voltage-boosting capacitors, are detailed. The effect of capacitance on boost voltage and increased motor base speed is presented. Simulation and experimental results confirm the effectiveness of the proposed converter.**

Index Terms - **Electric vehicles, neutral-point converter, regenerative braking, switched reluctance motor, voltage-boosting capacitors**

I. Introduction

THE greenhouse effect is a serious environmental problem. Since automobiles are regarded as a major source of greenhouse gases, researchers are oriented towards transportation electrification [1].

Different types of electrical machines are available for electric vehicle (EV) applications [2], [3]. Since the permanent magnet synchronous motor (PMSM) offers a wide torque-speed range with high efficiency and power density, it is considered the first-choice traction motor, as opposed to the squirrel cage induction machine (SCIM). However, supply limitations and escalating rare-earth material prices for the PMSM forced the market to search for suitable alternatives [4]. The switched reluctance motor (SRM) is a dark horse in this arena [5]. It has advantages of a stable, robust and simple structure with low cost. The absence of permanent magnets (which do not produce a mechanically, thermally, and environmentally stable rotor) and copper windings in the rotor allow the motor to operate in harsh environments and at high rotor temperatures [6]. Recent developments in the design of high power SRM for EV are promising [7], [8]. The new designs are competitive with the PMSM with respect to power density, efficiency and torque-speed range [9], [10].

As with the PMSM, the SRM cannot be connected directly to any ac or dc supply but, needs a suitable power converter for its operation. The asymmetric half bridge (AHB) converter based on two switches and two diodes per phase is a popular converter for SRM drives [11-13]. Recent developments in EVs involve increasing the dc link voltage from around 400V to between 600V and 950V [14]. Hence, the voltage rating of the converter must increase. Higher voltage rated power semiconductor devices not only imply slower response with lower overall efficiency but also higher cost and size. Thus, multilevel inverters become a viable solution [15].

In [16], a five-level neutral-point diode-clamped (NPC) converter and an asymmetric modular multilevel converter (MMC) were compared for high voltage, high power applications. However, only the full dc link voltage is utilized. Hence, SRM performance at different voltage levels is not exploited. In [17], a fault tolerant converter based on the NPC topology was proposed. However, the main drawback is half the switches withstand the full dc link voltage. In [18] the performance of a three-level NPC converter was compared with the conventional AHB converter. With the same overall rating, the NPC has the advantage of lower losses and current ripple, and less machine noise. However, motor performance (Nm/kg) is improved only at low speeds (below base speed). Since the SRM can be deployed for high-speed applications, its performance (W/kg) must be enhanced at higher speeds. Also, the NPC converter requires large dc link capacitances.

Enhancing single-phase SRM performance at high speeds is presented in [19], [20]. A boost-capacitor with a parallel diode is inserted in series with the dc link. The boosting-voltage provided by the capacitor aids the winding current to rapidly build-up and decrease thus, increasing the motor base-speed. The application of the boost-capacitor is extended to poly-phase SRM in [21] - [23].

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But the current overlap between incoming and outgoing phases reduces the boosting-voltage effect.

In [24], an MMC drive was proposed for the SRM, where the multilevel voltages reduce torque ripple. Nevertheless, for deploying different voltage levels the number of submodules (SM) increases, thus increasing converter cost. Also in [25], a five-voltage level converter was presented to reduce current noise and torque ripple at low speeds. However, the performance is not improved at speeds at or above base speed. In [26], the authors proposed a fault tolerant converter for SRM drives. Yet, the converter is only suitable for a three-phase SRM. Also four solid-state relays along with two sets of AHBs are required. In [27], a converter with a lower number of switches was studied. However, the converter has poor fault tolerance and is only suitable for six-phase SRM. In [28], a quasi-Z-source converter was presented to improve high speed SRM performance. Nonetheless, the voltages applied to the motor phases are not symmetrical. Also, the converter needs extra active (switches) and passive (bulky inductors and capacitors) elements. But the performance at low speeds is not enhanced. In [29], an improved C-dump converter was proposed to reduce the current tail time by applying twice the negative voltage during turn off. Although, the torque ripple is minimized, SRM power density is not improved since the applied voltage during turn on is the dc link value. In [30], an SRM operated from an AC supply was discussed. The cost of the required converter is not high; however, the motor has lower torque at high speeds, with increased torque ripple.

In this paper, a new asymmetric NPC converter, with inherent voltage boosting, is introduced for a four-phase SRM. The converter uses the double arm, common switch topology for better voltage boosting with a minimum number of switches. In the proposed NPC converter, inter-rail voltage levels are transient (dwelled at for few microseconds, just to ensure switch voltage sharing). Small sized capacitors are deployed instead of the large capacitances normally associated with the conventional NPC converter. The de-magnetization energy of the outgoing phase is stored in the NPC converter split dc link capacitors, hence decreasing the current fall time thereby effectively extending the positive torque production range, before operating in the negative torque region. The stored energy (which increases the dc link voltage) then feeds the next incoming phase, thus allowing faster current build-up which increases the motor output power. The new converter also allows regeneration energy to be fed back to the supply, instead of being dissipated, for rapid machine regenerative braking, thus increasing overall drive efficiency.

The paper is organized as follows. Section II highlights salient SRM features, including voltage and torque equations. Section III proposes a new NPC converter with inherent voltage-boosting capacitors and discusses the different converter modes of operation. A detailed method for sizing the boost capacitors is presented in section IV. Simulation results in section V are confirmed by experimentation in section VI. Three machine types (SRM, SCIM, and PMSM) are compared in section VII, based on their typical relative torque and power, to weight ratios. Conclusions form section VIII.

II. SRM OPERATION

In order to design a unified SRM drive, SRM operation needs to be briefly considered so as to elicit converter needs. The SRM is a double salient machine with a concentrated winding on each stator pole [31]. Air gap reluctance dominates the unaligned reluctance resulting in linear flux linkage λ versus current i characteristics. But core reluctance cannot be neglected in the aligned position whence the λ-i characteristics become non-linear. Torque is produced by the tendency of the rotor poles to align with excited stator poles thus, minimizing flux path reluctance. Torque production is defined by [23]:

$$T = \tfrac{1}{2} i^2 \frac{\partial L(\theta, i)}{\partial \theta} \quad (1)$$

where θ is rotor position.

Equation (1) shows that the developed torque depends on the rate of change of inductance with respect to rotor position as shown in Fig. 1, where θ_r is the rotor pole pitch and β_s, β_r are the stator and rotor pole arcs, respectively.

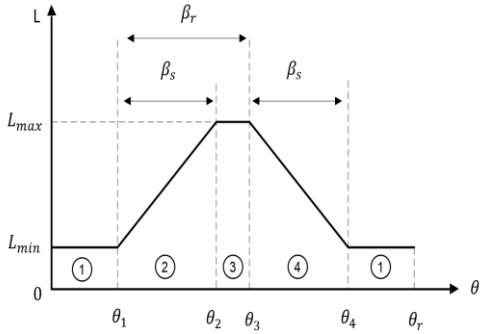


Fig. 1 SRM inductance profile.

The voltage equation [23], neglecting phase mutual effects, in terms of rotor speed ω is:

$$V_{DC} = iR + L(\theta, i)\frac{di}{dt} + i\omega \frac{dL(\theta, i)}{d\theta} \quad (2)$$

where V_{DC} is applied voltage and R is phase winding resistance.

III. ASYMMETRIC NPC CONVERTER WITH VOLTAGE-BOOSTING CAPACITORS

Fig. 2a shows a prior art asymmetric converter for a four-phase SRM [32]. The converter uses the double bridge topology with phases A and C in one bridge, sharing a common leg incorporating switch S_{AC}. The other two phases, B and D, are in an independent bridge with a common switch S_{BD}. The dc link blocking diodes and capacitors allow boosting of the dc link voltage by forcing recovered current to charge the capacitors to voltages in excess of the dc source V_{DC}. The two-independent bridge topology allows better voltage boosting (since no phase overlap occurs in each bridge) with a minimal number of switches. The dc link switch S_{xy} (and diodes D_{x1} and D_{y1}) is for regeneration.

Fig. 2b shows the new asymmetric NPC converter for a four-phase SRM, based on the topology in Fig. 2a. The NPC converter switch voltage clamping feature is used to exploit the series connection of switches. When changing switch states, the NPC rule of an outer switch is always first off and last on, is retained. The analysis of this converter in the motoring and braking modes is presented in the following subsections.

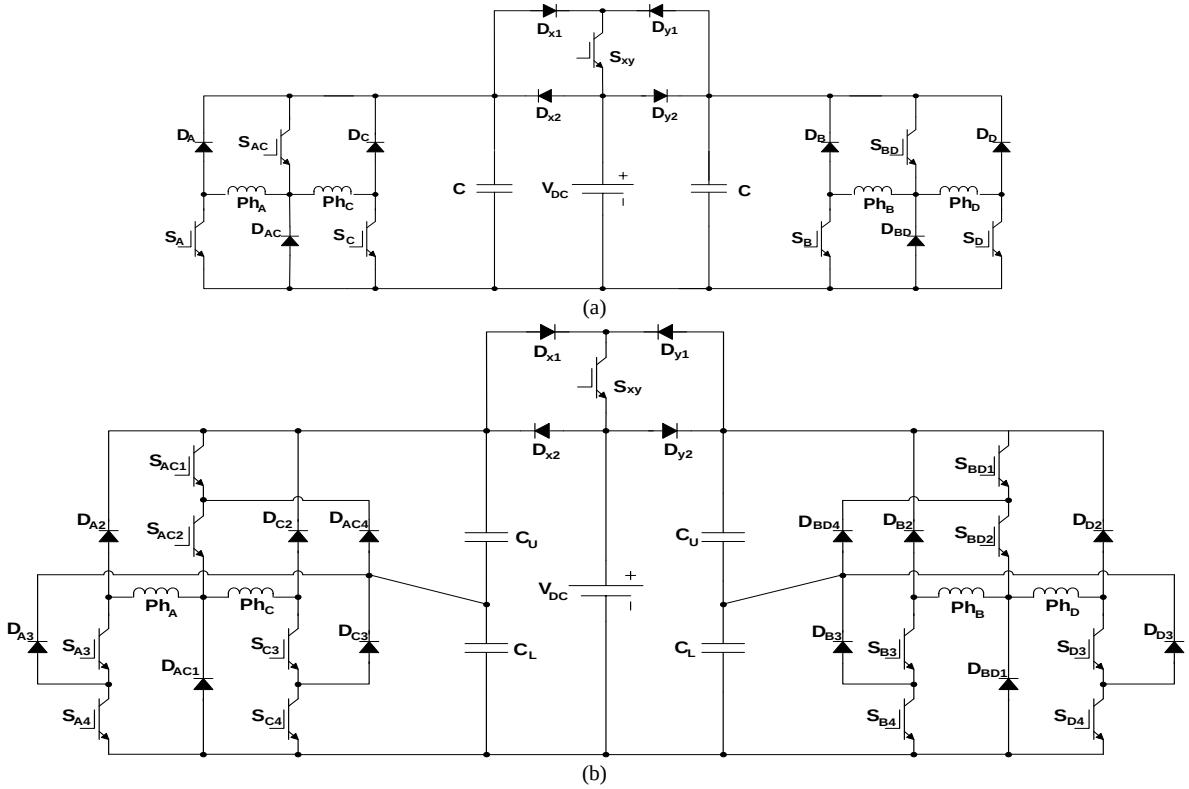


Fig. 2 SRM 8/6 converters with dc link capacitor voltage boosting: (a) prior art asymmetrical and (b) new asymmetrical NPC topologies.

A Motoring Mode

In the motoring mode of operation, the dc link switch S_{xy} is off and link diodes D_{x2} and D_{y2} conduct. Current is injected into the appropriate phase winding during the increasing inductance region for motoring action. According to the states of the phase switches, the converter offers five voltage levels, as shown in Fig. 3 and described in the following text for a given phase, e.g. Ph_A.

First voltage level, $+V_{DC}$*:* This voltage level is obtained by turning on the four switches S_1, S_2, S_3 and S_4 of the phase to be energized as shown in Fig. 3a. Any capacitor boosting effect helps the current in the phase winding to build up quickly reaching the desired reference value, thus increasing the motor output power. The dc link capacitors discharge so that the voltage on the motor winding equals the dc source voltage V_{DC}.

Second voltage level, $+½V_{DC}$*:* The second voltage level is realized by two possible switch combinations. The first is with S_1, S_2 and S_3 on while S_4 is off. The second combination is with S_2, S_3 and S_4 on with S_1 off. These two states are demonstrated in Fig. 3 parts b and c, respectively. Assuming that the boost capacitors are discharged to the link voltage source, only half the dc link voltage $+½V_{DC}$ is applied on the phase winding. This is a transient state and alternation between these two states enables NPC capacitor voltage balancing.

Third voltage level, $0V$*:* Three switch patterns are possible for this voltage level. The first pattern is S_1 and S_2 on while the other two switches, S_3 and S_4, are off. The second pattern is S_2 and S_3 on with S_1 and S_4 off. The final pattern is S_3 and S_4 on while the other two switches S_1 and S_2 are off. The three possible patterns are illustrated in Fig. 3 parts d, e and f respectively, where zero voltage is applied across the phase winding. The dc link capacitors are unaffected.

Fourth voltage level, $-½V_{DC}$*:* This voltage level involves two switch patterns. The first pattern is S_2 on while the other three switches S_1, S_3 and S_4 are off. The second pattern is S_3 on while S_1, S_2 and S_4 are off. Fig. 3 parts g and h illustrate the two patterns, where $-½V_{DC}$ is applied across the phase winding and alternation between the two patterns enables capacitor voltage balancing. This transient state ensures switch voltage sharing.

Fifth voltage level, $-V_{DC}$*:* The last voltage level is with all the switches S_1, S_2, S_3 and S_4 off, as shown in Fig. 3i. The de-magnetization energy via the motor winding charges the dc link capacitors in series, reducing the winding current to zero before the phase enters the negative torque production region.

Table I summarizes the possible voltage levels of the proposed converter, where alternation of the transient half voltage states $±½V_{DC}$ allows dc link capacitor voltage balancing. Table II summarizes the sequence of states during motoring below and above base speed and during regeneration. The half voltage states are transitional, and dwelling is long enough to ensure switch voltage clamping (sharing). The allowable state transitions are shown in Fig.4.

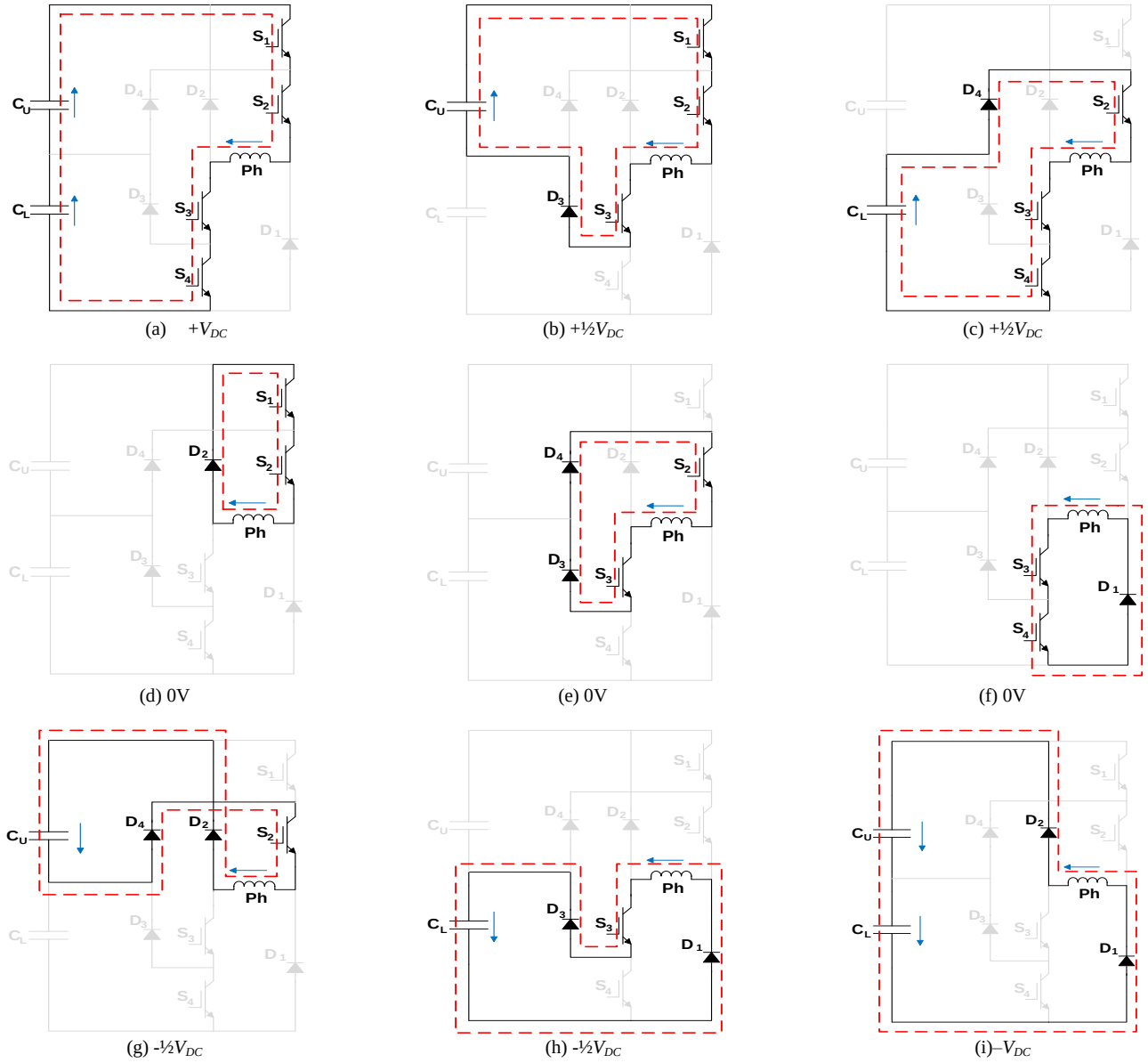


Fig. 3 Voltage levels of the converter in motoring mode (without boost voltage):
(a) First level, $+V_{DC}$, (b) and (c) Second level $+½V_{DC}$, (d), (e) and (f) Third level, 0V, (g) and (h) Fourth level, $-½V_{DC}$, and (i) Fifth level $-V_{DC}$.

TABLE II
NPC CONVERTER OUTPUT VOLTAGE STATE SEQUENCES

Two Quadrant Operation (one direction of rotation)						
	Increasing L Motoring with S_{xy} off			Decreasing L Braking/Regenerating with S_{xy} on when $V_{boost} = 0$		
	First +V	Center +V and 0V	Pulse End -V	First +V (energizing)	Center -V and 0V	Pulse End -V
Below base speed	Δ⇒*0V*⇒+V Δ⇒*(e)*⇒(a)	+V→*½V*→0V→*½V*→+V (a)→*(b)*→**(d)**→*(b)*→(a) alternating with (a)→*(c)*→**(f)**→*(c)*→(a)	0V→*-½V*→-V (d)→*(g)*→(i) or (f)→*(h)*→(i) +V⇒*0V*⇒-V (a) ⇒*(e)*⇒(i)	Δ⇒*0V*⇒+V Δ⇒*(e)*⇒(a) then +V→*½V*→0V (a)→*(b)*→**(d)** (a)→*(b)*→**(f)**	-V→*-½V*→0V→*-½V*→0V (i)→*(g)*→**(d)**→*(g)*→(i) alternating with (i)→*(h)*→**(f)**→*(h)*→(i)	0V→*-½V*→-V (d)→*(g)*→(i) or (f)→*(h)*→(i) -V (i)
Above base speed	Δ⇒*0V*⇒+V Δ⇒*(e)*⇒ (a)	na	V⇒*0V*⇒*-V* (a)⇒*(e)*⇒(i)	Δ⇒*0V*⇒+V Δ⇒*(e)*⇒ (a)	na	V⇒*0V*⇒*-V* (a)⇒*(e)*⇒(i)

States in brackets – as per figure 3
Δ is tri-state, all switches off, state (i)
→ single state changed
⇒ two states simultaneously changed
When changing switch states, an outer switch is always first off and last on
Dwell state (always for ±½V), <1μs, state is shown in italics
bold state – one of two alternating states

TABLE I
PROPOSED NPC CONVERTER OUTPUT VOLTAGE STATES

Level	Fig 3 state	State/KVL	dc link initial voltage	dc link final voltage	Capacitor voltage
$+V_{DC}$	3(a)	$S_3, S_4, C_L, C_U, S_1, S_2$	$+V_{DC} + V_{Boo}$	$+V_{DC}$	$C_U\downarrow$ $C_L\downarrow$
$+½V_{DC}$	3(b) 3(c)	S_3, D_3, C_U, S_1, S_2 S_3, S_4, C_L, D_4, S_2	V_{DC}	V_{DC}	$C_U\downarrow$ $C_L\uparrow$ $C_U\uparrow$ $C_L\downarrow$
$0V$	3(d) 3(e) 3(f)	D_2, S_1, S_2 S_3, D_3, D_4, S_2 S_3, S_4, D_1	V_{DC}	V_{DC}	$C_U\leftrightarrow$ $C_L\leftrightarrow$
$-½V_{DC}$	3(g) 3(h)	D_2, C_U, D_4, S_2 S_3, D_3, C_L, D_1	V_{DC}	V_{DC}	$C_U\uparrow C_L\downarrow$ $C_U\downarrow$ $C_L\uparrow$
$-V_{DC}$	3(i)	D_2, C_U, C_L, D_1	V_{DC}	$V_{DC} + V_{Boosi}$	$C_U\uparrow$ $C_L\uparrow$

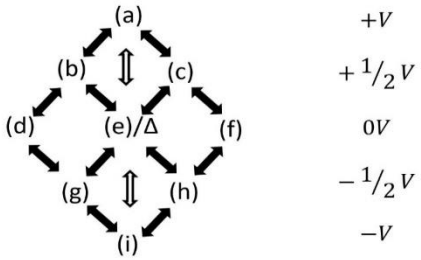


Fig. 4 Converter switch states and allowable single and simultaneous double state transitions.

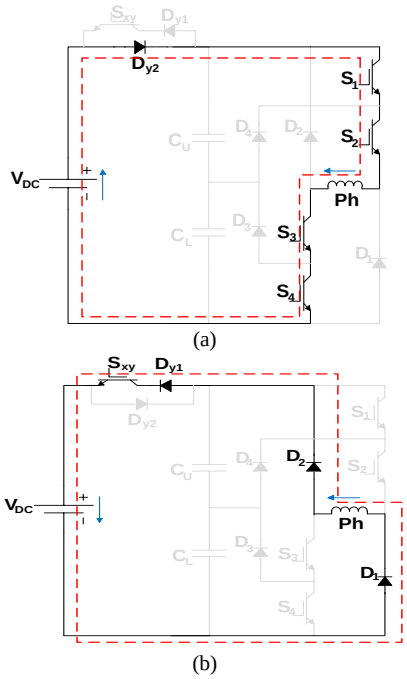


Fig. 5 Regenerative braking mode: (a) Magnetization and (b) de-magnetization.

B Braking (regeneration) mode

Any current in a phase during the decreasing inductance period (region 4 in Fig. 1) produces a negative (reversing) torque. Current is injected into the phase winding with all switches S_1, S_2, S_3 and S_4 on (Fig. 5a which is similar to state 3(a) but the dc link capacitors are not involved) after the start of region 3, before the decreasing inductance region 4, thus producing negative (reverse hence braking) torque in region 4. In this mode, the dc link switch S_{xy} is turned on after the boost capacitors discharge to V_{DC}. By turning off all four switches, (the state in Fig 5b, which is similar to state 3(i), except the dc link capacitors are not involved), before the end of period 4, braking with regeneration occurs, with current back into the V_{DC} via the dc link switch S_{xy} and diodes D_{x1} and D_{y1}. The braking (current) requirement and limit is controlled by interposing zero voltage states, 3(d), (e), (f), within the -V state. The current should reach zero before the start of the increasing inductance, region 2. Stored energy in the motor associated with that pole is fed back to the dc supply thus providing efficient and fast regenerative braking action, without the voltage on each boost capacitor increasing above $½V_{DC}$. Fig. 5 shows converter operation in the braking mode (zero voltage states are Fig. 3 (d) (e) (f)). Regenerative braking does not involve the boost capacitors, so is as for any SRM four quadrant drive. At low speeds, machine regenerative braking is not particularly effective (energy is related to speed squared), and any current associated with unwanted positive torque production should be reduced to zero. Braking down to and at standstill, necessitates a reverse rotation demand, where dc source energy is drawn, viz., braking without regeneration.

IV. SIZING OF BOOST CAPACITORS

Each dc link capacitor voltage rating is half the maximum dc link voltage expected after boosting. The dc link capacitance in this application is not based on the normal NPC converter requirement of providing full load energy at the intermediate voltage levels $\pm ½V_{DC}$. Capacitance is based on the boosting property of the proposed topology. Relatively low capacitance will result in an excessive over voltage, necessitating higher voltage rated devices. Relatively large capacitance results in no significant boost voltage (as with the conventional NPC converter). In [19], a formula provides sizing of the boost-capacitor. However, SRM magnetic non-linearity is neglected, with a linear model being adopted. In [22] and [23], no direct formula is presented to size the boost-capacitor. Also, phase-current overlap crucially affects boosting behavior. In the following section, a design approach for sizing the boost capacitors is presented that accounts for SRM magnetic non-linearity. The proposed double arm topology eliminates the problem of phase-current overlap. Fig. 6 shows an *RLC* circuit modeling the SRM during de-magnetization at the end of the torque producing period.

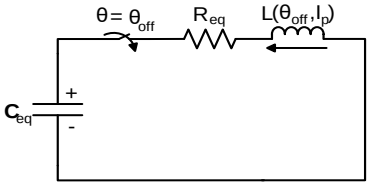


Fig. 6 Equivalent *RLC* circuit for the NPC based SRM drive during the de-magnetization period.

The equivalent capacitor initial voltage at the beginning of the de-magnetization period is the dc link voltage V_{DC}, while the initial current in the phase winding is given by [13]:

$$I_p = \frac{P}{m\eta k_d V_{DC}} \tag{3}$$

where P is the motor power, m is the number of phases conducting simultaneously, η is the motor efficiency, and k_d is the duty cycle.

The equivalent resistance and capacitance are calculated using (4) and (5) respectively.

$$R_{eq} = R + \omega_{rated}\frac{dL(\theta_{off}, I_p)}{d\theta} \quad (4)$$

$$C_{eq} = ½\, C \quad (5)$$

The phase inductance is defined by (6) which accounts for SRM magnetic non-linearity [33].

$$L(\theta, i) = L_0(i) + L_1(i)\cos(N_r\theta) + L_2(i)\cos(2N_r\theta) \quad (6)$$

The coefficients $L_0(i), L_1(i)$ and $L_2(i)$ are defined by:

$$L_0(i) = ½\{½(L_a(i) + L_u) + L_m(i)\} \quad (7)$$

$$L_1(i) = ½\{L_a(i) - L_u\} \quad (8)$$

$$L_2(i) = ½\{½(L_a(i) + L_u) - L_m(i)\} \quad (9)$$

where

L_u is the unaligned inductance - current independent.

$L_a(i)$ is the aligned inductance - calculated at current I_p.

$L_m(i)$ is the halfway inductance - calculated at current I_p.

The inductance values can be calculated using FEA or experimentally.

Applying KVL for the *RLC* circuit in Fig. 6, assuming constant inductance at the instant of phase turn off:

$$R_{eq}i + L\frac{di}{dt} + \frac{1}{C_{eq}}\int_{-\infty}^{t} idt = 0 \quad (10)$$

with the initial condition given by (11) and (12):

$$i(\theta_{off}) = I_p \quad (11)$$

$$\frac{di}{dt}(\theta_{off}) = -\frac{1}{L}(R_{eq}I_p + V_{DC}) \quad (12)$$

The current expression is defined by (13) for the overdamped case (normally $C_{eq} > \frac{4L}{R_{eq}^2}$).

$$i(t) = A_1 e^{p_1 t} + A_2 e^{p_2 t} \quad (13)$$

where p_1 and p_2 represent the poles of the characteristic equation, defined by:

$$p_{1,2} = -\frac{R_{eq}}{2L} \pm \sqrt{\left(\frac{R_{eq}}{2L}\right)^2 - \frac{1}{LC_{eq}}} \quad (14)$$

Using the initial conditions, A_1 and A_2 are defined by (15) and (16) respectively:

$$A_1 = \frac{I_p\left(p_2 + \frac{R_{eq}}{L}\right) + \frac{V_{DC}}{L}}{p_2 - p_1} \quad (15)$$

$$A_2 = \frac{I_p\left(p_1 + \frac{R_{eq}}{L}\right) + \frac{V_{DC}}{L}}{p_1 - p_2} \quad (16)$$

The time for the motor winding current to decay, is denoted by t_{off} and calculated using:

$$t_{off} = \frac{\ln\left(-\frac{A_2}{A_1}\right)}{p_1 - p_2} \quad (17)$$

When the current in the motor winding decays to zero after time t_{off}, the voltage on the capacitor $V_{cap}(= V_{DC} + V_{boost})$ is:

$$V_{cap}(t = t_{off}) = \frac{1}{C_{eq}}\left(\frac{A_1}{p_1}e^{p_1 t_{off}} + \frac{A_2}{p_2}e^{p_2 t_{off}}\right) \quad (18)$$

Solving (18), the boost capacitance is determined in terms of the boost voltage (dc link voltage in excess of V_{DC}).

The scope of the paper is to exploit the series connection of switches. However, taking advantage of the multilevel feature allows reduced current ripple, hence noise, especially at low speeds. In this case, the capacitance should be adequate to supply energy to the motor phase. Equation (19) describes capacitor voltage ripple.

$$i = C\frac{\Delta V}{\Delta t} \quad (19)$$

To allow 5% voltage ripple, the capacitance should be:

$$C = \frac{I_p}{0.05 V_{DC} f_s} \quad (20)$$

where f_s is the sampling frequency.

Equations (18) and (20) could be used to size the capacitor to improved performance at both low and high speeds.

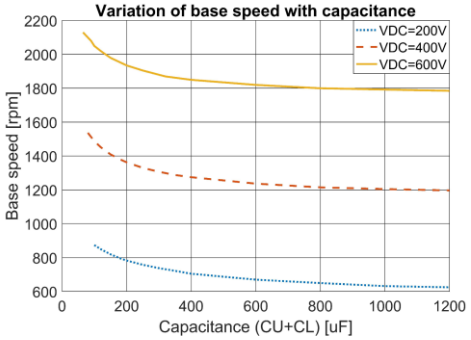
V. SIMULATION RESULTS

The SRM specifications used in the FEA and MATLAB\Simulink simulations are given in Table III.

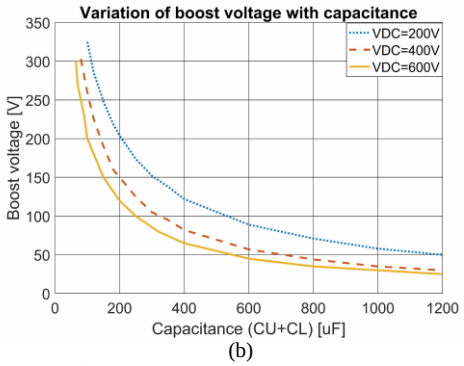
TABLE III
SPECIFICATIONS OF SRM

Parameter	Value
No. of motor phases *m*	4
Stator/rotor poles N_s/N_r	8/6
Number of turns per pole *N*	90
Phase resistance *R*	0.8Ω
Motor axial length	155mm
Shaft radius	15mm
Rotor outer radius	45mm
Thickness of rotor yoke	15mm
Ratio of rotor pole arc to pole pitch	0.35
Length of air gap	1mm
Stator inner radius	46mm
Stator outer radius	83mm
Thickness of stator yoke	12mm
Ratio of stator pole arc to pole pitch	0.42

The sampling frequency used for simulation is 20kHz, and the motor drives a constant load of 25Nm. Fig. 7 shows the variation of base-speed and boost-voltage with dc link capacitance (upper + lower capacitance for one arm) at different dc link voltages. The motor base-speed and hence output power (power = torque x speed) increase using boost capacitors.



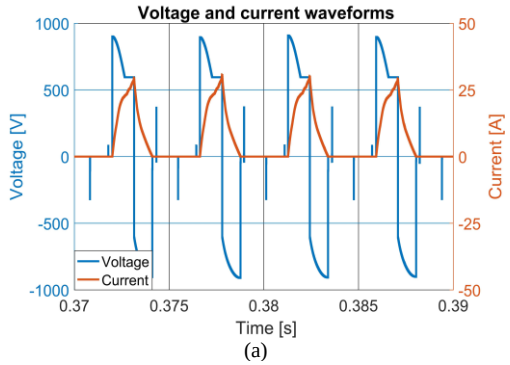
(a)



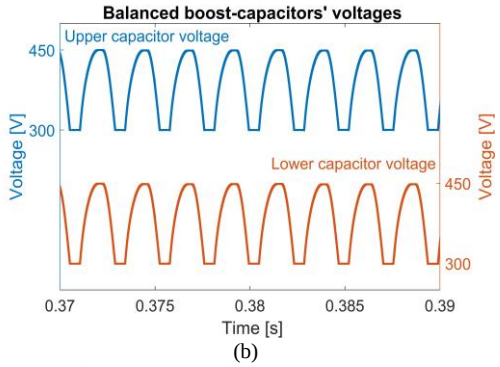
(b)

Fig. 7 Variation of (a) base-speed and (b) boost-voltage with capacitance.

For 300V boost-voltage, based on Fig. 7, 65µF, >450V dc capacitors are selected. The dc source voltage is fixed to 600V. The voltage and current waveforms for one motor phase using the selected capacitor are shown in Fig. 8a and the balanced boost-capacitor voltages are shown in Fig. 8b. Because two phases share a common converter leg, at $\frac{1}{2}V_{DC}$ states, small currents flow in the decreasing inductance regions.



(a)



(b)

Fig. 8 SRM waveforms with 65µF boost-capacitors: (a) phase voltage and current at base speed and (b) boost-capacitors, C_U and C_L voltages.

Fig. 9 shows the voltage and current waveforms below base speed, at 1825rpm. Half the dc link voltage $+\frac{1}{2}V_{DC}$ (which is alternated between states 3(b) and 3(c)) is used only for <1µs as a transient state to ensure voltage sharing between phase switches thus the clamping diodes D_3 and D_4 are only transient current rated if switch state (e) is not employed. The PWM adopted in this control strategy uses only 0% and 100% duty cycles for the switches which enables the sampling (phase current) frequency to be twice the switching frequency for more accurate operation with lower switching losses and current ripple noise. Device losses are symmetrical about the central leg (but not uniformly distributed). Capacitor balancing takes precedence over alternating of the $\pm\frac{1}{2}V_{DC}$ states. Any significant capacitor $\pm\frac{1}{2}V_{DC}$ state bias is compensated by adjustment of delay time or by advancing or retarding of the switch state demand.

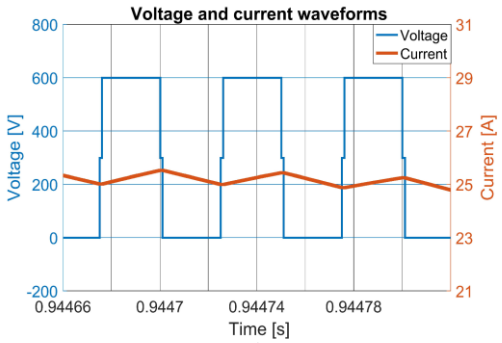


Fig. 9 Phase voltage and current waveforms during excitation at low speed.

The SRM torque/speed and output power/speed characteristics with and without boost-capacitors are shown in Fig. 10. Below base speed, current chopping control is applied for constant torque operation. Above base speed, the advance angle control method is employed for constant power operation. The proposed voltage-boosting method increases the motor base speed from 1735rpm to 2130rpm, giving a 23% increase in the output power (W/kg) at base speed. The machine power density has improved which allows the SRM to compete with PMSM.

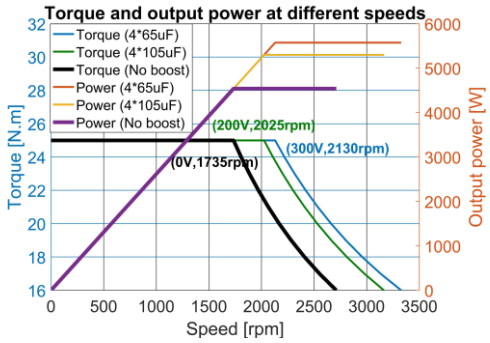
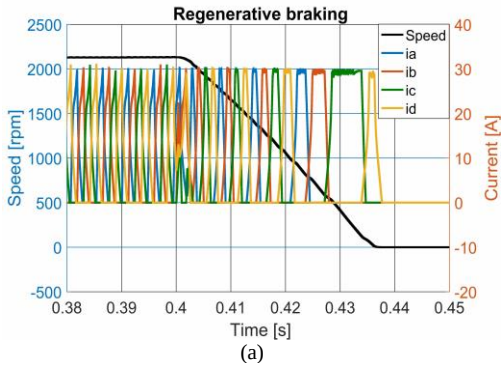


Fig. 10 Torque/speed and power/speed characteristics

To assess braking mode performance, the SRM is motored for 0.4s with current injected in the rising inductance region. After receiving a braking command all the phases are briefly turned on simultaneously to allow the boost capacitors to completely discharge into the machine and then all the switches are turned off until the current decays. Current is

then injected in the falling inductance region (the phase sequence is reversed) to allow (uncontrolled) regenerative braking as shown in Fig. 11a. Fast and efficient braking action is achieved without dissipating energy (regeneration). The dc supply is disconnected after the motor comes to rest, otherwise the motor will rotate in opposite direction (reverse). Since the SRM back emf is negative when current is injected in the falling inductance region ($\partial L/\partial\theta < 0$), a soft chopping current control mode (0V, -V) is applied during motor braking instead of hard chopping current control (+V, -V) as shown in Fig. 11b to minimize switching losses during braking.



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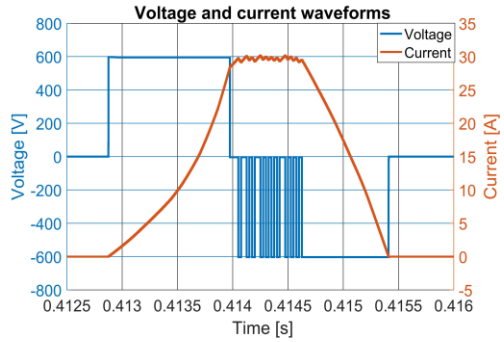


(b)

Fig. 11. (a) Regenerative braking and (b) Voltage and current waveforms during regenerative braking (soft chopping).

VI. EXPERIMENTAL RESULTS

The specifications of the 8/6 SRM, used for experimentation, are given in Table III and Fig. 12 shows the test rig.

A dc source voltage of 100V is utilized, the boosting capacitors are 75μF (±10%), and the sampling frequency is 20 kHz. The effect of voltage boosting on SRM performance is compared in two different cases; single pulse mode and current chopping mode. Fig. 13 shows the phase voltage, current, capacitor voltages, instantaneous torque and speed, in each case. Below base speed (that is, current chopping mode), where the torque is constant, the speed is controlled by adjusting the phase reference current. Allowing the current to build up quickly enables the SRM to operate at higher speed. Fig. 13a shows SRM performance without voltage boosting, where the phase voltage is equal to the dc link voltage, while the capacitor voltages are maintained at half the dc link voltage. Since the available dc link (source) voltage (without boost) is insufficient for the current to build up quickly, the speed is only 165 rpm.

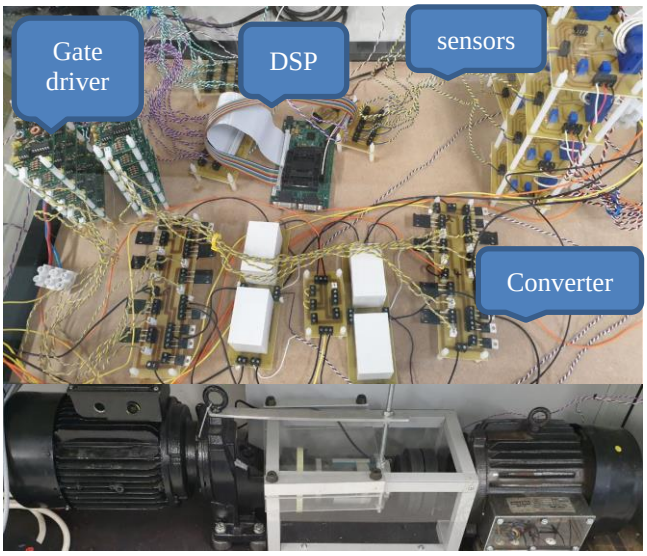
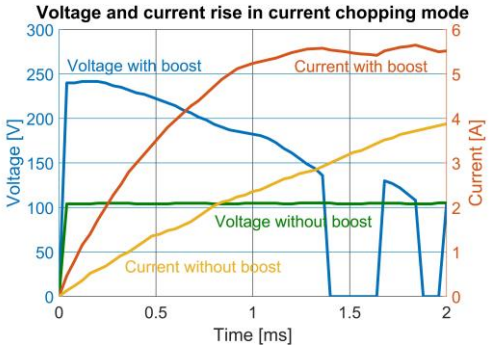


Fig. 12 Experimental test rig

Fig. 13b proves that the performance of the motor in the current chopping mode is enhanced, since the phase voltage is equal to the dc source voltage (battery) plus boost voltage. The extra voltage supplied by the boost capacitors allows fast current build-up. The speed increases to 290 rpm at the same load torque. A 1μs dwell is applied when turning on/off the outer/inner switches to assure equal voltage stress on the switches as presented in Fig. 13b. Above base speed, the speed is controlled by adjusting the turn on/off angles and the SRM operates in the constant power region. Fig. 13 parts c and d show SRM performance without and with boosting voltage respectively. The extra voltage offered by the boost capacitors allows the current of the incoming phase to build up quickly, thus quickly increasing the motor speed from 380 rpm to 660 rpm at the same load torque. Also, the outgoing phase current decays faster in the presence of the increasing boost-voltage. The exaggerated improvement in the motor speed obtained experimentally (around 75%) is due to the accentuated boost voltage compared to dc source voltage. To emphasize the importance of voltage boosting on current build up, the rise time of phase current with/without voltage boosting for the two cases; current chopping mode and single pulse mode, is presented in Fig. 14 parts a and b respectively.



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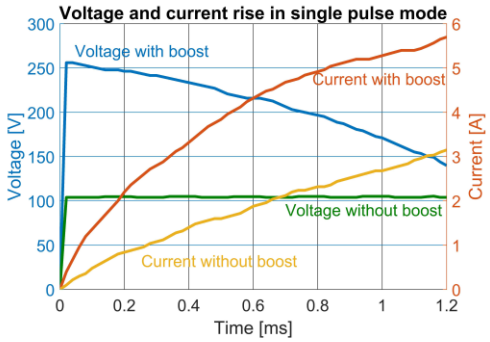
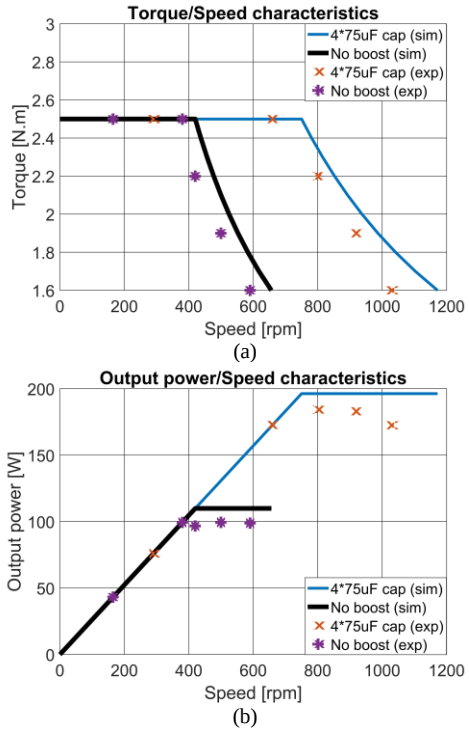


(b)

Fig. 14 Experimental voltage and current rise time: (a) current chopping mode (with and without voltage boosting) and (b) single pulse mode (with and without voltage boosting)

The simulated and experimental torque/speed characteristics are compared in Fig. 15a, while Fig. 15b shows the simulated and experimental output power. The effect of a boosting-voltage is shown to have significant effect on the motor base-speed, meaning the rated torque region is extended, with a corresponding increase in output power. The slight deviation between the experimental and simulated results is due to the modelling of the SRM using FEA along with ignoring machine core loss.



(a)

(b)

Fig. 15 Experimental versus simulated characteristics with and without dc link voltage boosting: (a) torque/speed and (b) output power/speed.

VII. MACHINE PERFORMANCE COMPARISON

Three machine types (SRM, SCIM, and PMSM) are compared in Table IV, based on their typical relative torque and power, to weight ratios [34]. In Table IV, the SRM has the highest torque to weight ratio, but the power to weight ratio suffers because of a compromised base speed due to the inability to force sufficient current into (or from) the machine at higher speeds (power = torque x speed). DC rail voltage boost (140%) increases the speed at which FLT can be delivered (from 420rpm to 750rpm), hence improving the power to weight ratio (by 75%) to be better than that of a PMSM, for a given source voltage. The NPC converter approach allows series connection of fast low-voltage (600/650V) switches. Hence a device switching frequency well in excess of 20kHz is possible. With alternating zero-volt loops, the load switching frequency is doubled to in excess of 40 kHz, hence minimizing current ripple below base speed and the switching frequency noise is above human audible levels. Below base speed, commutation current profiling can be used to minimize rotational torque ripple between commutating poles hence minimize mechanical audible noise (at multiples of the rotational speed). Radial torque (resonance) ripple (chirp noise at multiples of the rotational speed), due air gap asymmetry and stator compression, at phase commutation is reduced by the necessity of the half voltage (and zero voltage) state during voltage transitions, judiciously synchronized to produce a cancelling counter resonance (being mechanical, the excited frequency is independent of rotor speed).

TABLE IV
RELATIVE PERFORMANCE OF THREE MACHINE TYPES

Relative pu	PMSM	SCIM	SRM	SRM + Boost
Torque $\left(N.m/kg\right)$	0.8	0.8	1.0	1.0/1.0
Power $\left(W/kg\right)$	1.0	0.8	0.8	0.93/0.98
SRM power to weight ratio: 200V boost → 0.93pu, 300V boost → 0.98pu				

IV. CONCLUSION

A novel asymmetric NPC converter with inherent dc link voltage-boosting capacitors for a four-phase SRM drive was presented. Analysis of the proposed converter during motoring and braking resulted in a design approach for sizing the boost capacitors. The proposed converter improves SRM drive performance at low and high speeds. The boost voltage increases the motor base speed, hence output power and efficiency. The power to weight ratio of the SRM with voltage boosting capability is competitive with the PMSM and has the advantage of a higher torque to weight ratio. Regenerative braking can be deployed for efficient and fast braking action. The new converter allows series connection of fast, low-voltage, efficient switches. Topology penalties are increased number of gate drives and increased control complexity when introducing NPC intermediate dwell states.

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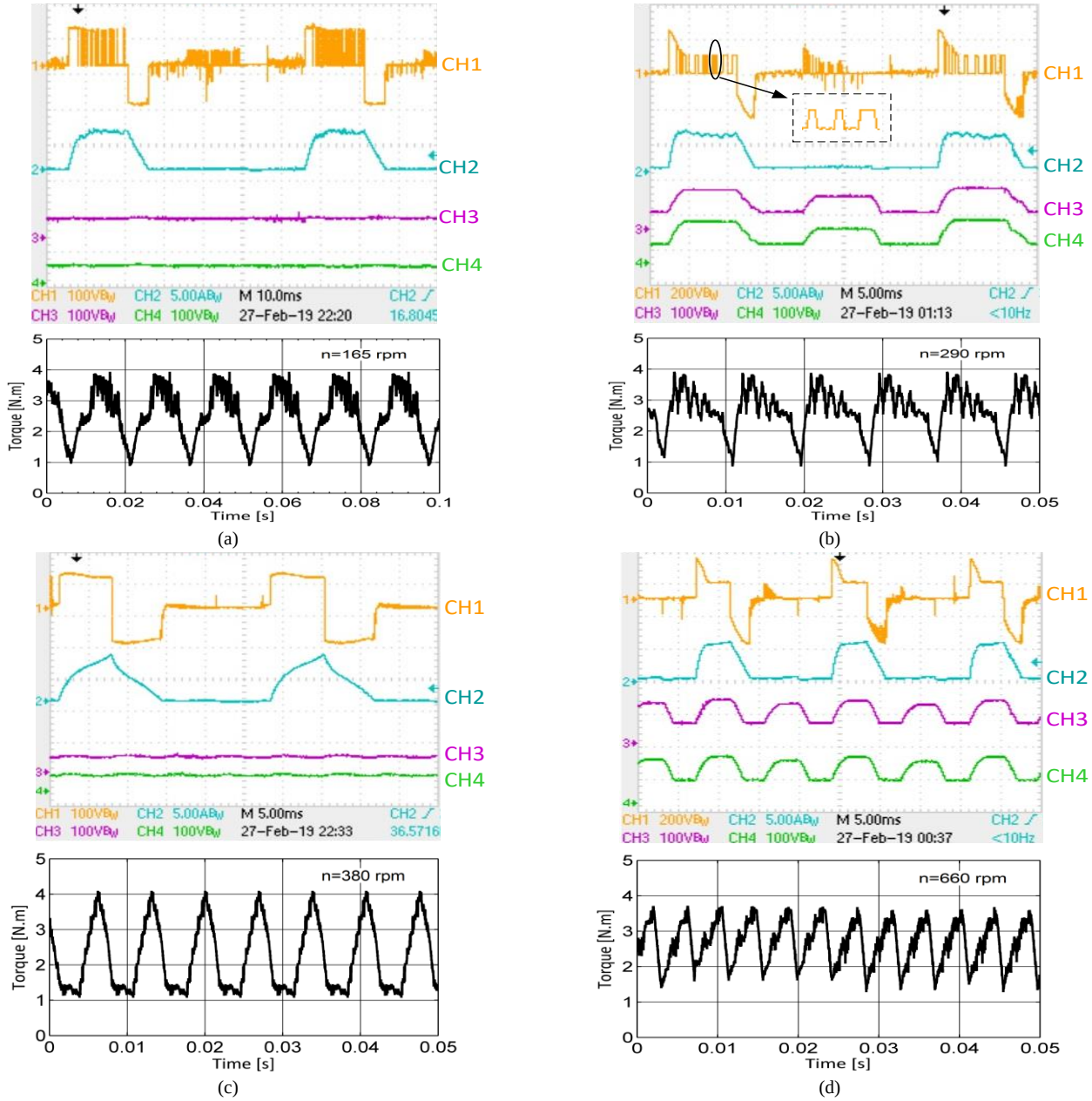

Fig. 13. Experimental results: current chopping mode (a) without voltage boosting and (b) with boost-capacitors, single pulse mode (c) without voltage boosting, and (d) with boost-capacitors. Phase voltage (CH1), phase current (CH2), upper capacitor voltage (CH3), lower capacitor voltage (CH4), and instantaneous torque.

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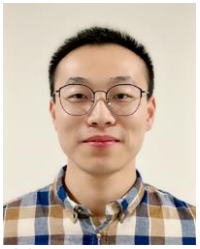

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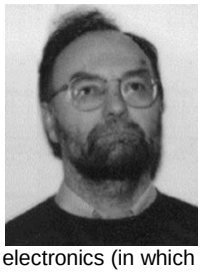

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