A Novel Converter Station Structure for Improving Multi-Terminal HVDC System Resiliency against AC and DC Faults

Shuren Wang, *Student Member, IEEE,* Khaled H. Ahmed, *Senior Member, IEEE,*
Grain P. Adam, *Member, IEEE,* Ahmed M. Massoud, *Senior Member, IEEE,* and Barry W. Williams

***Abstract*—In an effort to minimize the power disruption between a dc grid and ac grids that host power converters during ac and dc network faults, this paper proposes a novel converter station structure to improve ac and dc fault ride-through performance of the multi-terminal HVDC grid. The proposed structure consists of two independent ac and dc interfacing circuits, which are a half-bridge modular multilevel converter and a cascaded H-bridge (CHB) based energy storage system. Taking the advantages of high controllability and flexibility of the independent CHB converter and ease of integrating energy modules, a decoupled power relationship between the ac and dc sides is achieved, which is important for enhancing ac and dc fault performance. Operation of the proposed converter station under normal conditions and during ac and dc faults is explained, with the control system presented. Simulation validation of the proposed structure on a three-terminal HVDC grid confirms the enhanced performance, including the continuous operation during ac and dc faults with negligible power transfer disruption.**

***Index Terms*—Cascaded H-Bridge (CHB), Energy Storage System (ESS), Fault Resiliency, HVDC, Modular Multilevel Converter (MMC).**

Manuscript received Nov 28, 2018; revised May 04, 2019; accepted June 9, 2019. This publication was made possible by NPRP grant NPRP (9-092-2-045) from the Qatar National Research Fund (a member

of Qatar Foundation). The statements made herein are solely the responsibility of the authors. **(Corresponding author: Shuren Wang.)**

I. INTRODUCTION

The controllability and cost-effectiveness that multi-terminal HVDC transmission systems offer to future power systems (particularly, for large power exchange and maximum utilization of renewable energy reserves over wide geographical areas) are the main drivers that attract the research interest in all aspects of voltage-source converters (VSCs) [1]. Considering its significant advantages, the modular multilevel converter (MMC) has become the topology of choice in HVDC applications [2]-[3]. However, resiliency to ac and dc faults is important for reliable operation of multi-terminal HVDC networks.

MMCs are known for the resilience to symmetrical and asymmetrical ac faults, but the collapse of power transfer with the ac grid during ac faults can create significant disturbances in the dc side, viz., over/under voltage and transient power flows. Occurrences of such over/under voltage could lead to the unintended triggering of station protection systems. Some solutions such as the telecommunication-based protection, frequency modulation techniques, and the installation of dc choppers have been investigated to mitigate the impact of ac faults on the dc side [4]. But none of the proposed approaches fully addresses the mentioned technical challenges.

Generally, impacts of the dc fault present major technical barriers that hinder HVDC system interconnection and penetration of multi-terminal dc grids into critical and backbone power corridors of large power systems. The use of unipolar cells makes the half-bridge MMC (HB-MMC) vulnerable to dc faults. Therefore, additional measures (such as protective thyristors to divert some of the fault currents from the freewheeling diodes) are used to extend the time the dc fault can be sustained before dc circuit breakers isolation [5]. The full-bridge MMC (FB-MMC) and its variants (such as the mixed-cell MMC) have the ability to stop or control the fault currents during the dc fault [2], [6]-[8]. Other converters such as alternate

arm converter (AAC) [9] and hybrid cascaded MMC [10], [11] and its two-level version [12], are proposed to block the dc fault. However, these converters suffer from either relatively high semiconductor conduction losses or arm current commutation issues, which hinder the adoption in practical systems. Another attractive protection approach with lower losses is the adoption of dc breakers to interrupt the dc current and isolate the fault point within a few milliseconds [13]-[15]. All the converter and breaker topologies in the literature, which offer dc fault blocking and fault current control, prioritize the protection of converter semiconductor switches and provision of ac grid reactive power support during dc faults. However, such approaches could lead to zero dc/active power transfer between the dc and ac grid throughout the fault duration. And the impacts of active power mismatch due to sudden dc power transfer drop on the frequency and first swing angular stability of connected ac power systems will be exacerbated by declining system inertia, as a large number of synchronous generators are deemed to be displaced by the converter-based renewable energy generation.

Thus, regulating dc power within an HVDC grid is essential for system safe operation when an ac grid fault occurs. Also, mitigating the influence of the temporary power transfer loss, due to major disturbances in other parts of the asynchronous power system or dc grid faults, on the stability of connected ac grids is a necessity to be realized for large multi-terminal dc grids. A number of solutions that employ the shunt-connected energy storage system (ESS) in the ac or dc side, or integrating energy modules (EMs) of supercapacitors or batteries into MMC submodules (SMs), have been proposed, particularly, to enhance system inertial response and frequency stability [16]-[22]. The shunt-connected ESS in the ac side is effective for smoothing the short-duration active (and reactive) power variations of the host ac grid as a result of disturbances in remote asynchronous ac grids [16], [17]. However, it is unable to prevent over/under voltage in the dc side during nearby solid short circuit ac faults. Similarly, the shunt-connected ESS in the dc side can prevent the dc side over/under voltage during severe ac faults, but it is unable to support ac grids during dc faults; especially during sub-transient periods [18], [19]. Thus, two sets of shunt-connected ESSs are needed for both ac and dc side power flow smoothing. An HB-MMC integrated with batteries was investigated to minimize SM

capacitance and regulate the dc voltage during ac low-voltage ride-through operation in [20]. In [21], [22], HB-MMCs with batteries or supercapacitors were investigated as pure ESS for dc transmission. However, the use of HB-SMs compromises dc fault withstanding ability. With the advantage of FB-SMs and the integrated battery EMs, a control method of the hybrid MMC is proposed to regulate power flow continuously in normal and ac/dc fault modes [23]. During the dc fault, ac grid active power is controlled to exchange with the upper and lower arms, which operate as shunt-connected ESSs, where arm voltages and currents have zero offset, while dc current is nullified gradually as the common-mode current of each phase-leg is zero. However, this implementation (based on either FB-MMCs or hybrid MMCs) may be impeded in HVDC applications, as the transient discharge current (caused by the distributed parameters of the dc side long-distance overhead line or cable plus the ac current associated with the regulated active power being exchanged with the ac grid) may pose significant risks to the converter semiconductor switches. Additionally, the degraded special dc/dc converters formed by FB-SMs in ac fault mode are unable to inject reactive power into the ac gird, which is essential from the ac grid protection point of view [23].

Also, the difference between the rated voltage of HVDC-MMC SMs (typically ranging from 1.6kV to 2.8kV) and the battery or supercapacitor stacks (typically ranging from 400V to 850V) presents a technical restriction of integrating EMs into HVDC converters. To overcome this issue, hard and soft switching dc/dc converters are proposed to meet the high voltage requirements and reduce the ESS current ripple, but system complexity and conversion losses are increased [17], [20], [21]. Apart from active interfaces, connecting EMs and MMC SMs through passive interface circuits is desirable in terms of simplicity and efficiency [22].

In order to provide a global solution, this paper proposes a novel and efficient HVDC station structure for the operation of multi-terminal dc grids. This structure employs an HB-MMC in conjunction with an on-demand ESS to achieve enhanced ac and dc fault ride-through capabilities. Both isolation of the fault side and uninterruptable power flow of the normal side can be achieved. The proposed structure offers the following prominent features:

1) Resiliency against dc faults: The structure is capable of preventing the ac grid from contributing fault

current to the fault dc side;

2) Resiliency against ac faults: The structure can provide reactive power support during solid symmetrical and asymmetrical ac faults as expected in all grid codes;
3) Uninterruptable power transmission: The dc power and ac active power handled by the proposed converter station is decoupled. As a result, stability and reliability of connected ac/dc grids are improved as the loss of dc/active power due to dc/ac faults do not lead to power transmission interruption or attenuation;
4) Flexible implementation of ESS integration: The separation of EMs from the MMC-SMs and the introduction of the independent cascaded H-bridge converter (CHB) make integrating the ESS into HVDC systems much easier, without extra circuitry for voltage matching. Additionally, grounding of the ESS becomes feasible;
5) High efficiency: The on-demand feature of the CHB-based ESS is technically attractive as the proposed converter station is basically as efficient as conventional HB-MMC during normal operation; and
6) AC grid support: The structure is able to greatly enhance frequency and voltage support for the host ac grid by operating the HB-MMC together with the CHB-based ESS.

The remainder of this paper is organized as follows. In section II, critical topological configuration and operation principles of such HVDC converter station structure are proposed. Sizing of the ESS is discussed in section III. The corresponding control system for different operation modes is presented in section IV. Section V illustrates simulation results of a three-terminal dc grid, demonstrating the system behavior. Finally, conclusions are summarized in Section VI.

II. Topology and Operation Principles of the Proposed Structure

The main motivation of the proposed structure is to incorporate the on-demand ESSs into an HVDC system to act as buffers which provide/absorb active powers to/from the connected ac grids when the dc voltage collapses during the dc fault; and sink/source dc powers when one or more host ac grid is subjected to the ac

fault. Thus, the negative impacts of the ac/dc fault on the transient stability of connected dc/ac grids, particularly, sudden power mismatch, is avoided. Therefore, autonomous operation is needed to facilitate seamless transition between normal and fault modes for each station within the HVDC system. Meanwhile, station losses should be minimized during long-term normal operation. Unlike a conventional energy storage HVDC system with MMC integrated with EMs, each station converter of the proposed structure comprises an HB-MMC and an independent CHB-based ESS.

A. Topology Description

Fig. 1 displays the station converter topology of the proposed structure. The first stage is a conventional three-phase HB-MMC which is rated at the full power of each station and dc link voltage of the dc grid. It is mainly responsible for transferring power between the dc link and its ac side junction, node M, by synthesizing the ac voltage v_{MMC}. System protection and uninterrupted power transmission in fault cases are mainly realized by the second stage, namely the on-demand ESS, which employs a three-phase CHB converter, where each phase mainly consists of N_{FB} cascaded FB-SMs. To be able to source/sink the rated dc/active power and control the reactive power, the ESS is sized such that its maximum attainable ac voltage is the same as that of the HB-MMC stage. Rather than being shunt-connected, the on-demand ESS is series-connected, linking the HB-MMC ac side (node M) and the grid-interfacing transformer, with the generated ac voltage v_{ESS}. Thus, the following voltage expression holds:

$$v_{MMC} + v_{ESS} = v_C \tag{1}$$

where v_C is the overall converter station synthesized ac voltage.

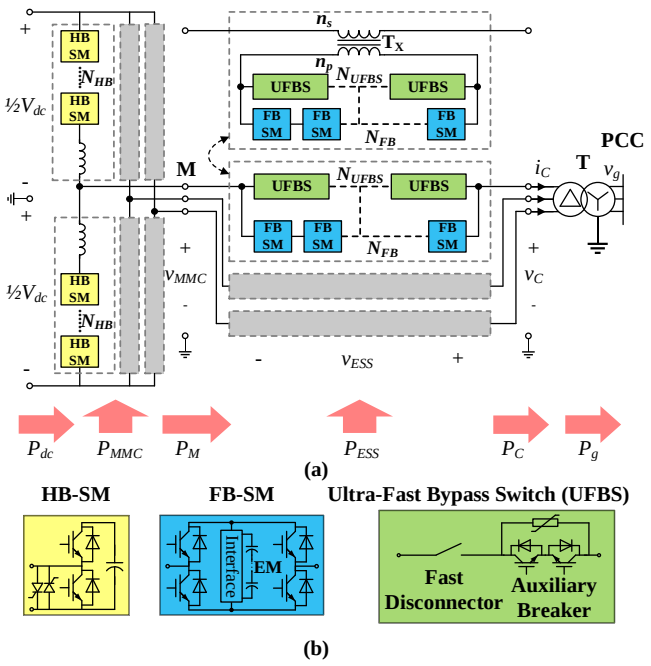


Fig. 1. Topologies of the HVDC station in the proposed structure. (a) HB-MMC and CHB-based ESS with and without transformer. (b) Different power modules.

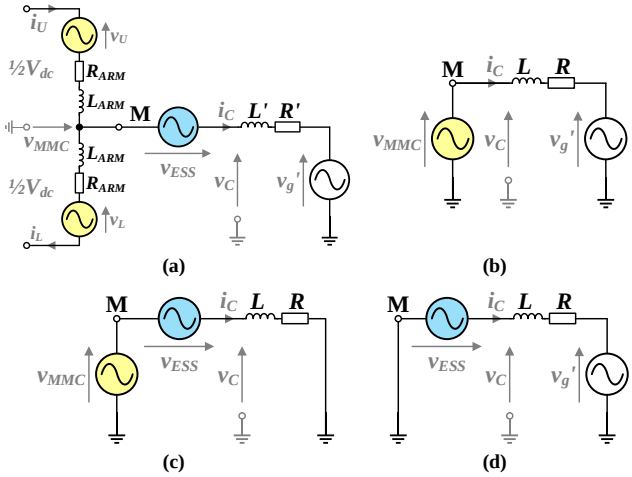


Fig. 2. Single-phase model diagrams of the proposed station structure in different operation modes. (a) Overall model. (b) Normal operation mode. (c) AC fault or boost mode. (d) DC fault mode.

Assuming that HB-MMC SMs and CHB converter FB-SMs have the same rated voltage, the number of IGBTs employed for active power conversion in the proposed structure (the HB-MMC plus the CHB) is equal to that of an FB-MMC, provided that both systems operate with identical rated ac and dc voltages. But the proposed structure of separating the EMs from MMC adds features, such as easier EM voltage leveling and independent operation of HB-MMC and ESS. Fig. 1(a) displays two possible implementations of the on-demand ESS, viz., non-isolated and isolated using the series transformer T_X. For the non-isolated (no

transformer) configuration, to block a solid fault and achieve uninterruptable power transfer, the maximum CHB ac output voltage must be at least equal to $½V_{dc}$, where V_{dc} represents the rated dc voltage of HB-MMC. For the isolated version, the galvanic isolated transformer T_X can be used to reduce the ESS insulation level and to establish bespoke trade-offs between CHB voltage and current ratings when compact design is not a priority. The additional leakage reactance introduced by the T_X has an impact on system performance, therefore, must be considered when designing the control system.

To reduce the continuous operational losses, a dedicated bypassing mechanism is incorporated into the ESS across the CHB FB-SMs, as shown in Fig. 1(a). For faster activation and deactivation times (inserting and bypassing) of the CHB, the on-demand ESS is divided into N_{UFBS} (N_{UFBS} can be much less than N_{FB}) modular units, with each rated at a fraction of the CHB total rated voltage. Thus, each unit is equipped with N_{FB}/N_{UFBS} FB-SMs and a parallel-connected ultra-fast bypass switch (UFBS), as shown in Fig. 1(b). Such modular topological connection is beneficial for UFBSs voltage balancing. As a result, each phase of the on-demand ESS resembles a hybrid dc circuit breaker [15]. The difference is that the circuit breakers of the proposed structure operate in the ac side. During the normal operation, the FB-SM chains can be bypassed by the UFBSs, thus avoiding the semiconductor switching and conduction losses. With the reduced resistance and on-state voltage drop in the bypassing path (mechanical disconnectors, a few IGBTs, and the T_X if configured), the efficiency of the proposed converter station is marginally different from that of a conventional HB-MMC station. Successful current commutation from the UFBS path to the CHB path is critical for the activation of CHB converter. In accordance with the mechanical characteristics in [14], this paper assumes that the total activation time of the on-demand ESS is 2ms.

B. Operation Principles

The overall equivalent circuit of the proposed station converter structure is shown in Fig. 2(a), where L' and R' are the leakage inductance and resistance of the interfacing transformer T (plus the series transformer Tx, if configured) respectively and v_g' is the PCC ac voltage referred through the T. According to Fig. 2(a), the ac and dc circuit loops of one phase-leg of the HB-MMC have the following relationships:

$$\frac{L'}{2}\frac{di_C}{dt}+\frac{R'}{2}i_C+v_{MMC}=\frac{(v_L-v_U)}{2} \quad (2)$$

$$2L_{ARM}\frac{di_{CM}}{dt}+2R_{ARM}i_{CM}=V_{dc}-(v_U+v_L) \quad (3)$$

where $i_C = i_U - i_L$, $i_{CM} = ½(i_U + i_L)$ and i_{CM} is the common-mode current of one phase-leg.

Based on the previous mentioned bypassing mechanism, the converter station equivalent circuit during normal operation is depicted in Fig. 2(b), where according to the HB-MMC ac loop model, $R = ½R_{ARM} + R'$ and $L = ½L_{ARM} + L'$.

When an ac short circuit fault occurs, successful activation of the on-demand ESS will enable its CHB converter to generate an ac voltage with appropriate phase and magnitude relative to those of the HB-MMC and the ac grid to facilitate controlled generation or absorption of the active (and reactive) power that cannot be exchanged with the ac grid due to voltage collapse. Fig. 2(c) depicts the theoretical converter station equivalent circuit during the worst-case ac short circuit fault, with the HB-MMC seeing the ESS as a replacement of the normal ac grid. In this way, the dc power flow (P_{dc}) is uninterrupted, while the station is able to provide reactive power support to the ac grid as well. Also, because of the extra ac voltage offered by the series-connected CHB converter, simultaneous operation of the HB-MMC and the on-demand ESS can increase the maximum ac voltage and capacitive reactive power that the converter station can generate based on (1), which is attractive for the host ac grid.

When a dc short circuit fault occurs, the HB-MMC SMs will be bypassed by the back-to-back protective thyristors, while the on-demand ESS is activated after successful current commutation. The theoretical converter station equivalent circuit during the worst-case dc short circuit fault is shown in Fig. 2(d), where the arm inductors and transformer leakages are parts of the system impedance, L and R, respectively. Long distance dc line inductance and resistance between the dc fault point and the station can also be included. Due to the bipolar output of FB-SMs and the energy stored inside the EMs, the activated ESS replaces the HB-MMC, sourcing or sinking active (and reactive) power during the dc fault period, and the phase and magnitude of the CHB ac voltage must be adjusted relative to those of the ac grid and mode M. Thus, during

a dc fault, the on-demand ESS takes the control over the ac current, including the ac current components that flow through the HB-MMC. As a result, a full control over active and reactive power exchanged with the ac grid is retained. As the upper and lower arm currents of the HB-MMC sum to be zero at the positive and negative dc nodes, the absence of dc components in HB-MMC arm currents will lead to a rapid fall of the dc fault current after bypassing the HB-MMC and activating the on-demand ESS.

From an energy flow point of view, the HB-MMC SM capacitors ideally exchange zero net dc/active power with the dc/ac grid during normal operation ($P_{MMC} = 0$). Accordingly, when converters are assumed to be lossless, the dc power P_{dc} will be transferred to node M of the HB-MMC ac side as the active power P_M. Thus, the ESS acts as a power buffer between P_M and P_C as:

$$P_{dc} = P_M = P_{ESS} + P_C = P_{ESS} + P_g \qquad (4)$$

where, P_C is the converter station active power; P_g is the active power that the converter station exchanges with the ac grid; and P_{ESS} is the active power that the ESS sources/sinks.

Based on the previous discussion, the ac/dc fault resiliency of the proposed structure is revealed in (1), while the power relationship in (4) depicts the uninterruptable power transmission principle. Also, extra functionalities of the activated on-demand ESS can be obtained by the simultaneous operation of HB-MMC and CHB during transient active/reactive power imbalance in the host ac grid.

III. Energy Storage System Sizing

Various existing energy storage technologies such as Lithium-ion batteries and supercapacitors can be used in the EMs of ESS in the proposed converter station due to their suitability for burst power applications [22]-[27]. Generically, ESS sizing includes estimates of the active power rating, stored energy capability and net energy exchanged for a given charge/discharge depth. For the uninterrupted active power transfer (sinking or sourcing) within a finite duration, each EM must be rated at:

$$P_{EM} = \tfrac{1}{3} P_{ESS}/N_{FB} \qquad (5)$$

where P_{EM} is the EM rated active power. Hence, the EM rated current is:

$$I_{EM} = P_{EM}/V_{EM} \tag{6}$$

where V_{EM} is the EM rated voltage.

The minimum EM energy capability is calculated based on the worst-case scenarios such as the three-phase solid ac fault and the pole-to-pole solid dc fault, in which the ESS is required to provide a rated power support for a duration of T_{ESS} ($T_{ESS} = T_2 - T_1$, and must be selected larger than the fault critical times). Therefore, the stored energy per EM (E_{EM}) is quantified as:

$$\begin{aligned} &\frac{dE_{EM}}{dt} = P_{EM} \\ &\Rightarrow \int_{E_{EM1}}^{E_{EM2}} dE_{EM} = \int_{T_1}^{T_2} P_{EM}\, dt \\ &\Rightarrow E_{EM2} - E_{EM1} = P_{EM}(T_2 - T_1) = P_{EM} T_{ESS} \end{aligned} \tag{7}$$

where E_{EM1} and E_{EM2} are the EM energy levels at arbitrary instances T_1 and T_2 respectively, and E_{EM1} and E_{EM2} are associated with the EM voltages V_{EM1} and V_{EM2} respectively. If the initial EM voltage V_{EM1} is assumed to be the rated voltage, the voltage V_{EM2} will define the maximum voltage stress on the EM and FB-SM components, and the minimum voltage level to synthesize the required CHB ac output voltage. Thus, assuming $E_{EM2} = kE_{EM1}$ (k is selected depending on the allowable charge/discharge depth, and usually, $0.8 < k < 1.2$ [22]), the estimate of the initial stored energy within each EM is:

$$|1-k|E_{EM1} = P_{EM} T_{ESS} \Rightarrow E_{EM1} = \frac{P_{EM} T_{ESS}}{|1-k|} \tag{8}$$

Other practical factors may vary from one energy storage technology to another; therefore, the presented EM energy storage estimate should be adjusted with technology-dependent considerations such as permissible current capability, current and voltage ripple requirements for extended lifetime, etc. [24]. Then, the corrected energy storage could be used to quantify and optimize the ESS scale and its capital cost [22], [25]-[27]. For the proposed structure, the deliberate use of low-rated FB-SM voltages within the ESS permits direct connection of the EM across the FB-SM [16], [28]. The CHB converter investment cost can be evaluated as in [29] and [30].

As FB-SMs in each phase of the ESS are divided into N_{UFBS} modular units by the UFBSs (according to the physical characteristics and interruption performances [14], [31]), the UFBS rated blocking voltage V_{UFBS} can be expressed as $V_{UFBS} = V_{EM}N_{FB}/N_{UFBS}$. Also, according to the mentioned principles, the IGBT pair and its paralleled MOVs within the auxiliary breaker are designed to withstand the on-state voltage drop sum of the N_{FB}/N_{UFBS} series-connected FB-SMs within one unit. If configured, the transformer T_X should be designed for the same rated voltage and power as those of the CHB converter, whereas isolation and insulation are necessary for such HVDC applications [1], [32].

IV. Control System

Fig. 3 depicts the control system that coordinates the operation of HB-MMC and ESS under normal and fault conditions, and its technical details are as follows.

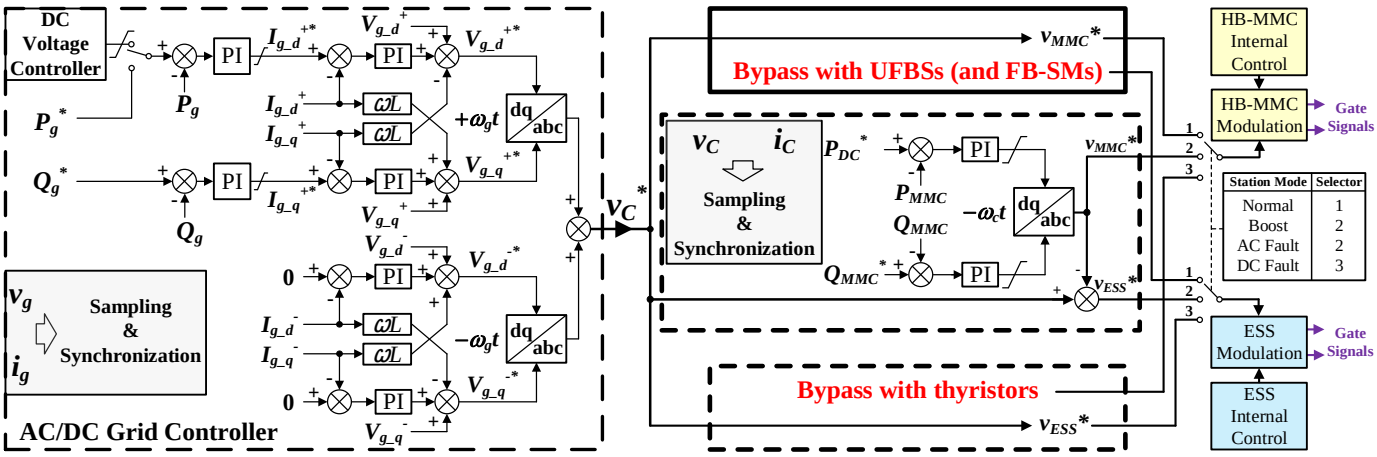


Fig. 3. Control system of the proposed HVDC station in different operation modes.

In general, for the given ac network impedances L and R, active and reactive power of the station ac grid (P_g and Q_g) are controlled through the ac grid current, which can be regulated by modifying the phase and magnitude of the station output ac voltage v_C based on:

$$v_C + L\frac{di_C}{dt} + Ri_C = v_g \qquad (9)$$

where i_C is the converter side ac current.

All converter stations with the proposed concept are equipped with active and reactive power control loops. The active and reactive power controllers generate direct and quadrature reference currents for the positive sequence inner current controller that defines the references for the positive sequence modulation signals. The negative sequence current controller suppresses the negative sequence current to zero and generates the negative sequence modulation signals. An extra dc voltage controller is added as the outer loop of the station that controls the system dc link voltage. To facilitate seamless transition between the various control modes, anti-windup and power limitations are incorporated. Thus, for different operating modes, the control system in Fig. 3 manipulates the HB-MMC and ESS stages seamlessly, facilitating ac/dc fault ride-through, uninterruptable power transmission, and boost operation (extended active and reactive power control range).

A. Normal Mode

During normal operation, the ESS remains in an idle state with all FB-SMs bypassed by UFBSs to increase station efficiency. Thus, HB-MMC ac voltage v_{MMC} equals converter station ac output v_C according to (1) and Fig. 2(b). This mode is similar to the operation of a conventional HB-MMC station.

B. AC Fault Mode

When an ac fault is detected, the HB-MMC remains its active power demand unchanged to minimize the transient dc power flow in the dc side. After a short delay of 2ms to account for current commutation from UFBS paths to CHB converters, the on-demand ESS is activated to limit the ac current contribution to the ac fault and participate in power balancing between the HB-MMC and the ac grid (and suppresses the negative sequence current in asymmetrical fault cases). As a result, HB-MMC control is modified to basic load-angle control as in Fig. 3, and the ESS compensates the depressed grid voltage to exchange active power with the HB-MMC and ac grid.

Also, as shown in Fig. 3, simultaneous operation of the HB-MMC and the ESS can be utilized for long-term reactive power boost for ac voltage support and short-term active power boost for inertial response and primary frequency support.

C. DC Fault Mode

When a dc fault is detected, the HB-SMs of HB-MMC are blocked and bypassed as described previously. After a short delay of 2ms to account for current commutation from the UFBSs to CHB converters, ESS is activated to take control of the PCC current and exchange active and reactive power with the ac grid, see Fig. 3. Thus, the ac side does not experience noticeable active and reactive power imbalance. Also, dc fault current diminishes rapidly in the dc side of the HB-MMC after the EES activation. During the dc fault, all converter stations of the HVDC system must be switched to dc fault mode to avoid the disruption of active and reactive power exchanged with their host ac grids.

D. Other Controllers

For HB-MMCs, other auxiliary controllers such as the HB-MMC circulating current suppressing controller, and the HB-SM capacitor voltage balancing controller are included, and EM voltage balancing within each phase of ESS is also needed as in Fig. 3. Additionally, as the energy stored within EMs may be changed by ESS utilization and EM self-discharge, active maintenance of the ESS energy is necessary, which can be achieved through a subtle fundamental voltage injection of CHB converter [11]. As the ESS charges/discharges (depending on the station operation mode) during the ac/dc fault, to ensure sufficient fault case power support duration, ac/dc fault probability information from the power system operators is needed to optimize the on-demand stored energy of the ESS.

V. Simulation of an HVDC Grid

Fig. 4 shows a dc grid with three terminals (I, II and III) to assess the technical viability of the proposed structure, with the system parameters displayed. The symmetrical monopole interconnection is adopted with the lumped parameter model of dc lines. The converter station of terminals I, II and III are modeled by an HB-MMC and an isolated ESS with the same power rating, as described in section II and shown in Fig. 1. Terminal I regulates the dc voltage V_{dc} at 80kV, while II and III control their active powers exchanged with ac grids II and III respectively. The positive direction of active and reactive power is assumed to be from the

dc side to ac sides. All three terminals maintain their capacitive reactive power references at the rated. Quantitative substantiation of the beneficial claims, with regard to the boost operation and the uninterruptable active/dc power in ac and dc fault cases, is presented based on MATLAB-SIMULINK time-domain simulations.

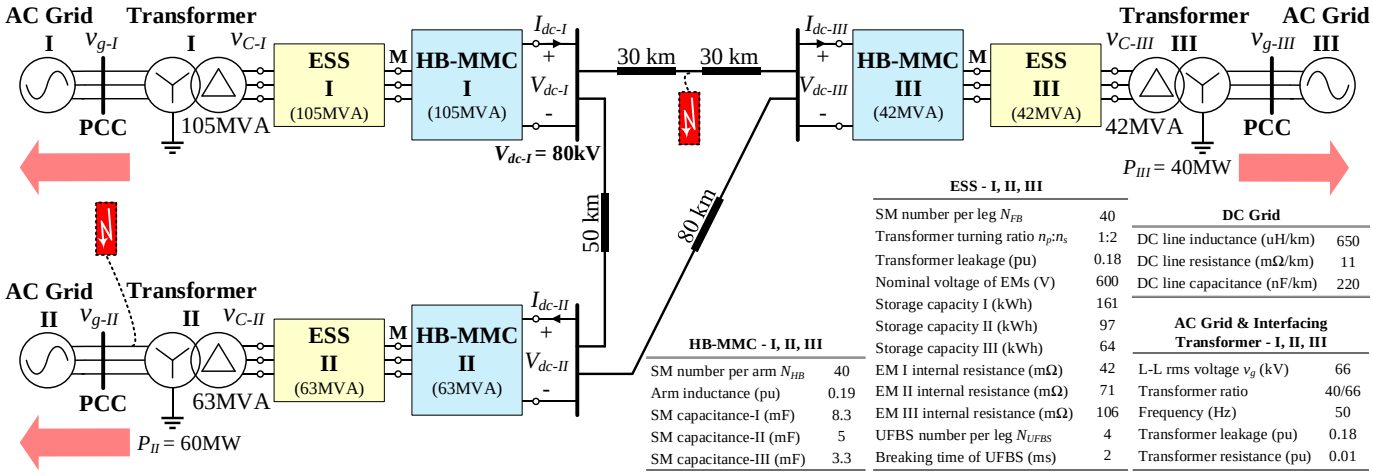


Fig. 4. Simulated three-terminal dc grid including the system parameters.

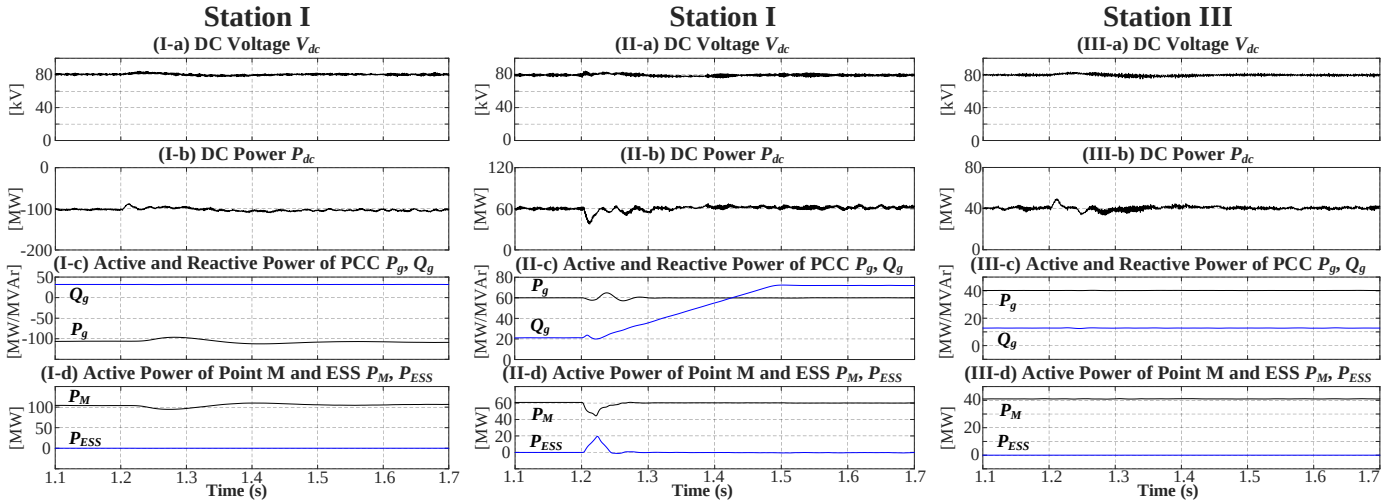


Fig. 5. Simulation waveforms of the station I-III with station II in boost mode.

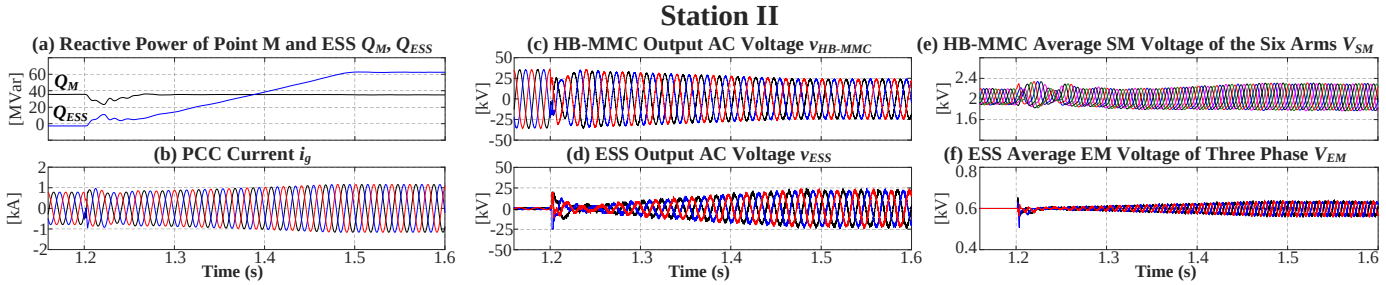


Fig. 6. Other waveforms of the station II with station II in boost mode.

A. Boost Mode

This subsection demonstrates the boost capability of the proposed station structure, in which station II exploits the reactive power capabilities of both the HB-MMC and the CHB of the ESS by ramping up its reactive power output beyond the possible range of the conventional HB-MMC. The maximum capacitive reactive power limit of station II is established by increasing the reactive power outputs until the ac current limit (1.2pu) is reached. Simulation results with station II operating in boost mode are presented in Fig. 5 and Fig. 6.

Fig. 5 II (a)-(d) show that station II starts increasing its grid reactive power at 1.2s from 20MVAr until the ac current hits the limit, where the reactive power output reaches the maximum of +75MVAr approximately, whereas its rated active power is unchanged. Waveforms in Fig. 5 I and III show that except for a minor disturbance for a short period after boost mode initiation, the operation of stations I and III remains unaffected. Fig. 5 II (c) and (d) and Fig. 6(a) indicate that before the initiation of boost mode, the HB-MMC of station II contributes the entire reactive power exchanged with ac grid II (Q_g) plus the reactive power consumption of the transformers. Fig. 6(a) shows the reactive power contributions from the HB-MMC and the ESS of station II, revealing that significant ac voltage boost is facilitated by the ESS. Fig. 6(b)-(d) show PCC current and ac voltages of the HB-MMC and the ESS. The grid current reaches its limit whereas the significant modulation index margin remains unexploited for both the HB-MMC and the CHB of ESS. Also, voltage stresses on the switching devices and EMs of station II remain controlled, see Fig 6(e) and (f). As the ESS contributes zero active power while boosting the reactive power capability of the proposed structure, it can be concluded that boost mode operation is not time-limited.

B. AC Fault Cases

This subsection examines the resiliency of the proposed station structure against symmetrical and asymmetrical ac faults.

A temporary solid symmetrical three-phase to ground ac fault is applied at the PCC of ac grid II at 1.2s and cleared at 1.4s. Simulation results are presented in Fig. 7 and Fig. 8.

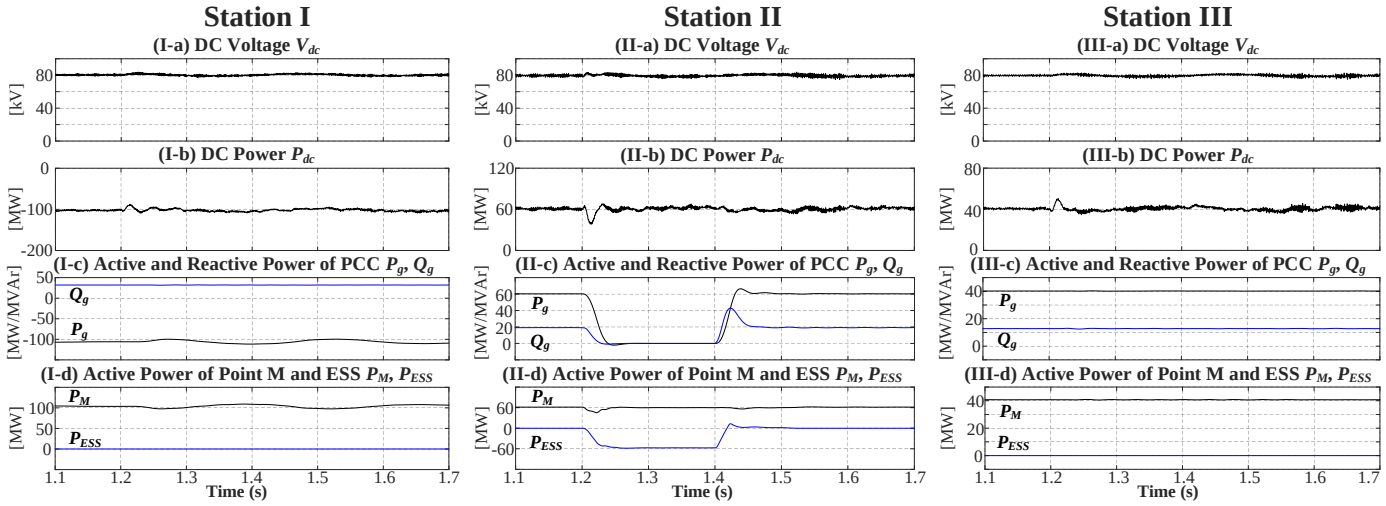


Fig. 7. Simulation waveforms of the station I-III in three-phase short circuit solid ac fault case.

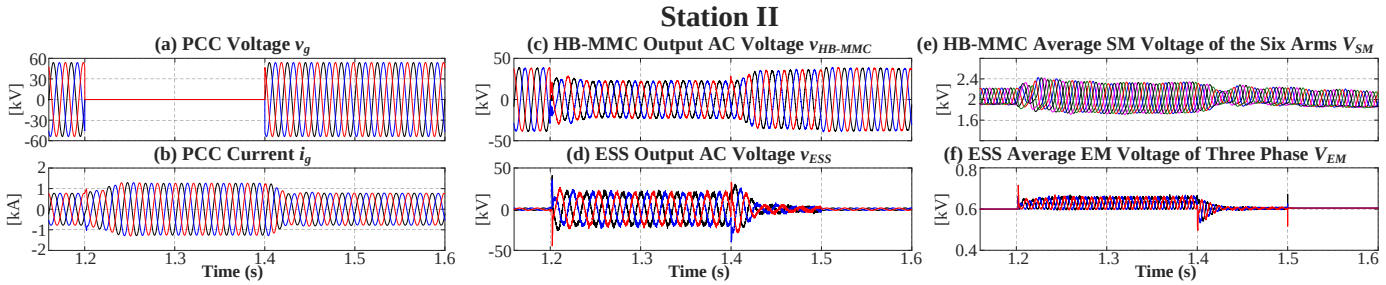


Fig. 8. Other waveforms of the station II in three-phase short circuit solid ac fault case.

Waveforms (a) and (b) of I, II and III in Fig. 7 show that during the ac fault the sudden active power drop of converter terminal II from 60MW to 0 has limited impact on the power flow of the dc grid, with dc voltages and powers of terminals I, II and III exhibiting minor disturbance at fault inception and clearance instances. Waveforms (c) and (d) of I, II and III in Fig. 7 present the net active and reactive power exchanged with their respective ac grids, and active powers of the HB-MMCs and ESSs of stations I, II and III. In this ac fault case, stations I and III continue in normal operation mode, where their ESSs are bypassed in the idle state. Waveforms (c) and (d) of II in Fig. 7 show that the ESS facilitates orderly diversion of the dc power P_{dc} (or active power P_M) that station II unable to inject into the ac grid II due to the ac fault.

Fig. 8(a)-(d) show simulation waveforms of the PCC voltage and current, and ac voltages contributed by the HB-MMC and the ESS of station II. This simulation assumes that the maximum over-current capability of each station is limited to 1.2pu. Fig. 8(a) and (b) show that the converter station with the proposed concept is capable of injecting the maximum current into the fault ac grid as expected, with a 2ms commutation

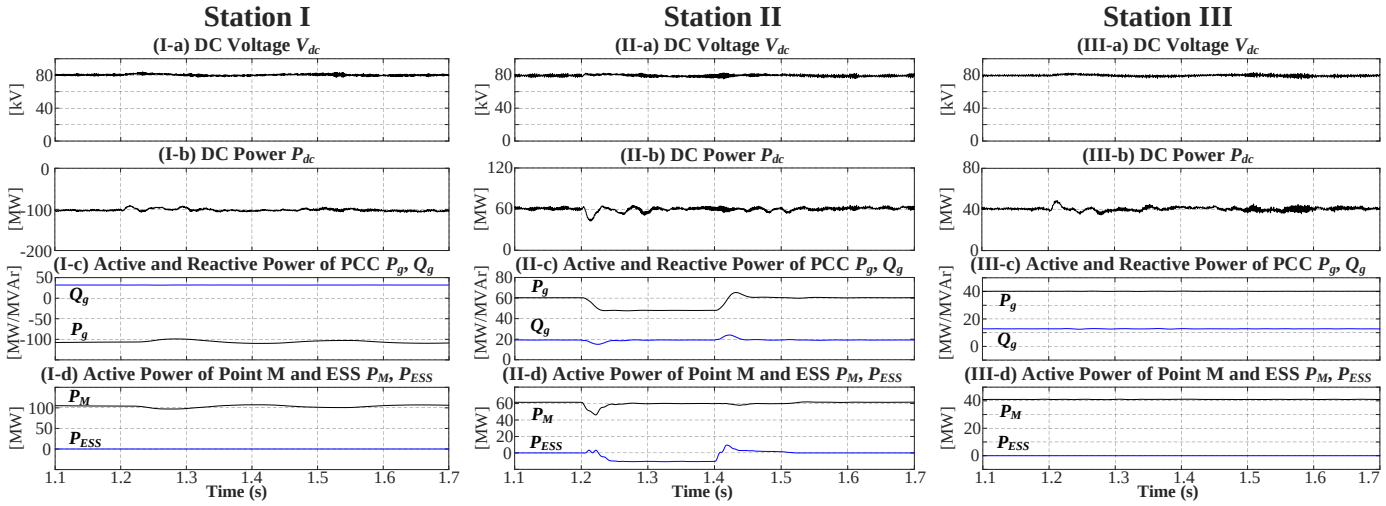


Fig. 9. Simulation waveforms of the station I-III in single-phase to ground solid ac fault case.

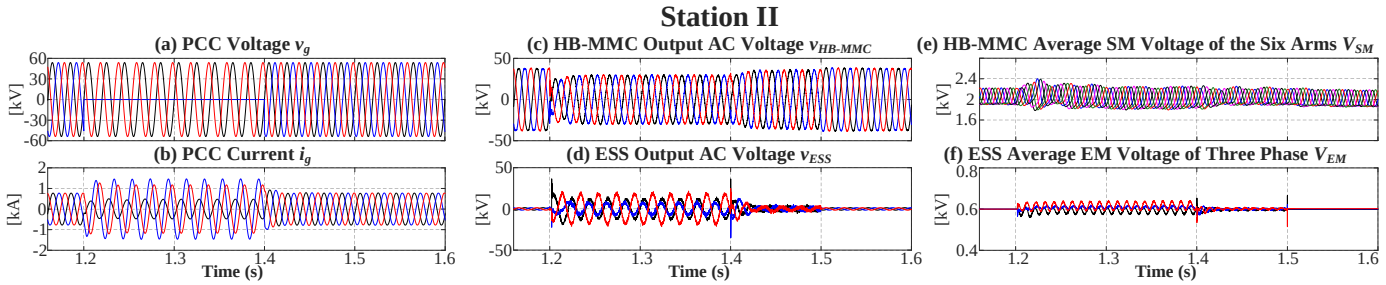


Fig. 10. Other waveforms of the station II in single-phase to ground solid ac fault case.

process after the ac fault at 1.2s. Fig. 8(c) and (d) reveal that the ESS is idle, and its ac voltage and active/reactive power contributions start at fault inception and gradually cease after fault clearance. Thus, the ESS is able to sink rated active power during the ac fault, while limiting ac current contribution to the fault grid as expected from any VSC, without excessive over-voltage in the dc network. Also, voltage stresses on converter switches, passive components and EMs remain regulated, see Fig. 8(e) and (f). To ensure seamless transition from the ac fault to post-fault, the bypass of the ESS after fault clearance is delayed by 5 cycles (100ms) to enable natural reduction to its contribution to the total output ac voltage and the active/reactive power, as shown in Fig. 8(c), (d) and (f).

The resiliency of the proposed converter structure to the asymmetrical ac fault is further examined, where station II is subjected to a temporary solid single-phase to ground ac fault at the PCC of ac grid II at 1.2s and cleared at 1.4s. Simulation results are presented in Fig. 9 and Fig. 10.

Waveforms (a) and (b) of I, II and III in Fig. 9 show that during the ac fault the active power of station II

drops from 60MW to 48MW, whereas dc voltages and powers of terminals I, II and III have small disturbance at fault inception and clearance instances. Waveforms (c) and (d) of I, II and III in Fig. 9 present the active and reactive power exchanged with their tied ac grids, and active powers of the HB-MMCs and ESSs of stations I, II and III. In this ac fault case, stations I and III continue the operation with ESSs bypassed in the idle state. Station II ESS absorbs a portion of the dc power P_{dc} (or active power P_M) that station II cannot inject into ac grid II due to the fault, see Fig. 9 II (c) and (d).

Fig. 10(a)-(d) show simulation waveforms of the PCC voltage and current, and ac voltages contributed by the HB-MMC and the ESS of station II. Fig. 10(a) and (b) show that station II suppresses the negative sequence current, with a 2ms commutation process after the ac fault inception. Fig. 10(c) and (d) reveal that the ESS remains idle during the pre-fault period, contributing near zero ac voltage and power. Its ac voltage and active/reactive power contributions start at fault inception and gradually cease after fault clearance. Participation of the ESS of station II to sink active power during the single-phase ac fault prevents substantial disturbance in dc power flow. In addition to active or dc power balancing, Fig. 10(b)-(d) show that the ESS functions as a series active power filter that injects negative sequence voltage to suppress the negative sequence current and present balanced three-phase ac voltage to the HB-MMC. Also, voltage stresses on converter switches, passive components and EMs remain regulated, see Fig. 10(e) and (f). Seamless transition from the ac fault to the post-fault condition is realized by delaying the bypass of the ESS to enable natural diminishing of its contribution to the synthesis of the total output ac voltage and the active/reactive power, as shown in Fig. 10(c), (d) and (f).

In summary, the ac fault case simulation indicates that the HVDC converter station employing the proposed structure in a multi-terminal dc grid can minimize the impact of the ac fault on the dc side, including, elimination of dc link voltage variations and minimization of transient dc power flow.

C. DC Fault Case

Fig. 11 displays simulation results for a temporary solid pole-to-pole dc short circuit fault between terminals I and III as marked in Fig. 4. For illustration, the fault is initiated at 1.8s and cleared at 2.0s.

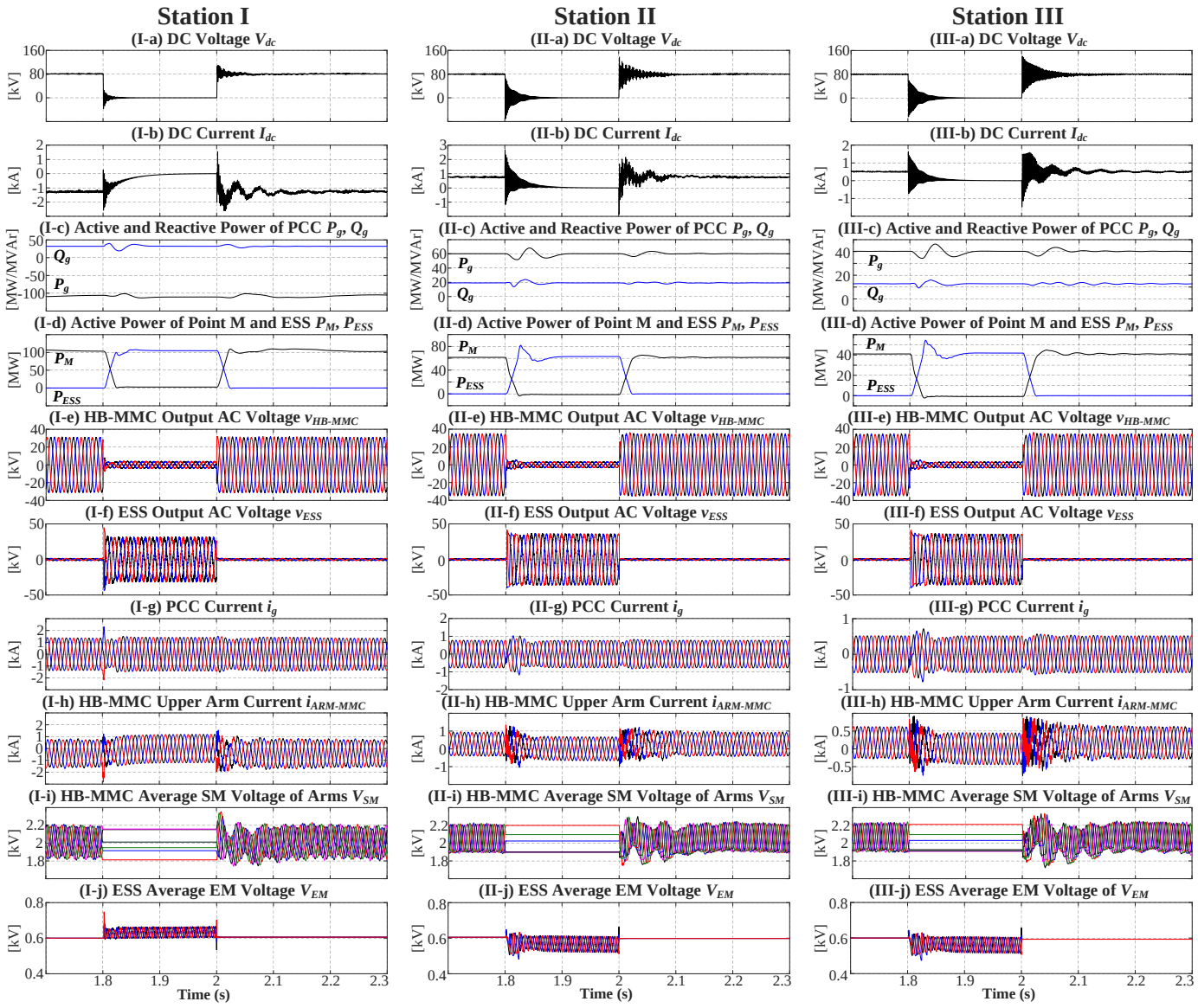


Fig. 11. Simulation waveforms of the station I-III in the pole-to-pole dc short circuit fault case.

Waveforms (a) and (b) of I, II and III in Fig. 11 show the dc side voltages and currents of stations I, II and III respectively. Waveforms (c) and (d) of I, II and III in Fig. 11 present the net active and reactive power exchanged with their respective ac grids, active powers of the HB-MMCs and the ESSs of stations I-III, respectively. These results show that the converter stations based on the proposed structure are capable of riding-through pole-to-pole dc short circuit fault, without interrupting the active/reactive power exchanged with their ac grids. The dc current in Fig. 11(b) for stations I, II and III and HB-MMC arm currents in Fig. 11(h) for stations I, II and III confirm the dc fault current drops to zero within 5 fundamental cycles.

Waveforms (c) and (d) of I, II and III in Fig. 11 show that the active and reactive power that converter stations exchange with their respective ac grids are unaffected by the dc fault, with the ESSs compensating for the lost dc/active powers from/into the HB-MMCs. Waveforms (e) and (f) of I, II and III in Fig. 11 show the sudden collapse of HB-MMC ac voltages as a result of dc fault and the subsequent action of bypassing HB-SMs, and then converter station output ac voltages are compensated by ESS ac voltages. As a result, the ESSs take over the control of ac grid currents and active/reactive powers, see (c)-(g) of I, II and III in Fig. 11. In Fig. 11 I-III (h), HB-MMCs are protected by the HB-SM back-to-back thyristors that shunt the arm current surges. Thus HB-SM capacitors are not exposed to more than the rated current and voltage stresses, and ESS EM voltages are within the limit, see Fig. 11 I-III (i) and (j).

In summary, the dc fault case simulation reveals that the proposed HVDC station structure relaxes dc fault requirements in a multi-terminal dc grid, through replacing conventional dc circuit breakers with dc disconnectors, without disrupting the active/reactive power exchanged with the host ac grids.

VI. Conclusion

This paper has presented a new converter station structure that employs energy storage system technology to improve ac and dc fault ride-through performance in a multi-terminal HVDC grid. Detailed control and operating philosophies of the proposed structure were explained, and its effectiveness in ac and dc fault cases has been validated on a three-terminal system, using time-domain simulations. The proposed structure helps decouple the active power at the point of common coupling from the dc power. The occurrence of a dc fault will not lead to noticeable disruption of active/reactive power exchanged with the ac grids. Also, the concept minimizes the dc power transient within the dc grid during ac faults; therefore no significant transient dc voltage or power flow is observed in the dc link.

References

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, “VSC-based HVDC power transmission systems: An overview,” *IEEE Trans. Power Electron.,* vol. 24, no. 3, pp. 592–602, 2009.

[2] R. Marquardt, “Modular multilevel converter: an universal concept for HVDC-networks and extended dc-bus-applications,” in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 502–507.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: A review,” *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 37–53, 2014.

[4] L. Xu and L. Yao, “DC voltage control and power dispatch of a multi-terminal HVDC system for integrating large offshore wind farms,” *IET Renew. Power Gener.*, vol. 5, no. 3, p. 223, 2011.

[5] Solas, G. Abad, J. a Barrena, S. Aurtenetxea, a Carcar, and L. Zajac, “Modular multilevel converter with different submodule concepts - part II: Experimental validation and comparison for HVDC application,” *Ind. Electron. IEEE Trans.*, vol. 60, no. 10, pp. 4536–4545, 2013.

[6] R. Zeng, L. Xu, L. Yao, and B. W. Williams, “Design and operation of a hybrid modular multilevel converter,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, 2015.

[7] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, “Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits,” *IEEE Trans. Power Deliv.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[8] J. Hu, M. Xiang, L. Lin, M. Lu, J. Zhu, and Z. He, “Improved design and control of FBSM MMC with boosted ac voltage and reduced dc capacitance,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 1919–1930, 2018.

[9] M. M. C. Merlin *et al.*, “The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability,” *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 310–317, 2014.

[10] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, “Hybrid cascaded modular multilevel converter with dc fault ride-through capability for the HVDC transmission system,” *IEEE Trans. Power Deliv.*, vol. 30, no. 4, pp. 1853–1862, 2015.

[11] S. Debnath, M. Saeedifard, “A new hybrid modular multilevel converter for grid connection of large

wind turbines," *IEEE Trans. Sustain. Energy,* vol. 4, no. 4, pp. 1051–1064, 2013.

[12]G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New breed of network fault-tolerant transmission system," *IEEE Trans. Power Syst.*, vol. 28, no. 1, pp. 335–346, 2013.

[13]M. K. Bucher and C. M. Franck, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. Power Deliv.*, vol. 31, no. 1, pp. 87–95, 2016.

[14]J. Häfner and B. Jacobson, "Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grid," in *Proc. Cigr'e Symp., Bologna, Italy*, 2011.

[15]K. Jinkun, W. Xiaoguang, Y. Bingjian, G. Yang, and H. Zhiyuan, "Control strategy of the full-bridge based hybrid dc breaker," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, 2015, pp. 315–320.

[16]J. Asakura and H. Akagi, "State-of-Charge (SOC)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, 2009.

[17]M. Vasiladiotis and A. Rufer, "A modular multiport power electronic transformer with integrated split battery energy storage for versatile ultrafast EV charging stations," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3213–3222, 2015.

[18]Zhu, Z. Yang, H. Xia, and F. Lin, "Hierarchical control and full-range dynamic performance optimization of the supercapacitor energy storage system in urban railway," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6646–6656, 2018.

[19]Y. Shi and H. Li, "Isolated modular multilevel dc-dc converter with dc fault current control capability based on current-fed dual active bridge for MVDC application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2145–2161, 2018.

[20]Hillers and J. Biela, "Low-voltage fault ride through of the modular multilevel converter in a battery energy storage system connected directly to the medium voltage grid," in *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1–7.

[21]M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated

battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, 2015.

[22]Novakovic and A. Nasiri, "Modular multilevel converter for wind energy storage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8867–8876, 2017.

[23]Q. Chen, R. Li, and X. Cai, "Analysis and fault control of hybrid modular multilevel converter with integrated battery energy storage system," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 64–78, Mar. 2017.

[24]M. Farhadi and O. Mohammed, "Energy storage technologies for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 1953–1961, 2016.

[25]M. Yassine and D. Fabris, "Performance of Commercially Available Supercapacitors," *Energies*, vol. 10, no. 9, p. 1340, 2017.

[26]I. N. Moghaddam, B. H. Chowdhury, and S. Mohajeryami, "Predictive Operation and Optimal Sizing of Battery Energy Storage with High Wind Energy Penetration," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6686–6695, 2018.

[27]F. Yahyaie and T. Soong, "Optimal operation strategy and sizing of battery energy storage systems," in *2012 25th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2012, pp. 1–4.

[28]S. B. Wersland, A. B. Acharya, and L. E. Norum, "Integrating battery into MMC submodule using passive technique," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics, COMPEL 2017*, 2017.

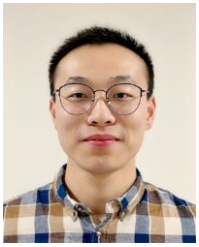
[29]G. Domingues-Olavarria, P. Fyhr, A. Reinap, M. Andersson, and M. Alakula, "From Chip to Converter: A Complete Cost Model for Power Electronics Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8681–8692, 2017.

[30]Y. Xue, B. Ge, and F. Z. Peng, "Reliability, efficiency, and cost comparisons of MW-scale photovoltaic inverters," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 1627–1634.

[31]C. Peng, X. Song, A. Q. Huang, and I. Husain, "A Medium-Voltage Hybrid DC Circuit Breaker—Part

II: Ultrafast Mechanical Switch," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 289–296, 2017.

[32]U. Astrom and V. Lescale, "Converter Stations for 800 kV HVDC," in *2006 International Conference on Power System Technology*, 2006, pp. 1–7.



Shuren Wang (S'18) received the first class B.Sc. and M.Sc. degrees in electrical engineering from Yangzhou University, Yangzhou, China, in 2013 and 2016, respectively.

He was with Bosch, TMR Energy, etc. He is currently working toward the Ph.D. degree in the University of Strathclyde, Glasgow, U.K. His research interests include energy conversion, power electronic converters, HVDC, RES and ESS.

Khaled H. Ahmed (M'09–SM'12) received the B.Sc. (first class hons.) and M.Sc. degrees in electrical engineering from Alexandria University, Alexandria, Egypt, in 2002 and 2004, respectively, and the Ph.D. degree in power electronics applications from the University of Strathclyde, Glasgow, U.K., 2008. He was appointed as an Associate Professor with Alexandria University since 2014. He is currently a Senior Lecturer in Power Electronics with the University of Strathclyde. He has published more than 91 technical papers in refereed journals and conferences as well as a published textbook entitled 'High Voltage Direct Current Transmission: Converters, Systems and DC Grids', a book chapter contribution, and a PCT patent PCT/GB2017/051364. His research interests include renewable energy integration, high power converters, off-shore wind energy, dc–dc converters, HVdc, and smart grids.

Grain P. Adam (M'12) received the B.Sc. and M.Sc. degrees (Hons.) from Sudan University for Science and Technology, in 1998 and 2002 respectively; and a PhD in Power Electronics from University of Strathclyde in 2007.

He is a researcher with University of Strathclyde in Glasgow, UK, since 2008. His research interests are fault tolerant voltage source converters for HVDC applications; modelling and control of HVDC transmission systems and multi-terminal HVDC networks; voltage source converter based FACTS devices; and grid integration issues of renewable energies.

Dr. Adam has authored and co-authored several technical reports, and over 100 journal and conference articles. Dr. Adam has published two books in applications of power electronics in power systems and renewable energy. He is an active contributor to reviewing process for several IEEE and IET Transactions, Journals and conferences, and a member of IEEE.

Ahmed M. Massoud (SM'11) received the B.Sc. (first class honors) and M.Sc. degrees in Electrical Engineering from Alexandria University, Egypt, in 1997 and 2000, respectively, and the Ph.D. degree in Electrical Engineering from Heriot-Watt University, Edinburgh, U.K., in 2004.

He is currently a Professor at the Department of Electrical Engineering, College of Engineering, Qatar University. His research interests include power electronics, energy conversion, renewable energy, and power quality. He holds five U.S. patents. He published more than 100 journal papers in the fields of power electronics, energy conversion, and power quality.

Barry W. Williams received the M.Eng.Sc. degree from the University of Adelaide, Australia, in 1978, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1980.

After seven years as a Lecturer at Imperial College, University of London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at Strathclyde University, UK. His teaching covers power electronics (in which he has a free internet text) and drive systems. His research activities include power semiconductor modelling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors to industrial electronics.