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Analysis of the charge sharing effect in the SET sensitivity of bulk 45 nm standard cell layouts under heavy ions

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Abstract

For nanometer technologies, SET is increasingly growing in importance in circuit design. Accordingly, different hardening techniques were developed to reduce the Soft-Error Rate. Considering selective node hardening technique based on standard cells, this work evaluates the SET response of logic gates from a Standard-Cell library under heavy ions. Overall, it is observed that the usage of NOR and NAND gates coupled with an output inverter provides reduced SET cross-section and increased threshold LET compared with the standalone OR gate and AND gate, respectively. With the results gathered in this work, circuit designers can implement reliability-aware synthesis algorithms with selective hardening more efficiently to tackle the threat of SET in combinational circuits.

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1. Introduction

Standard-Cell libraries containing thousands of pre-designed and characterized logic gates are widely used in the logic synthesis of VLSI designs. A Boolean function can be synthesized with a different combination of logic cells, implying a different number of transistors and layout design which directly impact the radiation robustness of the circuit. Recently, a great effort can be noticed from the research community in considering radiation hardening techniques early in the design flow of a VLSI circuit [1-5]. Once the highly vulnerable nodes are identified in a circuit, hardening approaches as transistor sizing or hardware redundancy can be added to improve the overall reliability of the circuit [6, 7]. However, transistor sizing techniques are only suitable for full-custom circuit designs for which the designer has control of the individual sizing of transistors. Additionally, hardware redundancy as Triple-Modular Redundancy (TMR) significantly increases the area and power consumption of the circuit. Considering semi-custom circuit designs based on Standard-Cell methodology, selective hardening can be applied in the logic synthesis to increase its radiation robustness. Reliability-aware logic synthesis, accounting for single event effects mitigation, consists in hardening a complex circuit by selectively using logic gates that minimize the SET generation or propagation in the most vulnerable subcircuits of a complex VLSI design [1]. The increase of the drive strength of cells by gate sizing or alternative implementation of a given logic function has shown to improve the radiation robustness of circuits [1, 8].

A standard cell library containing NAND, NOR, INV and D flip-flop gates is able to implement any function. Due to the downscaling of device feature sizes and the spacing, multiple-node charge collection is observed on secondary nodes affecting the SEE characterization and SER prediction [5]. This work aims to analyze the SET sensitivity of pairs of standard cells by considering the charge sharing under the impact of heavy ions to study its implication on the effectiveness of selective hardening approaches. The information gathered in this work can be used to improve hardening techniques applied in the logic and physical synthesis of a cell-based design. The radiation robustness of the circuit can be enhanced by choosing the best combination of standard cells that promotes the pulse quenching effect induced by charge sharing in electrically related combinational circuits [9].

This paper is organized as follows. Section 2 presents a review of published related work highlighting the actual state-of-the-art and the relevance of the present work. The methodology is discussed in Section 3, from the prediction tool point of view to the benchmarking standard-cell circuits. Section 4 provides the simulation results and discussion. Finally, Section 5 summarizes the paper and presents some conclusions.

2. Related Work

The SET characteristics are dependent on many factors as the type of particle, its energy, the strike location, the restoring current from adjacent transistors and the capacitance at the struck node. By increasing the node capacitance and the restoring current, the SET pulse width can be reduced. The work developed in [1] analyzed the effectiveness of three selective node hardening techniques which relies on the increase of the restoring current and nodal capacitance to harden against large SET pulse widths: (1) increase of drive strength by gate sizing; (2) by transistor stacking, and; (3) the usage of different logic gates for the same logic function.

Limbrick et al. [1] concluded that the three selective node hardening techniques can be effective

with different degree of improvement when it is included in a standard-cell design methodology. However, this work is purely based on spice injection, limiting the contribution of layout effects on the multiple-node charge collection by not considering the charge sharing, for example. Also, the cell placement in the third technique, which relies on the alternative implementation for the same logic function, influences the total collected charge and the Pulse Quenching effect in combinational cells [3, 9].

Experimental results from protons and heavy ion irradiation can be found for inverter, NAND and NOR gates from a 90 nm RHBD cell library in [8]. In this work, the logic cells were characterized considering different drive strengths available in the standard-cell library. The authors have concluded that both the NAND and NOR gates provide wider SET pulses than the minimum drive strength inverter of the cell library. Also, the effectiveness of hardening by increasing the cell drive strength was only observed for the inverter and NOR gate, and at low Linear Energy Transfer (LET) measurements. For higher LET, the increased drive strength cells presented a larger SET cross-section due to the greater collected charge induced by a larger sensitive/drain area [8]. The SET sensitivity depends on the total sensitive area and the drive strength of a logic gate in complex ways. For instance, different from the inverter and the NOR gate, the cross-section of the NAND2_X2 is larger than the NAND2_X1, whereas for the NOR gate, the opposite behavior is observed (cross-section of NOR2_X2 is lower than NOR2_X1) [8].

Another research has provided a comparative analysis of majority voters based on NOR and NAND gates under atmospheric constraints [10]. The circuits were designed with the 7-nm FinFET Predictive Process Design Kit (ASAP7) [11]. Unlike the observed in [8], both circuits have shown a similar radiation robustness. This behavior was attributed to the symmetric sizing of the PFET and NFET transistors and its consequent symmetrical collection/drain area and drive currents in both circuits.

Furthermore, in [5], a placement strategy for standard cells was presented considering the positive effect of charge sharing, i.e., the pulse quenching effect. In this sense, the present work analyzes the SET sensitivity of pairs of logic gates from a Standard-Cell library under heavy ions to measure the effectiveness of pulse quenching effect.

3. Methodology

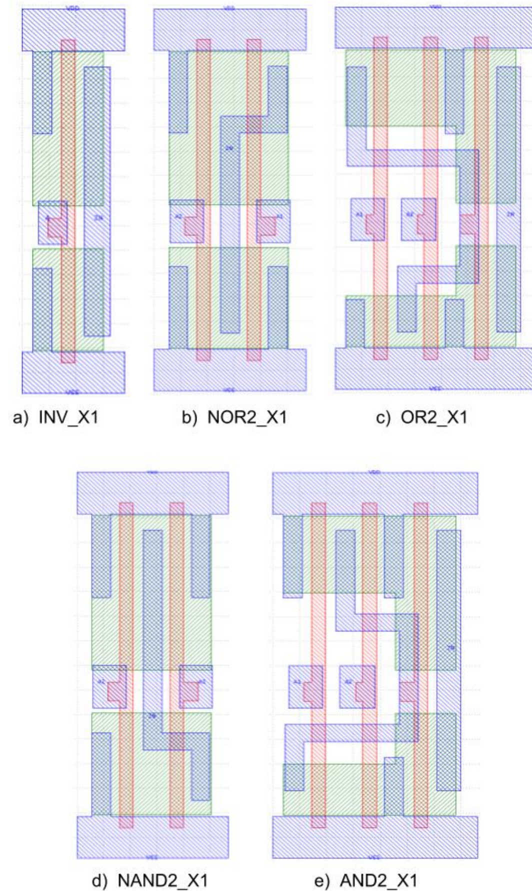


Fig. 1. Layout design of a) INV_X1, b) NOR2_X1, c) OR2_X1, d) NAND2_X1 and e) AND2_X1 in the 45 nm Open Cell Library [14]. The transistor geometries were extracted from the Graphical Design System (GDS) file and considered by MC-Oracle.

The calculation of SET sensitivity of complex integrated circuits is a challenge due to the plurality of dependencies in a not straightforward relationship [1,8]. Accordingly, in this work, the Monte-Carlo predictive tool MC-Oracle, developed at the Université de Montpellier [12, 13], is used to consider the multi-scale and multi-physics phenomena regarding radiation effects in electronics. The standard cells are issued from the 45-nm Open Cell Library [14]. Fig. 1 contains the simplified layout design of the INV_X1, NOR2_X1, OR2_X1, NAND2_X1 and AND2_X1, considering only the layers: Metal1, Active diffusion and Poly. As all analyzed circuits were chosen to be minimum sized, the suffix X1, which indicates the minimum cell drive strength available in the cell library, will be suppressed in the text for clarity.

3.1 Particle Physics Simulation

The MC-Oracle is a Monte-Carlo predictive tool able to calculate the transient current parameters considering the particle interaction physics and the layout design information of the circuit [12,13]. The tool is able to evaluate different radiation environments. For instance, in space application, the most relevant particles to affect electronics reliability are the heavy ions and protons produced by the sun. For heavy ions and alpha particles, the ionization mechanism is modeled by using the ion energy loss pre-calculated with SRIM [15]. Further, the information of the drain regions of each transistor is extracted directly from the cell layout design. The diffusion-collection model captures the carrier density at the electrodes as a function of time, determining the charge collection for each electrode of the circuit. For each particle interaction simulation, the transient current generated by the collected charge is stored for each electrode in a SET database. Therefore, multiple-node charge collection effects such as charge sharing mechanism can be evaluated using the tool. Moreover, only normal incidence strikes are considered as it was shown that deeply scaled CMOS technologies present a marginal difference in the overall charge sharing effect between normal and angled strikes [16].

3.2 Electrical Simulation

To complete the analysis, the SET database provided by MC-Oracle is used in the SPICE fault injection campaigns. Considering the layout parasitic extraction of each standard cell, different transient currents are injected in multiple drain junctions, due to the charge sharing mechanism. Three spacing for the combination of gates is evaluated to analyze the charge sharing effectiveness and its consequent pulse quenching effect as shown in Fig. 2. Only horizontal placements are considered in this study. It was previously shown that vertical placement, i.e. electrically connected cells placed in different cell rows, eliminates the pulse quenching effect due to the increased nodal separation and the presence of the well contacts which considerably reduces the charge sharing efficiency [17]. To calculate the SET cross-section a script routine is used to automate the fault injection and to measure the transient pulses. The transient currents are considered to be a SET only if it has reached half the value of the nominal supply voltage, which is 1 V in this technology node.

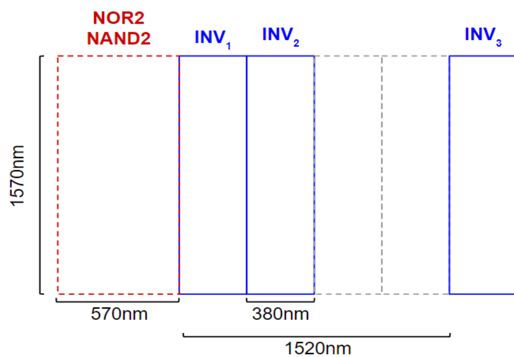


Fig. 2. Simulation setup accounting for different cell placement for the output inverter.

4. Results and Discussion

For reliability of the OR logic function implementation, it is evaluated a comparison of the SET response of the single cell OR2 and the NOR2 coupled with an INV in its output. Considering LET=78.23 MeV.cm^2/mg, Fig. 3 contains the SET cross-section for the standalone NOR2 gate and for the NOR2 gate coupled with a minimum drive strength inverter placed within the minimum distance. As can be observed, the pulse quenching effect is highly dependent on the cell input signals ranging from 7% to 17% of reduction on the SET cross-section. It can be explained by the different patterns of collection region produced under the cell input. From the cell layout design, the charge collection area of each input vector can be obtained for each circuit. In the case of input (0, 0), the NOR2 gate presents a collecting junction area of 0.0581µm^2 as only the

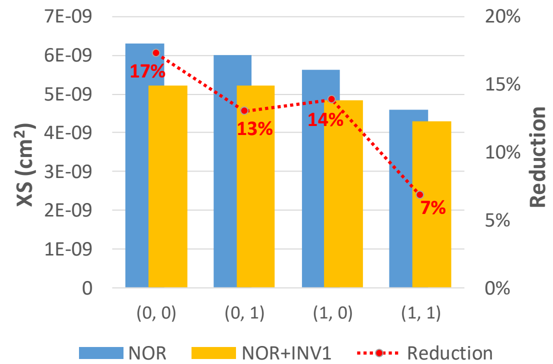


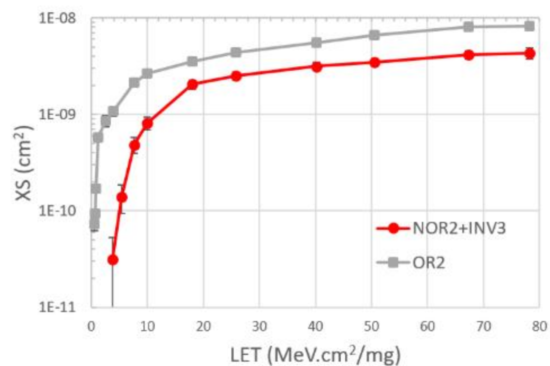
Fig. 3. Reduction on the SET Cross-Section due to the charge sharing and pulse quenching in the NOR gate with an inverter placed within the minimum distance.

NMOS devices are turned off. Moreover, the output inverter in the NOR+INV scheme presents a charge collection area of 0.0435μm^2 which corresponds to 75% of the NOR2 collecting area. The charge collected by the inverter presents a positive effect by reducing the number of SET generated in the NOR gate. On the other hand, for the input (1, 1) the NOR2 gate provides a greater collecting area of 0.1543μm^2 due to the off-state PMOS transistors. In this case, the output inverter provides solely a collection area of 0.0661μm^2, which corresponds approximately to 43% of the total NOR2 collection area. These differences in the collection area explain the cross-section differences observed in Fig. 3 for each input vector as it directly influences the effectiveness of the pulse quenching by the output inverter.

The worst-case scenario for the charge sharing in the NOR+INV scheme is for the input vector (1, 1). Similarly, it was found that this input also characterizes the worst case SET cross-section for the OR2 gate. Thus, the analysis of the results is particularly focused on input (1, 1). Table 1 presents the total area for the layout design and the total collection area for each cell used to implement an OR logic function. The total collection area corresponds to the total area of the drain p-n junctions in the cell layout design regardless of the cell input. Also, Table 1 provides the SET cross-section for an ion LET of 78.23 MeV.cm^2/mg and cell input (1, 1). Considering the standalone cells, the OR2 gate is 35.7% greater in area for the layout design and it presents only a slight increase in the total collection area when compared to the NOR2 gate. However, the SET cross-section increases approximately by a factor of 2. On the other hand, the OR logic function implemented using the NOR2 coupled with an inverter presents a greater area

Table 1
Total area for the cell layout design used for the OR logic implementation, the charge collection area and the SET cross-section for a LET=78.23 MeV.cm^2/mg and Input (1, 1)

	Layout Area (μm^2)	Total Collection Area (μm^2)	XS (cm^2)
NOR2	0.8792	0.2124	4.602E-09
OR2	1.1932	0.2163	8.268E-09
NOR2+INV$_1$	1.4758	0.3221	4.056E-09
NOR2+INV$_2$	1.4758	0.3221	4.134E-09
NOR2+INV$_3$	1.4758	0.3221	4.290E-09



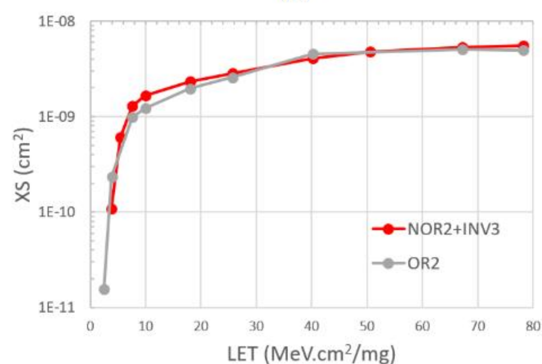


Fig. 4. SET cross-section curve of NOR2+INV$_3$ scheme and OR2 for LET = 78.23 MeV.cm^2/mg when cell input vector is (a) (1, 1) and (b) (0, 0).

than the standalone OR2 gate for both the layout design and collection region. However, a lower SET cross-section than the OR2 gate is expected, considering the three inverter placements in this study. Among the inverter placements, a slight difference is observed in the overall cross-section. As the distance between the NOR2 gate and the inverter increases, the SET cross-section increases. For clarity, only the SET cross-section curve of the NOR2+INV$_3$ is plotted against the cross-section curve of the OR2 gate in Fig. 4. As can be observed in Fig. 4 (a), the worst-case scenario of the OR2 gate can be highly improved with the adoption of the NOR2+INV scheme. An average reduction of approximately 60.14% on the SET cross-section is expected. Besides the overall cross-section decrease, the usage of NOR2+INV schemes also increases the threshold LET. Even at the worst-case SET cross-section for the NOR gate, which it is for the input vector (0, 0), the NOR2+INV scheme is a better option than the OR2 gate. As shown in Fig. 4 (b), it provides very similar SET cross-section and increased threshold LET than the standalone OR2 gate.

Table 2
Total area for the cell layout design used for the AND logic implementation, collection region and the SET cross-section for a LET=78.23 MeV.cm^2/mg and Input (1, 1)

	Layout Area (μm^2)	Total Collection Area (μm^2)	XS (cm^2)
NAND2	0.8792	0.1899	7.332E-09
AND2	1.1932	0.2053	6.984E-09
NAND2+INV$_1$	1.4758	0.2996	7.098E-09
NAND2+INV$_2$	1.4758	0.2996	7.254E-09
NAND2+INV$_3$	1.4758	0.2996	7.332E-09

Now, considering the AND logic function implementation, the single cell AND2 is analyzed and compared with the NAND2 gate coupled with a minimum sized inverter in its output. Table 2 contains the total layout design area, total collection area and the SET cross-section for each circuit. As it has a greater number of transistors, the AND2 gate design is bigger than the NAND2. However, a very similar cross-section is observed, even with a bigger collection area than the NAND2 design. It occurs due to the positive effect of certain charge collection electrodes that minimizes the overall number of SETs.

Considering the NAND2+INV schemes with 3 inverter placements, the usage of the standalone AND2 gate is superior in terms of reduced layout area and lower SET cross-section. The contribution of pulse quenching is very limited as the overall cross-section is quite similar to the standalone NAND2 gate. When the input vector is (1, 1), the NMOS device from the output inverter of the NAND2 is dominating the pulse quenching effect, different from the case of the NOR2+INV schemes which it was the PMOS device. The NMOS drain area in the inverter is approximately 35% smaller than its PMOS drain area, thus a reduction in the pulse quenching effect is expected as it directly reduces the positive effect of charge collection.

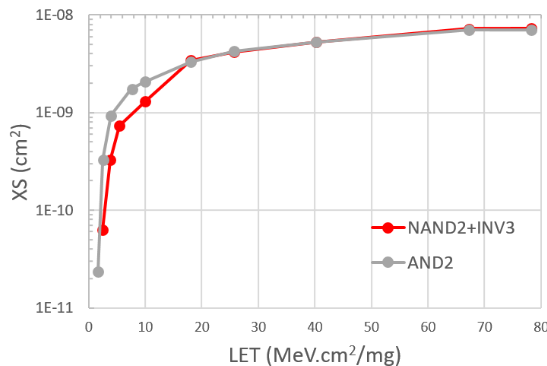


Fig. 5. SET cross-section curve of NAND2+INV$_3$ scheme and AND2 for LET = 78.23 MeV.cm^2/mg and cell input vector (1, 1).

Fig. 5 contains the SET cross-section curve of the NAND2+INV$_3$ and AND2 gate for LET = 78.23 MeV.cm^2/mg and cell input (1, 1). For high LET, both circuits present a comparable SET cross-section while the NAND2+INV$_3$ provides slightly reduced cross-sections for lower LET. Despite the quite similar cross-section trend, the NAND2+INV$_3$ provides a higher threshold LET than the standalone AND2 gate.

According to a previous work [18] that proposes the single event cross-section follows a power law of the Linear Energy Transfer (LET), the SET cross-section curves of Fig. 4 (a) is plotted in logarithmic scales in Fig. 6. Clearly, the OR2 cross-section follows a power law of the LET. As discussed in [18], the power law shape is attributed due to the collection efficiency of a single collection zone that depends continuously on the distance to location of the deposited charge. For lower LET and for the NOR2+INV$_3$ circuit, more collection zones might be at play in the collection process, providing a different shape of the SET cross-section curve.

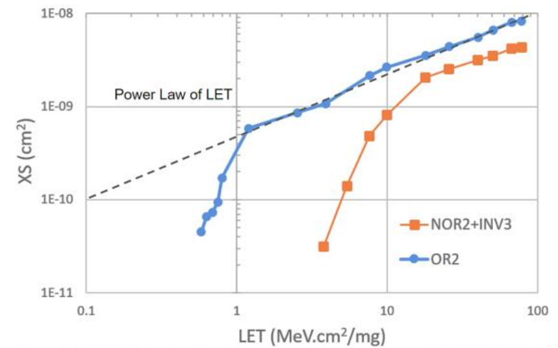


Fig. 6. The Power Law of Linear Energy Transfer.

4. Conclusions

A different implementation of the same logic function can induce different SET sensitivity. Considering a selective node hardening based on standard cells, this work analyzes the SET sensitivity of basic logic cells considering the layout effects to provide guidelines for the improvement of reliability-aware synthesis accounting for radiation effects. To implement the OR and AND logic functions, an

enhanced SET robustness can be achieved by considering using an inverter in the output of NOR and NAND gates, respectively. Besides lowering the overall cross-section, these combinations of gates can significantly increase the threshold LET.

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