A simple 1-D finite elements approach to model the effect of PCB in electronic assemblies

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Abstract

In this paper, a simple method to describe the effect of Printed Circuit Board (PCB) and environment on the thermal behavior of packaged devices is addressed. This approach aims at exploiting the benefit of compact thermal models, which are necessarily one-dimensional, together with the advantage of Finite Element (FE) modeling, which retains all the three-dimensional geometrical details, only in the regions of the model that must be accurately described. The main focus is on correct modeling of long power pulses for subsequent electro-thermal and thermo-mechanical analysis at chip level.

Keywords
thermal modeling; power devices; finite element modeling

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1. Introduction

In the field of automotive electronics, achieving strong device reliability is a primary requirement. Operating typical automotive loads, such as light bulbs or servo-motors, represents a strong thermal stress for the device itself due to high inrush current, long turn-off times, and high inductances these loads feature. As a result, switching these loads implies high switching losses, long turn-on and turn-off transients, and strong overheating. The switches will be cycled from thousand to million times and the corresponding power cycles will induce thermo-mechanical degradation, eventually leading to electrical failure. It is thus necessary to correctly model such power cycles to improve device reliability and understand failure mechanisms, and in particular an accurate thermal model is the first step to draw all the subsequent electro-thermal and thermo-mechanical conclusions.

From a modeling point of view, there is always a trade-off between (*a*) the duration of the power dissipation pulse and (*b*) the level of detail necessary to capture the important thermal effects. A typical electronic switch for low voltage automotive applications is shown in Figure 1. In case of short pulses (10 µs ÷ 1 ms) it is enough to model the device down to the die attach level, neglecting the effect of package and PCB on the overall thermal behavior, because the heat wave does not reach the latter domains.

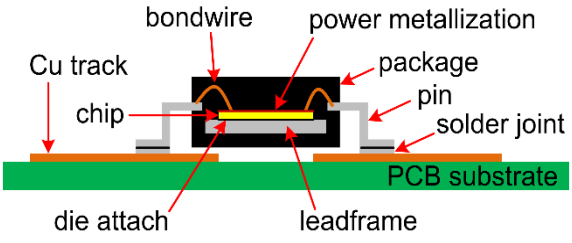

Fig. 1. A schematic view of a packaged device mounted on PCB with indication of some typically modeled features.

In case of long pulses (duration > 1 s), the situation is reversed: the internal structure of the device can be simplified while the correct modeling of pins, solder joints, and PCB is important.

However, this simplification approach has some limits, since the device is assumed to be mechanically perfect and always operating in a thermally-stable region. In case of automotive MOSFETs, they can indeed be operated below the Temperature Compensation Point (TCP), that is, under unstable regime [1]. In case of long pulses, the PCB should be included in the electro-thermal model, as well as a detailed model of the packaged device itself. These kind of problems where in the same model it is necessary to describe tiny and wide features at the same time (e.g., bonding wires, whose diameter is on the order of tens of µm, and PCB, with typical dimension on the order of centimeters) is always a challenging engineering topic.

While different approaches are available [2,3] for solving these problems, a simple alternative method is presented where, basically, the PCB is simplified in order to reduce the Degrees of Freedom (DoFs) of the overall simulation.

In the next sections the basics of the method are explained and two case studies are provided.

2. The simplification approach

Lumped Element Models (LEMs) are well known in literature and here will be briefly recalled. These models rely on the formal analogy between Fourier thermal equation and electrical circuit equations, thus allowing the description of a thermal system by means of *R-C* networks where thermal resistances and thermal capacitances model the heat flow path. Physics-based LEMs are useful since they can capture the actual heat flow in the structure, but generally they necessitate of many elements [4]; on the other hand, empirical models [5] (based on Foster and Cauer networks) are very quick to be solved but, except for multilayer stacks, there is no physical link with the structure they are describing.

The approach here explained aims at merging the benefits of LEMs with the advantages in terms of geometric description provided by Finite Element (FE) models. The fundamental assumption is that heat propagation through the contact surfaces between pin, or its solder joint, and PCB can be modelled in a quasi-1D way. As a rule of practice, each solder joint at a pin end corresponds to a contact surface as shown in Figure 2.

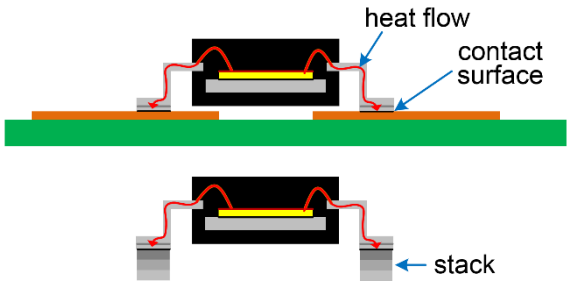

Fig. 2. Cross-sectional view of heat flow through the contact surfaces in the full model (top) and in a simplified model where an equivalent stack of different materials is determined (bottom).

A given heat flux P_{S_i} [W] will flow across the *i*-th contact surface, being T_{S_i} the surface-averaged temperature of the contact surface itself [K]. The thermal impedance at the *i*-th contact surface Z_{th_i} is calculated as follows:

$$Z_{th_i} = \frac{T_{S_i} - T_{amb}}{P_{S_i}} \quad [\mathrm{K/W}] \qquad (1)$$

Equation (1) describes the thermal behavior at the contact surface assuming 1D heat transfer. The reference temperature T_{amb} is that of the ambient.

The next step is to obtain a Cauer LE model which fits the above thermal impedance response at the contact surface, as described in Section 2.1

Once the set of (R_m, C_m) values for the Cauer representation is obtained, the LE model is back-transformed into its equivalent FE model on the basis of geometric considerations. For each *RC* stage, a fictitious layer of a stack with adiabatic lateral walls in the FE model will be generated. Material properties are determined in order to ensure the same 1D thermal impedance response for both LE and FE models.

Figure 3 shows the above-described process. Assuming a contact surface A_i, the thermal impedance at its location is calculated and the equivalent Cauer network is obtained. Then, if *n* stages are found (for instance $n = 3$ in Figure 3), a stack of *n* materials m_1, m_2, … m_n will be generated in the FE model. It is important to note that the bottom of the stack is fixed at $T = T_{amb}$, and that this stack of fictitious materials includes also the effect of the boundary conditions set in the original model around the PCB.

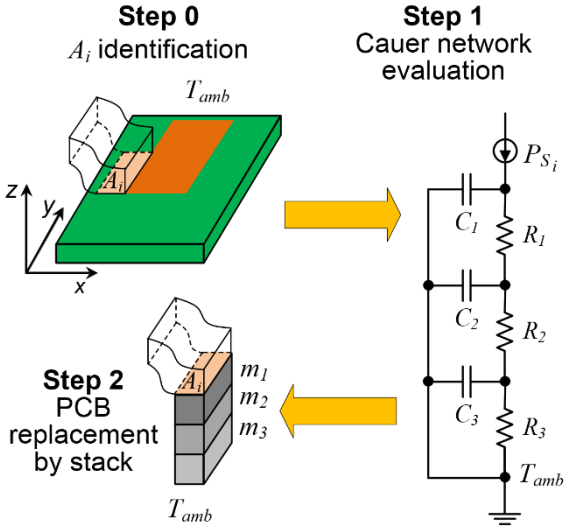

Fig. 3. Graphical representation of the simplification method.

As shown in Figure 3, the cross-sectional area on the *xy* plane is fixed by the contact surface, while the thickness of each layer is chosen considering mesh constrains. Mesh is eased when adjacent volumes feature comparable thickness.

Clearly, this equivalent model cannot be classified as a Boundary Condition Independent (BCI) model [6,7]: if the boundary conditions change, the simplification process must be re-performed.

2.1. Determination of the Cauer network

The determination of the Cauer network is needed in order to obtain the equivalent stacks replacing the PCB under the pins in the simplified FE model. Here, the procedure for one contact surface is explained using a reference model with a D2PAK MOSFET mounted on a PCB with a standard FR4 substrate (thickness 1.6 mm, 1 oz copper).

The main idea is to determine the Cauer networks for every contact surface (e.g. gate, drain and source) by applying a stepped heat-flux waveform at each A_i, keeping all the other contacts thermally insulated. It

is firstly necessary to obtain the corresponding Foster networks:

$$(t) \quad \left. \frac{(t)}{u(t)} \right|_{P} \qquad (2)$$

where $u(t)$ is the unit step function, P is the amplitude of the stepped heat flow ($P_{S_i}(t) = u(t)$).

The simplified model obtained in such a way did not provide satisfactory results, because it neglects the mutual thermal influence between each A_i.

A second attempt consisted in applying a stepped heat-flux waveform to every contact surface at the same time:

$$(t) \quad \frac{(t)}{u(t)} \qquad (3)$$

This approach resulted in unsatisfactory results too, since the mutual influence between each A_i couple is in general different from the others, due to different copper track dimensions, different area sections, and so on.

It turns out that none of the above mentioned methods produces reliable approximations. Thus, in order to calculate the Foster network to transform into Cauer form, the best way to take into account (a) the different paths (magnitudes and delays) between the chip and the contact surfaces, and (b) the $P_{S_i}(t)$ interactions in the PCB, is to apply the stepped heat source in the chip of the full model. With post-processing on simulation results it is possible to evaluate (t) and (t), needed to calculate the (t) at each A_i.

In this case it is worth mentioning that $P_{S_i}(t)$ is not anymore a power step, being the waveform smoothed by its flow from the chip through the system.

Despite this, $Z_{th_i}(t)$ is written in its Foster form:

$$(t) \quad \sum \quad \left(1 \quad {}^{t/(R \quad)}\right) \qquad (4)$$

A standard method to fit the above response is to fix the N time constant values $\tau_m = R_m C_m$, and then perform a least-square fit only on R_m values. In this case, instead, the fit routine was modified using both R_m and C_m as fitting parameters, and fixing the maximum number N of stages. Therefore, the following objective function had to be minimized:

$$f_{obj}(t) = \sum_{t=t_{start}}^{t_{end}} \left(Z_{th_i}(t) - Z_i^F(t) \right)^2 . \qquad (5)$$

Equation (4) clearly states that the minimization is performed on the full time response of the system, allowing both R_m and C_m as fitting parameters. This algorithm can lead to couples (R_m, C_m) which feature the same time constant τ_m and it is thus necessary to reduce them to a single equivalent Foster stage, leading to a number of effective stages $M \leq N$. Provided this check, the conversion to Cauer network is then performed by following the algorithm described in [8].

The algorithm can be performed by fixing an arbitrary number of stages N, but the least squares estimator does not ensure that the error between the original model and the simplified one will be under a desired tolerance, even if N is great. In general, as tested for this work, this is true also for other similar estimators.

Here, many stages are undesirable since a simple equivalent model is sought. In fact, the needed number of stages was always below 5.

For example, Figure 4 shows the temperature behavior in the chip's center of mass, and the relative error between the original and simplified models. The error at a given point, in a specific instant, is given by Eq. (6):

$$\mathrm{R(t)\%} \qquad \left| \frac{\mathrm{(t)} \qquad \mathrm{(t)}}{} \right| \qquad (6)$$

where $\Delta T_{OM}(t)$ represents the original model temperature increase in a given time, $\Delta T_{SM}(t)$ represents the simplified model temperature increase at the same time, and ΔT_{OM} is the temperature increase in the original model at the steady state.

Figure 4 shows that, during the heating phase, the error is greater than 5 % in the considered point, with N = 5. Such error is unacceptable in case of coupled electro-thermal simulations of long pulses, because it will result in a higher overall error.

2.2 Proposed approach

A fine-tuning step is added in the procedure to reduce the error below a desired tolerance. Figure 4 shows that the two temperature curves are shifted in time. The curve from the original model, in these simulation cases, differs in breadth and positioning from the simplified one.

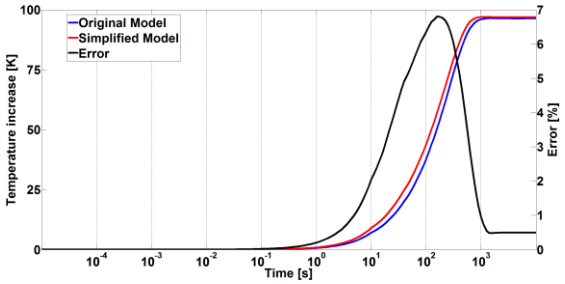

Fig. 4. D2PAK mounted on a PCB: temperatures of the chip's mass center as a function of time, obtained from the full original model and the simplified model built applying the $Z_{th_i}(t)$ fit routine with R_m and C_m as fitting parameters, limiting M to 5.

Therefore, the curve obtained from the simplified model should be properly delayed and adjusted in amplitude at steady state. An additional *RC* stage accounts for the heat spreading in the copper tracks and it is used for fine tuning purposes. The final *RC* ladder is shown in Figure 5.

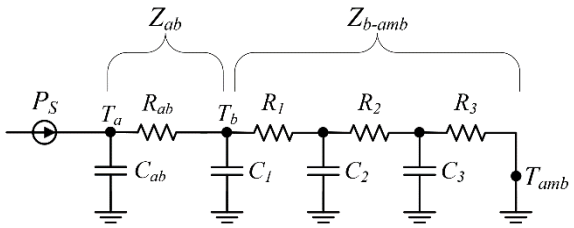

Fig. 5. Equivalent Cauer thermal network including the effect of the heat spreading in the *xy* plane of Figure 3 by the terms R_{ab}, C_{ab}.

Referring to Figure 3, the horizontal spreading in *x* and *y* direction is due only to copper tracks. Spreading effects due to the FR4 of the PCB can be neglected due to its poor thermal properties.

Starting from the above considerations, the heat transfer from a contact surface to the ambient was modeled as a series of two thermal impedances, evaluated as follows. T_a is defined as the surface-averaged temperature at the bottom of a pin, and as T_b the surface-averaged temperature at the top of its copper track. Usually $T_a > T_b$, because the Cu track helps in dissipating heat. Figure 5 shows the network topology, while in Figure 6 the pin is visually disconnected from its copper track for sake of clarity.

The first step is to calculate the time dependent thermal impedance between the Cu track and the ambient, $Z_{b\text{-}amb}(t)$:

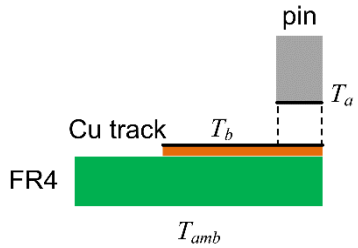

Fig. 6. Intermediate temperature points at a contact surface; pin is disconnected from its Cu track for sake of clarity.

$$Z_{b-amb}(t) = \frac{T_b(t) - T_{amb}}{P_s(t)} \qquad (7)$$

It is worth noting that, formally, Eq. (7) could not be applied, being valid only when $P_s(t)$ is a step function. However, this is a reasonable approximation that leads to a simple Foster model, which stages are determined by Eq. (8):

$$(t) \quad \sum \quad \left(1 \qquad ^{t/(R \qquad)}\right) \qquad (8)$$

As in Subsection 2.1, the maximum number N of stages was set, and the following objective function was minimized:

$$f_{obj}(t) = \sum_{t=t_{start}}^{t_{end}} \left(Z_{b-amb}(t) - Z^F_{b-amb}(t)\right)^2 . \qquad (9)$$

Acceptable results were obtained with 2÷4 stages.

The last step is to identify the two terms R_{ab} and C_{ab}. R_{ab} is obtained as:

$$R_{ab} = \frac{T_a - T_b}{P_S} . \qquad (10)$$

C_{ab} has to be determined iteratively after applying an algorithm based on Perturb & Observe (P&O) technique, which minimizes the difference between the original and the simplified response by operating on the time shift value τ_{ab}.

It is necessary to provide an initial guess τ_{ab0} for the unknown time constant τ_{ab} to guarantee the P&O algorithm convergence. A good guess value is given by $\tau_{ab0} = C_{ab0} \cdot R_{ab}$, where C_{ab0} is the thermal capacitance obtained from the volume of the copper trace outside the contact surface A_i.

As the full Cauer network is obtained, the transformation to the stack of equivalent materials is straightforward: once the thickness L of each layer is fixed, its thermal conductivity k_m [W/(m·K)] and

specific heat capacity ρC_{p_m} [J/(K·m^3)] are determined:

$$\_\_\_\_ \quad \_\_ \qquad (11)$$

Equation (11) has to be repeated for each of the M layers under a given contact surface, and clearly the full process has to be repeated for every contact surface between the device and the PCB to replace.

3. Simulation cases

In this section, two applications of the above explained method will be shown. A D2PAK and a SO-8 packaged device were chosen, in order to study different topologies. The first one is a three-terminals device. Assuming a MOSFET, then gate and drain are wire-bonded to the output pins, while the source is connected via the bottom flange. This gives rise to a 3D FE model with three copper tracks on the PCB, while the second one is an eight-pin bondless device mounted on a PCB with three copper tracks. Both devices have been simulated under two different sets of boundary conditions:

1) The lower surface, opposite to the device side, set at a fixed temperature of 293 K; the remaining boundaries set as adiabatic.
2) All the boundaries set with constant convective heat flux h = 10 W/(m^{2}K).

Table 1 summarizes all the models used to evaluate the effectiveness of this approach, that are four original models and four simplified models, giving a mnemonic code for everyone, that will be used in the next.

Table 1
3D FE models drawn for the two case studies, and mnemonic coding to use for sake of nomenclature.

Package	Boundary conditions setup	Mnemonic code	
		Original model	Simplified model
D2PAK	1	D2PAK_F_O	D2PAK_F_S
D2PAK	2	D2PAK_H_O	D2PAK_H_S
SO-8	1	SO8_F_O	SO8_F_S
SO-8	2	SO8_H_O	SO8_H_S

The D2PAK model was previously used and validated against measurements, even though a different set of boundary conditions was chosen [9].

3.1 D2PAK packaged device

The first two simulation cases refer to a D2PAK packaged device. The 3D FE models of the original structure of the D2PAK mounted on a PCB are shown in Fig. 7(A) for both boundaries setup considered simulation cases. They allowed generating the simplified models, whose boundary conditions are shown in Fig. 7(B). Fig. 7(C) highlights some details of the device. Fig. 8 shows the stacks obtained for boundaries setup 1 and 2: the number of layers needed is 4 and 3, respectively. The obtained *RC* stages of the Cauer networks for D2PAK_F_S and D2PAK_H_S are listed in Table 2.

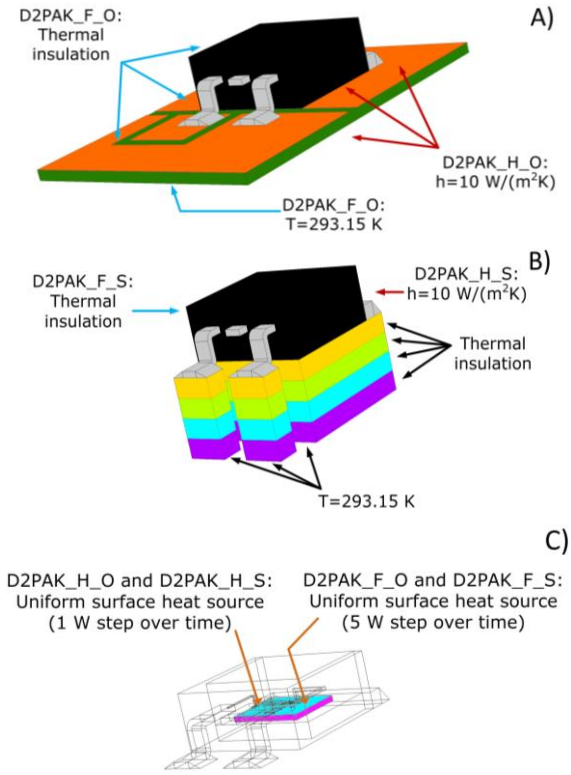

Fig. 7. 3D FE models with the D2PAK packaged device: (A) original model; (B) simplified model; (C) D2PAK details.

The total number of layers necessary to create simplified models is arbitrary. However, the smaller the number of layers, the smaller the number of DoFs. The number of layers cannot be lower than three: two for $Z_{b\text{-}amb}$ plus one for Z_{ab}.

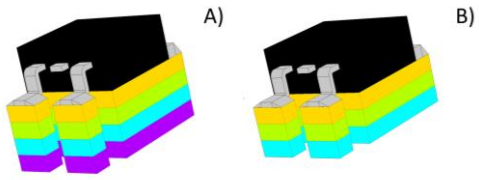

Fig. 8. FE simplified models with D2PAK packaged device: (A) D2PAK_F_S; (B) D2PAK_H_S.

The DoFs have been reduced by 53% and 54%, respectively in the two simulation cases, as shown in Table 3. Values between brackets in Table 3 represent the number of elements reduction related only to the PCB. It should be noted that the DoFs reduction depends on the shape of the copper tracks and on the PCB dimensions: with larger PCBs it is possible to obtain a higher DoFs reduction.

Table 2
D2PAK simplified models thermal resistances [K/W] and capacitances [J/K] in Cauer representation.
Legend: A_1 = gate, A_2 = source, A_3 = drain.

Model – Contact area		Layer 0	Layer 1	Layer 2	Layer 3
D2PAK_F_S - A_1	R	8.45	23.47	40.71	4.58
	C	0.024	0.039	0.089	2.97
D2PAK_F_S - A_2	R	29.25	4.23	8.76	0.73
	C	0.015	0.22	0.43	20.29
D2PAK_F_S - A_3	R	1.83	2.44	5.21	0.58
	C	0.0036	0.18	0.40	19.07
D2PAK_H_S - A_1	R	11.85	507.9	448.6	-
	C	0.017	0.11	0.25	-
D2PAK_H_S - A_2	R	42.46	270.1	57.23	-
	C	0.033	0.52	1.21	-
D2PAK_H_S - A_3	R	2.44	82.25	81.2	-
	C	0.58	0.65	1.52	-

To validate the approach here presented, the temperature behavior of different points of interest lying in the silicon chip was considered. Here, the error between the original and the simplified model is reduced thanks to the fine-tuning procedure previously explained.

Table 3
DoFs of the FE models set for the D2PAK.

Model	Entire model	Only Device	% Reduction of DoFs Ent. model (Only PCB)
D2PAK_F_O	24413	9965	-
D2PAK_F_S	11476	9765	53% (88%)
D2PAK_H_O	24413	9965	-
D2PAK_H_S	11221	9765	54% (90%)

Fig. 9 and Fig. 10 show the evolution over the time of the temperature increase in the middle point of top surface of the chip, highlighting the error, for the two simulation cases with fixed temperature at the bottom surface of the PCB and convective heat flux all around the structure.

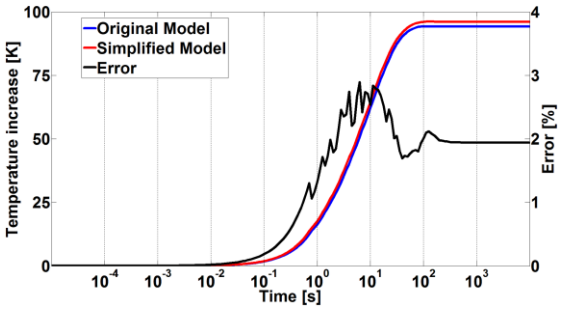

Fig. 9. Temperature increase in the middle point of the chip for D2PAK_F_O and D2PAK_F_S. Maximum error is almost 3% at t = 8 s.

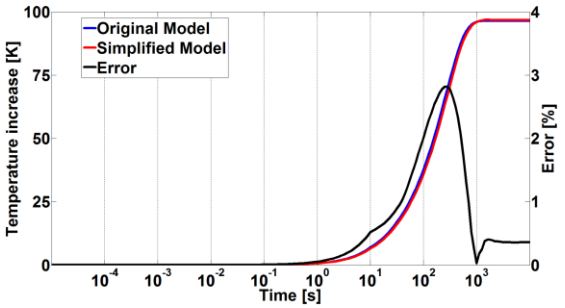

Fig. 10. Temperature increase in the middle point of the chip for D2PAK_H_O and D2PAK_H_S. Maximum error is almost 3% at t = 251 s.

The error in locations further away from the contact surfaces, e.g., on top of the package, was checked in addition.

In both simulation cases, the temperature distribution at the time of maximum error in the center of the chip top surface was checked. Fig. 11(A) and Fig. 11(B) show a slice of the structure on chip top surface in D2PAK_F_S and D2PAK_F_O simulation cases, while Fig. 12(A) and Fig. 12(B) show the evolution of temperatures on the entire structure in D2PAK_F_S and D2PAK_F_O simulation cases at the same time. Similarly, Fig. 13(A) and Fig. 13(B) show a slice in D2PAK_H_O and D2PAK_H_S simulation cases, while Fig. 14(A) and Fig. 14(B) show the entire structure. In this case a maximum error of 3% was found, below the 5% threshold set at the beginning.

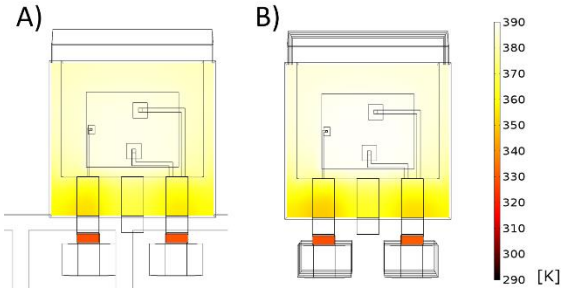

Fig. 11. Temperature distribution at the time of maximum error in a slice (top surface of the chip) of simulation cases (A) D2PAK_F_O and (B) D2PAK_F_S.

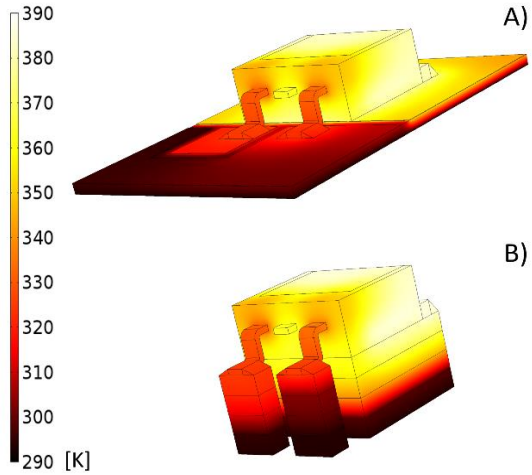

Fig. 12. Temperature distribution at the time of maximum error in a 3D plot of simulation cases (A) D2PAK_F_O and (B) D2PAK_F_S.

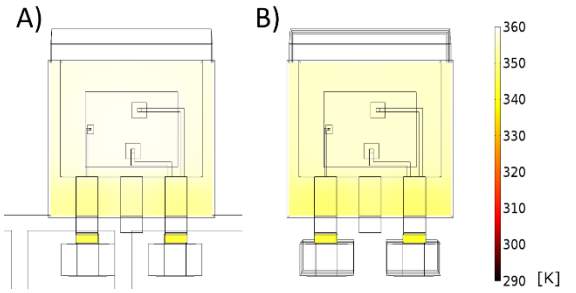

Fig. 13. Temperature distribution at the time of maximum error in a slice (top surface of the chip) of simulation cases (A) D2PAK_H_O and (B) D2PAK_H_S.

3.2 SO-8 packaged device

The second case study is an SO-8 bondless device, featuring more pins than a D2PAK. Here, some pins share the same copper track, increasing simulation complexity. Fig. 15 shows the original and the simplified model of all four simulation cases.

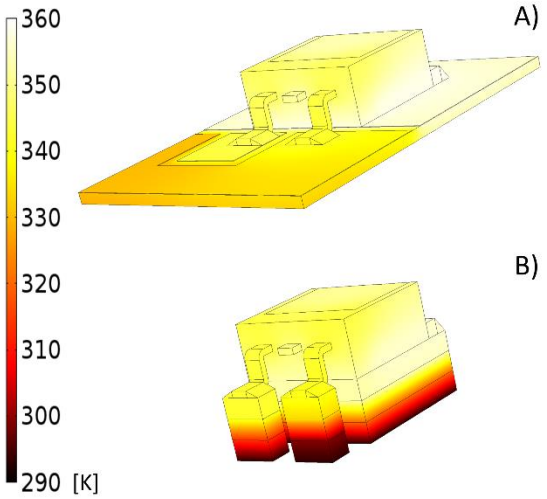

Fig. 14. Temperature distribution at the time of maximum error in a 3D plot of simulation cases (a) D2PAK_H_O and (b) D2PAK_H_S.

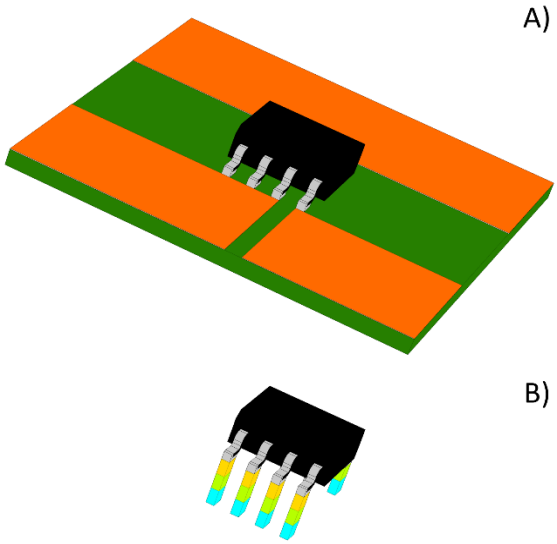

Fig. 15. SO-8 device packaged, (A) original models SO8_F_O, SO8_H_O and (B) simplified models SO8_F_S and SO8_H_S.

In this case, three layers in each stack were necessary (see Figure 15(B)). This particular model did not allow a high DoFs reduction, in fact only a reduction by 13% (91% referring to the only PCB) is feasible. This is due to contact surfaces, since SO-8 package features thin pins which already require a fine mesh, which cannot be furtherly coarsened.

Results about the quality of simplified models subjected to simulation cases are visible in Fig. 16 and Fig. 17 for SO8_F and SO8_H, respectively. The

maximum error is less than 2% and 4%, respectively, and it happens at the instants 9 s and 89 s, respectively.

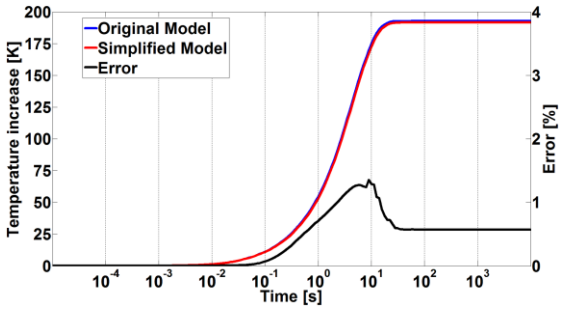

Fig. 16. Temperature increase in the middle point of the chip for SO8_F_O and SO8_F_S. Maximum error is 2% at t = 9 s.

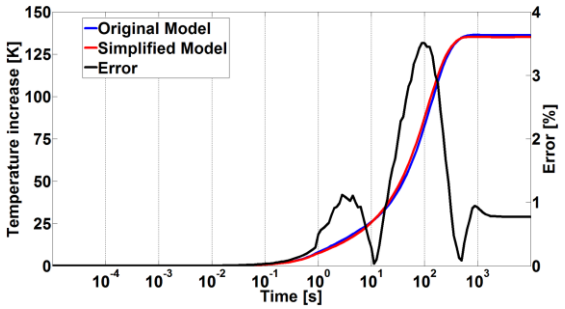

Fig. 17. Temperature increase in the middle point of the chip for SO8_H_O and SO8_H_S. Maximum error is 4% at t = 89 s.

4. Summary and conclusions

In this paper, a method to derive simplified 1D models able to take into account the effects of PCB and environmental conditions on a generic power device was introduced, as well as a way to implement them in a FE solver. This method accounts for the heat-spreading effect due to the copper tracks as well; it has been shown that neglecting this effect leads to poor modeling results.

The approach was successfully applied to two different simulated structures. A strong reduction of the PCB modeling complexity was achieved.

Concluding, it has been shown that it is possible to retain the geometrical details inside a packaged device even in the case of long pulses, by substituting the complex PCB model with a simpler material stack. This method could be useful in subsequent analysis at chip level, for instance to investigate the effect of small defects on the chip response.

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