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Estimation of DAC Weighting Capacitors Mismatch in Pipelined ADCs Employing Finite Gain Op-Amps.

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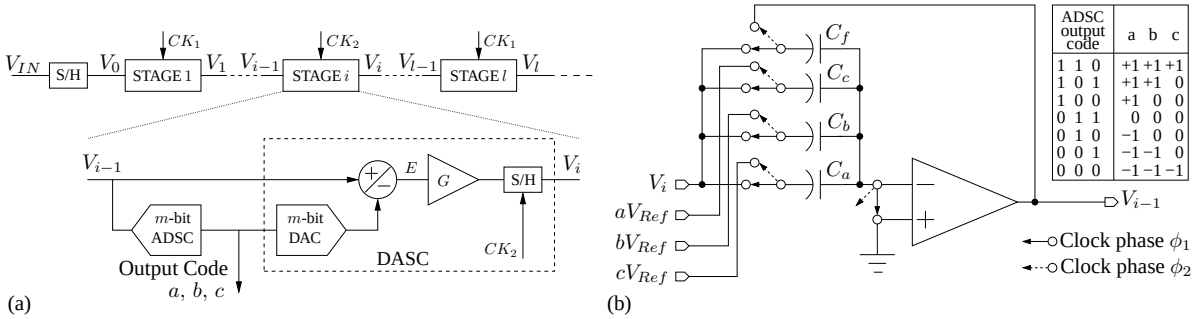
***Abstract*-** A D/A subconverter (DASC) error correction scheme based on weighting capacitor rotation is adapted to account for finite op-amp gain. Simulations show that reasonable estimates of capacitor mismatch can be obtained even if the actual gain is replaced by a nominal gain differing by as much as a factor of two.
DASC capacitor mismatch might therefore be estimated in the foreground at power-up, and most part of the corresponding mismatch noise and mismatch-induced interstage gain error might be cancelled, possibly delegating to a background calibration the task of correcting the remaining interstage gain error, induced by finite op-amp gain and drift with temperature.

I. Introduction

Pipelined A/D converters are the preferred choice for low-power applications requiring high speed and medium-high resolution, when a moderate amount of latency is tolerated.
The architecture of a pipelined A/D converter is shown in Figure 1. Each stage in the pipeline includes an analog-to-digital sub-converter (ADSC) and a digital-to-analog sub-converter module (DASC), including a DAC, a subtractor, a residue amplifier and a sample-and-hold amplifier.



ADSC output code	a	b	c
1 1 0	+1	+1	+1
1 0 1	+1	+1	0
1 0 0	+1	0	0
0 1 1	0	0	0
0 1 0	−1	0	0
0 0 1	−1	−1	0
0 0 0	−1	−1	−1

Figure 1. (a) A pipelined A/D converter. (b) Simplified model of a 2.5-bit DASC with 4 equal weigthing capacitors. During clock phase ϕ_2, capacitors C_a, C_b and C_c are connected, respectively, to aV_{Ref}, bV_{Ref} , and cV_{Ref}.

Each stage in the pipeline processes the residue V_{i-1} from the previous stage. V_{i-1} is measured by an analog-to-digital sub-converter ADSC, whose output drives an m-bit DAC. If the DAC output level corresponds to the centre of the quantisation cell where the input is classified, the output E of the subtractor block represents the quantisation error of the ADSC. E is then amplified by a suitable gain G, so that all the stages in the pipeline may operate on signals of comparable level, and fed to a S/H which provides residue V_i to the following stage.
ADSC non-linearity can be easily eliminated by digital correction [1], which requires a few additional decision levels in the ADSC and output levels in the DASC. The discussion which follows refers to a 2.5-bit ADSC $(G = 4)$ with 6 decision levels, driving a 2.5-bit DAC with 7 output levels by means of three, 2-bit output signals a, b, c.
A simplified DASC circuitry is shown in Figure 1(b) in single-ended form. Unlike the correction of ADSC non linearities, correction of interstage gain errors and DASC non linearity errors poses significant challenges. Mismatch between the DASC weighting capacitors contributes both to the so called "mismatch noise" and to interstage gain error. Several techniques reported in the literature [2, 3, 4, 5, 6] allow estimating mismatch, and canceling its effects provided the op-amp gain is infinite; a recent survey of the state of the art can be found in [7].
The method proposed in [6] for the calibration of a 2.5 bit DASC requires rotating the position of the four nominally equal weighting capacitors at each sampling instant, according to predefined pseudo-random-noise (PN) sequences.

By estimating the correlation between the measured residue of the stage to be calibrated and the PN sequences, it is possible to quantify the errors of the weighting elements and thus compute, in real time, digital correction terms to be added to the raw ADSC output. This allows achieving a considerable improvement of the noise floor, if the op-amp gain may be considered infinite.
The technology trend towards low supply voltages and low power consumption encourages, on one hand, the use of op-amps with low and inaccurate voltage gain, and on the other hand the use of weighting capacitors of the smallest size compatible with noise specifications, in order to reduce the op-amp bias current for equal clock frequency. Thus interstage gain error is no longer determined by capacitor mismatch only, but also by the uncertainty affecting op-amp gain, while mismatch noise becomes more relevant since relative mismatch increases with decreasing capacitor size.
Thanks to capacitors' stability, capacitor mismatch alone can be approximately determined at power-up even if a poor estimate of op-amp gain is available: this enables partial cancellation of mismatch noise and approximate correction of that part of interstage gain error which depends upon mismatch. The task of correcting the remaining interstage gain error, induced by finite op-amp gain and gain drift with temperature, can then be delegated to a background calibration technique like that described in [8].
This paper reconsiders the mismatch calibration procedure described in [6] taking finite op-amp gain into account, and demonstrates that useful mismatch estimates can be obtained even if the op-amp gain is known with poor approximation.

II. Capacitors' mismatch estimation in the case of finite op-amp gain

With reference to the switched capacitor DASC of Figure 1(b) during clock phase ϕ_1, input voltage V_{i-1} is processed by the 2.5-bit flash ADSC, which provides the three 2-bit output signals a, b, and c described in the insert of the figure. In the same phase the $G = 4$ identical capacitors are pre-charged to V_{i-1}, so that the total charge stored on the four capacitors is $Q = V_{i-1}(C_a + C_b + C_c + C_f)$. In phase ϕ_2, the bottom switch is connected to the amplifier's inverting input, capacitor C_f is placed in the feedback loop while the other capacitors are connected to ground or to $\pm V_{Ref}$ depending on the ADSC outputs a, b, and c, V_{Ref} being the reference voltage.
Leaving $C_a = C_0(1 + \varepsilon_a)$, where C_0 is the average of the four capacitances and ε_a is the relative weighting error, and similarly for C_b, C_c, C_f, it turns out that $\varepsilon_a + \varepsilon_b + \varepsilon_c + \varepsilon_f = 0$. Assuming an op-amp gain A_v, the residue is $V_i = V_{i-1} \cdot C_0G/(C_f + C_0G/A_v) - V_{Ref} \cdot (aC_a + bC_b + cC_c)/(C_f + C_0G/A_v)$. By recalling that the quantisation error of the ADSC is $E = V_{i-1}/V_{Ref} - (a + b + c)/G$, the residue, normalised to V_{Ref}, becomes

$$\widehat{V_i} \triangleq V_i/V_{Ref} = \frac{GE}{1 + \varepsilon_f + \frac{G}{A_v}} - \frac{a\varepsilon_a + b\varepsilon_b + c\varepsilon_c}{1 + \varepsilon_f + \frac{G}{A_v}} \tag{1}$$

Here, $G = 4$ is the nominal gain of the 2.5-bit DASC, and the difference $\widehat{V_i} - GE$ represents the error arising from capacitor mismatch in the DASC and finite op-amp gain. Finite op-amp input capacitance C_p and unity-gain bandwidth, neglected here, should be taken into account [9] if comparable to C_0G, to the sampling frequency, respectively . Op-amp gain variation with input signal level can probably be covered by combining capacitor mismatch estimation in the foreground with an interstage gain calibration procedure operating in background mode and covering non-linear effects in the interstage amplifier [8].
Eq. (1) can be used for the correction of DASC errors, once estimates of $\varepsilon_a, \varepsilon_b, \varepsilon_c, \varepsilon_f$ and of the op-amp gain A_v are available.
By linearizing (1), under the assumption of small ε's and $G \ll A_v$,

$$\widehat{V_i} = V_i/V_{Ref} \quad \cong \quad GE - \left(a\varepsilon_a + b\varepsilon_b + c\varepsilon_c + GE\varepsilon_f + G^2 \frac{E}{A_v} \right). \tag{2}$$

The calibration procedure proposed in [6] assigns, at each sampling instant, the role of C_a, C_b, C_c, and C_f to a different arrangement, obtained by rotation, of the four capacitors $\{C_1, C_2, C_3, C_4\}$ physically present in the DASC. The assignment is controlled by two zero-mean, PN sequences P_0 and P_1, with values ± 1, according to Table 1. By simple algebra, following step by step the procedure described in [6], ε_a may be written in the form

$$\varepsilon_a = \frac{1}{G} \{ -P_0(\Delta_2 + \Delta_3) - P_1\Delta_1 + P_1P_0(\Delta_2 - \Delta_3) \} \tag{3}$$

where

$$\Delta_1 = \varepsilon_1 + \varepsilon_2 - \varepsilon_3 - \varepsilon_4; \qquad \Delta_2 = \varepsilon_1 - \varepsilon_2; \qquad \Delta_3 = \varepsilon_3 - \varepsilon_4. \tag{4}$$

P_1	P_0	C_a	C_b	C_c	C_f
-1	-1	C_1	C_2	C_3	C_4
-1	$+1$	C_2	C_3	C_4	C_1
$+1$	-1	C_3	C_4	C_1	C_2
$+1$	$+1$	C_4	C_1	C_2	C_3

Table 1. Capacitor rotation scheme

Similar expressions can be derived for $\varepsilon_b, \varepsilon_c, \varepsilon_f$: by substituting these in (2)

$$\widehat{V_i} = \frac{V_i}{V_{Ref}} = GE\left(1 - \frac{G}{A_v}\right) - \frac{1}{G}\Big[P_0(\Delta_2+\Delta_3)(-a+b-c+GE) + \quad .$$
$$+P_1[\Delta_1(-a+c) + (\Delta_2-\Delta_3)(b-GE)] + P_1P_0[(\Delta_2-\Delta_3)(a-c) + \Delta_1(b-GE)]\Big]. \tag{5}$$

Note that, taking the expectation value of both sides of (5), it is found that

$$\mathcal{E}\{GE\} = (1 - G/A_v)^{-1}\,\mathcal{E}\left\{\widehat{V_i}\right\}, \tag{6}$$

since the terms in the large square bracket are products of PN sequences like P_0,P_1 and P_0P_1 with sequences, like $(-a+b-c+GE)$ or $(-a+c)$ which depend only upon the ADSC and the input signal, and are uncorrelated with the previous ones. It is thus natural to consider $\overline{GE} = \widehat{V_i}/(1-\frac{G}{A_v})$ as a noisy estimate of GE.
Assuming at first that $(-a+b-c)$ and GE are independent processes and that P_1 and P_0 are orthogonal sequences, so that $\mathcal{E}\{P_1P_0\} = 0$, if the zero-distance correlation A between the sequence of residues $\widehat{V_i}$ and the sequence $P_0(-a+b-c)$ is computed, only the term multiplying the unknown $\Delta_2+\Delta_3$ survives:

$$\begin{aligned} A &= \mathcal{E}\left\{\widehat{V_i}P_0(-a+b-c)\right\} \\ &= -\frac{(\Delta_2+\Delta_3)}{G}\left[\mathcal{E}\left\{(-a+b-c)^2\right\} + \mathcal{E}\{-a+b-c\}\cdot\mathcal{E}\{GE\}\right]. \end{aligned} \tag{7}$$

Quite similarly

$$\begin{aligned} B &= \mathcal{E}\left\{\widehat{V_i}P_1(-a+c)\right\} \\ &= -\frac{\Delta_1}{G}\mathcal{E}\left\{(-a+c)^2\right\} - \frac{(\Delta_2-\Delta_3)}{G}\cdot\left[\mathcal{E}\{b(-a+c)\} - \mathcal{E}\{-a+c\}\,\mathcal{E}\{GE\}\right], \end{aligned} \tag{8}$$

assuming $(-a+c)$ and GE as independent, and

$$\begin{aligned} C &= \mathcal{E}\left\{\widehat{V_i}P_1P_0(a-c)\right\} \\ &= -\frac{\Delta_1}{G}\left[\mathcal{E}\{b(a-c)\} - \mathcal{E}\{a-c\}\,\mathcal{E}\{GE\}\right] - \frac{(\Delta_2-\Delta_3)}{G}\mathcal{E}\left\{(a-c)^2\right\}. \end{aligned} \tag{9}$$

Now $\mathcal{E}\{GE\}$ can be replaced by the expression in (6), A_v by its nominal value A_{vnom}, and the expectation values can be computed as exponential moving averages requiring knowledge of the sequences a, b, c, available at the ADSC output, and $\widehat{V_i}$, the calibrated output of the back-end of the considered stage. At this point the three linear equations (7), (8), (9) may be solved in terms of the unknowns Δ_1, $\Delta_2+\Delta_3$ and $\Delta_2-\Delta_3$. In the following, this approach will be referred to as procedure "five", since it leads to a system matrix with five non zero elements.

However, as it will be shown in the next section, the mismatch estimates obtained by this procedure are fair, but not sufficient to improve to the desired level the performance of the pipeline converter. Thus, the validity of the assumptions behind (7) (8) and (9) was questioned.
It was remarked that, since during real world operation the input signal is unknown, the only possibility is replacing GE by the estimate $\overline{GE}$. Correlations (7), (8) and (9) were therefore evaluated, in simulation, removing any assumption of incorrelation between the amplified quantization error $GE \simeq \overline{GE}$, the ADSC outputs a, b, c, and the PN sequences P_0 and P_1. A, for instance, was evaluated as

$$
\begin{aligned}
A &= \mathcal{E}\left\{\widehat{V}_i P_0(-a+b-c)\right\} \\
&= \mathcal{E}\left\{P_0(-a+b-c)\overline{GE}(1-G/A_v)\right\} - \frac{(\Delta_2+\Delta_3)}{G}\left[\mathcal{E}\left\{(-a+b-c)(-a+b-c+\overline{GE})\right\}\right] + \\
&\quad -\frac{\Delta_1}{G}\left[\mathcal{E}\left\{P_0P_1(-a+b-c)(-a+c)\right\} + \mathcal{E}\left\{P_1(-a+b-c)(b-\overline{GE})\right\}\right] + \\
&\quad -\frac{(\Delta_2-\Delta_3)}{G}\left[\mathcal{E}\left\{P_0P_1(-a+b-c)(b-\overline{GE})\right\} + \mathcal{E}\left\{P_1(-a+b-c)(b-\overline{GE})\right\}\right] \qquad (10)
\end{aligned}
$$

Now $\overline{GE}$ is proportional to $\widehat{V}_i$ and therefore depends on the capacitor permutation, and thus on P_0 and P_1, and also depends on a, b, c. Therefore, the expectations appearing in (10) can make all the three coefficients of the unknowns $\Delta_1, \Delta_2+\Delta_3$ and $\Delta_2-\Delta_3$ non negligible, and indeed this was confirmed by simulations. Similar considerations hold when B and C are evaluated without incorrelation assumptions.
A problem arises from the first terms on the r.h.s., which become coincident with the term on the l.h.s. if $\overline{GE}$ is used in place of GE, making the system homogeneous, i.e. with null trivial solutions. With some surprise, however, it was experimentally verified that, if the first term at the r.h.s. of (10) and the likes is ignored (forced to zero), a system leading to a considerable improvement of the mismatch estimates is obtained. This second approach, supported only by the experimental evidence of improved performances, will hereafter be referred to as procedure "nine", since all the nine system matrix elements may be non negligible, depending on the mismatch and on the signal statistics.
Once the solutions $\overline{\Delta_1}$, $\overline{\Delta_2+\Delta_3}$ and $\overline{\Delta_2-\Delta_3}$ are known, by combining them with (3) and companions, expressions of the estimates $\overline{(1+\varepsilon_f)}$ and of $\overline{(a\varepsilon_a+b\varepsilon_b+c\varepsilon_c)}$ in terms of P_0, P_1, $\overline{\Delta_1}$, $\overline{\Delta_2+\Delta_3}$, and $\overline{\Delta_2-\Delta_3}$ are easily obtained, so that a rough estimate of GE may be obtained from (1), by replacing the op-amp gain with its nominal value. Note that the computation of the mismatch estimates $\overline{\Delta_1}$, $\overline{\Delta_2+\Delta_3}$ and $\overline{\Delta_2-\Delta_3}$, and the accumulations required to estimate the expected values can be carried out only at power-up. Only the calculations related to the correction of mismatch noise (and, in case, some calculations related to interstage gain calibration) require real time processing and substantially contribute to power dissipation.

III. Simulation results

The performance of the procedure for the estimation of mismatch parameters Δ_1, $\Delta_2+\Delta_3$ and $\Delta_2-\Delta_3$ in the case of finite gain of the op-amp was investigated, using Matlab-Simulink, by functional simulation of a pipeline formed by a 2.5-bit front-end stage followed by an ideal 12 bit back-end converter. Blocks describing the operation of the front-end were implemented using a floating point representation of the analog data within the pipeline. They include the ADSC with the error correction logic described in [1], the DASC/subtractor/amplifier and the capacitor rotation logic. Expectation values were estimated as exponential averages.
A first set of simulations aims at comparing the estimation error of procedures "five", Figure 2(a), and "nine", Figure 2(b), with different capacitor sets. The figures summarize the results of 100 simulations where the values of the four nominally equal weighting capacitors were extracted from a gaussian distribution with a standard deviation of 5% of the nominal value, and for each simulation the same PN sequences P_0, P_1 were used, with seeds chosen as large prime numbers. The dots represent the Δ_1 estimation error, i.e. the difference between the value of $\overline{\Delta_1}$,

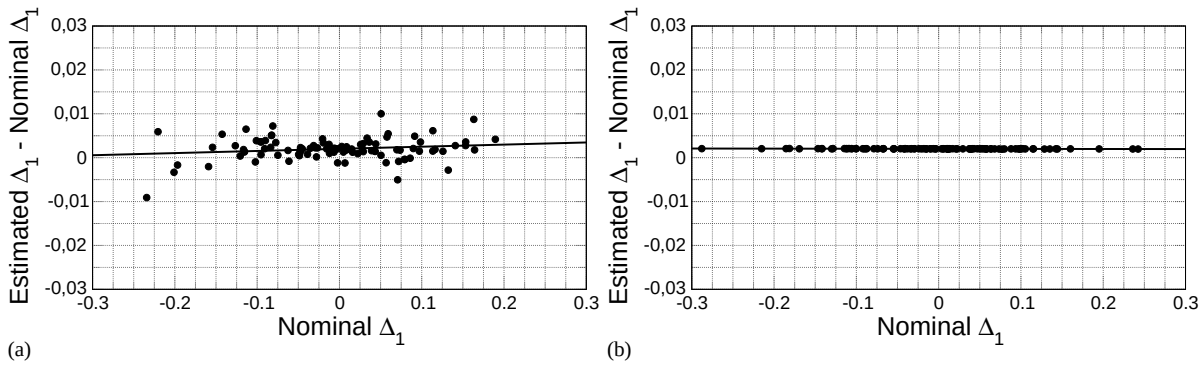


Figure 2. The graphs report the estimation error for mismatch parameter Δ_1 as a function of Δ_1 for $A_v = A_{vnom} = 10^6$, obtained (a) using procedure "five"; (b) using procedure "nine".

estimated using an averager time constant w of 10^5 time ticks, and the true value of Δ_1, known in simulation, as a function of the true value of Δ_1. It appears that the estimates obtained with procedure "nine" are affected by a much smaller dispersion than those of procedure "five". The two graphs correspond to a high value of the op-amp gain, $A_v = A_{vnom} = 10^6$, a condition in which the finiteness of the op-amp gain has limited impact. Besides a certain amount of dispersion, the estimation error includes an offset (intercept of the regression line) of about 2×10^{-3} plus a relative error (slope of the regression line) of -2×10^{-4} in the case of Figure 2(b).
In a similar experiment, where for each set of capacitors different PN sequences were used, with seeds chosen at random, the offset ($\approx 1.1 \times 10^{-4}$) virtually disappears , while the experimental dots are nearly as dispersed as those obtained by procedure "five" in Figure 2(a). This suggests that the offset in Figure 2(b) may be related to the specific sequences P_0, P_1 used, and of course, that the PN sequences should not be chosen at random.

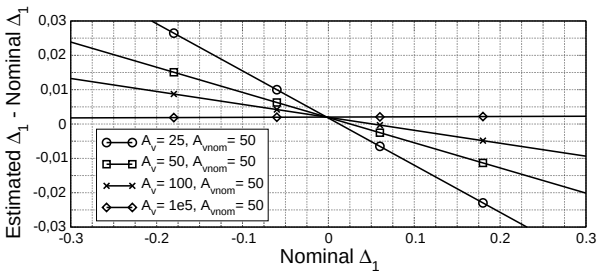
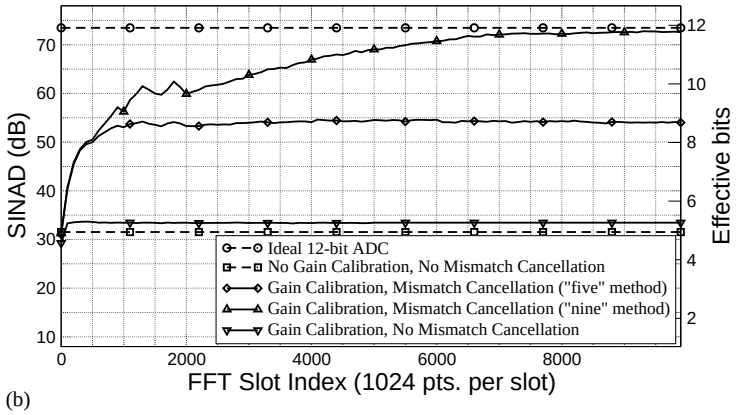


Figure 3. The regression lines for the Δ_1 estimation error obtained with procedure "nine" for different values of A_v and a fixed A_{vnom}.

Figure 3 represents the regression lines of the Δ_1 estimation error, obtained with procedure "nine" when $A_{vnom} = 50$ and $A_v = 25, 50, 100, 1 \times 10^5$, respectively, and demonstrates the strong influence of the true op-amp gain A_v on the relative error contribution: the largest the op-amp gain, the smallest the relative error term. For each value of A_v, similar slopes are obtained for Δ_2 and Δ_3; more noisy results were obtained with procedure "five". For both procedures "five" and "nine", on the contrary, the influence of the nominal op-amp gain A_{vnom} is minimal. The fact that the estimation error is not minimal when $A_v = A_{vnom}$ is rather surprising, anyway the results suggest that the relative error term is always negative and can be made small at desire, by ensuring that the actual op-amp gain never drops below a certain value.
Note that the estimates discussed so far were obtained using an ideal 12-bit back-end. In order to investigate the impact of a non-ideal back-end, simulations were carried out with back-ends with no linearity errors but different resolutions. It turned out that mismatch estimates are unaffected, provided the back-end resolution is larger than 6-bit and the input signal determines an amplified residue spanning most of the back-end input range.
In summary, irrespective of nominal op-amp gain, even with a low op-amp gain, the estimated values of the mismatch parameters are reasonably close to the exact values known in simulation. Therefore, the estimates thus obtained can be used to directly evaluate GE according to (1), in order to reduce mismatch noise, and to achieve an improvement of the complete converter performance.
Alternatively, mismatch estimation can be performed in the foreground, at power-up, and the estimates obtained can be used to approximately correct mismatch noise, while interstage gain calibration may be delegated to a background technique like that in [8], capable of tracking gain drifts.
In an experiment according to this last approach, mismatch estimation was performed in the first 2×10^6 conversion cycles, and the mismatch parameters were evaluated according to procedures "five" or "nine". Afterwards, the four capacitors were held in fixed positions, and the obtained estimates of ε_1, ε_2, ε_3, ε_4 were stored in memory.
The background interstage gain calibration algorithm was then activated, with mismatch noise subtraction according to (1) enabled.
The experiment simulated a 2.5-bit stage using a high nominal gain op-amp, with the four nominally equal weighting capacitors shown in 4(a), followed by an ideal 12-bit back-end, representing the rest of the pipeline after proper calibration, for a total of 14-bit. Assuming a target resolution of 12-bit, the converter performance was evaluated in terms of SINAD ratio calculated on the 12 MSBs of the output word. The interstage gain calibration was carried out with averaging time constant $w = 2 \times 10^5$ time ticks.
Figure 4(b) shows the evolution with time of the SINAD ratio of the entire converter as the estimate of interstage gain improves. The bottom line represents the SINAD of the converter if no calibration is performed; the top line the SINAD of an ideal 12-bit converter. The second line from the bottom shows that interstage gain calibration alone, without mismatch cancellation, brings limited improvement. The next line demonstrates a relevant improvement when interstage gain calibration is combined with mismatch noise cancellation according to procedure "five".

CAPACITOR	NORMALIZED CAPACITANCE	RELATIVE ERROR ε
C_1	0.8820	-0.0996
C_2	0.9339	-0.0467
C_3	1.0013	0.0222
C_4	1.1012	0.1241

(a)



(b)

Figure 4. Mismatch cancellation effect. (a) Capacitor test set. (b) The SINAD transient evolution during interstage gain calibration.

The best result however is obtained by interstage gain calibration combined with mismatch noise cancellation according to procedure ”nine”: this last combination allows to recover about three additional effective bits, and thus to achieve the target SINAD.

IV. Conclusions

A correlation-based procedure for mismatch parameters estimation proved its effectiveness even in the case of limited gain op-amps. A procedure with improved performances was defined on the basis of heuristic considerations. By combining foreground mismatch parameters estimation with background interstage gain calibration, real time tracking of op-amp gain drift is possible, and significant performance improvements can be obtained.

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