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1.2 Gb/s true PECL 100K compatible I/O interface in 0.35 μm CMOS

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Abstract

This paper describes the design and the implementation of input-output (I/O) interface circuits for serial data links in the Gb/s range. The cells were implemented in a 3.3 V-0.35 μm CMOS technology in a couple of test chips. The transmitter is fully compatible (DC coupling) with 100K positive emitter-coupled logic (PECL) systems and it is based on the voltage switching principle in order to allow different termination schemes besides the canonical ECL termination, i.e. 50 Ω towards (Vdd-2) V. The addition of some circuit techniques such as dynamic biasing and strobed current switching boosts the dynamic performance of the the basic voltge-switching scheme and relaxes the requirements for a high bias current and large-size output devices at the same time. Moreover, thanks to the developed reference circuit, using both feed-forward and feed-back controls, the output levels are within the 100K tolerance over the full range of process, supply voltage and temperature (PVT) variations without resorting to external components or on-chip trimming. The receiver cell is based on a complementary-differential architecture providing high speed and low error on the duty cycle of the CMOS output signal. The integrated receiver-transmitter chain exhibits a maximum toggle frequency of 1 GHz, while a chip-to-chip transmission link using the developed I/O interface was tested up to 1.2 Gb/s.

Keywords

CMOS integrated circuits, high-speed integrated circuits, input/output (I/O), back-plane drivers, emitter coupled logic.

I. Introduction

High-speed chip-to-chip signaling is one of the most significant bottlenecks in the design of several systems such as μ-processor motherboards, optical transmission links, intelligent hubs and routers, etc. In fact, while the increasing integration level of CMOS circuits has rapidly pushed the internal

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clock frequency of microprocessors and advanced ASICs into the GHz range, the chip-to-board signal frequency has increased at lower rates through silicon generations. Indeed, single-pin data rate is only partially affected by the integration level, while other aspects such as packaging and Printed-Circuit Board (PCB) technology have a significant impact on it. In recent years the ever increasing demand for higher data rates has been satisfied by massive parallelism, with the disadvantage of increased cost of packaging and PCB manufacturing. However, the Silicon Roadmap [1] forecasts that with the 100 nm generation (2006 year) the GHz limit will be surpassed for chip-to-board signaling in the case of peripheral busses. Even if novel standards such as LVDS [2], [3] exhibit superior performance in term of reduced power consumption, Positive Emitter Coupled Logic (PECL) is still a preferred choice in the design of very high-speed systems for compatibility with previous designs and hardware. Moreover, the maximum transmission speed for LVDS is limited to about 2 Gb/s [3].

Furthermore, the well known benefits in terms of cost reduction and increased density make desirable the implementation of I/O pad cells in low-voltage digital CMOS technology, thus avoiding additional masks for bipolar or 5 V devices. CMOS PECL transmitters may be implemented as switched current or switched voltage drivers, in order to provide standard PECL levels on the external termination resistor. Even though the switched current architecture was the preferred approach in previously published designs [4], [5], it supports only one termination scheme. On the contrary, switched voltage architectures [6] are more flexible and make available several termination schemes to the system engineer, provided that the output resistance is sufficiently low [7]. However, the constraints posed on the output resistance lead to large transistor sizes and additional power consumption due to multiple buffer stages. This may be a practical disadvantage if the transmitter has to be embedded in an ASIC with a large number of outputs.

This paper describes the design and the implementation of a PECL compatible CMOS I/O interface in digital 0.35 μm technology. The proposed PECL transmitter provides maximum compatibility to other PECL systems and it is based on a switched voltage architecture combined with additional

current switching which reduces the transition times and provides benefits in terms of power saving and smaller output devices. The driver supports both differential and single-ended transmission, with different termination schemes. Standard 100K levels and tolerance are provided with the canonical 50 Ω termination towards (V_{DD}-2) V [8], [7], [9]. The limits, in terms of a lower speed-to-power consumption ratio, of the switched voltage approach were overcome by revisiting known circuit techniques and by novel design solutions.

The implemented PECL receiver is based on a complementary-differential architecture which ensures a high toggle frequency and a low sensitivity of the duty cycle of the CMOS output signal to the process parameter variations.

The driver-receiver link was tested up to 1.2 Gb/s with random data patterns.

II. Transmitter

A PECL driver may be designed either as a switched voltage or a switched current source, Fig. 1. Traditional bipolar designs implement the voltage switching by means of an open emitter output stage, Fig. 2. A straightforward implementation of such a scheme in CMOS is impractical, unless low threshold voltage transistors are available, due to the reduced voltage headroom for the n-type follower when the output voltage is set to the high level ($V_{OH} = V_{DD} - 955$ mV). Therefore, implementation of the switched voltage principle rises several difficulties and involves the precision-speed trade-off, since the output levels have to be set within the required precision by means of a common-source p-MOS output stage with an active feedback loop [6]. This obviously poses stringent limitations in terms of bandwidth and rises stability problems in presence of a non negligible capacitive load. Therefore, feedback control must be avoided in Gb/s operation, but appropriate circuit solutions have to be developed in order to guarantee standard 100K level accuracy over the whole range of variation of process parameters, supply voltage and temperature (PVT). For this reason some proposed CMOS designs [4], [5] make use of the current switching principle. The main disadvantage of this scheme is that

the output levels exhibit the proper values only with a dedicated termination scheme. Changing the termination, i.e. the load resistor, largely affects the DC output level. Moreover, due to the high output impedance, source termination cannot be implemented. Note also that a recently proposed CMOS design [5] featuring very high speed operation requires a non canonical differential termination and can be coupled to PECL hardware only in AC mode. Moreover, a replica of the termination network and a reference voltage were externally provided in that design. The aim of the present design is to guarantee a full compatibility towards PECL systems, supporting DC coupling with both canonical and series termination. Moreover, in order to reduce both production and PCB manufacturing costs, standard PECL levels must be obtained over the full PVT range without resorting to external components or expensive wafer-level trimming procedures.

A brief review of the typical termination schemes used in ECL or PECL circuits is reported in Fig. 3. Besides the canonical (parallel) termination to the $V_{DD} - V_T$ voltage reference, with $V_T = 2$ V, a Thevenin termination, Fig. 3-b, can be used at the load end with the advantage that the additional V_T supply is avoided. With an appropriate choice of $R1$ and $R2$, the same loading condition as for the parallel termination is obtained, at the price of the highest power consumption. Series termination at the source end, Fig. 3-c, is an attractive alternative to the parallel termination because of the lower power consumption with respect to the Thevenin scheme, and of the highest suppression of reflected waves, e.g. caused by line-to-line crosstalk [10]. It should be noted that both Thevenin and series terminations increase the sensitivity of the output levels to the supply voltage.

On the basis of the considerations reported above the proposed PECL transmitter was designed as switched voltage driver with several modifications and improvements of the basic scheme. Indeed a combination of open-loop and closed-loop control guarantees standard PECL 100K levels over PVT variations without trimming or external references. Moreover, the implementation of circuit techniques such as variable biasing and strobed switched current boost the dynamic performance of the driver and relaxes the requirements for a high bias current and large-size output transistors. However, the

cell size of the proposed transmitter is larger than that of other reported designs based on the current-switching architecture, because of the unavoidable constraints posed on the output resistance, which must be low enough in order to benefit by the flexibility of the voltage switching principle. This may be regarded as a limit of the proposed driver, if embedded in ASICs with several high-speed outputs. Nevertheless, it should be noted that in the case of a transmission speed in the Gb/s-per-pin range, the number of output pins is usually limited.

A block diagram of the transmitter together with the DC biasing block and the external termination resistor is shown in Fig. 4. The required voltage references are obtained by means of a scaled replica circuit and a couple of feedback loops. The loading effect of the external termination resistor, R_T, is replicated by the internal resistors R_{TR} connected towards an internally developed voltage reference equal to $V_{DD} - V_T$, with $V_T = 2$ V. The canonical termination for ECL 100K gates was used as reference; indeed, the standard 100K output levels are specified under this loading condition [7]:

$$\begin{aligned} V_{DD} - 1.025\,V \quad &< \quad V_{OH} < V_{DD} - 0.880\,V \\ V_{DD} - 1.810\,V \quad &< \quad V_{OL} < V_{DD} - 1.620\,V \end{aligned} \tag{1}$$

Unlike conventional PECL, in CMOS designs V_{DD} may be lower than 5 V. In the proposed design, standard 100K levels must be guaranteed with canonical termination over the full process tolerance range and the operating temperature range for industrial applications, i.e. $-40°C \div 85°C$, together with a 3 V $\div$ 3.6 V variation of the power supply. Moreover, with respect to the junction temperature, the range must be increased in order to accommodate the thermal resistances associated to the package and the power consumption of the ASIC embedding the proposed cells. To this aim, simulations were carried out over an extended (junction) temperature range, i.e. $-40°C \div 125°C$.

A. Transmitter Circuit

The schematic diagram of the proposed PECL driver is shown in Fig. 5. CMOS inverters $INV1,2$ buffer the input signals V_{IN+}, V_{IN-}, and drive the differential stage *M1*, *M2* with resistive load. Source

follower *M3A* (*M3B* for the negative output) reduces the capacitive load at the output of the differential amplifier and provides an adequate level shifting. The output stage consists of p-MOS followers *M4A* and *M4B* with dynamic biasing and pull up/down boosting. Dynamic biasing was introduced in order to minimize the transition time of the output voltage without increasing the power consumption of the output stage. Indeed, the main limits of a class-A biased output stages are the large power consumption and the conflicting requirements posed on the bias current by the need of achieving short rising and falling transition times. In fact, approximate expressions of the maximum rate of change of the voltage at the output of a p-type source follower with capacitive load (C_L) for the rising and falling transition are reported below:

$$\left|\frac{d\,V_{OUT}}{d\,t}\right|_{UP} \leq \frac{I_{BIAS}}{C_L} \tag{2}$$

$$\left|\frac{d\,V_{OUT}}{d\,t}\right|_{DOWN} \leq \frac{\frac{K'_P}{2\,\alpha}\frac{W}{L}\,(V_{SG-MAX}\,-V_T)^2\,-\,I_{BIAS}}{C_L} \tag{3}$$

where I_{BIAS} is the bias current, α is the first derivative of the threshold voltage (V_T) with respect to the (substrate-referred) channel potential [11] and V_{SG-MAX} is the maximum source-to-gate voltage of the p-MOS follower at the high-to-low transition. It appears that, the rising transition benefits by a larger bias current, while the falling transition does not. A better efficiency can therefore be achieved by means of the dynamic biasing shown in Fig. 5 where a constant current, I_3, is always provided to the output stage, while an additional current, I_4, is provided by *M7A* (*M7B*) only when the output is in the high state. Therefore two different values of bias current are used in the falling and rising transition, so as to optimize both of them as indicated in (2),(3), while minimizing the power consumption. I_3 is set to the typical current required by the external $50\,\Omega$ resistor with the output in the low state (5.7 mA), with an addition of about 9 mA for the bias of *M4A* (*M4B*). Switched current generator *M7A* (*M7B*) provides the additional current (about 15 mA) required by the termination resistor when the output is in the high state. Therefore, dynamic biasing has the further advantage of keeping the bias current of the p-MOS device almost constant between different logic states. This

leads to an almost constant output resistance, which is useful in the case of series termination.

The reduced current through the p-MOS device leads to a lower size ratio, provided that (3) is satisfied, with benefits in terms of lower area and parasitics. In order to further reduce the transition times of the voltage at the driver output, a strobed current switching was added to the driver. Indeed, a couple of pulsers, *BP* and *BN*, provide a current pulse at the low-to-high, *BP*, and at the high-to-low transition, *BN*. The schematic diagrams of these blocks are reported in Fig. 6 [5]. With reference to the p-type pulser, signal $\overline{A}$ of Fig. 5 is provided to the drain and, through the delay line obtained by means of inverters $IN1$ and $IN2$, to the gate of of $M1A$. After the high-to-low transition $M1A$ is turned on for a short time, roughly corresponding to the delay introduced by *IN1* and *IN2*. Therefore, $M3A$ is switched on for this short period of time, providing a pulsed current at the driver output. The amount of delivered charge exhibits a little dependence on the process parameter variations, since the slower the devices, the larger the delay introduced by the inverters and the lower the peak current provided by $M3A$.

Fig. 7 shows the simulated waveforms of the proposed transmitter in presence of a 10 pF load at each output; the layout parasitics were included together with lead-frame and bond-wire inductance of the plastic SOIC package used for the experiment. A transition time lower than 400 ps and an input-output delay of 600 ps were achieved with the circuit of Fig. 5. Note that if the pulsers *BN* and *BP* were removed from the circuit, the transition time would increase up to about 800ps, under the same loading conditions.

The DC output levels are set by means of p-MOS transistor *M5* at the head of the differential stage and by the tail current generator $M8$, Fig. 5. Variable resistor $M5$ is used for setting the DC output high level, V_{OH}. $M8$ provides an additional tail current, I_S, to the differential stage, thus affecting the output swing and, consequently, the lower output level, V_{OL}. Current generator $M6$ avoids that the control current I_S flows through the variable resistor $M5$, thus decoupling the two control actions, as explained in the next section.

B. Transmitter Biasing

The voltage references V_{CL} and V_{CH} at the gate of the tail current generator $M8$ and of the variable resistor $M5$, Fig. 5, are provided by the DC biasing circuit in Fig. 8 based on a 10-times scaled replica of the transmitter. The feedback loop through amplifier $OP1$ sets the correct gate voltage V_{CH} by controlling the high voltage level, while $OP2$ sets the proper tail current in the differential stage in order to achieve the correct value for the lower output level. The voltage references V_{OH-REF}, V_{OL-REF} and V_T are internally developed from a bandgap circuit. The main problem arising in the circuit of Fig. 8 is the coupling between the two feedback loops, leading to difficult start-up and instability. Indeed if $M6$ were not introduced, any variation of the additional tail current I_S would affect also V'_{OL} (V_{OL} in Fig. 5) through the variable resistor $M5$. On the contrary, in the proposed circuit, only the constant tail current $I_1/10$ (I_1 in Fig. 5) flows through $M5$, while the controlled tail current $I_S/10$ (I_S in Fig. 5) is diverted from $M5$ by current generator $M6$, coupled to $M8$. Therefore, at start-up V_{CH} is set and the correct value of V_{OH} is achieved at the output. Then, the proper swing is determined across the resistor in the differential stage and the correct value of V_{OL} is established. It should be remarked that the compensation of op.amp.s $OP1$ and $OP2$ deserves some attention because of the voltage gain contributed by the feedback networks. A sufficient stability margin for the feedback loop providing V_{CH} was achieved by designing $OP1$ as a single stage amplifier with a pole-zero compensation network around $M5$, not shown in Fig. 8 for simplicity.

The simulated DC output levels of the proposed transmitter over the extended temperature range ($-40 \div 125\,°C$) and at different values of the supply voltage are always within the allowed tolerance, as shown in Fig. 9-a. Nevertheless, Monte-Carlo simulation considering random mismatch and PVT variations reveals a non negligible fraction of samples whose output levels are outside from the allowed 100K bounds, Fig. 9-b,. These errors are mostly due to the shift of the reference resistors R_{TR} in Fig. 8 from the nominal value of 500 Ω. Even though this error is neither critical for the receiver developed in this design context, nor for a standard 100K receiver, it was corrected by means of the improved

biasing scheme discussed below.

C. Correction Circuit for Differential Operation

The error affecting the DC output levels due to the tolerance of the integrated poly-silicon resistors R_{TR} might be avoided by means of an external reference resistor or corrected by resorting to a trimming procedure, at the cost of an extra pin or higher production costs. On the contrary, in the proposed transmitter, the residual error was suppressed by means of an additional correction circuit, Fig. 5 dashed lines, which is enabled in case of differential operation, i.e. when both outputs are terminated with an external 50 Ω resistor. With reference to the replica circuit of Fig. 8, a shift of R_{TR} from the nominal value causes a variation of the output current which is sustained by the output p-MOS devices, *M4A* and *M4B*. The relative error on the output current is equal for the two output ports, therefore the output device providing the PECL high level (*M4A*) experiences a larger shift of its bias point, since the two devices are biased with approximately the same current. Due to the not negligible output resistance of the p-MOS output buffer, this causes a larger error of the high output level provided by the transmitter, Fig. 5. This error can be corrected if the output common mode voltage in the transmitter of Fig. 5 is sensed by means of the large valued resistors $RC1$ and $RC2$ and compared by $OP3$ to an internally developed reference voltage V_{CM-REF}. Since the high output level exhibits the higher sensitivity to the tolerance of R_{TR} resistors, the results of this comparison is used to control the voltage at the head of the differential pair by means of $M5_D$. At the same time the variable resistor $M5$, driven by the reference circuit in Fig. 8, is disabled. Thanks to this closed loop control the proposed PECL driver exhibits correct 100K levels if full PVT variations (corner analysis) and random mismatch are taken into account in the Monte Carlo simulations, Fig. 9-c. The only few cases when the returned DC output levels are outside form the 100K bounds occur at a junction temperature of -40 $°C$. Note that manufacturers usually increase the tolerance of the output levels at low temperature [8], [7].

III. Receiver

A PECL receiver may be designed as a differential amplifier driving a cascade of inverters in order to achieve valid CMOS levels [4], [5]. However, the CMOS inverter interfaced to the input amplifier must be exactly biased at its threshold voltage to be effective as voltage amplifier, unless a large voltage swing is available at the output of the differential amplifier by means of a large voltage gain. Since the receiver has to operate in the Gb/s range, a large bandwidth is required and a low voltage gain is mandatory. At the same time an accurate setting of the DC bias point is difficult since minimum channel devices are used for maximum speed, leading to a significant sensitivity to process variations. Another limit of PECL receivers based on a voltage amplifier is the dependence of the duty cycle of the CMOS output signal on the difference between the falling and rising transition times at the output of the amplifier. A significant shift of the duty cycle from the nominal value may be unacceptable for the logic circuits in the case of digital signals in the hundred MHz to GHz range. A tighter control of the duty cycle can be achieved by resorting to the n-MOS variant of the typical LVDS receiver [12], which can be viewed as a transconductance amplifier, Fig. 10. Indeed, with an appropriate setting of the current gain of the involved current mirrors, equal pull-up and pull-down currents are obtained at the output. However, the higher delay of the pull-down control, achieved by two cascaded current mirrors, severely limits the maximum toggle frequency.

The speed limitation of the LVDS receiver is overcome in the proposed complementary-differential PECL receiver, Fig. 11, where two transconductance amplifiers operate in parallel. The n-MOS input amplifier, $M1_U$-$M6_U$, drives the p-MOS device, $M7$, of the output inverter, thus controlling the pull-up current available at the output. On the contrary, p-MOS amplifier $M1_D$-$M6_D$ controls the n-MOS device, $M8$, in the output inverter. Using the same value of bias current for both amplifiers and a 1:1 ratio for current mirrors $M4_U$-$M7$ and $M4_D$-$M8$, equal falling and rising transition times are achieved at the output of the first inverter in the case of a differential input. Some amount of positive feedback was introduced in the amplifiers ($M5_U$-$M6_U$ and $M5_D$-$M6_D$) in order to obtain an hysteresis in the

50-100 mV range. With respect to the receiver of Fig. 10, the proposed circuit achieves a higher toggle frequency since only one current mirror is involved at both the rising and falling transitions.
Post-layout simulations with package parasitics show a maximum toggle frequency of about 1 GHz with a negligible error introduced in the duty cycle of the CMOS output signal. With single-ended input the receiver may be used up to 600 MHz with a duty-cycle error always lower than 10%; in this case a constant voltage of (V_{DD}-1.3) V is internally provided to the negative input pin.

IV. Measurement Results

The PECL transmitter and receiver presented in this paper were implemented as pad-cells in a 0.35 μm CMOS technology [13], with custom ESD protections for 2 kV HBM. The proposed cells were integrated in a couple of test chips, Fig. 12, which allow different measurement modes. A first set of measurements were performed on a transmission link obtained by connecting the two chips with a 4-inch, 50 Ω microstrips over a 4-layers FR4 PCB. The test board is controlled by a PC card which provides a 8-bit word to the transmitter chip. This word is loaded in an internal shift-register and serially transmitted with a rate depending on the frequency of a VCO integrated in the same chip. Beside the data burst (SD), a clock signal (CK) is transmitted to the receiver chip. The frequency of this clock is half the frequency of the internal VCO. Furthermore, the clock reference (CK) exhibits a shift with respect to the data signal exactly equal to a quarter of its period, Fig. 13. Therefore the sampling at the receiver can be performed at both clock transitions, thus relaxing by a factor of two the frequency of the transmitted clock reference. The sampled data are provided by the receiver (deserializer) to the PC card. A program running on the PC compares at each transmission the received word with the original one. BER measurements at different transmission speeds can be performed by changing the VCO frequency. The functionality of the transmission link was verified up to 1.2 Gb/s.
In order to completely characterize the two pad cells, a receiver and a transmitter connected in series were integrated in a test chip. An input sine-wave is provided to the PECL receiver through a power

splitter and a DC block, which allows to set the correct common mode voltage at the receiver inputs. Each output of the transmitter was loaded by a 10 pF capacitor and DC connected to a 50 Ω input of a sampling oscilloscope with 20 GHz bandwidth. In order to meet the DC loading conditions for PECL gates the oscilloscope ground was connected to the $V_{DD} - V_T$ plane of the test board by means of the cable's shield. Measurements prove that 100K levels are provided up to a toggle frequency of 1 GHz (2 Gb/s). With a 10pF load the PECL transmitter exhibits transition times below 400 ps, Fig 14. The receiver accepts a differential input signal with a minimum swing of 150 mV.

Fig. 15 shows the measured DC output levels, well within the 100K bounds, of the developed PECL transmitter at different temperatures and supply voltages and with the closed loop correction enabled. A performance summary of the presented PECL transmitter and receiver cells is reported in Tab. I.

V. Conclusion

A PECL I/O interface implemented in a 0.35 μm CMOS technology and fully compatible with the 100K family was presented. The proposed transmitter is based on a voltage switching architecture combined with additional current switching and can be interfaced in DC mode to other PECL systems. A high toggle frequency was achieved by avoiding the typical closed loop control used in previous CMOS designs in order to set the output voltage within the required tolerance. Indeed, a tight control of the output levels was obtained by means of a biasing scheme based on a replica circuit. In addition, a feedback control not affecting the operation speed was implemented in the transmitter cell in order to fulfill the 100K requirements on the output level accuracy over the full range of PVT variations without resorting to expensive solutions involving external components or trimming procedures.

The receiver is based on a complementary-differential architecture providing high speed and low sensitivity of the duty-cycle of the CMOS output signal to PVT variations.

The integrated receiver-transmitter chain features a maximum toggle frequency of 1 GHz in differential mode. Moreover, a chip-to-chip link, 4-inch long 50 Ω microstrips over a FR4 substrate, was tested up

to 1.2 Gb/s.

VI. Acknowledgments

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TABLE I
PERFORMANCE SUMMARY OF THE PECL TRANSMITTER AND RECEIVER.

PECL Driver	
Output Levels	100K
Transmisson Speed	1.2 Gb/s
Capacitive load	10 pF
Falling/Rising edge	$\leq$400 ps
Current Consumption	35 mA
Cell Size	725 x 340 μm^2
PECL Receiver	
Input levels	100K
Input swing (diff. input)	$\geq$150 mV
Toggle Frequency (single-ended)	0.6 GHz
Current Consumption	7 mA
Cell Size	300 x 340 μm^2
Process	CMOS 0.35μm (3M, 2P)
Supply Voltage	3 V$\div$3.6 V
Operating temperature	-40°$C\div$85°C

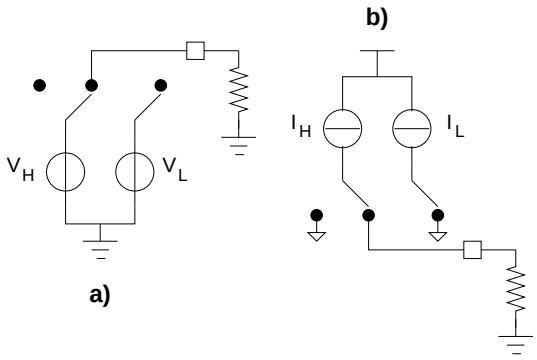

Fig. 1. Implementation of a line driver as a switched voltage (a) or switched current (b) source.

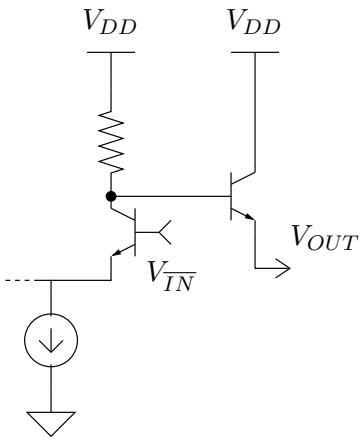

Fig. 2. Simplified schematic diagram of a bipolar ECL driver.

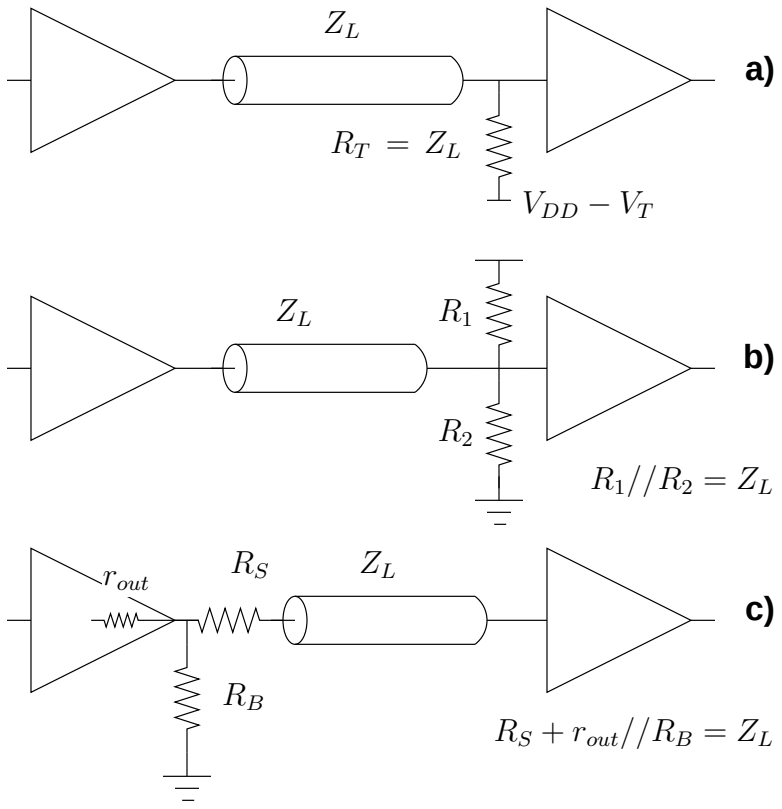

Fig. 3. Termination schemes for single-ended ECL drivers: a) canonical (parallel) termination to $V_{DD} - V_T$, b) Thevenin termination, c) series termination at the source end.

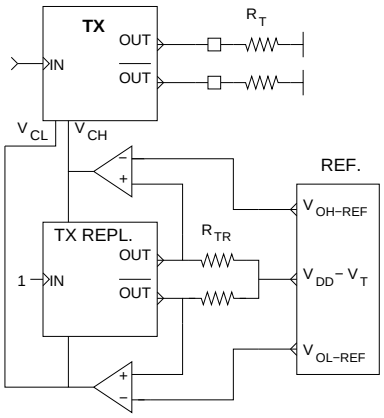

Fig. 4. Block diagram of the PECL transmitter with the DC biasing block based on a scaled replica.

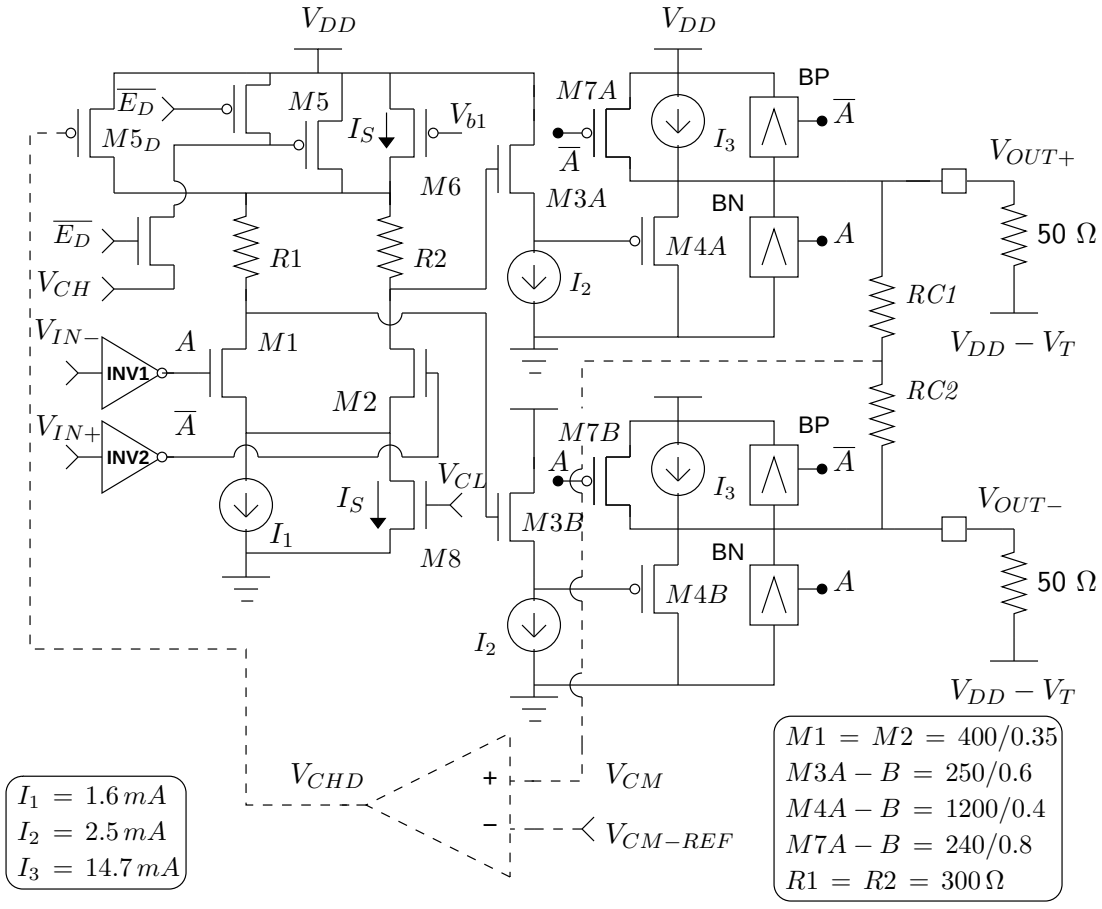

Fig. 5. Circuit diagram of the proposed PECL 100K driver.

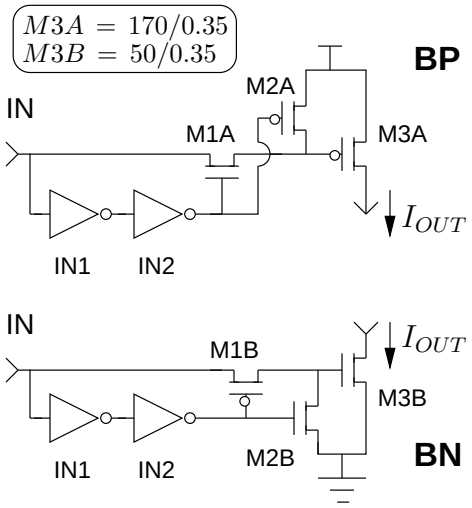

Fig. 6. Schematic diagram of the pulsers *BP* and *BN* in Fig. 5.

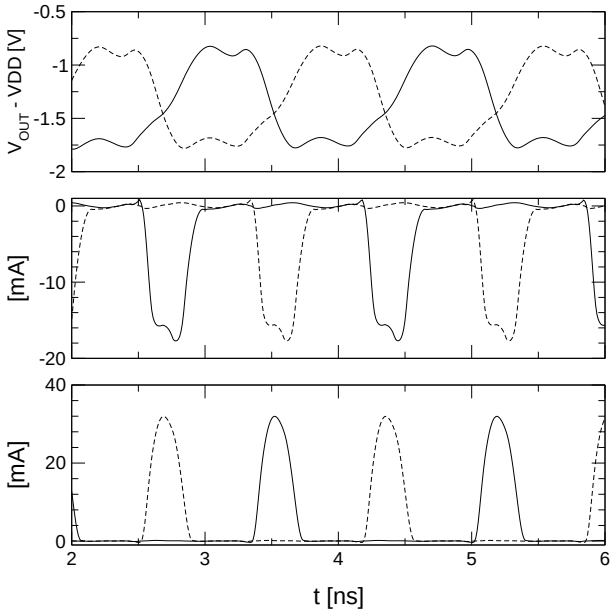

Fig. 7. Simulated voltage and current waveform of the proposed PECL transmitter. From top to bottom: voltage signal referred to the supply at the positive (solid) and negative (dashed) output; current drawn by *BP* at the positive (solid) and negative (dashed) output and current drawn by *BN* at the positive (solid) and negative (dashed) output, Fig. 5. Each output is loaded by 10 pF to ground.

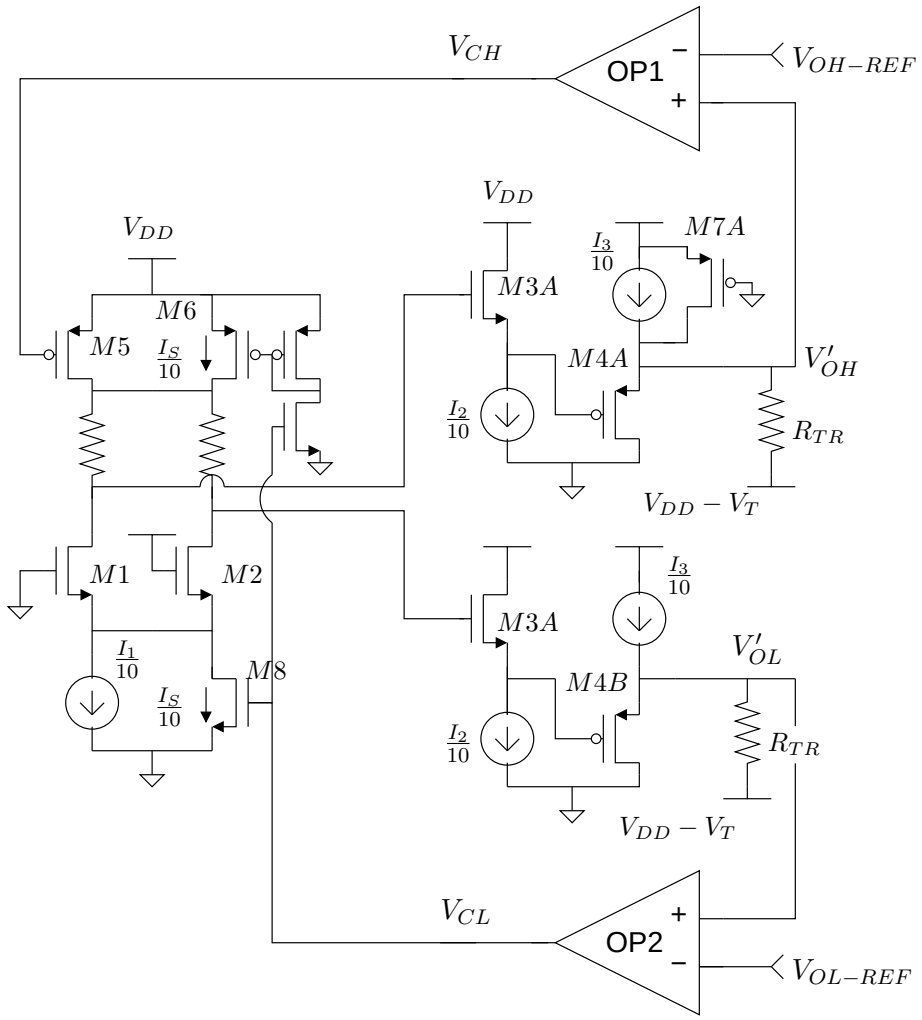

Fig. 8. DC biasing circuit for the proposed PECL transmitter.

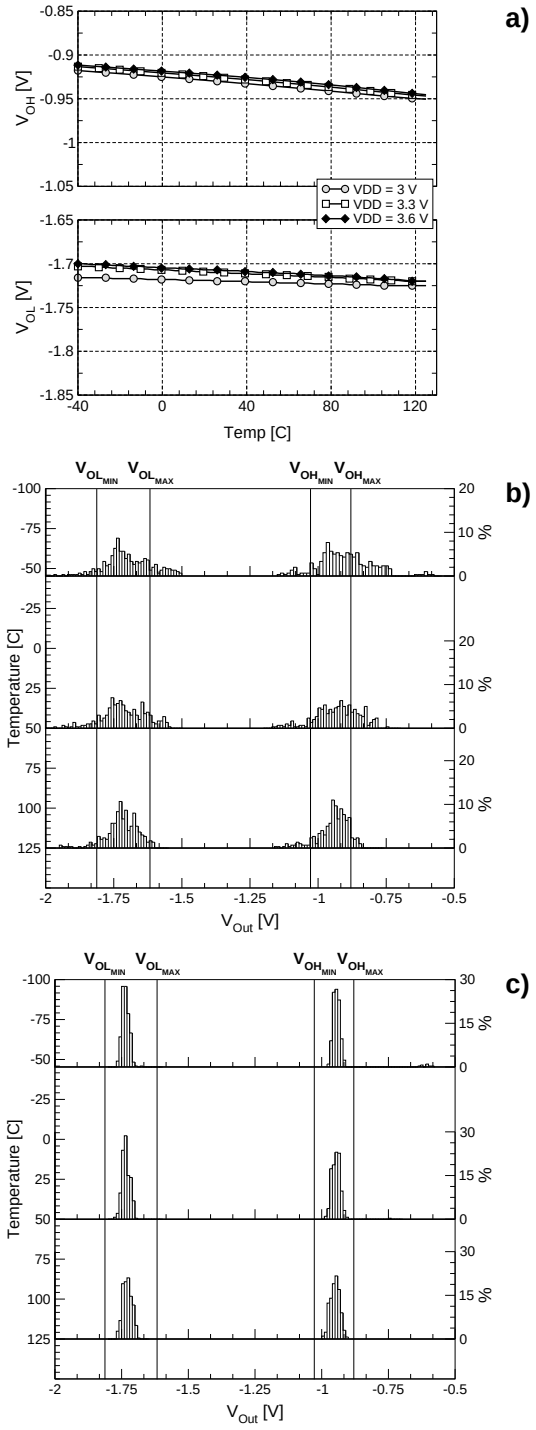

Fig. 9. From top to bottom: simulated DC output levels (referred to the supply) of the proposed PECL transmitter with the closed loop correction disabled (a). Results of Monte Carlo simulation covering PVT variations (corner analysis) and random mismatch with the closed loop correction disabled (b) and enabled (c). For graphs (b) and (c) the rate of occurrence is reported in the y-axis at the right, while the junction temperature used in the simulation is in the left y-axis in correspondence of the horizontal axis of each couple of histograms.

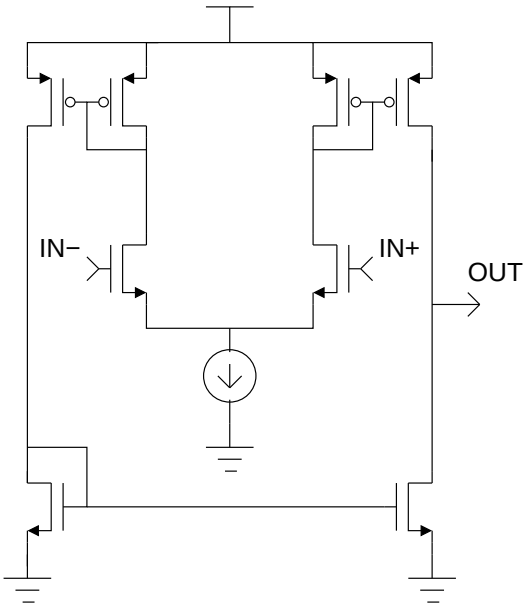

Fig. 10. Simple PECL receiver.

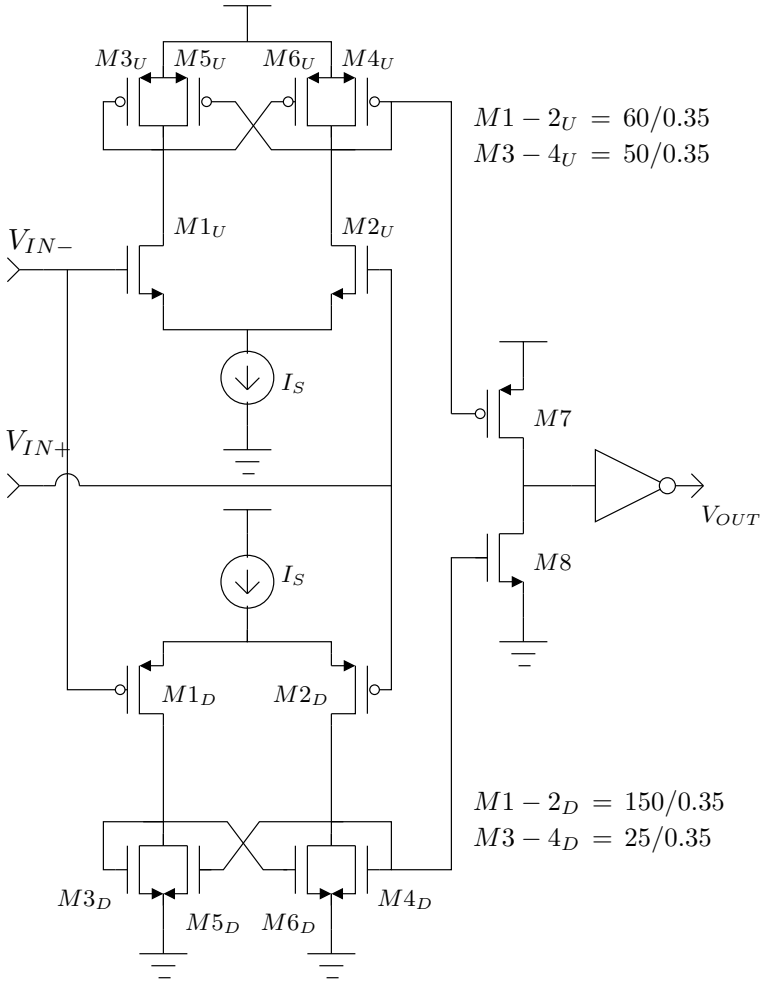

Fig. 11. Proposed PECL receiver with complementary-differential input stage for maximum operating speed.

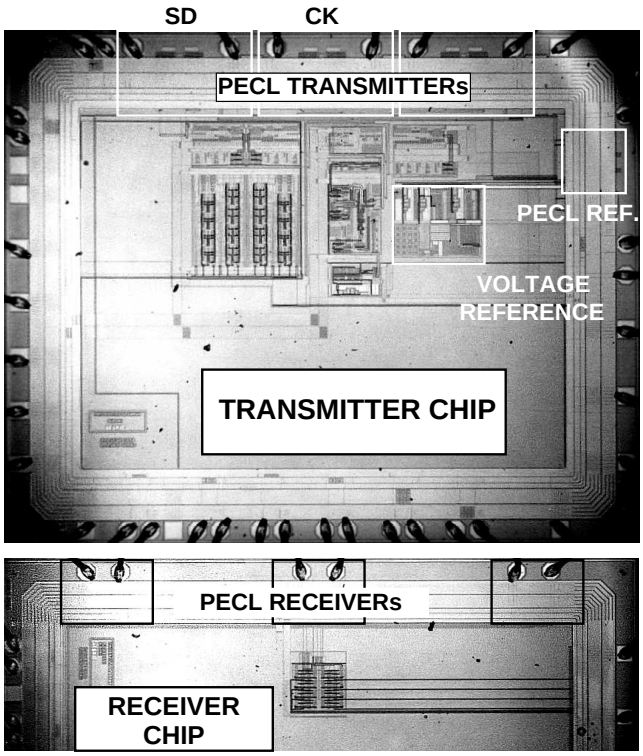

Fig. 12. Chip photograph of the transmitter (top) and the receiver (bottom) chip.

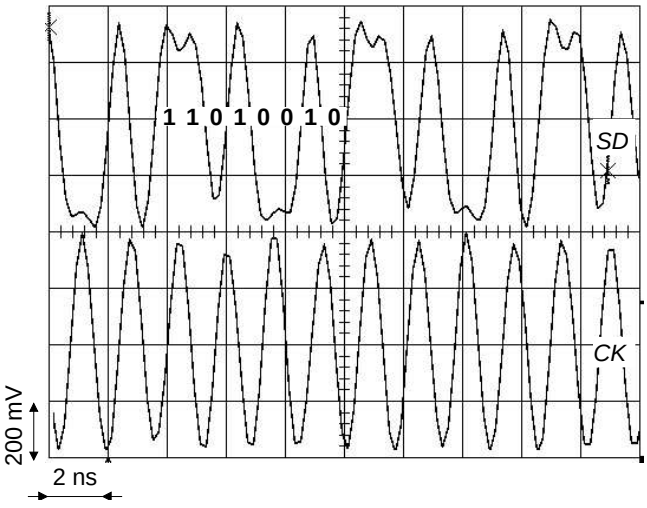

Fig. 13. Measured data (SD) and clock (CK) waveforms at the input of the receiver chip with a 11010010 pattern transmitted at 1.2 Gb/s. The bandwidth of the scope is limited to 1GHz.

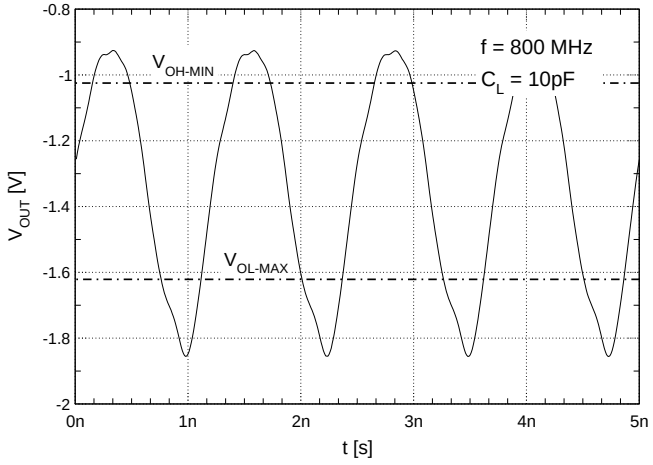

Fig. 14. Measured waveform at the output of the PECL transmitter running at 800MHz with a 10pF load.

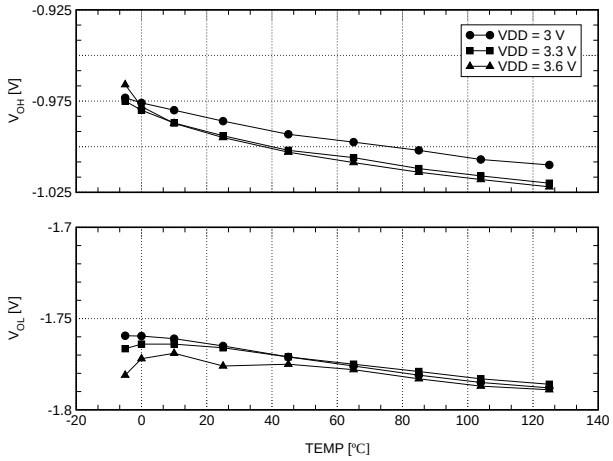

Fig. 15. Measured DC output levels of the proposed PECL transmitter (differential mode enabled) at different supply voltages and temperatures.

Figures' Captions

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Abstract

Title: **1.2 Gb/s true PECL 100K compatible**

I/O interface in 0.35 μm CMOS

Author: Andrea Boni, *Member, IEEE*

Abstract: This paper describes the design and the implementation of input-output (I/O) interface circuits for serial data links in the Gb/s range. The cells were implemented in a 3.3 V-0.35 μm CMOS technology in a couple of test chips. The transmitter is fully compatible (DC coupling) with 100K positive emitter-coupled logic (PECL) systems and it is based on the voltage switching principle in order to allow different termination schemes besides the canonical ECL termination, i.e. 50 Ω towards (Vdd-2) V. The addition of some circuit techniques such as dynamic biasing and strobed current switching boosts the dynamic performance of the the basic voltge-switching scheme and relaxes the requirements for a high bias current and large-size output devices at the same time. Moreover, thanks to the developed reference circuit, using both feed-forward and feed-back controls, the output levels are within the 100K tolerance over the full range of process, supply voltage and temperature (PVT) variations without resorting to external components or on-chip trimming. The receiver cell is based on a complementary-differential architecture providing high speed and low error on the duty cycle of the CMOS output signal. The integrated receiver-transmitter chain exhibits a maximum toggle frequency of 1 GHz, while a chip-to-chip transmission link using the developed I/O interface was tested up to 1.2 Gb/s.

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