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Robustness and Reliability Review of Si and SiC FET devices for More-Electric-Aircraft Applications

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Abstract

Increased electrification of traditionally hydraulic and pneumatic functions on aircrafts has put power electronics at the heart of modern aviation. Aircraft electrical power systems have traditionally operated at 115V AC and 28V DC with a constant speed generator and transformer rectifier units converting jet engine power into electrical power. However, due to the increasing trend towards the More Electric Aircraft (MEA), 270V DC systems are likely in the future. This calls into question, the power semiconductor device technology that enables the on-board power converters needed for electro-mechanical actuation as well as solid-state circuit breakers for system protection. Silicon IGBTs have been the work-horse of power electronics, but as switching speeds increase due to the need for high frequency operation, the bipolar nature of IGBT tail currents become a limiting factor for improved energy conversion efficiency. A number of unipolar FET technologies, including SiC trench MOSFETs, SiC planar MOSFETs, silicon super-junction MOSFETs and SiC JFETs in cascode with a low voltage Si MOSFET, have become commercialized at around 650 V. However, reliability and robustness, especially against single event burn-out and/or single event gate rupture is critical. This paper experimentally investigates the performance of the listed FET devices under Unclamped Inductive Switching and Bias Temperature Instability/gate oxide stress tests.

1. Introduction

The application of wide bandgap (WBG) devices in MEA applications is currently an active research and development topic in both academic and industrial circles [1, 2]. Silicon IGBTs have been the traditional device technology of choice for power conversion, however, improved switching performance of FET devices, particularly WBG devices has made them contenders in aerospace applications. Be that as it may, reliability and robustness are critical factors in technology adoption, especially in aerospace applications. Electrical reliability usually refers to gate oxide integrity over time as charges accumulate at oxide interface thereby resulting in increased gate leakage currents and shifting threshold voltage. Robustness in this context refers to the resilience of the power device against single event and/or anomalous conditions like cosmic-ray incidents, short-circuits and robustness under inductive over-voltages. The need for higher switching frequencies means improved switching performance is required for reducing switching losses. SiC power devices are generally known to have better switching performance for both the transistor and the body diode compared to similarly rated silicon FET devices. Fig. 1 shows the body diode switching transients for a silicon super junction (SJ) MOSFET, and a SiC MOSFET. The SiC device has nearly zero stored charge and the SJ device shows considerable stored charge in the body diode [3].

In this paper, a review of the latest generation FET technologies is performed with experimental measurements comparing performance under Unclamped Inductive Switching (UIS) and gate oxide robustness. 900V SiC planar MOSFETs, 650V SiC trench MOSFETs, 650V SiC JFET cascodes and the latest generation 650V silicon SJ MOSFETs have all been characterised. UIS performance is a good indicator for robustness of the device and it also reveals the true breakdown voltage of the device,

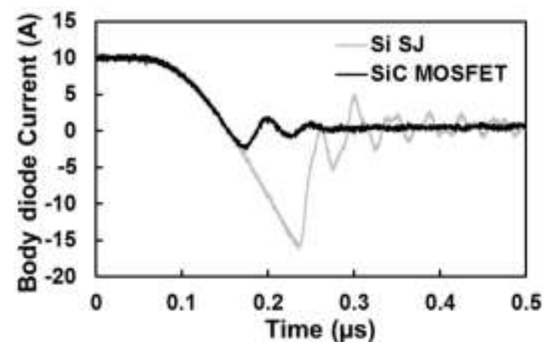

Fig. 1. Body diode switching characteristics

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which can be fundamental for operating voltage derating considering high altitude and cosmic rays. UIS measurements have been performed for all the technologies under high power avalanche (for testing parasitic BJT latch-up under high power density) and high energy avalanche (for testing the thermal impedance under large avalanche energy). Gate oxide stress and robustness tests have also been performed. Section 2 presents the UIS measurements, section 3 presents gate oxide stress tests, section 4 presents switching energy measurements while section 5 concludes the paper.

2. Unclamped Inductive Switching Measurements

The high-altitude operation of MEA applications makes single-event burn out from cosmic ray incidents more likely since the probability of contact with high energy particles increases with altitude above the sea-level [4]. If a device is blocking voltage while a high energy cosmic particle (tens to hundreds of MeVs) becomes absorbed in the voltage blocking drift region, the energy is deposited in the drift region and causes electron-hole pair generation [5]. Deposited charge plasma in the drift region can cause electric fields that exceed the critical field and subsequently result in avalanche breakdown of the power device. Due to the possibility of this occurrence, power devices are typically de-rated in voltage blocking capability so that additional headroom is used as a safety margin. The failure modes of power devices conducting current in the OFF-state (under avalanche conditions) are well understood. In power MOSFETs, the parasitic NPN BJT can latch while in IGBTs, it is a parasitic thyristor.

The ruggedness/robustness of the power device under avalanche mode conduction is evaluated by performing UIS tests [6]. These tests have been performed at low and high temperatures with 2 avalanche durations. Fig. 2 shows the avalanche test set-up together with the MOSFET equivalent circuit showing the parasitic BJT formed between the N source, P body and N drain.

Fig. 3 shows measured V_{GS}, V_{DS}, I_{DS}, avalanche power P and calculated junction temperature Tj waveforms obtained from the UIS test. As the Device Under Test (DUT) is triggered with a gate pulse, current ramps through the inductor at a rate (dI_{DS}/dt)

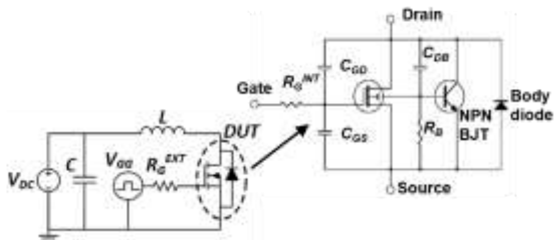

Fig 2. UIS test circuit and MOSFET parasitic elements

given by V_{DC}/L where V_{DC} is the supply voltage and L the value of the inductor in Fig. 1. During the inductor charging phase, the V_{DS} voltage is equal to the ON-state voltage of the device. As the device is turned OFF, using a gate voltage of 0 V in the experiments performed in this paper, the energy stored in the inductor E_{av}, given by Eq. 1, flows through the DUT as an avalanche current via impact ionisation. This causes high avalanche power dissipation through the device since V_{DS} goes to the breakdown voltage V_{BR} as shown in Fig. 3.

$$E_{av} = \frac{1}{2}\frac{LI^2}{1+\frac{V_{DC}}{V_{BR}}} \quad (1)$$

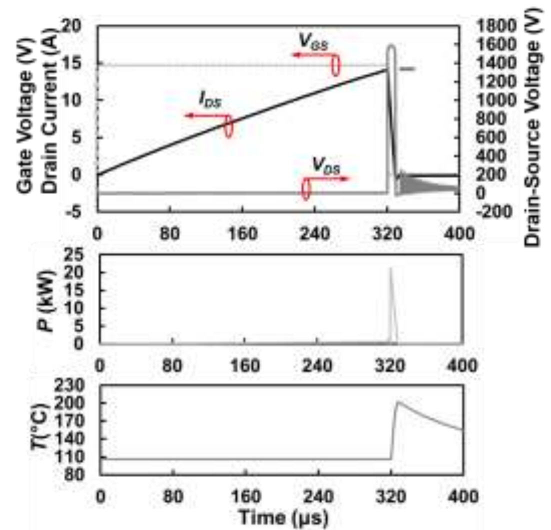

Fig. 3. V_{GS}, V_{DS}, I_{DS}, Power and junction temperature waveforms for device under UIS

By increasing the length of the V_{GS} pulse, the peak avalanche current is increased, hence, greater avalanche power is dissipated in the device. By doing this until the device breaks down, as shown in Fig. 4, the peak avalanche energy dissipated by the device is obtained. The junction temperature is calculated using the transient thermal impedance provided by the manufacturers.

Electrothermal failure under UIS occurs when the avalanche current rises during power dissipation as

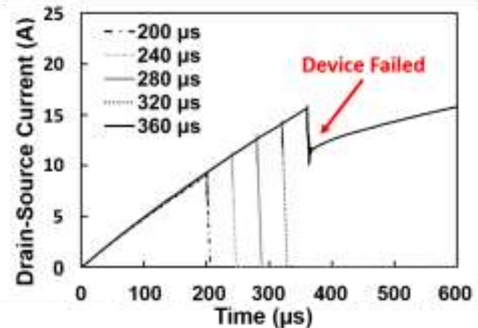

Fig. 4 Drain-Source currents for different V_{GS} pulse lengths until UIS failure

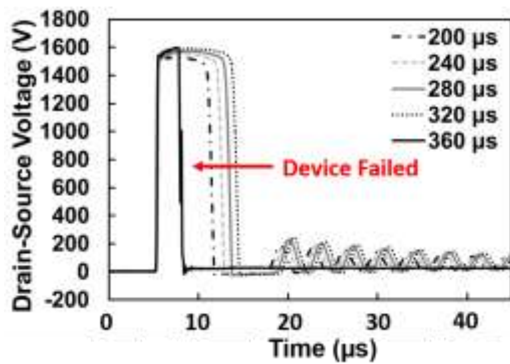

Fig. 5 Drain-source voltage during UIS until failure

shown in Fig. 4. The corresponding V_{DS} is plotted in Fig. 5, where it is observed that it falls to zero (short-circuit) as the current raises after failure.

2.1. High Avalanche Power Density

UIS tests have been performed on the SiC planar, SiC trench, SiC cascode and silicon SJ MOSFETs. Using a 1mH inductor, the avalanche current is controlled using the V_{GS} pulse as described earlier in Fig. 2 to Fig. 5. The maximum avalanche current (and energy) before electrothermal failure was determined for each technology. At least three devices of each technology were tested and the mean values are used for analysis.

Due to the different current ratings of the devices, the peak avalanche current I_{AV} before failure has been divided by the rated current I_{RATED} when comparing device ruggedness under UIS. Fig.6 shows this ratio for each technology for case temperatures 25°C and 105°C. At 25°C, the silicon SJ MOSFET outperforms all the SiC devices, followed by the SiC planar MOSFET, then the cascode and the SiC trench MOSFET. However, as shown in Fig. 7, at 105°C, the peak avalanche energy of the silicon SJ reduces approximately 1/3-(from 450 mJ to 150 mJ) whereas the peak avalanche energy of the SiC devices reduces marginally (less than 10%), except in the case of the high current SiC trench, which in the measurements was considerably affected by temperature.

As the chip sizes are different, with larger chips required for Si devices [3], it is important to analyse the avalanche energy density as a metric for comparing the avalanche performance of the material itself. This is shown in Fig. 8, where the measured avalanche energy E_{av} has been divided by the chip area to obtain the avalanche energy density. The chip areas were obtained with an optical microscope after decapsulating the chip.

The impact of the higher area of the Si chip is balanced and considering the avalanche energy density and the SiC cascode outperforms all the technologies, especially at high temperatures. It can be concluded that at elevated temperatures, the SiC MOSFETs are generally more avalanche rugged than the silicon SJ MOSFET. It is well known that the parasitic BJT is more easily latched at higher temperatures because of the positive temperature coefficient of the p-body resistance [7].

It is interesting to note the true breakdown voltage of the power devices which is evident during avalanche mode conduction as shown in Fig. 9.

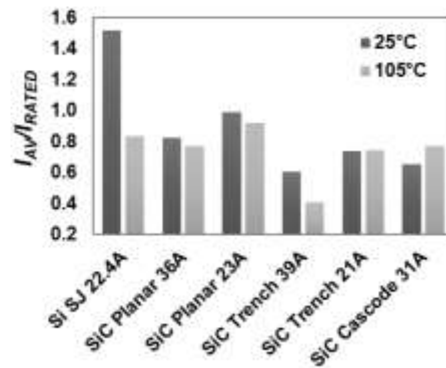

Fig. 6. I_{AV}/I_{RATED} ratio before failure (L=1 mH)

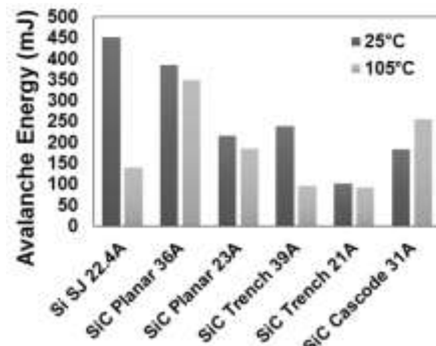

Fig. 7. Maximum avalanche energy (L=1 mH)

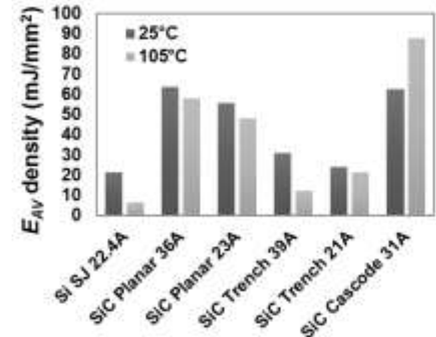

Fig. 8. Maximum avalanche energy density (L=1 mH)

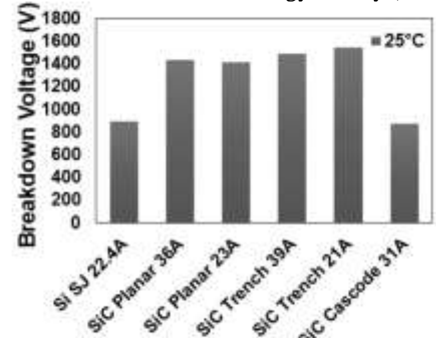

Fig. 9. Avalanche voltage during UIS (T=25 °C)

The 650V SiC trench MOSFET has an actual breakdown voltage that is higher than the 900V rated SiC planar MOSFET. The rated voltage of the trench MOSFET is 40% of the true breakdown voltage, whereas it is 65% in the 900 V planar MOSFET, 80% in the silicon SJ MOSFET and the SiC cascode. Hence, the SiC trench MOSFET has the largest headroom/safety margin as far as breakdown voltages are concerned. Although the 650V SiC trench MOSFETs record the lowest peak avalanche energy, it will have the largest safety margin for single event burn-out events since it has the highest breakdown voltage [8, 9]. Due to the SiC material properties, the volume where high field strength is 10 times smaller for the same device area whereas the electric field strength is 10 times larger [10]. Initial results, as stated in [10] were contradictory, with SiC Schottky diodes rated at 600 V showing a higher failure rate than Si PiN diodes and a better performance for 1200 V rated devices. Experimental results on cosmic ray failures results are recent, [8, 9] and more studies are expected, especially as the material quality of SiC is improving.

2.2. High Avalanche Energy

UIS measurements with large inductors (6mH) have also been performed. The difference between these and the previous measurements with 1mH inductor is that the avalanche duration is longer, hence the peak current is smaller. Since the avalanche duration is longer, the heat generated from the high avalanche power spreads more through the chip as opposed to high avalanche power (short duration UIS) where the chip fails by hot-spot generation. While short avalanche pulses with high current densities test the parasitic BJT design of the power device, longer avalanche pulses with low current densities, test the thermal impedance of the device. Fig. 10 shows the results of the peak avalanche current to rated current ratio while Fig. 11 shows the peak avalanche energy for each technology and Fig. 12 the avalanche energy density. Considering the absolute avalanche energy, the silicon SJ MOSFET demonstrates the best avalanche ruggedness followed by the planar, trench and cascode devices. Evaluating the energy density, the best performing device is the SiC planar MOSFET

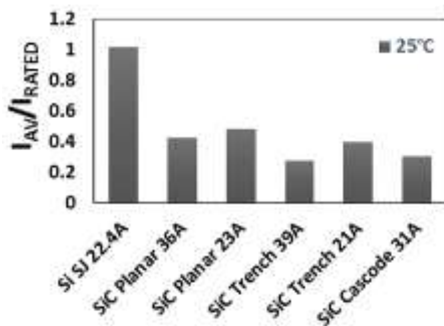

Fig 10. I_{AV}/I_{RATED} ratio before failure (L=6 mH)

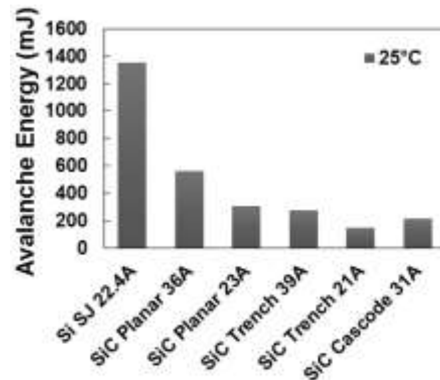

Fig.11. Maximum avalanche energy (L=6 mH)

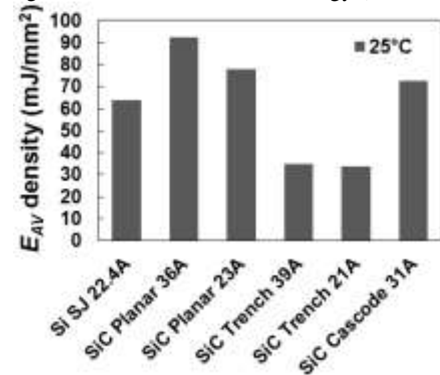

Fig.12. Avalanche energy density (L=6 mH)

followed by the SiC cascode. The material properties play a fundamental role in the case of the avalanche energy density, whereas in the case of the absolute energy the size of the SJ Si MOSFET chip plays a fundamental role as the thermal impedance of the chip is higher.

2.3. Peculiarities in Device Characteristics under UIS

Analysis of the waveforms for devices that failed under UIS showed certain peculiarities not previously observed for such measurements. Fig. 13 shows the V_{GS} waveforms (during failure under UIS) for the different technologies. As shown in Fig.13, the gate voltage for the trench devices increased during current runaway. The trench MOSFET was the only device with such a failure signature. The authors attribute this to an increased leakage current flowing through the gate terminal of the device. Fig. 14 shows the V_{DS}

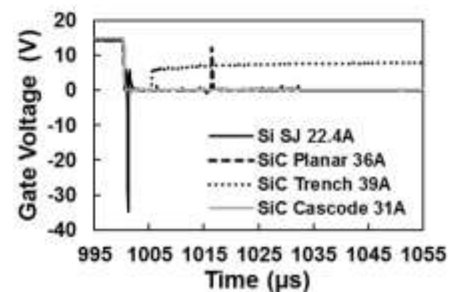

Fig. 13. Gate voltage waveforms for failed devices

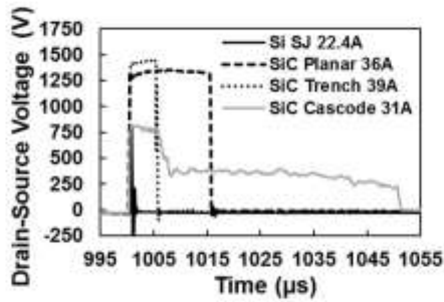

Fig.14. V_{DS} waveforms for failed devices

waveforms for all the technologies. Observing the V_{DS} waveforms during device failure under UIS also reveals some peculiar failure modes in the SiC cascode device. In the case of the SiC Cascode device, there are 2 distinct levels for V_{DS}, one at 750V at the start of avalanche and the other at about 300 V when the device goes into thermal runaway. This is likely due to the partial turn-ON (into linear mode) of the SiC JFET while the low-voltage silicon MOSFET is in avalanche. Since the JFET is not fully ON, the device is in linear mode, hence, there is a considerable voltage drop across the DUT until the device goes into thermal runaway.

3. Gate Oxide Robustness Tests

Gate oxide reliability is a critical component of power device reliability. The gate is ideally an insulator used to control current flow through the channel, however, increased gate conductivity occurs over the life of the device. Gate oxide reliability is particularly of concern in SiC MOSFETs due to the increased interface and fixed oxide trap density caused by the suboptimal oxidation of SiC during device fabrication [11]. In MEA applications, where the device is likely to operate at a higher junction temperature, higher switching frequency and with increased possibility of single event gate rupture from cosmic incidents, the performance of SiC gate oxides is particularly important. In this paper, the reliability/robustness of the gate oxide in the aforementioned 650 V power devices has been investigated, except for the SiC cascode. In this case, the presence of diodes for protection makes the study not comparable.

Firstly, a simple gate current I_G vs gate voltage V_{GS} sweep has been done on the SiC planar, SiC trench and silicon SJ MOSFETs. This test gives a quick indication of the performance of the gate oxide at high electric fields where various tunnelling mechanisms facilitate carrier flow through the gate oxide. These measurements were performed at 25°C and 150°C. Fig. 15(a) shows the result of the V_{GS} sweep at 25 °C where it can be seen that the SiC planar MOSFET breaks down below 25 V, the SiC trench MOSFET at around 27 V and the silicon SJ retains its insulating properties at 40 V. The results are not surprising and hence highlight one of the intrinsic problems with SiC. The measurements at 150°C, shown in Fig. 15(b), present a similar trend except that the gate oxides breakdown at lower V_{GS} for both SiC MOSFETs and silicon SJ MOSFET retains its insulating properties. The increase of the leakage currents with temperature in the SiC MOSFET is due to increased field emission across semiconductor/ insulator band-offset [12].

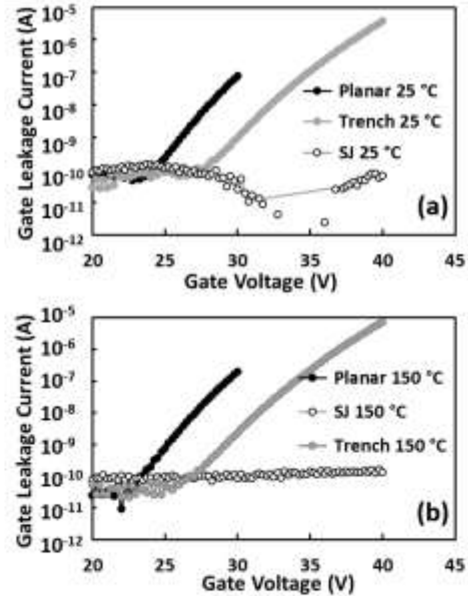

Figure 15. I_G vs V_{GS} characteristics (a) 25°C (b) 150 °C

Fig. 16 shows the measured leakage currents for the 3 devices at 150°C during 150 s, using a gate voltage bias of 30 V for the SiC devices and 40 V for the Si SJ. The trends show that the gate oxide of the SiC trench MOSFET exhibits lower leakage currents compared to the SiC planar MOSFET and the silicon SJ MOSFET is the best performing from the perspective of the gate oxide.

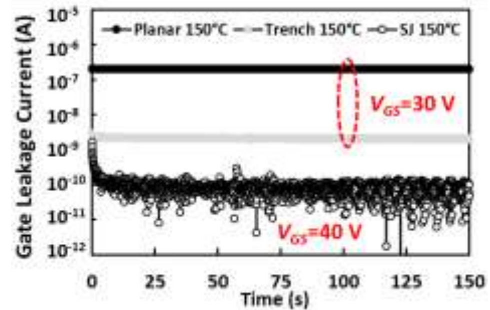

Fig. 16. Gate leakage current vs time at 150°C

Gate oxide leakage currents are a good indicator of the gate oxide reliability regarding Bias Temperature Instability (BTI). The presence of interface traps in the gate oxide not only contributes to the leakage currents but also exacerbates threshold voltage shift in a process known as BTI [13, 14].

Charge trapping due to the application of an electric field across the oxide from a V_{GS} stress causes a change in the threshold voltage. In the case of a positive stress, due to negative charge trapping, there is an upward drift of V_{TH}, which is referred as Positive Bias Temperature Instability (PBTI). Similarly, due to positive charge trapping, there is a downward movement of V_{TH} caused by negative V_{GS} stress. This is referred as Negative Bias Temperature Instability (NBTI). By applying a V_{GS} stress on the device at a defined temperature and duration and measuring the V_{TH} after stress removal it is possible to evaluate the extent of BTI in the devices.

To this end highly accelerated stress tests were performed in [15, 16] for both SiC trench and planar MOSFETs Cumulative gate voltage stresses with a duration of 30 minutes were applied to the devices at a temperature of 150 °C, followed by a recovery period of 16 hours before characterisation at ambient temperature. During the recovery phase the gate-source terminals of the MOSFETs were shorted (V_{GS}=0), to characterise only a more permanent V_{TH} shift. The transfer characteristics for PBTI stresses are shown in Fig. 17 for both devices while the transfer characteristics for NBTI stresses are shown in Fig. 18.

In the case of PBTI, the stress voltages required for cause a permanent V_{TH} shift in the evaluated conditions were in the range of +35 V (two stages) to +40 V for the SiC trench MOSFET while for the SiC planar MOSFET the gate voltage stress was in the range of +25 V to +30 V. In the case of NBTI, the stress voltage range was of -35 V (two stages) to -40 V for the SiC trench MOSFET and of -25 V (two stages) to -30 V for the SiC planar MOSFET. These shifts were not evident in the silicon devices at similar stress voltages. Hence, as far gate oxide reliability and

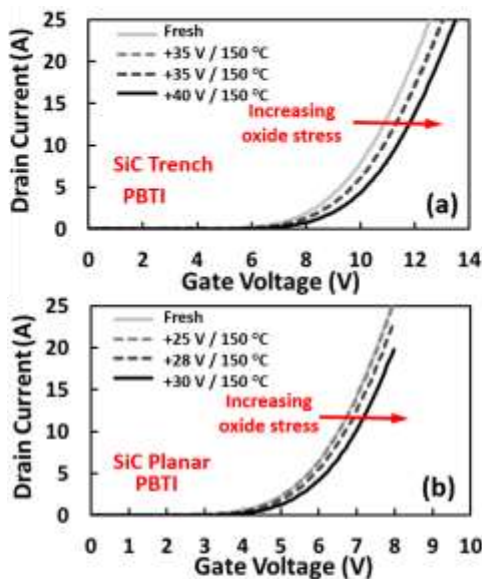

Fig. 17. I_{DS} vs V_{GS} for PBTI evaluation. (a) SiC Trench MOSFET, (b) SiC Planar MOSFET

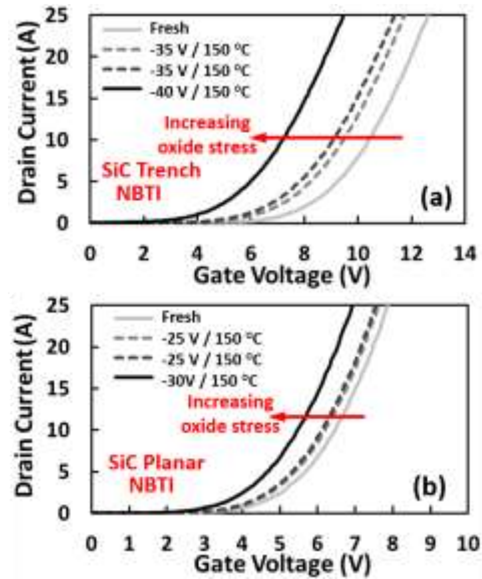

Fig. 18. I_{DS} vs V_{GS} for NBTI evaluation. (a) SiC Trench MOSFET, (b) SiC Planar MOSFET

robustness is concerned, SiC power devices, despite the improvements of the new generation devices, still lag behind silicon [17]. In this study, the SiC trench MOSFET performs better than the planar MOSFET. The change of threshold voltage due to BTI will have an impact on the on-state losses due to increased on-state resistance in the case of PBTI [14]. It the case of NBTI, the reduction of V_{TH} can aggravate the impact of cross-talk [18] and it can have catastrophic consequences for parallel connected devices in the case of uneven V_{TH} shift [7].

5. Conclusions

650V silicon SJ and SiC power devices are prime contenders to replace silicon IGBTs in MEA applications. Due to the high altitude of the MEA applications, robustness under single event burn out (from cosmic ray incidents) and single event gate rupture are important reliability and robustness metrics. UIS and gate oxide stress measurements have been performed on 650V SiC trench MOSFETs, 900 V planar MOSFETs, SiC JFET cascodes and silicon SJ MOSFETs. The results show that silicon SJ MOSFETs demonstrate the highest avalanche rug gedness performance at 25°C however, are outperformed by the SiC devices at 105°C. Although the SiC trench MOSFET shows the lowest performance under avalanche conditions, however, it has the highest safety margin in terms of breakdown voltage and is therefore well suited to MEA applications since it is less likely to go into avalanche. Certain peculiarities can be observed in the avalanche characteristics of the SiC cascode device where the peak avalanche energy uncharacteristically increases with temperature. Furthermore, the avalanche voltage falls significantly during UIS conduction and this tend increases with temperature. This is likely due to the

JFET turning ON during avalanche, however, more investigation is needed for this. Also, gate oxide breakdown is uniquely observed in the SiC trench MOSFETs during failure under UIS. This is not observed in the other devices. Despite the improvements of new generation SiC MOSFETs, under BTI and gate oxide stress tests, SiC MOSFETs are still behind silicon devices.

Acknowledgements
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