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Technology Independent Synthesis of CMOS Operational Amplifiers

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TECHNOLOGY INDEPENDENT SYNTHESIS OF CMOS OPERATIONAL AMPLIFIERS

by

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ABSTRACT

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Analog circuit design does not enjoy as much automation as its digital counterpart Analog sizing is inherently knowledge intensive and requires accurate modeling of the different parametric effects of the devices Besides, the set of constraints in a typical analog design problem is large, involving complex tradeoffs For these reasons, the task of modeling an analog design problem in a form viable for automation is much more tedious than the digital design Consequently, analog blocks are still handcrafted intuitively and often become a bottleneck in the integrated circuit design, thereby increasing the time to market

In this work, we address the problem of automatically solving an analog circuit design problem Specifically, we propose methods to automate the transistor-level sizing of OpAmps Given the specifications and the netlist of the OpAmp, our methodology produces a design that has the accuracy of the BSIM models used for simulation and the advantage of a quick design time The approach is based on generating an initial first-order design and then refining it In principle, the refining approach is a simulated-annealing scheme that uses (i) localized simulations and (ii) convex optimization scheme (COS) The optimal set of input variables for localized simulations has been selected by using techniques from Design of Experiments (DOE) To formulate the design problem as a COS problem, we have used monomial circuit models that are fitted from simulation data These models accurately predict the performance of the circuit in

the proximity of the initial guess The models can also be used to gain valuable insight into the behavior of the circuit and understand the interrelations between the different performance constraints

A software framework that implements this methodology has been coded in SKILL language of Cadence The methodology can be applied to design different OpAmp topologies across different technologies In other words, the framework is both technology independent and topology independent

In addition, we develop a scheme to empirically model the small signal parameters like 'gm' and 'gds' of CMOS transistors The monomial device models are reusable for a given technology and can be used to formulate the OpAmp design problem as a COS problem

The efficacy of the framework has been demonstrated by automatically designing different OpAmp topologies across different technologies We designed a two-stage OpAmp and a telescopic OpAmp in TSMC025 and AMI016 technologies Our results show significant (10 – 15%) improvement in the performance of both the OpAmps in both the technologies While the methodology has shown encouraging results in the sub-micrometer regime, the effectiveness of the tool has to be investigated in the deep-sub-micron technologies

This work is dedicated to

My paternal grandparents Sri Meduri Venkata Subbaraya Sitarama Anjaneyulu and Smt Meduri Suvarlachala Devi, my maternal grandparents Sri Pullela Subbaraidu and Smt Pullela Ramalakshmi and my parents Sri Meduri Venkata Rajagopal and Smt Meduri Mahalakshmi Their love and blessings are always with me and motivate me to be my best

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I am proud to have a wonderful brother-in-law Mr Shiva Sankar Pendyala, a caring sister Smt Vidya Sowmya Pendyala and a great brother Mr Naveen Koushik Meduri I am grateful for their love and support Vamsi Bharadwaj, my nephew, is always special to me

I am indebted to all my friends and relatives who gave me moral support and encouragement throughout my PhD years If it were not for them, who saw their happiness in my success, this work would not have been possible

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CHAPTER 1. INTRODUCTION

In this chapter, we provide a brief overview of the existing approaches to automating the transistor sizing of analog circuits The motivation for the dissertation work is outlined and the main contributions of the work are discussed

1.1. Analog Design Automation Background and Related Work

Design automation of analog circuits has a rich history, dating back more than two decades [1-5] Notwithstanding the considerable research effort in this field, analog circuit design does not enjoy as much automation as its digital counterpart Analog sizing is inherently knowledge intensive and requires accurate modeling of the different parametric effects of the devices Besides, the set of constraints and hence the degrees of freedom in a typical analog design problem are large, involving complex tradeoffs shown in Figure 1 1 [6]

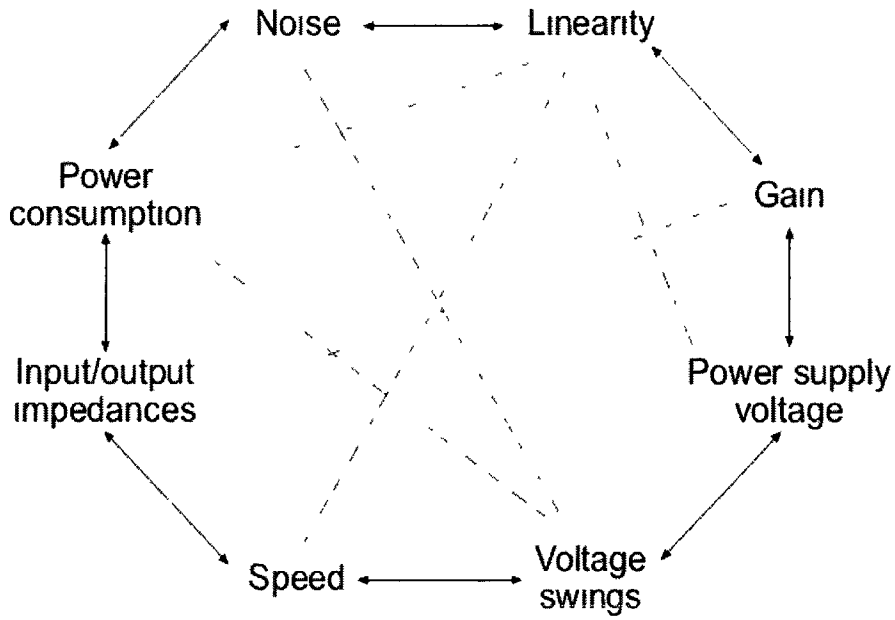


Figure 1 1 Trade-offs in analog amplifier design

For these reasons, the task of modeling an analog design problem in a form viable for automation is much more tedious than the digital design Consequently, analog blocks are still hand crafted intuitively [7] and often become a bottleneck in the System on Chip (SoC) design [8-13], thereby increasing the time to market

1.1.1. Analog Design

Analog design consists of topology selection, circuit sizing and layout, often at multiple hierarchy levels [1, 14] The typical design path for an analog design circuit is shown in Figure 1 2 [15] In this dissertation, we address the circuit sizing problem In other words, we propose methods to automate the transistor-level sizing of OpAmps However, the topology selection and layout phases are still critical steps in the design process

The topology selection step is crucial because proper selection of an appropriate topology determines whether or not the specifications for the block under consideration are met [16-21] This is more a heuristic and intuitive process, like other steps of the design process, requiring expertise of the designer, and is difficult to automate

The layout phase consists of physical realization of elementary circuit components and their interconnections [22-27] Repeated extraction and comparison with the schematic are very necessary to ensure that the parasitics in the layout do not disturb the circuit operation adversely

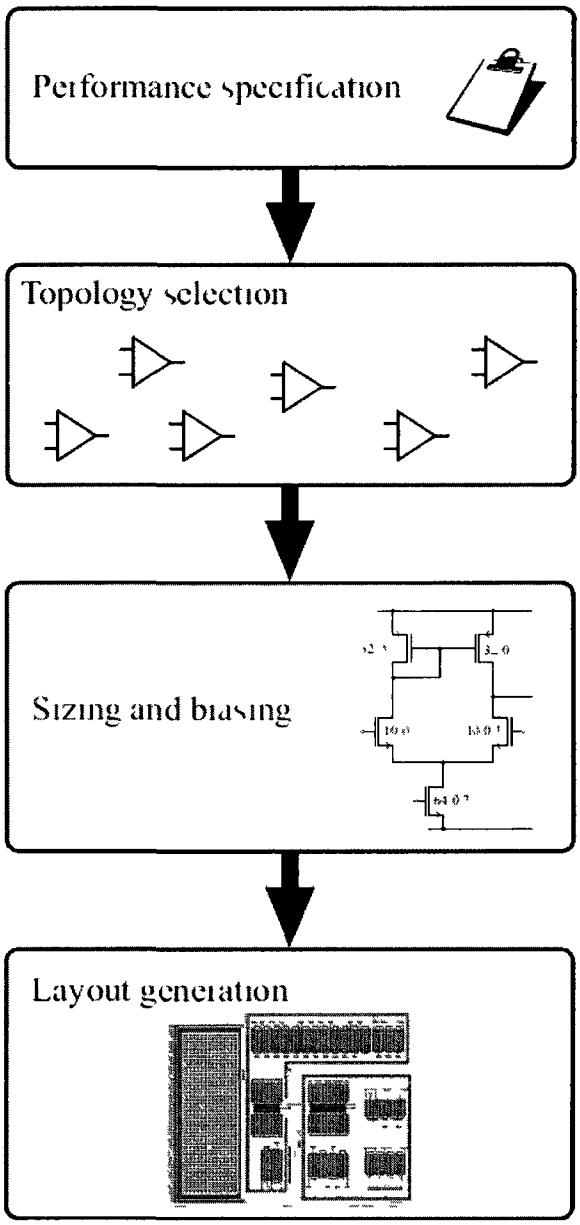


Figure 1 2 Typical analog design flow

During the circuit sizing stage, proper selection of the component values and bias voltages in the circuit is necessary to ensure the sub-blocks meet the specifications At the lowest level of hierarchy, these component values consist of transistor sizes, resistor and component values and bias voltages The general design flow of a typical analog block progresses by

translating the higher level specifications for a block in to those for sub-blocks This process is repeated until, finally, at the lowest level of hierarchy, the component values are determined to meet the specifications of that sub-block This methodology is called the top-down constrained-driven circuit design methodology [28-36]

1.1.2. Automation of the Analog Sizing Problem

A review of the existing approaches to solving the problem of analog circuit sizing is presented in [37] The current state of the art in analog design automation is presented in [38-41] The existing approaches to automatically solve analog sizing problems can be broadly classified into three categories Knowledge-based approaches, Equation-based approaches and Simulation-based approaches

- Knowledge-based approaches This first generation of automation methods, presented in the 1980s, relied on formally encoded expert designer knowledge to aid the sizing process A precompiled design plan is executed for each set of performance specifications to quickly yield a design solution, as shown in Figure 1 3 [15] IDAC [42], OASYS[43], [44], BLADES [45] and ISAID [46] are some of the early tools that implemented a Knowledge–based methodology in the analog synthesis problem This scheme resulted in quick execution time However, the overhead of obtaining and formalizing expert knowledge into computer executable format (library of sizing plans) for a wide range of topologies turned out time consuming and restrictive

- Simulation-based approaches A black box approach is employed and the circuit is simulated to model its behavior The resultant model is solved using optimization schemes to yield a final design This approach, shown in Figure 1 4 [15], results in designs with full SPICE-level accuracy DELIGHT SPICE [47], FRIDGE [48], and MAELSTROM [49] are the OpAmp

synthesis tools using the simulation based scheme In [50], a Genetic-Algorithm is used in conjunction with a simulation based scheme However, use of multiple numerical SPICE simulations proved to be time consuming

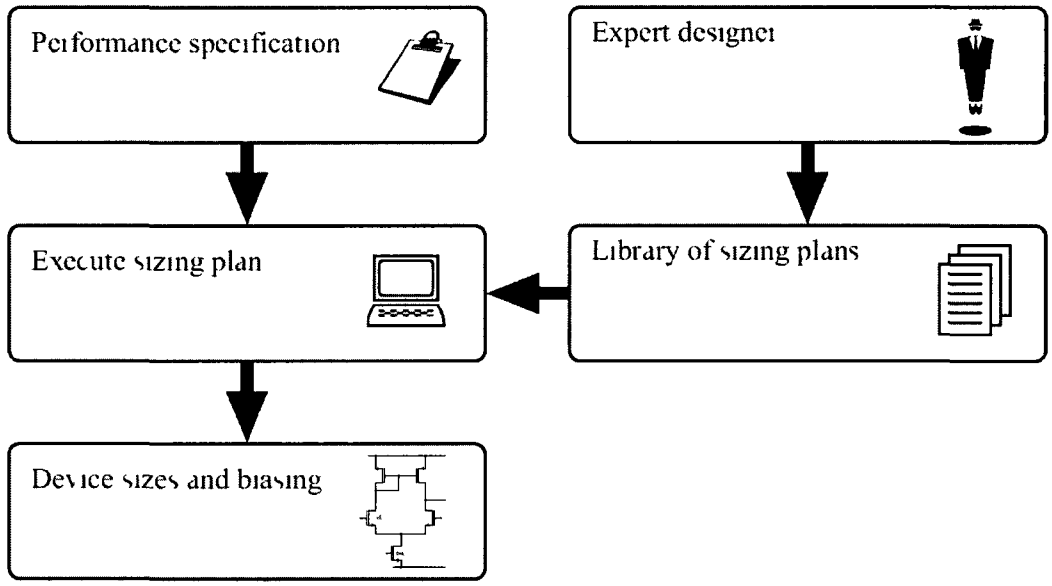


Figure 1 3 Knowledge-based device sizing

- Equation-based approaches The sizing problem, along with the circuit behavior and the different performance metrics is modeled as a set of equations that is compatible with an optimization algorithm, as shown in Figure 1 5 [15] The different degrees of freedom are automatically solved using the optimization algorithm to result in a design satisfying the performance requirements OPASYN [51], STAIC [52] and ASTRX/OBLX [53] use equation-based approach for analog synthesis The accuracy of the equations used to model the design problem, however, limits the accuracy of the final design

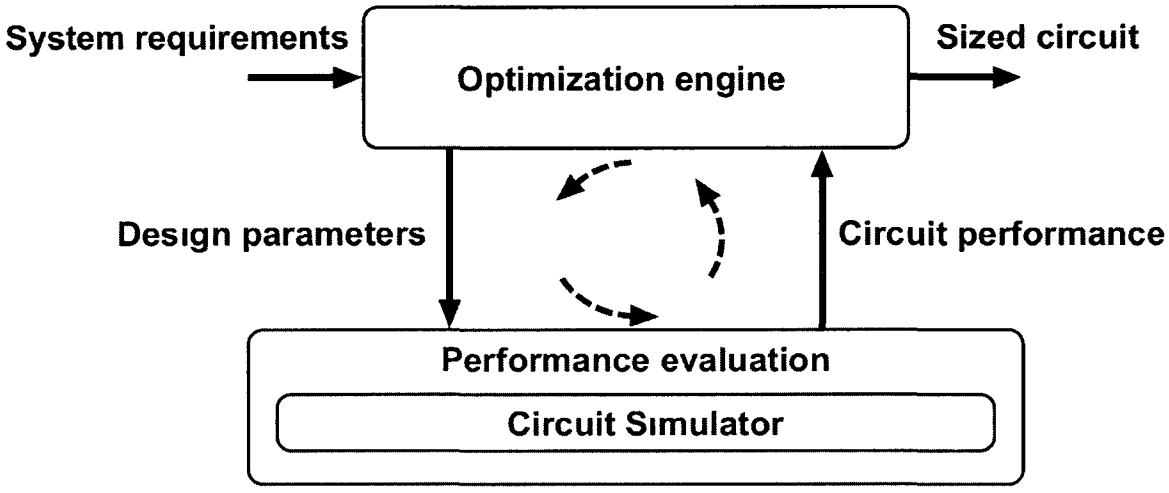


Figure 1 4 Simulation-based device sizing

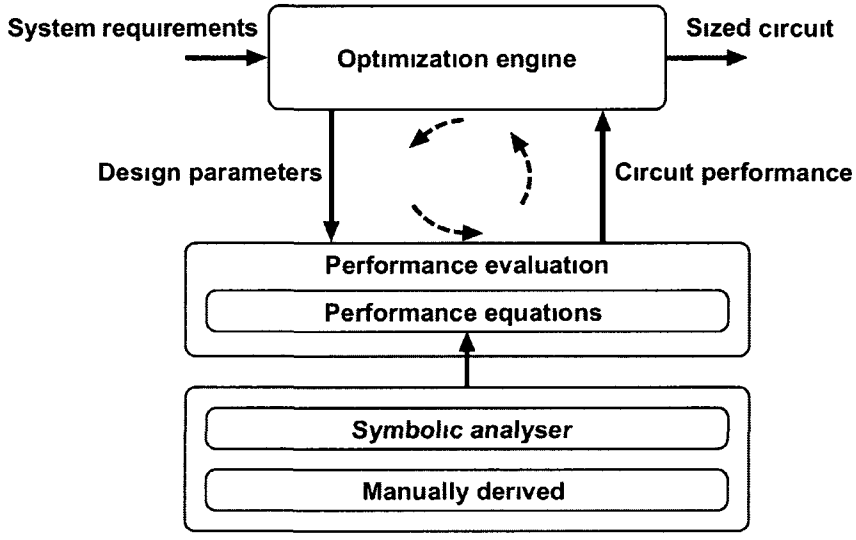


Figure 1 5 Equation-based device sizing

1.2. Motivation

One of the traditional drawbacks of the equation-based approach is the low accuracy due to the use of simplified models and approximations In modern process technologies, simple models do not accurately account for all effects that must be considered during the design On the other hand, the simulation based approaches, though accurate, suffer from lengthy execution times The use of time-costly extensive simulations proves exorbitantly expensive in terms of design time

To date there exists no OpAmp synthesis scheme that effectively solves these two issues simultaneously The trade off between design time and accuracy adversely affects the synthesis of Operational Amplifiers Walter Daems et al [54], proposed a simulation based posynomial model scheme that integrates the advantages of an optimization scheme while still preserving the accuracy of simulation schemes Their method is capable of generating posynomial equation models for both linear and non-linear circuit characteristics These posynomial models can be used to formulate a COS problem, that can be solved using Geometric Programming (GP), yielding a global optimal solution However, the main disadvantage of their approach is that the integration of the simulation based scheme into the algorithm increases the overall design time drastically Also, the overhead brought about by the posynomial generation engine itself undermines the advantage of an optimization scheme, namely, quick design time

The work proposed by Hagglund [55] addresses the issue of quick design time However, the optimization scheme they use results in several local minima, unlike the COS problem, which results in the global optimum design Moreover, the accuracy of the final design time is not

comparable to that achieved from a simulation scheme A robust design methodology is needed to address the issue of 'design time – accuracy trade off'

Secondly, to keep up with the Moore's law [56], the transistor feature sizes are halving every two years and fabrication industries are taping out in new process technology nodes every two years This brings the issue of reusability While digital circuits are easier to port to new technologies, analog circuits have to go through a steep learning curve to accurately model the I-V characteristics for each technology node All of the existing approaches in the literature [2 -14] have implemented either (i) an extensive learning algorithm to train for the technology in use or (ii) use exhaustive simulations to capture the technology specific parameters Both of these approaches, however, add to the overhead of the design scheme itself In other words, a technology independent synthesis methodology is desirable in the design automation of Operational Amplifiers This methodology should be capable of yielding reliable designs across several technology platforms, without bringing the overhead of extra 'learning' time

Thirdly, to accurately model the small-signal parameters for short channel devices, a simulation-based scheme is needed, which captures the higher order effects into reusable models Although efforts have been made ([57], [58] and [54]) to address this issue, the models generated by these approaches do not provide an accurate depiction of the small signal characteristics over the entire region of operation In other words, these models lack accuracy over the entire region of operation of the transistors and hence the final design obtained by using these models does not compare well with that obtained from simulations Moreover, the overhead of generation of these models, though required only once for each technology, is still a considerable effort Therefore a simple methodology to generate the small-signal models is needed, the accuracy of which does not adversely affect the final design solution

1.3. Contributions of This Work

In this work, we address the problems outlined in section 1 2 The main contributions of our work can be summed up as follows

(1) We develop a novel framework to automate the transistor-level sizing of OpAmps Given the specifications and the netlist of the OpAmp, our proposed methodology produces a design that has the accuracy of the BSIM models used for simulation and the advantage of a quick design time The approach is based on generating an initial first-order design and then refining it using localized simulations The simulation-based scheme provides the accuracy of higher order BSIM models, while localizing the simulations around the proximity of the initial guess drastically reduces the number of simulations required, thereby reducing the design time

(2) A software framework that implements this methodology has been coded in SKILL language of Cadence Our results have shown that the methodology can be applied to design different OpAmp topologies across different technologies In other words, the proposed framework is both technology independent and topology independent

(3) We developed a scheme to empirically model the small signal parameters like 'gm' and 'gds' of CMOS transistors The proposed monomial device models are reusable for a given technology and can be used to formulate the OpAmp design problem as a Convex Optimization problem

1.4. Outline

The rest of this work is organized in the following manner In Chapter 2, a brief review of the related concepts, namely, Geometric Programming and Design Of Experiments is provided In Chapter 3, the methodology for characterizing the small signal parameters as monomials is described Chapter 4 presents a detailed description of the novel methodology for CMOS OpAmp Sizing In Chapter 5, we discuss the results of a Two-stage OpAmp and a Telescopic OpAmp designed in different technologies Chapter 6 presents discussion and future work

CHAPTER 2. RELATED CONCEPTS

Geometric Programming and Design of Experiments form the core concepts on which our framework is built In this chapter, we provide a description of the Geometric Programming technique and the design of experiments approach

2.1. Geometric Programming

It has been demonstrated that a large variety of analog sizing problems can be formulated as a geometric program [59-61] In our approach, we use geometric programming to solve the convex optimization scheme (COS) problems formulated to model the OpAmp design problem Using geometric optimization in the design of an OpAmp automates the design process significantly This robust optimization scheme quickly converges to a solution set, giving a design that is globally optimal in the design space This method is based on formulating the design problem as a set of posynomial equations, which can be solved using convex optimization algorithms to converge to the solution that meets the different specifications, and the design space constraints The canonical representation of the GP is given below, along with the definition of the terms 'monomial', 'posynomial', etc and their properties

Let $x_1\ x_2 \quad x_n$ be n positive variables The vector $(x_1, x_2 \quad x_n)$ is denoted as x A function is called a posynomial function in x if it has the form

$$f(x_1, x_2, \quad , x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \quad x_n^{\alpha_{nk}} \qquad (2\ 1)$$

the coefficients c_k are positive numbers whereas α_{ij} can be any real numbers If t=1 then f is called a monomial

Posynomial functions are closed under addition, multiplication, and non-negative scaling Monomials are closed under multiplication and division

Geometric programming is an optimization problem of the form

$$\begin{aligned} &\text{minimize} && f_0(x) \\ &\text{subject to} && f_i(x) \le 1, \quad i = 1,2, \quad m, \\ &&& g_i(x) = 1, \quad i = 1,2, \quad p, \\ &&& x_i > 0, \quad\quad i = 1,2, \quad n, \end{aligned} \tag{2 2}$$

where f0 to fm are posynomial functions, g1 to gp are monomial functions It is quite clear that geometric programming handles posynomial inequalities and monomial equalities Several extensions are readily handled If f is a posynomial and g is a monomial then an inequality of the form f $\leq$ g can be handled as f(x)/g(x) $\leq$ 1 (f/g is a posynomial) Constraints of the form f(x) $\leq$ a, where f is a posynomial, can be handled as f(x)/a $\leq$ 1, where a $\geq$ 0 A monomial equality of the form g1(x) =g2(x) can be handled in geometric programming as g1(x)/ g2(x) =1 (since g1 / g2 is a monomial) [60]

Usually, functions whose reciprocals are posynomials are encountered If 1/h is a posynomial, then h is said to be an inverse posynomial Geometric programming can handle the constraints of the form f(x) $\leq$ h(x) as f(x)/h(x) $\leq$ 1 (since f/h is a posynomial) Another way inverse posynomials can be handled is maximizing h by minimizing 1/h [60]

A geometric program can be reformulated as a COS i e , the problem of minimizing a convex function subject to convex inequality constraints and linear equality constraints Formulation of a convex problem is explained in [59, 60] A comprehensive introduction to COS problem formulation, methods of effective numerical solutions and its applications to

engineering problems can be found in [62] Very efficient primal-dual interior-point methods used in linear programming have been extended to geometric programming which greatly reduce the computational time

2.2. Design of Experiments

Design of Experiments (DOE) is a systematic approach for investigating a system or process A series of structured tests or experiments are designed in which planned changes are made to the input variables of a process or system[63] The effects of these changes on a pre-defined output are then assessed DOE is important as a formal way of maximizing information gained while resources available for experiments are limited It has more to offer than 'one change at a time' experimental methods, because it allows a judgment on the significance to the output of input variables acting alone, as well input variables acting in combination with one another[63] Techniques from DOE provide a mathematical basis to select a limited but "optimal" set of sample points needed to fit a black-box model [64]

A good review of the application of Statistical Design of Experiments methods, Response Surface Modeling and their applications to Computer-Aided VLSI Design Methodologies is presented in [65]

Well-known and often-used sampling schemes range from full and fractional factorial design, over Placket-Burman[66] and Taguchi schemes [67], to Latin hypercube[68] and even random design The choice and the literature are vast [54, 64] A very interesting class of sampling schemes, however, are orthogonal arrays (a particular fractional factorial design), more specifically orthogonal arrays of strength three [54] This scheme places the sampling points on the boundary planes of a fitting hypercube of size around a center point The four-dimensional

level-two orthogonal array of strength three around zero shown in equation (2 3) illustrates this [54]

$$L_{Runs}^{Strength}(Levels^{Factors}) = L^{3}{}_{8}(2^{4}) = \begin{bmatrix} -dx & -dx & -dx & -dx \\ -dx & -dx & dx & dx \\ -dx & dx & -dx & dx \\ -dx & dx & dx & -dx \\ dx & -dx & -dx & dx \\ dx & -dx & dx & -dx \\ dx & dx & -dx & -dx \\ dx & dx & dx & dx \end{bmatrix} \quad (2\ 3)$$

The above equation (2 3) represents an orthogonal array The number of factors (design variables) affecting the system defined by this array is four, resulting in four columns in the array Each of the factors (design variables) can take one of the two levels 'dx' and '-dx' Here, the variation of these levels is around zero, but the factors may vary around a center point as well The number of columns represents the number of 'runs' or experiments to be performed and is eight in the above example The strength of the orthogonal array in the above example is three

In cases where the factors are not varied around zero, the center point is provided as well Orthogonal arrays of strength three allow the un-confounded estimation of linear, quadratic, and interaction terms of a second-order polynomial phenomenon [54] This is a very beneficial property when fitting local models of a more general system

CHAPTER 3. MODELING OF THE SMALL-SIGNAL PARAMETERS

To keep up with the Moore's Law, the process of manufacturing Integrated Circuits on silicon has undergone a steep learning curve There are several process technologies available today for realizing integrated circuits, including BiCMOS, CMOS, SOI, etc However, the most popular of these technologies, the CMOS (Complimentary Metal-Oxide Semiconductor) process has been a grand success commercially for several reasons

In the CMOS process, both the n-channel (NMOS) and the p-channel (PMOS) MOSFETs are used to realize a digital logic function The PMOS transistor is "ON" when a low voltage level is applied to the gate On the other hand, the NMOS is "ON" when the gate potential is high Using these devices to form complimentary circuits reduces the static power consumption drastically, because only one half of the circuit is "ON" for any given logic inputs Further more, the area required to implement logic functions in CMOS is small which translates into more functionality on a chip of given size The need to implement analog functions using the same process technology has motivated researchers to develop accurate models for the MOSFETS in CMOS Technology

In this chapter, we first describe a simple Level-One (Long-channel) model used for modeling the MOSFET behavior in section 3 1 In section 3 2, we describe a method to empirically model the small-signal parameters In section 3 3, the effectiveness of these new models is validated using a design example The results of the design example are also provided in section 3 3

3.1. Long Channel Model

In this section, a simple model for the CMOS transistor is discussed Even though this model does not predict the behavior of the deep sub-micron transistors accurately, the relations are still valuable to understand the relationship between different properties of the devices Also, some of the concepts presented here are used in more accurate models as well The equations presented here, called the long channel models, are normally used for performing hand calculations They are also an integral part of the manual device sizing approach

3.1.1. Large-Signal Model

The symbols of four terminal NMOS and PMOS transistors are shown in Fig 3 1 In this simple model the transistors are assumed to have three operating regions - cut-off, linear, and saturation The equations for the NMOS transistor are given, the corresponding relations and equations for the PMOS transistor are similar For the NMOS transistor the cut-off, linear, and saturated regions are defined by the following relations

cut-off $V_{GS} \leq V_{TH}$ (3 1)

linear $V_{DS} < V_{GS} - V_{TH}$ *and* $V_{GS} > V_{TH}$ (3 2)

saturation $V_{DS} \geq V_{GS} - V_{TH}$ *and* $V_{GS} > V_{TH}$ (3 3)

Here V_{TH}, the threshold voltage, is the minimum gate to channel voltage required in order to create a conducting channel between the drain and source in the transistor The threshold voltage is modeled by

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) \quad (3\ 4)$$

where V_{TH0} is the threshold voltage when V_{BS} is zero The additional terms model the body-effect The body-effect is an increase in the threshold voltage due to the voltage difference between the substrate (bulk) and the source of the transistor In (3 4), φ_F is the difference between the Fermi potential at the gate and the Fermi potential at the substrate γ is the body-constant determined by the process parameters

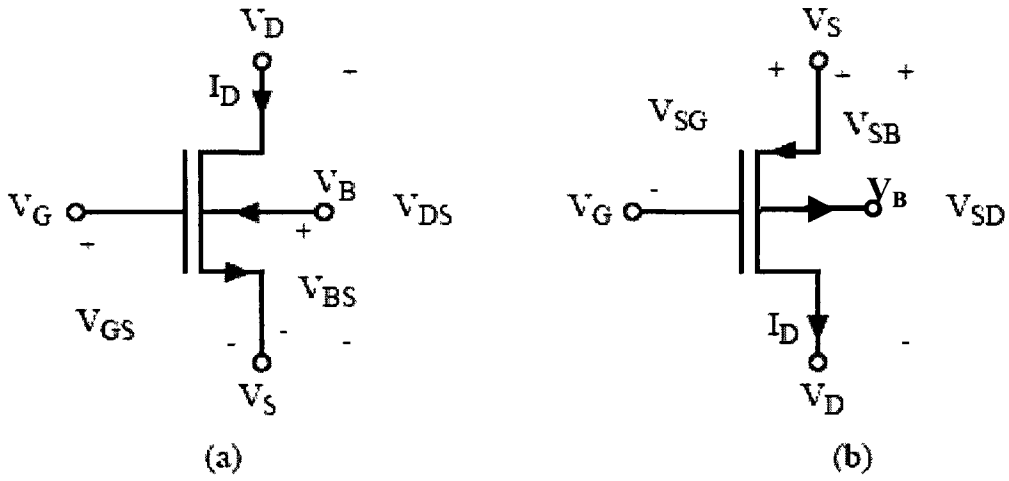


Figure 3 1 Voltage and current definitions for (a) NMOS and (b) PMOS transistors

Depending on the operating region the current through the transistor, I_D, is given by

cut-off $I_D = 0$ (3 5)

linear $$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right)$$ (3 6)

saturation $$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2[1 + \lambda V_{DS}] \quad (3\ 7)$$

where, μ_n is the mobility of electrons near the silicon surface for the NMOS transistor, Cox is the gate capacitance per unit area, λ is the output impedance constant, and W and L are the width and channel length of the transistor

In analog circuits, the transistors are usually biased to work in the saturated region The reason for this is that when a transistor operates in that region the current is controlled mainly by the gate-source voltage However, as stated in (3 7) the nonzero λ will introduce a dependence on the drain-source voltage as well

High accuracy models such as BSIM3v3 [69, 70] or EKV [37], used for simulation use modeling similar to the simplified models shown here However, the expressions for computing, e g , the drain current of the transistor include many more higher-order effects The expressions used in these high-fidelity, foundry models are not suited for hand calculations

3.1.2. Small-Signal Model

For large signal variations, the large-signal model can be used to predict the behavior of the circuit The small-signal model discussed here is a linearization of the large-signal model around the operating point of the circuit This model is only valid for small perturbations from the operating point The models can be used in order to simplify the calculation of, for example, the frequency dependent properties of the circuit The small-signal model for the NMOS transistor is shown in Figure 3 2

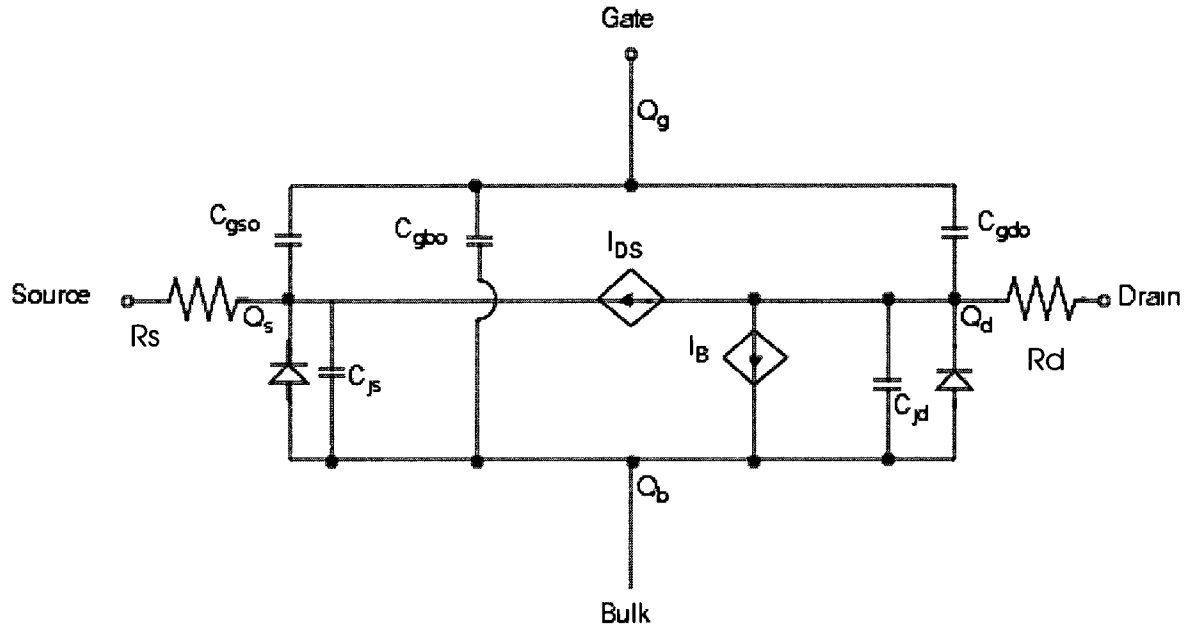


Figure 3 2 Small-signal model of a MOS transistor

The small signal model of a MOS transistor shown above includes the different parasitic capacitance, namely, The Gate-Source Capacitance Cgs0, the Gate-Drain Capacitance Cgd0, the Gate-Bulk capacitance Cgb0, the junction capacitances Cjs and Cjd The Source-Bulk and Drain-Bulk depletion region diodes are also shown in the above Figure 3 2

The different small-signal parameters can be defined for the above transistor as follows gm is the transconductance and gds is the output conductance The small-signal parameters are derived using the expressions (3 8) – (3 10) shown below

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \lambda \qquad (3\ 8)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \qquad (3\ 9)$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \frac{\partial V_{TH}}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} = \eta g_m \tag{3 10}$$

The equations (3 8) and (3 9) can be expressed in terms of the design variables, which typically include the bias current and the Ws and Ls of the transistors in the circuit The gds and gm are expressed below in terms of the design variables in equations (3 11) and (3 12)

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_D}{L(1 + \lambda V_{DS})} \tag{3 11}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2\left[\mu_n C_{ox} I_D \frac{W}{L}(1 + \lambda V_{DS}) \right]^{1/2} \tag{3 12}$$

As in the case with the large-signal model, more accurate small-signal transistor models take into account several additional parameters These higher order effects are accurately captured in the BSIM3v3 Models that are used for simulation

3.2. Modeling of gm and gds

In this section, we describe an improvised model for the small-signal parameters, namely, gm and gds suitable for geometric program based analog circuit sizing As outlined in section 1 1 2, the small signal parameters that are used for simulation based schemes are accurate, while those derived from the long-channel model are compatible for use in equation based approaches Small-signal parameters that are more accurate than the long channel models, but at the same time compatible with geometric programming are modeled through simulation of the transistors [58]

Errors introduced by the long channel model are mainly due to the expressions for the transconductance and the output conductance Here monomial expressions for output conductance (gds) and the transconductance (gm) have been developed for TSMC 0 25μm technology parameters by fitting the data obtained by high fidelity Spectre simulations The monomial expressions for the transconductance and output conductance for NMOS and PMOS are given by

$$g_m(\text{NMOS}) = 35\ 545\, I_D^{0\ 5570}\ W^{0\ 4813}\ \ L^{0\ 4313}, \tag{3 13}$$

$$g_{ds}(\text{NMOS}) = 1\ 187\, I_D^{0\ 6435}\ W^{0\ 3881}\ L^{-1\ 0888}, \tag{3 14}$$

$$g_m(\text{PMOS}) = 6\ 597\, I_D^{0\ 4769}\ W^{0\ 5626}\ \ L^{0\ 6101}, \tag{3 15}$$

$$g_{ds}(\text{PMOS}) = 9\ 67\, I_D^{0\ 8812}\ W^{0\ 1018}\ L^{1\ 2591}, \tag{3 16}$$

where, the output conductance and the transconductance are in milli siemens, the bias current is in amperes, and the width and length are in micrometers For all other device parameters level one model (long-channel model) is used

3.3. Design Example and Results

To test the efficacy of these models, a common source amplifier, shown in Figure 3 3 has been designed using the monomial models above TSMC025μ technology has been used for the design

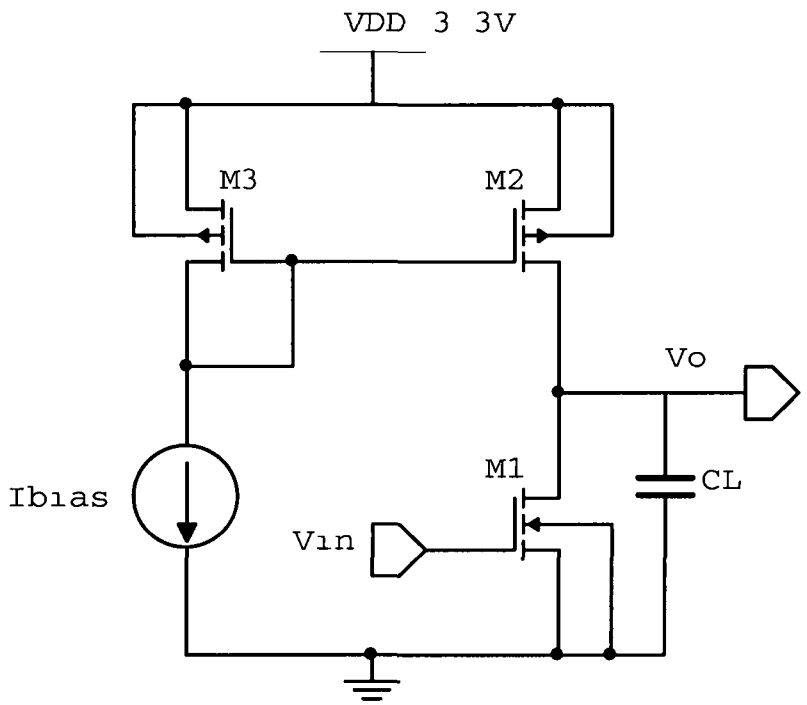


Figure 3 3 Common Source Amplifier

Table 3 1 shows the design constraints for the CS amplifier for which the unity gain bandwidth was maximized The minimum device length and width constraints are due to the lithography and layout rules Table 3 2 shows the solution (optimal value of the design variables)

of the geometric program for the imposed constraints shown in Table 3 1 Accuracy of the design predicted by MOSEK is verified using Spectre simulations It can be seen from Table 3 3 that the simulated values are in close agreement with the values predicted by MOSEK The small discrepancies are due to the use of Level I model for the DC characteristics of the MOS transistors

TABLE 3 1 Imposed Constraints

Constraint	**Value**
Device Length	$\geq 0\ 25\ \mu m$
Device Width	$\geq 0\ 5\ \mu m$
Area	$\leq 100\ \mu m^2$
Open Loop Gain	≥ 80
Unity Gain Bandwidth	Maximize
C_L	10 pF

TABLE 3 2 Mosek Generated Optimal Solution

Variable	**Value**
L1	1 0 μm
L2	1 6 μm
L3	1 6 μm
W1	73 9 μm
W2	11 0 μm
W3	1 6 μm
I_{BIAS}	47 87 μA

TABLE 3 3 Performance Of The Optimal Solution

Constraint	Requirement	Geometric Program	Spectre Verification
Area	$\leq 100\ \mu m^2$	$94\ 0\ \mu m^2$	$94\ 0\ \mu m^2$
Open Loop Gain	≥ 80	80	77 45
Unity Gain Bandwidth	Maximize	50 02 MHz	51 77 MHz

3.4. Summary

In this chapter, we presented a simple approach to model the small signal parameters of the transistors as monomials The monomial models can be used efficiently to solve design problems of low complexity like the simple Common-Source amplifier Our results show that the monomial models for the small-signal parameters are accurate in predicting the different performance constraints like the Open-Loop Gain, the Unity Gain Bandwidth etc The monomial models also accurately capture the dependence of the performance constraints on different design variables like I_D, W and L Our results show performance improvement over the designs using the simple first-order expressions for the small-signal parameters However, there are several critical limitations to the approach

First, we begin by observing the first-order expression for gds and gm in the equations (3 11) and (3 12) It can be seen from these equations that the small-signal parameters exhibit a dependence on the Drain–Source voltage V_{DS} This can be appreciated by understanding the fact that the small signal parameters are strongly dependent on the bias conditions Therefore, for

accurate results, any scheme to model the small-signal parameters should reflect this bias point dependence

It can be observed from equations (3 13) – (3 16) that the monomial models that we use do not accurately reflect this bias point dependence The fact that the equations (3 13) – (3 16) do not include the dependence on V_{DS} results in errors in the final design For a simple design like above, the results are reasonably accurate because the drain currents are estimated from simulations, which partially account for the 'λ' factor In more complex designs, however, the bias point dependence introduces large errors, if not accounted for The errors become unacceptable especially in the deep-sub micron regime, where the short channel effects are more pronounced Errors ranging up to 65% have been reported in estimating the g_{ds} [58]

Methods have been proposed to accurately model the small signal parameters including the bias dependence [57, 58, 71, 72] Especially, efforts have been made to model the small-signal parameters in a form compatible with geometric programming [57, 58] The underlying approach in these methods is to divide the saturation-region into several voltage ranges depending on the overdrive voltage and then fit a piece-wise linear model for each range of overdrive voltage In other words, there is no one global monomial to model the gm (and gds) Instead, the g_m (and g_{ds}) is modeled as a set of 2 – 3 monomials, each suitable for a specific range of overdrive voltage

These schemes result in accurate designs in the sub-micrometer regime However, the time-consuming nature of these schemes undermines the efficiency of the OpAmp design automation process itself Here, we also point out that these approaches to modeling the gm and gds as monomials also adds an overhead to the overall design process In other words, in order to

be compatible with Geometric Programming, the gm and gds have to be modeled as monomials, while incorporating the dependence on the V_{DS}

While we acknowledge that the above methods are worth the effort, we present a framework for design automation of OpAmps that is computationally less intensive Our methodology relies on localized simulation to reduce the errors introduced by the higher order effects

In the following chapter, we present a more straight-forward methodology to automate the design of OpAmps, where efforts are focused on refining the design from a simple first-order design

CHAPTER 4. A FRAMEWORK FOR AUTOMATIC SIZING OF OPAMP CIRCUITS

In this chapter, we propose a methodology [73-76] to automate the transistor-level sizing of OpAmps, which combines the advantages of both the Equation-based and the Simulation-based approaches, while alleviating the disadvantages of both these approaches The methodology is outlined in this section The methodology relies on the initial use of Equation-based scheme to generate a first order design, which can be refined by using a localized Simulation-based approach This method eliminates the need for DC root solving in each iteration [77, 78] and eliminates the need for relaxed DC formulation [79, 80] As the operating point is not calculated manually as in [81], we do not run in to similar convergence problems

The main strengths of our approach are

(i) The equation based scheme uses first order device models to generate a first-order model of equations that define the OpAmp sizing problem This model can be easily generated and easily solved using an optimization to yield a first-order design The lack of accuracy of this first-order design is addressed in the next step, where a localized simulation-approach is adopted

(ii) The simulation-based scheme provides the accuracy of higher order BSIM models, while localizing the simulations around the proximity of the initial guess drastically reduces the number of simulations required, thereby reducing the design time

(iii) The problem of modeling circuit behavior from empirical data has been solved by the use of monomial equations, which can be very easily generated from simple regression schemes Within the local vicinity of the initial guess design, the monomials have the full

accuracy of BSIM Models used for simulation This eliminates the overhead of generating elaborate posynomial design equations

(iv) The framework is technology-independent and topology-independent Our results show that the framework can be used to design different Operational amplifiers topologies across different technologies

In effect, our methodology has the advantages of (a) the equation-based approach through reduced design time, (b) the simulation-based approach through increased accuracy, as well as (c) ease of modeling the design equations and (d) technology independence and topology independence

The chapter is organized in the following manner Section 4 1 outlines the general design flow in the framework The framework is a cohesive tool that incorporates various rigorous mathematical techniques, alongside several algorithms programmed in SKILL language of Cadence Each of these sub sections are briefly outlined in section 4 1, while a detailed description of each is presented in the subsequent sections of this chapter

4.1. The Design Flow

The general design flow of the framework, shown in Figure 4 1, is presented in this section The design flow progresses by sequentially executing the following steps

Step–One: Netlist Parser: The OpAmp design problem is modeled as a set of first-order equations that can be solved using geometric programming based optimization scheme The result of the optimization is a first-order design, which is used in the next step as an 'initial-guess' design point

The design equations and design constraints based on the first-order device models can be easily derived from the netlist of the OpAmp by executing a set of general heuristic rules We use this approach to automatically generate the large-signal equations The small-signal equations can be generated using symbolic analysis techniques or handwritten equations can also be used to model the circuit's behavior and the various constraints As this model represents only the initial step of the design process, the accuracy of these equations does not adversely affect the final design

Step–Two: Design of Experiments: The OpAmp circuit is simulated on a set of data samples spaced in the proximity of the 'initial-guess' design point obtained from the previous step These simulations facilitate in capturing the performance of the circuit accurately, which constitutes the next step of the design flow The set of data samples is generated using design of experiments (DOE)

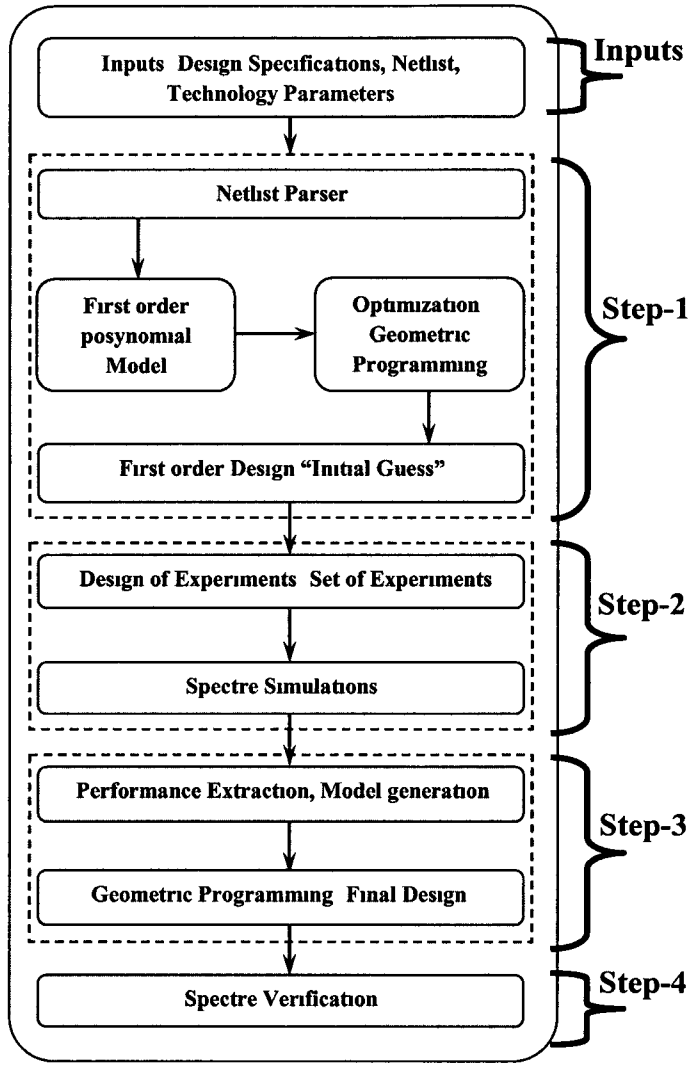


Figure 4 1 The Design Flow

Step–Three: Performance Extraction: The results of the simulations are now distilled and formulated as an optimization problem This optimization problem constitutes the design problem which, when solved using geometric programming, results in an accurate final-design that meets the various performance requirements

Step–Four: Spectre Verification: The accuracy of the design solution obtained from the previous step is validated using device-level simulations In Figure 4 1, each of these steps, 1 – 4, is enclosed in the dashed box to show the design flow

Our results show that this scheme results in an accurate design that meets all the performance specifications However, if one desires to further refine the design point, our framework allows for further refining of the results through iterative repetition of the design flow In other words, the final design obtained from Step-Three can be iteratively used as the initial-guess design to start another loop of design-flow that results in a more accurate design

In the following sections, a more detailed description of our approach is presented with a running example of a two stage OpAmp example shown in Figure 4 2

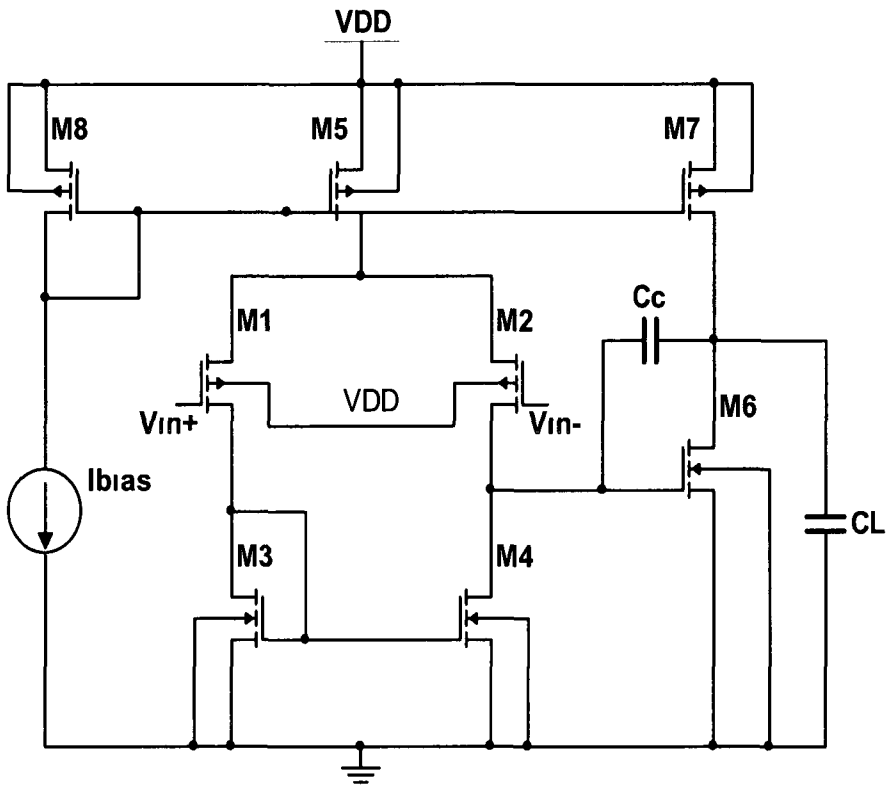


Figure 4 2 Two Stage OpAmp Circuit

The two stage OpAmps are among the most widely used electronic devices today, appearing in a vast array of consumer, industrial, and scientific devices The application of a two stage OpAmp is very wide spread Places where a high input impedance and low output impedance is required two stage OpAmps are suitably used The basic topology of the two stage OpAmp consists of a differential stage cascaded by a Common Source stage Generally, a compensation scheme called Miller Compensation is used for stability as shown in Figure 4 2

4.2. Netlist Parser

A set of equations that accurately describes the first order behavior of the OpAmp is modeled as posynomials This constitutes the first step in our framework This is accomplished by the Netlist Parser tool shown in Figure 4 3, which forms the initial step of our design flow The Netlist Parser is programmed in SKILL language of Cadence As seen from Figure 4 1, using the circuit's Netlist, design specifications and the technology parameters as inputs, the Netlist Parser accomplishes several tasks which are transparent to the designer From the designer's perspective, these are the only inputs the designer has to specify throughout the design process The Netlist Parser tool incorporates several appropriate programming principles as outlined in [82]

The Netlist Parser tool accomplishes several tasks (a) capture the circuit information from the Netlist into a data structure, (b) identify the different components of the Netlist and then establish a set of independent design variables for the design, and (c) formulate a set of first-order design equations to model the design problem as a GP problem In principle, this approach is similar to the constraints extraction method presented in [83] Two algorithms shown in Figure 4 3 and Figure 4 4 are the basic modules of the Netlist Parser tool that accomplish the above tasks

4.2.1. Netlist Parser – Module 1:

It can be seen from the Module 1 algorithm that we implement a depth first scheme while parsing the netlist In other words, for each component in the Netlist, we first identify its type, append its terminal connectivity information into a data structure, *netinfo*, identify the corresponding design variable and append that information into another data structure, *desvar* It

is only after all the above information for a particular component has been incorporated into respective data structures that the algorithm proceeds to parse the next line of the netlist This process is repeated till the end of the netlist is reached Module 1, thus accomplishes tasks (a) and (b) described in Section 4 2 The data structure implemented here is similar to that proposed in [84]

For the example OpAmp shown, the set of independent variables is

$$D = \{L1, L3, L5, L6, W1, W3, W5, W6, W7, (Ibias/W8) \text{ and } Cc\} \quad (4\ 1)$$

Note from Figure 4 2 that the transistors M1, M2 and M3, M4 form matched pairs The equations (4 2) – (4 5) shown below represent this constraint

$$W1 = W2 \quad (4\ 2)$$

$$L1 = L2 \quad (4\ 3)$$

$$W3 = W4 \quad (4\ 4)$$

$$L3 = L4 \quad (4\ 5)$$

The transistors M5, M7 and M8 have matched lengths for faithful current copy properties, as shown in equation (4 6)

$$L5 = L7 = L8 \quad (4\ 6)$$

Also, we use a single design variable (Ibias/W8) instead of two separate design variables The reason for this choice of design variable can be appreciated from Figure 4 2 by observing that Ibias and M8 together set the current flowing through the different branches In other words, the ratio (Ibias/W8) is a property of the circuit that effectively determines its performance This

observation suggests that the use of one design variable (Ibias/W8) in place of Ibias and W8 separately is more appropriate The advantage of this design variable becomes more obvious in the following section

Lithography constraints and layout rules impose minimum limits on the device sizes These conditions can be expressed as

$$Lmin \leq Li \tag{4 7}$$

$$Wmin \leq Wi \ , \ i = 1,2 \quad 8 \tag{4 8}$$

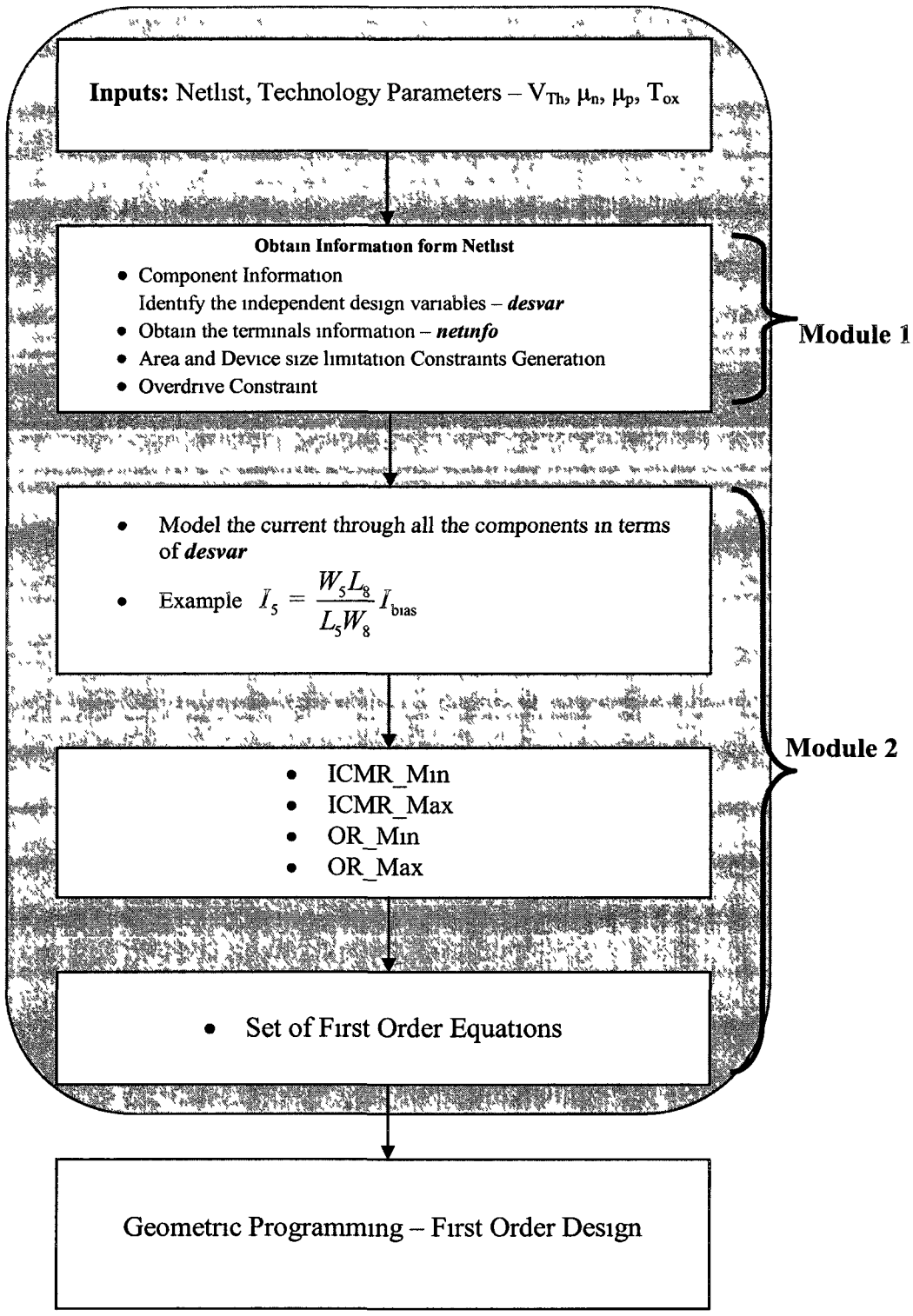


Figure 4 3 The Netlist Parser

4 2.2. Netlist Parser – Module 2

In addition to identifying the independent design variables, the Netlist Parser tool performs the task of automatically generating the first order model equations for the various large-signal constraints of the design This task of formulating a set of posynomial equations is addressed in Module 2 shown below Module 2 is comprised of three subroutines, each performing a critical task

The Current_Source subroutine implements a depth first scheme Its main purpose is three fold (a) to identify DC current source I and the current source transistor being fed by I, (b) to identify all the remaining current mirror transistors that ration the current from the current source transistor and finally, (c) express the current in each current mirror transistor as function of its W, L and the current source variable I In other words, the current through each current mirror transistor is expressed as a posynomial in design variables This is necessary because all the model equations have to be eventually expressed as posynomial functions of the design variables as in equation (4 9)

$$I_5 = \frac{W_5 L_8}{L_5 W_8} I_{bias} \qquad I_7 = \frac{W_7 L_8}{L_7 W_8} I_{bias} \tag{4 9}$$

The next two subroutines in the Module 2 are ICMR subroutine and OR subroutine They are programmed to derive posynomial expressions for the Input Common Mode Range and the Output Range respectively This is accomplished by performing a tree search on the data structure and identifying the different DC paths in the circuit It can be seen that to accomplish the task of modeling the ICMR and OR expressions, these subroutines implement a breadth first scheme For example, while evaluating the ICMR Max of the OpAmp, the corresponding

subroutine first identifies all the transistors in the DC path from Vin to Vdd After traversing all the allowable paths for the ICMR_Max, the subroutine then expresses each of these paths as a posynomial equation in the function of the design variables

```
1  Begin Module 2
2  Accept user_inputs, netInfo, desvar from Module 1
3  Start Current_Source_Count =0
4  Begin Current_Source subroutine
   4 1  Identify desvar I
   4 2  Load netInfo for I
   4 3  if netInfo I == netInfo V
        4 3 1  EXIT 4 1
   4 4  else if netInfo I == netnfo M
        4 4 1  DO
                  4 4 1 1  Current_Source_Count ++
                  4 4 1 2  temp = netInfo M
                  4 4 1 3  Append M to data structure Current_Comp
                  4 4 1 4  Express current through temp in W L of temp and I
                  4 4 1 5  Identify next Gate connected to Gate of M
               WHILE Next Gate is not Nil
5  END Current_Source subroutine
6  BEGIN ICMR subroutine
   6 1  for(i=0 i<1 i++)
        6 1 1  DO
                  6 1 1 1  Begin @ Vin
                  6 1 1 2  ICMR_Min_Path(i) == Trace Path to Gnd, obtain equation in W L, I
                  6 1 1 3  ICMR_Max_Path (i) == Trace Path to Vdd, obtain equation in W L I
                  6 1 1 4  For Each M in path Express Currnet through M in W, L and I
                  6 1 1 5  Return ICMR_Min_Path
                  6 1 1 6  Return ICMR_Min_Path
7  END ICMR subroutine
8  BEGIN OR subroutine
   8 1  Begin @ Vout
   8 2  OR_Min_Path = Trace Path to Gnd obtain equation in W, L I
   8 3  OR_Max_Path = Trace Path to Vdd, obtain equation in W, L I
   8 4  For Each M in path Express Currnet through M in W, L and I
   8 5  Return OR_Min_Path
   8 6  Return OR_Max_Path
9  END OR Subroutine
10 END Module 2
```

Figure 4 4 Netlist Parser Module 2

For the OpAmp example, the equations (4 10) and (4 11) ensure that all the transistors are in saturation region of operation

Input Common Mode Range ≥ ICMR-spec (4 10)

Output Range ≥ OR-spec (4 11)

In addition, it is desirable to impose conditions on minimum gate overdrive voltage on all transistors This is important to ensure that the transistors operate away from the sub-threshold region For any given transistor, the gate overdrive voltage can be expressed as

$$V_{gs} - V_T = \sqrt{\frac{I_D L}{\mu C_{ox}/2W}} \geq V_{\text{overdrive min}} \quad (4\ 12)$$

The small-signal and the time domain constraints are expressed manually in posynomial form Alternatively, with small modifications, our Netlist Parser tool can accommodate the use of symbolic analysis techniques to generate the small signal constraints [31, 85-92] However, the main advantage of our approach is that the use of complex small signal equations can be eliminated in the first step, thus gaining speed for accuracy The lack of accuracy of this step is addressed in the following simulation phase, where the models generated by fitting the simulated data more accurately describe the circuit's behavior

For the example OpAmp, the equations (4 13) – (4 18) shown below, together with the Objective Function, represent a complete set of posynomial equations that constitute the first order design model

Objective Minimize 1/ (Gain Band Width product (GBW))

Subject to Input Common Mode Range ≥ ICMR-spec (4 13)

Output Range ≥ OR-spec (4 14)

Overdrive ≥ Overdrive-spec (4 15)

PM, (Phase Margin) ≥ PM-spec (4 16)

W1 ≥ Wmin (4 17)

L1 ≥ Lmin (4 18)

The reason for using Gain Bandwidth Product as the objective is because this parameter characterizes the frequency dependence of OpAmps The GBW determines the maximum gain that can be extracted from a given topology for a given frequency By maximizing the GBW, the gain that can be obtained for a given bandwidth can be maximized Thus, the GBW is a more fundamental parameter of the circuits, maximizing which ensures maximum gain for a given bandwidth in a given technology

The expression for the GBW in terms of the design variables is shown below follows

$$GBW = \frac{g_{m1}}{C_L} = (2\mu_n C_{ox})^{1/2}(I_{bias})^{0.5}(W_1)^{0.5}(L_1)^{-0.5}(W_5)^{0.5}(L_5)^{-0.5}(W_8)^{-0.5}(L_8)^{0.5}(C_c)^{-1} \quad (4\ 19)$$

The PM-spec was chosen to be 60 degrees To ensure a 60 degree Phase Margin, the conditions to be satisfied can be shown as follows

$$(i) Output - Pole > 2.2 GBW \Rightarrow (g_{m6}/C_L) > 2.2(g_{m2}/C_c) \quad (4\ 20)$$

$$(ii) RHP - zero > 10 GBW \Rightarrow (g_{m6}/C_c) > 10(g_{m1}/C_c) \quad (4\ 21)$$

Combining equations (4 20) and (4 21), and observing that gm1 = gm2, the expression for constraint for PM can be expressed in terms of the design variables as follows

$$C_c > 0\ 22C_L \tag{4 22}$$

The expressions for ICMR in terms of the design variables are shown below

$$ICMR(Max) = 149\ 378(I_{bias})^{0\ 5}(W_1)^{-0\ 5}(L_1)^{0\ 5}(L_8)^{0\ 5}(W_5)^{0\ 5}(L_5)^{-0\ 5} + 211\ 25(I_{bias})^{0\ 5}(L_8)^{0\ 5} \tag{4 23}$$

$$ICMR(Min) = 59\ 39(I_{bias})^{0\ 5}(W_4)^{-0\ 5}(L_4)^{0\ 5}(L_8)^{0\ 5}(W_5)^{0\ 5}(L_5)^{-0\ 5} \tag{4 24}$$

Similarly, the expressions for OR in terms of the design variables are shown below

$$OR(Max) = 103\ 13(I_{bias})^{0\ 5}(W_6)^{-0\ 5}(L_6)^{0\ 5}(L_8)^{0\ 5}(W_7)^{0\ 5}(L_7)^{-0\ 5} \tag{4 25}$$

$$OR(Min) = 144\ 52(I_{bias})^{0\ 5}(L_8)^{0\ 5} \tag{4 26}$$

Thus, in effect, the Netlist Parser tool generates a set of posynomial equations (in design variables), that collectively defines an OpAmp Design problem However, this set of equations is first-order in nature as the higher order effects are not accounted for from these simple equations This set of posynomial equations yields a first-order design, when solved using Geometric Programming technique

4.3. Design Of Experiments

The first order design obtained from the Geometric Programing is used as the initial design point in this step A set of 256 design points placed on the boundaries of a hypercube centered on the initial design point is generated by following a Latin-hypercube scheme of DOE The size of the hypercube is selected so as to allow for a 10% variation of the design variables on

both sides of the initial-guess Now, the set of 256 data samples obtained from DOE is simulated using Cadence Spectre This constitutes the second step of our design flow

The use of (Ibias/W8) as a single design variable instead of two separate design variables is necessary here Using two separate variables results in the data samples where Ibias and W8 vary independently In other words, the DOE generates a set of samples that allow the variables Ibias and W8 to vary in opposite directions This results in an anomaly, because, it can be observed from Figure 4 2 that they form a pair of design variables that need to scale together To alleviate this anomaly, the use of a single variable (Ibias/W8) is more appropriate

Of the steps 1 - 4 described in this chapter, the second step, which constitutes simulation of 256 data samples, has been identified as the most computationally intensive part of the design flow For the example OpAmp, when simulated on Sun Sparcv9 processor operating at 1 5 GHz speed, running on Solaris platform, the second step took about 125 minutes to complete However, as all the simulations are independent of the others, parallelization of these simulations on a cluster of workstations with appropriate load balancing scheme can drastically reduce the design time The rest of the steps amounted to less than 240 seconds, which is only a fraction of the total design time

4.4. Performance Extraction

The next step of our approach consists of distilling the results from the Spectre simulations performed in section 4 3 Of the 256 data samples simulated, 165 samples yielded feasible DC solutions The rest of the data samples resulted in one or more transistors out of the saturation region A test bench subroutine has been programmed in SKILL to automatically eliminate those simulations that do not result in a feasible DC operating region In other words,

as the design variables are placed on the boundaries of the hypercube in the DOE stage, some of the simulations can correspond to such sample set of the design variables, which could place one or more of the transistors out of saturation This will inevitably introduce an error in the final model, thereby causing dubious results The test bench identifies the simulations in which one or more transistors are out of saturation by combing through the DC-operating point information for each simulation

We take advantage of the hierarchical format in which the Cadence Analog Design Environment saves the operating point information for each component after DC analysis The subroutine also performs the additional task of tabulating the different performance constraints for each simulation, by combing the different AC, DC and Transient Analyses results After filtering out the non-feasible data samples, the various performance constraints are automatically extracted in each run and tabulated

4.4.1. Performance Modeling

The method of generating monomial equations from these tabulated results is called performance modeling and is explained below

Consider an electronic system (E) shown in the figure below, where, I and O represent the input and output signals respectively

The mathematical modeling of the Input-Output relation is called behavioral modeling [93-98] and is beyond the scope of this work However, without delving into the concepts of actual behavioral modeling, let us assume, that the relation between I and O can be expressed as below

$$\mathbf{O = E(I, D)} \tag{4 23}$$

where, D is a set of design variables that governs the input-output relationship The job of a designer on the other hand, is to choose a set of appropriate values for D so as to satisfy a set of performance metrics P In other words, as a designer, one is interested in modeling the relation between the different performance metrics and the independent design variables as shown below

$$\mathbf{P = F(D)} \tag{4 24}$$

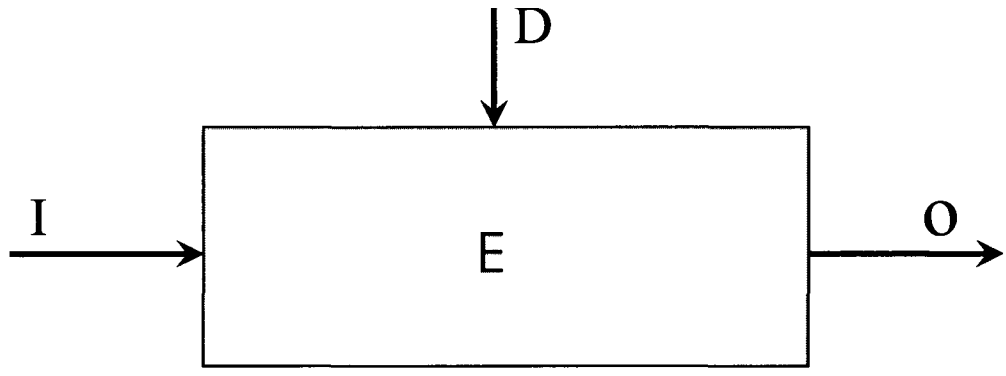


Figure 4 5 Behavioral Modeling

Modeling the relation between P and D is called performance modeling and forms the fundamental approach to model monomial design equations for the OpAmp design problem For the OpAmp example, the set of different performance metrics like Gain-Bandwidth Product, Phase Margin, etc , form the set of P, while the set of D is constituted by the independent variables shown in equation (4 1)

A monomial expression is fitted for each of the various performance constraints like Gain-Bandwidth Product, Phase Margin, etc These monomial expressions accurately predict the relation between the performance constraints and the independent design variables, within the

local proximity of the initial-guess design Our results show that these models are very accurate within ±10% of the initial-guess These models constitute a complete set of design equations that formulate the design problem compatible with mosek

4.5. Spectre verification

The result of this optimization is a final design that meets all the performance constraints For the OpAmp example, this constitutes the sizes for the different independent design variables The final design obtained is verified by using Spectre simulations

It has been seen that the final design meets all the performance specifications as imposed by the performance metrics for different OpAmp topologies across different topologies In effect, the final design solution is the final sized circuit obtained to meet all the performance metrics

CHAPTER 5. RESULTS

The framework presented in chapter 4 is applied to design different OpAmp topologies across different technology platforms To demonstrate and validate the efficacy of the approach, we designed the two stage OpAmp and a Telescopic OpAmp in TSMC025μ and AMI016μ technologies In this chapter, we present the results for these designs

5.1. Two Stage OpAmp

In this section, results are presented for the design problem of the two stage OpAmp example that we have been using as a running example (Figure 4 2) The two stage OpAmp has been designed in TSMC025μ and AMI016μ technologies The foregoing discussion of TSMC025μ technology is also relevant in the context of AMI016μ technology

5.1.1. TSMC025μ Technology

Table 5 1 shows the final monomial model obtained by fitting the TSMC025μ technology simulation data for the DC Gain (Av), Gain Bandwidth Product (GBW), and the Phase Margin (PM) The coefficients of the monomials are also provided along with the powers of the different independent variables in the monomial Both the GBW and PM exhibit dependence similar to that expected from the first-order model For example, the first order posynomial defining the GBW shown in equation (4 19) is reproduced below

$$GBW = \frac{g_{m1}}{C_L} = (2\mu_n C_{ox})^{1/2} (I_{bias})^{0.5} (W_1)^{0.5} (L_1)^{-0.5} (W_5)^{0.5} (L_5)^{-0.5} (W_8)^{-0.5} (L_8)^{0.5} (C_c)^{-1} \qquad (5\ 1)$$

However, the monomial model shown in Table 5 1 is more accurate than the first order model shown in (5 1) because the higher order effects are captured from the simulation Also, note that we have modeled the monomial to reflect the dependencies of GBW and PM on all the design variables This further improves the accuracy of the final model

TABLE 5 1 Two-Stage OpAmp Monomial Model Fitted From Simulations (TSMC025)

Design Variable	Power of the Design Variable			Units
	Av	GBW	PM	
L1	0 004	-0 537	0 157	μM
L3	0 066	0 006	-0 022	μM
L5	0 026	0 012	-0 104	μM
L6	0 064	-0 016	-0 214	μM
W1	0 049	0 441	-0 250	μM
W3	0 162	0 085	-0 067	μM
W5	-0 225	0 456	-0 113	μM
W6	-0 152	-0 142	0 210	μM
W7	0 132	0 049	0 092	μM
Ibias/W8	-0 062	0 489	-0 068	A /μM
Cc	0 002	-0 899	0 350	F
Coefficient	Exp(3 85)	Exp(-3 596)	Exp(12 72)	

It can be observed from Table 5 1 that variation of Cc affects the GBW and PM in opposite directions, as is the case with most of the other design variables Thus, by modeling the GBW as the objective function of optimization, and imposing a minimum restriction on the PM, the optimization converges to a solution in the design space that critically satisfies the PM

constraint, while maximizing the GBW Also, it can be seen that the final design improves the GBW In other words, the final design performs better than the initial first order guess However, the performance of the first order model for this simple circuit is not unacceptable The advantage of our approach could become more obvious in more complex circuits where the initial first order design can not accurately predict the performance

Table 5 2 shows the design for TSMC025μ technology obtained from the geometric optimization It can be observed that final design point is within ±10% of the initial first order design This is achieved by imposing additional constraints in Mosek that restrict the design variables within acceptable proximity of the first order design This is necessary to preserve the accuracy of the models The results of the spectre simulation on both the initial first order design and the final design for TSMC025μ technology are shown in Table 5 3

TABLE 5 2 Design Of Two Stage OpAmp For TSMC025

Design Variable	First Order Design	Final Design	Units
L1	0 5	0 5	µM
L3	0 5	0 5	µM
L5	0 5	0 5	µM
L6	0 5	0 5	µM
W1	157 03	140	µM
W3	14 5	13	µM
W5	34 97	36 14	µM
W6	281 72	275 26	µM
W7	339 73	382 6	µM
W8	0 5	0 5	µM
Ibias	12 6	12 1	µA
Cc	2 44	2 2	pF

TABLE 5 3 Performance Of Two Stage OpAmp In TSMC025

Performance	Specs	First Order Design	Final Design	Units
Av	--	64 54	63 89	dB
PM	≥ 60	59 6	60	degree
GBW	Maximize	221 57	231 49	M Hz

TABLE 5 4 Performance Of The Monomial Model (TSMC025) Of Two-Stage OpAmp

Design Constraint	Mean Absolute Error (%)	Maximum Absolute Error %
Av	3 8	15 4
GBW	1 8	11 0
PM	0 4	2 3

Table 5 4 shows the performance of the monomial model in estimating the various performance constraints For the 165 valid simulations, the percentage values of the maximum absolute error and the mean absolute error between the BSIM data and the monomial predicted values are shown in Table 5 4 It can be seen that the percentage mean absolute error is below 5% for all the three performance constraints considered here

The bode plots showing the magnitude response and the phase response of the two-stage OpAmp are shown in Figure 5 1 The bode magnitude response shows a low-frequency (DC) gain equal to 64dB It can be seen that the magnitude of gain falls at -20dB/decade as expected from a single pole circuit Unity Gain Frequency (UGF) is defined as that frequency where the gain falls to unity Shown on the dB scale, this corresponds to 0 dB Theoretically, the UGF and the GBW are equal for a single pole behavior However, the second non-dominant pole, which is in the proximity of the GBW affects the magnitude response of the circuit, thereby reducing the UGF to a value lower than the GBW

The bode phase response behavior, shown in Figure 5 1, is as expected for a system with Miller compensation The first dominant pole is moved close to the origin, while the second dominant pole is moved away The exact location of the two dominant poles is determined so as to satisfy the GBW and Phase Margin constraints The phase of the OpAmp is close to 180

degrees at low-frequencies and begins to fall at a rate of approximately –45 degrees/decade at a frequency that is ten times lower than the first dominant pole frequency At the pole frequency, the phase is 135 degrees The phase continues to fall at the –45 degrees/decade rate up to ten times the dominant pole frequency before stabilizing at 90 degrees The second dominant pole then begins to effect the phase, dropping the phase again at a rate of – 45 degrees/decade The location of the second dominant pole is carefully chosen to meet the Phase Margin specification of 60 degrees Phase Margin is defined as the value of the phase evaluated at UGF It can be seen from the Figure 5 1 that the Phase Margin is approximately 60 degrees

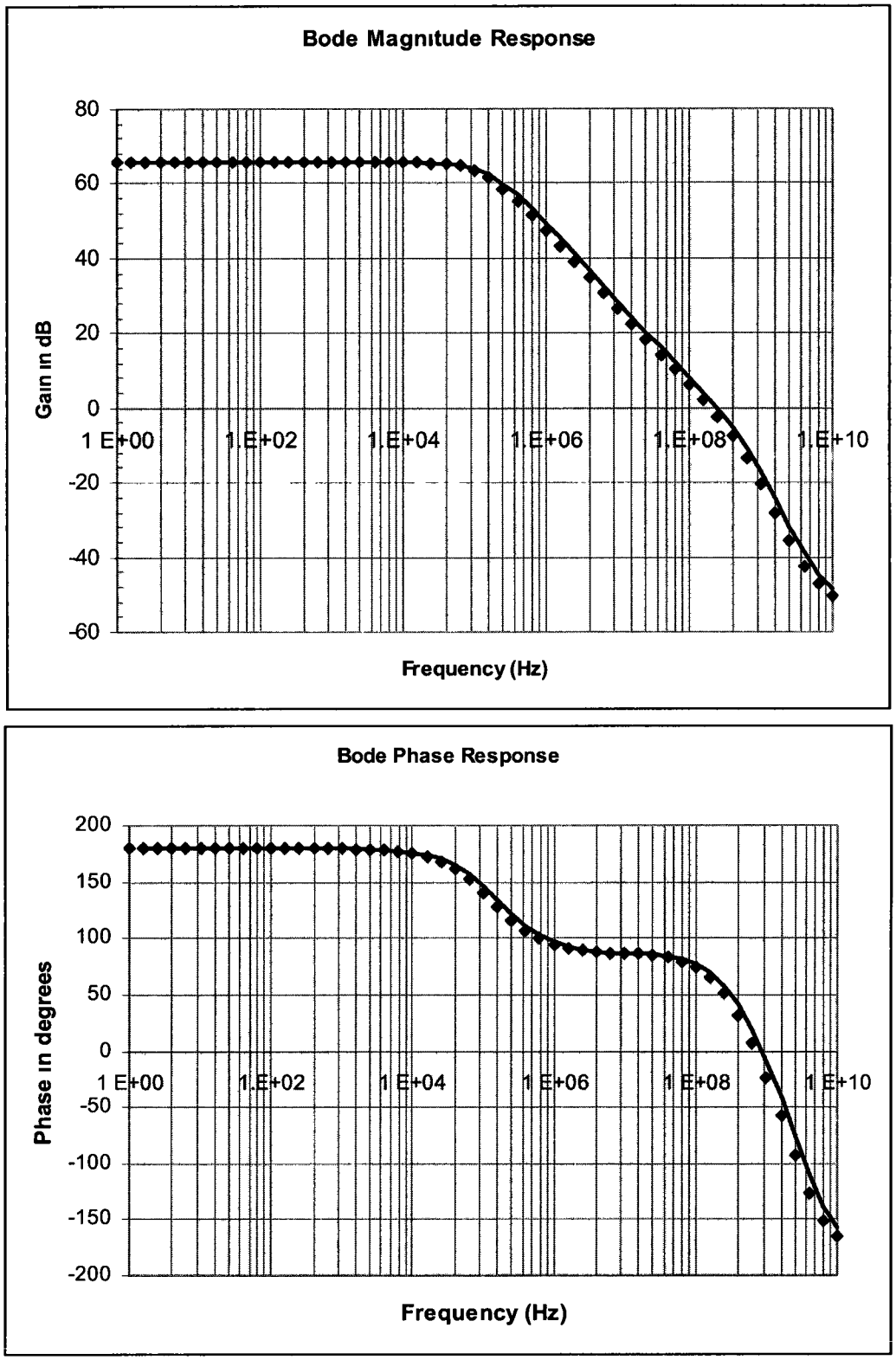


Figure 5 1 Bode plot for Two-Stage OpAmp in TSMC025 design

5.1.2. AMI016µ Technology

Table 5 5 shows the final monomial model obtained by fitting the AMI016µ technology simulation data for the DC Gain (Av), Gain Bandwidth Product (GBW), and the Phase Margin (PM) The coefficients of the monomials are also provided along with the powers of the different independent variables in the monomial

TABLE 5 5 Two-Stage OpAmp Monomial Model Fitted From Simulations (AMI016)

Design Variable	Power of the Design Variable			Units
	Av	GBW	PM	
L1	-0 033	-0 505	0 118	µM
L3	0 383	0 082	-0 055	µM
L5	-0 031	-0 025	-0 014	µM
L6	-0 362	-0 098	-0 180	µM
W1	0 062	0 47	-0 206	µM
W3	-0 369	-0 079	0 017	µM
W5	0 330	0 620	-0 176	µM
W6	0 429	0 080	0 079	µM
W7	-0 415	-0 104	0 166	µM
Ibias/W8	-0 125	0 600	-0 031	A /µM
Cc	-0 007	-0 966	0 330	F
Coefficient	Exp(2 22)	Exp(-4 668)	Exp(12 70)	

TABLE 5 6 Design Of Two Stage OpAmp For AMI016

Design Variable	**First Order Design**	**Final Design**	**Units**
L1	0 32	0 32	µM
L3	0 32	0 32	µM
L5	0 32	0 32	µM
L6	0 32	0 32	µM
W1	47 38	44 22	µM
W3	4 20	4 20	µM
W5	9 93	14 98	µM
W6	91 32	72 0	µM
W7	108 10	128 73	µM
W8	0 16	0 16	µM
Ibias	7 86	6 91	µA
Cc	2 44	2 2	pF

Table 5 6 above shows the design for AMI016µ technology obtained from the Geometric optimization The results of the spectre simulation on both the initial first order design and the final design for AMI016µ technology are shown in Table 5 7 below

TABLE 5 7 Performance Of Two Stage OpAmp In AMI016

Performance	Specs	First Order Design	Final Design	Units
Av	-	76 91	75 56	dB
PM	≥ 60	64 01	60 63	degree
GBW	Maximize	15 9	18 33	M Hz

Table 5 8 shows the performance of the monomial model in estimating the various performance constraints For the 115 valid simulations, the percentage values of the maximum absolute error and the mean absolute error between the BSIM data and the monomial predicted values are shown in Table 5 8 It can be seen that the percentage mean absolute error is below 10% for all the three performance constraints considered here The relatively high percentage error in this design, compared to the TSMC025 design, can be attributed to the fact that the number of valid simulations in this case is smaller This decreases the fidelity of the final monomial and hence increases the error percentage

TABLE 5 8 Performance Of The Monomial Model (AMI016) Of Two-Stage OpAmp

Design Constraint	Mean Absolute Error (%)	Maximum Absolute Error %
Av	7 3	22 4
GBW	5 8	16 4
PM	2 6	8 1

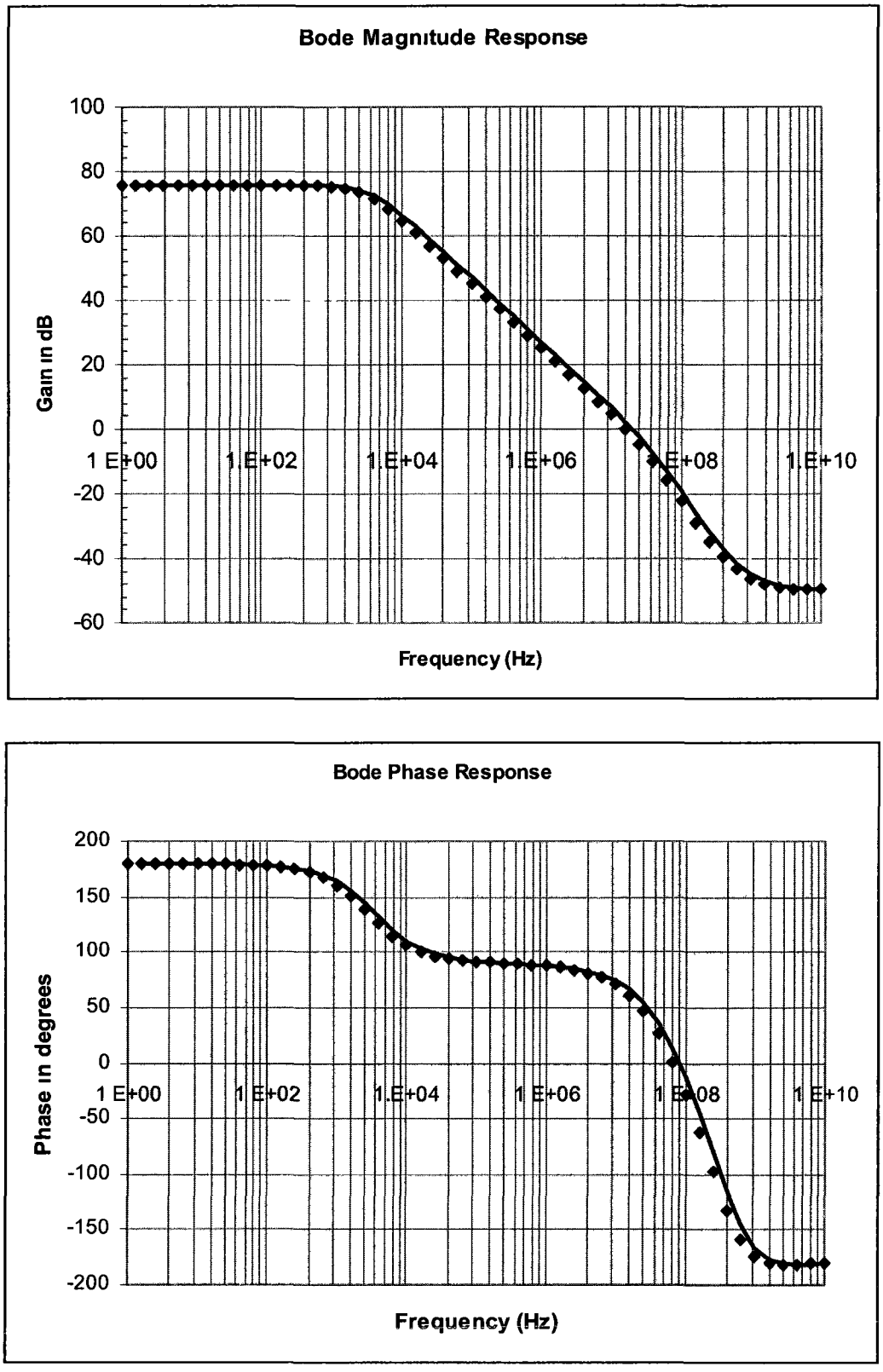


Figure 5 2 Bode plot for Two-Stage OpAmp in AMI016 design.

The bode plots showing the magnitude response and the phase response of the two-stage OpAmp for AMI016μ technology are shown in Figure 5 3 It can be seen that the UGF of the OpAmp is approximately 15 91 M Hz, while the Phase Margin, defined as the Phase at UGF is approximately equal to 60 degrees

5.2. Telescopic OpAmp

In this section, results are presented for the design problem of a Telescopic OpAmp shown in Figure 5 3 The Telescopic OpAmp usually provides the best tradeoff between gain, power dissipation and speed But the voltage head-room and leg-room or the swing of the output signal is limited because of the presence of multiple cascode stages This single stage OpAmp finds multiple applications in low power, high gain applications

The Figure 5 3 shows a conventional Telescopic OpAmp Several variations of this basic telescopic OpAmp have been devised in literature [99] We design a general purpose Telescopic OpAmp shown in Figure 5 3 for validation of the Framework in Chapter 4

The Telescopic OpAmp has been designed in TSMC025μ and AMI016μ technologies The foregoing discussion for TSMC025μ technology is also relevant in the context of AMI016μ technology

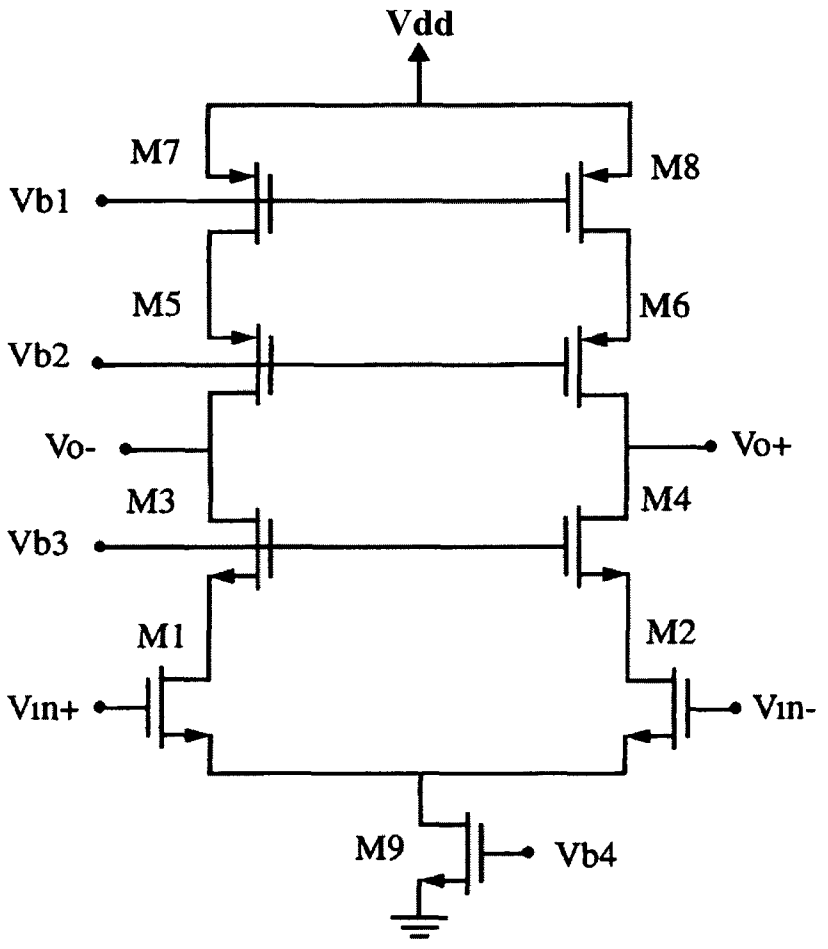


Figure 5 3 Telescopic OpAmp

5.2.1. TSMC025μ Technology

Table 5 9 shows the final monomial model obtained by fitting the TSMC025μ technology simulation data for the DC Gain (Av), Gain Bandwidth Product (GBW), and the Phase Margin (PM) The coefficients of the monomials are also provided along with the powers of the different independent variables in the monomial It can be seen that both the GBW and PM exhibit dependence similar to that expected from the first-order model However. this monomial model

is more accurate than the first order model because we have modeled the monomial to reflect the dependencies of Av, GBW and PM on all the design variables

TABLE 5 9 Telescopic OpAmp Monomial Model Fitted From Simulations (TSMC025)

Design Variable	Power of the Design Variable			Units
	Av	GBW	PM	
L1	0 112	-0 035	-0 075	μM
L3	0 056	-0 044	-0 089	μM
L5	-0 247	-0 027	-0 169	μM
L9	-0 002	0 006	0 002	μM
W1	-0 002	0 120	-0 273	μM
W3	0 040	0 052	0 071	μM
W5	0 234	0 021	-0 022	μM
W9	-0 275	0 799	-0 172	μM
Ibias	-0 269	0 779	-0 162	A/μM
Coefficient	Exp(1 561)	Exp(22 986)	Exp(4 624)	

Table 5 10 below shows the design for TSMC025μ technology obtained from the Geometric optimization It can be observed that final design point is within ±10% of the initial first order design This is achieved by imposing additional constraints in Mosek that restrict the design variables within acceptable proximity of the first order design

TABLE 5 10 Design Of Telescopic OpAmp For TSMC025

Design Variable	First Order Design	Final Design	Units
L1	0 5	0 5	μM
L3	0 5	0 5	μM
L5	0 5	0 5	μM
L9	0 5	0 5	μM
W1	898 26	873 64	μM
W3	21 29	23 42	μM
W5	30 25	33 27	μM
W9	39 91	43 90	μM
Ibias	48 9	44 54	μA/μM

The results of the spectre simulation on both the initial first order design and the final design for TSMC025μ technology are shown in Table 5 11 below

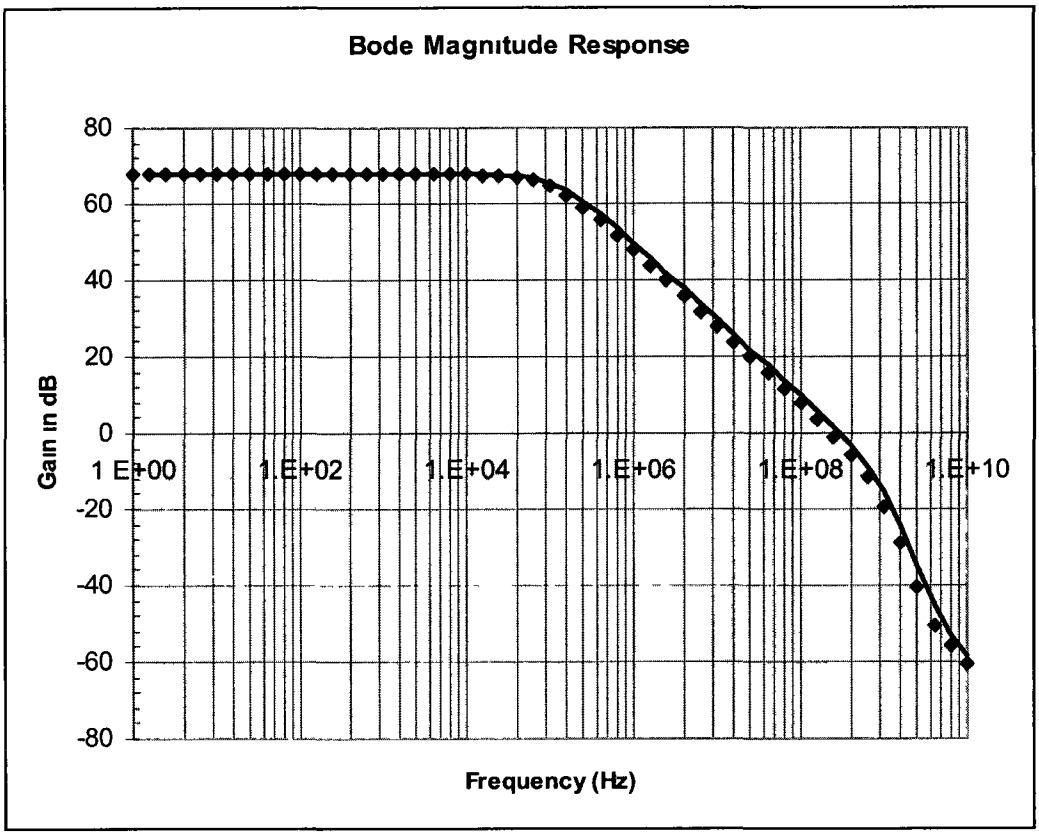
TABLE 5 11 Performance Of Telescopic OpAmp In TSMC025

Performance	Specs	First Order Design	Final Design	Units
Av	-	67 25	66 55	dB
PM	≥ 60	61 304	60	degree
GBW	Maximize	227	238 85	M Hz

Table 5 12 below shows the performance of the monomial model in estimating the various performance constraints For the 256 simulations performed, all the 256 simulations yielded feasible DC solutions The percentage values of the maximum absolute error and the mean absolute error between the BSIM data and the monomial predicted values are shown in Table 5 12 It can be seen that the percentage mean absolute error is below 2% for all the three performance constraints considered here

TABLE 5 12 Performance Of The Monomial Model (TSMC025) of Telescopic OpAmp

Design Constraint	**Mean Absolute Error (%)**	**Maximum Absolute Error %**
Av	1 6	8 2
GBW	0 9	4 7
PM	0 12	1 5



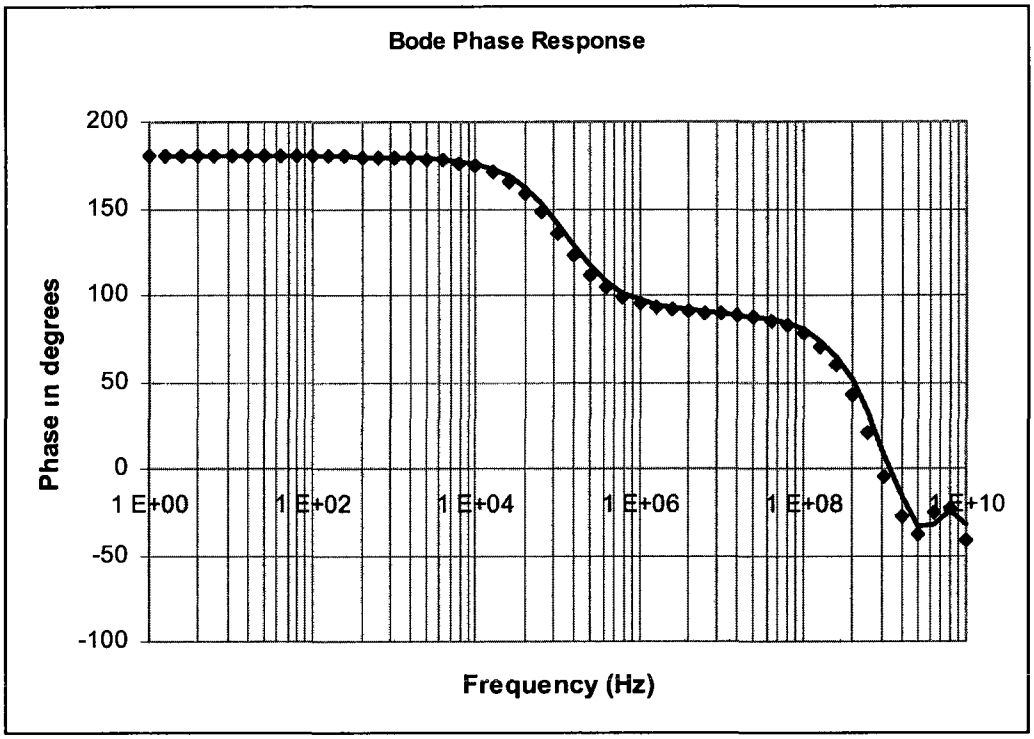


Figure 5 4 Bode plot for Telescopic OpAmp in TSMC025 design

The bode plots showing the magnitude response and the phase response of the telescopic OpAmp for TSMC025μ technology are shown in Figure 5 4 It can be seen that the UGF of the OpAmp is approximately 230 M Hz, while the Phase Margin, defined as the Phase at UGF is approximately equal to 60 degrees

5.2.2. AMI016μ Technology

Table 5 13 shows the final monomial model obtained by fitting the AMI016μ technology simulation data for the DC Gain (Av), Gain Bandwidth Product (GBW), and the Phase Margin (PM) The coefficients of the monomials are also provided along with the powers of the different independent variables in the monomial Both the GBW and PM exhibit dependence similar to that expected from the first-order model However, this monomial model is more accurate than the first order model because the higher order effects are captured from the simulations

TABLE 5 13 Telescopic OpAmp Monomial Model Fitted From Simulations (AMI016)

Design Variable	Power of the Design Variable			Units
	Av	GBW	PM	
L1	0 097	0 028	-0 081	μM
L3	0 074	-0 063	-0 112	μM
L5	-0 311	-0 096	-0 283	μM
L9	0 006	0 015	0 001	μM
W1	-0 006	0 097	-0 255	μM
W3	-0 002	0 121	-0 104	μM
W5	0 194	0 006	0 058	μM
W9	-0 312	0 682	-0 156	μM
Ibias	-0 237	0 397	-0 144	A /μM
Coefficient	Exp(2 599)	Exp(15 57)	Exp(2 499)	

Table 5 14 below shows the design for AMI016μ technology obtained from the Geometric optimization It can be observed that final design point is within ±10% of the initial first order design This is achieved by imposing additional constraints in mosek that restrict the design variables within acceptable proximity of the first order design

TABLE 5 14 Design Of Telescopic OpAmp For AMI016

Design Variable	First Order Design	Final Design	Units
L1	0 32	0 32	µM
L3	0 32	0 32	µM
L5	0 32	0 32	µM
L9	0 32	0 32	µM
W1	658 23	695 88	µM
W3	44 57	47 22	µM
W5	26 72	23 65	µM
W9	86 71	91 69	µM
Ibias	67 36	72 08	µA

The results of the spectre simulation on both the initial first order design and the final design for AMI016µ technology are shown in Table 5 15 below

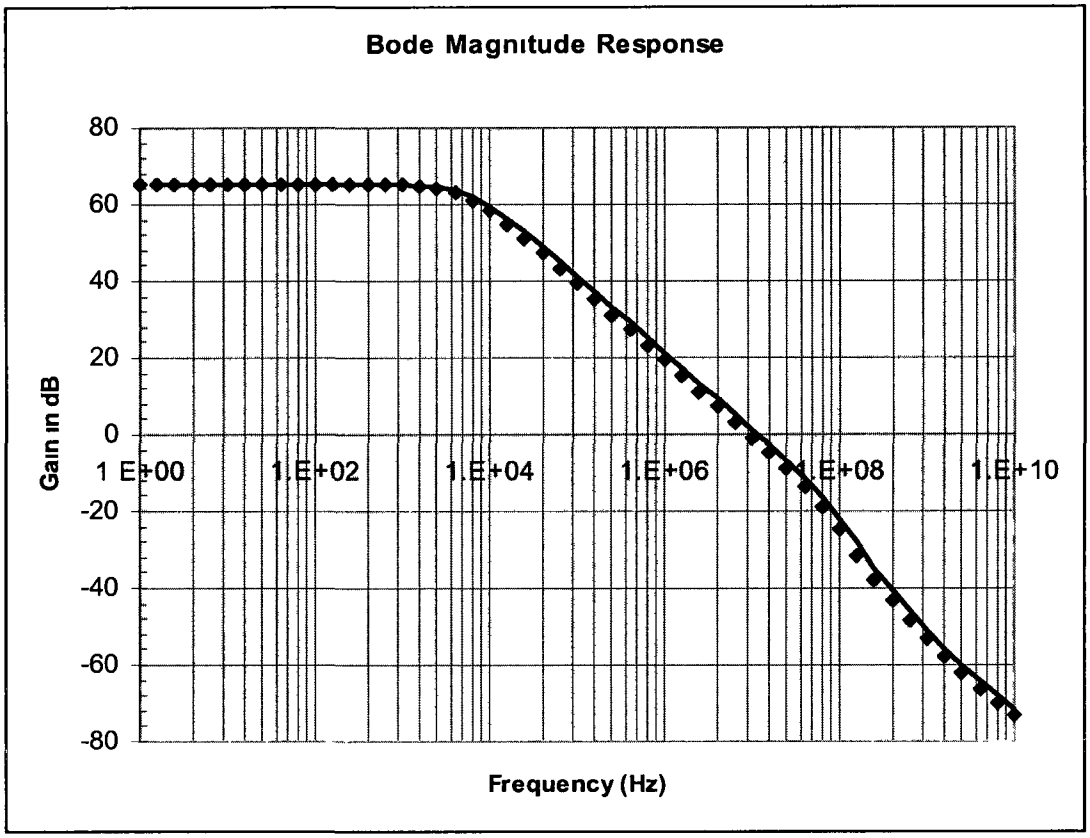
TABLE 5 15 Performance Of Telescopic OpAmp In AMI016

Performance	Specs	First Order Design	Final Design	Units
Av	--	66 41	65 183	dB
PM	≥ 60	69 85	60	degree
GBW	Maximize	8 62	9 831	M Hz

Table 5 16 below shows the performance of the monomial model in estimating the various performance constraints For the 256 simulations performed, 183 simulations yielded feasible DC solutions The percentage values of the maximum absolute error and the mean absolute error between the BSIM data and the monomial predicted values are shown in Table 5 16 It can be seen that the percentage mean absolute error is below 5% for all the three performance constraints considered here

TABLE 5 16 Performance Of The Monomial Model (AMI016) of Telescopic OpAmp

Design Constraint	Mean Absolute Error (%)	Maximum Absolute Error %
Av	4 3	19 6
GBW	1 1	16 4
PM	0 92	3 1



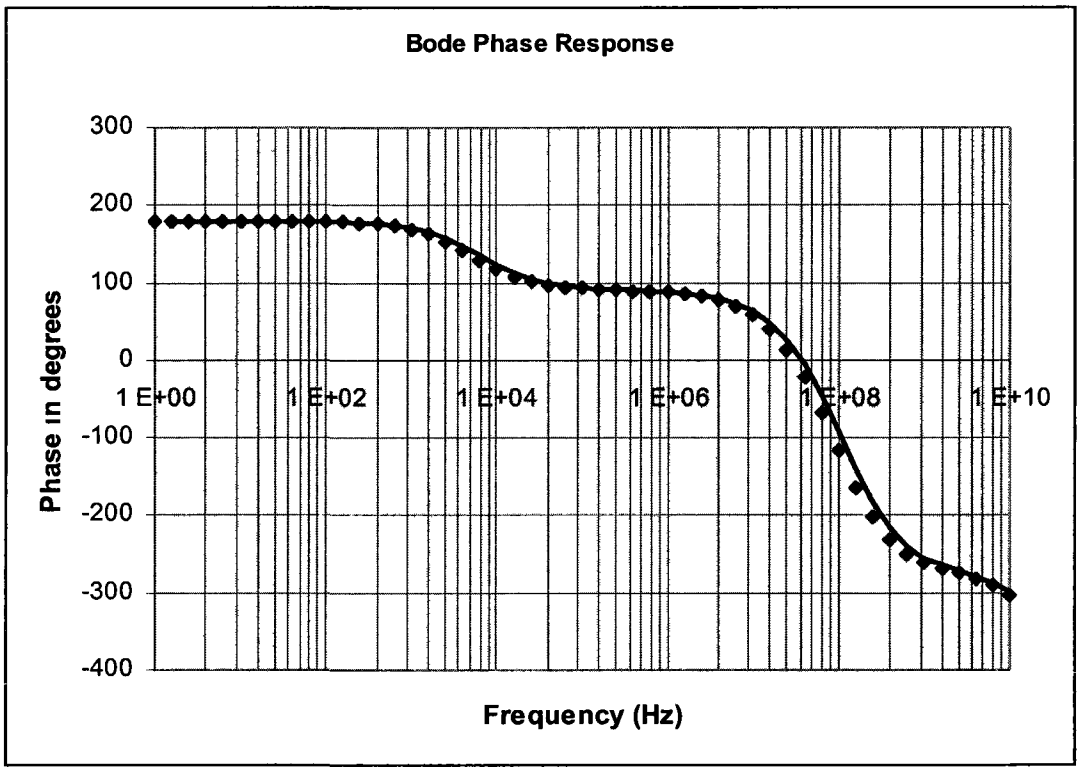


Figure 5 5 Bode plot for Telescopic OpAmp in AMI016 design

The bode plots showing the magnitude response and the phase response of the Telescopic OpAmp for AMI016μ technology are shown in Figure 5 5 It can be seen that the UGF of the OpAmp is approximately 9 M Hz, while the Phase Margin, defined as the Phase at UGF is approximately equal to 60 degrees

5.3. Summary

In this chapter, a novel methodology for automatic transistor-level sizing of OpAmps was proposed The methodology has the advantage of quick design time and still preserves the accuracy of BSIM models used for simulation The approach relies on generating simple but accurate monomial models that characterize the various design constraints The ease of generation of these monomial models alleviates the overhead of generating elaborate posynomials models Our results show that these models accurately predict the performance of the circuit in the proximity of the initial guess The models can also be used to gain valuable insight into the behavior of the circuit and understand the interrelations between the different performance constraints [100] As the methodology is simple and accurate, it can be used for exploring the performance space [98, 101-105] of Operational Amplifiers and identifying the boundaries on different performance metrics The methodology has been validated by designing a Two-Stage OpAmp and a Telescopic OpAmp in TSMC025μ and AMI016μ technologies Our results show an improvement of up to 15% over the first order design The methodology can be improved for speed by incorporating parallelization of the simulations

CHAPTER 6. CONCLUSIONS AND FUTURE WORKS

In this chapter, we summarize the work done so far and discuss some future directions

6.1. Summary

The work done so far addresses the problem of increasing the level of automation in analog design flow A design platform that automatically sets up the design equations and uses a hybrid of equation based and simulation based schemes is presented The platform is ideal for designing various OpAmp topologies across different technologies

The efficacy of the framework has been demonstrated by automatically designing different OpAmp topologies across different technologies We designed a two-stage OpAmp and a telescopic OpAmp in TSMC025 and AMI016 technologies Our results show significant (10 – 15%) improvement in the performance of both the OpAmps in both the technologies While the methodology has shown encouraging results in the sub-micrometer regime, the effectiveness of the tool has to be investigated in the deep-sub-micron technologies

In contrast to the existing approaches of the equation-based approach, we do not compromise with the performance accuracy to reduce design time Instead, the same high accuracy device models as those in a standard circuit simulator are used However, the increased accuracy is not gained at the expense of large design time By adopting a "localized simulation" strategy, we reduce the design time to lower than that taken for a simulation-based scheme

The first version of the design framework is designed to accommodate the use of various tools and algorithms, without much emphasis on the efficiency The framework can be modified to increase parallelization of simulations to increase the efficiency and reduce the design time

Further, the quality of the solutions reported by the design tool is high Experimental results show that the framework can produce circuits with performance at least 10% – 15% higher than the manual design methodology

The execution time for relatively large circuits is reasonable (For the two-stage OpAmp, approximately 120 minutes, on Sun Sparcv9 processor operating at 1 5 GHz speed, running on Solaris platform), although the framework is not implemented to parallelize the simulations on a farm of workstations Short execution times enables the possibility of exploring the design space and finding possible trade-offs in analog circuit design

6.2. Future Works

It is clear that much work remains in the field of analog design automation Our aim is to improve and extend the design framework to incorporate a larger portion of the analog design flow We briefly outline the possibilities and future directions in the following sections, while presenting the work currently under progress

6.2.1. Design of Supercircuit of OpAmps

We present the Supercircuit of OpAmps and the initial work done in the design of this circuit in this section

In the class of two-stage OpAmps, there is a basic structural similarity, in that the hierarchical structure of different configurations is the same It is only the sub circuits (the leaf cells of the hierarchy) that are different across the various topologies [59]

A two-stage OpAmp consists of an input stage, a second stage, and a compensating circuit The input stage has three parts current source, differential pair, and current mirror The

second stage has two parts transconductance amplifier and active load Each one of the four sub-circuits, namely differential pair, current mirror, transconductance amplifier, and active load, can be either simple or cascoded For a cascoded current mirror, a level shifter is required between the input stage and the second stage [59] The compensating circuit consists of a capacitor and a resistor Further, the transistors in the differential pair can either be n-type or p-type The choice of polarity of the transistors in the differential pair also determines the polarity of the transistors in the other sub-circuits With n-type differential pair transistors, the Supercircuit of the considered set of OpAmps [18] is given in Figure 5 So, from the Supercircuit, all other topologies can be constructed by selectively including/excluding the enclosed sub-circuits [59]

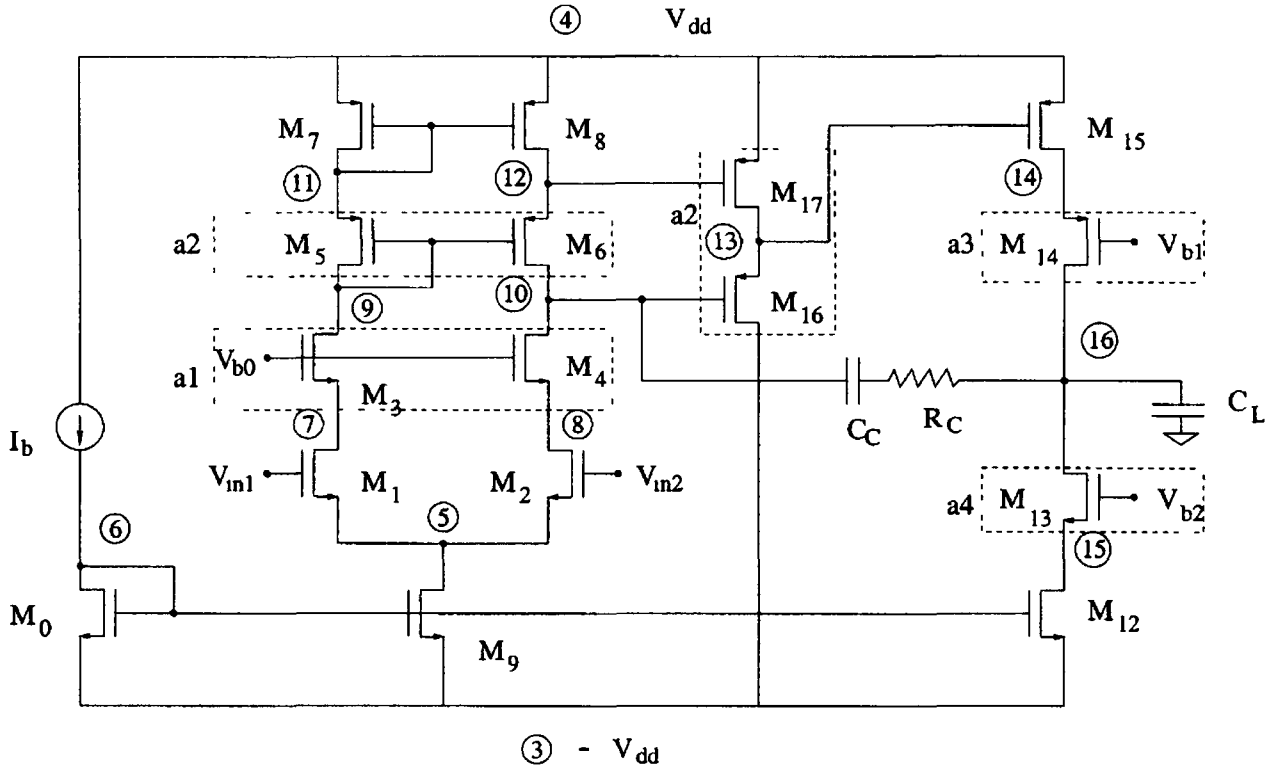


Figure 6 1 Supercircuit of CMOS OpAmps

As can be seen from Figure 6 1, the external bias voltages Vb0, Vb1 and Vb2 have to be critically designed for the proper biasing of the OpAmp itself The proper biasing of these external biases is critical for the overall performance of the OpAmp Furthermore, any change in the design of the device dimensions have to be reflected meticulously as changes in these bias voltages In other words, once the initial design is arrived at and the bias values chosen for Vb0 – Vb2, any subsequent changes in the device dimensions have to be compensated by proper re-design of the bias voltages This poses a significant problem for using this design in an automated environment Specifically, the use of DOE mandates that the device dimensions be varied around the initial design This calls for a tedious redesign of the bias voltages In order to eliminate this difficulty, we implemented a self-bias scheme [106, 107] This self bias scheme not only reduces the number of external bias voltages required for proper biasing, but it also decreases the sensitivity of the OpAmp bias point to any changes in the device dimensions Figure 6 2 shows the self-biased Supercircuit [106]

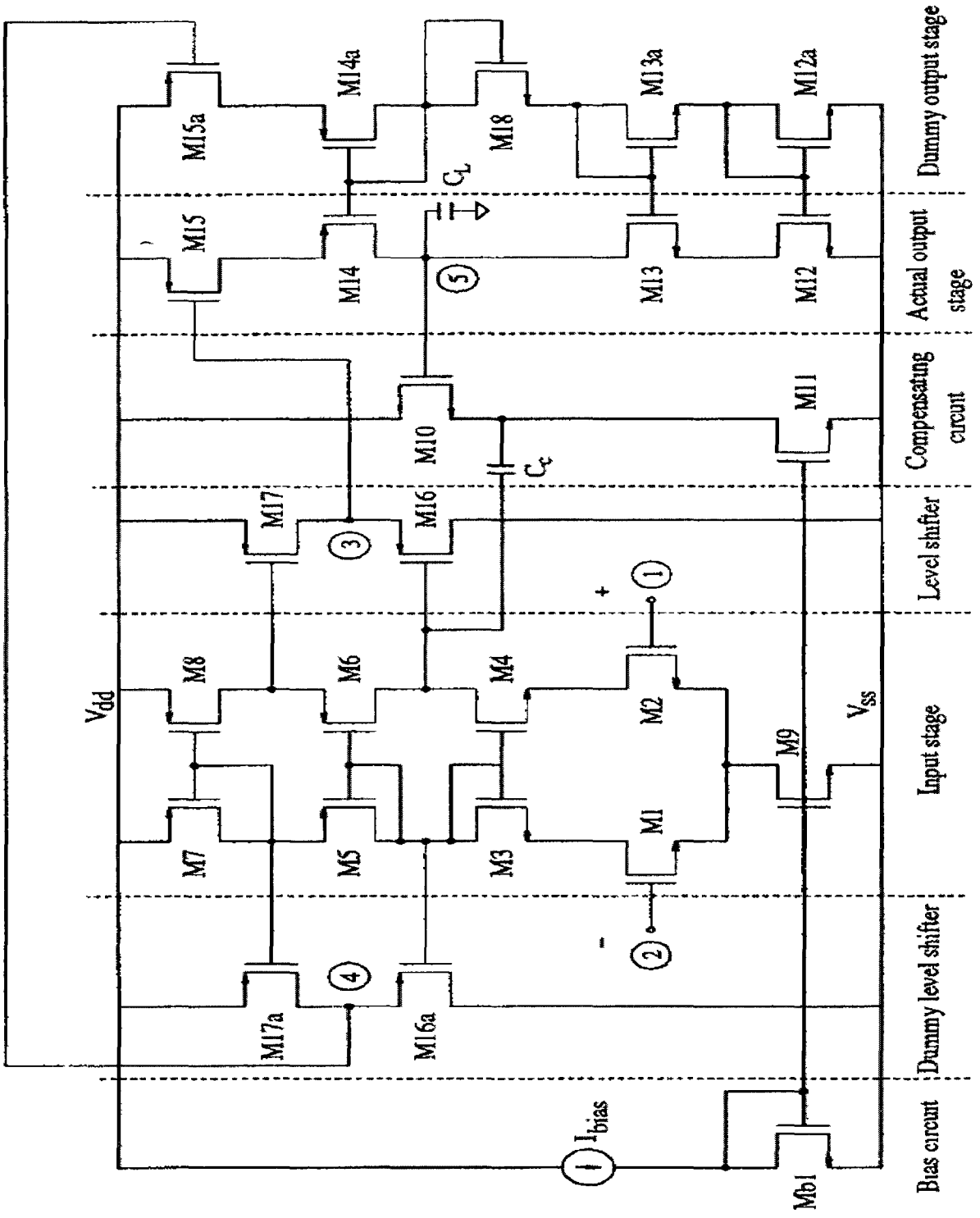


Figure 6 2 Self-biased Supercircuit [106]

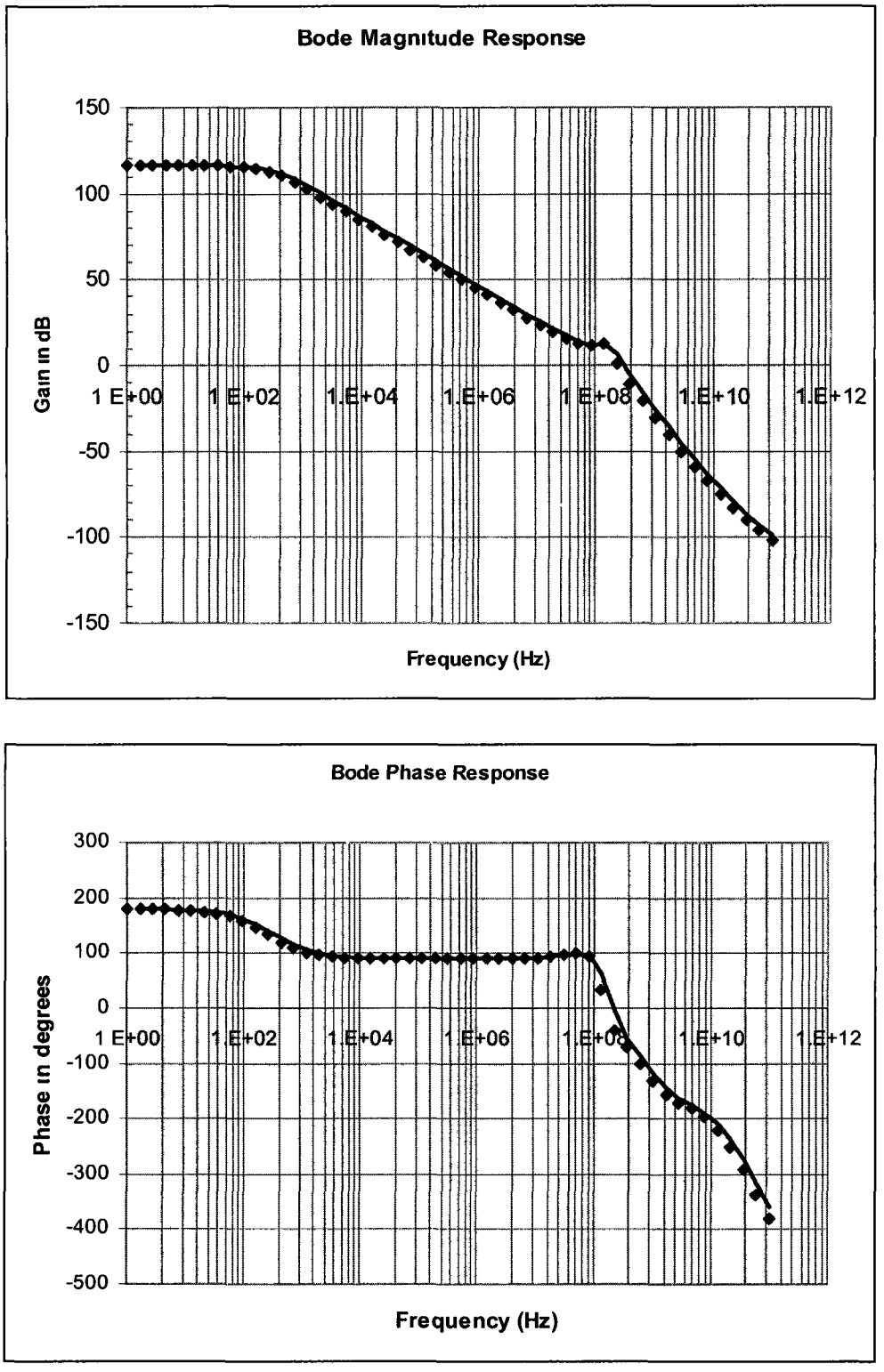


Figure 6 3 Bode Plots of the Supercircuit in TSMC025 showing effect of the Complex Pole

The first order design of this OpAmp suffers from a complex pole in the vicinity of the Gain Bandwidth Product The complex pole adversely affects the Phase margin of the OpAmp, thereby, jeopardizing the stability of the OpAmp The Magnitude and the Phase response of the Supercircuit are shown in the Figures 6 3 and 6 4

In order to mitigate the effect of the Complex Pole, several schemes like the Nested Miller Compensation Scheme [108-111] have been proposed The basic idea behind this approach is to counteract the effect of the Complex zero by introducing RHP Zeros into the proximity of the complex pole This negates the degradation of Phase margin by the Complex Pole However, the implementation of this compensation scheme is beyond the scope of this dissertation and could be a good extension to the work presented here

Another approach to improve the frequency response of the Supercircuit is to model the poles as monomials of design variables In our approach, we presented a scheme to automatically model the different performance constraints as monomials of design variables The same approach can be extended to model the poles (and zeros) as monomials in design variables The idea is that, by including monomials of the poles as constraints in the design problem, the different design variables can be chosen to selectively place the poles at convenient locations This could be a more straightforward approach to understanding and controling the pole location because the monomials relate the pole (and zero) behavior to design variables This method can result in superior control of the pole/zero location than the approximate symbolic expressions approach[112]

6.2.2. Posynomial Generation Scheme

In this work, we demonstrated that the use of monomials to model the performance constraints can be have several advantages like (i) ease of modeling and (ii) compatibility with Geometric Programming However, we did not focus our attention on increasing the accuracy of the models Experimental results show that the errors introduced by the monomial generation scheme can range from as low as 1% to as high as 22% The errors introduced by the monomial models can be explained from the fact that these models, although a good approximation in the vicinity of the initial design, cannot predict the performance of the different constraints over the entire design space A good alternative is to use posynomials to model the performance metrics The advantage is that the posynomials can be a better fit than the monomial models, while still being compatible with Geometric Optimization scheme

Efforts have been made [16], [57, 71, 113-115] to formulate a posynomial generation scheme Two approaches to model posynomials stand out in literature - (i) the Direct Fitting approach and (ii) the Indirect Fitting approach

The Direct Fitting approach relies on using a posynomial template The different powers and coefficients of the posynomial terms are evaluated by using a regression scheme that uses a least-squares approach On the other hand, the indirect posynomial fitting scheme first generates a polynomial to fit the performance constraints Then an approximate posynomial is generated from the polynomial model

As can be seen, generation of posynomials is a more tedious and time taking task than the simple monomial modeling scheme presented in our approach Further investigation is needed to compare the performance of posynomial models to that of the monomial models

6.2.3. Topology Selection and Parasitic Aware design

The automated device sizing is the part of the work where most of our efforts have been made So far, we addressed the problem of designing the device sizes for a given topology Moreover, the design methodology does not address the issue of incorporating the layout parasitics into the design flow Layout induced performance degradation is becoming more important as the technology scales The automatic topology selection and parasitic–aware design [116] are important steps of the analog design flow and our frame work can be extended to incorporate these stages of the analog design flow, thereby solving the next generation of automation challenges outlined in [117-119]

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