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High-Performance Bus-Based Architectures - Guest Editorial

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Guest Editorial

STEPHAN OLARIU and RONG LIN

This special issue of **VLSI Design** presents a collection of seven papers selected out of more than 35 submissions received following the Call for Papers. Each submission was sent to three referees, all of them experts in the area of bus-based architectures. The result is impressive. The papers featured in this Special Issue cover a wide range of topics from sorting to string matching, to load balancing, to simulation, matrix operations, to robotics, to the design of high-performance scalable architectures.

Before we summarize the papers of this issue we would like to thank all the referees for their thorough reviewing job and all the authors for submitting their manuscripts to the Special Issue. Last but certainly not least, our thanks go to Professor Zobrist for all the help and advice provided during the various stages of this undertaking.

We now turn to the task of introducing briefly the papers of this issue.

In the work "Sorting on Reconfigurable Meshes: An Irregular Decomposition Approach", Lai and Sheng demonstrate that dividing a problem evenly is not necessarily a good way to partition. There are occasions where an irregular partitioning is preferable. They go on to apply this approach to sorting on the reconfigurable mesh, obtaining a sorting algorithm that is simple, scalable, and as broadcast-efficient as the best known result.

In the paper "Single Step Undirected Reconfigurable Networks", Ben-Asher and Schuster show that for the reconfigurable mesh the constant involved in a number of $O(1)$ time algorithms can always be reduced to 1, still using a polynomial number of processors. Given a reconfigurable mesh that computes a set of values in $O(1)$ time, they show that it can be simulated by a single-step reconfigurable mesh whose size is polynomial in the size of the original mesh.

In the paper "Investigation of various mesh Architectures with Broadcast Buses for High-Performance Computing" Ziavras carries out an extensive comparative analysis between various mesh-connected architectures that contain sparse broadcast buses for low-cost high-performance parallel computing. Shared memory and Reconfigurable Mesh", Matias and Schuster look at relations between the PRAM model and the reconfigurable mesh providing mutual simulations between these models.

In the paper "Partitionable Bus-Based String Matching Algorithm for Run-Length Coded Strings with VLDCs, Chen and Chung present an efficient parallel string matching algorithm. For run-length coded strings with variable length don't cares. Given a run-length coded text of length $2n$ aver Σ and a run-length coded pattern of length $2m$, their algorithm runs in $O(1)$ time on a reconfigurable mesh of $O(mn)$ processors. In order to be suitable for VLSI modular implementation a

partitionable parallel algorithm on the reconfigurable mesh is further presented.

In the paper "Multiplication of Matrices with Different Sparseness Properties on Dynamically Reconfigurable Meshes", Middendorf *et al.*, present algorithm for multiplying several types of sparse matrices of size $n \times n$ on dynamically reconfigurable arrays of the same size. Among other results, they obtain $O(kn^{1/2})$ algorithms for the case that one matrix is a general sparse matrix with at most kn nonzero elements and the other matrix has at most k nonzero elements in every row or every column.

In the paper "Reconfigurable Shift Switching Parallel Comparators", Lin and Olariu present novel asynchronous VLSI comparator schemes based on the recently proposed reconfigurable shift switching logic and the traditional precharged CMOS domino logic. The proposed schemes always produce a semaphore as a byproduct of the process to indicate the end of the domino process, which requires no additional delay and a minimal number of additional devices.

Finally, in the work "Finding Combined L_1 and Link Metric Shortest paths in the Presence of Orthogonal Obstacles: A Heuristic Approach", Lim *et al.*, present new heuristics search algorithms for searching combined rectilinear and link metric shortest paths in the presence of rectilinear obstacles. Their algorithms combine the best features of maze-running algorithms and line-search algorithms.

We trust you will be as stimulated as we are by the enclosed contributions.

Guest Editors' Biographies

Stephan Olariu received the M.Sc. and Ph.D. degrees in computer science from McGill University, Montreal in 1983 and 1986, respectively. In 1986 he joined the Computer Science Department at Old Dominion University where he is now a professor.

Dr. Olariu has published extensively in various journals and conference proceedings. His research interests include parallel algorithms, parallel algorithms, image processing and machine vision, computational graph theory, computational geometry, and mobile computing.

Rong Lin received the B.S. in mathematics from Peking university (China), M.S. in Computer Science from Beijing Polytechnical University (China) and Ph.D. in computer science from Old Dominion University in 1989. He is currently an associate professor with the Department of Computer Science of SUNY at Geneseo. His current research interests include VLSI arithmetic, parallel architectures and algorithms, digital signal processing, and reconfigurable architectures.