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Simulation, Measurement, and Emulation of Photovoltaic Modules Using High Frequency and High Power Density Power Electronic Circuits

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SIMULATION, MEASUREMENT, AND EMULATION OF PHOTOVOLTAIC MODULES USING HIGH FREQUENCY AND HIGH POWER DENSITY POWER ELECTRONIC CIRCUITS

by

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ABSTRACT

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Old Dominion University, 2016
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The number of solar photovoltaic (PV) installations is growing exponentially, and to improve the energy yield and the efficiency of PV systems, it is necessary to have correct methods for simulation, measurement, and emulation. PV systems can be simulated using PV models for different configurations and technologies of PV modules. Additionally, different environmental conditions of solar irradiance, temperature, and partial shading can be incorporated in the model to accurately simulate PV systems for any given condition.

The electrical measurement of PV systems both prior to and after making electrical connections is important for attaining high efficiency and reliability. Measuring PV modules using a current-voltage (I-V) curve tracer allows the installer to know whether the PV modules are 100% operational. The installed modules can be properly matched to maximize performance. Once installed, the whole system needs to be characterized similarly to detect mismatches, partial shading, or installation damage before energizing the system. This will prevent any reliability issues from the onset and ensure the system efficiency will remain high.

A capacitive load is implemented in making I-V curve measurements with the goal of minimizing the curve tracer volume and cost. Additionally, the increase of measurement resolution and accuracy is possible via the use of accurate voltage and current measurement methods and accurate PV models to translate the curves to standard testing conditions. A move

from mechanical relays to solid-state MOSFETs improved system reliability while significantly reducing device volume and costs.

Finally, emulating PV modules is necessary for testing electrical components of a PV system. PV emulation simplifies and standardizes the tests allowing for different irradiance, temperature and partial shading levels to be easily tested. Proper emulation of PV modules requires an accurate and mathematically simple PV model that incorporates all known system variables so that any PV module can be emulated as the design requires.

A non-synchronous buck converter is proposed for the emulation of a single, high-power PV module using traditional silicon devices. With the proof-of-concept working and improvements in efficiency, power density and steady-state errors made, dynamic tests were performed using an inverter connected to the PV emulator. In order to improve the dynamic characteristics, a synchronous buck converter topology is proposed along with the use of advanced GaNFET devices which resulted in very high power efficiency and improved dynamic response characteristics when emulating PV modules.

This thesis is dedicated to my family
who span the corners of the world.

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CHAPTER 1

INTRODUCTION

1.1. Introduction

There is significant growth in the photovoltaic (PV) market, thanks to the wide availability of low-cost PV modules, good federal and state incentives such as tax credits and feed-in tariffs in the United States [1-4]. With increased numbers in commercial and residential deployments, it becomes important to properly model, measure, characterize, and emulate photovoltaic modules to better utilize PV technology [5-6].

PV models are important to understand and simulate the behavior of PV modules under different conditions and configurations [7]. Such conditions relate to different amounts of sunlight (irradiance), the varying outdoor temperatures and the amount of partial shading (when a section of the PV module receives less light than others) [8-10]. Internal configurations of PV modules include the number of solar cells connected in either series or parallel combinations, and the type of the material i.e. Silicon (Si), Copper Indium Gallium Selenide (CIGS), Cadmium Telluride (CdTe) or Gallium Arsenide (GaAs) [11-15]. External configurations include the number of PV modules in a "string" (a series chain of PV modules) and the number of strings connected together in parallel via a junction box [16].

Measurements of a PV system typically include the open-circuit voltage V_{oc}, short-circuit current I_{sc}, voltage, current and power at the maximum power point V_{mpp}, I_{mpp}, P_{mpp}, respectively [17]. These measurements, while perfectly representative of PV modules in ideal laboratory conditions and operation at the maximum power point (MPP), fail to properly characterize the PV system throughout its operational region [18].

As one can imagine, testing PV modules requires them to be under sunlight. PV module manufacturers use devices known as solar simulators to shine a calibrated amount of light on the PV module under test, and bin the modules according to power output and provide certain operational parameters in the module datasheets [19-20]. While it is straightforward to test and characterize PV modules under standard testing conditions (1000W/m^2 irradiance and 25°C ambient temperature), the same testing methods cannot be applied to systems connected to PV modules, such as inverters, protection devices, measurement devices, and cabling and junction boxes [21-25].

In order to test the external electrical hardware "PV electronics" used in PV systems, the tests need to cover all expected operational conditions. The goal of designing PV electronics is to have them work under varying conditions of sunlight, temperature, and partial shading. For fully testing the capabilities and guaranteeing the robustness of PV electronics, the use of actual PV modules is undesirable. Testing high power PV equipment would require enormous and costly testing facilities [26]. Besides costs, problems arise from inconsistent and difficult to predict fluctuating conditions of solar irradiation and ambient temperature [27].

PV module emulators are designed to emulate the output of actual photovoltaic modules using electrical circuits [28-31]. In order to do so, an accurate PV module model is necessary to generate the output curve that correctly represents a PV module [32-35]. Afterwards, the simulated I-V characteristics are input into the electrical circuit control algorithm to control the output of the emulator resulting in an accurate representation of PV module characteristics. The use of PV module emulators provides the flexibility and cost effectiveness required to test all kinds of PV equipment.

1.2. Overview of I-V curve Tracers

I-V curves of photovoltaic strings provide relevant information that ordinary monitoring systems at the inverter level and fault detection systems at combiner level cannot measure. Information about partial shading, PV module mismatch, effects of solar insolation and temperature, shunt resistance, and series resistance can be gathered from the analysis of a typical I-V curve [36-44].

Many topologies are described in the literature regarding I-V curve measurement circuits [45-46]. The main ones in concern can be listed as: variable resistor load, capacitive load, electronic load, four quadrant power supply, and DC-DC converter. Ultimately, the goal of all of these topologies is the same: to measure the I-V curve accurately. The requirements for an I-V curve tracer can be listed as [47]:

1. Flexibility,
2. Modularity,
3. Fidelity,
4. Fast response: all points recorded at same climatic conditions,
5. Direct display: test results are displayed while running, and
6. Cost

Considering the criteria above, all topologies listed have their benefits and drawbacks. Table 1.1 presents a summary of the most common I-V curve tracer topologies.

Table 1.1: Capabilities of different curve tracer topologies based on [47].

	Flexibility	Modularity	Fidelity	Response	Display	Cost
Variable Resistor	Medium	Medium	Medium	Low	No	Low
Capacitive Load	Low	Low	Medium	Low	No	High
Electronic Load	High	High	Medium	Medium	Yes	High
4-quadrant PSU	Low	Low	High	High	Yes	High
DC-DC Converter	High	High	High	High	Yes	Low

1.2.1. Variable Resistive Load

The simplest and most intuitive way of measuring the I-V curve of a photovoltaic module or array is to use a variable resistive load. The operational point of the module can be varied by altering the value of the load resistance. Two distinct load topologies are possible: a switched load bank that changes the load resistance via automated relays, or a simple rheostat (variable resistance) that can be swept from nearly 0 to a large enough value.

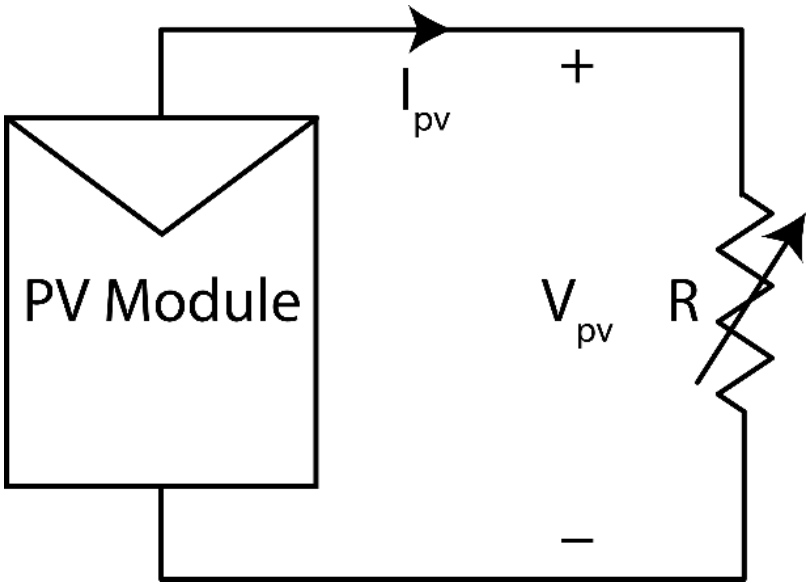

Figure 1.1. Variable resistive load based on [47].

The power consumed by the resistors turns into heat and may destroy the resistors in question. Coupled with the fact that it is difficult to get large power resistors, this circuit topology is only suitable for low power modules and not large power arrays. The measurements tend to be very slow if manually operated and this may lead to the conditions to change during measurements.

Willoughby *et al*. present a simple resistive load to monitor the I-V characteristics of PV modules [48]. Their methodology consists of a 10 minute interval timer that triggers measurements. The counter connected to the timer energizes a sequence of relays connected to high power resistive loads of 0.1Ω to about 100Ω. The circuit is an analog design and while claimed to be cost effective due to the low-cost low voltage relays, the authors suggest the use of a single microcontroller to eliminate the timer and counter circuit, and the use of MOSFETs over relays to reduce the relay bouncing effect. The maximum electrical values tested were just below 22V, 3A, and 45W.

Rivai and Rahim investigated a binary-based I-V curve tracer [49]. When compared to a traditional curve tracer with different load resistance values, their resistor selection is optimized to trace many points with the use of only 8 resistors. The circuit is based on a binary counting system with resistors values ranging from 1Ω to 128Ω in powers of 2, and through switching the resistors in and out, it is possible for them to change the load resistance from 1Ω to 255Ω in 1Ω increments.

1.2.3. Capacitive Load

A capacitor is used to bias the module under test in this topology. When *S1* is closed in Figure 1.2, the capacitor begins charging. Assuming the capacitor is fully discharged, the initial capacitor voltage will equal to zero. As the capacitor initiates charging, the I-V curve

relationship will be constrained by the PV module and, thus, a highly accurate measurement is made possible.

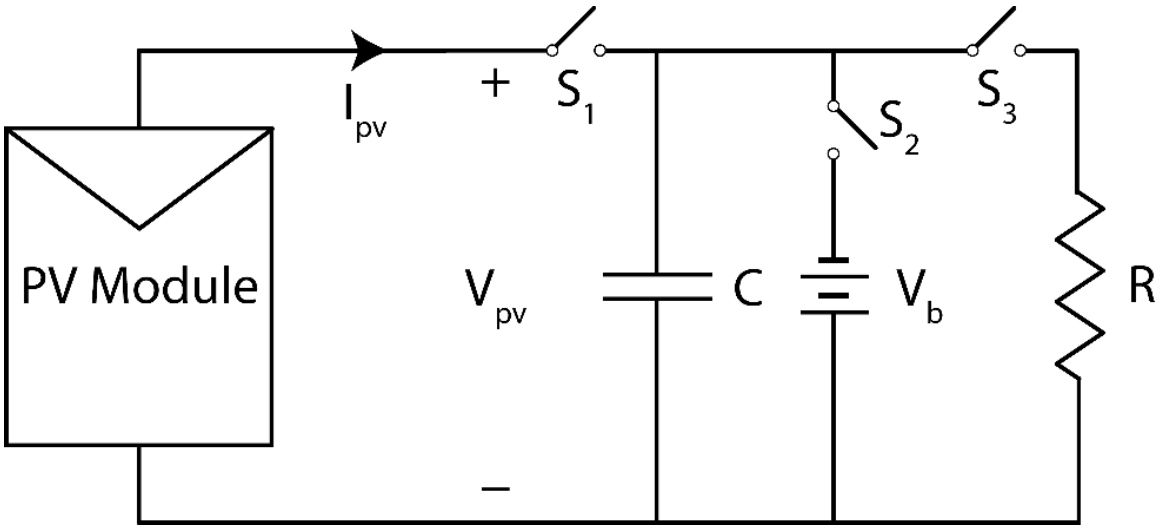

Figure 1.2. Capacitive load based on [47].

Typical requirements are good quality capacitors with low equivalent series resistor (ESR) values to keep the capacitors from overheating. Since the energy stored in the capacitor is in the form of reactive power, it leads to no heat related issues. Varying the size of the capacitor will vary the stored energy but, generally speaking, there is very little energy transferred to the circuit when compared to other forms of measurement.

The capacitor can also be pre-charged with a reverse voltage (negatively biased) by closing *S2* before the measurement takes place. This is an important factor for the measurement of the true-short circuit current, otherwise there will be an absolute minimum measurable voltage that will be greater than zero. This inhibits the measurement of the true short-circuit current.

Finally, the capacitor is discharged via *S3* and the capacitor energy is dissipated within the resistor bank. Resistor values above 10W generally yield good thermal characteristics without temperature issues.

The capacitor size is highly dependent on the conditions, which makes this circuit a challenge to accommodate for all circumstances. The capacitor size is directly proportional with I_{sc} and indirectly proportional with V_{oc}. That is, a large system consisting of photovoltaic modules in a series array will need a much smaller capacitor than a single module or modules connected in parallel. The capacitor size is still quite important as it should allow for fast enough measurements for the climatic conditions to remain constant and it should be slow enough to overcome the junction capacitance of the modules.

Munoz *et al*. propose a capacitive load with insulated gate bipolar transistors (IGBTs) used as switches for the purposes of tracing the I-V curves of photovoltaic modules connected in a combinational series/parallel array in [50]. The circuit consists of three switches, which serve various functions. The first switch is connected to a shorting diode which allows for making short-circuit current measurements near zero volts. Due to the high system voltage and the high short-circuit current, the diode used is very large and has a large voltage drop, leading to increased losses. Therefore, the authors recommended that a very quick pulse test should be used to confirm the short-circuit current.

The second switch connects the PV modules to the capacitor bank comprised of four capacitors, which can be connected all in parallel or in two-series and two-parallel for doubling the open-circuit voltage capability. The voltage across the capacitors is balanced by two balancing resistors.

A pushbutton located on the panel allows for negatively charging the capacitor bank using a 9V battery before measurements are made to capture the module current at zero volts. The third switch is used for discharging the capacitor bank after measurements are performed through a discharge resistor and blocking diode.

The voltage and current values are measured through a voltage divider and series connected shunt resistor respectively, and there is no data logging capability in the device. Therefore, the aid of an oscilloscope for data acquisition is necessary.

The paper discuss the complex switching and gate drive arrangement, which are part of the largest drawbacks of this design. The gate driver circuit is a complex system consisting of 9V batteries, a DC capacitor, manual trigger pushbuttons, optocouplers, gate resistors, and large package chassis mount IGBTs costing hundreds of dollars.

A human operator is necessary to charge, discharge, and negatively bias the capacitor and no automation is possible. The lack of data storage is also a huge problem. Because the operator comes in contact with the device, the operator is at risk of electrical shock. Other drawbacks include bulky and heavy components weighing a total of 15kg and a high cost over $1000. The oscilloscope used to capture the data costs about $2200.

The authors' results show that there is measurement noise coupled into the system, but it performs an adequate sweep from what appears to be 0V to the short-circuit current. The algorithm used to extrapolate to STC appears to be highly questionable due to the wide gap it introduces between I_{sc} and the measured lowest voltage.

1.2.4. Electronic Load

The electronic load topology is a practical and simple method of measurement. Most products sold in the market titled "DC electronic load" work using this operational principle. In

the simplest sense, a transistor will be operated in its cut-off, active and ohmic regions by modulating the gate voltage to vary its resistance. This makes the transistor act like a variable resistor, which is very easy to construct.

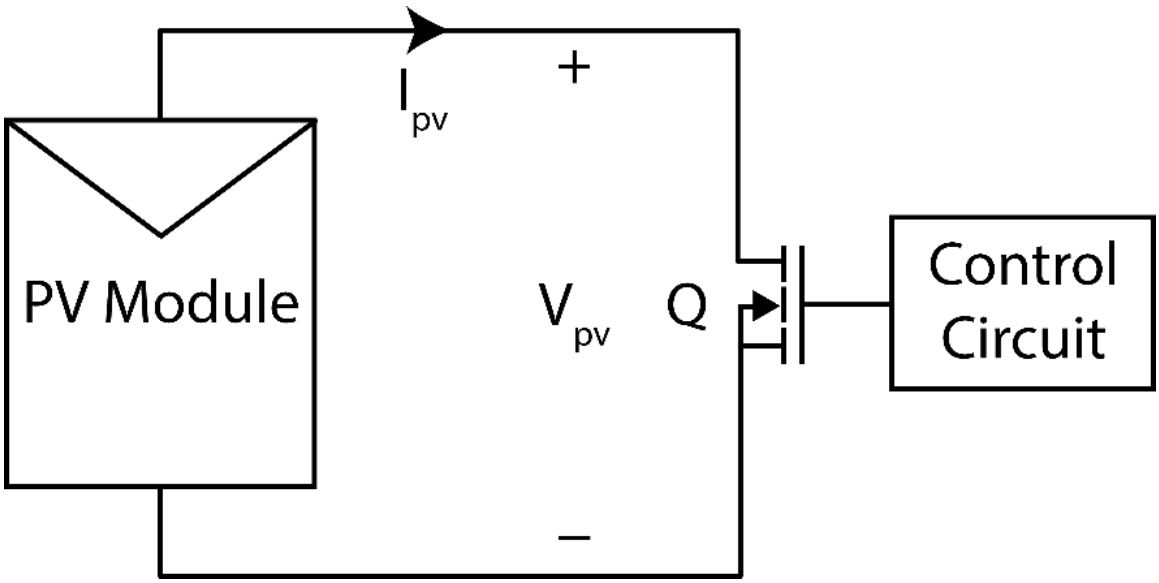

Figure 1.3. Electronic load based on [47].

The main challenge of this circuit comes from the fact that the transistor dissipates all the power and large heat sinks and many parallel MOSFETs are required to build a large enough device to carry out measurements for larger systems.

Although technology has vastly improved MOSFETs high frequency capabilities and figures of merit through the reduction of the gate charge and series resistances, the reduced cell areas in the MOSFET structure cause an imbalance of current [51]. During fully-on operation (ohmic region), there certainly is no problem as the resistances are small and similar to each other. But in the saturation region the resistances will be significantly larger than the minimum

resistances possible and this will cause current localization and regions with smaller resistances [52]. With increased temperatures the resistances of the regions will further drop and will cause premature failure [53]. Therefore, older generation devices with larger cells and devices designed especially for linear use are required in the design of an electronic load.

1.2.5. Four Quadrant Power Supply

The four quadrant power supply requires a large power supply which is usually limited to a maximum power of 1 kW to both source and sink current from the PV module under test. This method is the only way of making a 3 quadrant measurement on a photovoltaic module. However, with the capability comes the tremendous costs and difficult switching schemes. The low power limit of this load (mainly from sinking power) disallows large array testing and it is only useful for single module testing.

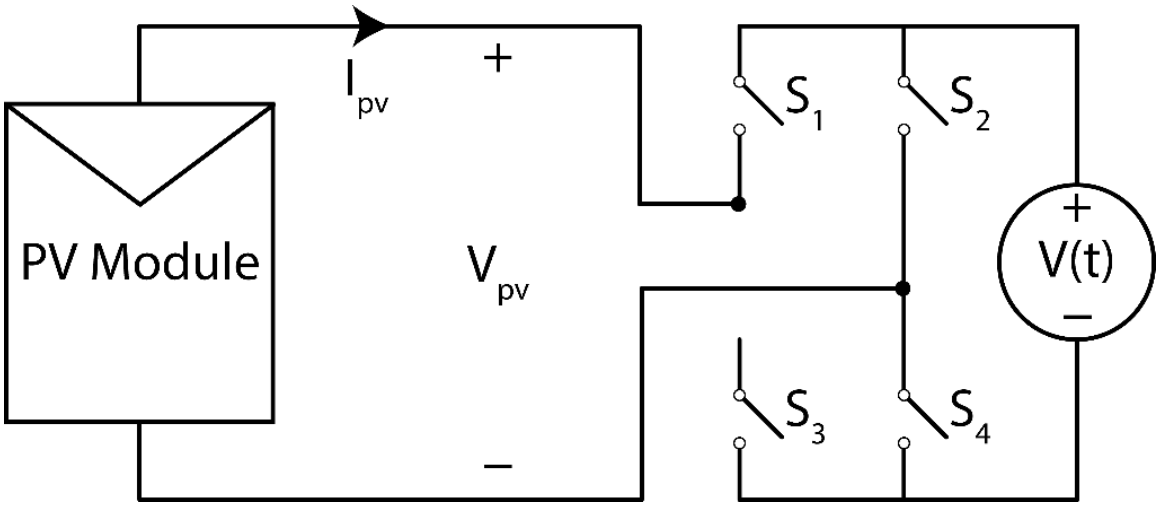

Figure 1.4: Four quadrant power supply based on [47].

1.2.6. DC-DC Converter

The DC-DC converter shown in Figure 1.5 is a device connected between the PV module and a resistive load that allows for a variable resistor, variable current, and a variable power load to be constructed. The main power electronics topologies for this circuit consist of buck, buck-boost, and boost converters operating as DC transformers. The buck converter topology is incapable of emulating a resistive load below the physically connected resistor and therefore is incapable of tracing near I_{sc}. Conversely, the boost converter cannot emulate a load larger than the physical resistor and it is not capable of making measurements at or near V_{oc}. The buck-boost converter, on the other hand, is capable of resolving the whole curve. Two other exotic converters such as SEPIC and Ćuk converters are good for reduced ripple in the reproduced curves. The current ripple and voltage ripple caused by the switching action reduce the quality of the measured curve and large passive filters are necessary to eliminate noise in the measurements. This method can take single quadrant measurements only.

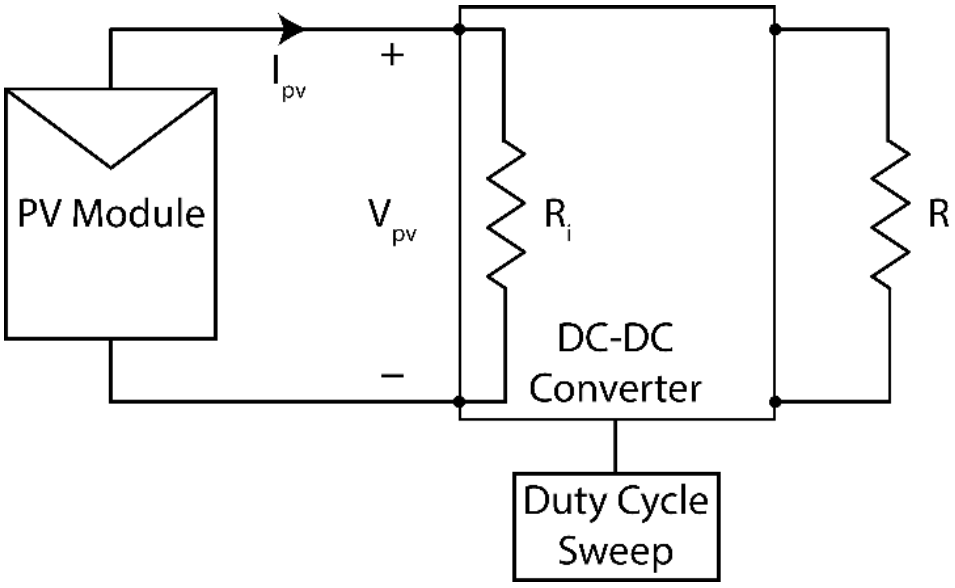

Figure 1.5: DC-DC converter based on [47].

1.2.7. Industrial I-V Curve Tracers

There are quite a few I-V curve tracers in the market, some of which operate with an electronic load topology, and others with capacitive load topologies. The portable devices are usually capacitive while rack-mount units designed for production testing with a solar simulator are DC electronic load type. Example of devices for portable measurements and their characteristics are given in the following paragraphs.

The MP-11 I-V Checker by Eko Instruments is a portable I-V curve tracer that relies on the capacitive load topology [54]. It is capable of taking voltage measurements in the range of 10-1000V and current measurements in the range of 0.1-30A with a power range of 10W-18kW. It is capable of recording 400 data points and storing 300 I-V curves in the internal memory. The device comes with a pyranometer, a reference cell, and two thermocouples for sensing irradiance and module temperature. The unit dimensions are 23 x 32 x 18 cm^3 with a total weight of 2.5kg for the tester, 0.5kg for the sensor unit, and 0.5kg for the battery box. Power is supplied by 8 x AA batteries or a 9V/1A DC adaptor. The sensor unit runs off a single 9V battery (006P type).

The TRI-KA I-V Curve Tracer from Tritec Energy [55] is capable of measuring 1.0-1000V and 0.1-15A PV systems. The unit includes a sensing unit that measures temperature and irradiance through a direct contact with the face of the PV module and the sensing unit, and a reference silicon cell, respectively. It is recommended to make I-V measurements above 700W/m^2 irradiance for reliable results per EN 61829 standards [56]. Data points are stored in an SD card, which provides over 1000 measurements per 1 GB. The unit weighs just 0.5kg with dimensions of 21 x 10.5 x 4.1 cm^3. The cost of the unit is $5,595 at Solar-PV-Tester.com

The DS-1000 I-V curve tracer from Daystar is a portable curve tracer weighing 12 kg and measuring 44 x 35 x 20 cm^3 [57]. Each measurement includes 1000 data points and requires a

computer to transfer the data. The unit includes two thermocouple inputs (Type T) and two analog voltage inputs that can be used to connected irradiance sensors. The device has 3 ranges of voltage (10, 100, 1000V) and current (1, 10, 100A).

The Solmetric PVA-1000S PV Analyzer Kit provides a portable solution to I-V curve measurements [58]. In its standard configuration it is capable of measurements of up to 1000V and 20A and for an additional $600 it can measure up to 30A. The voltage and current resolution are 25mV and 2mA, respectively. The minimum measurements points are 100 and the device uses an external sensor wirelessly connected to the main unit to acquire the irradiance and module temperature. A computer is needed to transmit and receive the data and the unit weighs 12 lb. with dimensions of 15 x 8 x 5 cubic inches. The sensor unit has an irradiance resolution of 1 W/m^2 and a measurement range of 0-1500W/m^2. The temperature resolution of the sensor unit is 0.1°C with a measurement range of 0-100°C. The sensor unit weights 2 lb. with dimensions of 14 x 4.5 x 3 cubic inches. The total cost of the PVA-1000S as indicated on the manufacturer website is $5,695 or $6,295 including the 30A capability.

1.2.8 Summary

There is limited development in the literature concerning I-V curve tracers. Most of the focus on I-V curves is the extraction of the PV module parameters using novel methods. The capacitive load topology has not been improved upon since it was first proposed in [59]. Most of the research of capacitive topologies is focusing on improving the high power characteristics as shown in [60]. There is a significant issue with size, weight and price when it comes to products both in the market and in literature. The main challenges that have to be overcome are the size and costs of the switches and also the complicated switching circuits need to be simplified.

1.3. Overview of PV Emulators

PV emulators come in different topologies but mostly rely on switching converters for power output capability. Since PV systems are connected to dynamic loads via inverters and maximum power point (MPPT) trackers, there is a lot of work being done to optimize the quality of the emulated output. When selecting or designing a PV emulator, the following attributes carry significant importance:

1. The PV emulator should be able to emulate any PV module as long as the outputs lie within the limits of the emulator output;
2. Emulate PV module outputs for different irradiance, temperature, and partial shading conditions;
3. Be portable;
4. Have high efficiency as to not require active cooling;
5. Have good dynamic response; and
6. Allow testing solar equipment such as inverters and maximum power point trackers.

1.3.1. Circuit Topologies

While generally constructed from switching circuits, it is possible to construct a low power PV module emulator using a linear regulator connected to a DC power supply [61-62]. This approach will give the purest and cleanest DC output of any topology while being extremely inefficient and suitable for only applications lower than 100W.

For high power applications, switching power supplies are preferred for their superior efficiency values. There are two main types of switching power supplies considered for PV module emulation: AC-DC and DC-DC power supplies.

If the PV module emulator in question is designed to be run off the ac grid, it is possible to choose an AC-DC topology such as power factor correction, flyback, or forward converters. On the other hand, if the emulator runs off a DC power supply, then a DC-DC topology such as buck, buck-boost, or boost converters will be more suitable. Examples in the literature include single-phase DC-DC buck converter, three-phase AC-DC voltage source and current source rectifier, and an LLC resonant DC-DC converter [63-65].

In addition to circuit topologies, there are two main ways of generating the current-voltage relationship of the photovoltaic curve: analog-based and digital techniques [66-71]. The analog-based reference generation relies on analog circuits. One example is the use of a physical solar cell to generate the I-V relationship and simply amplify it for higher power output [31]. The digital techniques involve two methods of reference generation. The first method relies on equation solving where the complex equation in the photovoltaic model is used [72-73]. This method requires a sophisticated digital signal processor to make very fast calculations as to not slow down the loop frequency. The second method relies on generating the I-V reference and storing it in memory within a look up table with or without linear interpolation [74-77]. Increasing the number of points allows for greater resolution and accuracy.

The physical cell method relies on the implementation of an actual solar cell with a small amount of light illuminating it. The cell bias is simply the downscaled version of the PV emulator output voltage, and the solar cell current generated at the solar cell is outputted into the load using analog amplifiers. This requires a lighting source and a small circuit and area to accommodate the solar cell.

Equation solving implies that the photovoltaic emulator is calculating the diode equation given in the PV model section between each iteration. This requires the least amount of memory

with the most amount of computational time, and as shown in Chapter 4, does not appear to be fast enough to keep the loop frequency high for dynamic loads.

The look up table (LUT) method is one of the preferable methods since it relies on calculating the operational points before running the tests; therefore, saving tremendous amount of computational time at the expense of memory bandwidth. The points in between the values can be connected in two ways: either a few key points can be set and the program simply performs a linear interpolation between the two adjacent points, or as proposed in Chapter 4, a unique look up table value for each ADC value that eliminates linear interpolation overhead while adding a lot of memory requirements.

1.3.2. Photovoltaic Emulators in Literature

Koran *et al*. propose a PV module emulator device based on an AC-DC topology using the physical cell method [30]. The physical cell reference circuit schematic is based on a single solar cell connected across a MOSFET operating in the saturation region as a constant voltage load. The voltage and current values of the reference cell are measured to drive the control circuit.

The power section is complicated as it utilizes multiple circuits connected in series. The grid voltage is fed into an AC-DC synchronous rectifier and the resulting high DC voltage is filtered via a DC-link capacitor. This output is connected to the input of a DC-DC boost converter to increase the output voltage. The output of the DC-DC boost converter is scaled and fed into the physical reference circuit and the current output is again scaled and fed into a digital PI controller that drives the PWM signal to the boost converter. The output of the PV emulator is capable of emulating PV systems up to 200V and 20A.

The switching frequency of the PV emulator is 33 kHz, leading to unnecessarily large passive components with significant bulk and large volume. The high voltages and the multiple stages make it hard to choose efficient switching devices, which necessitates the usage of large heat sinks with large fans. Multiple boards are connected within a large box with the reference cell and light fixture placed on top.

While the authors have extensive knowledge on power electronics circuit design, the waveforms of the emulated curves do not look particularly good as their fill factors are much lower than the expected 60-80% range. Nevertheless, they were able to emulate a partially shaded PV system with great success. Their use of bulky analog references and low switching frequencies seems to be a problem for robust and high power density designs.

Gonzalez-Medina *et al*. propose quite a different approach in their PV module emulator which is based on a DC-DC converter with a simple non-synchronous buck converter power stage running at 100 kHz switching frequency [29]. Unlike others, the authors use a look up table with 26 strategically selected points, including a higher density of points near the maximum power point, with linear interpolation between two successive points to calculate the output. The authors have elected to use analog PI controllers for their inherent speed advantage at the expense of difficult tuning and large constant variations introduced by large capacitor variations in the PI circuit. The authors simply measure the output voltage and feed it into the look up table, which outputs a voltage through a digital to analog converter that drives the analog PI controller.

Due to the relatively high switching frequency of 100 kHz, the circuit requires smaller passive components and is possible to have it fit over the size of a typical mouse pad. Key advantages are look up table execution, which eliminates the need for a reference cell and challenging illumination and measurement circuits. The analog PI controller is a proven

topology, which gives good results but is being quickly phased out in literature and in the industry for digital controls.

1.3.3. Summary

Two of the main concerns in power electronic circuits are the power density and power efficiency. While most of the literature on power converters and topologies focuses on these two parameters, when it comes to PV emulators, these values have not been deemed important. One reason being that PV emulators are stationary units and portability is not desirable. Another reason given is that efficiency is not very important because a cooling system can be devised.

While both concerns are true at first thought, a deeper look into the power density and efficiency metrics paints another picture. Having a very high power density circuit allows for improved portability and plug-and-play simplicity that is not common. A high efficiency circuit allows for fanless designs as discussed in Chapters 4 and 5, and also makes long tests possible because heating and local hot spots are not a concern. The emulator can also run in elevated temperature environments to better emulate high ambient temperatures that occur in summer when testing inverters and other equipment.

The industry has been moving towards digital controls in power electronic circuits for a while, and keeping up with this latest trend is important for innovation. Most PV emulators in the literature rely on analog controllers; however, all PV emulators in this dissertation rely on digital controls.

Analog-based I-V reference generation is not very straightforward and easy as it is claimed to be, since it does not allow for easily changing the open-circuit voltage, short-circuit current, fill-factor, operational temperature, irradiance, and partial shading parameters. Digital-based references are capable of much higher flexibility in these regards. With digital references,

it is possible to program changing dynamic conditions of irradiance, temperature and partial shading as well. Therefore, all circuits proposed in this work are based on digital I-V reference generation.

1.4. Dissertation Outline

This dissertation consists of six chapters all geared towards the main objective of this work: improving the capabilities and reducing the volume and price of I-V curve tracers, and improving the power density, efficiency, and dynamic performance of silicon and GaN-based photovoltaic emulators using buck converters. I-V curve tracers allow for the measurement of typical curves for single module and high power PV arrays and PV emulators make possible the use of DC power supplies in emulating PV module characteristics.

Chapter 1 discusses the background of this research, drawing examples from academic literature and industrial products. Different examples of I-V curve tracers and PV module emulators are presented with their merits and drawbacks. The main issue with the I-V curve tracers in literature and market are the high costs and the high volume of the measurement system. These issues will be challenged and overcome as outlined in Chapter 3. The main drawbacks of PV module emulators are the dynamic capabilities, the power density, and the power efficiency. The PV models used in specific literature examples leaves a lot to be desired in producing an accurate emulated output. Work on PV module emulators will be carried out in Chapters 4 and 5.

In the second chapter, suitable PV models will be investigated with a focus on simplicity, accuracy and applicability within I-V measurements and PV emulators. The PV model chosen must model PV modules at different temperature, irradiance and partial shading conditions

accurately. The elimination of the series and shunt resistance parameters will make it possible to simplify the required calculations for the PV emulator. The parameter conversion from arbitrary values to standard testing conditions (STC) will allow the I-V curve tracer to translate the measurements taken to STC conditions with great accuracy.

In Chapter 3, two distinct generations of curve tracers will be proposed with the goal of minimizing volume, costs and increasing measurement accuracy, resolution and the number of data points. Generation 1 will lay the foundation as the proof of concept for capacitive load I-V curve measurements. Generation 1.5 will build upon it with algorithm optimizations to make measurements at different conditions including partial shading. Generation 2 will do away with the mechanical relays from the previous generation and MOSFET switches will be explored with the goal of allowing for a more compact and lower-cost design with improved reliability.

In Chapter 4, new PV module emulator designs is investigated through two distinct generations. While both are buck converters, generation 1 will focus on creating the algorithm and basic circuitry that forms the heart of the PV emulator with the use of a non-synchronous buck converter and an equation solving system. Generation 2 will demonstrate innovation in high switching frequency along with significant reduction in steady-state errors and power losses. In generation 2.5, the dynamic performance of the emulator will be increased to work with dynamic loads. This will be accomplished by moving from an equation solving approach to a look-up table approach. The new approach will reduce the execution time and improve the loop frequency significantly.

Chapter 5 examines the use of novel GaN devices to replace traditional silicon devices in PV module emulators. The impact of GaN MOSFETs for increasing the efficiency, power density and dynamic response of PV module emulators is explored. Static tests using an

electronic load and dynamic tests using an inverter are demonstrated that show the accuracy of emulating both static conditions and temporal changes of irradiance, temperature, and partial shading. The design of the algorithm and the controller are described as well, as they have a significant effect on the loop frequency, and obtaining better dynamic performance to match the dynamic characteristics of actual PV modules.

Chapter 6 summarizes the main contributions of this work and proposes future work and research avenues.

CHAPTER 2

MODELING OF PHOTOVOLTAIC MODULES

2.1. Introduction

Modeling the behavior of photovoltaic modules is important for module characterization, I-V curve measurements, and PV module emulation. The model used must represent photovoltaic modules accurately without prohibitively difficult mathematical operations that make the solutions hard to obtain.

PV module measurements taken outdoors are under an uncontrolled solar irradiance and ambient temperature. For consistent results, these measurements must be converted to standard testing conditions (STC) for proper characterization of PV modules. Similarly, with I-V curve measurements, the measured curves need to be transposed to STC for meaningful and comparable results.

In order to convert the I-V measurements of PV modules to STC, there are only six parameters that can be used towards STC conversion:

- Voltage V_{pv} and current I_{pv} output of the module,
- Incident irradiance S, the ambient temperature $T_{ambient}$, and
- Temperature coefficient of voltage α_V and temperature coefficient of current α_I.

The PV model will have to only work with S and $T_{ambient}$ variables and rely on the datasheet values of α_V and α_I to convert the measurements of V_{pv} and I_{pv} from arbitrary conditions to STC. After STC conversions are made, if desired, the values for open-circuit voltage V_{oc}, short-circuit current I_{sc}, diode saturation current I_o, diode ideality factor n, series resistance R_s, and shunt resistance R_{sh} can be extracted from the I-V curve.

PV module emulation on the other hand, does not require STC conversions and must work with any given values for V_{oc}, I_{sc}, I_o, R_s, R_{sh}, S and $T_{ambient}$. The complexity of the PV model can be increased for emulation purposes as the curve is drawn from scratch, unlike the conversion processes used for measurements.

There are two approaches to modeling PV modules, the first of which can be modeled as multiple solar cells connected in series (usually 60) to construct what is known as a high power module with a power rating between 200W and 250W. The second approach, which is the approach taken in this dissertation, is to model the entire PV module as a single solar cell. This has some advantages when working with PV modules, as we do not have to calculate individual solar cell V_{oc} and factor in the number of cells, which reduces the complexity of the model.

2.2. Diode Models

There are three main ways of modeling photovoltaic modules in the literature: single-diode, ideal single-diode, and dual-diode models. These models slightly differ among themselves in theory, but there is a large discrepancy when it comes to mathematical complexity. Among these, the ideal single diode model provides the simplest mathematical equation that is easily solvable without using iterative methods, which both the single diode and the dual-diode require. In the single and dual-diode models, the presence of photovoltaic current both on the left side of the equation and within an exponential on the right side of the equation calls for the Lambert W method, which significantly increases the mathematical and computational overhead [78].

2.2.1. Single Diode Model

The single diode model is the most commonly used model in solar cells owing to its relative simplicity and good correlation. The solar cell is modeled as a current source with I_{ph}, a

series anti-parallel diode, the series resistance R_s that models the series losses in the device, and the shunt resistance R_{sh} that models the recombination losses in the device. The schematic of the model is given in Figure 2.1.

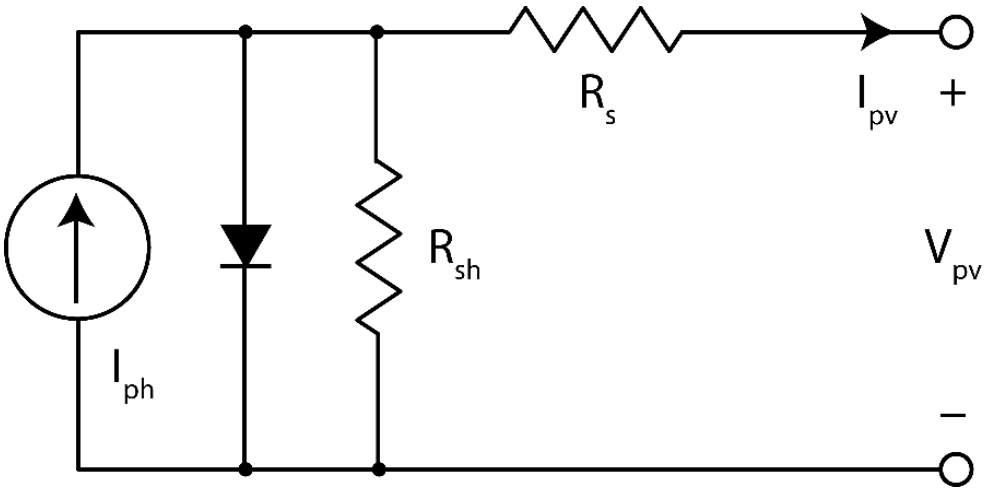

Figure 2.1: Single diode model of a solar cell with series and shunt resistances based on [79].

The equation for the single-diode model is given by Equation 2.1,

$$I_{pv} = I_{ph} - I_o \left[\exp\left(A\left(V_{pv} + R_s I_{pv}\right)\right) - 1\right] - \frac{V_{pv} + R_s I_{pv}}{R_{sh}} \tag{2.1}$$

where A combines the diode ideality factor, Boltzmann's constant, cell temperature and electronic charge,

$$A = \frac{q}{nkT} \tag{2.2}$$

For modern PV cells and modules, the effects of R_s and R_{sh} are not as significant as they used to be, due to the improvements in manufacturing processes in recent years.

2.2.2. Ideal Single Diode Model

The ideal diode model ignores the non-ideal effects of series and shunt resistances and simplifies both the schematic and the equations.

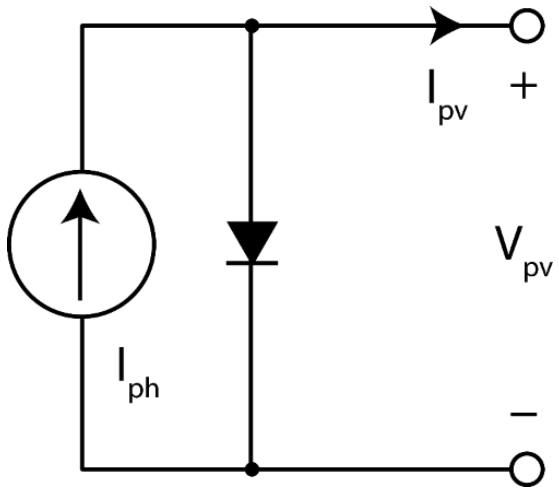

Figure 2.2: Ideal single diode model of solar cell without resistances based on [80].

A few assumptions are made for the ideal single diode model: the series resistance is assumed to be zero, the shunt resistance is assumed to be infinitely large, the photon current I_{ph} is assumed equal to the short-circuit current I_{sc} and the exponential term is assumed much larger than one, allowing the removal of the "-1" term. The new equation describing the diode therefore is:

$$I = I_{sc} - I_o \exp(A \cdot V) \tag{2.3}$$

$$I_{sc} = I_o \exp(A \cdot V_{oc}) \tag{2.4}$$

$$I_o = I_{sc} \exp(-A \cdot V_{oc}) \tag{2.5}$$

$$I = I_{sc}(1 - \exp[A \cdot (V - V_{oc})]) \tag{2.6}$$

$$I_{mpp} = I_{sc}\left(1 - \exp\left[A \cdot \left(V_{mpp} - V_{oc}\right)\right]\right) \tag{2.7}$$

$$A = \frac{\ln\left(1 - \frac{I_{mpp}}{I_{sc}}\right)}{V_{mpp} - V_{oc}} \tag{2.8}$$

$$I = I_{sc}\left[1 - \exp\left(\frac{\ln\left(1 - \frac{I_{mpp}}{I_{sc}}\right)(V - V_{oc})}{V_{mpp} - V_{oc}}\right)\right] \tag{2.9}$$

In the end, the current equation can be simply derived from the open-circuit voltage V_{oc}, the short-circuit current I_{sc}, the maximum power point voltage V_{mpp} and the maximum power point current I_{mpp}. This eliminates the requirement for knowing I_o and a, values which are not provided by module manufacturers.

2.2.3. Two Diode Model

Both the single diode and the ideal single diode solar cell model assume a fixed value for the diode ideality factor n. This assumption does not hold in reality since the diode ideality factor is dependent on the bias voltage across the solar cell.

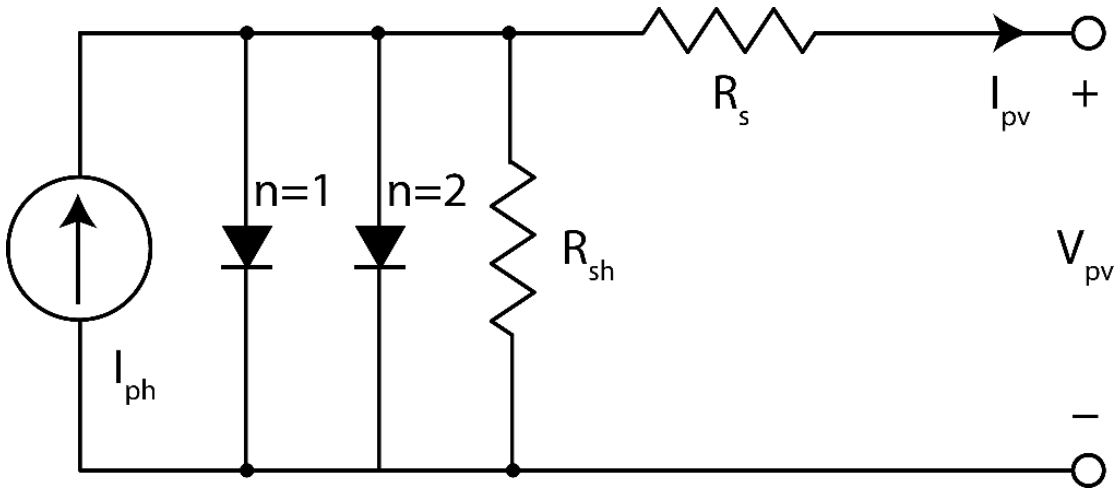

Figure 2.3: Two diode model of solar cell with series and shunt resistances based on [81].

When V_{pv} is large, the recombination of the charge carriers (holes and electrons) is dominated by surfaces and bulk regions, therefore the ideality factor *n* converges to 1. On the other hand, when the cell voltage V_{pv} is low, the recombination at the junction dominates and *n* converges to 2.

The second diode in the two diode model is necessary to account for junction recombination effects. Some drawbacks have been observed in literature, i.e. the recombination is dependent on carrier concentration, the two diode model is challenging to resolve mathematically, small fluctuations in light intensity overwhelm the second diode effects, and the two diode model is more common for dark measurements (without light) [81].

The current equation used in the two diode model is given below,

$$I = I_L - I_{o1}\left(\exp\left[\frac{q(V+IR_s)}{kT}\right]-1\right) - I_{o2}\left(\exp\left[\frac{q(V+IR_s)}{2kT}\right]-1\right) - \frac{V+IR_s}{R_{sh}} \qquad (2.10)$$

For dark measurements (which are more common) the equation becomes,

$$I = I_{o1}\left(\exp\left[\frac{q(V+IR_s)}{kT}\right]-1\right) + I_{o2}\left(\exp\left[\frac{q(V+IR_s)}{2kT}\right]-1\right) + \frac{V+IR_s}{R_{sh}} \qquad (2.11)$$

Ignoring the "-1" term makes analysis much easier under light,

$$I = I_L - I_{o1}\exp\left[\frac{q(V+IR_s)}{kT}\right] - I_{o2}\exp\left[\frac{q(V+IR_s)}{2kT}\right] - \frac{V+IR_s}{R_{sh}} \qquad (2.12)$$

and under dark conditions,

$$I = I_{o1}\exp\left[\frac{q(V+IR_s)}{kT}\right] + I_{o2}\exp\left[\frac{q(V+IR_s)}{2kT}\right] + \frac{V+IR_s}{R_{sh}} \qquad (2.13)$$

2.2.4. Comparison of Diode Models

The ideal single diode model provides the easiest method for modeling solar cells. With the inclusion of the series and shunt resistances, the model becomes highly accurate and can approximate the small current reduction from the short-circuit point to maximum power point

very well [34]. The two-diode model on the other hand, complicates matters beyond what is generally worth accomplishing; that is to say, the drawbacks far outweigh the benefits.

Mahmoud *et al.* studied different models to model photovoltaic modules accurately [34]. In their paper, they propose the following enhancement to the single diode model:

$$I = I_{ph} - I_s\left(\exp\left[\frac{\alpha_0 + \alpha_1 V + \alpha_2 V^2 + \alpha_3 V^3}{\frac{N_s kTA}{q}}\right] - 1\right) - \frac{\alpha_0 + \alpha_1 V + \alpha_2 V^2 + \alpha_3 V^3}{R_{sh}} \quad (2.14)$$

As shown above, the goal is to eliminate the difficult to calculate "current-within-the-exponent" issue by using a polynomial that approximates the relationships,

$$\alpha_0 = I_{sc} R_s \quad (2.15)$$

$$\alpha_0 + \alpha_1 V_{mpp} + \alpha_2 V_{mpp}^2 + \alpha_3 V_{mpp}^3 = V_{mpp} + I_{mpp} R_s \quad (2.16)$$

$$\alpha_0 + \alpha_1 V_{oc} + \alpha_2 V_{oc}^2 + \alpha_3 V_{oc}^3 = V_{oc} \quad (2.17)$$

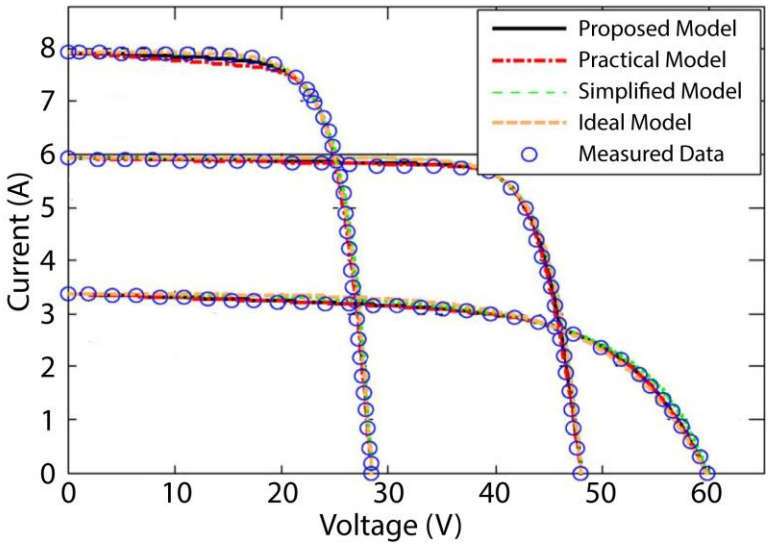

Figure 2.4: Comparison of different models when fitting to measured data based on [34].

Their results show that the computational times decreased at a cost of increased inaccuracy at low irradiance levels. In Figure 2.4, the practical model refers to the single-diode model, the simplified model refers to the single-diode model with the shunt resistance omitted, the ideal model is the ideal single-diode model, and the proposed model is the polynomial fitted model [34]. As clearly shown, all models lie within the measured data circles indicating that regardless of model chosen, they all model PV modules well.

2.3. Model Used in Dissertation

2.3.1. Model selection

The model chosen for the purposes of this work needs to fulfill the following criteria:

1. Must be easily solvable,
2. Must model irradiance, temperature and shading effects accurately,
3. Must allow the input of V_{oc}, I_{sc}, I_o, S, T, α_V, α_I, *system shading* and *shading strength*,
4. Must be highly accurate,
5. Must work in any given application, and
6. Must model the whole PV module or PV array as a single cell.

After the analysis of different models in the literature and especially looking at Figure 2.4, the ideal single diode model was chosen as the most suitable model for this work. To confirm the validity of our choice, the ideal diode model was then verified with the photovoltaic modules installed on the roof of Kaufman Hall at the Old Dominion University consisting of 8 series connected Bosch c-Si m60 photovoltaic modules. The results are shown in the Figures 2.5 and 2.6 below.

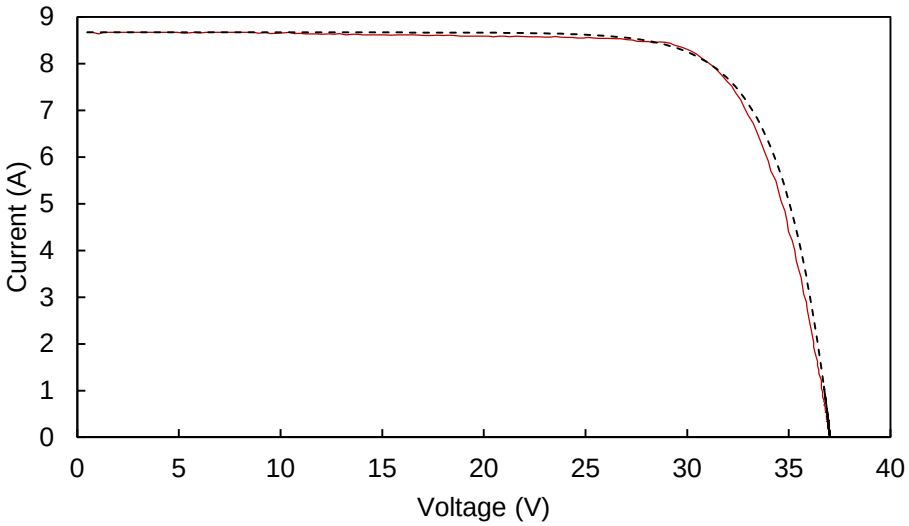

Fig. 2.5: Measured (solid line) vs. simulated (dashed line) I-V curves.

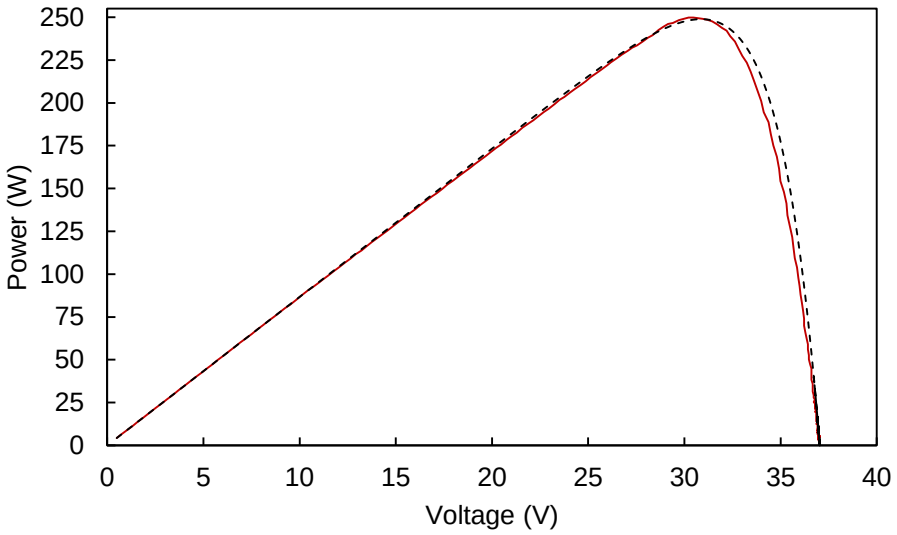

Fig. 2.6: Measured (solid line) vs. simulated (dashed line) P-V curves.

The conditions in Figures 2.5 and 2.6 were V_{oc} = 37.03V, I_{sc} = 8.67A and I_o = 1μA with a fill factor of 77.8% show suitable correlation between the measured and calculated curves.

2.3.2. Modeling Effects of Irradiance and Temperature

The power output of PV modules are dependent on irradiance and temperature. This section discusses the equations used to convert values from STC to different *S* and *T* conditions. In Chapter 3, measurements made in arbitrary *S* and *T* conditions are converted to STC using similar equations.

The procedure to model effects of irradiance and temperature are as follows. First, the values for the variables shown in Table 2.1 are input. These inputs correspond to the STC values of short-circuit current, open-circuit voltage and dark saturation current, values of irradiance and temperature, the temperature coefficients found in the module datasheet, and the band gap of the PV module material (1.12eV for silicon).

Table 2.1: Ideal model initialization parameters.

Symbol	Name	Value
T_{cell}	Module temperature	25.0°C (user input)
T_{ref}	Reference temperature	25.0°C
$V_{oc,stc}$	Open-circuit voltage	40V (user input)
$I_{sc,stc}$	Short-circuit current	8A (user input)
$I_{o,stc}$	Dark saturation current	10µA (user input)
S	Irradiance	1000 W/m^2 (user input)
α_I	I_{sc} temperature coefficient	0.00053 A/°C (datasheet)
α_V	V_{oc} temperature coefficient	-0.0034 V/°C (datasheet)
$E_{g,stc}$	Silicon band gap	1.12 eV
$k_{boltzmann}$	Boltzmann coefficient	0.00008617332478 eV/K

First, cell temperature and reference temperature values are converted to Kelvin,

$$T_{cell_k} = T_{cell} + 273.15 \tag{2.18}$$

$$T_{ref_k} = T_{ref} + 273.15 \tag{2.19}$$

Next, an intermediary value for *a* is calculated and transposed to cell temperature,

$$A_{stc} = \frac{\ln\left(\frac{I_{sc_{stc}}}{I_{o\,stc}}\right)}{V_{oc_{stc}}} \tag{2.20}$$

$$A = \frac{A_{stc} \cdot T_{cell_k}}{T_{ref_k}} \tag{2.21}$$

Afterwards, the new values of V_{oc} and I_{sc} are calculated for given temperature and irradiance conditions,

$$V_{oc} = \left[V_{oc_{stc}} + \frac{\ln\left(\frac{S}{1000}\right)}{A}\right]\left[1 + \alpha_V \cdot \left(T_{cell} - T_{ref}\right)\right] \tag{2.22}$$

$$I_{sc} = \frac{S}{1000} \cdot I_{sc_{stc}} \cdot \left[1 + \alpha_I \cdot \left(T_{cell} - T_{ref}\right)\right] \tag{2.23}$$

Next, the new values of E_g and I_o are calculated for the given temperature and irradiance conditions,

$$E_g = E_{g_{stc}} \cdot \left[1 - 0.00002677\left(T_{cell} - T_{ref}\right)\right] \tag{2.24}$$

$$I_o = I_{o_{stc}} \cdot \left(\frac{T_{cell_k}}{T_{ref_k}}\right)^3 \cdot \exp\left(\frac{E_{g_{stc}}}{T_{ref_k}} - \frac{E_g}{T_{cell_k}}\right) / k_{boltzmann} \tag{2.25}$$

Finally, *a* is recalculated to correct the fill factor,

$$A = \frac{\ln\left(\frac{I_{sc}}{I_o}\right)}{V_{oc}} \tag{2.26}$$

Shown in Figures 2.7 and 2.8 are the effects of different irradiance and temperature conditions for the conditions in Table 2.1. Figure 2.7 shows the I-V and P-V curves for changing irradiance values starting from 1000W/m^2 at the top and decreasing in 100W/m^2 steps to the lowest value of 100W/m^2. The linear relationship between I_{sc} and S is apparent, but the voltage

dependence is not as straightforward to model.

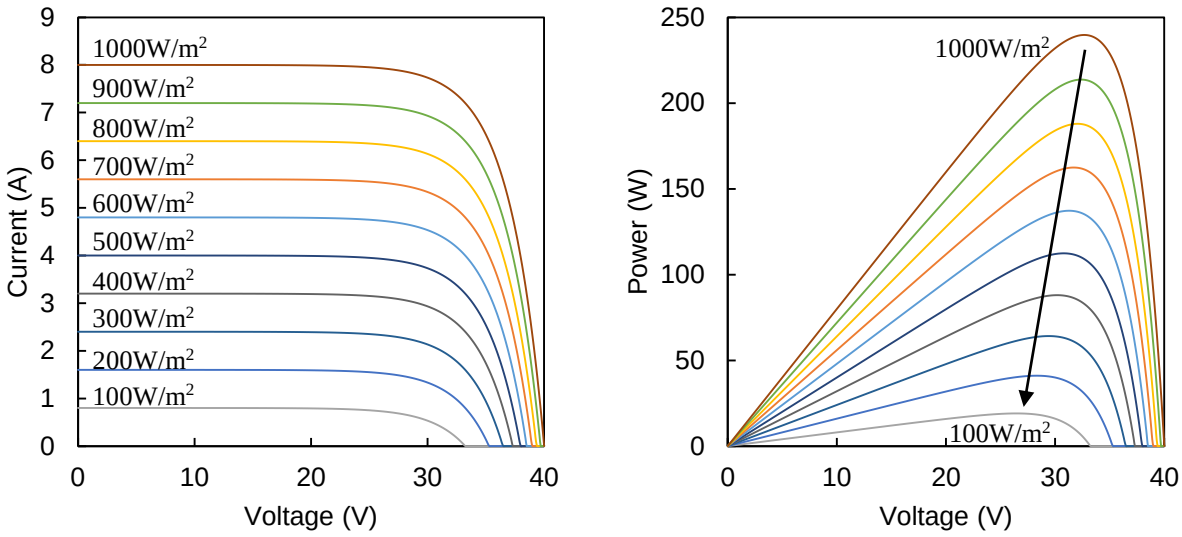

Figure 2.7: I-V and P-V curve dependence on incident irradiance (100-1000W/m^2).

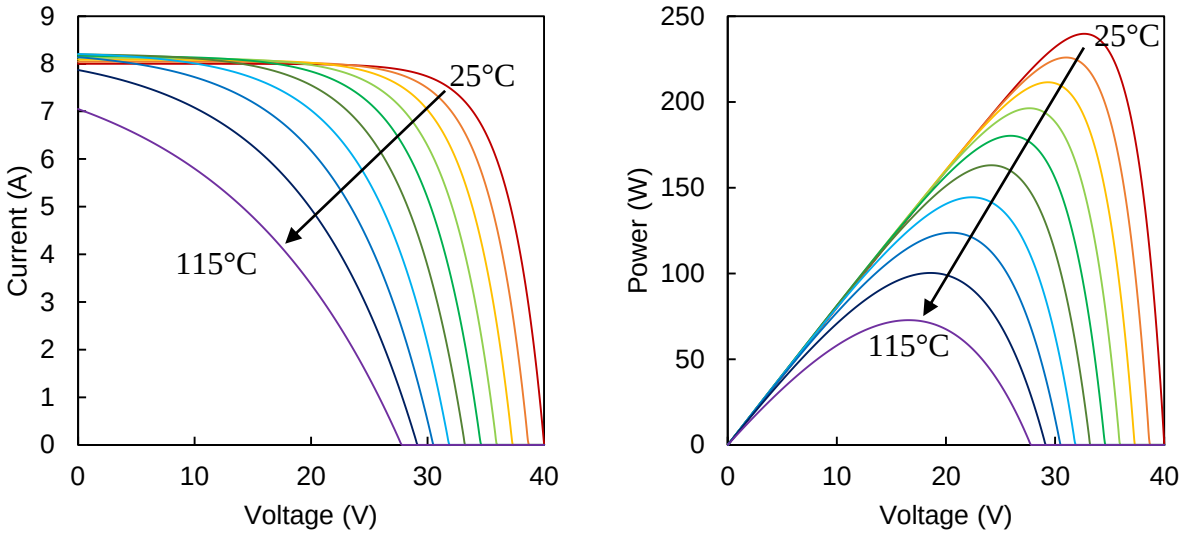

Figure 2.8: I-V and P-V curve dependence on ambient temperature (25-115°C).

In Figure 2.8, the I-V and P-V curves from 25°C to 115°C are shown in 10°C increments, with the curves moving left and down with increasing temperature. Since the model used models temperature in terms of linear coefficients, V_{oc} and I_{sc} vary linearly but the shape of the curve significantly changes. The effect of increasing temperature adds a positive gain to the short-circuit current and negatively impacts the open-circuit voltage. In the end, for increasing ambient temperatures, PV modules perform worse than their rated performance at STC. Therefore, if high ambient temperature conditions exist, it is important to select PV modules with lower temperature coefficients.

2.3.3 Modeling Partial Shading Conditions

Partial shading is defined in two terms: *system shading*, the percentage of the PV module shaded, and *shading strength*, the percentage of the incident light blocked by shading. Modeling partial shading conditions is more involved when compared to modeling different temperature and irradiance conditions. Modern PV modules have bypass diodes located in parallel with the internal cells to protect the PV module in the case of partial shading, and the effects of the bypass diodes need to be correctly modeled.

During operation at MPP, when partial shading occurs, the cells that receive less irradiance than the unshaded cells produce less current I_{shaded} when compared to the unshaded cell current $I_{unshaded}$ as shown in Figure 2.9.

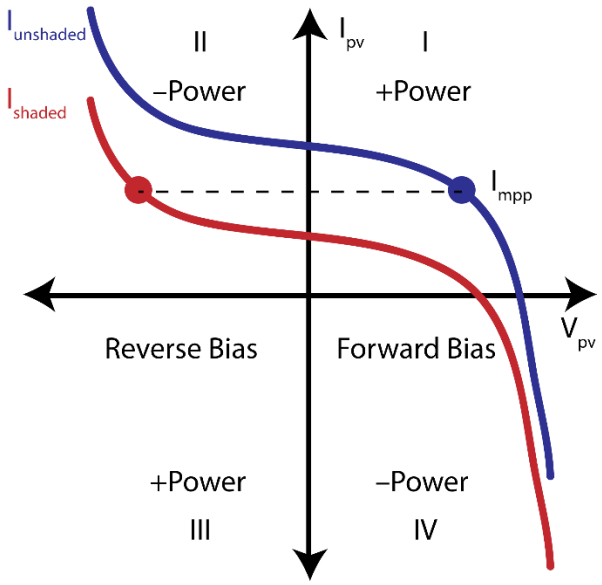

Figure 2.9: PV cell operation regions for unshaded (blue) and shaded cells (red).

Since all cells are connected in series, the current exiting the unshaded cells will have to circulate through the shaded cells causing them to operate in the reverse bias region (quadrant II) and consume power. The power consumed will then be dissipated across the shaded cell and may cause it to overheat and fail. To overcome this problem, bypass diodes are connected across solar cells to route the excess current externally, as shown in Figure 2.10, allowing the reverse bias across the shaded cells to be limited to a single diode drop of about 0.5V. This, while not eliminating losses, reduces them significantly. The shaded cell in Figure 2.10 is shown in dark blue and the conducting bypass diode is shown in green. In a 60-cell high power PV module, there are three bypass diodes connected to 20 solar cells each and partial shading implies that either 1/3 or 2/3 of the PV module is partially shaded.

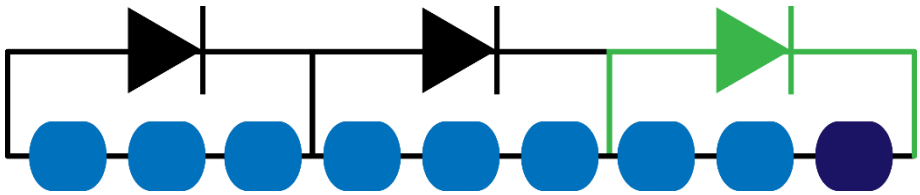

Figure 2.10: Bypass diodes connected across series-connected solar cells.

To model partial shading, the I-V curve is divided into three sections. Section 1 corresponds to the portion beginning at 0V until $I_{pv\_unshaded}$ is equal to I_{sc_shaded}. The second section corresponds to a flat output current equal to I_{sc_shaded}. The third section begins when the regular output of the unshaded module current I_{pv} is lower than I_{sc_shaded}. The individual sections are highlighted in Figure 2.11 where the blue line represents $I_{pv\_unshaded}$, the red line represents I_{sc_shaded}, the green line represents I_{pv} and the dashed line represents the I-V curve of a partially shaded PV module.

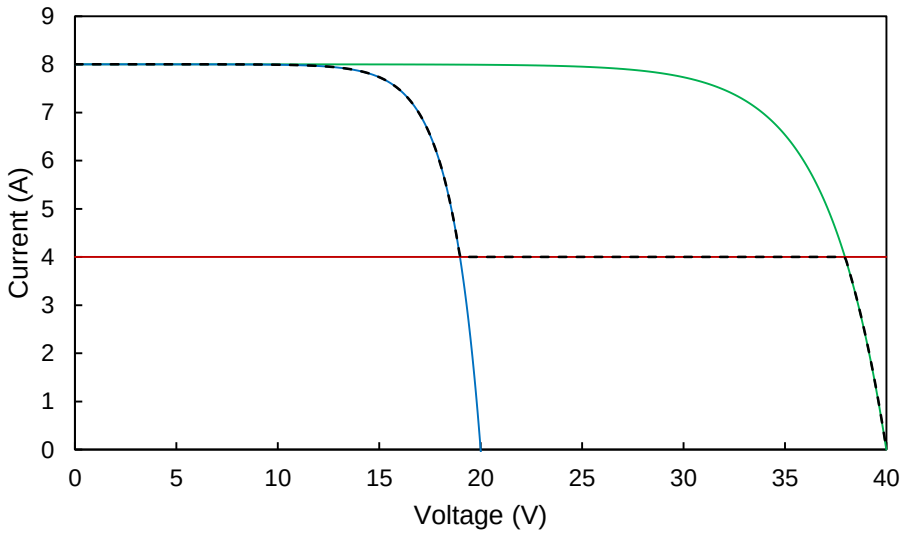

Figure 2.11: Construction of a PV module partial shading model for V_{oc} = 40V, I_{sc} = 8A, *system shading* = 0.5, and *shading strength* = 0.5.

The equations used for modeling sections 1, 2, and 3 respectively are given below,

$$I_{pv_{unshaded}} = I_{sc} - I_o \cdot \exp\left(\frac{A \cdot V}{1 - system\ shading}\right) \tag{2.27}$$

$$I_{sc_{shaded}} = I_{sc} \cdot (1 - shading\ strength) \tag{2.28}$$

$$I_{pv} = I_{sc} - I_o \cdot \exp(A \cdot V) \tag{2.29}$$

If *system shading* is equal to 1 (fully shaded), then the PV module is modeled at an irradiance corresponding to the shading strength without partial shading. In this case the body diode will not conduct and there will not be a flat-line as observed in section 2 of the I-V curve. The accuracy of the partial shading model was compared to the output of an actual PV module as shown in Figure 2.12.

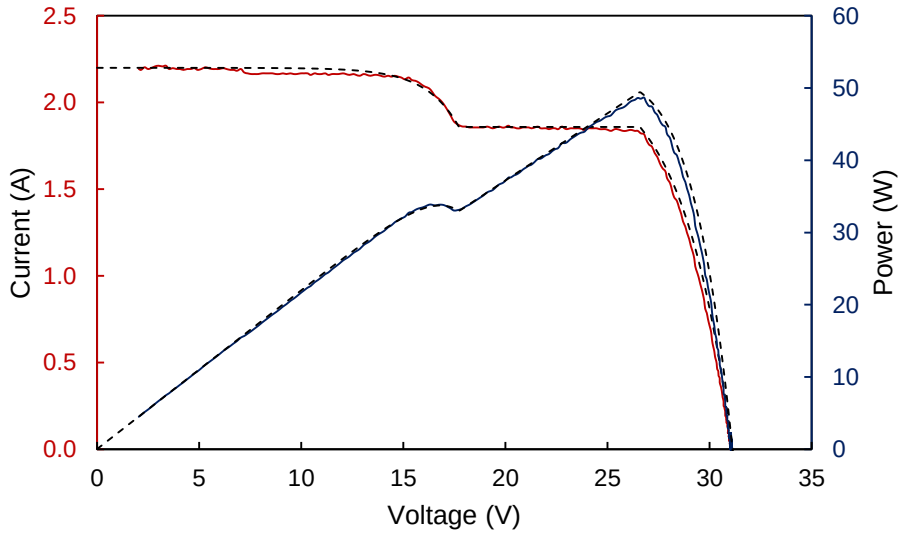

Figure 2.12: Measured (solid lines) and modelled curves (dashed lines) for a partially shaded PV module.

Figure 2.12. shows the I-V curve of a Bosch c-Si M60 PV module tested under partial shading conditions. A single cell of the PV module was partially shaded by a sheet of cardboard. The ambient conditions were 240.8 W/m^2 and 52.8°C. The measured values of V_{oc} and I_{sc} were 31.1V and 2.2A, respectively. *System shading*, *shading strength* and I_o were adjusted until the measured and modeled curves matched each other. The *system shade* was 1/3 due to the configuration of the bypass diodes, the *shading strength* (15.5%) was calculated from the flat line corresponding to I_{sc_shaded} and I_o was determined to be 6.1µA.

2.4. Conclusions

A good model to simulate the operation of the photovoltaic module is critical for successful applications of I-V curve measurements and simulations. Four different models were presented with their merits and drawbacks. In the end, the application demanded a simple and reliable model, therefore the ideal diode model was chosen to model the whole module or photovoltaic array as it would a single solar cell. It has been demonstrated in this chapter that for unshaded conditions, the ideal-diode model successfully models I-V curves of single PV modules with negligible errors. For shaded conditions, the three part piecewise model has been proven to work successfully.

CHAPTER 3

I-V CURVE MEASUREMENTS OF PHOTOVOLTAIC MODULES

3.1. Introduction

I-V curve tracers are critical for detecting possible anomalies throughout the whole range of the operational curve of photovoltaic modules. Among the vast selection of curve tracer topologies, only the capacitive load is portable enough to be used in field applications. The devices observed in literature so far tend to be large, bulky, expensive, and consist of a very complex array of switches, switch driver configurations and lack modern data acquisition techniques.

The devices proposed in this chapter abide by the following criteria:

1. Capacitive load with built-in data logging capability,
2. Highly portable and lightweight,
3. Low-cost (ideally less than $100),
4. Provide a simple switching mechanism, and
5. Modular (works with different PV system sizes)

Various generations of devices have been built to get closer to these ideal goals. Before discussing the two generations in detail, an overview of the possible voltage and current sense methods are discussed first. Afterwards, the design challenges pertaining to selecting a mechanical switch are discussed. Furthermore, the different topologies are touched upon with a detailed overview of the capacitive load topology. Finally, the two distinct generations are discussed in full detail with additional comments for the improvement of Generation 1 (dubbed Generation 1.5).

3.1.1. Voltage and Current Sense Methods

There are many methods available in the industry that allow for accurate measurements of current and voltage. Among them there are two popular methods: transducers and resistors.

Transducers offer the easiest solution to designing highly reliable measurement circuits at a cost of limited customization abilities, price, size, difficult supply requirements (±12V) and limited accuracy and linearity. It is most common to use hall sensors to measure current in an isolated manner whereas for voltage measurements, isolated measurements are more complicated. Technically speaking, voltage transducers are not common and in reality they do not exist. Rather, the voltage must be converted to a measurable current to create the galvanic isolation of a transformer when the voltage is measured using a hall sensor. This makes it challenging to measure voltages using transducers and voltage measurements are usually carried out with resistor dividers or other methods using isolated operational amplifiers.

Voltage divider resistors are very accurate when using 0.1% resistors, they come in different sizes and values and can be perfectly tailored for the measurement requirements. A low impedance buffer, i.e. an operational amplifier, is needed to transform the high impedance voltage signal to a low impedance voltage so that measurements can be taken accurately. This is the solution chosen thus far for voltage measurements.

Current sense resistors can be used to indirectly measure current by measuring the voltage drop observed across a serially connected resistor on the return path of the system to measure the current flow. This method is slightly more difficult to implement than a current transducer, but it offers great flexibility and modularity. In the case of current sense resistors, a compromise is made between a large voltage drop (and losses) and noise susceptibility (low voltage drop). Operational amplifier gain is required with various possible choices of schemes,

i.e. inverted, non-inverted and differential measurements to properly measure the small voltage drop across the current sense resistor, usually in the millivolt range.

3.1.2. Mechanical Switch Selection

Mechanical switch selection is perhaps the most challenging part of designing an I-V curve tracer for a high voltage and high current system. Since all photovoltaic modules produce DC current, a DC relay must be selected for reliable operation. Unfortunately, the availability of DC relays becomes limited once operational voltages go above 30VDC. There are indeed very few DC relays that can operate above 400 VDC in a compact and cost efficient package.

The high prices of relays and their general bulkiness due to the large contact clearance, coupled with the design objective of driving the relays in a compact device with a 5V DC bus reduces the choice of relays significantly. A selection of relays is presented in Table 3.1 from which among them the Fujitsu FTR-J2 was selected due to its high voltage and current rating suitable to make measurements of our own PV system, and for its low cost and small volume.

Table 3.1: Comparison of different relays with over 10A current rating.

Manufacturer	Model	Voltage Rating	Current Rating	Unit Price
Fujitsu	FTR-J2	450 VDC	10A	$16.78
Omron	G6C-1114P-US	125 VDC	10A	$6.25
Panasonic	HEV2AN-P-DC	800 VDC	20A	$99.31

3.1.3. Circuit Topology Selection

Initially, a variable resistive load and three different electronic load topologies were explored: buck, cascaded buck-boost, and boost converter; however, they were proven to be non-

robust and quite unsatisfactory in providing a noise-free measurement. It also took quite a long time (10 seconds) to trace the full curve, leading to large power sinking issues. Therefore, resistive load and electronic load topologies were abandoned in favor of a capacitive load. The properties of resistive loads, electronic loads and capacitive loads are highlighted in Table 3.2.

Table 3.2: Summary of I-V curve tracing methods explored.

Metric	Resistive Load	Electronic Load	Capacitive Load
Speed	Slowest	Faster	Fastest
Cost	Expensive	Less expensive	Least expensive
Weight	Heavy	Light (heavy resistor)	Lightest
Robustness	Not scalable	Resistor limitation	Capacitor limitation
EMI	Low noise	High noise	Low noise

3.1.4. Principles of Operation

Figure 3.1 depicts the simplified schematic of a curve tracer for a string of PV panels using a capacitive load consisting of two switches (Switch 1 and Switch 2, a load capacitor and discharge resistors.

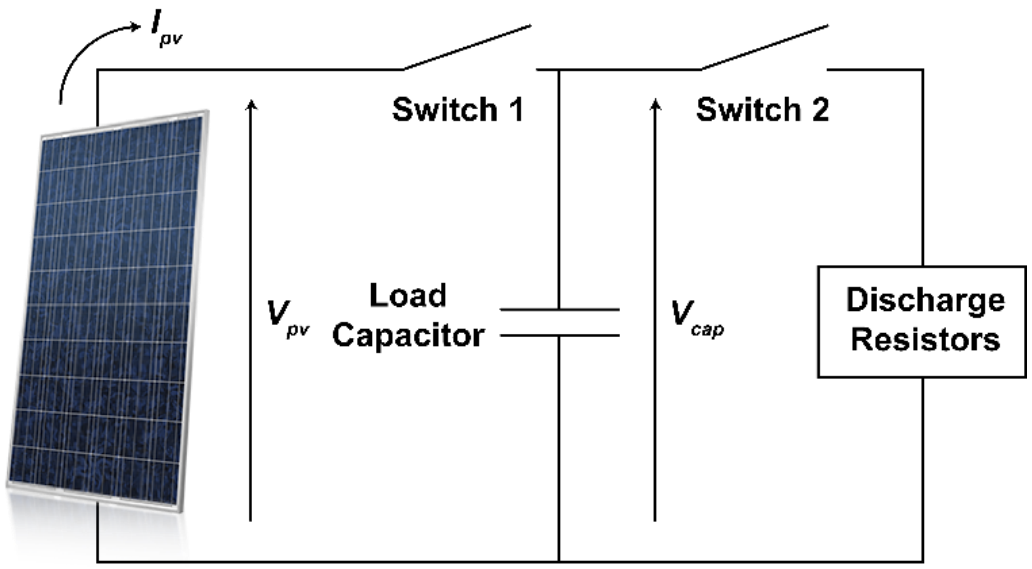

Figure 3.1: Simplified schematic of a curve tracer using a capacitive load based on [59].

This circuit, owing to its passive nature, is capable of only making single-quadrant measurements, i.e. the circuit can sink power but cannot inject any power into the PV system. To make I-V curve measurements, the load capacitors are allowed to fully discharge through the discharge resistors by closing switch 2. Once the load capacitor is fully discharged (confirmed when $V_{cap} = 0$), switch 2 is opened and switch 1 is closed to begin charging the capacitor via the PV array. The charge profile of the capacitor allows for measuring the I-V curve of the PV array.

There are a few ways of building a capacitive load, in which the switches can be either semiconductors (i.e. MOSFET, IGBT) or mechanical (DC relays). Voltage and current measurements can be taken either isolated or non-isolated depending on the complexity of the measurement system and the safety of the design.

3.1.4.1. Constant Voltage Source

When a capacitor is charged with a constant voltage source, the capacitor voltage, current and power profiles as a function of time are shown in Figure 3.2. The capacitor voltage and

current follow Equations 3.1 and 3.2,

$$V_c = V_s\left(1 - e^{-t/RC}\right) \tag{3.1}$$

$$I_c = \frac{V_s}{R} e^{-t/RC} \tag{3.2}$$

where V_s is the supply voltage, V_c is the capacitor voltage, t is the instantaneous time, R is the circuit resistance, C is the capacitance and I_c is the capacitor charge current. The conditions in Figure 3.2 demonstrate that the capacitor can absorb a lot of power without any heating whatsoever. This property allows the capacitive load to be used in large PV systems without any concern for capacitor heat sinking. The discharge resistors on the other hand have to be sized large enough to dissipate the energy stored in the capacitor without significant heating.

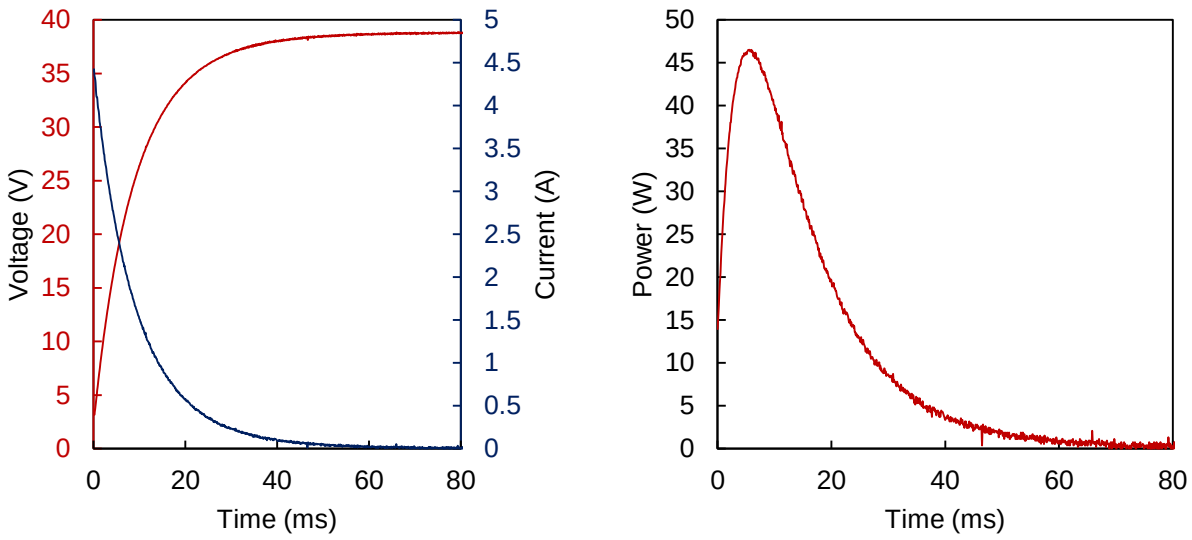

Figure 3.2: Measured voltage, current, and power vs. time curves of a capacitor charged with a constant voltage source (38V) and an 8Ω resistor connected in series.

3.1.4.2. Photovoltaic Source

When a capacitor is charged with a PV source (e.g.: V_{oc} = 32.8 V, I_{sc} = 6.8 A) as shown in Figure 3.3, the shape of the voltage curve differs from the constant voltage case.

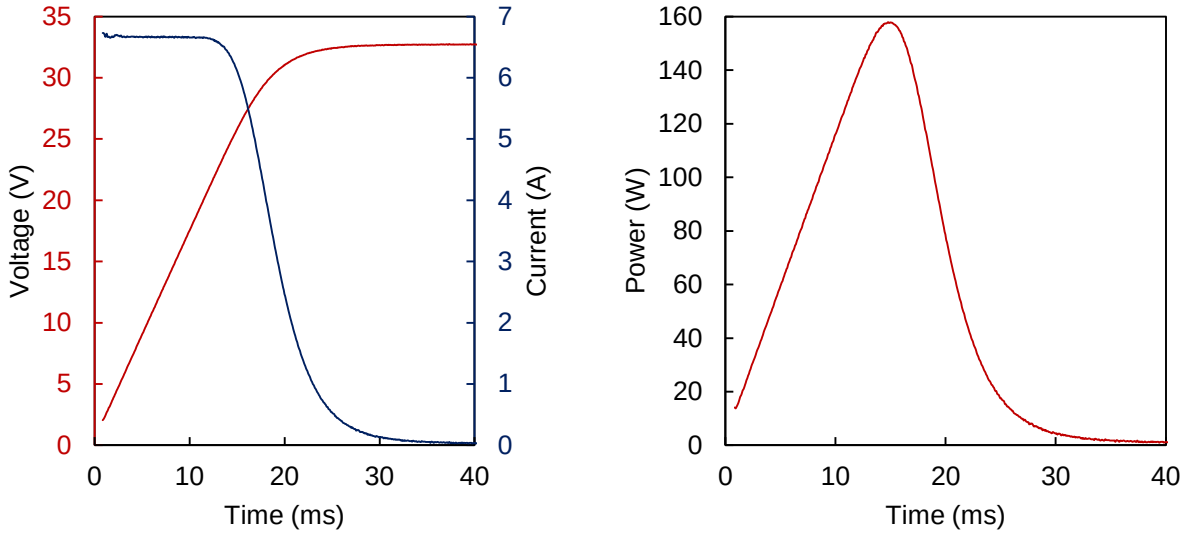

Figure 3.3: Measured voltage, current, and power vs. time curves of a capacitor charged with a PV module.

A photovoltaic module behaves like a constant current source nearly to the maximum power point at which it delivers its maximum power. When operated beyond the MPP, the PV output current begins to quickly drop and reaches zero at V_{oc}.

Assuming an ideal PV system that has a square output with current remaining constant and equal to I_{sc} up until V_{oc} (fill-factor of 1), the capacitor charge time can be calculated using Equation 3.3,

$$Q = I_{sc} \cdot t_{charge} = C \cdot V_{oc} \rightarrow t_{charge} = C \cdot \frac{V_{oc}}{I_{sc}} \tag{3.3}$$

where *Q* is the capacitor charge. For real conditions where the fill factor is much less than 1, the charge time in Equation 3.3 can be modified to include the charge slowing component (*FF*),

$$t_{charge} = \frac{C}{FF} \cdot \frac{V_{oc}}{I_{sc}} \tag{3.4}$$

The properties of the expected PV string properties, such as short-circuit current and open-circuit voltage, limit the type of switch (mechanical or electrical) and the methods to measure current and voltage (isolated vs. non-isolated). Finally, selecting a proper value for the load capacitor is important and poses challenges as outlined below.

The capacitor charge time in Equation 3.4 can be approximated with the following formula, which will be used throughout this chapter:

$$\mathrm{t_{charge}} \cong 1.5 \times \mathrm{C_{load}} \times \frac{\mathrm{V_{oc}}}{\mathrm{I_{sc}}} \tag{3.5}$$

where t_{charge} corresponds to charge time, C_{load} is the size of the load capacitor, V_{oc} is the open-circuit voltage and I_{sc} is the short-circuit current. The 1.5 correction term is inserted to compensate for the fill-factor of PV modules leading to a longer charge time when compared to a constant current source.

For instance, a photovoltaic array with an open-circuit of 300V and short-circuit current of 10A will charge a capacitive load of 4700 µF in just under 213 milliseconds. The same PV system under half the insolation levels will take twice as long to charge. For a similar system with an open-circuit voltage of 300V but short-circuit current of 1A, the load capacitor will charge in 2.1 seconds.

Table 3.3: Summary of various charge times using C_{load} = 4700µF for two PV systems.

Source	1A	5A	10A
PV Array (300V)	2115 ms	423 ms	212 ms
Single Module (37V)	261 ms	52 ms	26 ms

One the other hand, if a single photovoltaic module rated for V_{oc} = 37V and I_{sc} = 10A is tested with C_{load} = 4700 µF, the charge time will be as little as 26 milliseconds. For the same system with a 1A short-circuit current (assuming fixed voltage), the charge time will increase to 261 milliseconds. The summary of various charge time values for both systems is presented in Table 3.3.

As shown in Table 3.3, charge time variation depending on the source (i.e. single module vs. PV array), along with fluctuations of solar insolation, makes charge times hard to predict with a degree of certainty. It must also be kept in mind that charge times should be high enough to overcome the internal capacitance of large panels and strings, but not too high to prevent operating conditions from changing during measurements [50]. Therefore, it would be advisable to have a smaller capacitor value for large strings (where the open-circuit voltage to short-circuit ratio is higher), and a higher capacitor value for single panel measurements (where the open-circuit voltage to short-circuit current ratio is relatively smaller). This poses challenges in creating a single device that allows for making I-V curve measurements at all possible operating scenarios with a single capacitive load bank.

The proposed solution to this problem is to have two different capacitor values for the two different applications. Generation 1 and Generation 1.5 devices are designed for string-level measurements, and the capacitor value was optimized to allow for reliable string level I-V curve

measurements. Generation 2 was designed for both string-level and module-level measurements; and since tests were performed on module-level measurements, the capacitor was sized accordingly.

3.2. Generation 1: I-V Curve Tracer Using Mechanical Switches

3.2.1. Introduction

The Generation 1 I-V curve tracer was built as a proof of concept to test the feasibility of making accurate I-V measurements of PV arrays rated up to 450V and 10A (switch limitation). The curve tracer makes use of mechanical switches to allow the charging and discharging of the load capacitor and the load capacitor is discharged through the use of high power discharge resistors.

3.2.2. Circuit Construction

The schematic of the first generation curve tracer is shown in Figure 3.4. The circuit consists of the *J1* connector used to connect the PV system to the device, *J2* connector to connect a capacitive load, *RLY1* charge relay, *RLY2* discharge relay, *LED1* and *LED2* to indicate if the relay is on, led current limiting resistors *R.LED1* and *R.LED2*, *D1*, *Z1* and *D2*, *Z2* regular and Zener diodes used to allow the relay coil to discharge when off. The switching action is performed via *CHARGE* and *DISCHARGE* signals, which pass a current through the input of the Fairchild 4N35 optoisolators (*U1* and *U2*) designed to protect the outputs of the Atmel ATMEGA328P microcontroller used to run the curve tracer algorithm via optical isolation. The LED current of the isolator drives the output transistor, which is connected to *TR11*, *TR12* and *TR21*, *TR22* (Fairchild 2N5551) operating in a Darlington pair configuration to multiply the output current gain of the switch. PV system and capacitor voltages are measured through

resistive voltage dividers *R1*, *R_PV* and *R2*, *R_CAP*. *R_PV* and *R_CAP* (IRC GS-3-100-1003-F-LF) are rated for 100kΩ and 3W. With the resistor divider ratio of 101, the maximum measurable voltage is 505V with a resolution of 0.5V/bit.

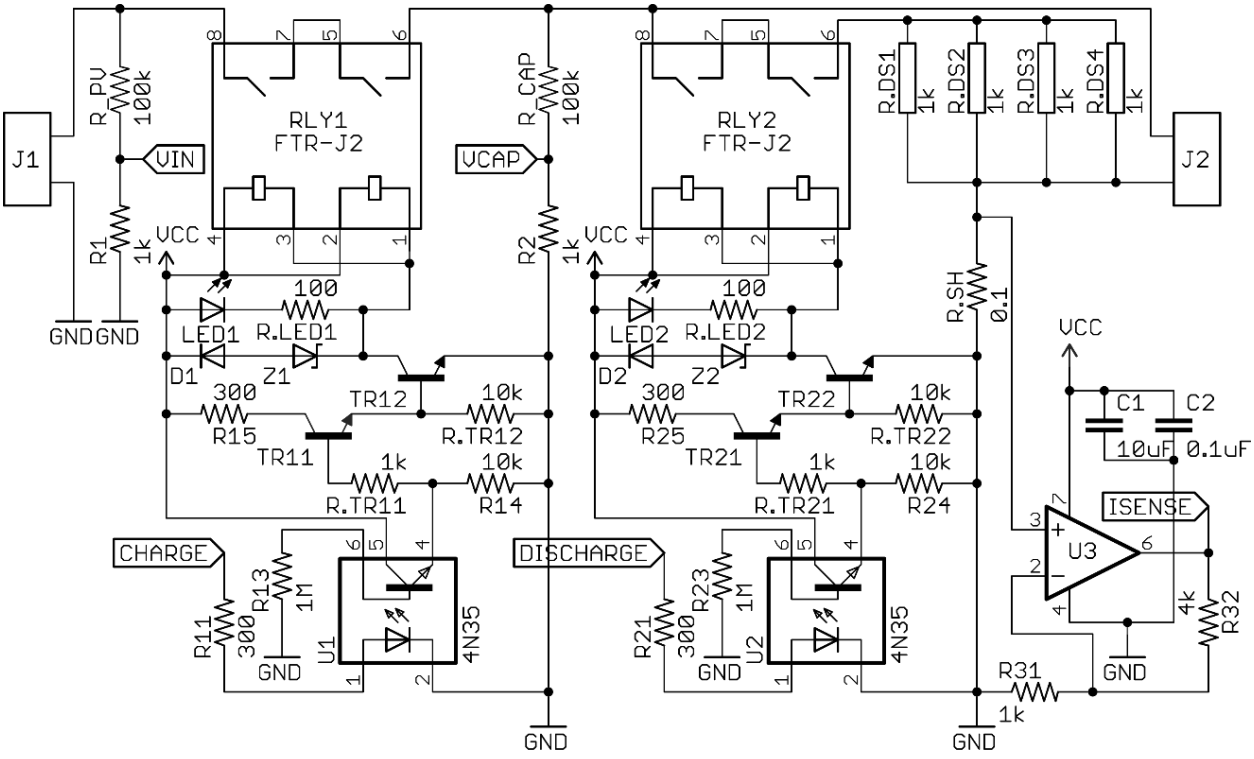

Figure 3.4: Schematic of the first generation I-V curve tracer.

The current is measured through a small series shunt resistor *R.SH* and the voltage drop across the resistor is multiplied using a Texas Instruments OPA350 operational amplifier set to non-inverting configuration with a gain of 5, with gain equaling (*R32*/*R31* + 1). The gain is user selectable by replacing resistor *R32*. With 5x gain, the maximum measurable current is 10A and the current resolution is 9.8mA/bit. Discharge of the load capacitor is accomplished by the use of 4 high power resistors *R.DS1-4* rated f 1kΩ and 100W (Ohmite TEH100M1K00JE). The board

layout of the curve tracer is shown in Figure 3.5.

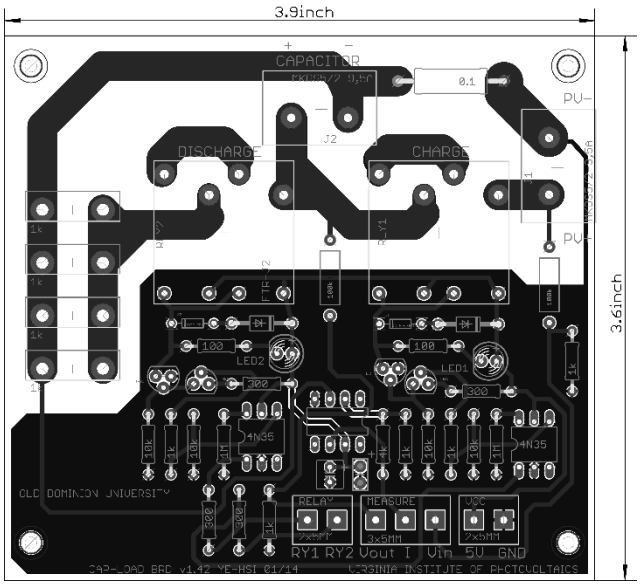

Figure 3.5: First generation I-V curve tracer board.

The I-V curve tracer, as shown in Figure 3.6, was constructed on a PC board measuring 3.90” x 3.60” (99 x 92 mm^2) with a height of 1.25” (30 mm) and volume of 17.55 cubic inches (287.6cm^3), excluding capacitors, which makes it extremely portable for field applications. The capacitors are connected at the green connector shown on top center, and can be externally optimized to lower weight and volume. The maximum string values supported are 450V and 10A, or 4.5 kW.

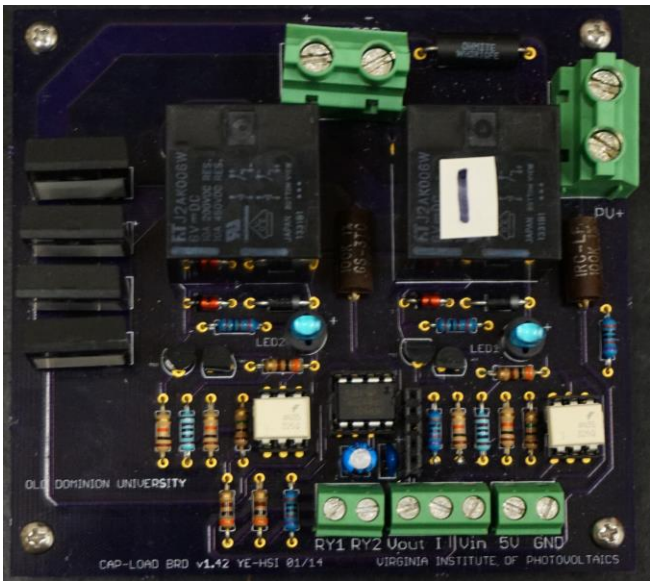

Figure 3.6: Photograph of the populated first generation I-V curve tracer.

3.2.3. Experimental Results and Discussion

Experimental results taken on January 13 of 2014 are shown in Figure 3.7.

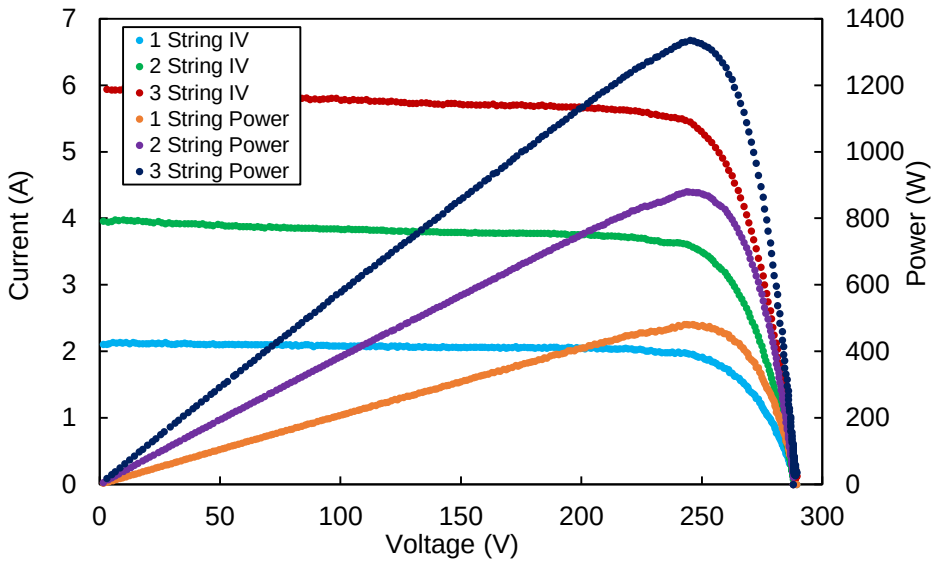

Figure 3.7: Measured I-V and P-V curves for 1, 2, and 3 strings under 25% illumination.

At AM1.5 (1000 W/m^2) the strings are rated for an open-circuit voltage of 300V and a short-circuit current of 8.61A each; however, due to lower insolation levels in winter, measurements of 1, 2, and 3 PV strings together were possible through a combiner box built in-house that allows for string monitoring and testing. As shown in Figure 3.7, the curves are very smooth and exhibit very little noise when current is at the levels indicated. No curve smoothing algorithms or electronics were in effect. The capacitor charge times were 786 ms, 400 ms, and 264 ms for 1-string, 2-string and 3-string measurements, respectively.

When current drops to under 2% of normal operation for AM1.5, the curves exhibit significantly more noise as shown in Figure 3.8. This is due to the low precision used in taking measurements that yield undesirable results in low light conditions. For given conditions, the capacitors took a considerably longer time to charge at 6.6 s, 4.4 s, and 2.4 seconds for 1-string, 2-string and 3-string measurements, respectively.

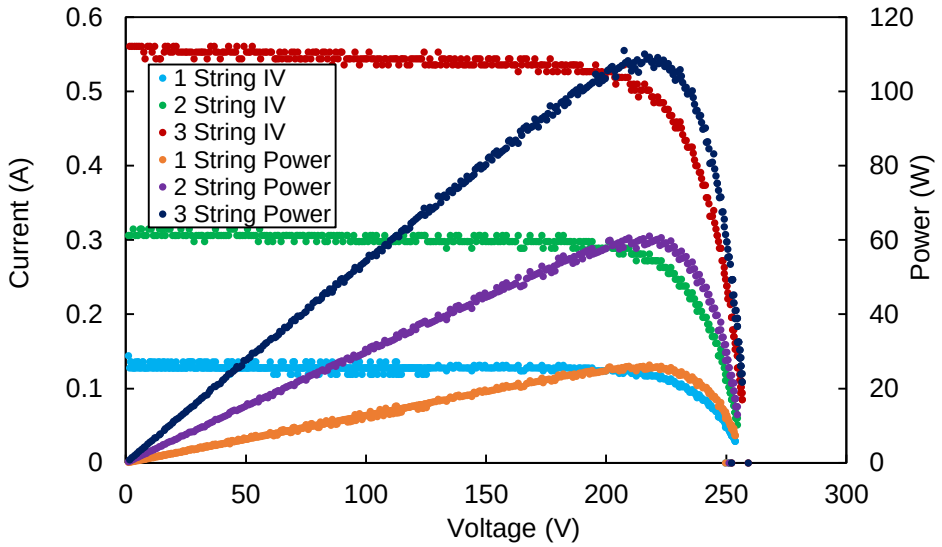

Figure 3.8: Measured I-V and P-V curves for 1-3 strings under 1.75% illumination.

Shown in Figure 3.9 are the results of the measurements taken at 50% illumination on January 15, 2014.

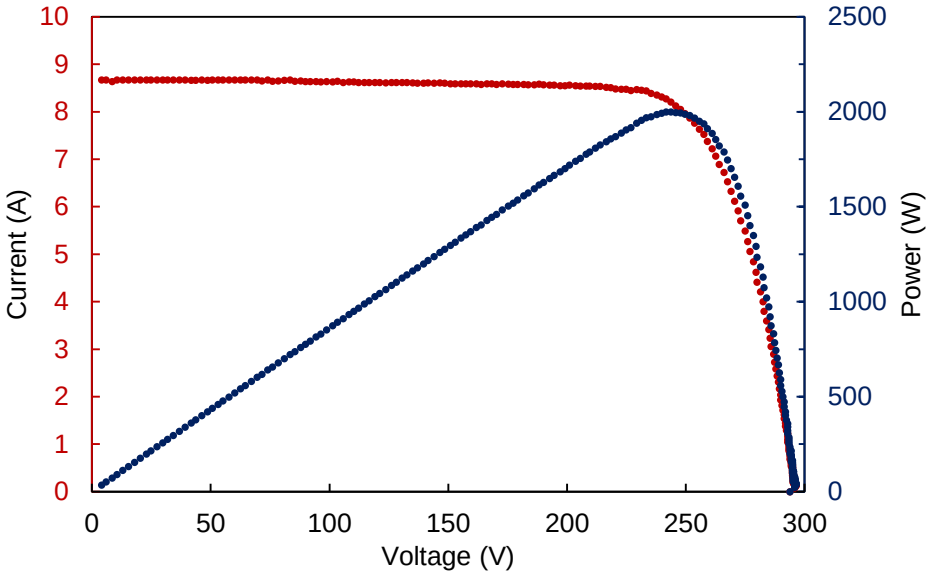

Figure 3.9: Measured I-V and P-V curves for 2 strings under 50% illumination.

The 2-string measurement exhibits the characteristics of a single-string measurement at one sun. This measurement is proof that the I-V curve tracer works remarkably well for the photovoltaic strings currently located at the Virginia Institute of Photovoltaics. With the proof-of-concept working, enhancements were made to generation 1 to improve performance and the number of recorded points.

3.3. Generation 1.5: Improvements to Generation 1

3.3.1. Introduction

After testing the first generation I-V curve tracer as a proof of concept, significant enhancements to the circuit were made in volume, parts count, and cost reduction. The measurement algorithm was optimized through the use of a more advanced microcontroller, allowing the storage of significantly more data points for each measurement. The majority of the signal level components were designed to use surface mount components, and the oversized discharge resistors were downsized in footprint, power rating and price.

3.3.2. Circuit Design

The improved curve tracer consists of a power circuit and a signal conditioning circuit. Details of the circuits are outlined in the sections below.

3.3.2.1. Power Circuit

The detailed schematic of the capacitive load is shown in Figure 3.10. The PV array is connected using connector *J1* on the left and the capacitor load is connected using *J2* on the right. The circuit comprises of two mechanical DC relays (Fujitsu FTR-J2) capable of switching 450VDC and 10A through a coil voltage of 5V (6V recommended). The first relay named *RLY1* is used to charge the capacitive load to V_{oc}. The second relay named *RLY2* is used to discharge the capacitive load to 0V.

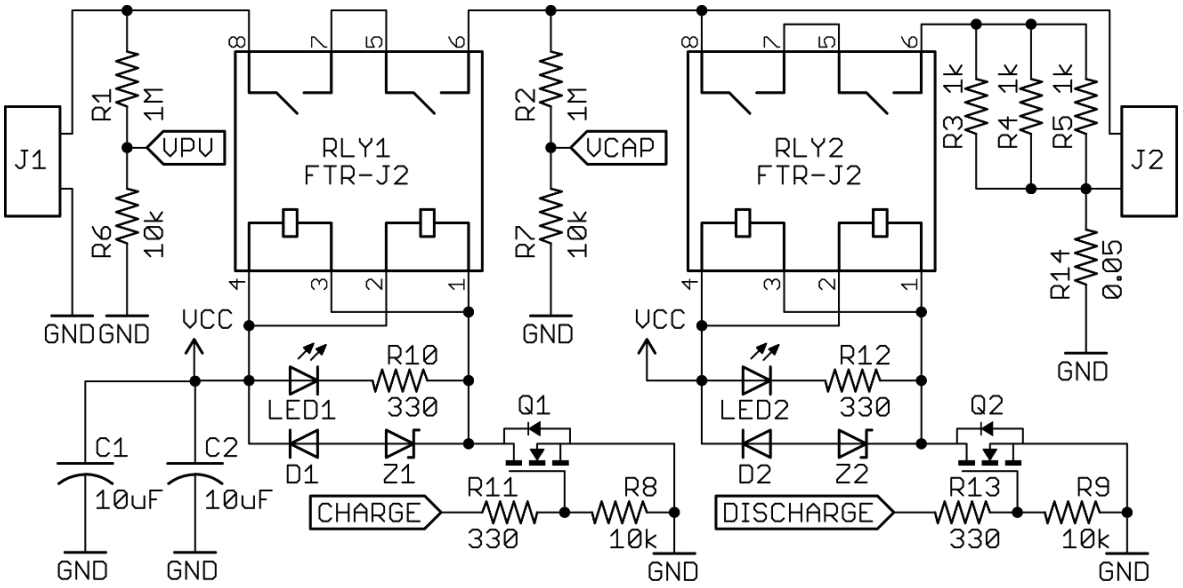

Figure 3.10: Schematic of the Generation 1.5 power circuit.

The discharge of the load capacitors is accomplished by the use of high power discharge resistors *R3, R4* and *R5*, each with a value of 1kΩ and a power rating of 35W, shown near *J2*.

The voltage of the PV array is measured using a voltage divider circuit comprising of resistors *R1* (1MΩ) and *R6* (10kΩ). Similarly, the voltage of the capacitor load is measured using resistors *R2* (1MΩ) and *R7* (10kΩ). Here, *R1* and *R2* are specially selected to have a high working voltage of up to 1600V.

The current is measured through a small series shunt resistor *R14* (0.05Ω) at the low side of the capacitor connection.

The signaling circuit for operating the charge relay (*RLY1*) comprises of *D1, LED1, Q1, R8, R10, R11, Z1, LED1* and *R10*. *LED1* is used to visually indicate relay operation and *R10* limits the current flowing through *LED1*. *D1* and *Z1* are used for freewheeling the relay coil. Since the relay coil stores energy in an inductive circuit, turning off the signal requires discharging the relay coil externally. Otherwise, the induced voltage at the coil terminals from

the magnetic field collapsing might damage the relay. A modified freewheeling diode circuit was chosen to clamp the relay coil voltage at nearly 24V using a blocking diode and Zener diode connected back to back. The increased voltage of a diode-Zener combination over a single blocking diode clamping at 0.7V allows for faster demagnetization of the coil and a quicker opening of the relay contacts, prolonging relay lifetime [82-83]. The *Q1* MOSFET is used to turn-on or turn-off the relay through a microcontroller output. The *R11* (330Ω) gate resistance is used to limit the MOSFET peak charge and discharge current to 15 mA, a value chosen to protect the general purpose output pin of the microcontroller. Resistor *R8* is used as a pull-down resistor on the gate to prevent the MOSFET from parasitically turning-on. This circuit is duplicated for the discharge relay (*RLY2*) circuit.

The relays are each signaled through connector *J3* (not shown) with an active current draw of 150 mA. The sudden action of the relay coils can cause voltage disturbance at V_{cc} during relay switching, therefore necessitating 10µF capacitors *C1* and *C2* placed very close to the relay contacts. Noise immunity could be further improved with the use of ferrite beads at the relay coils.

3.3.2.2. Signal Conditioning Circuit

Signal conditioning of the measured voltages and current (Fig. 3.11) were performed using *U1*, a Texas Instruments OPA4350 4-channel operational amplifier. This amplifier was chosen for its high bandwidth (38MHz), high slew rate (22V/µs), rail-to rail input and output, low input offset voltage (±150µV), and low input bias current (±0.5pA). The decoupling capacitors *C3*, *C4* (0.1 µF) are connected at the V_{cc} terminal.

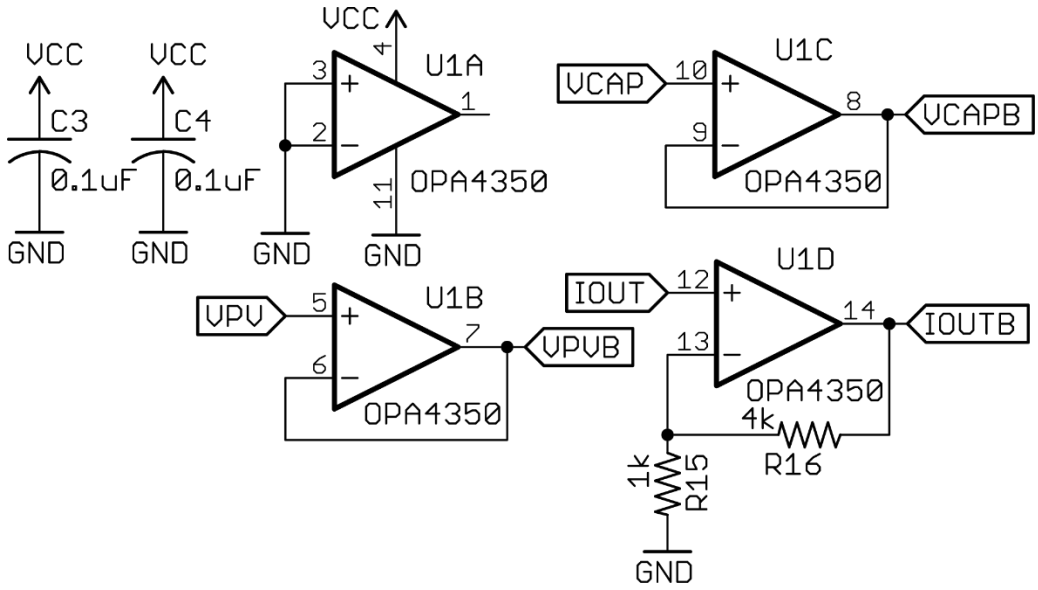

Figure 3.11: Schematic of the signal conditioning circuit.

Channel A of the operational amplifier (*U1A*) remains unused and the inputs were connected to ground to reduce noise interference between the four channels.

Channels B and C of the operational amplifier (*U1B* and *U1C*) are connected to the voltage dividers of the PV array voltage V_{pv} and capacitor load voltage V_{cap}, respectively. Channels B and C are configured in a non-inverting unity gain configuration to convert the high impedance input to a low impedance output (signal buffer).

The PV current is measured through channel D of the operational amplifier (*U1D*). The current flowing through resistor *R14* creates a small voltage drop that allows for measuring the PV current. This voltage is then amplified using a non-inverting configuration with a gain of 5.

All buffered values of V_{pvb}, V_{capb}, and I_{outb} (connection via *J5*) are connected to the analog-to-digital (ADC) inputs of an Arduino MEGA 2560 development board, which utilizes an ATmega2560 microcontroller running at 5V operating voltage and 16 MHz clock speed.

The built-in ADC inputs of the microcontroller convert voltages ranging between 0-5V to 0-1023 bits at 10-bit resolution (1024 unique values). The large memory of the microcontroller allows storing 1600 unique measurement points.

In order to best utilize the full range of the ADCs the value of the voltage divider resistors is critical. With the selection of resistor divider ratios of 101, it is possible for the curve tracer to measure the voltage of PV arrays with an open-circuit voltage of up to 505V. A voltage margin of 55V was imposed over the maximum operating voltage of 450V to properly trigger an overvoltage condition. The voltage resolution of the curve tracer, i.e. the difference between two consecutive bits of the ADC conversion is 493.6mV.

The largest measurable current is a function of the voltage drop across the current shunt resistor and the operational amplifier gain, which results in a maximum measurable current of 20A, allowing the curve tracer to be used with systems up to 20A of short-circuit current. The current resolution is therefore 19.6mA; however, the nonlinearity of the circuit limits current measurements up to 10A.

The power circuit, signal conditioning circuit, and microcontroller circuit, run off a 5VDC supply (*J4*). In order to do so, either USB power, a DC voltage adapter (9V), or a 5V supply can be used. USB power is not recommended as the bus voltage is imprecise and can vary between 4.75V and 5.25V, which causes errors in the ADC converter due to the incorrect 5V reference. All power circuit components are listed in Table 3.4.

Table 3.4: Bill of materials of the Generation 1.5 curve tracer.

Name	Description	Value
C1,C2	SMD capacitor, GRM319R61E106KA12D	10µF,25V
C3,C4	SMD capacitor, C1206C104K5RAC7867	0.1µF,50V
D1,D2	High speed diode, LL4148-GS18	75V,300mA, t_{rr}:4ns
J1, J2	High power connector, MKDS 5/2-9,5	600V, 32A
J3,J4	Power and relay connectors, ED555/2DS	2 position
J5	Voltage and current connectors,ED555/3DS	3 position
LED1, LED2	Chip LED, APTD3216SECK	Orange,1000mcd
Microcontroller	Arduino MEGA 2560	ATmega2560
Q1, Q2	Signal MOSFET, 2N7002P,215	60V,0.36A
R1, R2	High voltage resistor, RNV14FAL1M00	1MΩ,1600V
R3, R4, R5	High power resistor, PF2203-1KF1	1kΩ,35W, TO-220
R6, R7, R8, R9	Chip resistor, RC1206JR-0710KL	10kΩ, 5%
R10, R11, R12, R13	Chip resistor, RC1206JR-07330RL	330Ω, 5%
R14	Current shunt resistor, LVR01R0500FE70	0.05Ω, 1W
R15	Chip resistor, RC1206FR-071KL	1kΩ, 1%
R16	Chip resistor, RC1206FR-074K02L	4.02kΩ, 1%
RLY1, RLY2	High power DC relay, Fujitsu FTR-J2AK006W	450VDC,10A, 6V coil voltage
U1	Operational amplifier, OPA4350EA	38MHz,22V/µs
Z1, Z2	Zener diode, BZV55-C24,115	24V, 0.5W

3.3.2.3. Circuit Construction

The I-V curve tracer circuit shown in Figures 3.12 and 3.13 were constructed on a one-sided two-layer PC board measuring 2.73” x 1.93” (69.4 x 49.1 mm^2) with a height of 1.25” (31.8 mm), for a total volume of 6.6 cubic inches or 108.3 cm^3 (excluding capacitors), making it extremely portable for field applications.

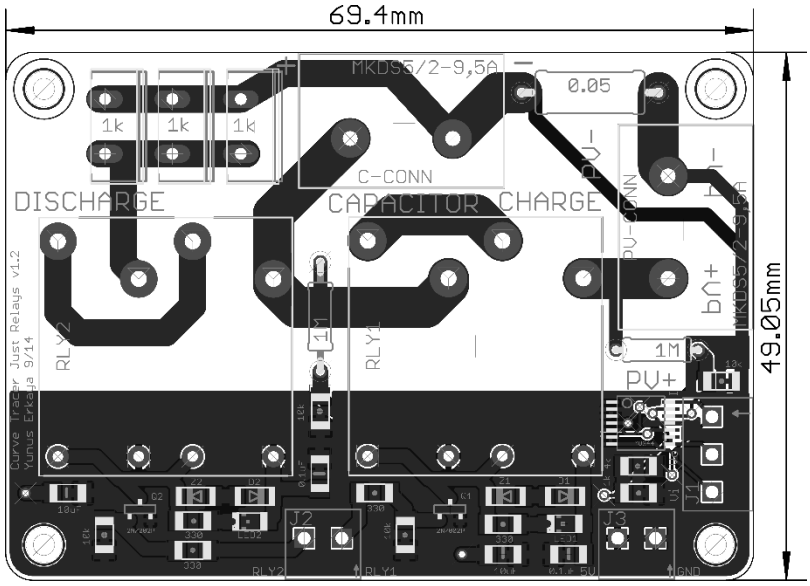

Figure 3.12: Generation 1.5 I-V Curve Tracer Board.

The capacitors are interchangeable through the green connection shown on top of Fig. 3.13, allowing the load to be adjusted to the PV system for optimized charge times, and leading to improvements in measurement performance. The maximum string values supported are 450V and 10A, or 4.5 kW. Measurements taken with the curve tracer are discussed in the following sections.

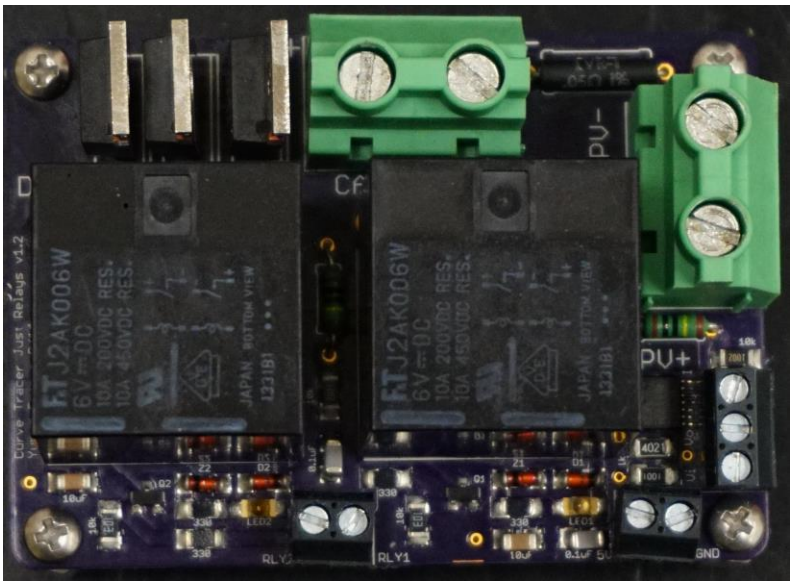

Figure 3.13: Photograph of the populated curve tracer.

3.3.2.4. Cost

Table 3.5 lists the costs of the curve tracer, where all components are priced for single quantities. The cost of the curve tracer board and its components adds up to $76.32, while the cost of the microcontroller and the largest value capacitors tested cost $45.95 and $61.30 respectively. In order to bring the costs further down, it is possible to purchase the components in bulk, especially the relays and the capacitors. The microcontroller can also be fully integrated into the same board to reduce the number of boards and interconnections. Prices quoted do not include an enclosure.

At a total cost of $183.57, the I-V curve tracer meets the design criteria of being low cost, especially for its high voltage and current capabilities.

Table 3.5: Component costs of the curve tracer.

Component	Cost per unit ($)
Capacitors (5x1000µF max)	61.30
C1, C2	0.48
C3, C4	0.20
D1, D2	0.28
J1, J2	2.96
J3, J4	1.36
J5	0.92
LED1, LED2	1.04
Microcontroller	45.95
Q1, Q2	0.28
R1, R2	0.52
R3, R4, R5	9.21
R6, R7, R8, R9	0.40
R10, R11, R12, R13	0.40
R14	1.77
R15	0.10
R16	0.10
RLY1, RLY2	36.00
U1	11.12
Z1, Z2	0.38
PCB	8.80
Total	**183.57**

3.3.3. Results and Discussion

3.3.3.1. Testing Procedure

The PV system we used for the testing procedure is situated on the roof of Old Dominion University's Kaufman Hall and consists of 3 strings of 8 series-connected Bosch c-Si M60 modules rated for 245W. The total string power is rated at 2kW and the total system is rated at

6kW. The inverters are wired so that every string has a dedicated inverter. This configuration allows us to test up to three strings individually or together.

In order to make tests possible, a switcher box was designed and assembled (Fig 3.14). The three green buttons allow for separately switching three different strings between the inverters (normally-closed) and a combiner bus inside the switching box (normally-open). The green buttons are connected to individual relays running at 24V. The buttons have a latching design and remain pressed-in when the PV string is diverted to the combiner bus. It is possible to combine up to three strings on this bus. The green LEDs indicate inverter connection and the red LEDs (not lit) indicate the combiner bus connection. The red emergency switch cuts power to the relays and forces the PV system to connect to the inverters. The black switch on the bottom right is for turning on the 24V supply to the relays. The PV system and the inverters are grounded within the switching box. The system is designed for a negative grounding configuration where the PV strings are grounded on the negative DC connection rather than the positive.

Figure 3.14: PV load switching enclosure.

When taking measurements, the biggest human and device safety factor is the quality of the ground connection. Since the I-V curve tracer is passive, costs were kept to a minimum with a non-isolated design, meaning that the negative power supply rail to the boards shares a connection with the negative wire of the PV string, and in some cases with the earth ground.

The curve tracer device requires a computer connection to transmit data. Data transmission can either be done through a terminal program, or through purpose-written software using Processing Language (Fig. 3.15). The use of a non-isolated USB cable may result in the PV system being grounded through the USB port of the computer even if power is drawn from a dedicated supply, requiring utmost care to the safety of the computer and the operator.

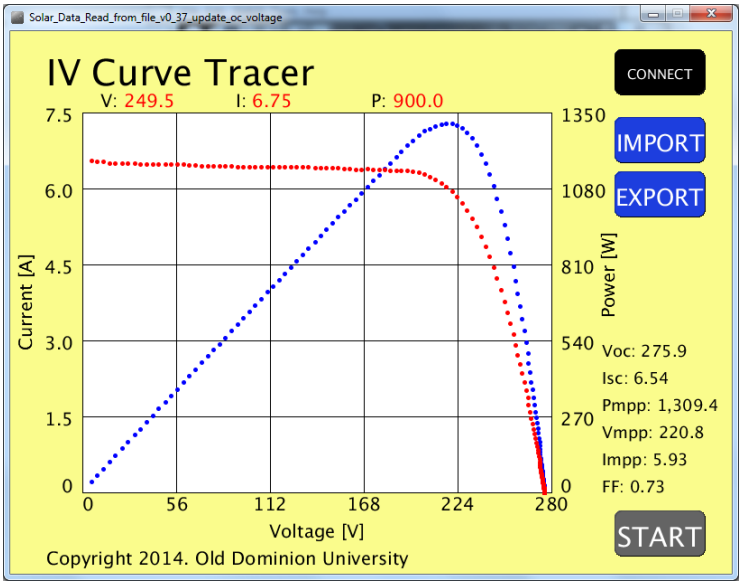

Figure 3.15: Custom IV Curve Tracer software.

The IV Curve Tracer software initializes communication over the USB-UART bridge with the microcontroller development board when the connect button is pressed. Once

connected, the start button becomes active. After the press of the start button, the curve tracer will run a test trace to capture the charge time t_{charge} and discharge time $t_{discharge}$ of the load capacitor, and the short-circuit current I_{sc} and open-circuit voltage V_{oc} of the PV array.

If suitable correlation exists between Eq. 3.5 and t_{charge}, the algorithm will use t_{charge} to time the measurement trace. In the current arrangement, the minimum measurement time t_{charge_min} for tracing 1600 points is 26 µs. Therefore, if t_{charge} is less than t_{charge_min} there will be fewer unique data points captured. If t_{charge} is greater than t_{charge_min}, a delay t_{delay} is calculated using Eq. 3.6 and rounded up to the nearest microsecond. This value is inserted between measurements to increase the measurement time to a value slightly higher than t_{charge} in order to fully capture the I-V curve.

$$\mathrm{t_{delay}} = \left\lceil \frac{\mathrm{t_{charge}} - t_{charge_{min}}}{1600} \right\rceil \tag{3.6}$$

If the correlation between t_{charge} and Eq. 3.5 is not good, i.e. charge times are much longer than expected due to shading or module mismatch, the circuit will use Eq. 3.5 to track the curve, which might result in some points near V_{oc} omitted (refer to Fig. 3.20). Finally, if any two points have equal current and voltage values, the duplicate data points are discarded.

3.3.3.2. Effect of Load Capacitor Size

The effect of different load capacitor values of 5000 µF, 1000 µF, and 680 µF on the resulting I-V curve of a single photovoltaic string is shown in Fig. 3.16.

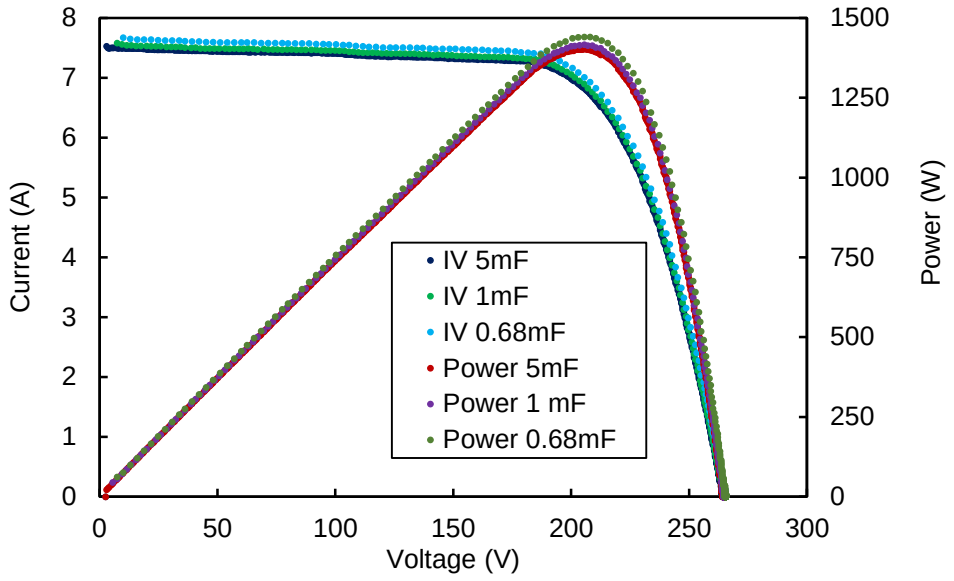

Figure 3.16: Measured effect of different capacitor values on I-V and P-V curves.

In this case, the smallest capacitance value performed equally well compared to others indicating that the I-V curve measurements are performed long enough to overcome the parasitic capacitances of the modules and short enough to have stable conditions.

As expected, since all charge times are above 20 ms (refer to Table 3.6), the effects of the capacitance of the PV array are negligible. An undesirable side effect of using large capacitors for the load is the increased stored energy leading to longer charge and discharge times and more energy dissipated in the discharge resistors. This could be a major speed bottleneck if fast successive measurements are desired, therefore the capacitor selection should be based on:

1. The highest expected open-circuit voltage, V_{oc_max},
2. The highest expected short-circuit current, I_{sc_max}, and
3. A capacitor size that will result in at least 20 ms charge time using Eq. 3.5.

Table 3.6: Capacitor charge and discharge times and measurement delay between points.

	680µF	1000µF	5000µF
Charge time	41.7 ms	57.6 ms	287.9 ms
Discharge time	919 ms	1348 ms	6621 ms
Measurement delay	10 µs	20 µs	163 µs
Minimum voltage	9.93 V	7.44 V	2.97 V

One critical point worth mentioning is the minimum measured voltage of the I-V curve. For larger load capacitor values, it is possible to capture data points at lower voltages when compared to small capacitors. This is due to the hard to synchronize nature of the charge relay switch-on time (imprecise), the measurement of the first point (usually before the relay closes) and the delay between the first point and the second point. Depending on the system size, the minimum voltage value might become a concern and the size of the capacitor load will have to be considered accordingly.

3.3.3.3. Effects of Shading

Shading tests were performed using the PV array (Fig. 3.17) to analyze the performance in shaded conditions. No shading, single shaded cell, single shaded panel, and two shaded module results are shown in Figures 3.18 to 3.21, respectively.

Figure 3.17: Shading arrangement for two shaded PV modules.

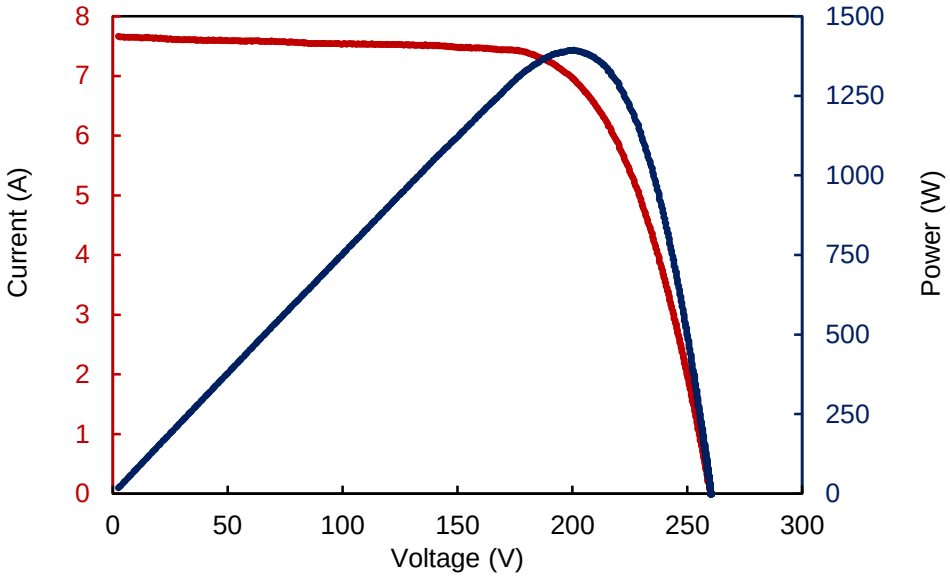

Figure 3.18: Measured I-V and P-V curves of an unshaded single string.

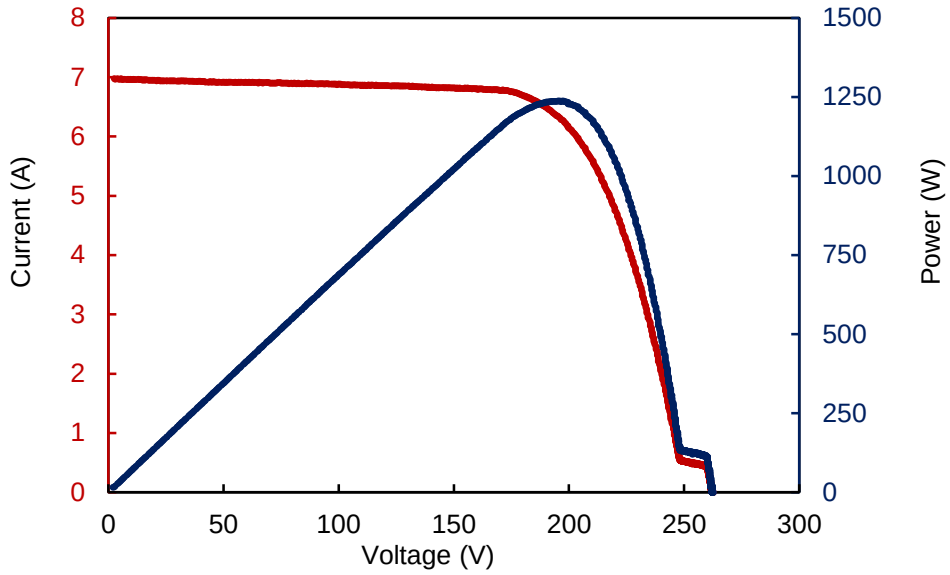

Figure 3.19: Measured I-V and P-V curves with a single shaded cell.

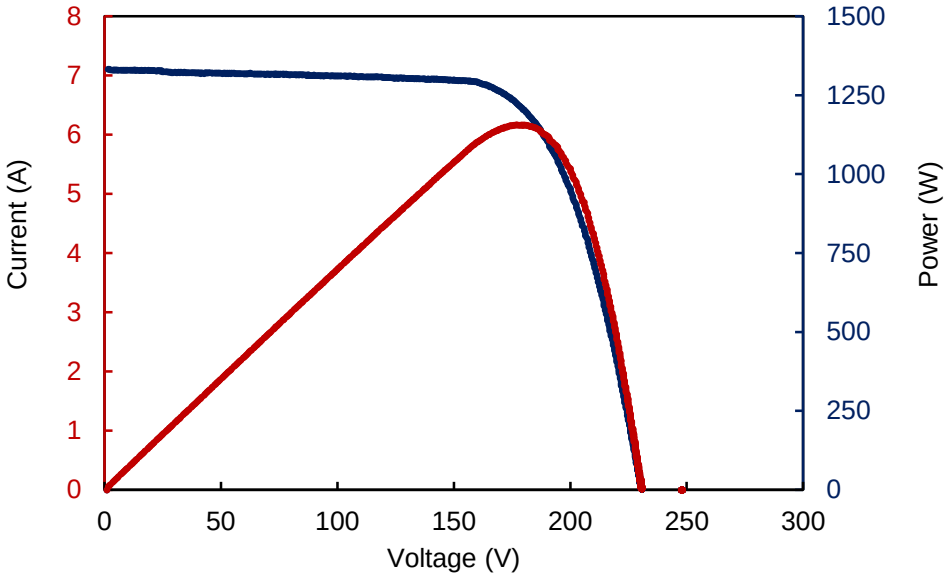

Figure 3.20: Measured I-V and P-V curves with a single shaded module.

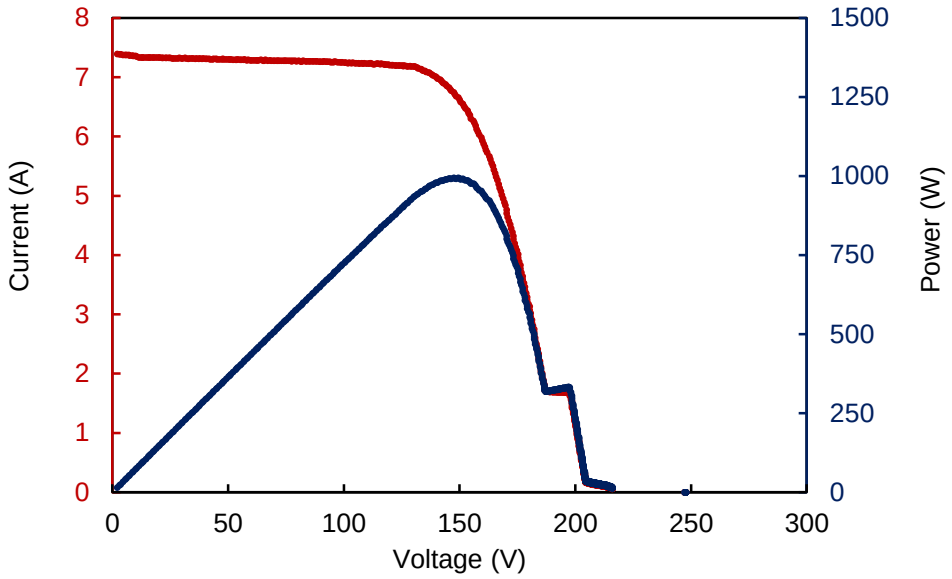

Figure 3.21: Measured I-V and P-V curves with two shaded modules.

When measuring shaded systems, Eq. 3.5 is not adequate because it does not take shading effects into account when used to predict charging times. Results show that for shaded and unshaded systems, the V_{oc} remained nearly the same (250V) (single data points can be seen in Figures 3.20 and 3.21), and this can be attributed to the large quantity of modules per string and the percentage of shaded modules being minimal. However, the shaded panels do not provide enough current to charge the capacitors quickly above a certain voltage. The I-V curve tracer algorithm was modified to trace the full I-V curve of a PV string with a single shaded panel by using the complete charge time required to charge the load capacitor to V_{oc}, and the results are shown in Figure 3.22.

Waiting for the PV array to actually charge the capacitors to the V_{oc} voltage lengthened the charge process by 50-80 times (20.8 seconds) for a single panel depending on the test. Data points with equal time spacing (13 ms delay between measurements) in Figure 3.22 illustrate that the charge time significantly increased at voltages above 220V. The low density of useful data

points results in an imprecise measurement.

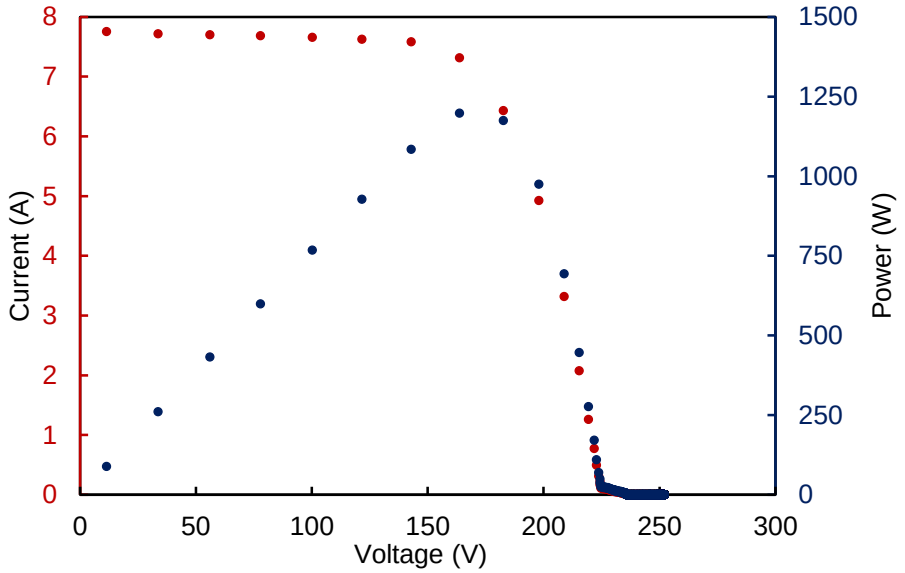

Figure 3.22: Measured I-V and P-V curves of a single string charged using Eq. 3.1 with a single shaded panel.

Therefore, it was concluded that even though Eq. 3.5 does not take shading effects into account, it can still be used in a reasonable matter to trace I-V curves of photovoltaic strings down to 1.5% illumination levels.

Figures 3.23 and 3.24 demonstrate the comparative outputs of the PV modules when unshaded, a single cell is shaded, a single module is shaded, and two modules are shaded. To simplify comparisons, all voltages are referenced to the V_{oc} taken during the measurement, resulting in voltage values ranging from 0 to 1. Similarly, the current values shown in Figure 3.23 are referenced to the individual I_{sc} per measurement and scaled between 0 and 1 on a per unit basis. The power values are the multiplication of the per unit values of voltage and current referenced to V_{oc} and I_{sc} respectively.

Figure 3.23 shows the effects of shading in which shading doesn't affect module performance near the I_{sc} region. However, there are significant current losses near the V_{oc} region which effect both the fill-factor (FF) and the power output of the modules, with:

$$FF = \frac{V_{mpp} \cdot I_{mpp}}{V_{oc} \cdot I_{sc}} \tag{3.7}$$

where V_{mpp} is the maximum power point voltage, I_{mpp} is the maximum power point current, and the maximum power point is the point at which the module power output is the highest.

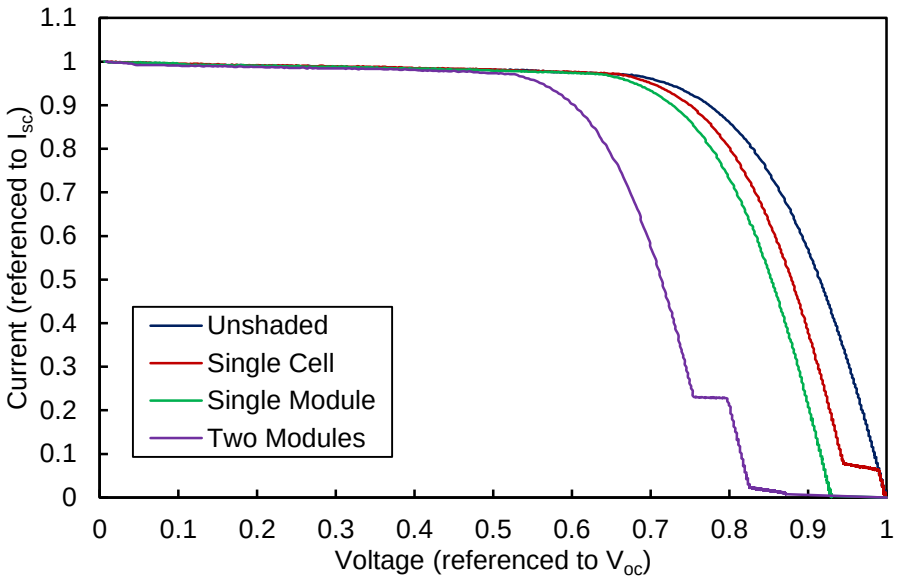

Figure 3.23: Comparison between the normalized measured I-V curves for unshaded, a single shaded cell, a single shaded module, and two shaded modules.

In Figure 3.24, the power outputs of the modules are compared, and the maximum power point (MPP) shifts toward lower voltages due to the loss of power at higher output voltages near V_{oc}. As expected, shadowing reduces system efficiency and creates local maxima that can severely affect the performance of MPPT algorithms.

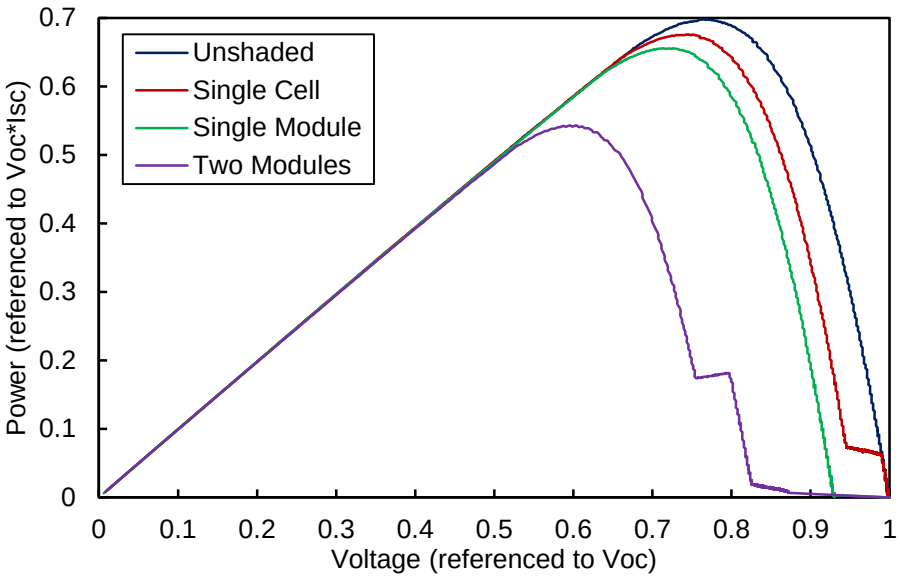

Figure 3.24: Comparison between the normalized measured P-V curves for unshaded, a single shaded cell, a single shaded module, and two shaded modules.

3.3.4. Conclusions

In conclusion, an effective and highly portable solution for measuring I-V curves of photovoltaic strings has been developed with the circuit details and measurement procedure explained in detail. The design provides significant improvements on the compactness and the cost of curve tracers when compared to examples shown in Chapter 1. The biggest limitation of the generation 1 and generation 1.5 curve tracers are the mechanical relays, especially in terms of cost, volume and reliability. In order to improve the voltage rating and the current rating of the I-V curve tracer circuit, the mechanical relays will have to be replaced with electronic switches.

3.4. Generation 2: I-V Curve Tracer Using Solid State Switches

The reliance on mechanical switches in generations 1 and 1.5 made these units not very reliable in terms of drop rating and switch lifetime. For improved reliability, the mechanical

switches have to be replaced with electronic switches. The price of the relays at nearly $20 each was also a concern in optimizing costs.

The list of improvements made to generations 1 and 1.5 in generation 2 are shown below:

1. Compactness: fits in the palm of hand, and is very light weight,
2. Costs: low cost and low parts count,
3. Accuracy: high linearity, low noise, high resolution,
4. Reliability: tens of thousands of measurements, operation at elevated temperatures outdoors (nearly automotive grade) and drop rated (unlike mechanical relays), and
5. Modularity: 100V and 600V configurations (previously only 450V value)

3.4.1 Circuit Construction

The second generation I-V curve tracer consists of five circuits: the power circuit, the temperature and irradiance measurement circuit, the irradiance monitor circuit, the MOSFET switching circuit and the microcontroller circuit.

3.4.1.1 Power Circuit

In order to keep costs low and the size of the circuit board small, the circuit was designed to have the fewest number of components possible. There are two connectors, one for the PV module (*J1*), and one for the capacitor bank (*J2*). There are two switches consisting of N-channel MOSFETs to charge (*Q1*) and discharge (*Q2*) the capacitive load. Two power resistors in parallel (*R6*, *R7*) discharge the capacitor load. Voltage is measured through two series voltage dividers (R1-R4) at the capacitor and at the PV module, allowing the circuit to sense complete capacitor discharge.

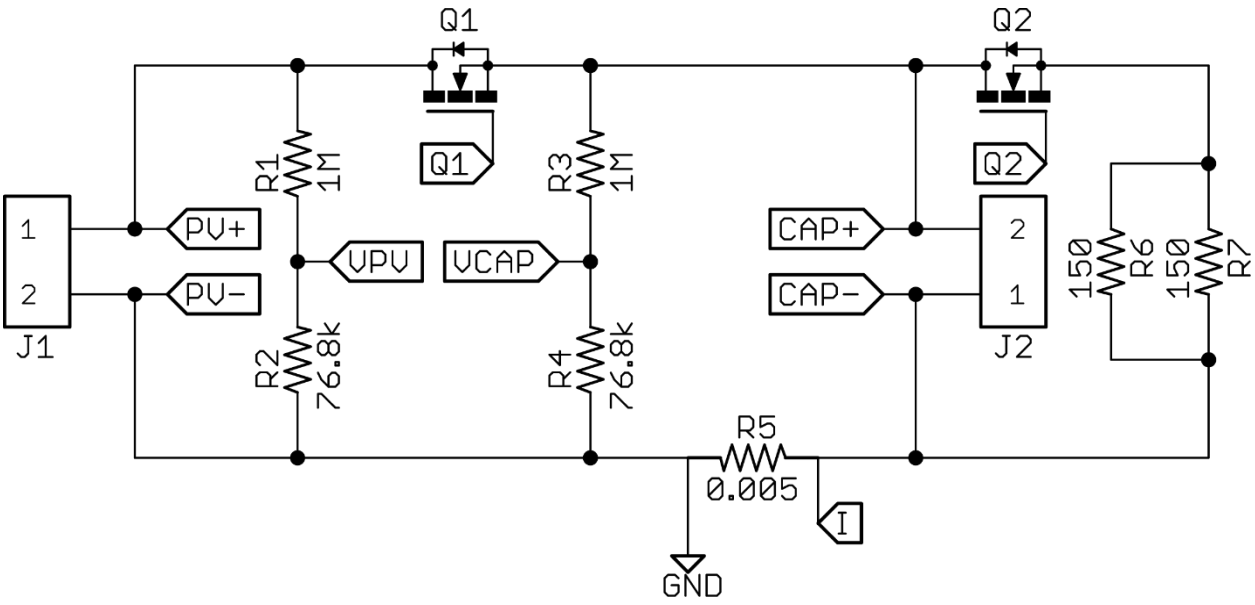

Figure 3.25: Power circuit schematic.

Table 3.7: Power circuit components.

Part	Description	Value
J1, J2	Connector, Phoenix Contact MKDS 5/2-9,5	600V/30A, 9.52 mm
Q1, Q2	N-channel MOSFET, STP24NF10	100V/26A, TO-220-3
R1, R3	High voltage resistor, RNV14FAL1M00	1MΩ, 1%, 1600VDC
R2, R4	Voltage measurement resistor, RC0603FR-0776K8L	76.8kΩ, 1%
R5	Current measurement resistor, WSK25125L000FEA	5mΩ, 1%, 1W, 35ppm/°C
R6, R7	Capacitor discharge power resistor, PF2203-150RF1	150Ω, 35W

Current is measured through a series shunt resistor (R5) with a very small value to capture the current as precisely and as linearly as possible. Due to the reduced parts count, the circuit does not offer reverse polarity protection. If the PV modules were to be connected in

reverse, the capacitor might be damaged and the parasitic body diode of *Q1* and *Q2* will conduct the short-circuit current of the PV system. The device is powered by a single 9V battery but it could also be powered by a rechargeable battery such as Li-ion or Li-polymer.

Both voltage measurements are buffered through operational amplifiers with a unity gain configuration. Current is measured through the series shunt resistor on the return path of the circuit, defining the measurement as a low-side current-measurement that is insensitive to the PV module voltage. The common-mode voltage can be neglected because the voltage drop across the resistor is at most 100 mV at 20A short-circuit current, the maximum current the circuit was designed to measure, which can be further increased by tweaking the series resistance and operational amplifier gain values. The operational amplifier that sets the gain of the current measurement is configured for non-inverting operation with a gain of 33x.

3.4.1.2. Irradiance and Temperature Measurement Circuit

Besides measuring voltage and current, the circuit also performs measurements of temperature and irradiance. A decision was made to keep the I-V circuit analyzer board fully analog without any digital components introducing unnecessary noise. Therefore, temperature is measured using a combination of a reference voltage of 0.1V, a thermocouple IC with an analog output (AD8495), and an operational amplifier connected in non-inverting mode with a gain of 6.6x. This setup allows for measurements between -20°C and +80°C using a type-K thermocouple that can be mounted to the back-side of the PV module under test. The equation to calculate the temperature output is given in the ADC8495 datasheet as,

$$T_{MJ} = (V_{OUT} - V_{REF})/(5mV/℃) \tag{3.8}$$

The components of the circuit are shown in Table 3.8 and the circuit schematic is shown in Figure 3.26.

Table 3.8: Temperature and irradiance measurement circuit components.

Component	Description	Characteristics
C11,C19,C15	Capacitor, GRM188R71E104KA01D	0.1 µF, 10 V, X7R
C16,C17	Capacitor, GRM188R71E103KA01D	10 nF, 25 V, X7R
R15,R18,R19	Resistor, RC0603FR-0710KL	10 kΩ, 1%
R16	Resistor, RC0603FR-0756KL	56 kΩ, 1%
R17	Resistor, CRCW06031M00FKEA	1 MΩ, 1%
R20	Resistor, RC0603FR-077K5L	7.5 kΩ, 1%
R21	Resistor, RC0603FR-07240KL	240 kΩ, 1%
U5, U6	Operational Amplifier, MAX4238AUT	0.1 µV offset, 1 pA input bias
U7	Thermocouple IC, AD8495ARMZ	Type K, analog output (5mV/°C)

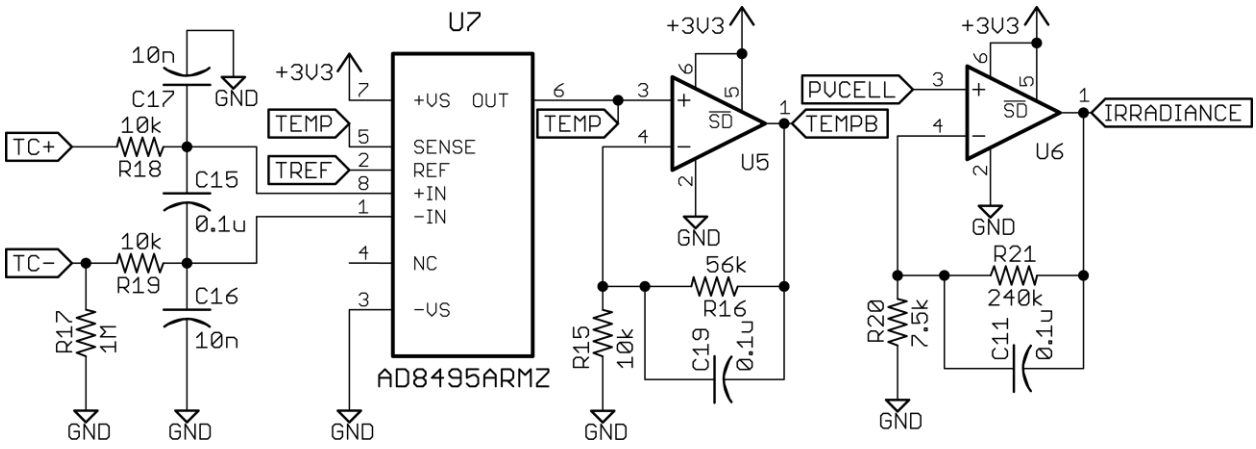

Figure 3.26: Temperature and irradiance measurement schematic.

The power circuit and irradiance and temperature circuit were designed together on the same PCB (Figures 3.27 and 3.28) with dimensions of 43 x 60.2mm^2 and a height of 25mm for a total volume of 64.7cm^3, achieving significant compactness when compared with the Generation

1 (287.6cm^3) and Generation 1.5 (108.3cm^3) I-V curve tracers.

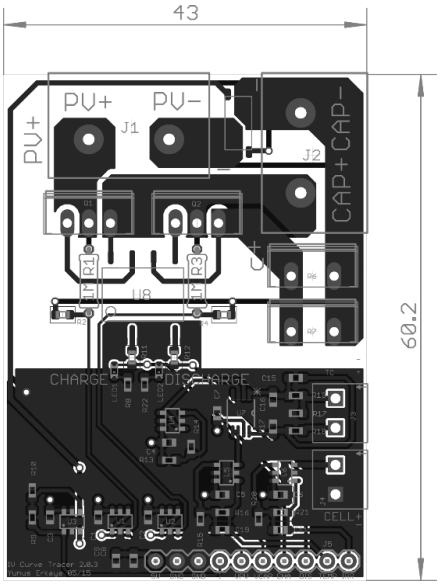

Figure 3.27: I-V curve tracer board (dimensions are in mm).

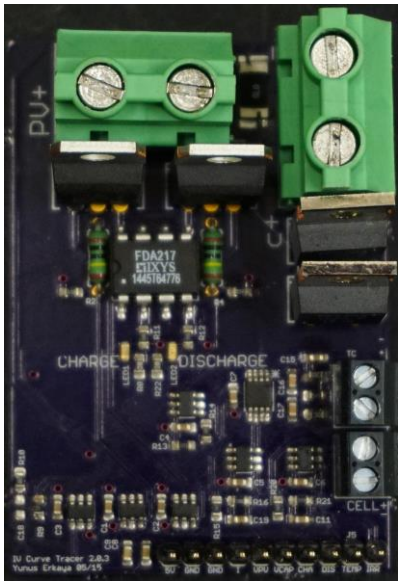

Figure 3.28: I-V curve tracer circuit board after assembly.

3.4.1.3. Irradiance Monitor Circuit

For measurements of irradiance, a separate board was designed containing four small mono-crystalline silicon (c-Si) solar cells connected in parallel to have a short-circuit current of 200 mA at 1 sun as shown in Figure 3.29. The short-circuit current is converted into a "short-circuit voltage" through a 0.25Ω shunt-resistor leading to a 50 mV voltage value at 1 sun. This voltage is then scaled up using an operational amplifier with a non-inverting configuration set to 33x gain allowing the irradiance board to measure irradiance up to 2 suns. The output of the irradiance monitor board connects with the irradiance input of the temperature and irradiance measurement circuit. The components of irradiance board are listed in Table 3.9.

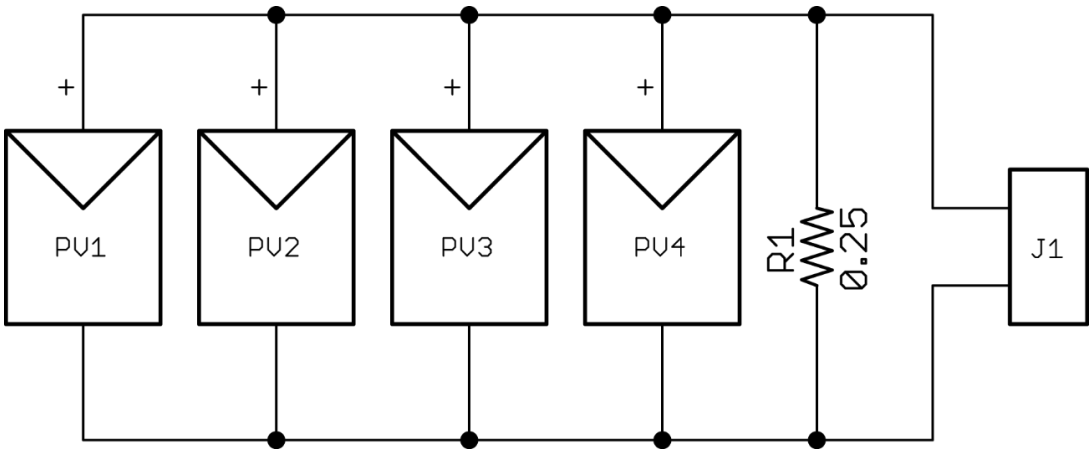

Figure 3.29: Schematic of the irradiance monitor PCB.

Table 3.9: Irradiance measurement board circuit components.

Part	Description	Value
J1	Connector, On Shore Tech. ED555/2DS	150V, 6A, 3.5 mm
PV1,PV2,PV3,PV4	Solar cell, IXYS KXOB22-12X1L	0.63V, 50mA
R1	Resistor, CSR0603FKR250	0.25Ω, 1%

With measurements of just 22 x 36.5 mm^2, it is possible to attach the irradiance monitor board to the frame of the latest generation high power PV modules without shading the device, and guaranteeing the correct plane of measurement for the irradiance measurement. The board design in shown in Figure 3.30.

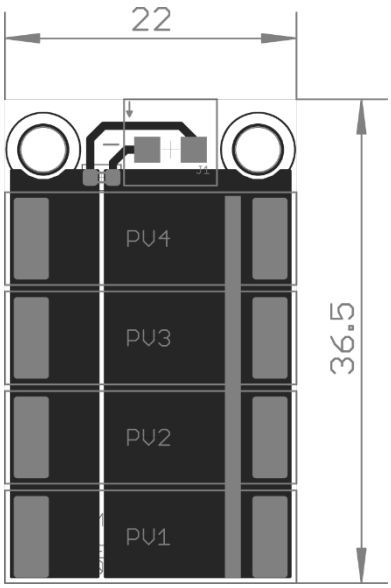

Figure 3.30: Irradiance monitor board (dimensions are in mm).

3.4.1.4. MOSFET Switching Circuit

The switching operation of this circuit is where there has been tremendous amount of research in minimizing components and keeping the switches safe and the rest of the circuit away from high voltages. With many options available in the market, a solution that did not require an additional voltage rail or many additional components associated with charge-pumping circuit was found. The solution revolves around the operational principle of solid-state relays. Solid-state relays embed a light-emitting diode and photovoltaic coupling circuit for the

switching operation. When a signal is applied, the LED is illuminated and the light absorbed by the photovoltaic cell turns the low-level input current into a voltage high enough to turn MOSFETs on. Most solid-state relays have a few MOSFETs in series in order to block AC or reverse DC voltages. In order to keep costs low and the circuit simple, a simplified solid-state relay was built with a FDA217 dual photovoltaic MOSFET driver from IXYS introduced in January 2014. This IC, rated for 3750 V_{dc} isolation voltage, having two parallel outputs, allows the control of two switches with a single IC with just two current limiting resistors at the input, which minimizes component counts, costs and PCB footprint. The single negative aspect of using such a circuit topology is that while MOSFET turn off is very fast, MOSFET turn on is quite slow (1-2ms) and is dependent on the input current of the FDA217, the specific MOSFET used, and the open-circuit voltage of the PV module under test.

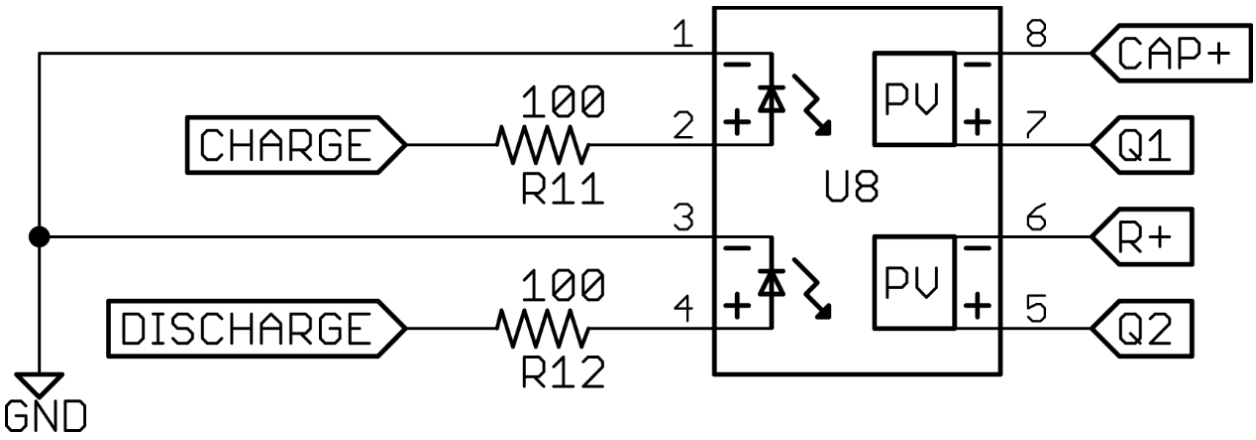

Figure 3.31: MOSFET switching circuit.

There are two simple ways of improving the MOSFET turn-on time, if necessary. These are (1) by increasing the control current of the FDA217, or (2) by paralleling the outputs of the

FDA217. Increasing the control current can be accomplished by using MOSFETs to control the input side of the FDA217, which can increase the input control current to a rated 50 mA, as opposed to the 25 mA limitation from the microcontroller general purpose output pin, or add an additional charge-pumping circuitry that can inject 1A of current within 10 ms to have extremely fast turn-on times. The second approach would be to use the dual outputs in parallel to double the output current to halve the MOSFET turn-on time.

Both solutions come at the expense of increased component count, cost, and PCB footprint and, so far, tests show that with a large enough capacitor used as a load, the slow turn-on does not have much of an effect when measuring a single 245 W PV module rated to less than 40V open-circuit voltage. For small capacitor values, it is practically impossible to measure points near zero volts due to the parasitic charging that occurs during MOSFET turn-on. Large arrays with multiple PV modules connected in series will have a higher voltage, and a smaller capacitor would be able to capture a higher percentage of the voltage sweep when compared to systems with a smaller voltage.

Higher PV module voltages and higher PV module currents make proper MOSFET selection important, as they will increase the switching losses at the MOSFET. MOSFET selection when used as a switch is very critical in terms of break down voltage (V_{DS}), packaging, on-state resistance ($R_{DS,on}$), gate charge (Q_g), and cost. The voltage rating of the MOSFET should be higher than the PV module with some headroom to keep the MOSFET from breaking down. The packaging should allow the MOSFET to dissipate the switching and conduction energy into the ambient and should be small and compact to reduce PCB footprint. The on-state resistance should be as low as possible for the measurements to begin near 0V at short-circuit current, with the ideal minimum measurable voltage being,

$$V_{minimum} = I_{sc} \cdot R_{DS,on} \tag{3.9}$$

With an I_{sc} value of 10 A and $R_{DS,on}$ value of 0.1 Ω the minimum measurable voltage is 1 V assuming ideal conditions. This may not be a problem when measuring many PV modules configured in a series array; however, measurements of a single module or even just a single cell become very challenging as the minimum measurable voltage becomes a higher percentage of the open-circuit voltage.

The gate charge of the MOSFET determines how fast the MOSFET can switch on or off. Since switch-off is performed at V_{oc} with no current flowing, turn-off losses can be ignored. Unfortunately, it is not the same story with MOSFET turn-on.

When a positive voltage is applied between the MOSFET gate and source terminals (V_{GS}), charge will flow into the MOSFET and begin to charge the MOSFET capacitance between gate and source (C_{GS}) (shown in Figure 3.32).

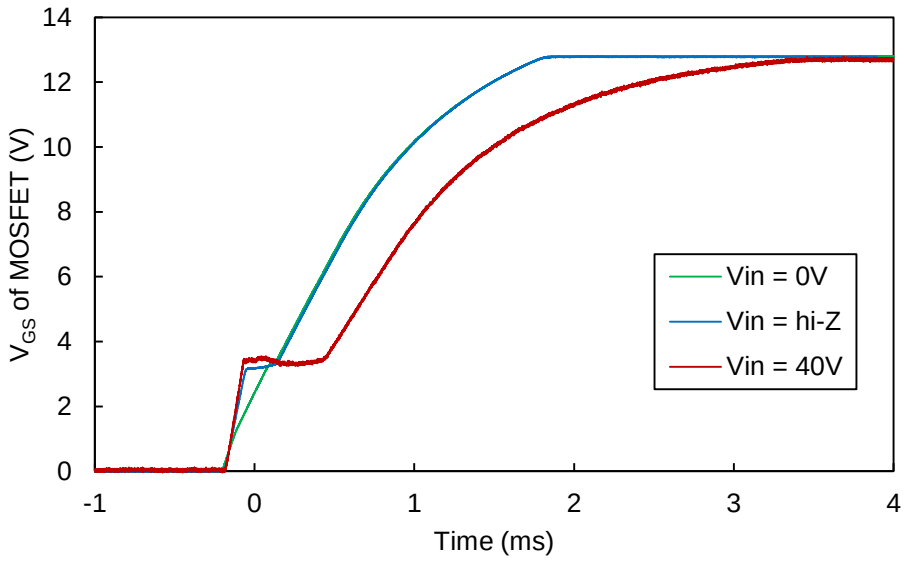

Figure 3.32: Measured MOSFET turn-on waveforms for high-impedance, 0V, and 40V applied at PV input.

After this capacitor is partially charged, the parasitic capacitance between the gate and drain pins (C_{GD}) will begin to rob charge current and divert it out of the drain pin instead of the source pin, leading to a loss in charge energy and increases charge time. This effect causes V_{GS} to plateau (Miller Plateau) during Q_{GD} charging and will significantly slow-down MOSFET turn-on. Higher MOSFET drain voltages lead to longer C_{GD} charging times and thus slow down the MOSFET turn on, whereas MOSFET turn-off is practically unaffected by the input voltage (shown in Figure 3.33).

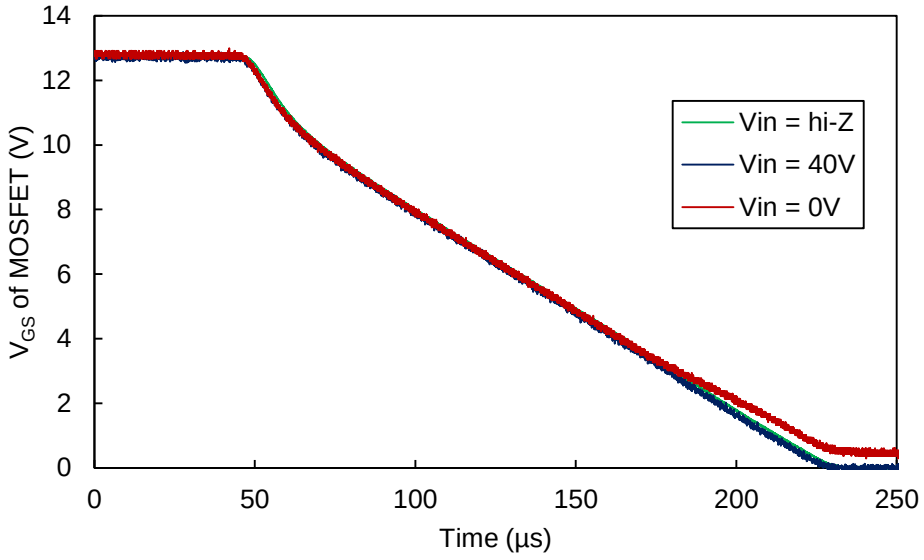

Figure 3.33: Measured MOSFET turn-off waveforms for high-impedance, 0V, and 40V applied at PV input.

There are two possible solutions to decrease turn-on time which is (1) by selecting a MOSFET with a low Q_G value at the expense of higher $R_{DS,on}$ due to device manufacturing constraints or (2) selecting a MOSFET which has a larger Q_{GS}/Q_{GD} ratio that will minimize the percentage of charge-current robbed by the drain side.

Finally, MOSFET costs can be significant depending on the selection criteria. MOSFETs with higher voltage ratings, due to manufacturing constraints, have what is called a higher figure of merit (FOM), which is the product of the on-state resistance and total gate charge, with some publications considering the gate-to-source charge instead.

$$FOM = R_{DS,on} \cdot Q_G \tag{3.10}$$

For up to two series connected high power PV modules a good minimum voltage rating for a MOSFET would be 100V. Bearing that in mind, a low-priced MOSFET by ST Microelectronics (STP24NF10) was chosen because it had the lowest cost on a distributor website but also because it has very good properties that helps it satisfy the selection criteria.

Table 3.10: Properties of MOSFETs that fit the selection criteria.

Name	STP24NF10	IPP50R190CE
Manufacturer	ST Microelectronics	Infineon Technologies
Drain to Source Voltage	100V	500V
Continuous Drain Current at 25°C	26A	18.5A
On-state resistance ($R_{DS,on}$) at I_D, V_{GS}	60mΩ at 12A, 10V	190mΩ at 6.2A, 13V
Turn-on threshold ($V_{GS(th)}$) at I_D	4V at 250µA	3.5V at 510µA
Gate charge (Q_G) at V_{GS}	41nC at 10V	6.1nC at 10V
Package	TO-220-3	TO-220-3
Single price (US Dollars)	$1.18	$1.53

The circuit was designed to accommodate MOSFETs with the TO-220-3 package and different voltage class MOSFETs can be connected to the same circuit by just changing the voltage measurement resistors and the capacitor bank allowing for different measurement configurations. The circuit has a maximum V_{oc} measurement range of 600V limited due to the

use of the Phoenix Contact MKDS5/ 2-9,5 connectors owing to their 30A nominal current and 600V nominal voltage rating (CUL and UL listed) (300V in Canada per CSA). For higher measurement voltages, the circuit can be redesigned to accommodate MOSFETs in TO-247 packages, which come in voltage ratings of up to 2500V, and IXYS has a few MOSFETs that have ratings up to 4500V with prohibitively high on-state resistances above 20Ω. At higher voltages and dwindling MOSFET availability, it would be recommendable to use IGBTs instead of MOSFETs.

3.4.1.5. Microcontroller Circuit

The I-V curve analyzer circuit is connected to a microcontroller board utilizing a STM32F303CC microcontroller from ST Microelectronics with an ARM Cortex M4F core with floating-point support running at 72 MHz with an 8 MHz external crystal and 9x PLL multiplier. This microcontroller was chosen because it is specifically marketed towards mixed-signal applications by ST Microelectronics, offering many useful peripherals such as 7x ultra-fast comparators (25ns), 4x op-amps with programmable gain, 2x 12-bit digital to analog converters (DACs), and 4x ultra-fast 12-bit analog to digital converters (ADCs) running at 5 Msps. The microcontroller comes in a 48-pin LQFP package measuring just 7x7 mm^2. It has 256 KB of Flash memory to allow large and complex programs stored in the firmware, and it has 40 KB of RAM allowing for thousands of measurement points. The board design in shown in Figure 3.34.

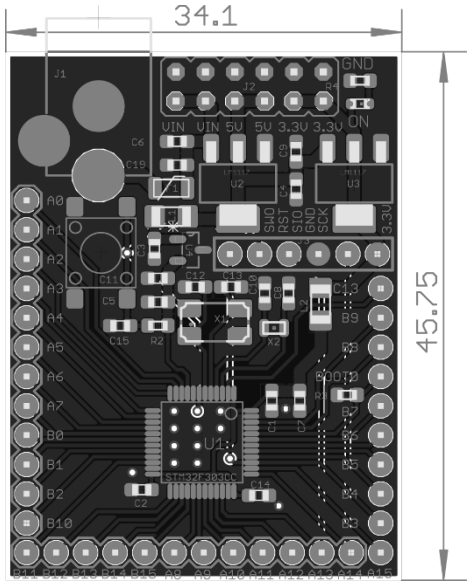

Figure 3.34: Microcontroller board (dimensions in mm).

Data are stored as a text file onto a micro SD card operating on the Serial Peripheral Interface (SPI) bus running at 2.25 MHz, with speeds up to 36 MHz possible. The built-in Real-Time Clock (RTC) allows saving files in folders with the date and file names timestamped allowing for hundreds of thousands of automated measurements, if necessary. The data written into a text file include the temperature, irradiance, capacitor charge time, and voltage and current measurements with their respective timestamps, which can be exported to any program to analyze the data.

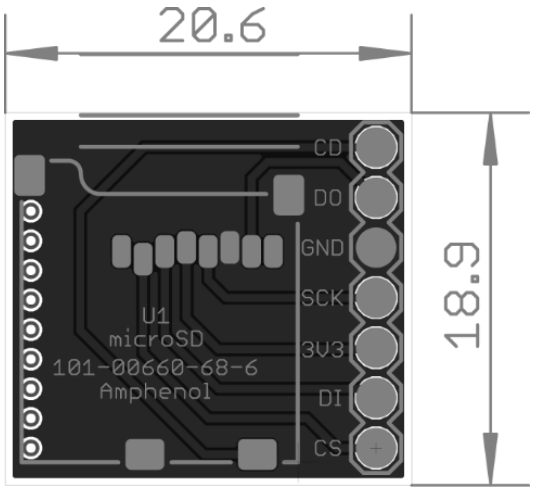

Figure 3.35: Micro SD card board (dimensions in mm).

To aid with the measurements, a generic 8-digit, 7-segment LED display with an encoder is used to read the measurements of V_{oc}, $V_{capacitor}$, I_{sc}, temperature, irradiance, date, and time and to look at measurements points.

For timely and precise measurements of voltage and current, ADCs 1 and 2 are set to run in dual mode, which allows them to run off the same trigger, practically measuring voltage and current at the same time. A custom design with a reference IC and passive filtering components is used as the voltage reference for the ADCs, leading to a reduction in noise. The ADCs are set to their slowest setting of 601.5 ADC clock cycles for the highest possible precision. The total conversion time of the ADCs is

$$T_{conv} = Sampling\ time + 12.5\ ADC\ clock\ cycles \tag{3.11}$$

The total measurement time for 4000 samples is measured to be 270 ms (14.80 ksps) including additional code to perform the iteration and store the values into memory. The application has chosen not to implement direct memory access (DMA) to simplify the code, resulting in a slower time retrieving the ADC conversion values from the ADC common regular

data register for dual mode operation (ADC12_CDR). The performance of the ADCs dominates the time it takes to move data between registers and any small amount of gain in register memory access speed would be insignificant.

Although the current ADC setting is not the fastest possible setting, this setting measures voltages and currents accurately from 0V to V_{oc} thanks to the selection of highly linear operational amplifiers designed for single-supply operation. I_{sc} currents below 350mA have been proven challenging to measure as the operational amplifier output overshoots at low input voltages of less than 2 mV. Otherwise, for higher short-circuit currents, the operational amplifiers track current down to zero at V_{oc} very well.

3.4.1.6. Experimental Results and Discussion

The first prototype was designed to measure open-circuit voltages up to 46.27V and short-circuit current up to 20A using only resistors with 1% tolerance to keep costs low. The linearity of the voltage and current measurements are plotted in Figures 3.36 and 3.37 below.

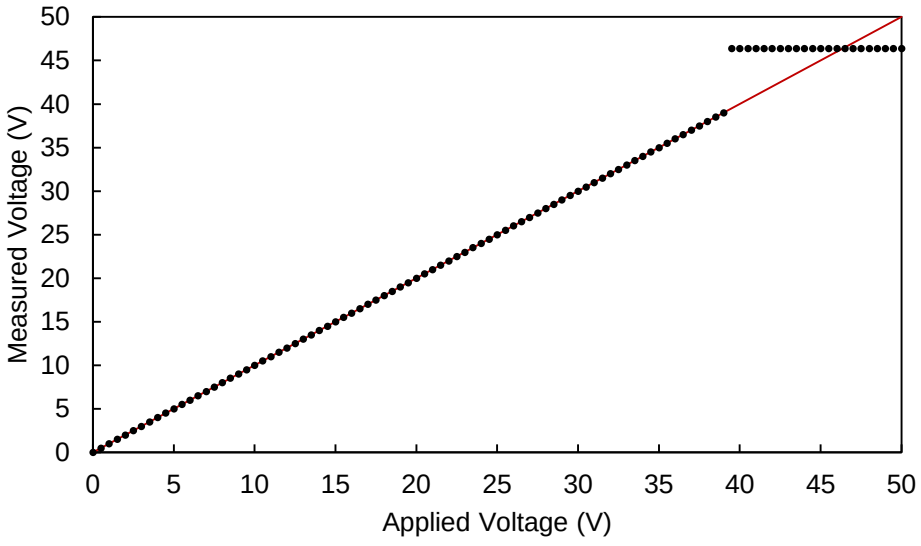

Figure 3.36: Applied voltage vs. measured voltage.

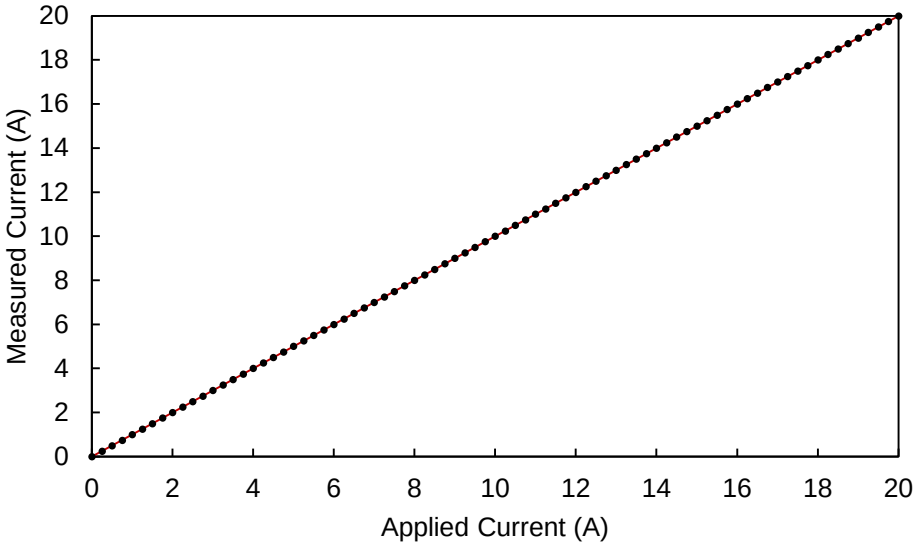

Figure 3.37: Applied current vs. measured current.

One unfortunate effect of the optimization of the operational amplifiers for lower rail (ground) operation is that the output begins to oscillate and start latching to the upper rail when the input voltage approaches approximately 0.5V of the upper rail. All circuits on the system are running off a 3.3V supply, and this puts quite a constraint on the operational amplifier headroom. A solution to this would be to increase the supply rail of the operational amplifier at the risk of damaging the microcontroller, especially during operational amplifier turn on when a very short high output pulse occurs. Passive clamps, such as Zener diodes, could be used to clamp the voltage to 3.3V at the ADC inputs to increase the conversion headroom – at the cost of increased parts count. A design choice was made to sacrifice about ~15.75% of the ADC headroom to better accommodate voltage measurements near zero volts.

The resulting allowable maximum measurable input voltage for the circuit is 39 V_{max}. The limitations of the voltage measurement do not carry over to the current measurement as seen in the figure above. This is due to the very low input voltage seen at the input of the operational

amplifier.

There are a few different ways of measuring current in a circuit like this. Some available options are hall-effect sensors, i.e. Allegro ACS712, LEM LA-55P and current measurement resistors. The selection of a current measurement resistor with a low temperature coefficient and a small resistance value, coupled with the use of high quality operational amplifiers, i.e. low input bias current, low input offset voltage, and good linearity, yield higher quality measurements than any current transducer ever could – and is the basis for the current measurement choice.

The cost breakdown by board is shown in the table below. For future work, the separate boards can be combined together into a single board. The total cost of all components comes down to $73.33 when purchased in singles. This is a significant cost reduction when compared to generation 1.5 ($183.57) and shows that significant cost optimizations are possible by using smaller discharge resistors, a different microcontroller board design, and replacement of the mechanical switches with electronic switches.

Table 3.11: Component costs per board.

Board Name	PCB Cost	Components Cost	Total Cost
I-V curve tracer board	$6.69	$24.59	$31.28
Irradiance monitor board	$2.07	$9.28	$11.35
Microcontroller board	$4.04	$18.59	$22.63
Micro SD card board	$1	$2.07	$3.07
Capacitor	n/a	~$5	$5
Total	$13.80	~$59.53	$73.33

On device startup, the user is prompted to input time and date. After completed, the device assumes a false measurement state. This state allows the user to see the time, date, temperature, irradiance, module voltage V_{pv}, module current I_{pv}, and capacitor voltage $V_{capacitor}$.

Once the run button is depressed and if an SD card is detected, the measurement state bit becomes true and the firmware runs the measurement loop. Initially, the user display is turned off to increase the measurement accuracy since the display has a pulse-width modulator to adjust segment brightness. The capacitor is discharged in case there is any stored parasitic charge in the capacitor, which is very common for aluminum electrolytic capacitors. Afterwards, the circuit runs a function to determine the capacitor charge time. Once the charge time is known, the capacitor is discharged again. At this point, the measurement function runs and it captures the time stamp, V_{pv} and I_{pv} values and adds a delay between measurements if the charge time is more than 270 ms. The capacitor is discharged afterwards and the data are transferred to the SD card for retrieval.

Multiple measurements were taken to observe the effects of different capacitor values connected at different temperature and irradiance levels. As mentioned in the MOSFET switching circuit section, it is impossible to take a current measurement at exactly 0V. The speed of the turn-on of the MOSFET, in addition to the on-state resistance of the MOSFET, makes it challenging to take measurements at voltage points near 0V.

When a gate signal is sent to the MOSFET, during turn on, a small amount of current flows through the MOSFET into the capacitor, charging it up to a minimum voltage as shown in Figure 3.38. This minimum voltage is dependent on the size of the capacitor. Equation 3.3 shows that for a fixed amount of charge, the voltage rise is inversely proportional with the capacitance.

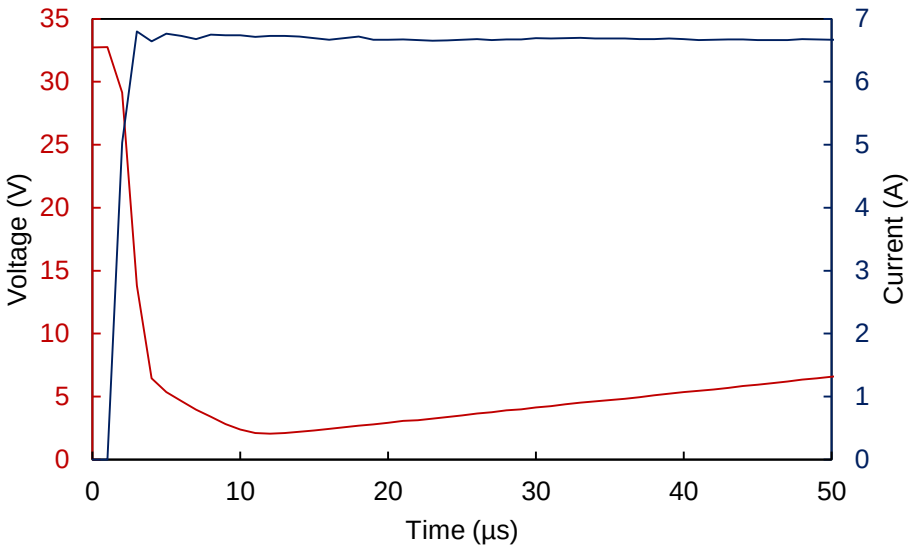

Figure 3.38: Measured PV module voltage and current during charging MOSFET turn-on.

The measurements shown in Figure 3.39 were taken on the same day with a long period between the 2200 µF load and the others. The module was initially indoors at a room temperature of about 25°C. When the initial measurement was taken, the module was not at a thermal equilibrium and was warming up as the measurements progressed. This is the reason why the 2200µF curve is farther than the others – before taking measurements, it is very important to have the module reach a stable temperature, usually achievable within 10-15 minutes. Otherwise, the strong thermal dependence of the open-circuit voltage (V_{oc}) may result in incorrect measurements.

Another visible point is the different minimum measured voltages. With decreased capacitance values, the minimum voltage increases and below a certain capacitance value, the measurement would become unacceptable.

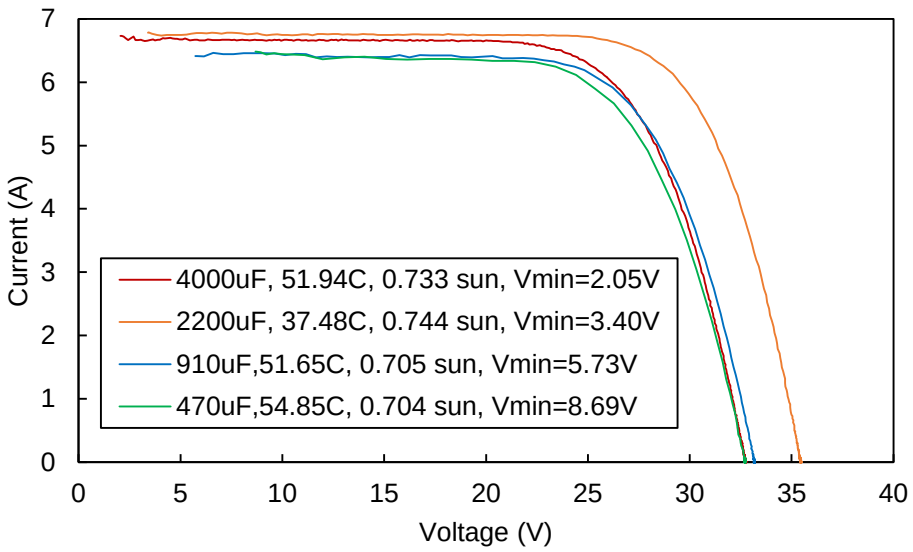

Figure 3.39: I-V curve measurements using different capacitors.

Once the measurements are taken, the values were converted to standard test conditions as outlined in Chapter 2. STC conversion results are shown in Figure 3.40.

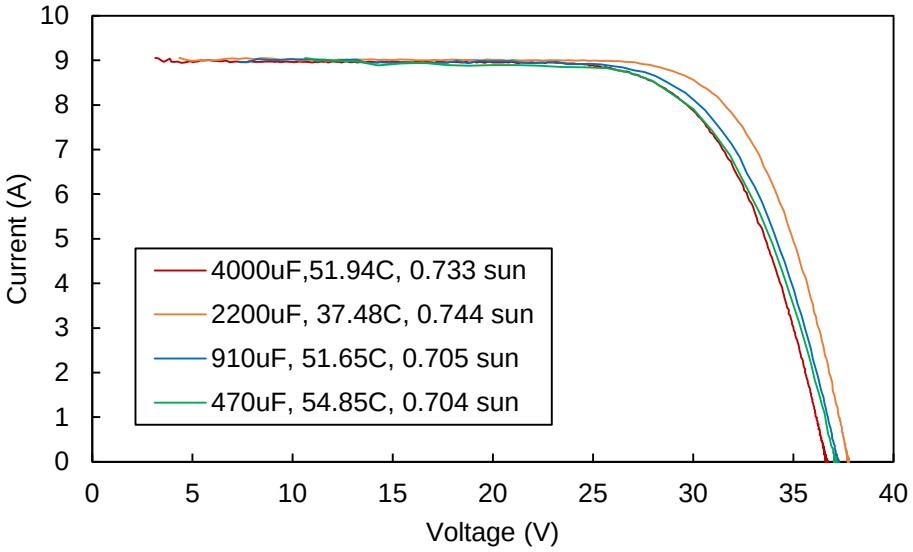

Figure 3.40: STC converted I-V curve measurements using different capacitors.

The datasheet indicates measurement tolerances of 3% for all measurements including V_{oc} and I_{sc}. This, coupled with the overly simplified STC conversion process introduces a small error margin for the short-circuit current, and a somewhat greater error margin for the open-circuit voltage measurement.

Regardless of the small error margins, the shapes of the curve and the comparative I_{sc} and V_{oc} measurements of the PV modules that will be connected together are very important in determining compatibility prior to installation. Once installed, the shape of the I-V curve of the whole array should appear similar to the shape of a single module, with a similar I_{sc} value and $n \times V_{oc}$ for series connected PV array containing *n* modules, and $n \times I_{sc}$ value and a similar V_{oc} value for *n* modules connected in parallel.

3.5. Conclusions

The designs of high accuracy, high resolution, low-cost, and highly portable I-V curve tracers for photovoltaic modules and arrays were pursued in this chapter. The design of three different circuits comprised of two distinct generations of the I-V curve tracer has been presented thoroughly in this chapter. The first generation circuit is based on mechanical switches while the second generation circuit is based on MOSFETs.

In generation 1, a baseline for measurement performance, resolution, circuit volume and price was established. In generation 1.5, the performance of the curve tracer was optimized to have more points in a smaller and more compact package. The redundantly large discharge resistors of generation 1 were replaced for smaller and less expensive alternatives in generation 1.5, which are capable of handling the power requirements just as well. With generation 1.5, the limitation of the circuit going forward clearly became the switching mechanism, especially in

terms of volume, cost and reliability.

Therefore, in generation 2, a whole new switching topology was explored with the use of MOSFETs to replace the bulky and unreliable relays that also consume quite a lot of power, which drain the battery much more quickly. Generation 2 also combines irradiance and temperature measurement circuits with an auxiliary thermocouple connection for module temperature measurements, and an external irradiance measurement board that can be placed directly on PV modules for proper measurements. With the use of a more advanced microcontroller, it was possible to acquire 4000 points per measurement with unique naming for each measurement. The large amount of data can be easily written to SD cards stamped with the date and time for identification. The costs have been brought down to $73.33 per unit with generation 2, and can be further reduced through combining the I-V curve tracer and microcontroller boards. The volume of the I-V curve tracer board also has shrunk to just 64.7cm^3 (excluding capacitors and microcontroller board), improving the compactness over examples shown in Chapter 1.

CHAPTER 4

EMULATION OF PHOTOVOLTAIC MODULES USING SILICON DEVICES

4.1. Introduction

As previously discussed, PV module emulators are critical because they allow for standardized testing conditions for PV related equipment, and they offer customization abilities that would simply be impossible to offer using actual photovoltaic modules.

There are two main DC-DC converter topologies: those which increase the output voltage when compared to the input are called boost converters. Buck converters on the other hand, allow the output voltage to be varied between 0V and the input voltage. Buck and boost converters can be combined in a circuit to form buck-boost converters.

The buck converter topology was chosen in this work due to its inherent stability and ease of control, and also for safety concerns since the input and output voltages need to be limited. Over voltages may cause harm to operators and equipment, and the buck converter reduces the risk of over voltage.

The devices observed in literature are not concerned with high power density or high switching frequency operation. They are also not concerned with compactness and high efficiency. In order to overcome these limitations, it is proposed to build a PV emulator to produce a light-weight, portable and high switching frequency emulator using digital controls without an analog reference cell. The first generation of devices (Generation 1) is based on a relatively slow non-synchronous buck converter that utilizes equation solving as a proof-of-concept.

Generation 2 focuses on high power density and high switching frequency operation with a high efficiency to reduce the device footprint. The method of equation solving coupled with external ADCs was noticed to slow down the loop frequency considerably, which had a negative effect on dynamic loads such as microinverters. Therefore, in Generation 2.5, the equation solving method was replaced initially with a look up table with a current value for every 1V increment from 0V to V_{oc}. The values between the two points were calculated through basic linear interpolation.

This solution provided for increased loop frequencies but it did not model the curve of the photovoltaic module accurately enough, especially when equally spaced 40 points were concerned. Therefore, this approach was abandoned in favor of an increased number of points, negating the use of linear interpolation. In determining the sampling points, instead of equally dividing V_{oc}, it was decided that the use of unique analog-to-digital conversion values of the output voltage would be much faster. These values were combined with the analog-to-digital conversion values of the current to run the digital control loop even faster. As shown in the relative subsections, this provided for a substantially improved design.

4.2. Generation 1: 62.5 kHz Non-Synchronous Buck Converter

The block diagram of the proposed PV module emulator is shown in Figure 4.1. The PV module emulator operates as a voltage controlled current source and the basic functions of I-V curve generation using equation solving, window comparator, incremental controller, PWM generator, power stage and the input voltage, output voltage, and output current measurement stage are shown along with the load connection.

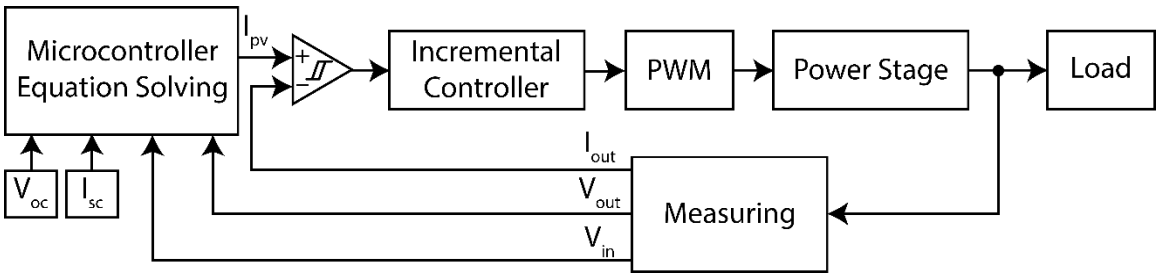

Figure 4.1: Block diagram of the proposed PV module emulator.

4.2.1. Circuit Topology

A non-synchronous buck converter shown in Figure 4.2 was chosen over a synchronous buck converter for simplicity and ease of control for the design of the first generation PV module emulator. The buck converter allows for varying the output voltage V_{out} by changing the duty cycle d of the circuit, with the output voltage varying between 0 and $0.9V_{in}$ and d varying between 0 and 0.9 (90%) as calculated in the equation below,

$$V_{out} = d \cdot V_{in} \tag{4.1}$$

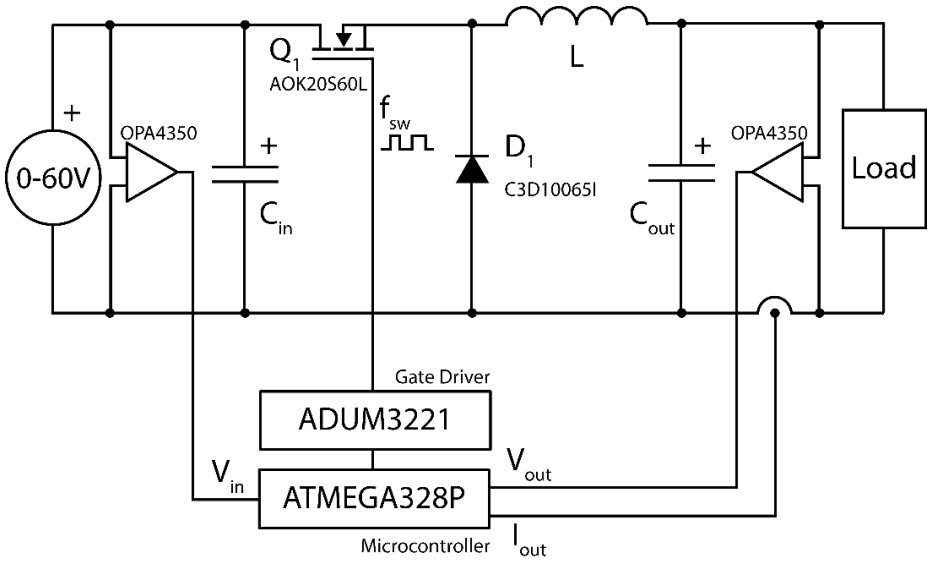

Figure 4.2: Schematic of a non-synchronous buck converter [84].

A DC power supply is connected at the input voltage V_{in} and the input ripple voltage is filtered through the input capacitor C_{in}. Q_1 denotes the MOSFET (AOK20S60L) that performs the switching action. D_1 is the diode (C3D10065I) that allows the current to commute through inductor L when Q_1 is switched off. C_{out} is used to limit the voltage ripple at the output.

The PV module emulator control circuit consists of an Atmel ATMEGA328P microcontroller running at 16 MHz connected to an Analog Devices ADUM3221 gate driver driving the high-side switch Q_1 at 12V using a charge-pump configuration.

The PV module emulator accepts any DC power supply at the input up to 60V. Using a power supply with a voltage higher than the desired V_{oc}, a buck converter topology makes it possible to scale down the voltage while increasing current output, allowing for a broad range of PV system conditions to be simulated with DC supplies that have output current limitations. The robust design measures the input voltage of the emulator, and automatically limits the highest output voltage possible. The user is trusted with matching the input power to the selected output power through comparing the output capabilities of the input power supply with the maximum power output (P_{mpp}) readout on the display. In the case of photovoltaic modules, maximum power is generated at the maximum power point (MPP) and is calculated using,

$$P_{mpp} = V_{oc} \cdot I_{sc} \cdot FF \tag{4.2}$$

where FF is the fill factor and V_{oc} and I_{sc} are the open-circuit voltage and short-circuit current of the emulated PV module.

During operation, the input voltage V_{in}, output voltage V_{out}, and output current I_{out} are measured using voltage divider resistors and a series shunt resistor, respectively. The measurements are taken differentially and buffered using a Texas Instruments OPA4350 4-channel high-speed operational amplifier connected to the input of the built-in analog to digital

converter (ADC) of the microcontroller. The built-in ADCs offer 10-bits precision and convert values every 100 µs. Since three values are measured using the ADCs, the total measurement time is 300 µs.

4.2.2. Algorithm Development

The PV emulator first checks for the presence of an input voltage. Once an input voltage is detected, the maximum adjustable open-circuit voltage is limited to 90% of the input voltage. If an input voltage is not detected or if the input voltage is below an adjustable minimum value, the PV emulator waits until the input conditions are satisfied.

Once V_{oc} and I_{sc} are adjusted with potentiometers and the select button is pressed, these values are stored and the emulator calculates A (ideality factor multiplied by thermal voltage) as outlined in Chapter 2 using I_o = 1µA. At the conclusion of the calculations the *ready* status light indicates system readiness. Afterwards, the operator presses the *run* button and actives the PV module emulator loop. Once running, the run status light is lit and the initial duty cycle is set to 0 which has 8 bits precision (256 unique values).

While the loop is running the emulator constantly measures V_{in}, V_{out} and I_{out} and the measured output voltage is fed into the ideal diode equation outlined in Chapter 2 and an output current is calculated for the specific output voltage. The control algorithm takes control afterwards.

4.2.3. Control Algorithm

An incremental control algorithm was implemented using a window comparator with a small hysteresis window, as shown in Figure 4.1. If the output current value is 10% or 100 mA higher than calculated (whichever is smaller), the duty cycle of the buck converter is digitally decremented, and likewise when the current is 10% below or 100 mA lower than the set value

(whichever is smaller), the duty cycle is incremented. The small window allows for the stable operation of the system when loaded with devices that might inject some noise and disturb output current and voltage measurements.

4.2.4. PWM Control

The pulse-width-modulation (PWM) resolution is based on a division of the microcontroller's operational frequency. Running at 16 MHz, an 8-bit PWM with 256 unique values allows for a maximum switching frequency of 62.5 kHz. Conversely, increasing the PWM resolution to 10 bits reduces the maximum switching frequency to 15.63 kHz – a switching frequency which puts a lot of stress on the passive components (inductors and capacitors) and requires very large inductor and capacitor values to reduce current and voltage ripple.

4.2.5. Component Selection

Choice for the circuit parameters shown in Figure 4.2, such as the input capacitance C_{in}, output capacitance C_{out}, inductance L, the selection of switching frequency f_{sw}, MOSFET type, and diode type were guided by the use of Taguchi's Orthogonal Arrays [85]. An effort was made to minimize the root-mean-square deviation (RMSD) [86-87] between the algorithm and the output of the emulator using,

$$RMSD = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(I_{out}(v_i) - I_{calc}(v_i)\right)^2} \tag{4.3}$$

where I_{out} represents the measured current output dependent on the output voltage v_i and I_{calc} represents the current value calculated by the equation given in the model section.

Standard buck converter equations can be used to calculate and optimize to achieve higher efficiency or higher power density, but these equations do not allow to optimize for output errors. Therefore, for RMSD optimizations, a combination of different MOSFET models, diode

models, switching frequencies, inductor, and capacitor values were tested. The circuit design was finalized to have low RMSD values with a compromise in the inductor size to limit circuit footprint. The experiments led to the selection of the parameters shown in Table 4.1.

Table 4.1: PV emulator operational parameters.

Symbol	Name	Designed Value
L	Inductor	100 µH
C_{in}	Input filter capacitor	2210 µF
C_{out}	Output capacitor	2210 µF
f_{sw}	Switching frequency	62.5 kHz
V_{in}	Input voltage	60 V
Q_1	Switching MOSFET	AOK20S60L
D_1	Rectifier diode	C3D10065I

Tests show that the large electrolytic capacitors shown in Figure 4.3 do not contribute much toward reducing the high frequency ripple and instead, the smaller polymer capacitors (red colored beside the rear connectors) provide all of the high frequency filtering necessary. The electrolytic capacitors play a central role in improving the DC characteristics of the PV emulator circuit. The drum core inductor shown in the top middle portion of the circuit was chosen because of its high inductance per square area, but this resulted in a drawback of a high magnetic leakage due to the unshielded design, which coupled noise to neighboring traces and connections.

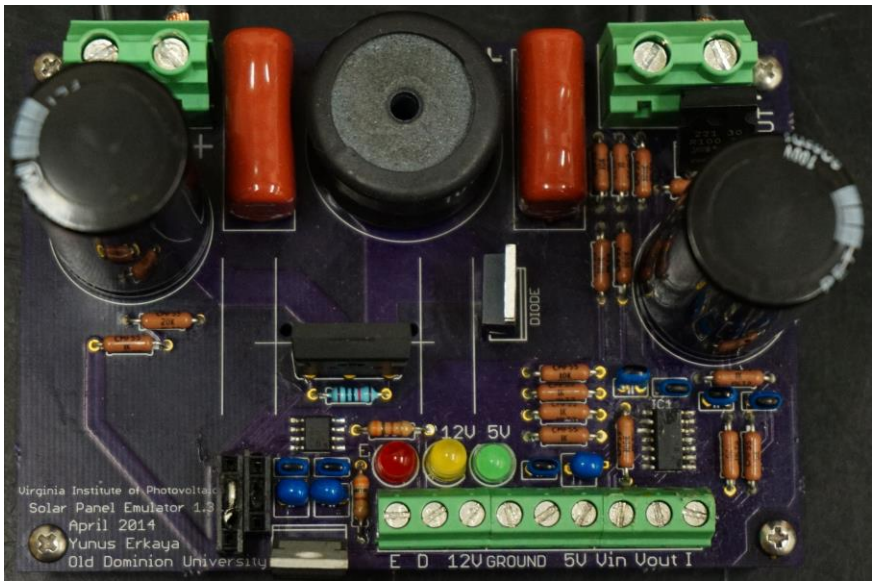

Figure 4.3. Photograph of the PV emulator.

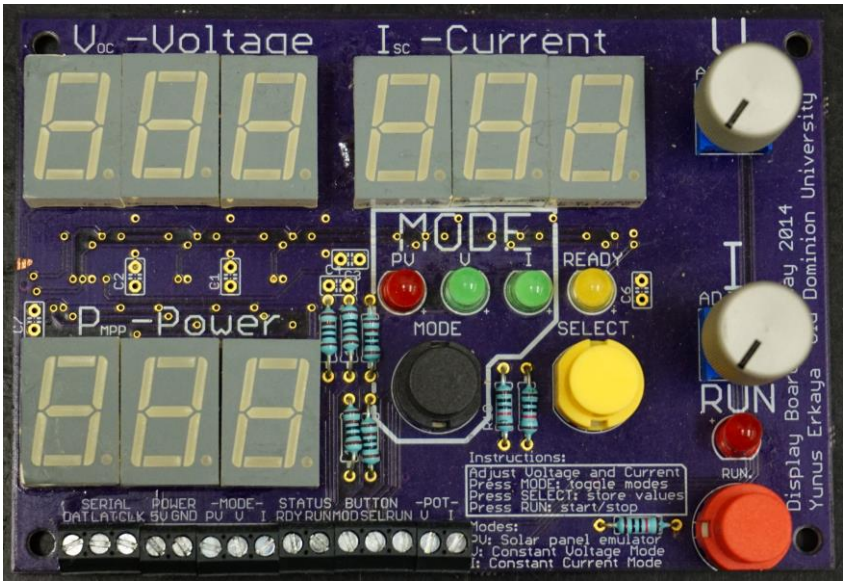

Figure 4.4. Photograph of the PV emulator user interface.

The user interface shown in Figure 4.4 allows the setting of open-circuit voltage and short-circuit current along with the adjustment of the output mode: photovoltaic emulator,

constant voltage, and constant current modes. The operator is expected to adjust the open-circuit voltage and short-circuit current values along with the operation mode. Once the desired values are chosen, pushing the *select* button stores the values into memory. At this point the 7-segment display will indicate V_{oc}, I_{sc} and P_{mpp} respectively. Pressing the run button begins the active operation at which point the voltage, current, and power measurements relate to the actual PV emulator output.

4.2.6. Results and Discussion

The output of the PV emulator was connected to two 250W rheostats with values of 10Ω and 100Ω. Incremental load resistance values were chosen with manual precision. The results are shown in Figures 4.5 and 4.6 below, where V_{oc} was fixed to 40V and I_{sc} values from 1A to 7A.

In Figures 4.5 and 4.6, the points calculated with the algorithm are drawn with colors, representing I_{sc} values ranging from 1A to 7A with V_{oc} of 40V. The black dots represent actual emulator outputs measured with a voltmeter and an ammeter. The data points closely correlate with the calculated values. The intervals between the measurement points were kept approximately equal by using equal resistor increments. The dot density changes when the value of the load resistor changes from 10Ω to 100Ω.

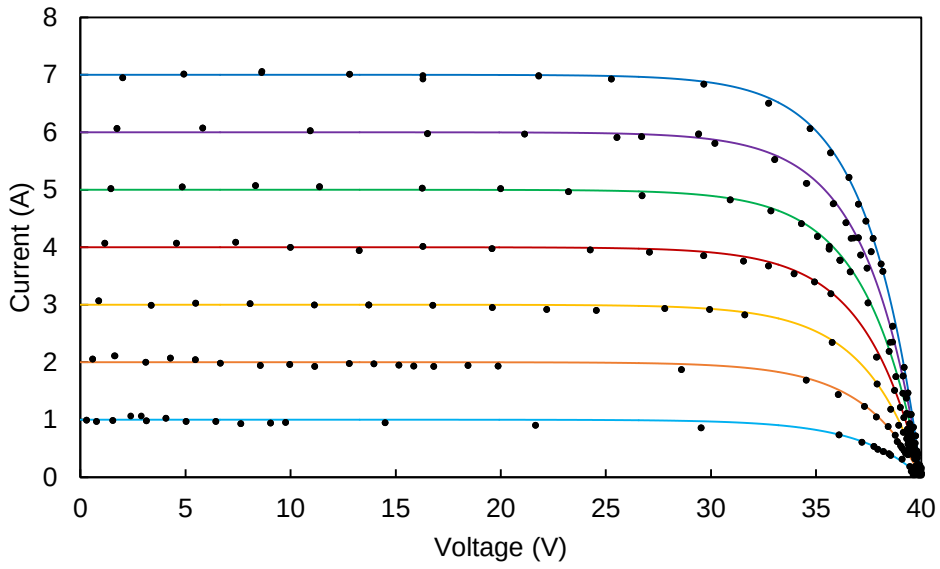

Figure 4.5: Measured operation points over simulated I-V curves of the PV emulator for V_{oc} = 40V and I_{sc} = 1-7A.

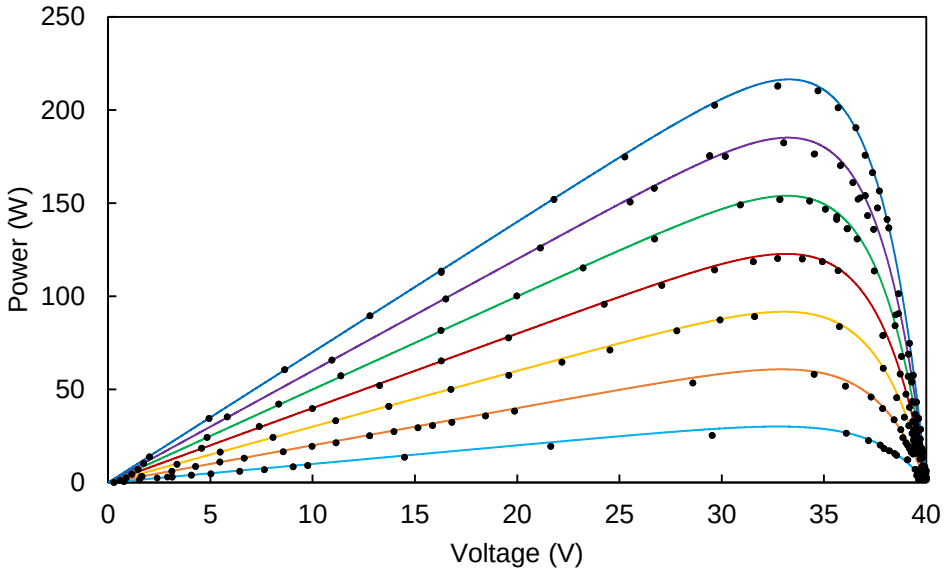

Figure 4.6: Measured operation points over simulated P-V curves of the PV emulator for V_{oc} = 40V and I_{sc} = 1-7A.

At I_{sc} values lower than 2A, the emulator failed to provide a good output at a direct short, but lightly loading the emulator allowed for the current to settle near the calculated value. Data points in Figures 4.5 and 4.6 were used in determining the accuracy of the emulator with the RMSD method. The results are given in Table 4.2, where V_{oc} is 40V, and I_{sc} ranges from 1A to 7A. A minimum of 59 data points were used to calculate the RMSD, where lower RMSD values indicate better accuracy.

Table 4.2: PV emulator accuracy for various I_{sc} conditions.

V_{oc} (V)	I_{sc} (A)	RMSD (A)	Data points
40	1	0.04	59
40	2	0.06	70
40	3	0.09	69
40	4	0.11	78
40	5	0.13	85
40	6	0.24	72
40	7	0.16	74

The conditions that contribute the most to the RMSD value are when the output voltage is near V_{OC}. In this case, due to the steep slope of the I-V curve near the V_{oc} region, a slight error in the output voltage measurement causes a large error between calculated current and output current as shown in Figure 4.7. In all other cases, the circuit performs remarkably well and output current percent errors generally remain under ±10% or ±100 mA. Although the control scheme involves a very simple incremental duty cycle algorithm, the output errors are acceptable up until near V_{oc} conditions.

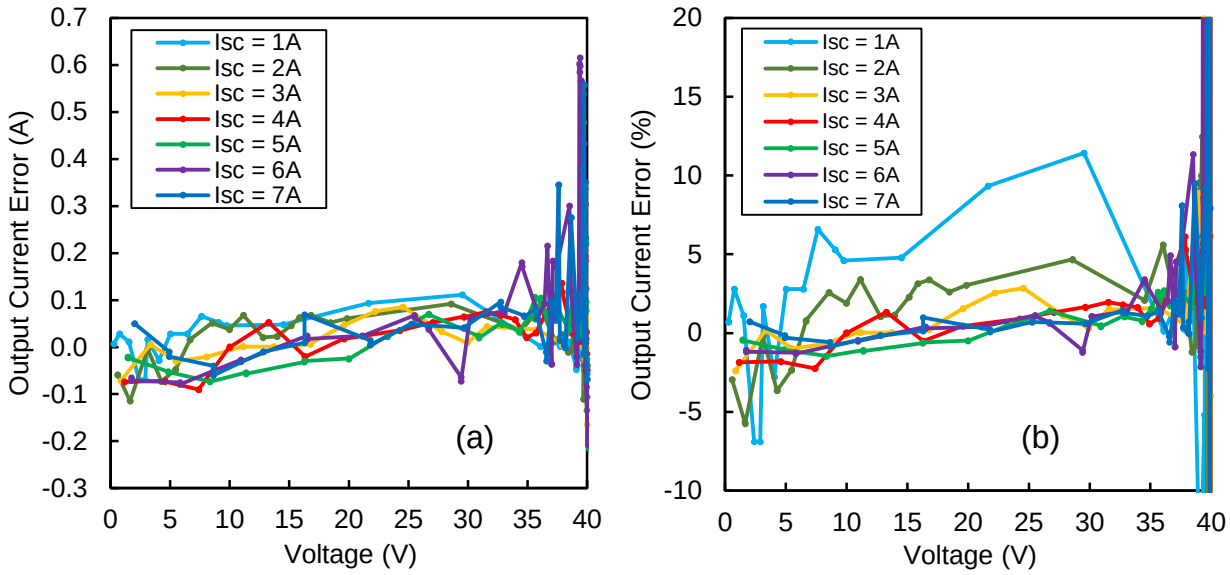

Figure 4.7: Output current error in absolute (a) and percentage (b) vs. output voltage of the PV emulator.

Figure 4.7 also demonstrates that the percent output current errors are significant for I_{sc} = 1A and comparatively high for I_{sc} = 2A. This is due to the control algorithm limiting errors to ±100mA (10% for 1A and 5% for 2A) and it can be improved with a smaller hysteresis window or by using a different control algorithm such as PI control.

4.3. Generation 2: 500 kHz Non-Synchronous Buck Converter

The block diagram of the second generation PV module emulator is shown in Figure 4.8. The PV module emulator operates as a voltage controlled current source and the basic functions of I-V curve generation using equation solving, output current error calculation, integrative controller, PWM generator, power stage and the input voltage, output voltage, and output current measurement stage are shown along with the load connection.

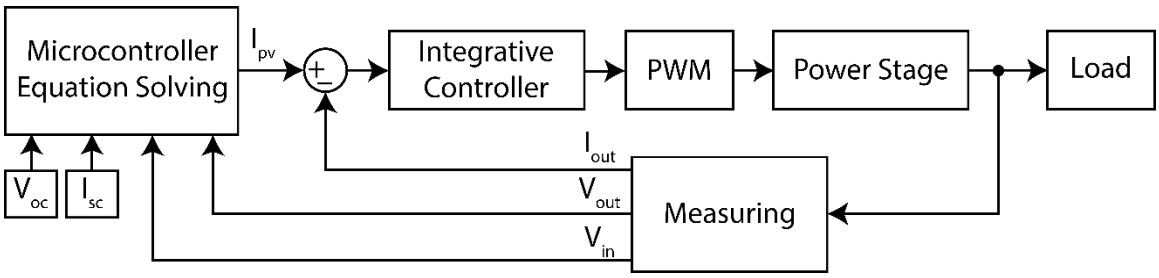

Figure 4.8: Block diagram of the proposed PV module emulator.

4.3.1. Circuit Topology

A non-synchronous buck converter topology with an isolated gate driver was implemented for design simplicity [29]. The isolated gate driver eliminates the charge-pumping necessary to keep the bootstrap capacitor charged during MOSFET turn off. This improves output characteristics by eliminating the circulating parasitic gate charge currents that disturb measurements and prevents a voltage rise at the output for light loads [88]. A frequency of 0.5 MHz was chosen to facilitate the need for only small energy storing elements (i.e. input and output capacitors, inductor), which allows for higher power density. An upper limit of 48V for the input voltage was imposed in order to use 60V class Si-MOSFETs instead of 100V class Si-MOSFETs with a higher figure of merit (FOM). The FOM is the product of the on-state resistance ($R_{ds,on}$) and the total gate charge (Q_g) given by [89]:

$$FOM = R_{ds,on} \cdot Q_g \tag{4.4}$$

where a lower value indicates a better device. The design goal was to create a photovoltaic emulator front-end device for any switch-mode or linear power supply commonly available in laboratories across universities, with outputs ranging from 5V/5A to 60V/10A. The buck topology allows an effective increase in output vs. input current when operated at any duty cycle value within a range of 0 – 95%.

The robust design of the PV emulator makes it challenging to fine tune efficiency for every operational point, therefore all tests and efficiency calculations were performed at the maximum input voltage of 48V to create a reliable and high power density device without any requirement for active cooling.

4.3.2. Component Selection

A hardware prototype was constructed to verify circuit performance and determine efficiency characteristics. Key design attributes and component selections are also described.

Component selection is critical for efficiency, reliability, and output accuracy. For this reason, a high switching frequency was chosen to reduce the size of the passive components, which lead to a reduction of stored energy between cycles and an improvement in dynamic performance. The stored energy in the inductor E_L and capacitor E_C can be calculated as,

$$E_L = \frac{1}{2}LI^2, E_{L_{max}} = \frac{1}{2} \cdot 6.8 \times 10^{-6} \cdot 10^2 = 0.34 \text{ mJ} \tag{4.5}$$

$$E_C = \frac{1}{2}CV^2, E_{C_{max}} = \frac{1}{2} \cdot 50 \times 10^{-6} \cdot 40^2 = 40 \text{ mJ} \tag{4.6}$$

In the case of a rapid disconnection of the load, the stored energy in the inductor will be absorbed by the output capacitor bank. The maximum voltage rise can be computed as follows:

$$E_{L_{max}} = 0.34 \text{ mJ} = \frac{1}{2}CV^2 \rightarrow V = 3.687 \text{ V} \tag{4.7}$$

Knowing the maximum voltage rise allows setting the minimum output capacitance to achieve a permissible level of under 10% rise at 40V. Taking the output ripple equations into consideration, the inductor and capacitor size were confirmed to keep the output ripples below 40% for current and 1% for voltage. The equations used to calculate the ripple values are shown in Eq. 4.8 and Eq. 4.9. The maximum current ripple was calculated to be 3.53A (35.3%) and the maximum voltage ripple was calculated to be 17.65 mV (0.044%).

$$\Delta I = d\frac{V_{in} - V_{out}}{f \cdot L} = \frac{V_{in}(1-d)d}{f \cdot L} \rightarrow \Delta I_{max} = \frac{V_{in}}{4f \cdot L} \tag{4.8}$$

$$\Delta V = \frac{\Delta I}{8f \cdot C_{out}} \tag{4.9}$$

The second design challenge, beyond satisfying output ripple requirements, was to satisfy efficiency requirements. Initially, the design utilized 100V class MOSFETs in the first prototype for good voltage overshoot protection. However, the lower figure of merit ($R_{ds,on}$ x Q_g) of 60V Si-MOSFETs led to designing the circuit around 60V devices, meaning the switch node voltage overshoot during turn-on has to be limited by slowing down device turn-on. This design, therefore, had to meet strict voltage overshoot requirements to prevent the MOSFET and diode from avalanching.

The loss calculations for the MOSFET were split into three categories: switching losses at turn-on $P_{sw,on}$, turn-off $P_{sw,off}$, and conduction losses P_{cond}. Also, of note, these calculations do not take the duty cycle into consideration in order to calculate worst-case losses. Equation 4.10 applies for both turn-on and turn-off losses.

$$P_{sw,on/off} = 0.5 \cdot V_{in} \cdot I_{out} \cdot f_{sw} \cdot t_{sw,on/off} \tag{4.10}$$

The switch-on time ($t_{sw,on}$) is modeled using Eq. 4.11, where Q_g is the MOSFET gate charge, $R_{g,int}$ is the MOSFET internal gate resistance, R_{driver} is the gate driver source path resistance, and $R_{g,ext}$ is the externally connected gate resistor value.

$$t_{sw,on} = Q_g \cdot \frac{R_{g,int} + R_{driver} + R_{g,ext}}{V_{gs}} \tag{4.11}$$

The switch-off time ($t_{sw,off}$) is calculated in Eq. 4.12, where I_g is the gate driver sink current.

$$t_{sw,off} = \frac{Q_g}{I_g} \tag{4.12}$$

The switching losses were minimized by using a two-stage gate driver circuit with a resistive turn-on path and a forward biased diode for the turn-off path [90]. This allowed for slowing the MOSFET turn-on while not affecting the turn-off speed by permitting nearly 3A discharge of the MOSFETs gate capacitance. This was done bearing in mind that the driver resistance and the internal gate resistance limit the upper value of this current, with the gate drive diode assumed to instantly conduct.

The conduction losses are given in Eq. 4.13, where $R_{ds,on}$ is the on-state resistance.

$$P_{cond} = I_{out}^2 \cdot R_{ds,on} \tag{4.13}$$

To increase the efficiency of the power stage, it is important to optimize the MOSFET for both conduction and switching losses. After considering several different MOSFET models, the Texas Instruments CSD18534KCS NexFET MOSFET was chosen having a non-isolated TO-220 package, 1.5Ω typical series gate resistance, 15mΩ typical on-resistance, and 19 nC typical gate charge. The combined MOSFET losses at the maximum output current of 10 A are 5.68 W, calculated using,

$$P_{loss,mosfet} = I_{out}^2 \cdot R_{ds,on} + 0.5 \cdot V_{in} \cdot I_{out} \cdot f_{sw} \cdot Q_g \left(\frac{1}{I_{gate}} + \frac{R_{g,int} + R_{driver} + R_{g,ext}}{V_{gs}} \right) \tag{4.14}$$

A Schottky diode was chosen to provide minimal voltage drop, leading to the selection of ST Microelectronics STPS20M60D with a two-pin non-isolated TO-220 package and forward voltage drop V_F of 0.47V at 10A at 25°C. The equation to calculate the diode conduction loss is given in the manufacturer datasheet as Eq. 4.15 and when the effect of RMS current is ignored the losses are 3.85 W.

$$P_{diode,cond} = 0.385 \cdot I_{average} + 0.0073 \cdot I_{rms}^2 \tag{4.15}$$

Another contributing factor to diode losses are the reverse recovery losses, which are a trade-off between a high-speed low reverse-recovery charge Q_{rr} with high forward voltage V_F,

and slightly lower speed diodes with improved forward voltage drop with significant reverse current flow. Since the diode datasheet omits Q_{rr} completely, the value used in Eq. 4.16 was experimentally verified. Total diode losses are given in Eq. 4.17.

$$P_{diode,rr} = Q_{rr} \cdot V_{in} \cdot f_{sw} = 8 \times 10^{-8} \cdot 48 \cdot 5 \times 10^{5} = 1.92\ \text{W} \tag{4.16}$$

$$P_{loss,diode} = P_{diode,cond} + P_{diode,rr} = 3.85 + 1.92 = 5.77\ \text{W} \tag{4.17}$$

Experiments show that diode switching losses mainly contribute at low output power conditions. At high output power levels, the diode conduction losses dominate. Since the optimization was carried out for high current output, a diode with the lowest possible forward voltage drop was chosen so that at low duty cycles and high currents, i.e. at or near I_{sc} conditions, the diode will be able to carry the current without overheating.

Table 4.3: Hardware components of the photovoltaic emulator.

Symbol	Part Name	Value or Model
L	Inductor	6.8 µH
C_{in}	Input filter capacitor	5x 4.7 µF
C_{out}	Output filter capacitor	5x 10 µF
R_L	DCR of inductor	23.3 mΩ
R_{sense}	Current sense resistor	5 mΩ
R_{bleed}	C_{out} bleed resistor	6.8 kΩ
R_{out}	V_{out} resistive divider	11 kΩ
R_{in}	V_{in} resistive divider	101 kΩ
Q_1	60v Si-MOSFET	CSD18534KCS
D_1	60V Si-Schottky diode	STPS20M60D

The resistive elements in the circuit produce additional power losses. Significant losses arise from the DC resistance of the inductor (R_L), the resistances of the input and output voltage

divider circuits (R_{in} and R_{out}), the capacitor discharge resistor (R_{bleed}), and the current sense resistor (R_{sense}).

For the resistance values given in Table 4.3, the total resistive losses calculated with Eq. 4.18 are 3.23 W.

$$P_{loss,res} = I_{out}^2 \cdot (R_L + R_{sense}) + \frac{V_{in}^2}{R_{in}} + \frac{V_{out}^2}{R_{bleed}//R_{out}} \tag{4.18}$$

Here, R_{bleed} is necessary to allow the slow discharge of the output capacitor when the load is disconnected. The total converter losses are the sum of MOSFET, diode and resistive losses as shown in Eq. 4.19,

$$P_{loss} = P_{loss,mosfet} + P_{loss,diode} + P_{loss,res} = 5.68 + 5.77 + 3.23 = 14.39 \text{ W} \tag{4.19}$$

Knowing the total power losses at 40V and 10A output, the worst-case efficiency at the maximum power output can be calculated as follows, if both the MOSFET and diode were to fully conduct without considering their duty cycle:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} 100\% = \frac{400}{400 + 14.39} 100\% = 96.53\% \tag{4.20}$$

Factoring the duty cycle into the MOSFET and diode conduction equations via the input voltage to output voltage ratio, the realistic power loss is lower at 11.35 W and the calculated efficiency is higher at 97.64%. Figure 4.9 shows calculated vs. measured values for efficiency. The circuit was tested at a maximum output power of ~350 W due to power supply constraints.

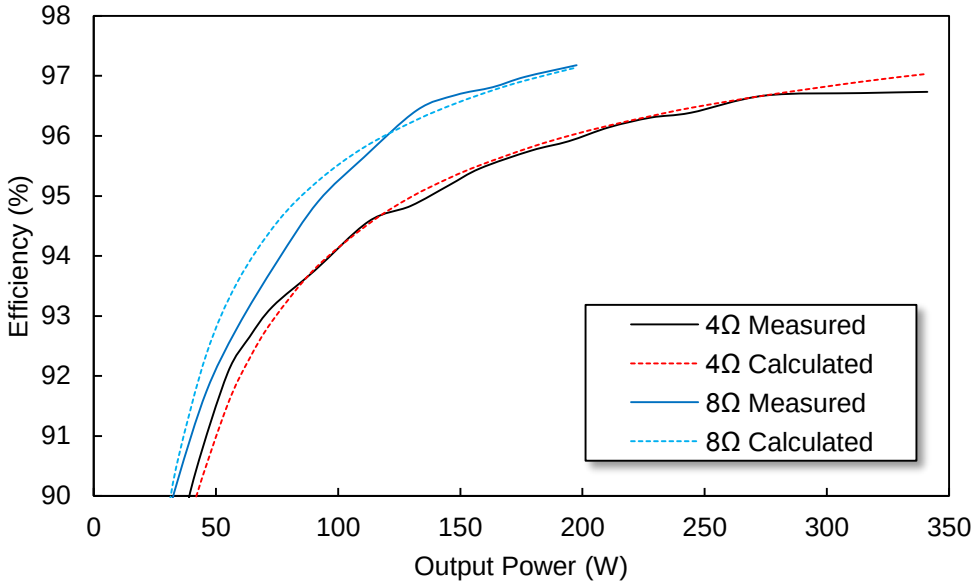

Figure 4.9: Measured and calculated efficiency for 4Ω and 8Ω loads.

4.3.3. Circuit Construction

The power circuit is connected to an Atmel ATMEGA328P microcontroller operating at 16 MHz and the input voltage, output current, and output voltage measurements are taken with an ADS1115, a 16-bit, 4-channel, single ended, sigma-delta ADC with built-in multiplexer, clock and voltage reference. The ADC operates at 860 samples-per-second (sps) with the internal reference set to 4.096V. The output of the buck converter is controlled via an MCP4725 12-bit digital-to-analog converter (DAC) using I^2C communication. The output of the DAC is fed into an LTC6992-3 voltage controlled pulse width modulator with a maximum operation frequency of 1 MHz. The output of the oscillator is fed into an ADUM3221 isolated gate driver to accomplish MOSFET switching. Figure 4.10 illustrates the main components and their connections.

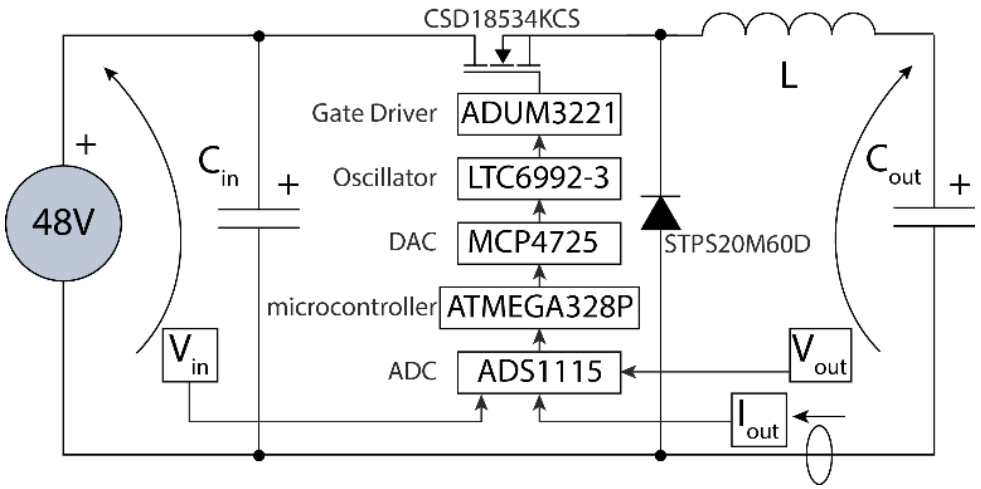

Figure 4.10: Circuit schematic with main component blocks of the PV emulator.

4.3.4. Experimental Results and Discussion

The experimental setup consists of the following: A TDK Lambda Z+ 60V/7A power supply which provides the input current measurement readout and is connected at the input voltage terminal, one Agilent E3631A power supply for driving the gate at 5V, two digital voltmeters to measure input and output voltage, one digital ammeter to measure the average output current and variable 250W and 300W power resistors.

The test criteria in this case are two-fold: the output accuracy is paramount, but the loop speed is also important especially when the devices connected to the emulator have loop speeds ranging in the few kHz. For this work, a decision was made to build a PV module emulator with the highest accuracy possible where a tradeoff was made between higher accuracy and lower loop speed. Therefore, a 16-bit resolution sigma-delta analog to digital converter (ADC) was used over a successive approximation register (SAR) type even though SAR ADCs generally have very good sampling speeds in the 0.1-10 MHz with comparable resolution. However, SAR ADCs also tend to be prone to noise that adds a random non-linear offset to the measurement

which is a significant challenge for good calibration. The only real disadvantage of using a sigma-delta ADC in this case is that the ADC in question, ADS1115, has a maximum sampling frequency of only 860 samples per second along with a delay in the internal analog multiplexer. This means that in order to get valid results in single acquisition mode, there needs to be a 3 ms delay between the data transmission into the ADC where the registers are written, and data output from the device. Since the output current and voltage are sequentially measured within the loop, the loop speed was measured to hover around ~220 Hz. The loop speed discouraged use of an incremental duty cycle control scheme that would have made it easier to clamp the voltage output to V_{oc} without significant oscillation at lightly loaded conditions because it is slower than integrative current-mode control.

The performance of the PV emulator was measured for different current-voltage and power-voltage characteristics as shown in Figures 4.11 and 4.12. For these experiments, V_{oc} was set to a fixed 40V value while I_{sc} values were varied between 0.5-10A in incremental steps. During operation, the emulator was connected to multiple fixed and variable power resistors (i.e. Vishay AVE030020E8R00KE, ranging between 0 and 4 kΩ) and the output voltage and current were recorded when the emulator output settled. The experiments were repeated for different resistance values in small increments and the data points were recorded using multimeters and a camera. The results indicate that the PV emulator can accurately reproduce a wide range of module characteristics.

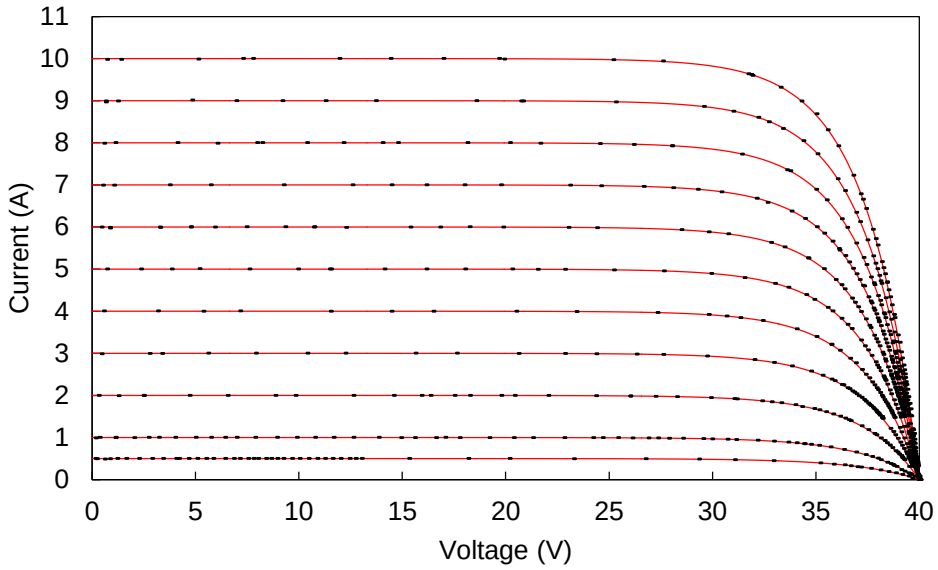

Figure 4.11: Experimental I-V curve results, dots are measurements on simulated red lines.

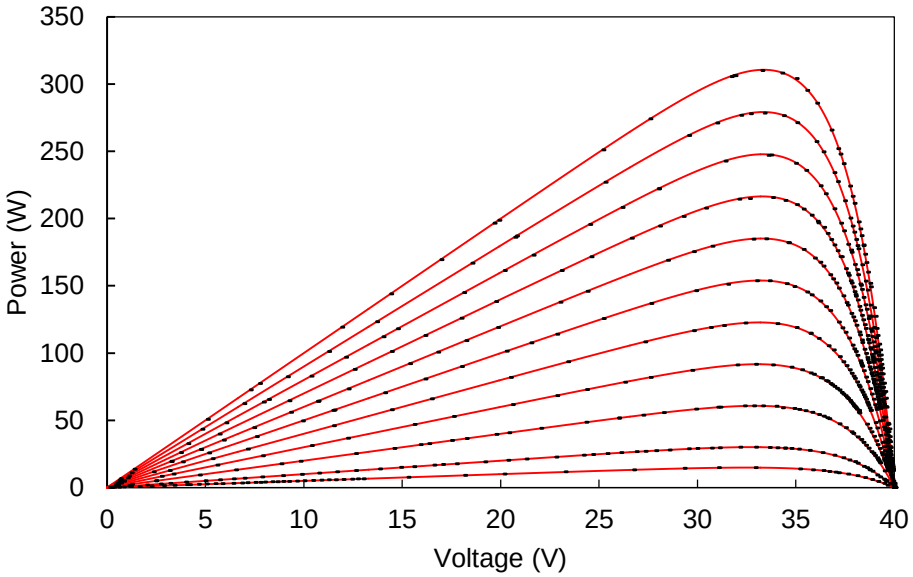

Figure 4.12: Experimental P-V curve results, dots are measurements on simulated red lines.

For the quantitative analysis of the output current and power errors, utilization of the root-mean-square-deviation method (RMSD) was employed as described by Eq. 4.21, below

[86][87]. The results are shown in Table 4.4.

$$i_{RMSD} = \sqrt{\frac{\sum i_{error}^2}{n_{samples}}}, \quad P_{RMSD} = \sqrt{\frac{\sum P_{error}^2}{n_{samples}}} \tag{4.21}$$

Table 4.4: Output Errors of the PV Emulator expressed in RMSD.

I_{sc} (A)	I_{RMSD} (mA)	P_{RMSD} (W)	$n_{samples}$
0.5	4.296	0.142	58
1.0	8.678	0.418	68
2.0	8.113	0.419	58
3.0	21.758	0.754	74
4.0	27.572	0.884	67
5.0	29.704	0.915	65
6.0	40.012	1.106	93
7.0	38.099	1.046	88
8.0	50.152	1.257	78
9.0	53.304	1.283	60
10.0	58.317	1.345	62

Table 4.4 shows that for low values of I_{sc} (0.5A–2A), I_{RMSD} is significantly lower, and as the set short-circuit current increases there is an increase in both current and power RMSD. This is caused by the measurement offset induced by the disturbance at MOSFET turn-on, which is more pronounced at higher output current. As shown in Figure 4.13, at MOSFET turn-on at -2, 0, and 2 µs, the large current surge through the diode interacts with the parasitic inductance of the elements on the return path of the power supply. With the current sensing resistance (R_{sense}) having a datasheet inductance value of 0.5–5 nH, this creates a ground bounce of 185 mV across R_{sense}. The ground bounce voltage has no apparent relation with the current ripple. Once the

ground bounce energy is consumed in the circuit at MOSFET turn-off (at -1.5, 0.5 and 2.5 µs), the voltage spike disappears and the measured voltage across R_{sense} (5 mΩ) corresponds to the current ripple at the output.

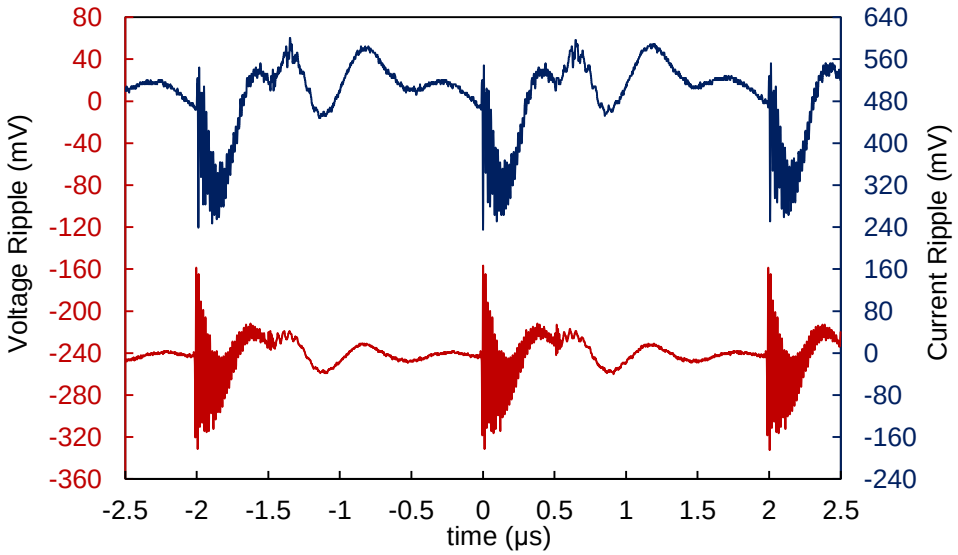

Figure 4.13: Voltage and current ripple waveforms at 48V input and 12V output with an 8Ω load using an HP E3631A power supply.

Figure 4.14 shows the measured switch node voltage across the diode. Although the inductances of the traces of the PCBs have been designed to be at a minimum, the use of a TO-220 packaged MOSFET and diode introduces an inductance at component leads between 10 – 20 nH. The ring frequency of the oscillation was measured as 63.2 MHz. The LC resonance equation shown in Eq. 4.22 can be used to calculate the lead inductance with a known capacitance.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.22}$$

The diode datasheet indicates that the diode has a junction capacitance equal to 500pF at 50V, and when fed into Eq. 4.22, yields a stray inductance of 12.68 nH, which lies within the lead inductance tolerances. The voltage across the diode peaks at 67.25V. Fortunately, the diode has a maximum repetitive peak avalanche voltage rating of 80V and the circuit is safe. Use of surface mount components can significantly reduce the peak value of the voltage overshoot and can also push the resonance frequency of the stray inductance to higher frequencies.

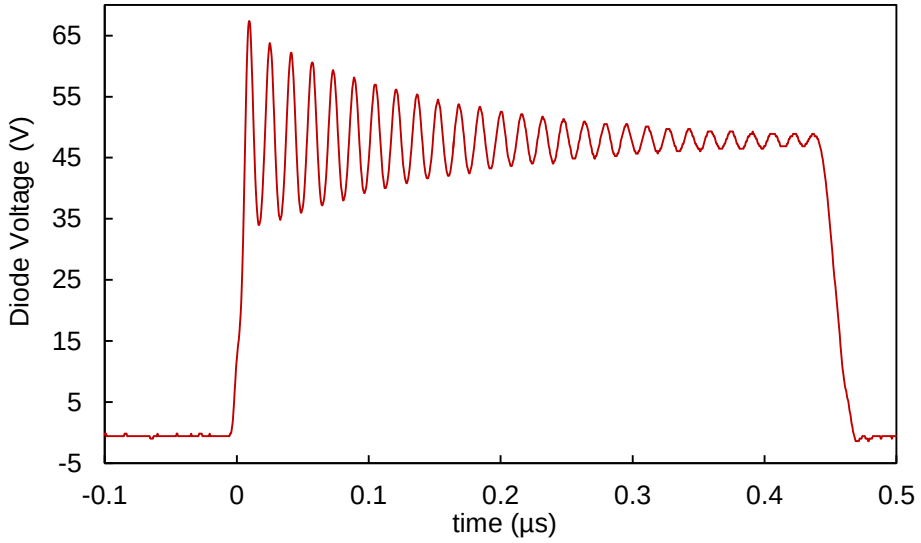

Figure 4.14: Voltage ringing across the diode, with an undesired overshoot of 67.25V at a fundamental frequency of 63.2 MHz.

The voltage overshoot across the MOSFET was insignificant because the input capacitor is placed as closed as possible to the MOSFET. However, the input capacitor cannot completely eliminate the common source inductance between the MOSFET and the diode.

The efficiency vs. output power plots are given in Figure 4.15. In addition to varying the output duty cycle at two fixed loads, the PV emulator efficiency was also recorded from short-

circuit to the maximum power point condition, with maximum efficiencies recorded at the maximum power point. Moving away toward the open-circuit condition from the maximum power point condition, the emulator efficiency significantly improves for lower output power levels due to higher duty cycles with most conduction losses occurring across the MOSFET with much lower on-state losses (Figure 4.15).

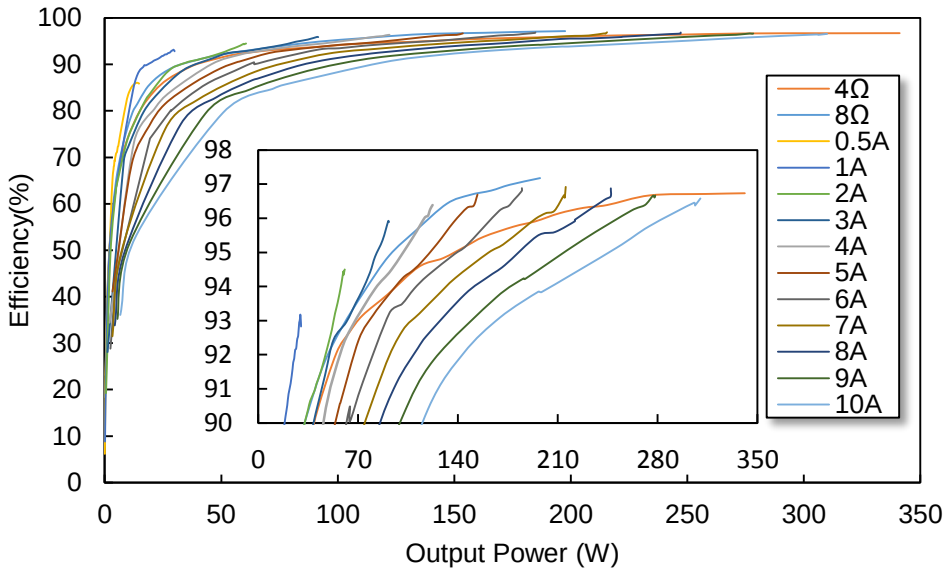

Figure 4.15: Efficiency vs. output power of the PV module emulator.

The vertical portions of the efficiency curve shown in Figure 4.16 correspond to operation between short-circuit and maximum power point conditions, indicating a sharp efficiency rise with increased output voltage and output power while the current stays constant.

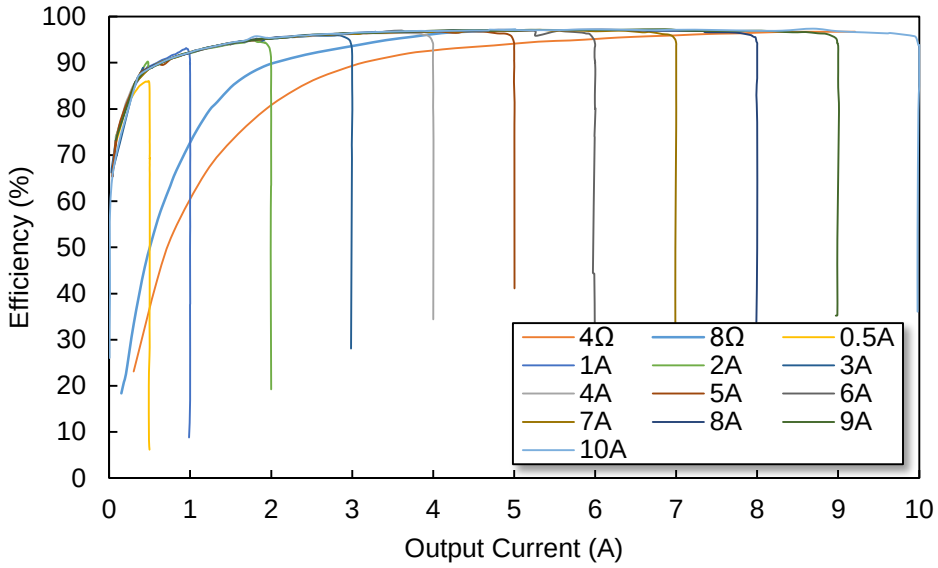

Figure 4.16: Efficiency vs. output current of the PV module emulator.

The increase in efficiency comes from the reduction in conduction losses with the increased on-time of the MOSFET and decreased on-time of the diode. Between maximum power point and open-circuit conditions, the efficiency drops following a smooth maximum efficiency curve that is shared between different emulated I_{sc} values.

Figure 4.17 shows the power loss vs. output power at the same conditions as Figure 4.15. Lower duty cycles lead to large diode losses reinforcing the point that the forward voltage drop of the diode is very critical and should be kept to a minimum for improving power loss and efficiency performance.

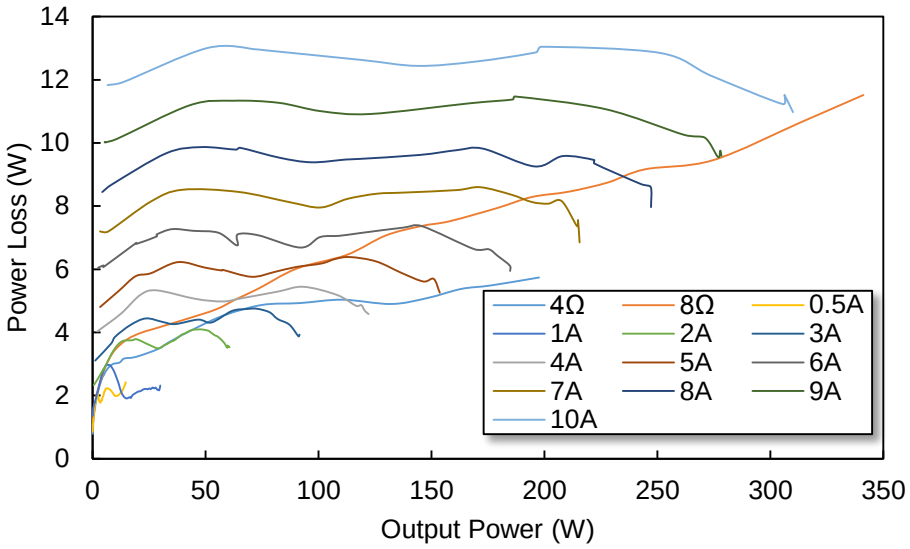

Figure 4.17: Power loss vs. output power of the PV module emulator.

The second generation PV emulator circuit sets out to meet the design challenge of building a low-cost, high power density PV emulator. In doing so, some trade-offs between accuracy, resolution, and loop speed were made. The target of achieving high output accuracy with high resolution measurements was accomplished, yet we believe that the loop speed needs improvement. Current efforts of increasing the loop frequency beyond 220 Hz by staggering measurements of the output current and voltage resulted in the unwanted effect of output destabilization for the PV emulator function of the prototype. The staggered approach works very well for the constant current and constant voltage modes.

Going forward, use of delta-sigma ADCs, while desirable, must be abandoned in favor of SAR ADCs for the loop speed to increase to 10 kHz or more. Another approach to increasing the loop frequency would be to use a microcontroller that is capable of floating point math. This would cut down the equation solving time rather dramatically; however, when all things are considered, the major challenge is the accurate and high resolution measurement of the output

current and voltage values. It is possible to use 12 and even 10-bit converters that are very accurate and very fast, but these converters do not provide enough resolution, especially when the output voltage is concerned. In order to have a voltage accuracy of 1 mV, the ADC must have a resolution of at least 16-bits.

The volumetric power density of the power converter circuit is 20.82 W/cm^3 with dimensions of 33.7 mm x 28.5 mm x 20 mm. When auxiliary components are included, i.e. analog conditioning, digital components, and a manual duty cycle adjustment potentiometer, excluding the microcontroller, the power density of the PV emulator measures at 5.26 W/cm^3 with total dimensions of 50.7 mm x 60.02 mm x 25 mm (Fig. 4.18). It is possible to increase the power density to over 50W/cm^3 by using surface mount components and increase the peak efficiency to over 98% while still retaining the asynchronous buck converter topology.

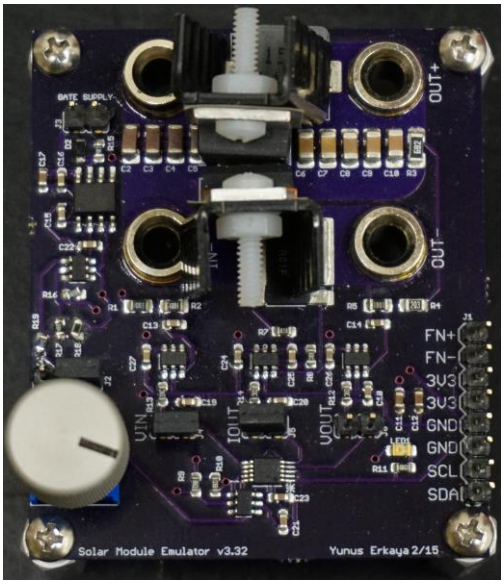

Figure 4.18: Photograph of the second generation PV module emulator.

4.4. Generation 2.5: Improvements to Generation 2 Dynamic Performance

All around improvements were made for Generation 2.5 after learning lessons from Generation 2. General deficiencies about Generation 2 were its general slowness and that it was unsuitable to be tested with dynamic loads. The models used in Generation 1 and Generation 2 devices did not include temperature and irradiance effects to simplify calculations; however, these effects were added, as shown in Chapter 2.

Dynamic and static performance experiments were conducted using the setup shown in Figure 4.19. The setup consists of DC power supplies, 1 GHz bandwidth oscilloscope, digital multi-meters, and the device under test (either high power resistors as shown, or an Enphase M250 inverter for dynamic tests).

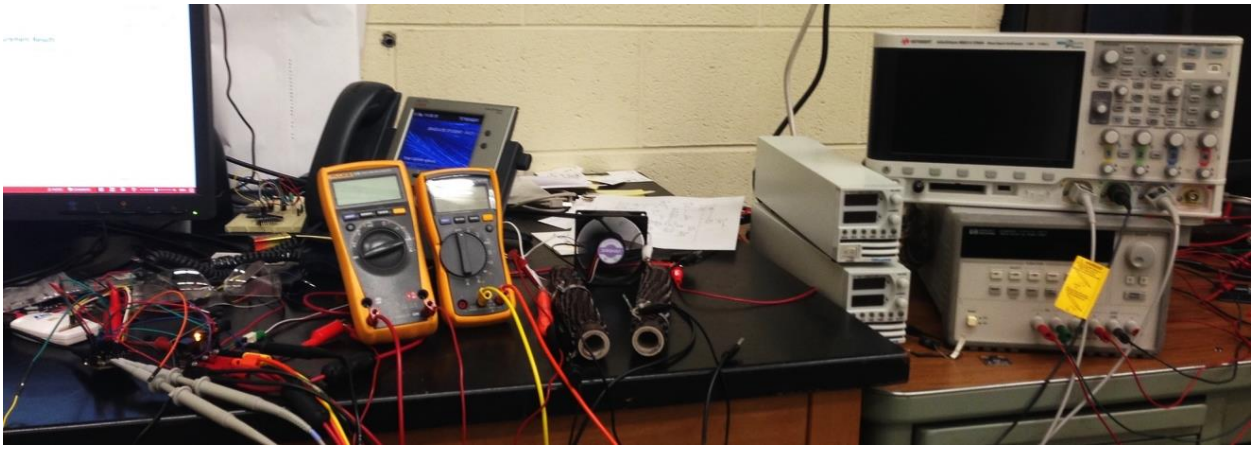

Figure 4.19: PV module emulator test setup.

A look up table initially with 1V increments was set up and once verified, the look up table was converted to a per bit basis running off ADC values which improved program execution, leading to increased loop speeds. The memory of the ATMEGA328P microcontroller

allows for 750 unique points, which is a bit short of the possible 1023 values; however when moved to the ARM Core M4F microcontroller by ST Microelectronics, it was possible to have the full 4095 values corresponding to all ADC bits. The values of voltage and current were scaled into bits using the following formula:

$$I_{pv}[m] = \frac{\left(I_{sc} - I_o \cdot \exp\left(A \cdot m \cdot k_{voltage}\right)\right)}{k_{current}} \tag{4.23}$$

where m is the array index (bit value) ranging from 0 to 750, $k_{voltage}$ and $k_{current}$ are the scaling factors for voltage and current with units in bits per voltage and bits per amperes, respectively. The algorithm also converts all values below zero to zero in order to use unsigned integer values for better memory utilization.

The external ADS1115 ADC was abandoned in favor of the internal ADC of the ATMEGA328P microcontroller for increased measurement speed, which brought together increased offset errors caused by the switching transient noise. The sampling time of the internal ADC was reduced to a minimum value, which allowed for operation with tolerable errors. This resulted in a loop frequency of 8.62 kHz, a large increase from the loop frequency of 220 Hz obtained in generation 2.

For the dynamic tests shown in Figures 4.20 and 4.21, V_{oc} was set to 40V and I_{sc} was set to 7V. The ideal diode model, which includes temperature and irradiance effects, was used as discussed in Chapter 2. The measurement points correspond to different digital proportional and integrative constant K_p, K_i values of 0.9 to 1.4. For higher I_{sc} values, lower K_p and K_i values performed just as good as higher values; however, for lower I_{sc} values, it was necessary to increase K_p and K_i, otherwise the circuit would not converge to MPP. Nevertheless, these results are preliminary for dynamic tests and the circuit was not fully optimized. These tests were conducted as a proof of concept for working with dynamic loads. These tests will form the basis

for the improved PV module emulator discussed in Chapter 5.

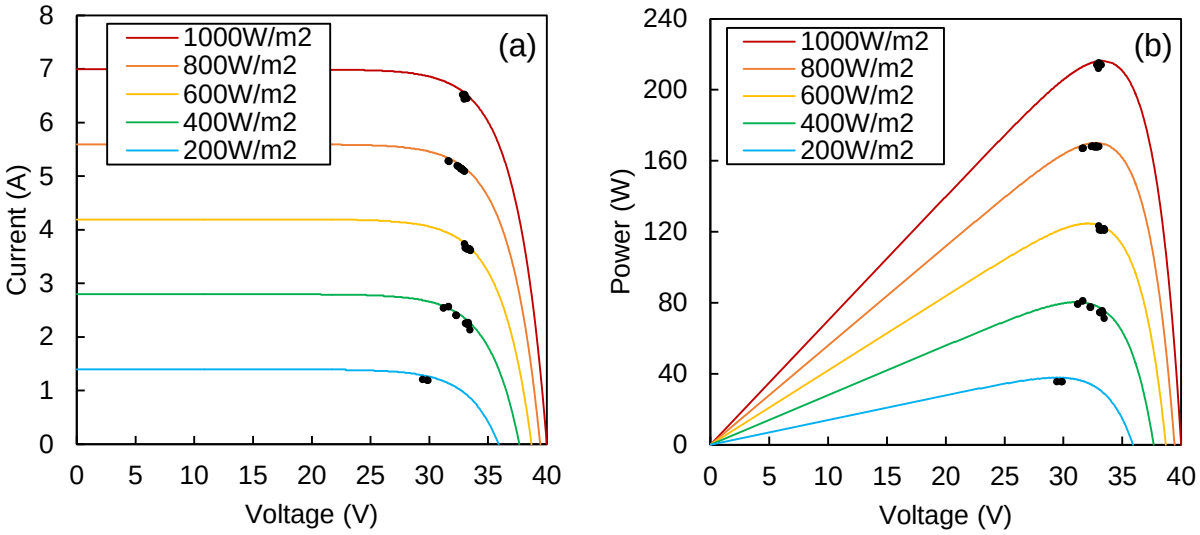

Figure 4.20: Measured operation points (black dots) on simulated I-V (a) and P-V (b) curves (color lines) at constant temperature (25°C) for different irradiance values.

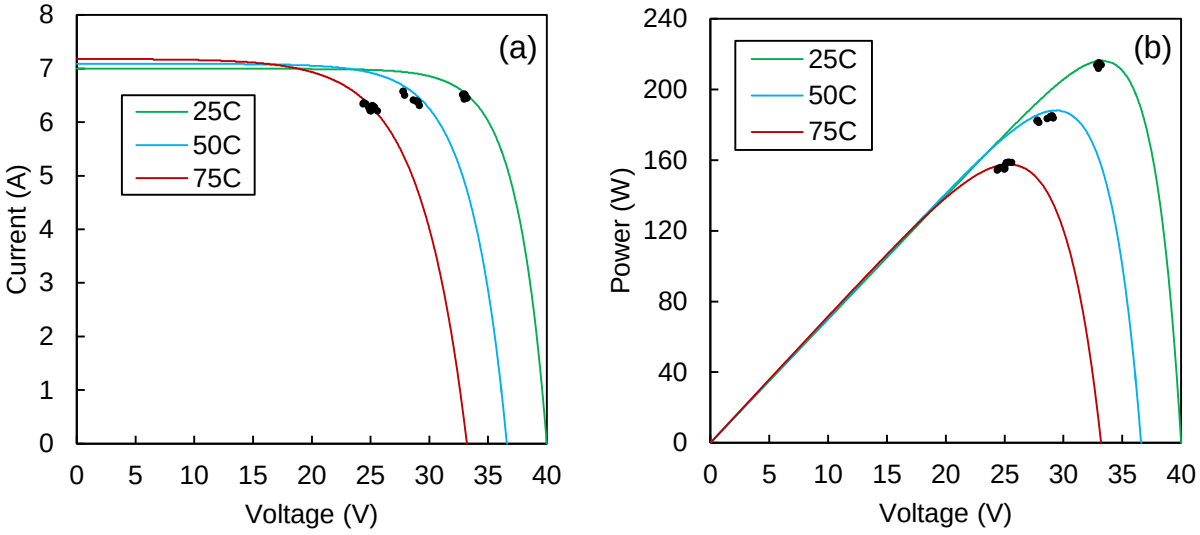

Figure 4.21: Measured operation points (black dots) on simulated I-V (a) and P-V (b) curves (color lines) at constant irradiance (1000W/m^2) for different temperature values.

4.5. Conclusions

Various prototypes were built following an in-depth literature review for emulating PV modules. The efforts produced different circuits as meant to work as a proof of concept with Generation 1, and to build on the experience and minimize steady-state output errors in Generation 2. Generation 2.5 makes improvements towards enhancing the dynamic capability of the module emulator to test dynamic loads such as inverters which track the MPP of the emulated curve.

In Generation 1, the ideal diode model was chosen and the PV equation was solved at every loop iteration. This circuit was built as a proof of concept and due to the lack of optimizations, the algorithm loop speed and circuit efficiency were not deemed important. Rather, the desire was to see if it was possible to model PV modules effectively with minimal errors using buck converters.

In generation 2, the idea was to enhance the Generation 1 circuit with the use of a higher switching frequency to reduce the size of the passive components, and to improve upon the steady state errors of the emulated PV output. This created challenges that had to be overcome, mainly in generating the fast frequency with very high resolution and measuring the output accurately to improve the steady state error. The power losses when compared to Generation 1 were minimized through extensive mathematical calculations and appropriate parts selection. However, the power losses were still too high to enable long term testing, especially without the use of active cooling fans.

With the encouraging results of Generation 2, the circuit was tested with a dynamic load to see how it would perform. The circuit generally defaulted to between 16-20V operation with the output current equal to I_{sc}. This led to the conclusion that the loop speed was the culprit and

with further investigation, Generation 2.5 was developed.

In Generation 2.5, the external ADC that allowed the minimization of steady-state errors was abandoned in favor of a faster loop speed. Through optimizations of the internal ADC, a loop speed upwards of 8 kHz was achieved. The higher loop speed permitted testing dynamic loads.

In order to make significant enhancements to the static performance, dynamic performance, power density, and efficiency, a faster microcontroller and a synchronous buck converter topology is necessary. The methods to achieve these design goals are discussed in Chapter 5.

CHAPTER 5

EMULATION OF PHOTOVOLTAIC MODULES USING GANFET DEVICES

5.1. Introduction

Significant changes are required to improve the performances of the PV emulators discussed in Chapter 4. In this chapter, GaN high electron mobility transistors (HEMT) are explored in developing a high performance PV module emulator with a high loop speed, a high power density, high efficiency, minimized parts count, optimized layout, and improved dynamic performance. The choice for using GaN devices was made as they allow for significant compactness and increased efficiency when compared to traditional silicon devices as demonstrated in Chapter 4.

Unlike previous efforts, PV module characteristics will not be modelled on the fly between iterations, but rather the full curve will be modelled before the power stage is turned on, and the model will be stored in memory. This results in fast data point generation between iteration to reduce overhead, while increasing the dynamic characteristics of the emulator.

5.2. Algorithm Development

In order to reduce parts count and circuit complexity, the ST Microelectronics STM32F334K8 microcontroller was chosen for its 32-bit operation, ARM Cortex M4 core with floating point support, 64 KB Flash, 16 KB SRAM, 5 Msps (million samples per second) fast analog-to-digital converters (ADC), and high-resolution timer (HRTIM) with 217 ps (picosecond) resolution. A printed circuit board was designed to evaluate the performance of the microcontroller as shown in Figure 5.1.

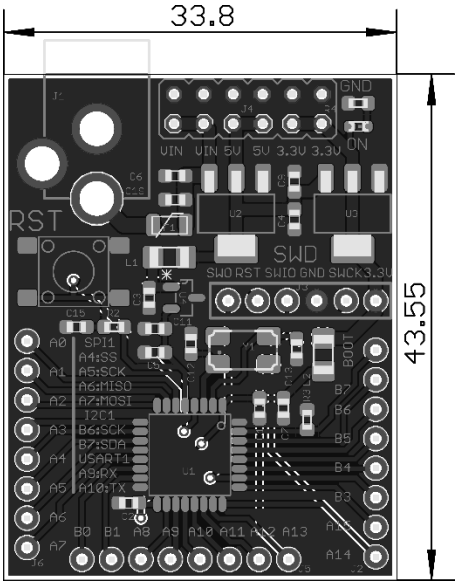

Figure 5.1: STM32F334K8 development board.

When building synchronous buck converters with digital control, the control algorithm and firmware are critical for the proper operation of the circuit. The firmware consists of six parts: ADC converter setup and triggering, HRTIM setup and signal generation, photovoltaic I-V curve model, error calculation, proportional-integrative (PI) controller setup with anti-windup, and the changing conditions function.

5.2.1. Analog-to-Digital (ADC) Converter Setup and Triggering

The two built-in 12-bit ADCs named ADC1 and ADC2 are used for sampling output current I_{out} and output voltage V_{out} respectively. ADC1 is configured for a sampling frequency of 2.25 Msps, using input channel 2, single channel sequence, single conversion with hardware trigger enabled using HRTIM ADC trigger 1 event (internal signal from on chip timers). ADC2 is configured for a sampling frequency of 3.6 Msps, using input channel 1, single channel sequence, single conversion with hardware trigger enabled using HRTIM ADC trigger 1 event (internal signal from on chip timers). ADCs 1 and 2 are running independently off of the same

trigger source which allows for flexibility when reading the converted values from their respective registers (ADC1_DR and ADC2_DR) while taking simultaneous measurements.

5.2.2. High Resolution Timer (HRTIM) Setup and Signal Generation

The high resolution timer allows for generating pulse width modulation signals with very high resolution with the HRTIM clock running at 4.608 GHz (144 x 32 MHz) when the clock source is chosen as the internal phase locked loop (PLL) and the pre-scaling ratio is 1. The resolution of the HRTIM clock at this frequency is 217 picoseconds, which allows a minimum switching frequency of 70.3 kHz. The DLL calibration period for the HRTIM is set to 14 µs. To prevent switch-on overlap at the buck converter, a dead-time of 14.76 ns is inserted at the rising and falling edge of the output of HRTIM Timer A Channel 1. The HRTIM counter is set to operate at a continuous mode with the set register configured at the HRTIM Timer A Period, and the reset register configured to HRTIM Timer A Compare 1.

HRTIM Timer A, therefore, begins counting from 0 until HRTIM Timer A period and overflows back to zero to be repeated infinitely. The period value is adjusted so that the switching period of the buck converter can be adjusted in 217 ps increments. The value of period for the converter running at a frequency of 100 kHz is 0xB400. The reset occurs at HRTIM Timer A Compare 1 instead of zero because the minimum recommended reset value has to be greater than or equal to 3 periods of the HRTIM clock frequency (0x60), which is defined as *duty_min* and is set to 0x20. The HRTIM Timer A Compare 2 register is initialized at 50% duty cycle *half_period* to trigger the ADCs at the middle of the switching period.

Finally, the HRTIM Timer A is enabled with outputs Channel 1 and Channel 2 (inverted) enabled. Channel 1 is connected to drive the switching MOSFET and Channel 2 is connected to drive the synchronous MOSFET of the synchronous buck converter. General purpose input

output (GPIO) PA8 and PA9 are connected to Channel 1 and Channel 2 of the HRTIM respectively through the alternate function register.

5.2.3. Photovoltaic I-V Curve Model

The ideal diode model is chosen for modeling photovoltaic modules within the emulator. The emulator receives the cell temperature T_{cell}, open-circuit voltage V_{oc_stc} and short-circuit current I_{sc_stc} at standard testing conditions (STC), the dark saturation current I_o, the irradiance S, the short-circuit temperature coefficient *alpha_Isc* and the open-circuit voltage temperature coefficient *alpha_Voc*. The microcontroller performs the calculations of short-circuit current I_{sc}, diode saturation current I_o and A, the diode ideality factor multiplied by the thermal voltage ($n \cdot V_t$), and is outlined in Chapter 2.

The I-V curve is calculated and placed in a 4096-value look-up table (LUT) corresponding to the unique conversion bits of the ADCs. The values of the LUT are generated using the function shown below,

$$I_{pv}[m]\Big|_0^{4095} = \frac{I_{sc} - I_o \exp\left(A \cdot m \cdot k_{voltage}\right) + I_{offset}}{k_{current}} \tag{5.1}$$

where $I_{pv}[m]$ is the LUT array of the photovoltaic current, m is the array element, I_{sc} is the short-circuit current, I_o is the dark saturation current, A is the diode ideality factor multiplied by the thermal voltage ($n \cdot V_t$), $k_{voltage}$ is the voltage gain, I_{offset} is the current offset and $k_{current}$ is the current gain. The voltage gain and current gain are chosen to accommodate the highest expected output voltage and output current measurements.

The voltage gain is dependent on the output voltage resistor divider ratio, the ADC reference voltage (V_{ref}) and the maximum ADC conversion value $2^{12} - 1 = 4095$.

$$k_{voltage} = \frac{V_{ref} \cdot Resistor\_Divider\_ratio}{Max\_ADC\_Value} \tag{5.2}$$

The current gain is dependent on the current transducer's sensitivity *Sens* (V/A), the ADC reference voltage V_{ref} and the maximum ADC conversion value $2^{12} - 1 = 4095$.

$$k_{current} = \frac{V_{ref}}{Sens \cdot Max\_ADC\_Value} \tag{5.3}$$

The current offset is dependent on the current transducer's voltage output at zero current $V_{IOUT(Q)}$, and the current transducer's sensitivity *Sens* (V/A).

$$I_{offset} = \frac{V_{IOUT(Q)}}{Sens} \tag{5.4}$$

If modeling partial shading is necessary, the microcontroller calculates the photovoltaic current $I_{pv}[m]$ in a piece-wise fashion:

$$I_{pv} = \begin{cases} if\ I_{pv_{unshaded}}[m] > I_{sc_{shaded}}[m]; & I_{pv_{unshaded}}[m] \\ else\ if\ I_{pv}[m] > I_{sc_{shaded}}[m]; & I_{sc_{shaded}}[m] \\ else\ I_{sc_{shaded}}[m] \geq I_{pv}[m]; & I_{pv}[m] \end{cases} \tag{5.5}$$

$$I_{pv_{unshaded}}[m]\Big|_0^{4095} = \frac{I_{sc} - I_o \exp\left(A \cdot m \cdot \frac{k_{voltage}}{(1 - System\_Shading)}\right) + I_{offset}}{k_{current}} \tag{5.6}$$

$$I_{sc_{shaded}}[m]\Big|_0^{4095} = \frac{I_{sc} \cdot (1 - Shading\_Strength) + I_{offset}}{k_{current}} \tag{5.7}$$

where $I_{pv_{unshaded}}[m]$ is the photovoltaic current generated by the unshaded section of the PV module, $I_{sc_{shaded}}[m]$ is the short-circuit current of the shaded section of the PV module, *Shading_Strength* is the shading strength and *System_Shading* is the percent area of the PV module shaded. For example, a 20% shading strength results in 80% of the irradiance arriving at the PV module causing the short-circuit current of the shaded portion to be 20% less than the unshaded portion. For a typical 60-cell module, 20% system shading will mean that 12 cells will be shaded and will output less power.

The piece-wise partially shaded I-V current waveforms assume the existence of a fully conducting bypass diode as outlined in Chapter 2.

5.2.4. Error Calculation

In order to keep the loop frequency as fast as possible, the algorithm needs to run in the most efficient way possible. The 12-bit ADCs output a value ranging between 0 and 4095 and these values are stored in the ADC regular data registers for ADC1 and ADC2. The converted values are fetched using unsigned 32-bit pointers **current_ptr* and **voltage_ptr* directly addressing the ADC regular data registers ADC1_DR and ADC2_DR. The ADC readings are not converted to either volts or amperes to save on calculation time and are immediately compared to the desired I_{out} value using,

$$error = I_{pv}[*voltage\_ptr] - *current\_ptr \tag{5.8}$$

where the LUT array element is the measured voltage (in bits) which operates as a voltage controlled current source with each unique ADC voltage reading having a corresponding current output, i.e. $I_{pv}(V_{out})$.

5.2.5. PI Controller with Anti-Windup

The controller chosen is a proportional and integrative controller with the proportional portion directly driving the output in relation with the error and the integrative component accumulating the error at each iteration. The output of the controller is the sum of the proportional and the integral components. The integrator is bounded by 0 and 90% duty cycle, while the output is bounded by the minimum duty cycle (0.07%) and the maximum duty cycle (90%) to prevent wind-up. Both the proportional constant K_p and integral constant K_i are set to 0.1.

The duty value is then passed on to the unsigned 32-bit pointer **duty_ptr* to directly update the HRTIM Timer A Compare 1 register to alter the duty cycle.

If the duty cycle is equal to or greater than 50%, the Compare 2 register used to trigger the ADCs is updated with an unsigned 32-bit pointer **compare2* to duty_cycle/2 -15% duty cycle trigger. If the duty cycle is less than 50%, then **compare2* is fixed to 60% duty cycle.

The PI function runs within the SysTick interrupt set to 100 kHz operation, which is set by dividing the System Core Clock (72 MHz) by 100,000. The SysTick timer also updates the counter at 10 µs intervals to program irradiance, temperature and partial shading changes. The maximum measured loop frequency when all functions are running is 287.3 kHz. Figure 5.2 demonstrates the time it takes all functions (static conditions) to run along with the 10 µs SysTick timer interval. This shows that the switching frequency of the circuit can be increased while keeping cycle by cycle control up to 285 kHz.

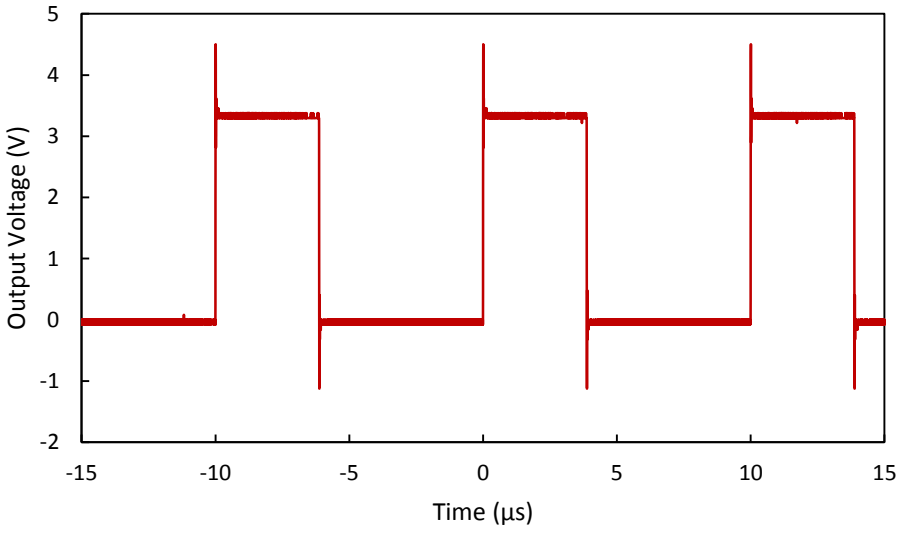

Figure 5.2: Measured SysTick timer interval and algorithm speed.

5.2.6. Programming Changing Conditions

In order to emulate changing conditions of irradiance, temperature, and system shading percentages, three functions are set up for the three specific changes. Due to the two minute start-up delay of the Enphase M250 microinverter used for testing changing conditions, the PV module emulator waits for 2 minutes before initiating the changes.

The step irradiance function allows for adjusting different irradiance levels and the speed of the irradiance change from one level to another. Similarly, the step temperature function allows for programming the different temperature steps, the temperature ramp rate, and wait time between temperature steps. The programs require the recalculation of the specific constants (voltage, current, band gap, etc.) and the 4096 value LUT. Doing so requires overhead taking about 0.25 seconds per calculation.

The step system shading function also has similar functions of different system shading percentage steps, ramp rate, and wait time between the steps; however, unlike the previous two functions, only the 4096 value LUT needs to be recalculated since the module is operating at the same irradiance and temperature conditions. This function also requires about 0.5 seconds per calculation.

5.3. PV Emulator Circuit Construction

The block diagram of the proposed PV module emulator is shown in Figure 5.3. The PV module emulator operates as a voltage controlled current source and the basic functions I-V curve generation, LUT, error calculation, PI controller, high resolution PWM generation, the power stage and the output voltage and current measuring stages are shown along with the load connection.

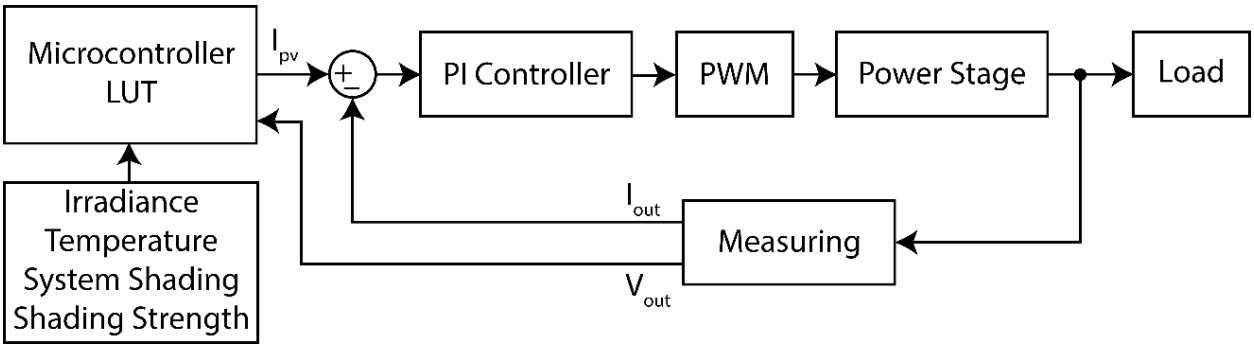

Figure 5.3: Block diagram of the proposed PV module emulator.

The circuit is designed to operate in one of the following modes: constant current, constant voltage, constant power, and PV module emulation. The constant current and constant voltage modes allow for tuning the circuit constants ($k_{voltage}$, $k_{current}$) and the ADC trigger points to minimize measurement and output errors from 0-40V and 0-10A.

5.3.1. Circuit Topology

The photovoltaic module emulator is based on a synchronous buck converter as shown in the simplified circuit schematic in Figure 5.4.

A voltage source rated at 48V is connected at the left and the input voltage is filtered through the input capacitor C_{in}. The main switch is Q_1 and switches either fully on or fully off depending on the desired output voltage. Q_2 turns on when Q_1 is off and turns off when Q_1 is on to provide a low voltage circulation path for the output current. This is accompanied by a dead-time inserted between the two switches turning on to prevent both Q_1 and Q_2 being on at the same time, also known as shoot-through. L is the output inductor, which keeps the current flowing when Q_1 is switched off. C_{out} is the output capacitor used to filter the output voltage.

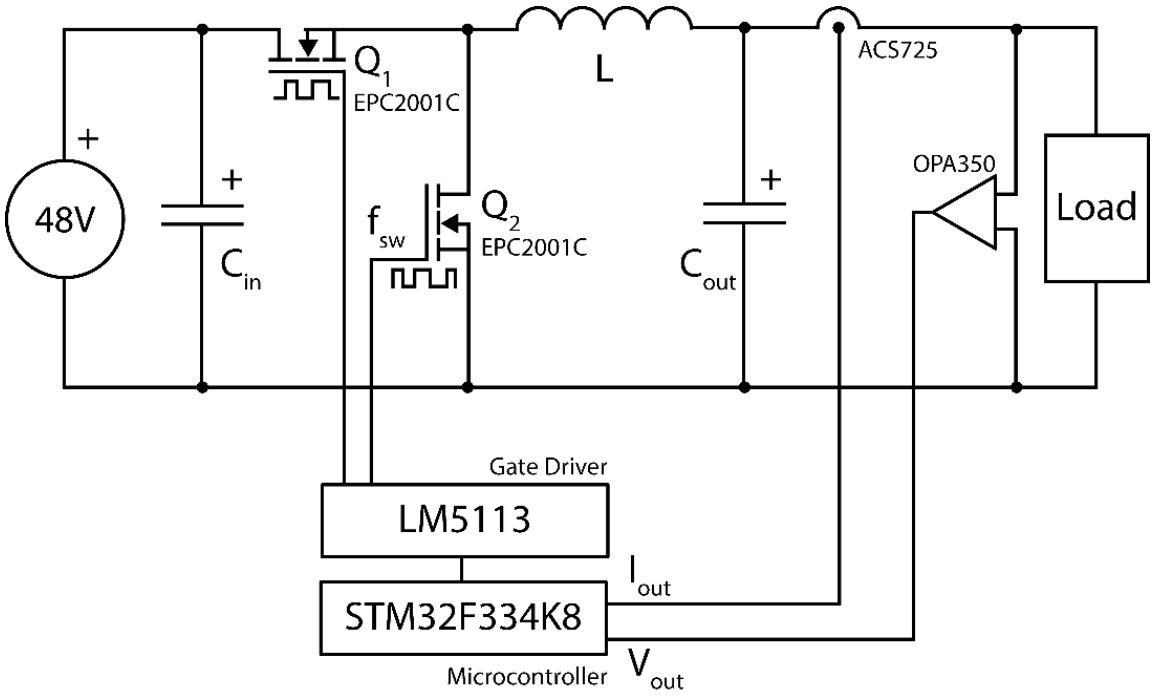

Figure 5.4: Simplified circuit schematic of the proposed PV emulator.

5.3.2. Component Selection

The circuit consists of four boards, the STM32F334K8 development board which houses the microcontroller circuit (Fig. 5.1), the power board which houses the buck converter circuit (Fig 5.5), the current board consisting of the current measurement IC (Fig 5.6), and the voltage measurement circuit consisting of the voltage divider resistors and the operational amplifier on a breadboard. The power board is 1oz. Cu (35µm), 1.6mm thick, two-layer, two-sided construction, measuring 38mm x 51mm.

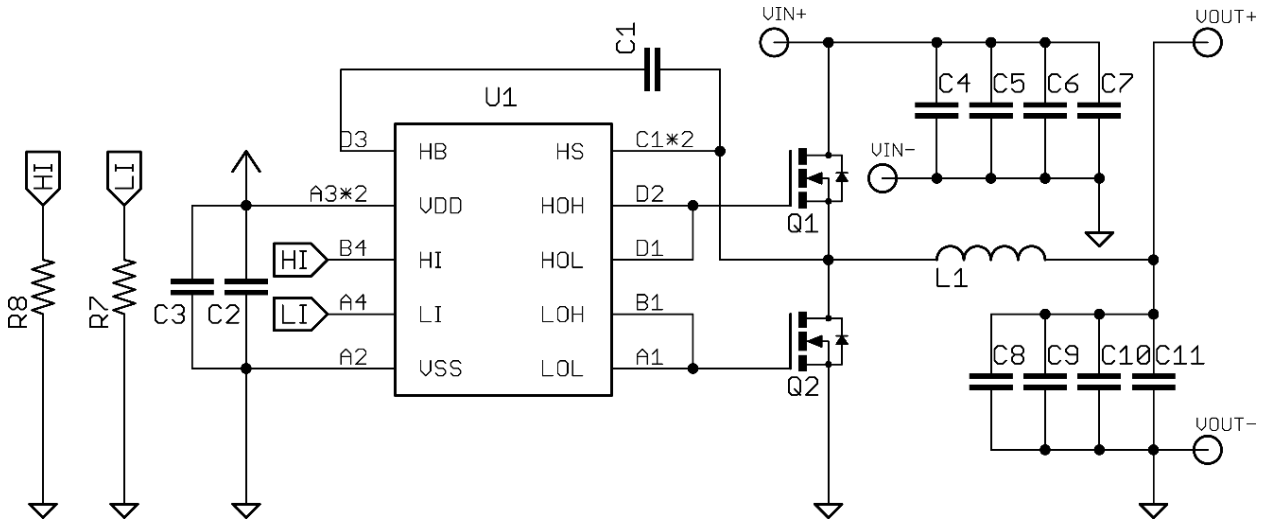

Figure 5.5: Detailed schematic of the power board.

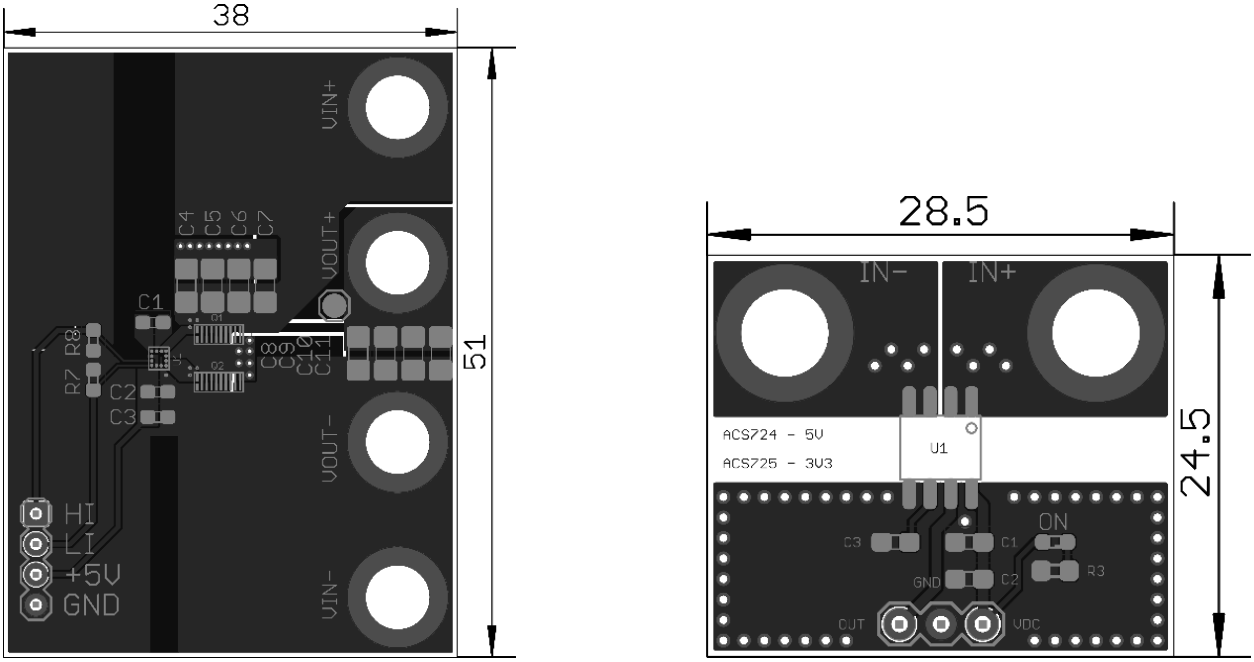

Figure 5.6: Power board (left) and current board (right) design (dimensions are in mm).

The output current is measured through the use of an Allegro ACS725 current measurement IC and the output voltage is measured through a voltage divider resistor connected

to a Texas Instruments OPA350 operational amplifier configured for a unity gain operation. The output of the operational amplifier is connected to a RC low-pass filter circuit (R=100Ω, C=0.1μF). The output voltage and current values are measured by the ST Microelectronics STM32F334K8 microcontroller and the switching signals are connected to the Texas Instruments LM5113 half-bridge gate driver.

With the introduction of the LM5113 gate driver from Texas Instruments, it is possible to drive enhancement-mode GaN on silicon devices at up to 10 MHz with little worry for gate protection and special circuitry at up to 100V input [91]. The LM5113 does not have a dead-time control circuit and instead has separate high-side and low-side inputs to allow the microcontroller to dictate the dead-time control. Similarly, the LM5113 provides two outputs each for the high-side and low-side switches for separate turn on and turn off paths, which allow for tuning the turn-off and turn-on times through the use of different gate resistors. For the proposed emulator, the outputs were connected without the use of external gate resistors to increase switching speeds.

For a high density and high efficiency design, the synchronous buck converter circuit is set to operate at a switching frequency of 100 kHz. The switching frequency can be increased during low output power operation to further increase dynamic response. All emulator properties are shown in Table 5.1.

An inductance value of 33 μH was chosen to limit ripple current below 4A at 100 kHz operation (40%). A 48V limit on the input was imposed to protect the GaN devices from possible voltage spikes that can cause a breakdown. The EPC2001C device from Efficient Power Conversion Corporation was chosen for its low on-state resistance $R_{ds,on}$ of 7 mΩ and low gate charge Q_g of 9 nC. Latest generation traditional silicon MOSFETs cannot compete with the low

figure of merit ($R_{ds,on}$*Q_g) offered by GaN devices [92].

Table 5.1: Properties of the GaN-based PV Emulator.

Symbol	Part Name	Value or Model
L	inductor	Wurth Electronics 7443643300, 33 μH
C_{in}	input filter capacitor	4x 4.7 μF
C_{out}	output filter capacitor	5x 10 μF
V_{in}	input voltage	48V
V_{out}	output voltage	0 – 40 V
I_{out}	output current	0 – 10 A
f_{sw}	switching frequency	0.1 – 1 MHz
Q_1, Q_2	100V GaN MOSFET	Efficient Power Conversion, EPC2001C

5.3.3. Switch Node Voltage Overshoot and Ringing

The circuit shown in Fig. 5.7 contains the GaN devices (Q1, Q2) in the middle and the gate driver (U1) just above them, with the input capacitors (C4-C7) placed as close as possible to reduce the size of the input power loop. The inductor is on the reverse side of the board to save space. Placing the inductor on the reverse side does not have an adverse effect due to the positive impact from the increased parasitic inductance caused by the multiple vias; however, the vias used for the input capacitor ground connections will impact performance and contribute to a higher switching noise at the switch node.

Switch node voltage overshoot and ringing occurs due to the parasitic inductances and parasitic capacitances within the printed circuit board (PCB) contributed by the GaN devices Q_1 and Q_2, the output inductor L and the PCB traces. The use of a two-layer PCB highly limits circuit layout optimizations possible for reducing the parasitic elements; layout optimizations

were made to reduce the path between C_{in} and the switches Q_1 and Q_2.

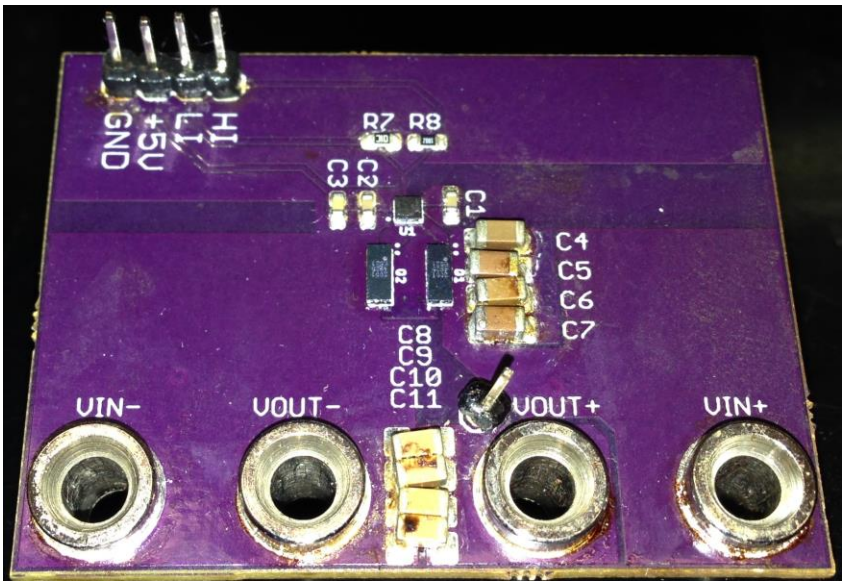

Figure 5.7: Photograph of the populated PV module emulator.

The EPC2001C devices are supplied in passivated die form with solder bars and are not packaged like conventional silicon MOSFET devices. This reduces the parasitic inductance caused by the bonding wires needed to connect the package to the die, and instead, all connections are provided on the bottom with a separate connection for the gate return path to reduce the gate circuit loop inductance which delays the gate driver from changing the output states.

The inductor L also contributes to the voltage overshoot and ringing due to its parasitic capacitance between the windings. The inductor was chosen to have an inductance value larger than 30 μH with the lowest possible DC resistance of 2.4 mΩ. The datasheet of the inductor indicates a resonant frequency of 7 MHz, corresponding to a parasitic capacitance of,

$$f = \frac{1}{2\pi\sqrt{LC}} \rightarrow C = \frac{1}{L(2\pi f)^2} = \frac{1}{33 \cdot 10^{-6} \cdot (2\pi \cdot 7 \cdot 10^6)^2} = 15.66 \text{ pF} \qquad (5.9)$$

As shown in Fig. 5.8, the peak voltage overshoot at the switch node during Q_1 turn on measures 63V for 48V input, and reduces the safety margin of the GaN device to 37V. The turn-on time is below 10 ns without external gate resistances connected.

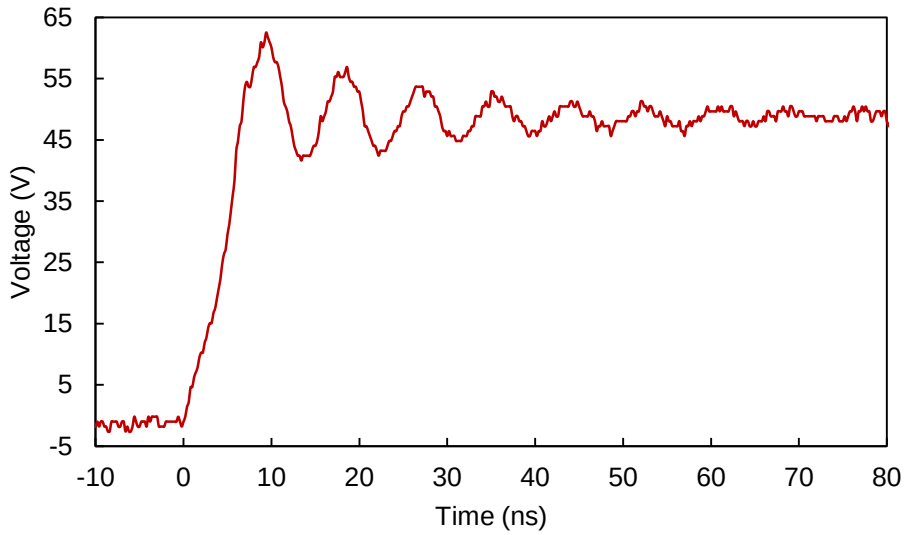

Figure 5.8: Measured switch node voltage at high-side MOSFET turn-on.

The turn-on spike can be reduced by placing an external gate resistor between the gate driver and the high-side GaN switch; however, this will slow down device turn-on and will increase switching losses which are greater at increased frequencies.

The switching algorithm employs a dead time $t_{deadtime}$ of 15ns both at turn-on and turn-off, providing a safe switching margin to prevent shoot-through as seen at the input; however, it reduces the efficiency due to increased body diode conduction losses, especially at higher switching frequencies and output current.

5.3.3. Circuit Efficiency

One of the design goals of the PV emulator is to have very high operational efficiency so that the circuit can run for a long time without the need of active cooling or high temperature shutdown protection. To test the circuit efficiency at different output current levels, 2 300W 8Ω resistors (Vishay AVE030020E8R00KE) were connected in parallel for a 4Ω load (4.25 Ω actual with connectors and cabling), so that the output voltage can be kept below 40V to protect the output capacitors that are rated for 50V (Murata GRM31CR61H106KA12L). The input power supply used for the tests is the TDK Lambda Z60-7-U rated for 60V and 7A output, and with a 48V input and 4Ω load, the maximum input power is 350W and the maximum output current is 9A. Figure 5.9 demonstrates the efficiency observed at different frequencies.

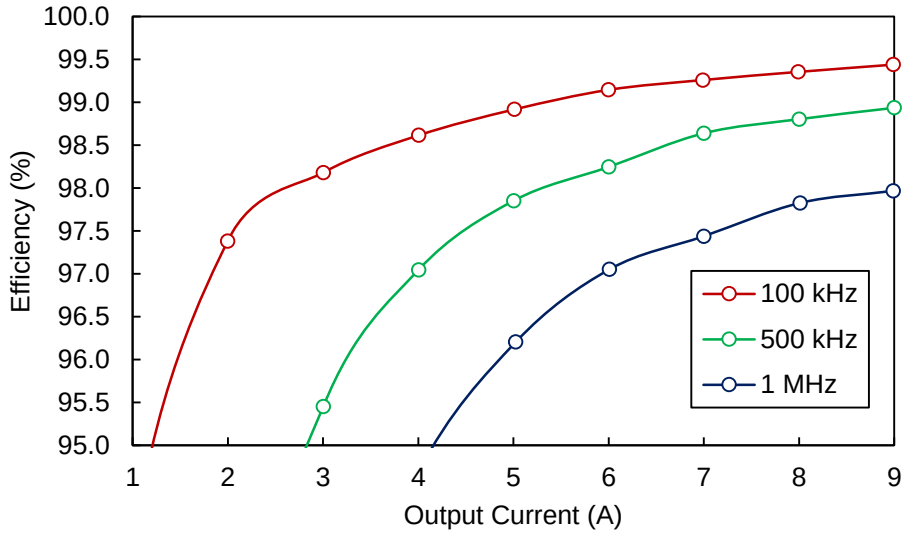

Figure 5.9: Efficiency vs. output current for a 4Ω load.

The efficiency was calculated by taking independent simultaneous measurements of the input voltage, input current, output voltage, and output current using digital meters (Fluke 115).

With a switching frequency of 100 kHz for 9A output (344W), the observed maximum efficiency was 99.4% with 1.94W loss. With the total height of the emulator at 20.1 mm (due to inductor), the power density is 144.7W per cubic inch (8.8 W/cm$^{3)}$ at 344W output. It is possible to increase the power density using an inductor with a reduced height and smaller connectors to reduce the PCB dimensions.

5.4. Performance under Static and Dynamic Conditions

The performance of the PV module emulator was tested for both static and changing conditions using a constant voltage electronic load and an Enphase M250 microinverter. The constant voltage electronic load was used to evaluate the output errors at different operating points, and the inverter was used to test maximum power point (MPP) accuracy and observe MPP tracking for static and changing conditions.

The Enphase M250 inverter has a DC MPPT range of 27-39V, a maximum DC current rating of 10A, maximum continuous output power rating of 240W and operates at either 208Vac or 240Vac nominal with an AC output current of 1.15 or 1A respectively. The inverter is configured to run at 208Vac three-phase power with L1, L2, neutral and ground connections. The inverter performs a resistance measurement between the PV module negative input and the earth ground, and if for any reason these two connections are shorted, the inverter triggers a DC resistance low fault and requires an Enphase Envoy to clear this condition [93]. Therefore, a floating input is required at the PV emulator side.

The constant voltage electronic load was built for the purposes of testing the PV module emulator at fixed voltage steps, rather than having to measure the output performance using high power variable resistors as has been done in Chapter 4. The load itself is rated to only 100W and

does not allow the full characterization of the PV emulator output for currents above 3A. The electronic load failed at 36.67V and 3A (110W) and requires significant cooling capacity to operate above these values. The electronic load is shown in Figure 5.10.

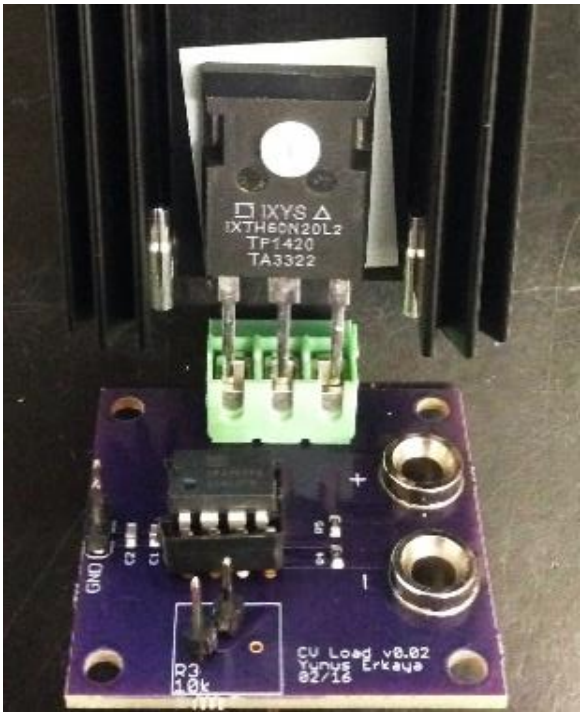

Figure 5.10: Constant voltage electronic load that uses a MOSFET in linear operation.

5.4.1. Static Condition Performance

The static conditions evaluated with the inverter are for different system shading values ranging between 0 – 20% in 5% increments. The PV module values are V_{oc} = 40V, I_{sc} = 8A and I_o = 10µA to limit the PV module output to below 240W (inverter limitation). Shown in Figure 5.11, the highest peak is observed with 0% system shading and the gradually diminishing peak outputs correspond to 5%, 10%, 15%, and 20% system shading. The shading strength was set to

50% so that the shaded cells only receive 50% of the available irradiance. The solid colorful lines are the simulated curves and the black dots correspond to the measured voltage and current of the inverter operating at MPP. It is clearly visible that the inverter was capable of tracking the MPP of the 0, 5, 10 and 15% system shading values. Unfortunately, with 20% system shading the inverter was incapable of tracking the MPP. This is due to the inverter's startup algorithm, which after two minutes begins drawing power by gradually dropping the PV module voltage. Afterwards, the operating voltage continues to drop until the inverter finds V_{mpp}, the maximum power point voltage, and similarly, the operating current gradually rises to I_{mpp}, the maximum power point current, which allows the output power to be maximized at P_{mpp}.

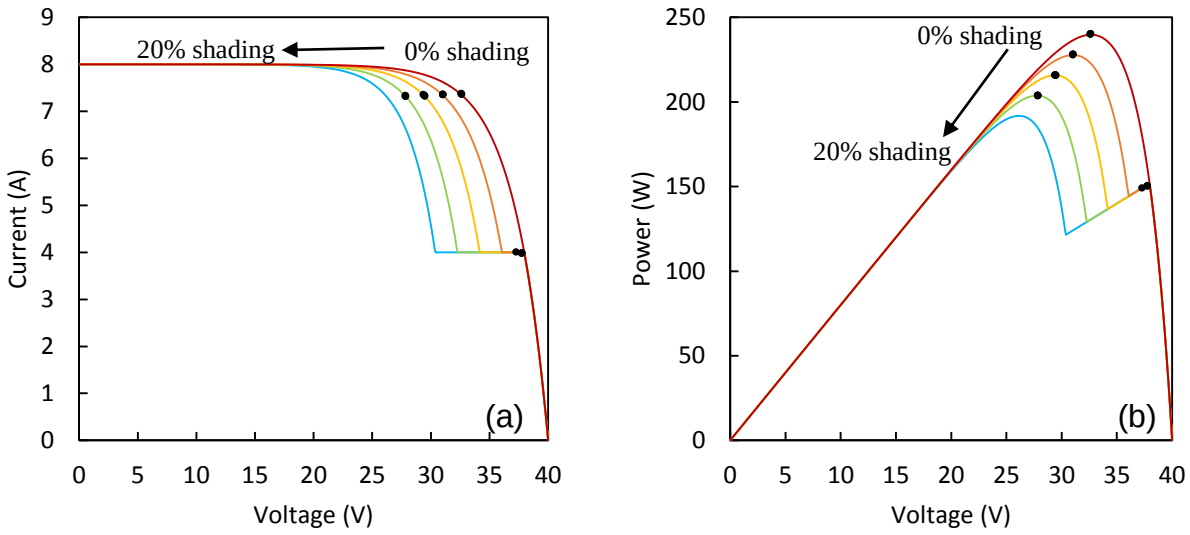

Figure 5.11: Inverter MPP (black dots) over simulated I-V (a) and P-V (b) curves (color lines) at different system shading conditions (0%-20%).

The startup sequence show a few surprises, especially observed at the third second mark in any of the following figures. First of all, all plots are portions of the 3-5 minute sequence

captured with the Keysight MSO-X 3104A oscilloscope. All voltages have been probed using the Keysight N2890 500MHz (10MΩ/11pF), and all current measurements were taken with an LEM LA-25P current transducer running at ±15V connected to a 100Ω resistor at the output. The resulting voltage output of the current transducer was measured using the identical probe as used for voltage measurements. In order to use the full capabilities of the oscilloscope, channels 1 and 3 were used instead of channel 1 and 2, which halve the sampling speed when both are on at the same time.

As shown in Figure 5.12, at the third second mark, the inverter polls the PV emulator and draws about 1A of current for about 0.25 s and reverts to V_{oc} for 0.75 seconds. Afterwards, the inverter pulses the output for reasons unknown and begins drawing current at the 5 seconds mark. The inverter lowers the operating voltage and by the 5.5 seconds mark, raises the voltage for a final drop to reach the MPP.

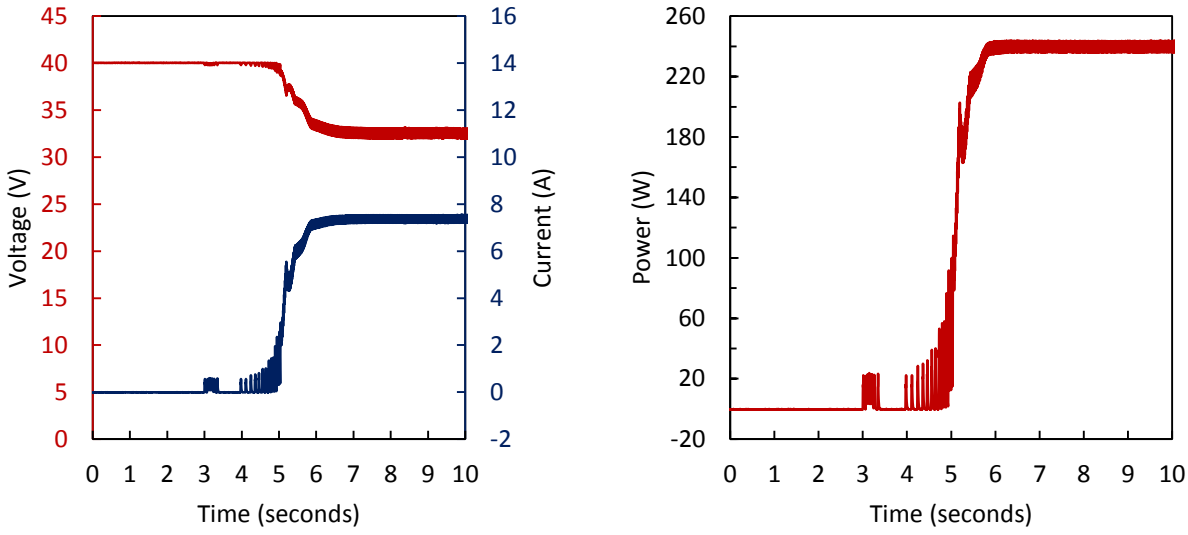

Figure 5.12: Inverter startup sequence for 0% system shading.

A 0% system shading has a broad maximum power point peak and the broadness is reflected by the steady state oscillations of the inverter (thicker lines of voltage, current, and power, beginning at the 6 second mark). There is negligible difference between 0% and 5% operation as shown in Figure 5.13.

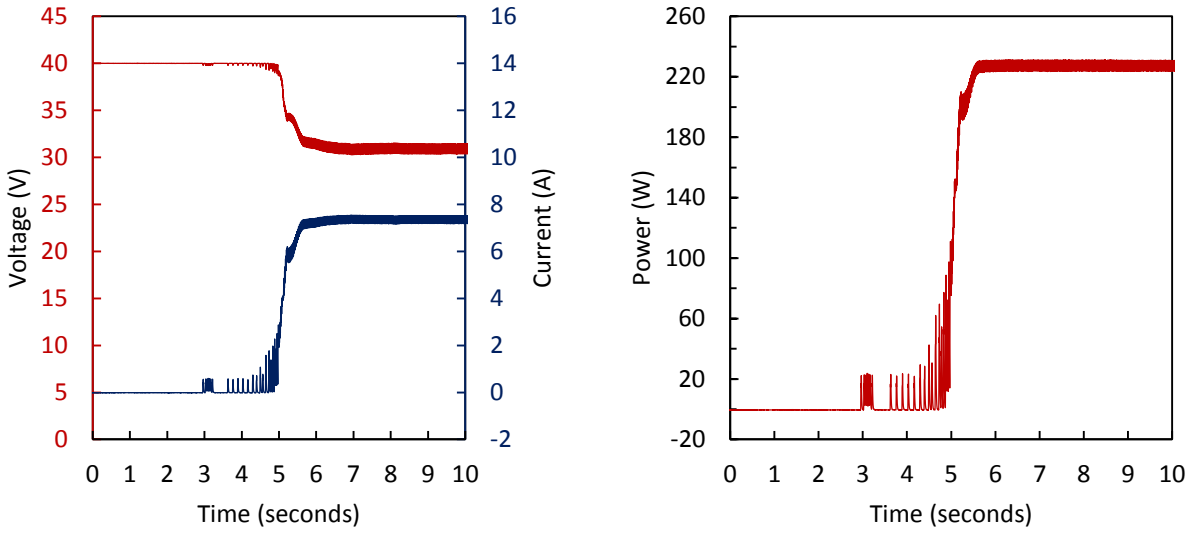

Figure 5.13: Inverter startup sequence for 5% system shading.

With system shading increased to 10%, the sharper peak of the MPP leads to a smoother and narrower oscillation around the MPP as indicated by the narrower voltage, current and power traces shown in Figure 5.14. It is also possible to discern two different slopes of the voltage derivative indicating a slower movement of the MPP algorithm.

For the 15% system shading condition, the power drop of the local maxima becomes more pronounced as shown in Figure 5.15 at the 5.5 seconds mark; however, the inverter MPP algorithm has no trouble finding the global maxima of the power curve as indicated by the significant power rise beyond the 6 seconds mark.

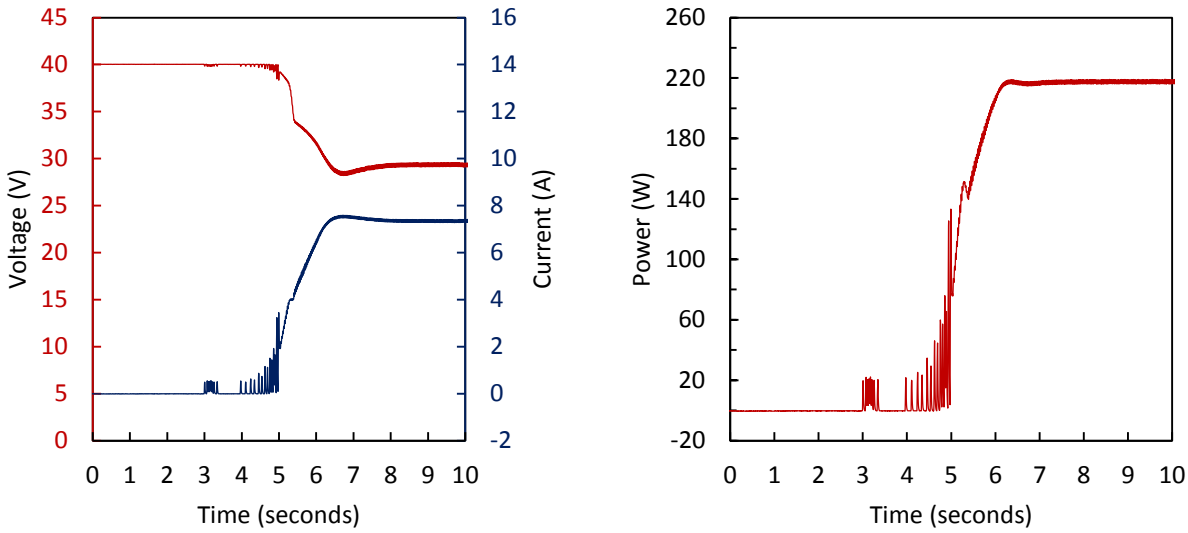

Figure 5.14: Inverter startup sequence for 10% system shading.

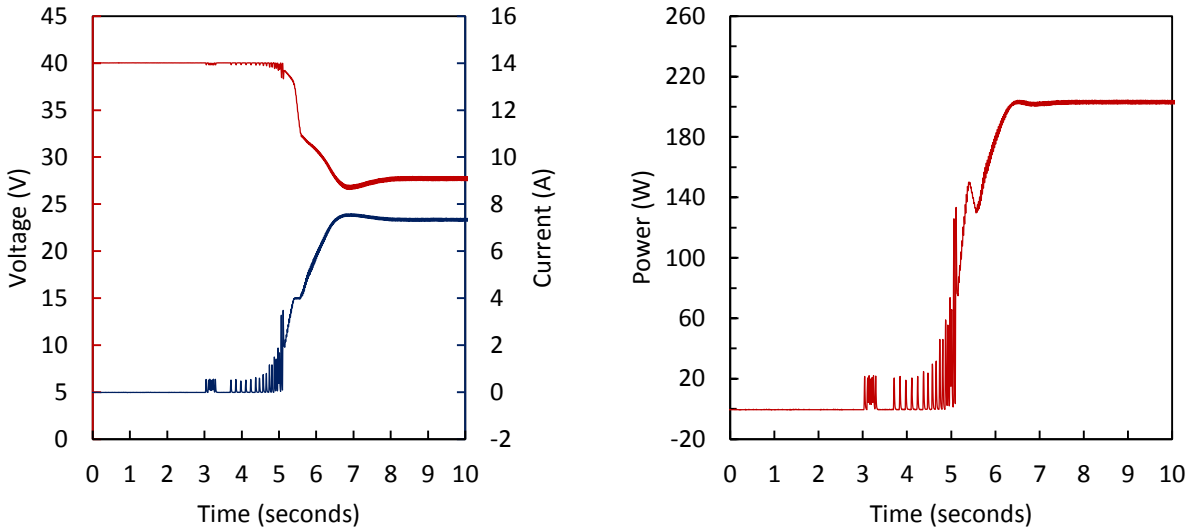

Figure 5.15: Inverter startup sequence for 15% system shading.

For 20% system shading the inverter tracked the MPP from V_{oc} down to 31.15V (up to 148.5W) and simply returned back to the local maxima and failed to find the global maxima. This could be due to the higher than the allowed power drop between the 5th and 6th seconds. The

local peak of current observable at the five second mark of Figure 5.16 requires investigation of the PV emulator operation in order to determine if there is an undesired overshoot.

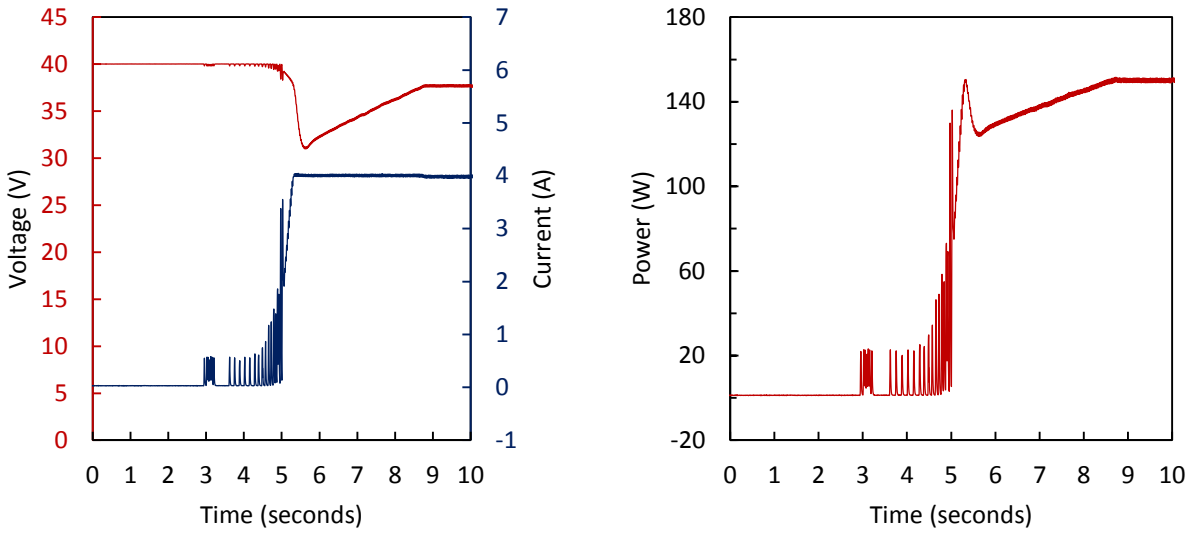

Figure 5.16: Measured inverter startup sequence for 20% system shading.

The investigation of rather a current overshoot occurred through observing Figure 5.17 proves that a current overshoot does not exist and the PV emulator never deviated from the PV model. The black dots indicate measured operation points over a red simulated line.

With the static operation using an inverter satisfied, the PV emulator static current errors were tested with the constant voltage electronic load both for PV module emulator and constant current operation.

One can observe in Figure 5.18 the slight variation of the current output (black dots) compared to the PV module model (red line). As previously discussed in the algorithm section, the ADC trigger position along the switching cycle depends on the instantaneous duty cycle. Originally set to trigger at (duty + 1)/2 and duty/2 duty cycle points for under 50% and over 50%

duty cycle, the errors were further minimized by altering the trigger location. A lot more work can go into optimizing the trigger points and thus far, the solution outlined in the algorithm section is used.

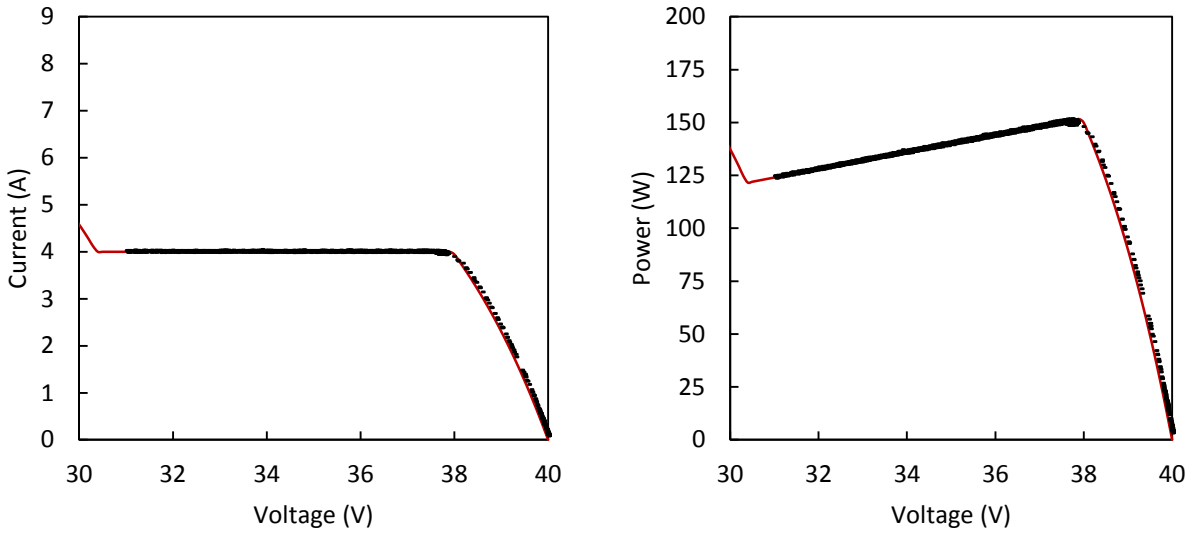

Figure 5.17: Detailed view of the inverter operation at 20% shading.

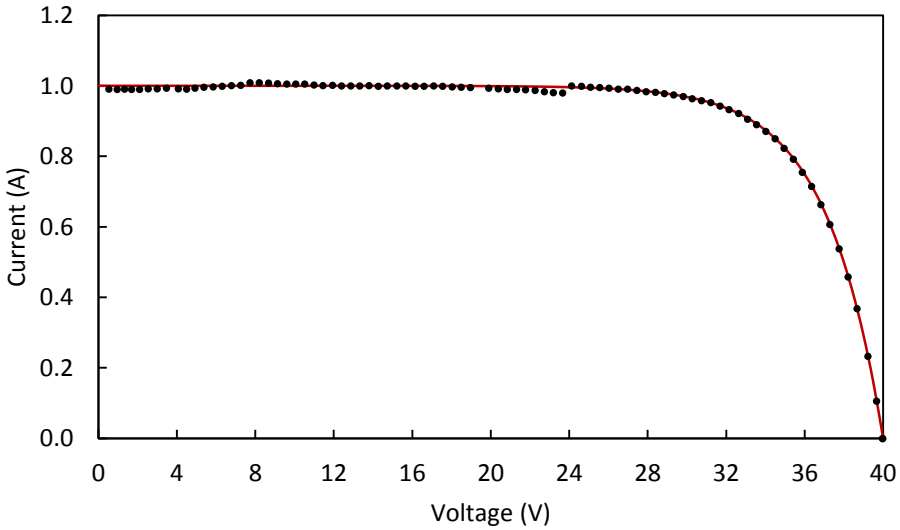

Figure 5.18: PV module emulator tested with constant voltage electronic load.

The dots abruptly transition from below the red line to above the red line at 24V, corresponding to a 50% duty cycle when operating at an input voltage of 48V. It is important to note that measurements of current and voltage are ideally made further away from the switching point as possible to pick up the least amount of switching noise. With the duty cycle near zero, it is best to have the ADC triggered above 50% so that the turn-off of Q1 and the associated noise does not affect the measurements. Conversely for duty cycles above 50%, it is more appropriate to trigger the ADC before the 50% mark.

5.4.2. Current Output Error

For PV module emulator operation, measurements generally conform to the model for output voltages over 24V; however, the points at 8V and 23V appear to produce the highest errors as shown in Figure 5.19. For the purposes of this work a current error margin of 1% (±10mA for 1A) was chosen. When looking at the current error plot in Figure 5.19, the points of the most concern are between 22 and 24V.

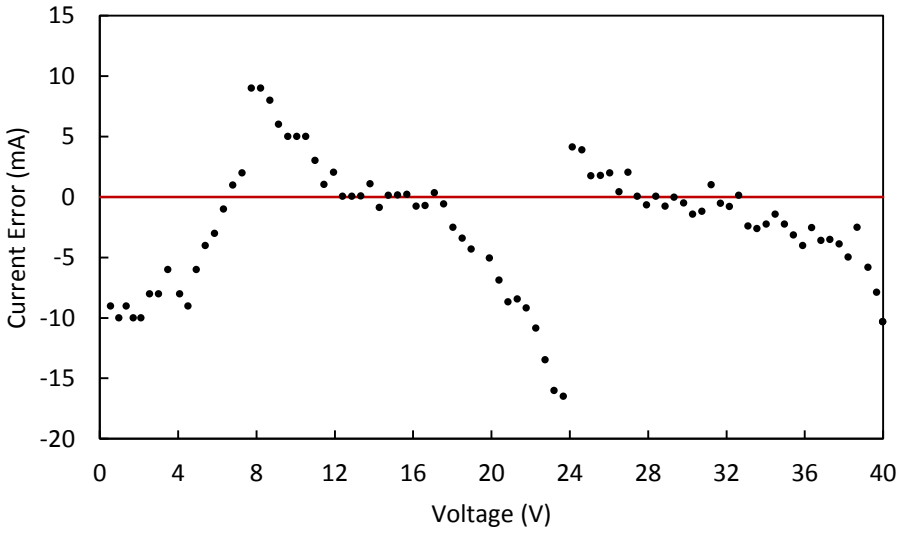

Figure 5.19: Current error vs. output voltage for PV emulator operation for V_{oc}=40V and I_{sc}=1A.

Figure 5.20 illustrates the current errors for 1A, 2A and 3A constant current mode operation when connected to a constant voltage electronic load. Similarly to the PV module emulator operation, the 8V and 23V points appear to have the worst performance, along with an abrupt error shift at the 24V point. One noticeable difference with the 3A operation is the higher sustained error above 24V operation. The effects of the increased error are negligible since on a percentage basis they have much less of an effect when compared to lower output currents.

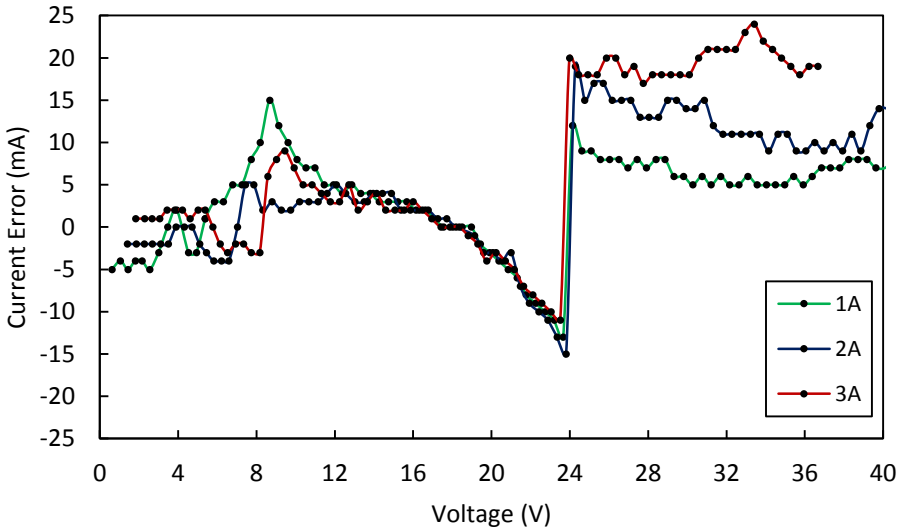

Figure 5.20: Current error vs. output voltage for constant current mode operation for 1A, 2A, and 3A.

As shown in Figure 5.21, there is a visible efficiency increase with higher output voltages. This can be attributed to the constant switching losses with increased power.

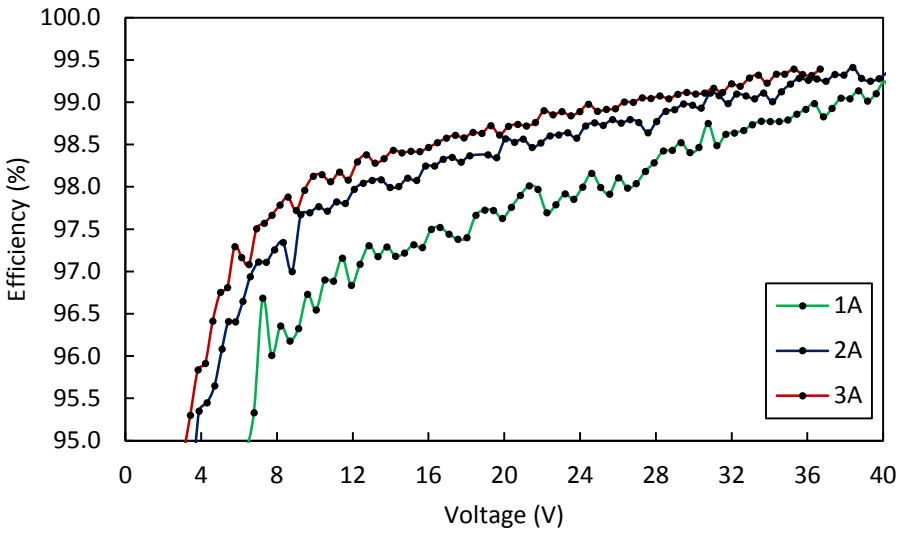

Figure 5.21: Efficiency vs. output voltage of the emulator circuit when operating at constant current mode.

5.4.3. Dynamic Performance

With satisfactory static condition test results, tests for changing conditions were conducted. For the purposes of this study, three changing conditions were analyzed in isolation: irradiance variation, temperature variation, and shading variation. All tests were performed with V_{oc} = 40V, I_{sc} = 8A, and Io = 10µA to limit the PV module power to the inverter rating of 240W.

5.4.3.1. Irradiance Variation

Tests for irradiance variation were performed beginning with 1000W/m^2 and dwelling at 900, 800, 700, 600, 500, 400, 300, 200, and 100 W/m^2 points for 10 seconds with a ramp rate between steps of 5W/m^2 with each $I_{pv}[m]$ calculation taking 261 ms, as shown in Figure 5.22.

The nearly linear relationship between irradiance and I_{mpp} is observable in the time sequence shown in Figure 5.22. On the other hand, changes in V_{mpp} are more subtle. At 250 W/m^2 (just below 2A output current), the inverter hits the low end of its MPP tracking point of 27V and quickly oscillates around the MPP to confirm proper MPP tracking. The same situation

occurs for 150W/m^2 irradiance as well, at which the MPP tracking algorithm begins to make broader oscillations

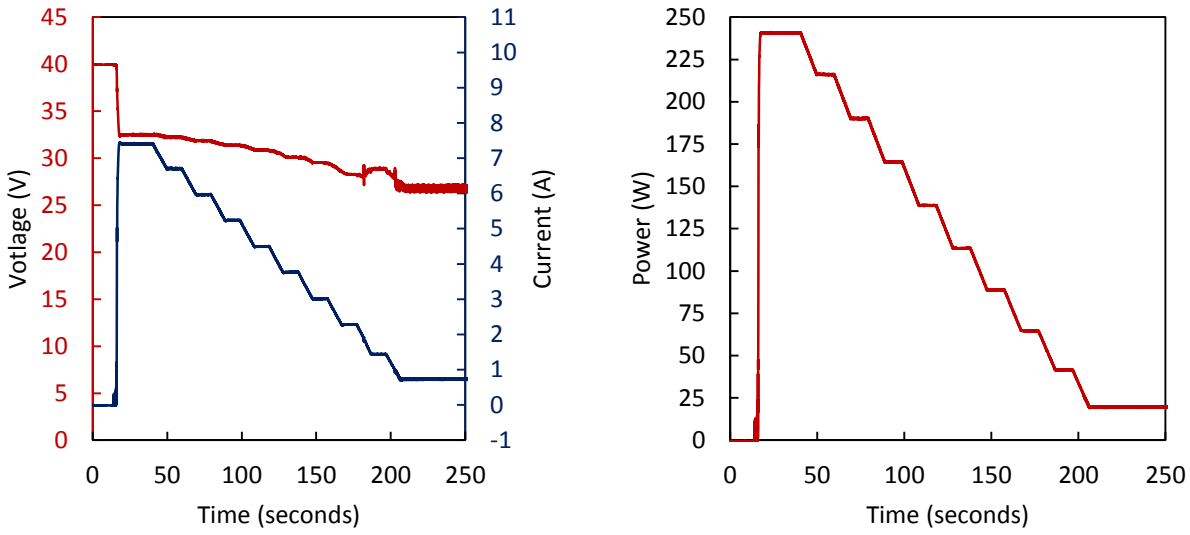

Figure 5.22: Voltage/current vs. time and power vs. time for irradiance variation tests.

In Figure 5.23, it is easier to observe the MPP tracking algorithm which starts from 40V at 1000W/m^2 and finds the MPP of the 1000W/m^2 curve, and with decreasing irradiance levels tracks the MPP rather successfully up until the circuit operates at 250W/m^2 irradiance and 27V MPP voltage, which forces the MPP algorithm to look for a new MPP. The rise in voltage is clearly visible and small errors with current and voltage quantization (3 mA/bit and 52 mV/bit, respectively) become more apparent with the MPP points being slightly different than the ideal MPP point.

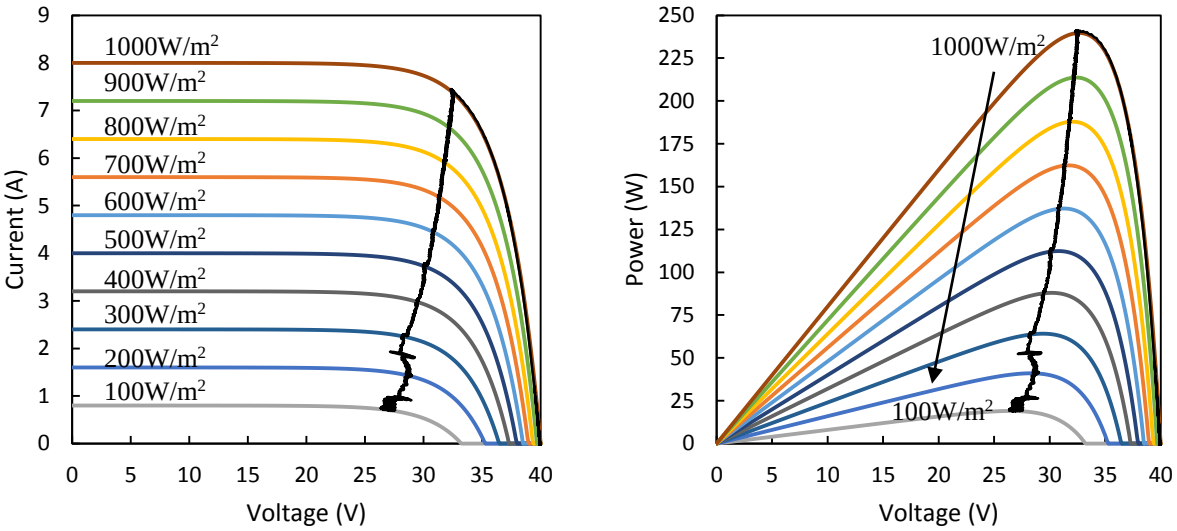

Figure 5.23: I-V and P-V curves as a function of irradiance levels (1000W/m^2 to 100W/m^2) along with MPP tracking.

5.4.3.2. Temperature Variation

Tests for temperature variation were performed beginning with 25°C and dwelling at 35, 45, 55, 65, 75, 85, 95, 105, and 115°C for 10 seconds with a ramp rate between steps of 0.5°C are shown in Figure 5.24. The temperature variations have an increasingly greater effect on I_{mpp} and an almost linear effect on V_{mpp}. Unlike the irradiance variation test, the temperature variation test does cause the inverter to trigger a MPP tracking algorithm oscillation around 27V, and the inverter performs better.

In Figure 5.25, increasing the temperature pushes the I-V curve to the left and reduces the output power of the PV module emulator. In this test, the inverter seems to have overshot the MPP point for the 25°C temperature setting when rising from V_{oc}. The inverter generally tracks the MPP well with a peculiar bump between 75°C and 85°C.

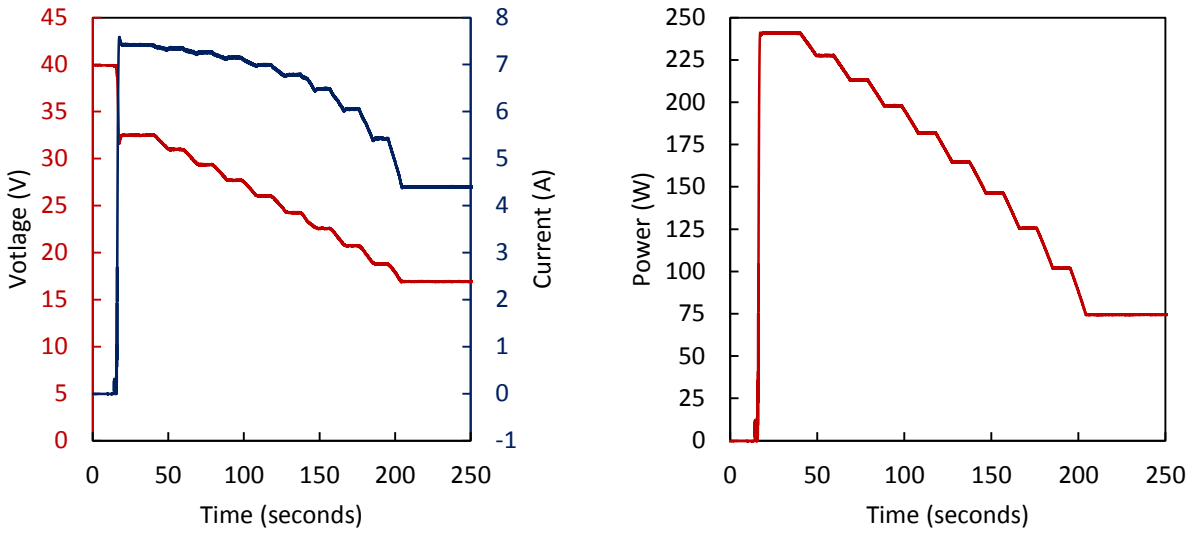

Figure 5.24: Voltage/current vs. time and power vs. time for temperature variation test.

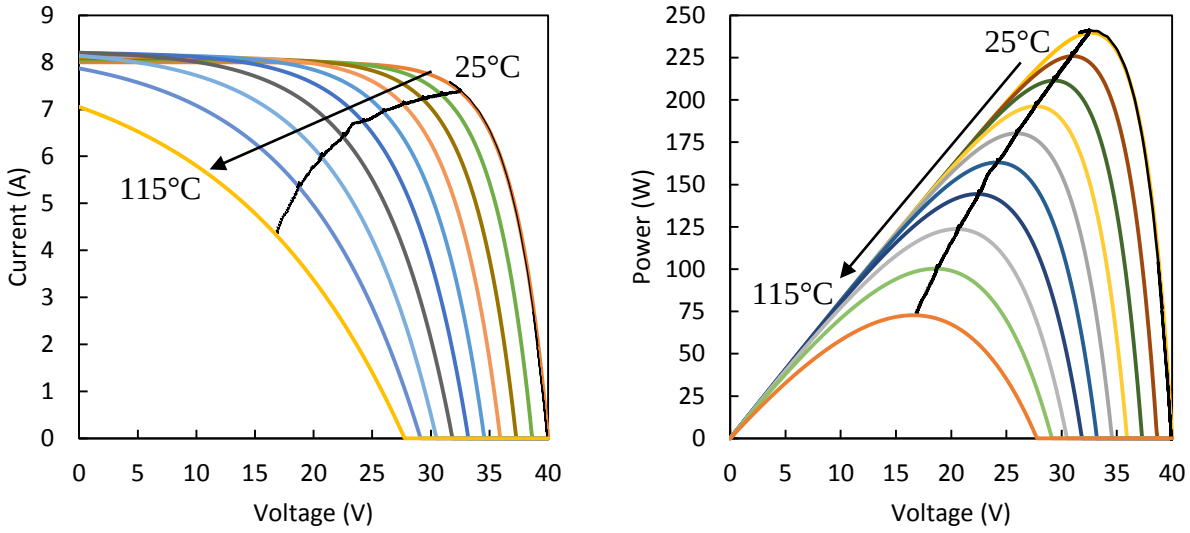

Figure 5.25: I-V and P-V curves as a function of temperature levels (25°C to 115°C) along with MPP tracking.

5.4.3.2. System Shading Variation

System shading variation tests were performed with a fixed shading strength of 0.5 and by altering the system shading from 0% to 20% and back to 0% with 1% increments and 10

second dwell *ad infinitum* as shown in Figure 5.26.

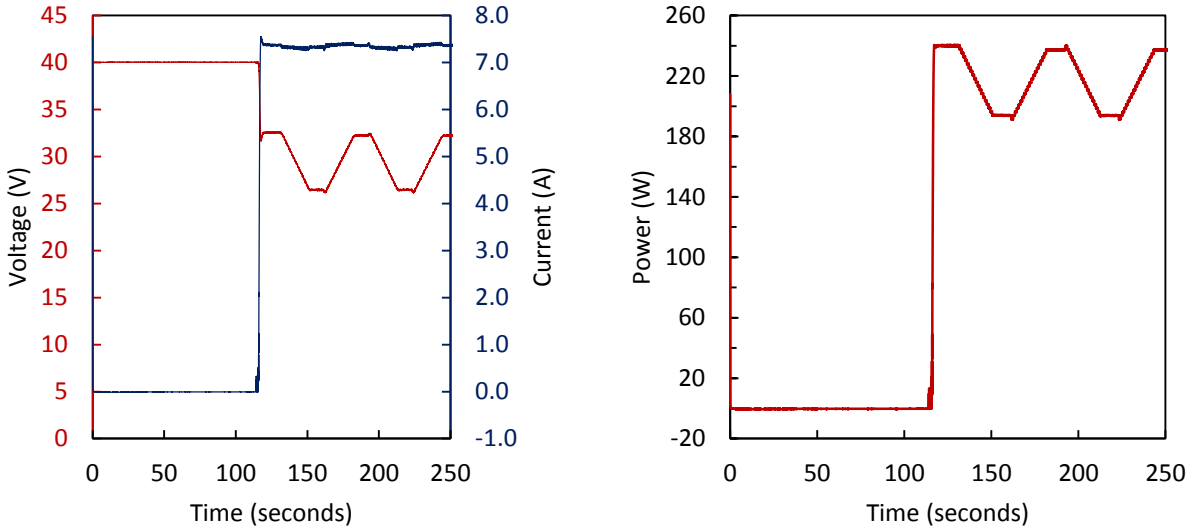

Figure 5.26: Voltage/current vs. time and power vs. time for the shading variation test.

Unlike in the static system shading tests, the inverter has no problem tracking the MPP at all system shading levels as the MPP tracker isn't required to track the MPP beginning from V_{oc} for the shaded conditions, but rather shifts to lower voltage points with the increase of system shading.

Figure 5.27 shows the MPP tracking algorithm beginning at V_{oc} and climbing the power curve up to the MPP with a slight overshoot. Unlike the tests of changing irradiance and changing temperature conditions, for changing system conditions, it is actually possible to visually see the different shading points due to the very obvious steps taken by the inverter. A detailed view of these points are shown in Figure 5.28.

The steps show in Figure 5.28 include both the MPP points for increasing system shading and decreasing system shading conditions with the black dots representing the recorded

measurements and the red line representing the simulated MPP values.

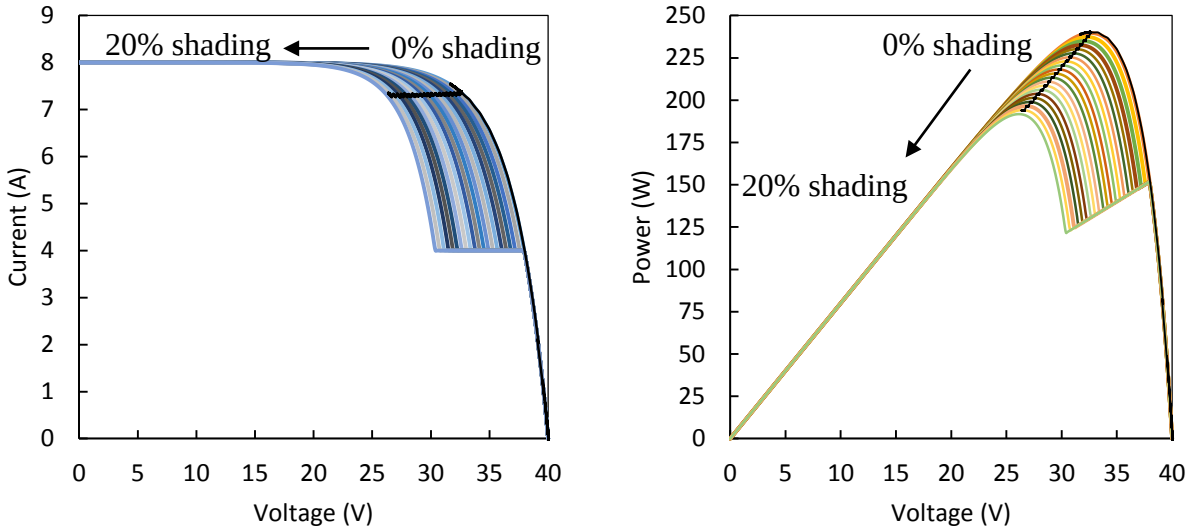

Figure 5.27: I-V and P-V curves as a function of system shading levels (fixed shading strength of 0.5 and system shading from 0% to 20%) along with MPP tracking.

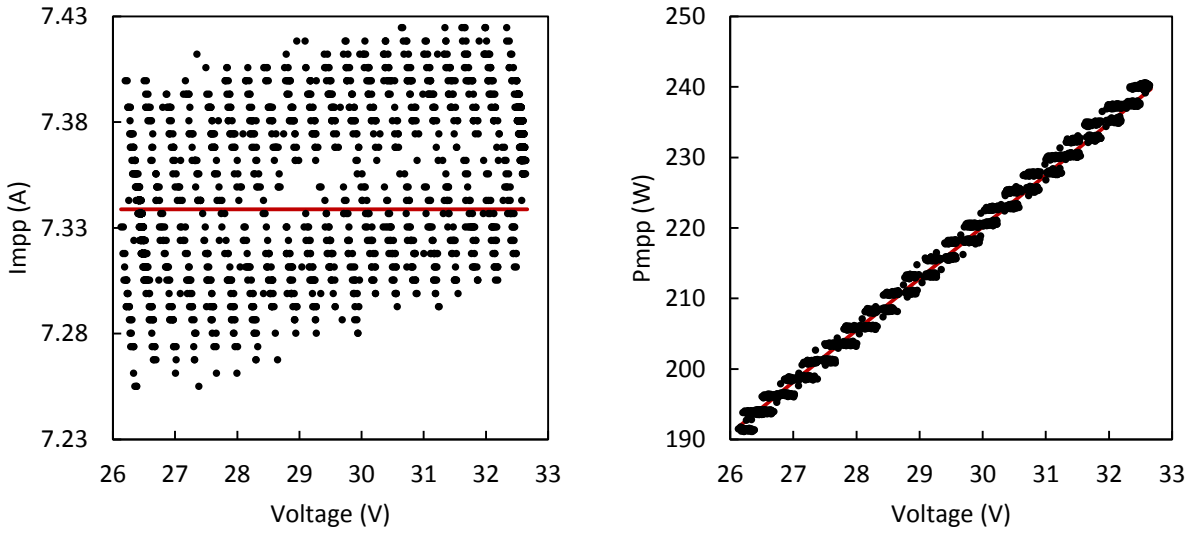

Figure 5.28: I-V and P-V curves with the detailed view of the MPP tracking algorithm for changing system shading.

The black dots above the red line are caused by the MPP tracking when system shading is reduced and this causes an initial output current overshoot and settles with a small positive current error. For increasing system shading values, the output current undershoots and carries a negative error value. This is due to the relatively flat peak of the MPP curve due to the quantized nature of the ADC values (3.05mA/bit).

5.5 Conclusions

This chapter sets out to meet the design challenge of building a high efficiency PV emulator using novel GaN devices offering better performance when compared to traditional silicon MOSFETs. The control algorithm offers a cycle-by-cycle digital control up to over 285 kHz and efficiency values well over 95% for typical MPP ranges, allowing long term testing of dynamic loads such as micro-inverters with very low losses contributing to an immeasurable temperature rise. The PV module emulator fits in a compact high power density package with over 140W per cubic inch power density. Static and dynamic tests confirm the accuracy over the inverter for changing irradiance, temperature and shading conditions. Due to the power limitations of the inverter under test, it was not possible to fully utilize the 400W output capability of the PV module emulator (which is limited by the 350W DC input voltage supply).

For future work, the power density can be improved by using a thinner inductor and a 4-layer PCB can be implemented for reducing switch node ringing. A comparative analysis of the effects of the loop speed (SysTick timer frequency) can be made to determine the effects of the loop speed on MPP tracking accuracy of the inverter. For proper characterization of the full curve at static conditions, a high power electronic load rated above 400W is necessary and can be built in-house if the needs were to arise.

CHAPTER 6

CONCLUSIONS

6.1. Conclusions

PV systems are in high demand requiring significant improvements in modeling, simulation, characterization, measurement, and emulation tools. This dissertation focused on improving the modeling, measurements and emulation of PV systems. In Chapter 1, the need for good modeling, measurement and emulation systems were highlighted with examples from industrial and academic literature.

Chapter 2 explored the different PV models used in literature with a goal of selecting the best model that fitted the needs of this work. The ideal single diode model significantly reduced computational overhead while not sacrificing too much accuracy in modeling the latest generation modules made with improved manufacturing processes. Another benefit of the ideal single diode model was that it only relied on datasheet values given by PV module manufacturers, negating the need for painstaking measurements or having to use arbitrary parameters for PV module internal losses. The inclusion of irradiance, temperature, and partial shading effects were important in modeling PV modules under different conditions. These models were utilized in Chapter 3 to properly make I-V curve measurements of PV modules and translate them to standard testing conditions (STC) and to create proper outputs for static and changing conditions for the PV module emulators shown in Chapters 4 and 5.

Chapter 3 focused on the development and optimization of I-V curve tracers based on a capacitive load. At first, different topologies were briefly considered and the basis of selecting a capacitive load were given. Afterwards, different voltage and current measurement topologies

were investigated. Considered in this chapter were two distinct generations of curve tracers that rely on completely different switching topologies. The first generation device utilized mechanical DC relays to accomplish the switching action, resulting in a volume of 287.6 cm^3. The first generation device was also improved substantially with an intermediary design named generation 1.5. The intermediary design with a volume of 108.3 cm^3 was tested under different shading conditions to create an algorithm that could accurately measure PV systems under varied conditions. The second generation device was built upon a completely new switching topology utilizing swappable MOSFETs for different application requirements. The smaller footprint of the electronic switches when compared to the mechanical switches allowed for significant reductions in volume with a final volume of 64.7 cm^3 obtained. The second generation device was also capable of measuring the incident irradiance and the PV module temperature, often higher than ambient due to the heating effect of the sun. Coupling I-V measurements with irradiance and temperature values allowed the conversion of the measured values to standard testing conditions (STC). With standardized values, different I-V measurements became comparable and the effects of irradiance and temperature were decoupled from the measured values. This allowed the modules to be characterized under known conditions and can be translated for other conditions, i.e. if it is cloudy and the short-circuit current is lower than expected, the converted values can properly indicate expected short-circuit current at STC.

Chapter 4 discussed the development of a PV module emulator based on traditional silicon MOSFETS. The first generation PV module emulator was built as a proof-of-concept to test the feasibility of using buck converters for emulating the outputs of PV modules. For this reason, the circuit used a window comparator driven control system and the circuit was not optimized for high efficiency, high power density, or dynamic loads. The purpose of the second

generation device was to increase the switching frequency, efficiency, density, and reduce the current output errors at static conditions. The second generation device increased the switching frequency of the PV emulator to 500 kHz while achieving a peak power efficiency of 97.17% and a power converter density of 20.82W/cm^3. The slow analog to digital converter (ADC) sampling method used to reduce steady state errors result in a comparatively slow loop frequency of 220 Hz. The low loop frequency did not allow testing dynamic loads connected to the PV module emulator. To overcome the dynamic challenges, the second generation device was enhanced in generation 2.5 to increase the loop frequency to over 8.62 kHz and allow testing the emulator using dynamic loads. This feature was accomplished through the use of a look-up table as opposed to equation solving as used previously, but also through the use of the internal ADC instead of the external one used in generation 2 to reduce output errors. The use of the internal ADC compromised the output current error for a large increase in loop frequency. The circuit was demonstrated to operate satisfactorily connected to an inverter.

In Chapter 5, GaN switches were investigated for their superior figure of merit when compared to traditional silicon devices. The use of GaN MOSFETs resulted in a better figure of merit when compared to similar voltage class traditional silicon devices, allowing the reduction of both conduction and switching losses at similar operational conditions. A comparatively lower frequency of 100 kHz was chosen to limit the switching losses of the emulator to achieve 99.4% efficiency with just 1.94W loss operating at 344W output power. This would not be practical with higher switching frequency operation as shown by the output current vs. efficiency graph at different switching frequencies. The power density of the GaN emulator was 8.8W/cm^3 when outputting 344W, while the circuit was capable of outputting larger amounts of power it was limited by the power rating of the DC power supplies in the laboratory. The GaN emulator also

used an enhanced PV module model to include variable irradiance, temperature, and partial shading conditions. The dynamic capabilities of the GaN emulator were vastly improved compared to previous efforts with a loop frequency of 100 kHz, limited to the switching frequency. This allowed for cycle by cycle control of the output current to improve the dynamic behavior of the GaN emulator. The emulator was tested under different emulated irradiance, temperature and partial shading conditions to test the capabilities of the inverter and emulator combination in converging the output at the MPP. The results clearly show that the dynamic capability of the GaN emulator allows the tracking of MPP for fixed and changing conditions.

6.2. Research Contributions

In this section a list of research contributions is given and identified specific to each chapter. Chapter 1 is an introductory chapter and sets the research expectations by use of a literature review process. The academic contributions of this dissertation can be summarized below. In Chapter 2:

- Accurately models PV modules using an ideal diode equation for different temperature, irradiance, and partial shading conditions.
- Use of an effective method of arbitrary condition to STC conversion and vice versa.

In Chapter 3:

- Significant volume reductions of the PV emulators were made starting from 287.6 cm^3 in generation 1, to 108.3 cm^3 in generation 1.5, and a final value of 64.7 cm^3 in generation 2.
- Significant cost reductions were made with generation 1.5 costing $183.57 to total cost of $73.33 in generation 2.

- Irradiance and temperature monitoring circuits were built into a single board in generation 2 for single unit operation.
- Design of a compact and low-cost irradiance monitor board with high linearity and good accuracy.
- Measurement algorithm that works with a single module and up to 3 PV strings at different temperature, irradiance, and partial shading conditions.

In Chapter 4:

- Significant power loss reduction and efficiency improvements by selecting circuit components using power loss equations.
- A power density of over 20 W/cm^3 with use of a traditional non-synchronous buck converter design.
- High frequency 500 kHz operation while delivering acceptable switching losses.
- Complex pulse width modulation generation circuit for 12-bit precision and use of external ADC to improve steady-state output current errors.

In Chapter 5:

- Investigated GaNFETs for use with PV module emulators
- 100 kHz cycle-by-cycle control limited to switching frequency delivering significant improvements in dynamic performance
- Very little power losses contributing to over 99% maximum converter efficiency.
- High resolution 12-bit look-up table without the use of linear interpolation for improved calculation speed and output resolution.
- Significant compactness and resilience allowing indefinite PV emulation times.

6.3. Future Work

There are several avenues for future work to build upon the research presented in this dissertation. In Chapter 2, the model can be enhanced to include series and shunt resistances by using mathematical approximations to improve modeling time. This will allow modeling and simulation of older generation PV modules with increased parasitic resistance effects.

In Chapter 3, the circuit boards pertaining to different functions can be combined and properly encased in an electronics enclosure for safe handling. Also, different capacitors can be connected in parallel depending on the load to easily switch between module-level and array-level measurements that require different voltage and capacitance ratings. Furthermore, the measured data points can be transferred over Bluetooth low energy (LE) to a dedicated application written for mobile phones. MOSFET switch on time will have to be improved for larger systems to prevent the MOSFETs from dissipating switch-on energy. Finally, all devices can be designed to be surface mounted to further improve circuit volume with a constraint coming from the load capacitors.

In Chapter 4, the non-synchronous converter topology can be abandoned in favor of a synchronous buck converter topology to increase efficiency and reduce power losses. Additionally, an external ADC with a faster conversion speed (such as a pipelined ADC) can be used to reduce the steady-state errors while increasing the loop frequency.

In Chapter 5, higher voltage rating GaN devices can be used from other vendors to increase the maximum open-circuit voltage output of the emulated PV system. This will allow the emulator to emulate larger PV systems beyond a single high power module. Additionally, the GaNFETs can be run in higher switching frequency to increase the power density of the emulator, which is limited by the inductor size.

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1. **Yunus Erkaya**, Paul Moses, Sylvain Marsillac, "On-Site Characterization of PV Modules Using a Portable, MOSFET-Based Capacitive Load," *43rd IEEE Photovoltaic Specialists Conference*, 2016
2. **Yunus Erkaya**, Sylvain Marsillac, "A PV Module Emulator Based on GaN Devices with Over 99% Peak Efficiency," *43rd IEEE Photovoltaic Specialists Conference*, 2016
3. **Yunus Erkaya**, Paul Moses, Isaac Flory, Sylvain Marsillac, "Steady-State Performance Optimization of a 500 kHz Photovoltaic Module Emulator,"*43rd IEEE Photovoltaic Specialists Conference*, 2016
4. **Yunus Erkaya**, Paul Moses, Isaac Flory, Sylvain Marsillac, "Development of a Solar Photovoltaic Module Emulator," *42nd IEEE Photovoltaic Specialists Conference*, 2015
5. Chad Herndon, **Yunus Erkaya**, Chunsheng Xin, Isaac Flory, Shirshak Dhali, Sylvain X. Marsillac, "Smart Combiner for Fixed Commercial Photovoltaic Systems Using Power Line Communication," *40th IEEE Photovoltaic Specialists Conference*, 2014
6. **Yunus Erkaya**, Hareen Illa, Caitlin Conway, Shirshak Dhali, Sylvain Marsillac, "Development of a String Level Fault Detection System for Solar Tracking Applications," *40th IEEE Photovoltaic Specialists Conference*, 2014
7. **Yunus Erkaya**, Isaac Flory, Sylvain Marsillac, "Development of a String Level I-V Curve Tracer," *40th IEEE Photovoltaic Specialists Conference*, 2014 • nominated best poster award

Honors, Awards and Scholarships

- 2014 - 2016 National Science Foundation Scholar: Solar Engineering Academic Program S-STEM SoLEAP