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Rapid and Accurate C-V Measurements

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Abstract

We report a new technique for the rapid measurement of full capacitance-voltage (C-V) characteristic curves. The displacement current from a 100 MHz applied sine-wave, which swings from accumulation to strong inversion, is digitized directly using an oscilloscope from the metal-oxide-semiconductor (MOS) capacitor under test. A C-V curve can be constructed directly from this data but is severely distorted due to non-ideal behavior of real measurement systems. The key advance of this work is to extract the system response function using the same measurement set-up and a known MOS capacitor. The system response correction to the measured C-V curve of the unknown MOS capacitor can then be done by simple deconvolution. No de-skewing and/or leakage current correction is necessary, making it a very simple and quick measurement. Excellent agreement between the new fast C-V method and C-V measured conventionally by an LCR meter

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is achieved. The total time required for measurement and analysis is approximately 2 seconds, which is limited by our equipment.

Index Terms

MOS devices; Capacitance measurement; C-V measurement; Fast C-V measurement; Transient measurement; Semiconductor device measurements

I. Introduction

Capacitance-voltage (C-V) measurements are essential to monitor and control the electrical characteristics of metal-oxide-semiconductor (MOS) devices [1]. For semiconductor integrated circuit (IC) manufacturing as well as development, it is desirable to map the variability across the wafer using C-V measurements. However, C-V measurements using conventional LCR meters are slow, making it impractical to perform full wafer C-V mapping. Therefore, the development of rapid and accurate C-V measurements technique is highly desirable.

Typical approach to fast C-V measurements, which has been introduced in recent years [2 – 6, 11], is to apply short voltage pulses spanning from accumulation to strong inversion and capture the displacement current directly. Short pulses allow high repetition rates and fast signal averaging. Full C-V curves can be obtained in a very short time, in principle. However, the main attention of this approach has been to determine the transient changes in the devices, not to measure the C-V curve accurately. This is because, with the exception of [11], agreement with measured result from conventional LCR meters was never achieved. High-speed measurements are full of pitfalls and the measured C-V curves are badly distorted. By focusing on transient changes, the hope is that the distortion in these pulsed C-V measurements is constant and any observed transient shift is valid.

Pulsed C-V techniques are based on measuring the transient displacement current (I_{displ}) corresponding to the gate voltage ramp rate (dV_G/dt). The capacitance value can be obtained as follows:

$$I_{displ}=C\frac{dV_G}{dt} \quad (1)$$

As device size and gate oxide thickness scale down, the displacement current becomes small and the gate leakage becomes high. The solution to this problem is to increase the V_G ramp rate to increase the magnitude of the displacement current and to decrease the error due to leakage current. Using shorter pulses (more precisely, faster rise and fall times) effectively increases the V_G ramp rate. However, measurement artifacts increase with signal speed, leading to distorted C-V curves. A compromise was reached in [11] where a V_G ramp rate up to 7 MV/s was achieved while maintaining good agreement with an LCR meter result. Unfortunately, this ramp rate was not high enough to ignore the gate leakage current. Separate gate leakage measurements and a point by point leakage correction was required. In

addition, the method requires manual timing de-skew, a task that adds complexity. While it greatly increases the confidence in the measurement of device characteristic changes, it is not suitable for very fast measurement.

The acquisition of C-V characteristic curves using RF frequency is another technique that has been introduced in recent years [7–9] to increase the V_G ramp rate. While successful in measuring accurate full C-V curves, it is slow, difficult to use, and requires special test structures and calibration devices. Very fast measurements using a fast RF C-V technique has also been reported, but MOS devices with small capacitance value were not examined [10].

In this paper, we report a new approach for highly accurate C-V measurements that is fast enough for wafer mapping. We use a 100 MHz pure sine-wave as a gate input, leading to GV/s V_G ramp rates. In addition, we developed a deconvolution method to remove system response distortion, achieving simple and fast correction with high accuracy. While we demonstrated measurement and analysis time of less than 2 seconds, we discuss the potential for much faster measurements. Fig. 1 shows the key result of this work.

II. Experimental Setup

The devices measured in this work are MOS capacitors with a 20 nm-thick SiO_2 gate oxides fabricated by MOSIS. It is a standard two-terminal device with two contact pads for easy probing. The use of a standard test device makes this technique particularly versatile. The equipment requirement for this measurement method is also very simple, involving a sine-wave generator and a moderately fast oscilloscope. An important detail is that both wafer probes are coaxial semi-rigid cables in which the transmission line shielding extends very close to the probe tip to minimize the inter-probe capacitance and to provide a tight return current path (a short between the two shields near the probe tips) for the RF signal.

As shown in Fig. 2, a 100 MHz sine-wave with peak to peak voltage covering accumulation to strong inversion (−3.0 V to 3.0 V) is applied to the gate of a MOS capacitor using a 50 Ω terminated probe. At 100 MHz, this is easy to do and commercially available. Ours are homemade (picture in inset). A pick-off TEE splits part of this driving signal to the oscilloscope. The displacement current from the substrate is also captured by the same oscilloscope. The peak sweep rate for this waveform is ~1.8 GV/s. At this rate the peak displacement current becomes high enough (100 fF → 180 μA) to be measured directly with an oscilloscope with 50 Ω input impedance (9.0 mV), minimizing the gate leakage effect. Since the measured displacement current from MOS devices with changing capacitance contains much higher frequency components than gate waveform input, the oscilloscope bandwidth must be chosen to capture these higher frequencies. Empirically, we determined that one must capture the gate waveform with 25× the bandwidth of the input waveform frequency, meaning the oscilloscope must have 2.5 GHz bandwidth to correctly capture all the frequency components arising from our 100 MHz gate input waveform.

III. Measurement Procedure And Results

A. Acquisition of Signals

Several sine-wave cycles are captured at 200 GS/s to make sure that data from a complete cycle is available for processing. At 100 MHz, this happens very fast. To reduce noise, 20 averages are used. Again, at 100 MHz, it should theoretically be over in less than 1 μs. For convenience, we use the oscilloscope's averaging function which is much slower. Nevertheless, it is completed in less than 2 seconds.

The sampling rate of the oscilloscope is an important consideration. By Nyquist's theorem, a minimum of two data points is required to represent a frequency. As discussed earlier, we empirically determined that 2.5 GHz is the minimum bandwidth to capture the C-V curve driven by a 100 MHz signal, the minimum sampling rate is therefore 5 GS/s. We use 200 GS/s (maximum for our oscilloscope) for reasons which become apparent below. During the subsequent analysis, we need to accurately determine the start and end point of a cycle, for both the driving signal and the displacement current signal. The density of time points affects the accuracy of this determination because the displacement current waveform is not a simple sine-wave. This will translate into small timing errors between the driving signal and the displacement current signal. The result will be a distortion of the extracted C-V curve. For comparison, the signals sampled at 20 GS/s were also obtained. The effect of the sampling rate will be discussed later.

Before using the captured data to extract the C-V curve, we must first remove any DC offset. As this is a purely AC measurement, DC offset contributes only as error. No oscilloscope is perfect and some DC offset is inevitable. To correct the DC offset, the signals are converted to the frequency domain by fast Fourier transform (FFT) and the DC component is removed. Fig. 3 shows the comparison between captured current signal before and after DC offset correction.

B. System Response Extraction

There are many parasitic elements in a measurement system and their effect is larger at higher frequencies. However, if we make sure that the system does not change between measuring a known reference device and an unknown device under test, then all the parasitic effects can be determined using the reference device and then removed from the device under test. The parasitic effects, along with the performance of the oscilloscope together forms the system response function. From the measurement of the reference device with a known C-V curve, this system response function can be extracted.

How do we make sure that the system does not change when we change the device under test? This is quite easy with modern probe stations. As we move from device to device, only the wafer is moved. With accurate positioning, the probe will land at the same location on the pad every time so that the pad to probe parasitic will be the same. Probe to probe parasitic will not change because the probes remain fixed and all the cabling and oscilloscope setting remain the same.

To obtain the system response function, we need to compare the measured response of a known device to the "ideal" response of the same device. Since we measure displacement current, along with gate voltage, as a function of time, displacement current is what we use for the system response extraction. A reference C-V curve is measured from a MOS capacitor using a commercial LCR meter (assuming the LCR meter is properly calibrated). The measurement is carried out at an oscillation voltage of 50 mV and a high frequency of 1 MHz. This same MOS capacitor is also measured using the fast C-V method to obtain both the time varying gate voltage curve (100 MHz sine-wave) ($V_G(t)$) and the time varying displacement current curve ($D_{mea}(t)$). Using the reference C-V curve, equation (1), and the time varying gate voltage sweep rate ($R(t)$) which is obtained by differentiating numerically (Savitzky-Golay method) the measured $V_G(t)$, we generated the reference ("ideal") displacement current versus time curve ($D_{ref}(t)$). Note that the LCR meter measurement and the oscilloscope measurement do not have the same gate voltage points and use vastly different point densities. To overcome this an interpolation operation is performed on the reference C-V curve so that every point in the reference C-V curve has a matching point in the measured gate voltage. Fig. 4 shows the reference C-V curve of the reference MOS capacitor before and after interpolation.

The measured displacement current ($D_{mea}(t)$) and the reference displacement current ($D_{ref}(t)$), along with the gate voltage ($V_G(t)$) are shown in Fig. 5. As can be seen, there is a clear discrepancy between the two displacement currents due to non-ideal system response. To calculate the system response function, deconvolution was performed in the frequency domain. Using the FFT of the reference and measured displacement current waveforms, we write

$$H(\omega)=D_{mea}(\omega)/D_{ref}(\omega) \quad (2)$$

where $H(\omega)$ is the system response function, $D_{mea}(\omega)$ is the measured displacement current, and $D_{ref}(\omega)$ is the reference displacement current in the frequency domain.

C. Applying the System Response Function to an Unknown Capacitor

The extracted system response function can now be used to correct the measured displacement current of unknown MOS capacitor device under test ($D_{DUT}(t)$), after it is transformed into the frequency domain. A simple re-arrangement of equation (2) obtains:

$$D_{corr}(\omega)=D_{DUT}(\omega)/H(\omega) \quad (3)$$

where $D_{corr}(\omega)$ is the corrected displacement current of the unknown MOS capacitor and $D_{DUT}(\omega)$ is the measured displacement current of the unknown MOS capacitor, both in the frequency domain. The corrected time domain displacement current curve ($D_{corr}(t)$) is recovered by a reverse FFT of $D_{corr}(\omega)$. Using equation (1) and $R(t)$, the corrected C-V curve of the unknown MOS capacitor is calculated from $D_{corr}(t)$.

Fig. 1 (a) illustrates the poor result of fast C-V measurement when the system correction is not done, and (b) shows the successful result after the correction removes the artifacts. The system response was extracted from a reference device (not shown in Fig. 1) with capacitance value in between the two samples. As can be seen, the corrected fast C-V is in very good agreement with the LCR meter measurement on both samples.

All the post measurement data processing described above can be fully automated which has been done for this work. The speed of data processing is dependent on the computer used and the program quality. It is very fast in our case. As mentioned earlier, we are limited by the averaging function of the oscilloscope and the measurement itself takes less than 2 seconds. If raw data of many cycles is directly captured in real time by the oscilloscope (averaging done in post processing), it can all be done in a microsecond. A conventional C-V measurement by LCR meters will take minutes for a bidirectional sweep.

IV. Discussions

A. Effect of Sampling Rate

Using deconvolution to remove the system response to achieve highly accurate C-V measurements at high speed is an extremely simple and robust method. All that is needed is a single reference device of similar type that can be measured reliably using known method (commercial LCR meter in our work). This is a time domain measurement, yet timing de-skew operation is not necessary. In theory, the timing skew between the gate waveform measurement and the displacement waveform measurement is automatically corrected as long as completely consistent conditions are achieved from measurement to measurement. In practice, the discrete nature of the digital measurement can introduce small timing inconsistencies.

A key assumption is that a single cycle of the sine-wave is used in the data treatment. As mentioned earlier, the displacement current waveform is not a simple sine-wave that can be modeled accurately. Instead, it is a complex waveform that differs from device to device. Precise determination of the start and end point of a cycle requires careful consideration and is affected by the sampling rate of the measurement.

Fig. 6 shows the result of fast C-V from sample B when the sampling rate is dropped to 20 GS/s. The agreement to the LCR meter result is clearly nowhere as good as in Fig. 1. We should mention that for this case as well as the case in Fig. 1 we use the first positive point of the rising edge of the waveform as the starting point and the last negative point of the next rising edge as the end point of the cycle. Obviously, the density of the point spacing has a direct impact on the timing accuracy.

The demand for high sampling rate drives up the cost of the oscilloscope. A simple way around this problem is interpolation. For example, after using interpolation to increase the time resolution of the signals digitized at 20 GS/s by 10 folds, the resulting fast C-V curve of sample B becomes identical to the one sampled at 200 GS/s as shown in Fig. 7.

The ability to use a lower sampling rate oscilloscope allows low cost equipment to be used and, as a bonus, smaller data file sizes. The lowest sampling rate one can use, theoretically, is set by the Nyquist's theorem as mentioned before, meaning 5 GS/s for the 100 MHz gate voltage signal. However, being lower cost one must caution that lower sampling rate oscilloscopes may have larger timing jitter that can also introduce timing error that cannot be removed by interpolation.

B. Limitation

In the example we showed, the reference device and the device under test have rather similar capacitance. This is a limitation of the method. This limitation originates from two main factors. One is the linearity of the oscilloscope, the other is series resistance. Fig. 8 illustrates the problem. When the device under test is only 15% higher capacitance than the reference, the method works very well. When the device under test is 85% higher in capacitance, the agreement with the LCR meter deteriorated noticeably.

For the method to work, the system response function must remain unchanged between the measurement of the reference device and the device under test. In practice, we keep all the settings unchanged. However, a different capacitance value will result in a different amplitude of the displacement current. Even if the oscilloscope gain setting remains the same, the amplifier gain within the oscilloscope is still amplitude dependent. This is a very common problem of amplifiers and is very difficult to avoid. This subtle change in signal gain changes the system response function. The bigger the difference in signal amplitude between the reference and the unknown sample, the bigger is the gain error. In most cases, this is the biggest contribution to the limitation of the validity range of the method.

The series resistance is a well-known problem in C-V measurements, particularly when high frequency is used. As we measured the displacement current using a 50 Ω terminated oscilloscope, it adds to the total series resistance. In general, it is important to make sure the capacitance's impedance is much larger than the total series resistance. At 100 MHz, the impedance of a 100 fF capacitor is 15.9 kΩ. Assuming the total series resistance is 100 Ω (device design dependent), the effective gate voltage is 0.6% lower than the applied gate voltage.

When these errors are not large, it is interesting to note that as long as the capacitance of the device under test is close to the capacitance of the reference device, these errors are corrected automatically by the deconvolution method. However, when the difference between the device under test and the reference device increases, these errors show up.

Because we terminate the gate probe with 50 Ω resistor, there is a potential parallel resistance effect. When the impedance of the capacitor is low, the effective impedance becomes smaller than 50 Ω and can cause reflection of the gate waveform. At 100 MHz, keeping the gate probe cable less than 1 meter in length is sufficient to remove this problem.

It is entirely possible to produce a set of system response functions to cover a wide range of capacitance. For the purpose of wafer mapping, one usually measures the same test device across the wafer. Thus only one reference device is needed and one system response

function is required. Even when the wafer-level variability is large, and the accuracy degraded as the 85% change case shown in Fig. 8, the data still can closely reflect the variation.

When measuring capacitances much smaller than those demonstrated here, we can use a higher gate frequency, and perhaps an additional pre-amplifier is required. The limit in gate frequency is determined by the impedance of the capacitor which we like to keep above 500 Ω. For 1 fF, this allows up to 300 GHz. A practical limit is the scope bandwidth. Since we need the scope to have a bandwidth at least 25× higher than the gate frequency, 4 GHz becomes the practical limit. Using a broad band amplifier covering 4 to 100 GHz, we can still have very healthy signal even at a fraction of a fF. So in theory, we can measure sub-femtoFarad accurately. There is no obvious limit to how low in capacitance one can go.

The accuracy of the measurement only depends on the overall gain of the measurement system. Without calibration, the scope accuracy is about 5%. However, calibration is straight forward. Note that we did not have to calibrate our measurement system directly because we used a known reference device for deconvolution. The calibration is already built-in. The hard part of measuring smaller capacitance is the availability of references. The absence of it is the reason we did not demonstrate the method on really small capacitance.

V. Conclusion

A fast C-V measurement technique is demonstrated. It is simple in operation and requires only a sine-wave source and a moderate speed oscilloscope. The method is fast and accurate, and does not require special test structures. The main limitation is the device under test must not be too different from the reference device with which the system response is extracted. This fast method will be applicable to wafer-level mapping of capacitance variation.

Acknowledgments

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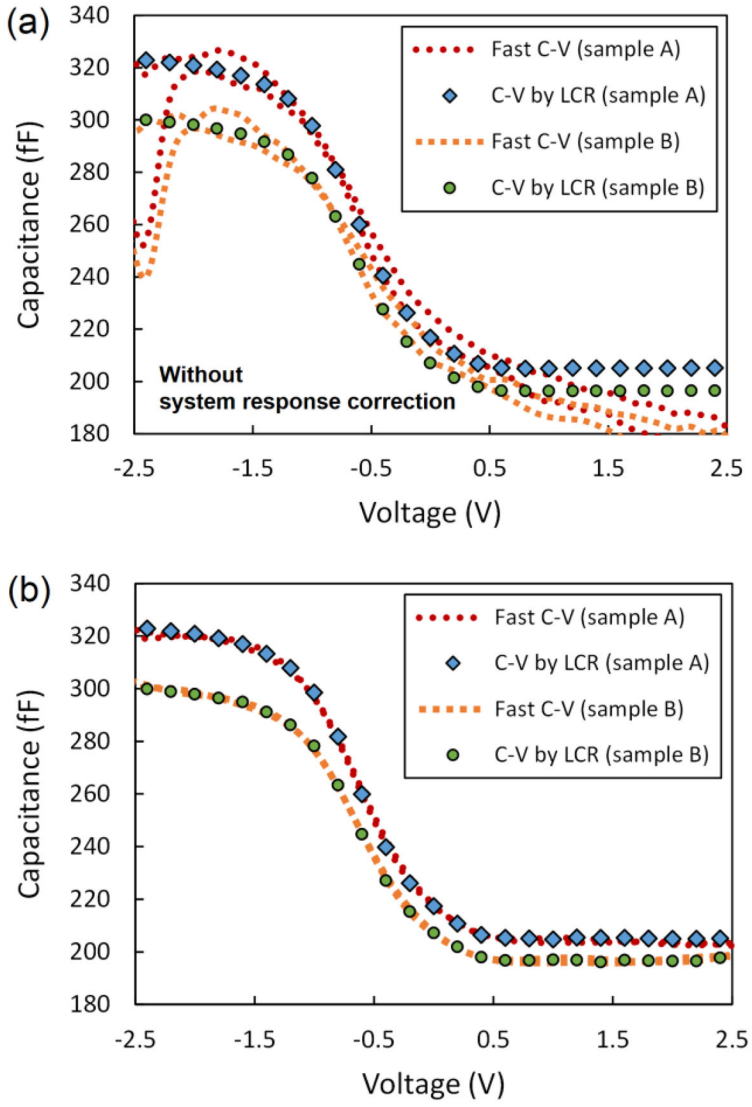

Fig. 1.

(a) Comparison between measured fast C-V (1.8 GV/s V_G sweep rate) and conventional C-V curves without system response correction. While a bi-directional sweep shows both directions have large discrepancy between the two methods of measurement, one of the directions is far worse. (b): the same bi-directional sweep showing the two measurement methods are in excellent agreement once the system response is corrected by deconvolution.

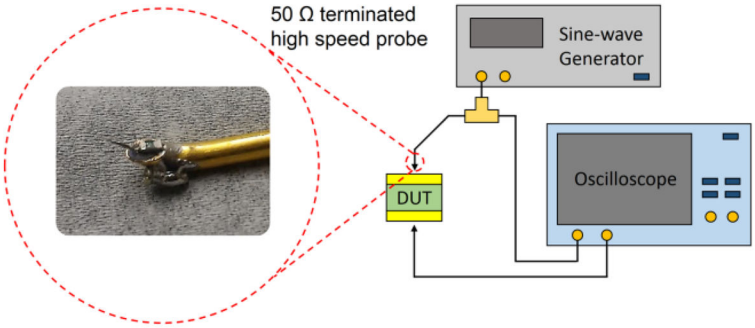

Fig. 2.
Schematic of the fast C-V measurement system.

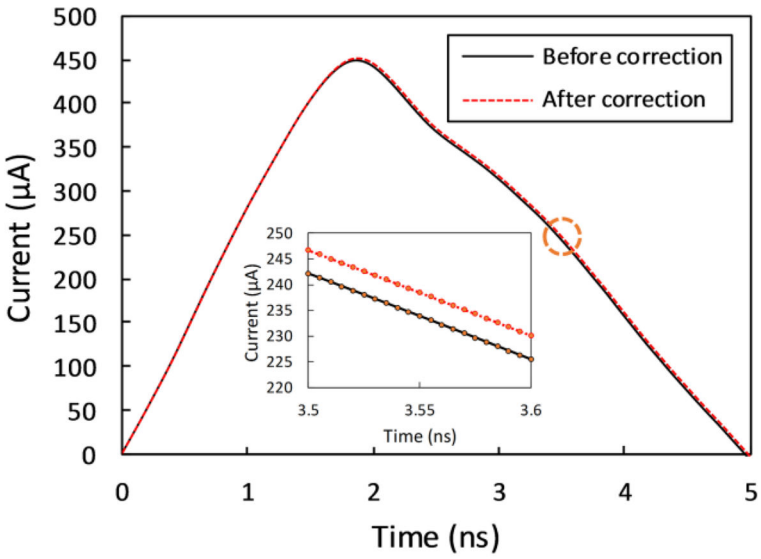

Fig. 3.

Comparison between captured current signal before and after DC offset correction (half cycle).

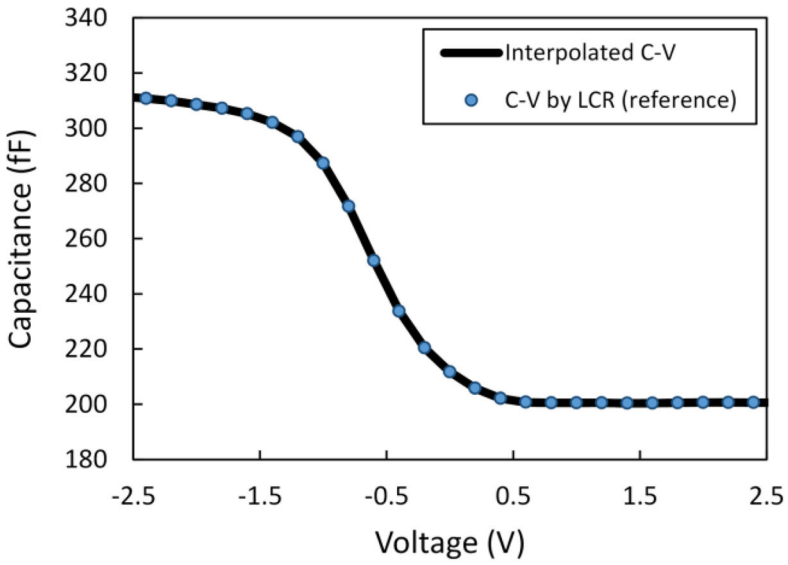

Fig. 4.
The reference C-V curve from an LCR meter before (circle) and after interpolation (solid).

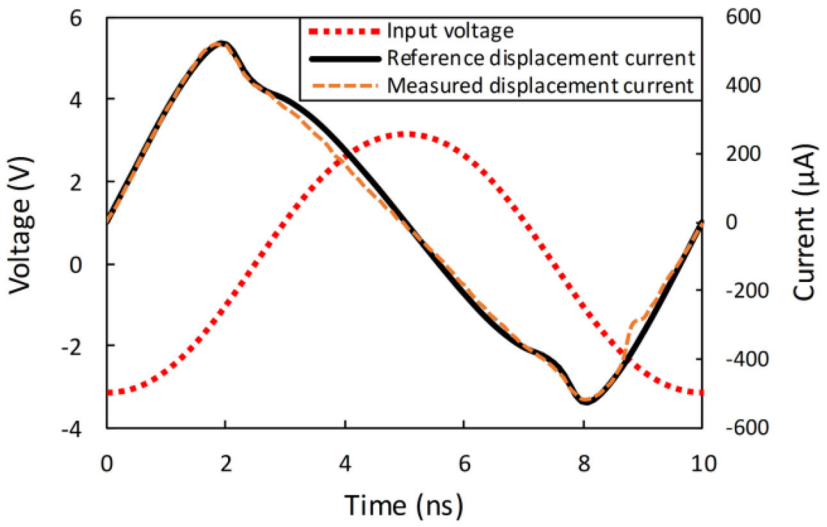

Fig. 5.

Calculated reference displacement current and measured displacement current are compared to show discrepancy due to non-ideal system response. Also shown is the gate voltage (V_G) waveform.

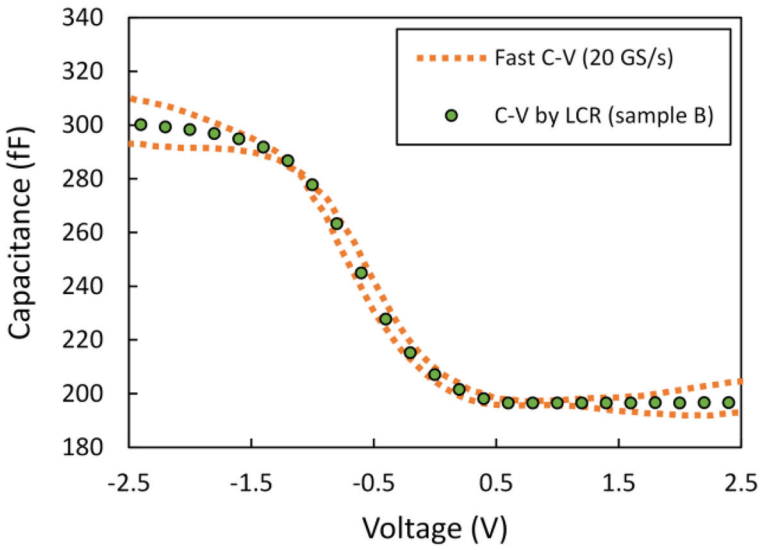

Fig. 6.

Comparison between fast C-V measured at 20 GS/s sampling rate (square dot, both direction of sweeps) and conventional C-V (circle).

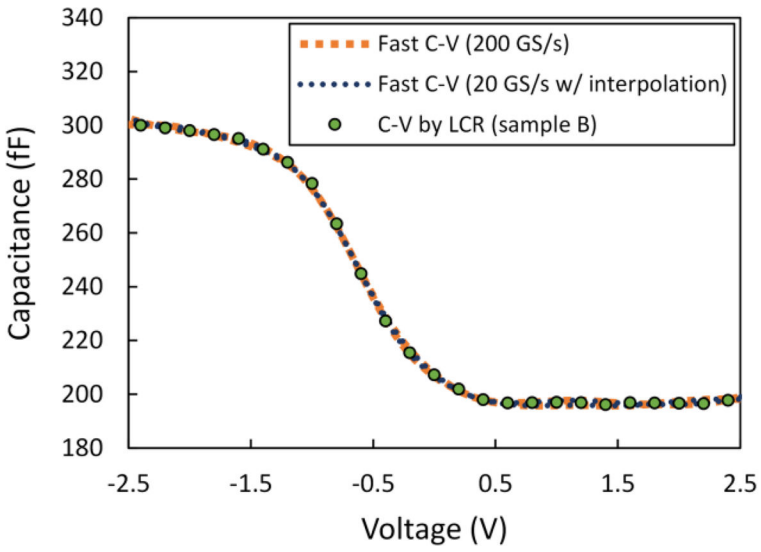

Fig. 7.

Fast C-V measured at 20 Gs/s and with 10× enhancement in timing resolution by interpolation (round dot) is in perfect agreement with the one measured at 200 GS/s (square dot). Both are in perfect agreement with the C-V curve measured using an LCR meter (circle).

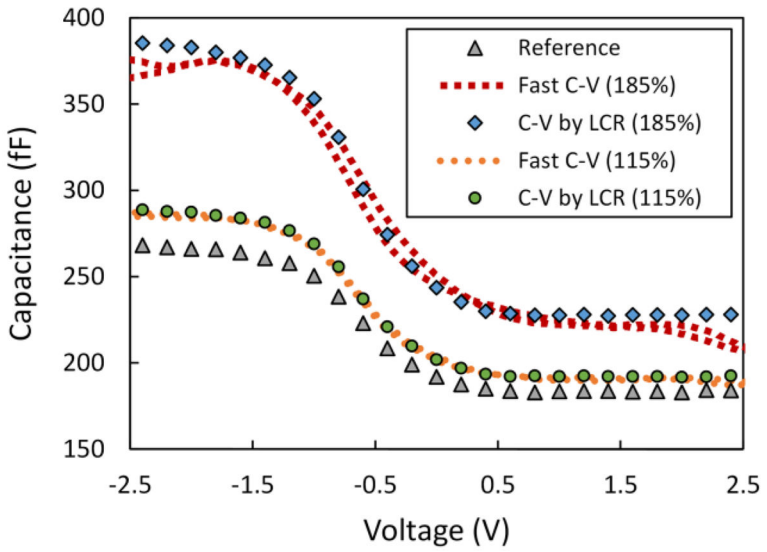

Fig. 8.

Effect of the difference between device under test and the reference device in fast C-V measurement. The sample with very different size (185%) from the reference (100%) clearly works far less well than the sample with relatively close size (115%). Pad capacitance was measured (separately) to be ~130 fF for all the MOS capacitors.