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Polarization of Bi$_2$Te$_3$ thin film in a floating-gate capacitor structure

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Metal-Oxide-Semiconductor (MOS) capacitors with Bi$_2$Te$_3$ thin film sandwiched and embedded inside the oxide layer have been fabricated and studied. The capacitors exhibit ferroelectric-like hysteresis which is a result of the robust, reversible polarization of the Bi$_2$Te$_3$ thin film while the gate voltage sweeps. The temperature-dependent capacitance measurement indicates that the activation energy is about 0.33 eV for separating the electron and hole pairs in the bulk of Bi$_2$Te$_3$, and driving them to either the top or bottom surface of the thin film. Because of the fast polarization speed, potentially excellent endurance, and the complementary metal–oxide–semiconductor compatibility, the Bi$_2$Te$_3$ embedded MOS structures are very interesting for memory application. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4904003]

Topological insulators (TIs) are materials that have an insulator (or semiconductor) bulk and gapless surfaces which are protected by time reversal symmetry.[1] These materials have a Dirac cone at the surface that can be detected by angle resolved photo emission spectroscope (ARPES).[2,3] The electrons at the TI surface can be considered as massless Dirac fermions.[4,5] Therefore, carriers in these surface states have fast response and high mobility.[6] The robustness of the TI surface states is protected by time reversal symmetry and is resistant to external perturbations such as defects and electric field.[7]

Several groups have recently reported the surfaces state analysis and the magneto-electric effects of the TI materials.[8–11] They found that different quantum states can coexist in the surface and can be changed by external magnetic field which breaks the time reversal symmetry. However, these studies were mostly based on theoretical approach, delicate surface characterization method (e.g., ARPES), or scanning tunneling microscopy (STM). There is limited progress in the study of device applications. It would be very important and interesting to study how the TI materials behave in a device structure. We have previously reported a study of high-performance TI nanowire field effect transistor (FET) in which the TI materials acted as a conducting medium.[12] FETs based on topological crystalline insulator SnTe thin film have also been recently demonstrated.[13] Besides the emerging interests in TI, typical TI materials such as Bi$_2$Te$_3$ have also attracted a lot of attention as thermoelectric material.[14] However, the study of floating-gate structure in which TI materials are surrounded by dielectric has not yet been reported. It would be very interesting to see how the TI materials behave with a vertical electric field across them, as well as how they act as an information storage medium.

Information storage is of great interest in microelectronics. It is well recognized that the future information technology relies on novel electrically accessible non-volatile memory (NVM) with high speed and high density.[15] There are several NVM candidates, including ferroelectric NVM, charge-storage memory (e.g., flash memory), molecular memory, and resistance random-access memory (RRAM).[16–19] Among them, ferroelectric NVM is very attractive for its low power consumption, fast write/erase and good endurance.[11] However, the conventional perovskite ferroelectric materials are disadvantageous for low storage density and high integration cost.[20,21]

In this work, we fabricated Metal-Oxide-Semiconductor (MOS) capacitors with a Bi$_2$Te$_3$ thin film sandwiched by two oxide layers. The Bi$_2$Te$_3$ film acts as a "floating gate" similar to the poly-Si floating gate in a FLASH memory. We have studied the polarization of the Bi$_2$Te$_3$ thin film for memory application. Such a hybrid MOS structure is very interesting for information storage and can also provide a good platform to study the properties of TI materials.

The schematic of the MOS capacitor structure is shown in Fig. 1(a). The Bi$_2$Te$_3$ film was inserted in between the SiO$_2$ and Al$_2$O$_3$, forming a metal/Al$_2$O$_3$/Bi$_2$Te$_3$/SiO$_2$/Si (MABOS) capacitor structure. The fabrication of these MABOS capacitors followed a conventional photolithographic procedure. The substrate is low doped (doping concentration about 10^{15} cm^{-3}) n-type Si wafers with 300 nm thermally grown SiO$_2$. First, an active area (100 μm × 100 μm, 50 μm × 50 μm, 25 μm × 25 μm, or 10 μm × 10 μm) was defined by etching through the 300 nm SiO$_2$ on n-Si wafers. The wafers were then oxidized at 900 °C for 22 min to achieve 11 nm dry SiO$_2$. The dry oxide was thinned down to 6 nm by 2% HF etch for

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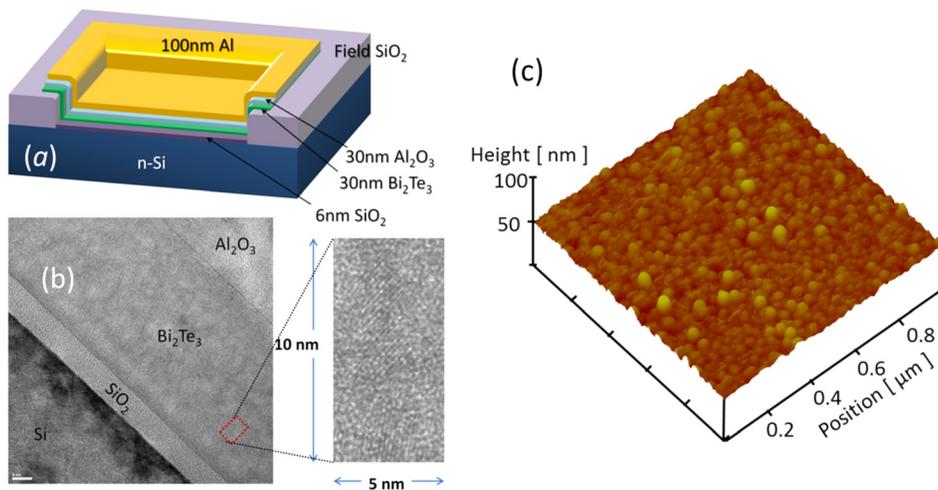
FIG. 1. (a) Schematic of the capacitor with Al/Al$_2$O$_3$/Bi$_2$Te$_3$/SiO$_2$/Si structure. (b) High-resolution transmission electron microscopy (HRTEM) image of the capacitor cross-section. The scale bar is 5 nm in the image. The rectangular HRTEM image (10 nm × 5 nm) on the right is an amplification of the Bi$_2$Te$_3$ film within the red rectangle on the left image, showing the polycrystalline structure in the film. (c) AFM image of Bi$_2$Te$_3$ film grown on SiO$_2$ with OH-hydroxyl groups by ALD.

60 s. Then, atomic layer deposition (ALD) was used to deposit 30 nm Bi$_2$Te$_3$ and 30 nm Al$_2$O$_3$ on the samples followed by the formation of top Al gate. The extra Bi$_2$Te$_3$, Al$_2$O$_3$, and Al top gate beyond the active region were removed by ion mill before electrical measurement. Finally, the samples were annealed at 300 °C in Ar by rapid thermal annealing (RTA).

The detail ALD conditions for Bi$_2$Te$_3$ and Al$_2$O$_3$ are as following. The Bi$_2$Te$_3$ thin films were synthesized using bismuth trichloride (BiCl$_3$) and (trimethylsilyl) telluride ((Me$_3$Si)$_2$Te) as ALD precursors. The growth temperature was 170 °C. The BiCl$_3$ precursor was volatilized at a temperature of 140 °C, and the Te precursor was heated at 45 °C. Furthermore, 10 sccm of N$_2$ was used as a carrier gas flow for the precursors. The ALD reaction chamber base pressure was kept at 40 mTorr (5.33 Pa). The deposition of Al$_2$O$_3$ thin film followed a conventional ALD procedure which uses trimethylaluminum (TMA, Al(CH$_3$)$_3$) and O$_2$ plasma as precursors. The growth temperature was 300 °C. N$_2$ was used as a carrier gas and the ALD reaction chamber base pressure was kept at 20 mTorr (2.67 Pa).

The resulting devices were first characterized with the transmission electron microscopy (TEM). The TEM image of the MOS capacitor cross-section (shown in Fig. 1(b)) indicates that the Bi$_2$Te$_3$ is poly-crystalline. Atomic force microscopic (AFM) image of the Bi$_2$Te$_3$ film grown by ALD on SiO$_2$ is shown in Fig. 1(c). It clearly shows that the Bi$_2$Te$_3$ is poly-crystalline, and the film is uniform with a smooth surface. The whole process we used is compatible with complementary MOS (CMOS) technology, which provides a smooth transition to the application in microelectronics.

Then, capacitance-voltage (C-V) characterization was carried out by using an impedance analyzer (Agilent® E4980A Precision LCR Meter) and a vacuum probe station (Lake Shore® FWPX Cryogenic Probe Station). During the measurement, the samples were kept in 4×10^{-7} Torr (5.33×10^{-5} Pa) vacuum. Fig. 2 shows the C-V characteristics of MABOS capacitors with an area of 100 μm × 100 μm. The C-V measurement was carried out at 1 MHz. These capacitors exhibit a hysteresis in C-V characteristics at room temperature. The hysteresis has a same direction of ferroelectric base capacitors.[22,23] As shown in Fig. 2(a), the flat-band voltage (V_{FB}) of the C-V curve shifted to positive direction as the gate voltage was scanned from negative to positive. The hysteresis is larger

when a larger range of gate voltage was scanned. But the hysteresis did not disappear even during a lowest voltage scan. The same hysteresis also shows in the MABOS capacitors with smaller area.

The hysteresis of MABOS capacitors is different from the hysteresis of a floating-gate memory cell. First, this hysteresis shift direction is opposite to that of a floating-gate memory device based on charge-trapping mechanism.[24,25] As shown in inset of Fig. 2(a), in a floating-gate memory cell, positive charges (holes) will tunnel from Si into the floating gate after gate voltage sweeps from negative to positive, resulting in V_{FB} shift to negative. Second, the hysteresis of MABOS capacitors exists in all sweep ranges, even in a small voltage sweep range from −3 V to 3 V. This is different from the charge-trapping devices in which the hysteresis is present only when gate voltage exceeds tunneling threshold voltage.[23,26]

In these MABOS capacitor devices, 6 nm SiO$_2$ is thick enough to prevent the electron/hole tunneling between the Bi$_2$Te$_3$ and Si at such a low electric field. Even in the worst case that a small amount of charges tunnel through the 6 nm SiO$_2$, the hysteresis shift should be in the opposite direction as mentioned above. Also, the Al$_2$O$_3$ layer is about 30 nm, thick enough to block the charge transfer between Bi$_2$Te$_3$ and the top gate metal. Therefore, the hysteresis shift must be resulted by the polarization of Bi$_2$Te$_3$ film. In detail, the polarization is a result of charge accumulation on the two surfaces of Bi$_2$Te$_3$: the electrons and holes within the Bi$_2$Te$_3$ film are separated and driven by the electric field, and then are accumulated on either surface of the Bi$_2$Te$_3$ film, building an internal electrical field in the opposite direction to the external electrical field. This is quite similar to the polarization of metals and semiconductors in an electrical field.

The movement of carriers is much faster than the displacement of atoms/ions in the ferroelectric materials. The polarization shown in the C-V hysteresis is a result of accumulation of charge carriers on the surfaces. Unlike ferroelectrics where the polarization is due to the displacement of ions in the crystal, the polarization of Bi$_2$Te$_3$ film is induced by the accumulation of carriers (electrons and holes). Therefore, the polarization of the Bi$_2$Te$_3$ film in the MABOS structure should be much faster than that of normal ferroelectric films. Also, compared to the ion displacement in
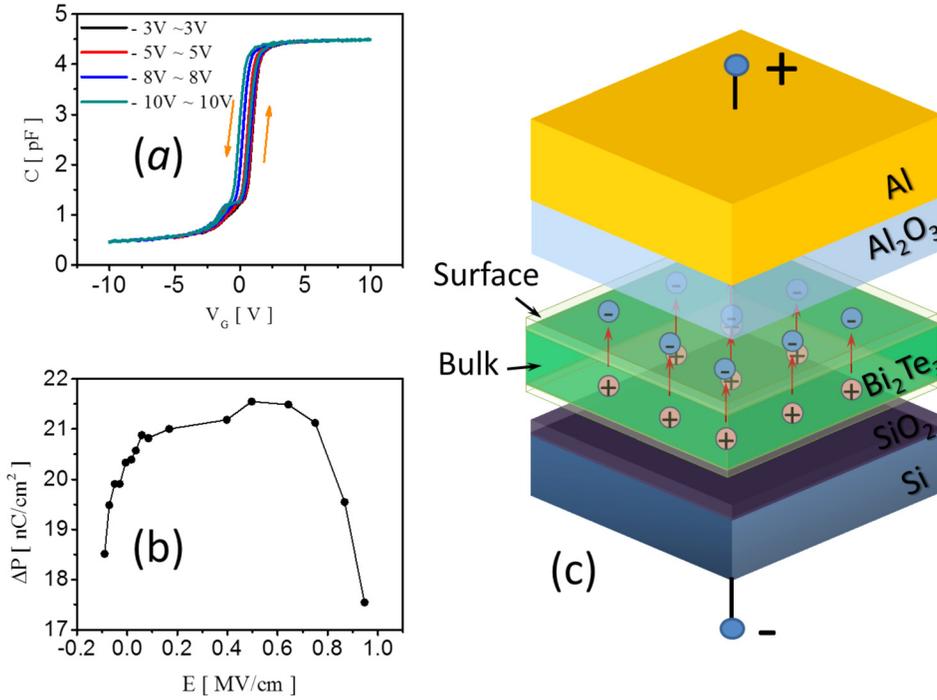
FIG. 2. (a) Capacitance-Voltage (C-V) characteristics of the Bi_2Te_3 capacitor structure at 1 MHz with different voltage sweep ranges. The area of the capacitor is $100\,\mu m \times 100\,\mu m$. (b) The changes in polarization versus the electric field at room temperature. (c) Illustration of the charge separation and polarization of Bi_2Te_3 when an external field is applied.

conventional ferroelectric materials, the electron movement should have less damage on the materials, leading to better device endurance.

To extract the polarization of Bi_2Te_3, we estimated the capacitance of dielectric layers based on the conventional model of MOS capacitor at high frequency. We can consider the polarized Bi_2Te_3 as a parallel-plate capacitor with opposite polarized carriers (electrons or holes) on each surface. So, the capacitance of insulating layers (C_{INS}) can be obtained from the capacitance in accumulation region ($100\,\mu m \times 100\,\mu m$ capacitors), that is

$$C_{INS} = 4.6\,pF. \tag{1}$$

Because the capacitance was measured with a small signal method at a high frequency, the transient polarized charges do not contribute to the total capacitance. However, this charge separation (or polarization) shifts V_{FB} of the MABOS capacitor to negative or positive directions so that the hysteresis in the C-V measurement appears. The value of the applied gate voltages at the same capacitance in forward and reverse sweep directions can be obtained. As discussed above, the difference between these two gate voltage values (ΔV_G) is due to the difference in polarization (ΔP) of Bi_2Te_3 between the two sweep directions. Their relationship can be expressed as

$$\Delta V_G = \frac{\Delta Q_P}{C_{Bi_2Te_3}} = \frac{\Delta P \cdot A}{C_{Bi_2Te_3}}. \tag{2}$$

Here, ΔQ_P stands for the difference in polarized charges between two sweep directions, A for area of the capacitor, and the capacitance of Bi_2Te_3 ($C_{Bi_2Te_3} = 6.07\,pF$) is calculated from the total insulator capacitance which is assumed to be the total capacitance of SiO_2, Bi_2Te_3, and Al_2O_3 in serial.

Fig. 2(b) shows the ΔP at different electric field. To calculate the electric field, a standard MOS capacitor with the same insulating layer capacitance (the capacitances of Al_2O_3, Bi_2Te_3, and SiO_2 in series, $\approx 4.6\,pF$) and doping concentration ($1 \times 10^{15}\,cm^{-3}$) as the measured capacitors was designed for simulation. The applied voltage of the standard MOS capacitor is recorded at the same value of capacitance measured in the experiment. This recorded voltage is over flat band voltage, i.e., gate voltage (V_G) − flat band voltage (V_{FB}). The net voltage drop across Bi_2Te_3, V_{BT}, which is partial of ($V_G - V_{FB}$), can be extracted from the serial capacitor model. The electric field is V_{BT} divided by the thickness of Bi_2Te_3. We extract the ΔP in the transition region between depletion and accumulation where the capacitance exhibits largest change with applied voltage. In the depletion or accumulation region where the measured capacitance only changes slightly with the applied voltage, the extraction of the ΔP would be inaccurate. The result indicated that the ΔP is largest around the flat-band voltage when the voltage drop across Bi_2Te_3 is small.

The memory window ΔV_{FB} is equal to the ΔV_G when the capacitance is equal to the flat band capacitance (C_{FB}). C_{FB} can be expressed as[27]

$$C_{FB} = \frac{C_{SFB} \cdot C_{INS}}{C_{SFB} + C_{INS}} = 2.92\,pF, \quad \text{and} \tag{3a}$$

$$C_{SFB} = \frac{\varepsilon_S \varepsilon_0 A}{\lambda_n} = A\sqrt{\frac{q^2 N_D \varepsilon_S \varepsilon_0}{kT}} = 8 \times 10^{-12}\,F, \tag{3b}$$

where the flat-band condition capacitance of Si (C_{SFB}) is the capacitance of Si (C_S) at flat-band condition, λ_n is the depletion width in Si at flat-band condition, A is the area of the capacitor, N_D is the doping concentration ($= 10^{15}\,cm^{-3}$), ε_S and ε_0 are Si relative permittivity and vacuum permittivity, respectively.
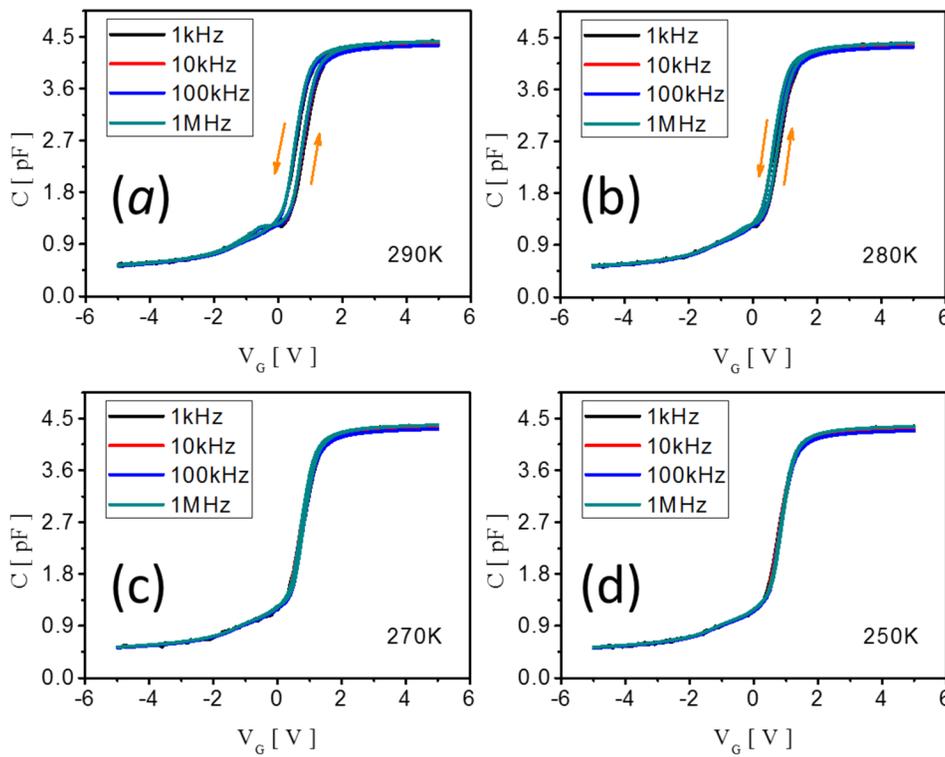
FIG. 3. C-V characteristics the Bi_2Te_3 capacitor structure at different frequencies (1 kHz to 1 MHz) at different temperatures: (a) 290 K, (b) 280 K, (c) 270 K, and (d) 250 K. The hysteresis shift decreases as the temperature decreases.

We have performed temperature-dependent C-V characterization to study the polarization formation. The sample was measured at temperatures from 80 K to 290 K. As shown in Fig. 3, the hysteresis decreases as the temperature decreases. Below 250 K, the hysteresis is very small, almost negligible (Fig. 3(d)). At each temperature, the C-V curves measured at different frequencies are approximately the same. Also, the hysteresis of the C-V curves at different frequencies is the same. This indicates that there is negligible frequency-dependence in the C-V measurement when frequency ≤ 1 MHz. In addition, the devices have been repeatedly tested for many times over a long period of duration (>6 months). The measured results are very reproducible in all these tests. The devices exhibit better programming/erasing characteristics than conventional poly-Si Flash memory (1×10^6 cycles). This is because the polarization of surface state in Bi_2Te_3 causes much less damage than hot-electron injection in conventional Flash memory cells.

Fig. 4(a) showed that ΔP changes with electric field at different temperatures. The largest value of ΔP always shows at around flat-band voltage. The ΔP decreases as the

temperature decreases and finally disappears below 250 K. Fig. 4(b) shows the memory window (ΔV_{FB}) changes versus the temperature. The quantitative analysis of polarization of Bi_2Te_3 indicates thermal activation of the surface carriers is the origin of polarization. In this case, ΔV_{FB} can be written as

$$\Delta V_{FB} = \frac{A \Delta P}{C_{Bi_2Te_3}} = \frac{A}{C_{Bi_2Te_3}} \Delta P_0 e^{-\frac{q\phi_B}{kT}}, \qquad (4a)$$

$$\ln \Delta V_{FB} = C_0 + \frac{q\phi_B}{k_B T}, \qquad (4b)$$

where ΔP_0 is a fitting parameter, and $q\Phi_B$ is the activation energy. Fig. 4(b) clearly shows that the ΔV_{FB} exponentially decreases with $1/k_B T$. We can extract the value of $q\Phi_B$ as 0.33 eV from linear fitting of $\ln(\Delta V_{FB})$ versus $1/k_B T$. This relationship between ΔV_{FB} and temperature indicates the carriers were thermally activated from surface state to bulk; and they were separated and accumulated on each surface when an external electric field was applied.

In addition, we have also fabricated and measured MOS capacitors with different thickness of Bi_2Te_3. We found that
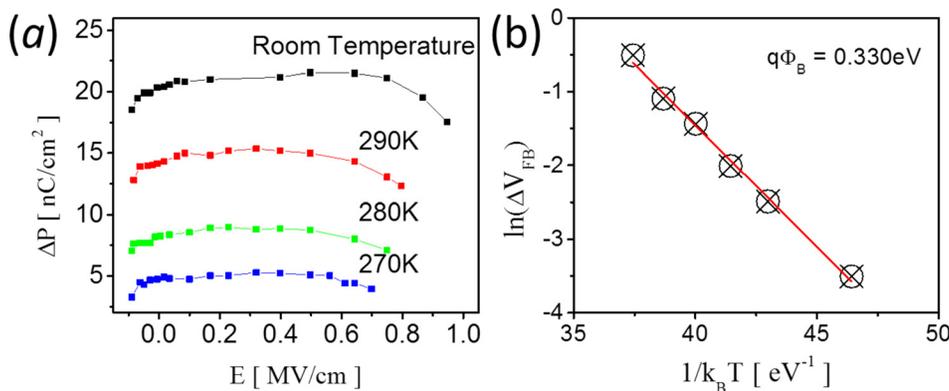
FIG. 4. (a) Polarization difference at vs. applied voltage different temperatures. (b) Memory window vs. temperature. The memory window is shrunk as the temperature decreases, indicating that the remnant polarization becomes smaller at lower temperature. The memory window is fitted as an exponential function of $1/k_B T$ ($k_B T$ is the thermal activation energy), agreeing well with both the linear- and log-scale experimental data. The activation energy is 0.33 eV according to the fitting.

MOS capacitors with Bi_2Te_3 thinner than 15 nm did not exhibit significant hysteresis. It seems that the thin Bi_2Te_3 in the capacitor behaves as a conductor. On the other hand, thick Bi_2Te_3 will significantly decrease the electric field across it, resulting in small polarization and memory window.

In summary, we have fabricated and characterized floating-gate-like MOS capacitors with a topological insulator (Bi_2Te_3) thin film sandwiched between insulating dielectric layers. The capacitors exhibited ferroelectric-like hysteresis. We have fully characterized and analyzed the hysteresis, and confirmed that it was a result of the polarization of Bi_2Te_3 under vertical electric field. Also, the polarization was identified as a result of carrier separation under vertical electric field, which is different with ferroelectrics. The thermal activation energy for the carriers (electron and hole) to separate and accumulate at the top and bottom surface of Bi_2Te_3 was extracted to be 0.33 eV which happens to be two times of the energy band gap of Bi_2Te_3. Due to the fast polarization speed and excellent endurance insured by the protected surface states, as well as the CMOS compatibility, the Bi_2Te_3 embedded MOS structures are very interesting for memory application. Besides, this work demonstrated that the floating-gate capacitor structure is an effective platform to study the properties of topological insulator thin films.

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