University of Wisconsin Milwaukee
UWM Digital Commons

Theses and Dissertations

May 2017

Fault Discrimination Using SiC JFET Based Self-Powered Solid State Circuit Breakers in a Residential DC Community Microgrid

Mengyuan Qi
University of Wisconsin-Milwaukee

Follow this and additional works at: https://dc.uwm.edu/etd

 Part of the Electrical and Electronics Commons

Recommended Citation
Qi, Mengyuan, "Fault Discrimination Using SiC JFET Based Self-Powered Solid State Circuit Breakers in a Residential DC Community Microgrid" (2017). *Theses and Dissertations*. 1531.
https://dc.uwm.edu/etd/1531

This Thesis is brought to you for free and open access by UWM Digital Commons. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of UWM Digital Commons. For more information, please contact open-access@uwm.edu.

FAULT DISCRIMINATION USING SIC JFET BASED SELF-POWERED SOLID STATE CIRCUIT BREAKERS IN A RESIDENTIAL DC COMMUNITY MICROGRID

by

Mengyuan Qi

A Thesis Submitted in

Partial Fulfillment of the

Requirements for the Degree of

Master of Science

in Engineering

at

The University of Wisconsin-Milwaukee

May 2017

ABSTRACT

FAULT DISCRIMINATION USING SIC JFET BASED SELF-POWERED SOLID STATE CIRCUIT BREAKERS IN A RESIDENTIAL DC COMMUNITY MICROGRID

by

Mengyuan Qi

The University of Wisconsin-Milwaukee, 2017
Under the Supervision of Professor Robert M. Cuzner

This thesis validates the use of ultra-fast normally-on SiC JFET based self-powered solid state circuit breakers (SSCBs) as the main protective device for a 340Vdc residential DC community microgrid. These SSCBs will be incorporated into a radial distribution system so that line to line short circuit faults and other types of faults can be isolated anywhere within the microgrid.

Because of the nature and characteristics of short circuit fault inception in DC microgrids, the time-current trip characteristics of protective devices must be several orders of magnitude of faster than conventional circuit breakers. The proposed SSCB detects short circuit faults by sensing its drain-source voltage rise, and draws power from the fault condition to turn and hold off the SiC JFET. The new two-terminal SSCB can be directly placed in a circuit branch without requiring any external power supply or additional wiring.

To achieve the coordination between upstream and downstream SSCBs in the DC community microgrid, a little change has been made to the proposed SSCB. A resistor in the schematic of SSCB has been changed to a potentiometer to have a different response time to short circuit fault. In order to figure out the value of that potentiometer to get the best coordination, a transfer function is derived.

LTspice VI and PLECS are used to verify the analytical work in the design. In the simulation layout, the DC community microgrid has been simplified to a radial system and 5 SSCBs are connected in series. Short circuit fault is applied at different locations in the DC system to test the effectiveness of the coordination scheme.

Keywords—DC community microgrid, solid state circuit breaker, fault discrimination, breaker coordination.

© Copyright by Mengyuan Qi, 2017
All Rights Reserved

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF EQUATIONS

ACKNOWLEDGEMENTS

First, I would like to express my heartfelt gratitude to my advisor Professor Robert M. Cuzner for his patient guidance. I sincerely appreciate for all those discussions and conversations in which Dr. Cuzner shared his profound knowledge and experience, and helped me to work out difficulties. I feel so lucky and blessed to have such a great advisor who spears no effort to help students. I would like to specifically thank Professor David C. Yu, for his support and encouragement to me, and for his effort to build up the cooperative relationship between University of Wisconsin-Milwaukee and the universities in China, which provide opportunities to students like me to study here.

I want to say thanks to all my friends and teammates for the things we have been through together whether good or not. Specially thanks to Yihui and James for helping me both academically and personally. The time I spent here will always be a beautiful memory for my whole life.

Finally, I would like to express my deepest appreciation to my family, for their endless love and support, only with their love I can go so far to know more about the wonderful world.

Chapter 1 Introduction

In this chapter, the background, research status, research objective and article layout are presented.

1.1 Background

Faced with the problems of greenhouse gas, energy growth demand and the depletion of traditional energy resources, renewable energy sources such as photovoltaic (PV) panels, fuel cells, and battery storages are gaining popularity recently. These kinds of renewable sources are inherently direct current (DC) and don't have the difficulty to be synchronized when connecting to each other through a common DC bus with power electronics converters. Further, this DC inherently character also makes large traditional alternating current (AC) grids not compatibly friendly to these new and renewable sources which leads to the emerging of microgrids. According to literature [1], microgrids are the key technology to meet the requirements of commercial applications of renewable energies.

A microgrid is a group of interconnected loads and distributed energy resources within clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid and it can also connect and disconnect from the grid to enable it to operate in both grid-connected or island mode. The function of energy storage devices in microgrids is to maintain the balance between energy consumption and generation when there is a sudden change in generation or loads and make microgrid system more resilient. This sudden change may come from major storm (which will affect the generation of PV panels) or an interruption in the supply of power imported from AC grids. Distributed energy sources (DES) are usually close to the load area and they can improve energy efficiency through combining electrical energy together with thermal energy. Meanwhile, using of distributed sources can reduce the emissions of carbon dioxide and help to

keep a good natural environment. Since generation positions of distributed sources are close to load, it can greatly lower the transmission loss during long-distance power delivery and can also increase the reliability of power supply and power quality. By many experts and scholars around the world, the combination of large power grids and distributed generation is considered as a feasible way to reduce energy consumption and improve the reliability and flexibility of modern power system. As shown in Figure 1-1, a typical microgrid has many kinds of distributed resources and connected to AC grid through transformers or AC to DC converters.

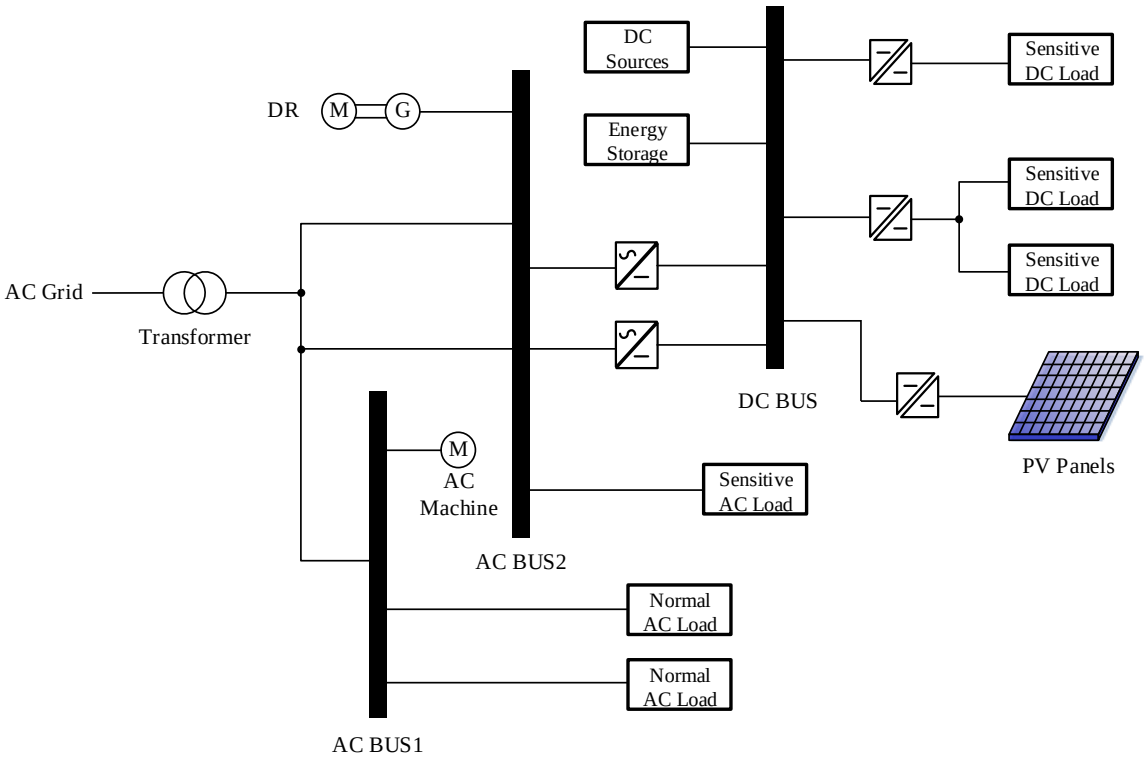

Figure 1-1 Typical layouts of a microgrid

The operations of a microgrid are very flexible. When the main AC grid is working under normal conditions, the microgrids and the AC power grid are connected and the AC grid will provide with the voltage and frequency support. While the AC grid is under maintenance or happening a fault, the microgrid can trip off and disconnect from point of common coupling (PCC). Then the

microgrid will work in island operation mode and the reliability of the whole system is relied on its control. In addition, due the “plug and play” function of distributed energy sources and controllable loads, the number of distributed power sources, loads and total power of the microgrid are in dynamic changes. Therefore, the control and energy management of microgrid are the most difficult problems and also the key technologies need to be solved. The control technology of microgrid should ensure that the access of micro powers doesn’t affect the normal operation of the main AC power system and achieve that the seamless switching between grid connected and islanded conditions. Meanwhile, the control scheme should have the ability to control the system active and reactive power independently and calibrate or regulate the voltage drop in an unbalanced system as well.

Microgrid has two types - AC microgrid, and DC microgrid. In the history of power system, DC system was used as mode of power supply contrived by Thomas Edison. The appearance of AC system, however, took the place of DC system for higher transmission efficiency and easier access [2]. With the advantages of easily transforming voltages and tuning circuits under AC condition, AC power system has been treated as the optimum alternative for transmitting power in all domains of the power system like generation, energy conversion, transmission and distribution. With the advancement attained in power electronics technologies, DC system are now fighting back and showing many irreplaceable strengths over AC system, especially in microgrids. Some key facilities like grid inverters have been invented and make DC microgrids have more access to traditional AC grids. According to reference [3] and [5], from a practical standpoint, micro-grid implementations are AC systems. AC microgrids are considered as an effective way to integrating distributed energy systems with utility power systems. Arguably, in literatures [6] to [10], DC microgrids present an effective means of integrating distributed systems and distributing high

quality power more efficiently to residential, urban and rural areas and to commercial facilities as well. DC microgrids also demonstrate substantial heightening of handling electronic loads and the debut of renewable energy sources. Furthermore, DC microgrids have less power conversion units, which means that the number of DC/AC or AC/DC converters is less and can reduce the costs compared to AC microgrids. Nevertheless, the protection of DC power system is still one of the major barriers [11].

Traditional mechanical circuit breakers, in power distribution system, are widely used for all kinds of fault protections. But in DC microgrids, mechanical circuit breakers meet some problems. 1) Long clearing time. Typical molded case mechanical circuit breakers have long response time to a fault (around several tens of milliseconds). However, the protection for power electronic devices require in a range of several hundreds of microseconds. 2) Arc extinguishing. In a DC microgrid, the DC bus voltage never pass through zero comparing to AC, so when turning off the circuit breaker, arc is generated at that moment. Arcing is very dangerous and may cause fire or damage to both devices and people. As well, it will greatly shorten the lifetime of the mechanical circuit breakers.

Nowadays, relays, reclosers, and fuses with time -coordinated characteristics that respond to phase and residual currents protect most distribution system. Sequencing and reclosing schemes of relays and reclosers use instantaneous elements, which are generally difficult to coordinate. Schemes that use instantaneous elements must balance the pros and cons of sensitivity, fuse-saving, trip-saving, cost and complexity. To solve the protection problems in DC microgrids, solid state circuit breakers (SSCB) has been invented as a cost-effective protection solution.

1.2 Research Status

1.2.1 Solid State Circuit Breaker

The concept of SSCB is not new and a lot of SSCB prototypes based on thyristor, IGCT or IGBT devices have been proposed previously. Most of the previously reported SSCBs, according to reference [12], typically rely on complex and costly over-current sensing circuitry, digital signal processing and data communication functions. In paper [13], it introduces a 400-Vdc practical SiC-SIT DC circuit breaker. The schematic of SiC-SIT DC circuit breaker is shown in Figure 1-2. This SiC-SIT circuit breaker demonstrates a much higher interruption capability in both analytical and experimental results. SiC-SITs have short channel lengths, offer ultralow conduction resistance and high breakdown voltage. And it was found that SiC-SIT is very suitable for suppressing voltage overshoots during the turnoff of the switch with the tirode-like characteristics.

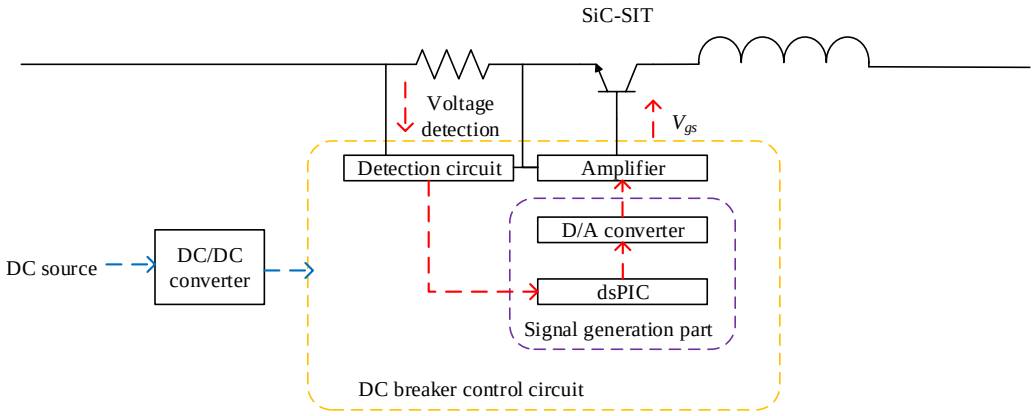

Figure 1-2 Schematic configuration of experimental circuit breaker using SiC-SIT.

Reference [14] shows a normally-off cascode structure SSCB. Its integrated short-circuit and overload protection offers reliable protection not only for the switch but also for the entire electrical equipment. The integrated voltage and current measurement allows the reactive and active power of the load to be determined. These values can be transmitted via a serial interface, thus making on-line load monitoring, metering and energy management possible.

For the previously presented SSCBs, most of them require one or more isolated auxiliary power supply to power up the control electronics of the SSCBs, which may not be available during the same short circuit fault. The gate drive and control scheme are somehow complicated so that will lead to lower reliability [15]. Therefore, it would be highly desirable to develop a simple, reliable, two-terminal SSCB with fast response time and without requiring any external power supply.

1.2.2 Wide bandgap (WBG) devices

With the development of microelectronics technology, the performance of conventional semiconductor such as Silicon (Si) and Gallium Arsenide (GaAs) has almost reached their peak due to the nature of the materials. And the opportunities for both power density and efficiency improvements of inverter have come with the development of commercially available wide bandgap (WBG) devices. "Wide-bandgap" refers to higher-energy electronic band gaps, the difference in energy levels that creates the semiconductor action as electrons switch between the two levels. Silicon and other common non-wide-bandgap materials have a bandgap on the order of 1 to 1.5 electronvolt (eV). Wide-bandgap materials in contrast typically have bandgaps on the order of 2 to 4 eV.

In general, WBG devices have high electron saturation velocity and high thermal conductivity which enables the power devices to operate at higher voltage, higher temperature and higher switching frequencies than their Si-based counterparts. Another advantage to the use of some WBG materials is that the thermal coefficient of expansion (CTE) is better suited to the ceramics used today in packaging technology.

According to literature [16], SiC unipolar devices such as JFETs or MOSFETs exhibit a very low on-resistance and a large safe operating area (SOA) below a voltage rating of 4500 volts. For the voltage rating of 1200V, SiC JFETs and MOSFETs exhibit a typical specific $R_{DS(ON)}$ of 2-4 mΩ-

cm2, or 100X lower than silicon MOSFETs or 10X lower than silicon IGBTs. Furthermore, SiC devices can sustain a much higher junction temperature under both static and transient conditions, making them suitable for SSCB applications where the energy burst during a short circuit event can drive the junction temperature beyond the silicon limit. Table 1-1 below shows the detailed information of some commercial semiconductor devices.

Table 1-1 Semiconductor devices types in detail

Devices / Parameters	Si IGBT	Si MOSFET	SiC BJT	SiC JFET	SiC MOSFET
	FGH40T120SMD	IXFB30N120P	GA50JT12-247	UJN1205K	C2M0025120D
I_D with specific T_{Case}	40A @ 100℃	23A @ 100℃	80A @ 100℃	23A @ 125℃	60A @ 100℃
R_{th}	0.27K/W	0.1K/W	0.26K/W	0.65K/W	0.27K/W
Max Junction temperature	175℃	150℃	175℃	175℃	150℃
Max P_D @ T_{Case}=25℃	555W	1250W	583W	230W	463W
P_D @ T_{Case}=100℃	277W	500W	288W	115W	185W
On-state Characteristics	$V_{CE(sat)}$=1.8V	$R_{DS(on)}$=350mΩ	$R_{DS(on)}$=20mΩ	$R_{DS(on)}$=45mΩ	$R_{DS(on)}$=25mΩ

However, WBG devices reducing the losses and increasing system power density is accompanied by higher *di/dt* and *dv/dt* which have impacts on many aspects of the system design, such as stresses on the insulation systems of any components that the WBG devices are switching against, impacts on EMI and excitation of high frequency parasitic that exist within the LCL filter components which can reduce the effectiveness of the filter if not taken into account in the filter design stage. Therefore, WBG devices not only bring better performances compared to silicon devices, but also leave new challenges and problems.

1.3 Research Objective and Article Layout

1.3.1 Research Objective

The main objective of this thesis is to study on the protection and fault discrimination of a DC community microgrids. In this thesis, it will validate the use of ultra-fast SiC JFET based self-power solid state circuit breakers as the enabling protective device in the previously-mentioned DC community microgrid. Then short circuit faults happened in different locations in the system and the coordination among all the SSCBs will be introduced. And all the theoretical analysis will be verified by simulations.

1.3.2 Article Layout

There will be 5 chapters in this thesis.

Chapter 1 will focus on the brief introduction about the development process and system characteristics for the DC microgrids. And the protection schemes for DC microgrids will also be discussed. Research objective and article layout are also included in this chapter.

Chapter2 mainly shows the DC community microgrid using WBG device-based solid state circuit breakers. The system specification for that DC community microgrid will also be included in this chapter. It is the fundamental basis that what kind of system the protective devices will work in.

Chapter 3 is about the design of the SiC JFET based SSCBs and the coordination between upstream and downstream devices. All the SSCBs are applied in a radial system and the cascaded SSCBs can be coordinated based upon compressed time-current characteristics.

Chapter 4 talks about the simulations of the working principal of SSCB and the coordination among cascaded SSCBs. All the fault scenarios in the radial system will be presented. The simulation results verify the analytical works introduced before.

Chapter 5 discusses about the conclusions and prospects future work of this thesis.

Chapter 2 A Residential DC Community Microgrid

In this section, a residential DC community microgrid is proposed which is embedded within an urban neighborhood in an underserved community in Milwaukee, Wisconsin.

2.1 Overview of Proposed DC Community Microgrid

According to literatures [17] and [18], community microgrids aim primarily at supplying electricity to a group of consumers in a neighborhood or several connected neighborhoods in close proximity community microgrids enable unique opportunities for every day consumers to take advantage of renewable energy resources, such as solar, and to utilize independently produced energy resources, such as combined heat and power (CHP), through a shared use of such resources. The proposed DC community microgrid is building in Milwaukee's Garden Homes, Wisconsin. This area used to be very prosperous and had a lot of factories. With the long period of economic recession, however, most of the factories were moving out of this district leaving many unskilled workers behind. Low income households expend over 16% of their income on utilities compared to middle class households, which spend only 3% of their income. The installations of DC community microgrid is a great opportunity for low income households to have access to cost saving and environmentally friendly resources such as PV panels and wind power. Milwaukee's Garden Homes neighborhood consists of older homes with detached garages. Within this neighborhood, there are several vacant single family homes that are being purchased and renovated by a non-profit community development corporation. The intention is to sell these homes to owner-occupant buyers which will help to stabilize the neighborhood. The community microgrid is currently being built in these vacant houses as part of an effort to revitalize under-served neighborhoods and as a means of alleviating the high relative cost of utility services to low income

households as well. In addition, their energy usage is being monitored and managed with in a non-invasive way to gather the essential information for the cloud server to help the microgrid achieve better performance.

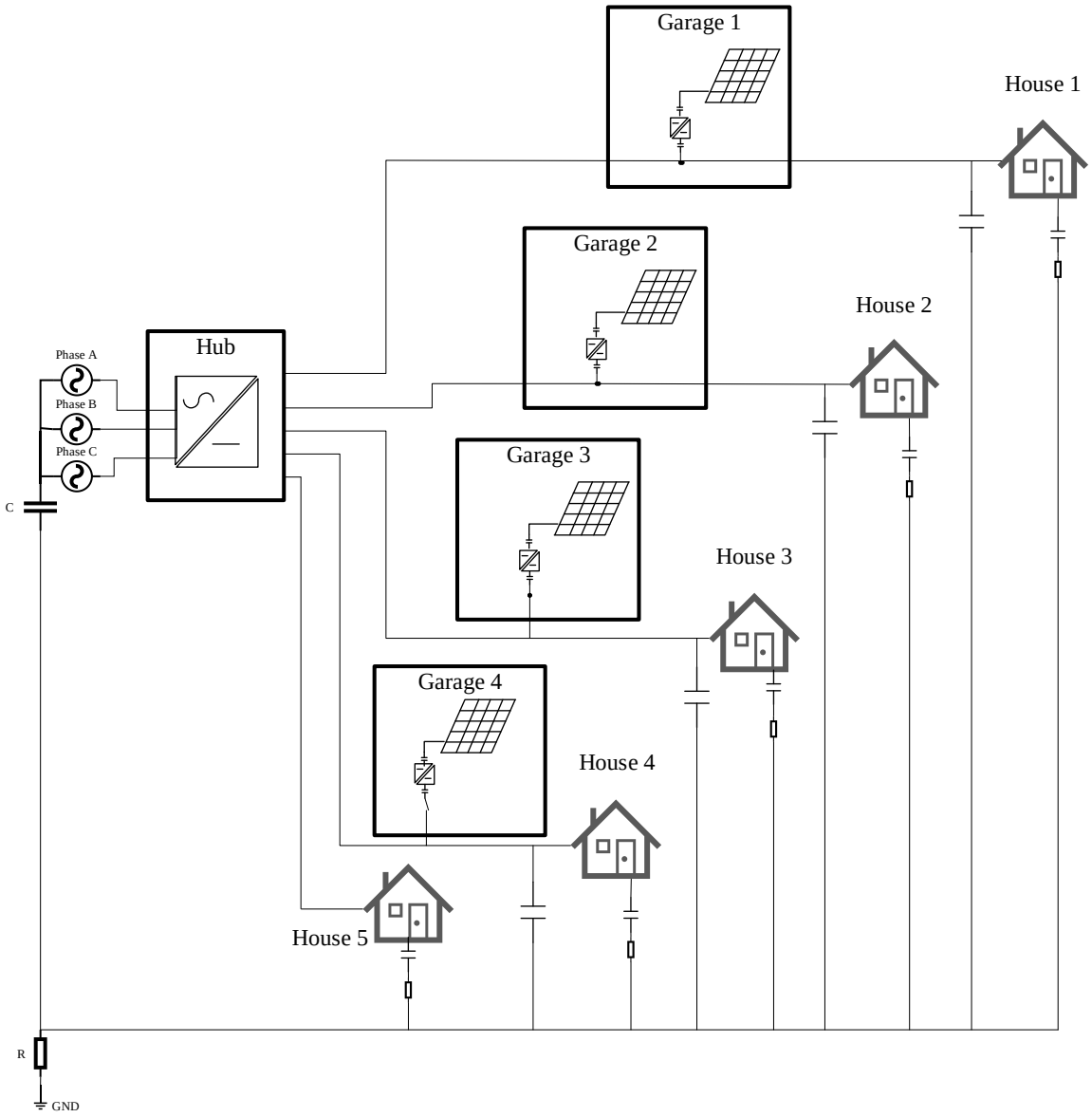

Figure 2-1 Overview of DC community microgrid

The characteristics of short circuit faults discussed in this thesis, are being analyzed in the DC community microgrid showed in Figure 2-1. As you can see in the graph, there are five houses in the community microgrid and all the houses are coming with a garage. One of the houses has been

chosen to be the hub house. The energy management system (EMS) is set up in that house or garage. PV panels are installed on the roofs of garages. The average dwelling size is 1200 ft^2 (140 m^2). Typical service to such a home is 230Vac/60Hz, 100-200A. Moreover, to have a better control of this community microgrid, battery storages have been settled in every garage.

2.2 Protections for DC Community Microgrid

2.2.1 The Problems for DC Microgrid Protections

Most of today's distribution feeders are radial and are protected by overcurrent devices, including relays, reclosers, and fuses.

Basic design criteria for the protective system [11] are:

a) Reliability—Predictability of the protective system response to faults and dependability to not trip spuriously on transients or noise; b) Speed—Fault is removed from the system and normal operating voltages is rapidly restored; c) Performance—Continuity of service to the loads; where a lower performing system loses a significant portion of its loads when a fault occurs; d) Economics—Installation and recurring costs; generally, in opposition to performance, i.e. a good performing system generally costs more; e) Simplicity—Quantity of parts, zones of protection, level control de-centralization needed to ensure its reliability.

However, the traditional overcurrent protection for AC microgrids has many limitations [19]:

1) Phase overcurrent relays must be set above the maximum load current. Therefore, maximum load expectations limit the sensitivity and speed of the protection for phase-to-phase and three-phase faults.

2) Protection settings must be checked against load levels frequently and seasonally, because load growth and extreme temperatures can result in load current tripping unfaulted circuits when energy is most needed.

3) Ground overcurrent relays must be set above the maximum load unbalance expected on the feeder. Unbalance, whether from uneven loading of the three phases, from single-phase switching operations, or from blown fuses, limits the sensitivity of ground protection.

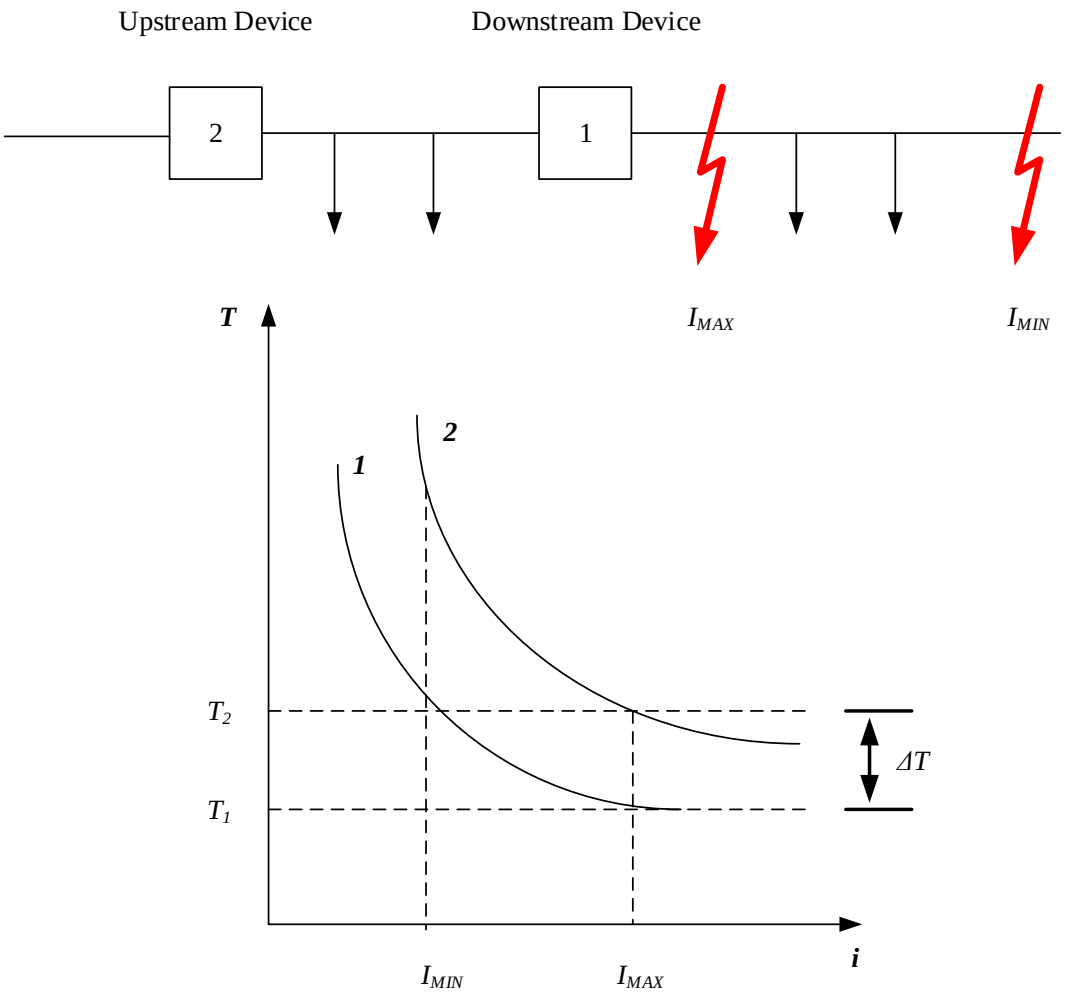

Figure 2-2 Coordination of overcurrent protection in a radial system

Overcurrent protection coordinates by current, time, or both. Figure 2-2 depicts a radial system with two inverse-time overcurrent devices. To ensure selectivity, the upstream (backup) device must wait for the downstream (primary) device to clear the fault. Otherwise, users between the upstream device and downstream devices will lose service unnecessarily. The time-current curve of the upstream device must be above the downstream device curve, with some time margin. Unfortunately, this level of selectivity requires a sacrifice in speed. Fault-clearing time increases as the fault moves to the line sections located closer to the source, where the fault current is higher. The undesirable result is longer clearing times for more severe faults.

Although instantaneous overcurrent elements provide faster tripping, they can be coordinated only when the feeder impedance creates substantial difference in fault current between close-in and remote faults. In tightly knit distribution systems, such as those in urban areas, in manufacturing plants, and aboard ships, these elements become difficult or impossible to coordinate, because the fault current may not change significantly from the source to the farthest load.

2.2.2 Characteristics of DC Microgrid Short Circuit Fault and Viable Solutions

To find a solution to the DC protection dilemma, a complete paradigm shift away from how conventional AC systems are protected must be acknowledged.

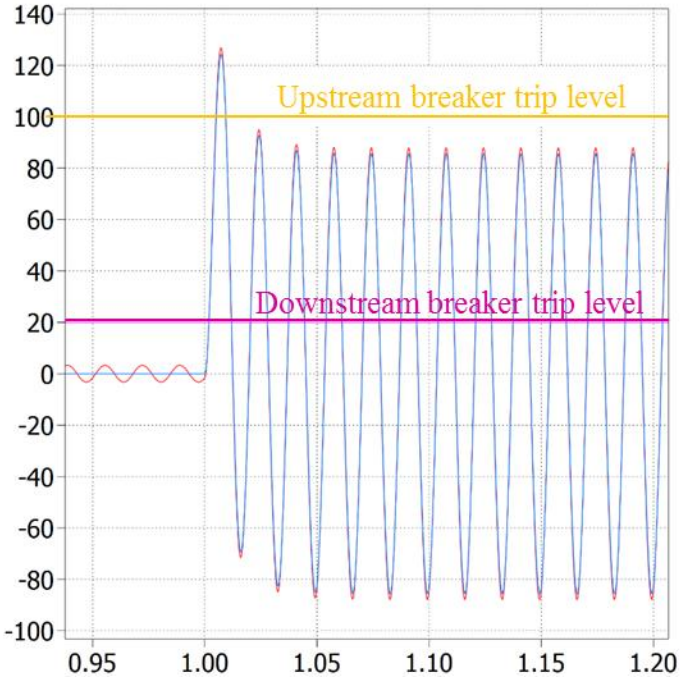

Figure 2-3 Upstream and downstream circuit breaker currents with a fault downstream of the downstream breaker location in an AC system

Figure 2-3 shows that the short circuit fault characterization in a conventional AC distribution system. In literature [20], a zero-ohm short circuit fault is applied at the location of downstream circuit breaker. As it depicts in the graph, the superimposed current and time envelopes from the set time-trip characteristic of upstream and downstream breakers show that this current does not exceed the upstream breaker's time-current trip points, which means only the downstream will be tripped and the loads between upstream and downstream will not be cut off incorrectly. The upstream and downstream circuit breakers can achieve coordination because the AC reactance limits the increasing rate of fault current.

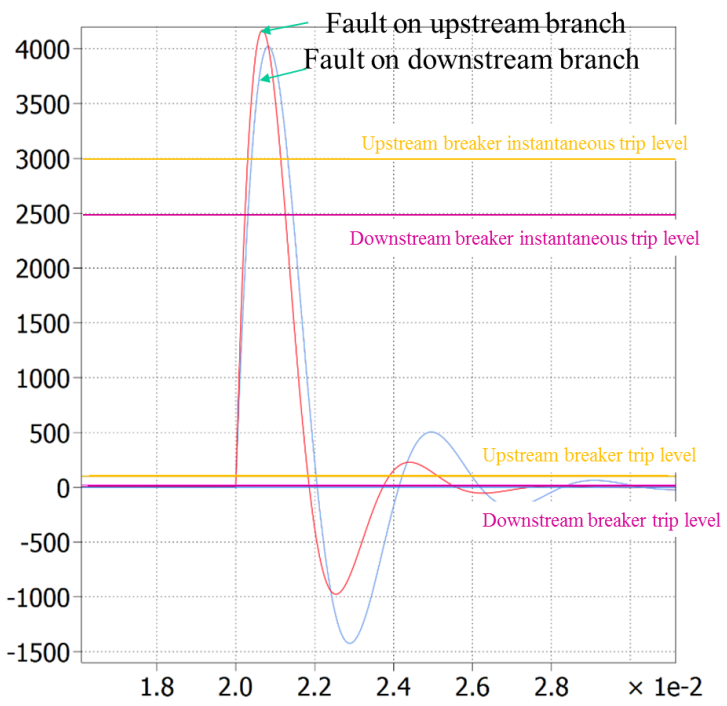

Figure 2-4 Upstream and downstream circuit breaker currents with faults at two locations in a DC system

The equivalent zero-ohm short circuit fault has been applied to both upstream and downstream circuit breaker and the simulation results are shown in Figure 2-4. The fault current for upstream (red line in picture) and downstream (blue line in picture) both exceed the time-current trip points of upstream circuit breaker, which is telling that any of that two faults will make the upstream circuit breaker tripped. The reason for this characteristic in DC system is that sudden discharge of upstream power converter filter capacitor. It is impossible for two normal circuit breakers to coordinate with the current limitation of upstream source.

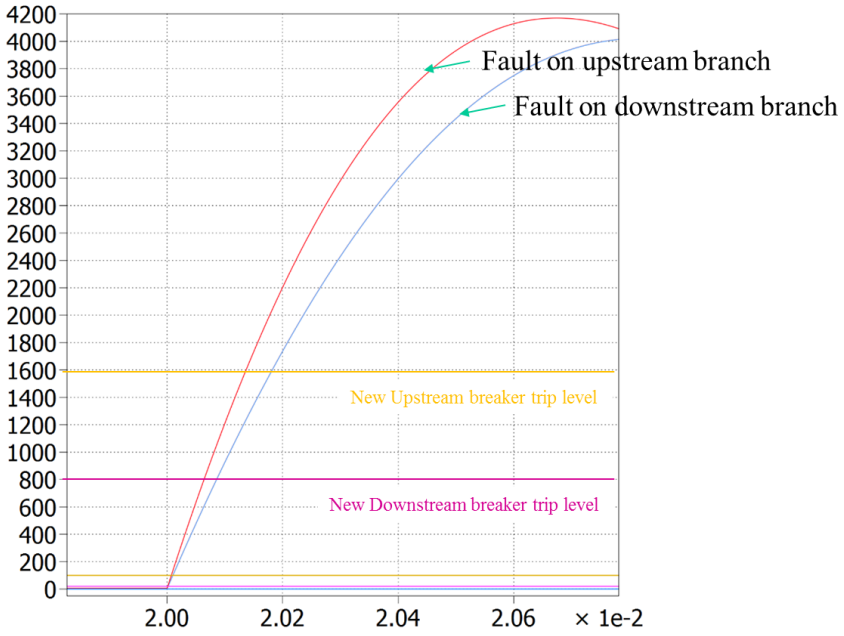

Figure 2-5 Zoomed in upstream and downstream circuit breaker currents with faults at two locations in a DC system

On the other hand, if we keep zooming in the fault starting part of DC short circuit, we will find protective devices could trip within microseconds of fault inception it would be possible to coordinate upstream and downstream devices by simple trip levels [20]. This characteristic is verified by simulation results illustrated in Figure 2-5.

The short circuit fault is characterized by the system capacitance and cable inductance, so the device must be able to act very quickly to limit current surge during sudden fault inception. Current surge is characterized by the bus capacitance and cable inductance connected to the fault, shown in the equations below:

$$i(t) = \frac{v_c(0)}{L * \omega_d} * e^{-\alpha t} * \sin(\omega_d t) \qquad \text{Equation 2-1}$$

where $\omega_d = \sqrt{\omega_0^2 + \alpha^2}$, $\alpha = \frac{R}{2 * L}$ and $\omega_0 = \frac{1}{\sqrt{L * C}}$.

As demonstrated in Figure 2-6, the traditional electromechanical circuit breakers minimum response time to fault is around several tens of milliseconds but they can achieve very high current

rating. Many SSCBs that have been proposed previously, exhibit a minimum response time about several milliseconds with a reasonable current rating. However, the typical self-protection response time of DC-AC power converter is in microsecond time scales, which means both electromechanical and previously-proposed solid state circuit breakers cannot serve as a reliable overcurrent protection for the DC power converter or DC microgrid.

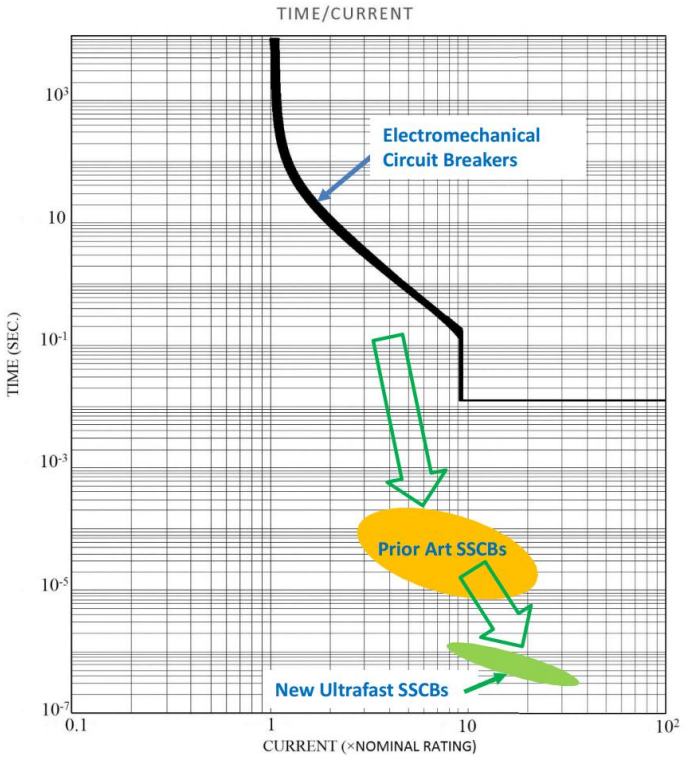

Figure 2-6 Comparison of time-current characteristics of different circuit breaker technologies

To solve this problem of DC system protection, it is required a faster circuit breaker that could reliably trip on the fault current within tens of microseconds (marked with green bubbles in Figure 2-6). If a SSCB were implemented using normally-off devices, such as an insulated-gate bipolar transistor (IGBT) or integrated gate-commutated thyristor (IGCT), the device would need to be commanded on when connected to the load and utilize external current sensing circuitry to detect a high current fault so that the switch could be commanded to the off state and thus drive fault

current to zero, removing the fault from the circuit. No load isolating switches connected in series with the solid-state portion of the SSCB would then need to open in order to isolate the fault. In reference [15] and [21], a new SSCB using a normally-on SiC JFET has been presented to provide a feasible solution to DC short circuit faults. This new SSCB shows many excellent characteristics over previously-proposed circuit breakers, such as self-powered, ultra-fast response. It offers a reaction time of 1-2 microsecond, about 10 times faster than any previously reported SSCBs and 10,000 times faster than any mechanical circuit breakers, and is well within the overload tolerance time window of a typical power converter. The basic working principals for the new SSCB will be introduced in next chapter.

2.3 Summary

In this chapter, a unique implementation of a DC community microgrid has been introduced and the protection schemes has been discussed as well. Then the characteristics of DC system is compared with traditional AC system. Finally, a viable solution, ultra-fast SSCB using normally-on SiC JFET has been presented.

Chapter 3 Normally-On SiC JFET Based SSCB and Its Coordination

In this chapter, the working principals of protective SiC JFET device and the gate driver will be discussed. To find how to achieve the coordination between SSCB, the transfer function of voltage sensor network is derived.

3.1 Concept of Normally-On SiC JFET based SSCB [22]

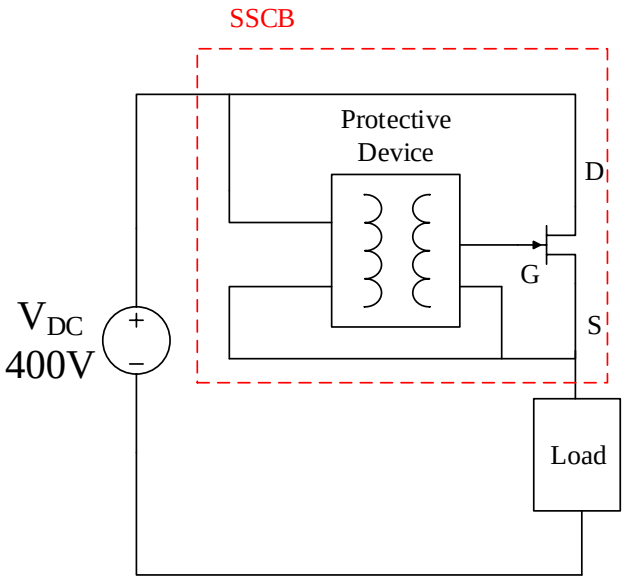

Figure 3-1 A unidirectional self-powered SSCB using a normally-on SiC JFET as the main static switch and a fast-starting isolated DC/DC converter as the protection driver

In Figure 3-1, the block diagram of proposed normally-on SiC JFET based SSCB has been illustrated. The SiC JFET SSCB is very similar to conventional electromechanical circuit breakers with no extra wires except for two terminals. The SSCB is built with 3 main parts: a normally-on SiC JFET served as the main static switch, a voltage sensing network as the detective probe of short circuit fault and a fast-starting isolated DC/DC converter as the switch driver. During normal working conditions, the normally-on SiC JFET carries a normal load current from the DC source

to loads with a relatively small voltage drop. This voltage drop is too small to activate the isolated DC/DC converter and the gate of SiC JFET is unbiased, which means SiC JFET is working under its on-state operation area. When there is a short circuit fault happening in the system, the SSCB detects the fault by sensing the voltage drop between its drain and source rather than the current passing through it. The voltage drop between drain-source, when exceeding a threshold value about 3-5 volts, will make the isolated DC/DC converter begin to work and the output of isolated DC/DC converter will generate a negative voltage to turn off the SiC JFET. Therefore, the SSCB can discriminate the short circuit fault very fast and it withdraws power from the fault to power itself up until the short circuit fault is removed. After the fault has been cleared, the drain-source voltage of the SSCB will reduce to normal and the SiC JFET will turn on again.

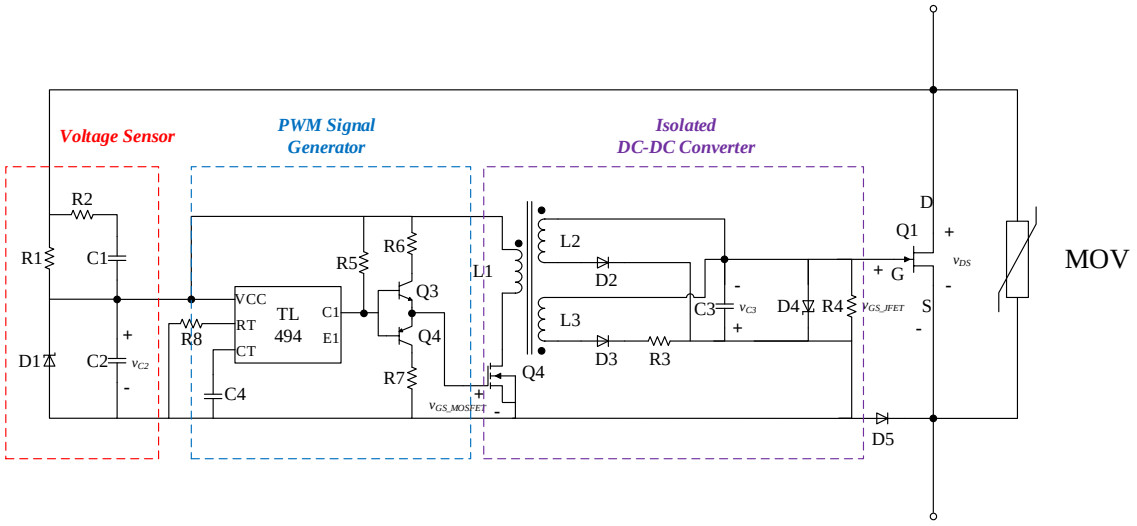

Figure 3-2 A detailed circuit schematic of the SSCB with a combined forward-flyback DC/DC converter design

Figure 3-2 shows the schematic of the SiC SSCB in detail. A commercial normally-on 1200V SiC JFET (UJN1205K from USCi) [23] is used in this project. The JFET exhibits a typical $R_{DS(ON)}$ of 45 mΩ at zero gate bias and a breakdown voltage of 1420 V at a gate reverse-bias of -16V. This normally-on characteristic, while undesirable for most power converter applications, is ideal for this SSCB design due to the extremely small conduction resistance.

The driver for the protection device is made up with a voltage sensor network, a pulse width modulation (PWM) signal generator and an isolated DC/DC converter. When a short circuit fault occurs, the drain-source voltage of the JFET suddenly increases as a result of a large overcurrent through the JFET. For example, an overcurrent of 200A will yield a drain-source voltage of 9V assuming the 45mΩ JFET does not enter its quasi-saturation regime yet. Capacitors C1 and C2 are charged through resistor R2 in the voltage sensor network. When the current continues to charge C2 and the voltage across C2 hits the threshold value around 3-4 volts, PWM signal generator will be activated. The PWM generator will provide the gate signal of MOSFET Q2 through a simple amplifier circuit made up with two transistors and turn Q2 on and off to transfer energy from primary winding to secondary windings of the transformer. The isolated DC/DC converter is a combined forward and flyback converter to achieve a faster response time. When Q2 turns on during the initial cycle, charge from C2 is quickly transferred to the output capacitor C3 via the forward secondary winding L3 of the transformer. The negative C3 voltage is quickly established between the gate and source of the JFET. At the end of the first PWM cycle, the flyback secondary winding L2 starts to charge C3 and contributes to the negative gate biasing of the JFET. After around 2-3 duty cycles, the voltage on C2 accumulates to hit the threshold value of -16V and the JFET will be turned off.

When the JFET is turned off, the L3 winding of transformer becomes solely responsible for maintaining the negative JFET gate voltage while the forward secondary winding is no longer active. The reason is that the voltage on C2 decreases slightly and thus the voltage induced in the forward secondary winding L3 drops below the voltage of C3 after the initial transient phase. So, the forward converter cannot transfer energy from L1 to L3. After the JFET is fully turned off, the DC bus voltage is entirely dropped across the JFET, supplying a current of approximately 22 mA

through R1 to keep the SSCB off. Resistor R4 dissipates a small amount of power during the protection mode and serves the purpose of resetting the JFET gate voltage to zero once the short circuit fault is cleared. A metal-oxide varistor (MOV) device is used to clamp a voltage spike between the drain and source of the JFET caused by a parasitic inductance in the circuit when the fault current is interrupted. D5 is a blocking diode to prevent current flow through the protection driver in the reverse direction.

3.2 Operation of Protection Driver

In this ultra-fast SiC JFET based SSCB, a flyback topology was initially adopted for the protection driver. To achieve shorter response time of the SSCB, a new combined forward-flyback topology is investigated using an additional secondary winding of the transformer. The design considerations of these two different topologies will be discussed in the following sections.

3.2.1 SSCB with Flyback Topology

The isolated DC/DC converter shown in Figure 3-2 could be reduced to a flyback topology when L3, D3 and R3 are removed. The switching waveforms of the SSCB implemented with the flyback topology are shown in Figure 3-3, and will be introduced as following.

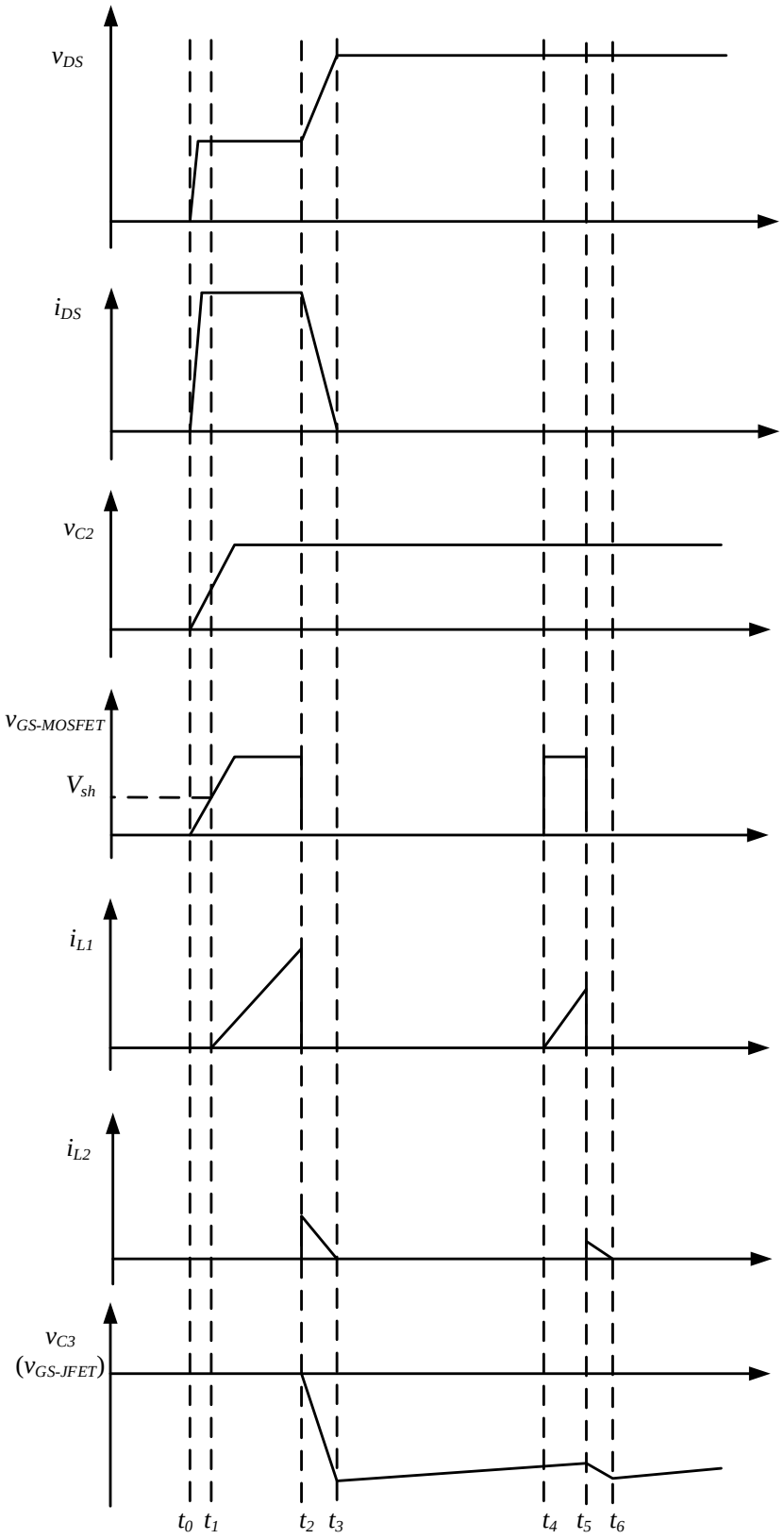

Figure 3-3 Switching waveforms of SSCB with a flyback DC/DC converter

At *t0* a short circuit event occurs. The current through the JFET i_{DS} increases immediately and the drain-source voltage of the JFET v_{DS} also increases proportionally, due to the on-resistance of the JFET. Both i_{DS} and v_{DS} reach a plateau at *t1* given by

$$i_{DS}(t) = \frac{V_{DC}}{R_{DS(ON)} + R_{SC}} \quad \text{Equation 3-1}$$

$$v_{DS}(t) = i_{DS} * R_{DS(ON)} \quad \text{Equation 3-2}$$

where V_{DC} is the DC bus voltage, $R_{DS(ON)}$ is the on-resistance of the JFET, and R_{SC} is the short circuit loop resistance. Strictly speaking, the rate of rise of i_{DS} is also limited by the parasitic inductance in the short circuit loop.

C1 and C2 are charged by drain and source current v_{DS} via R2 during the short circuit fault. The voltage on C2 is derived by

$$v_{C2}(t) = \frac{C1}{C1+C2} v_{DS}(t) * (1 - e^{-\frac{t(C1+C2)}{R2C1C2}}) \quad \text{Equation 3-3}$$

The voltage of C2 is applied between the gate and source of the MOSFET Q2 through R6 and Q3. The gate-source voltage of Q2 v_{GS_MOSFET} is the same as v_{C2} during this time period.

At *t1*, the C2 voltage v_{C2} first exceeds the threshold voltage (roughly 3 V) of the MOSFET Q2 and then the minimum supply voltage of the PWM control IC (roughly 4.5 V). Q2 is turned on through R5, R6, and Q3. Current of L1 begins to flow through the primary side of the transformer

$$i_{L1} = \frac{V_{C2}}{L_1}(t - t_1) \quad \text{Equation 3-4}$$

At *t2*, Q2 is turned off by the PWM control IC. The energy stored in the transformer is transferred to the flyback secondary winding L2 and to charge C3. The L2 current i_{L2} decreases as v_{C3} increases, until i_{L2} becomes zero at *t3*. The energy stored in C3 at *t3* is approximately given by

$$\frac{1}{2} v_{C3}^2(t_3) = \frac{1}{2} i_{L1}^2(t_2) \quad \text{Equation 3-5}$$

The JFET is turned off by the negative voltage between its gate and source. The fall time is estimated by

$$t_3 - t_2 = \frac{1}{2}\pi\sqrt{L_2 * C_3} \qquad \text{Equation 3-6}$$

At *t3*, the SSCB is completely turned off, and the responsibility of protection driver from this point on, is only to maintain the negative voltage of C3. Between *t3* and *t4*, C3 is partially discharged through R4 until the falling edge of the next PWM pulse at *t5*. The flyback DC/DC converter charges C3 again from *t5* to *t6* during the second switching cycle. It repeats this operation until the short circuit fault is cleared. R4 serves the purpose of maintaining a zero-biasing voltage on the JFET gate in absence of short circuit faults.

3.2.2 SSCB with Combined Forward-Flyback Topology

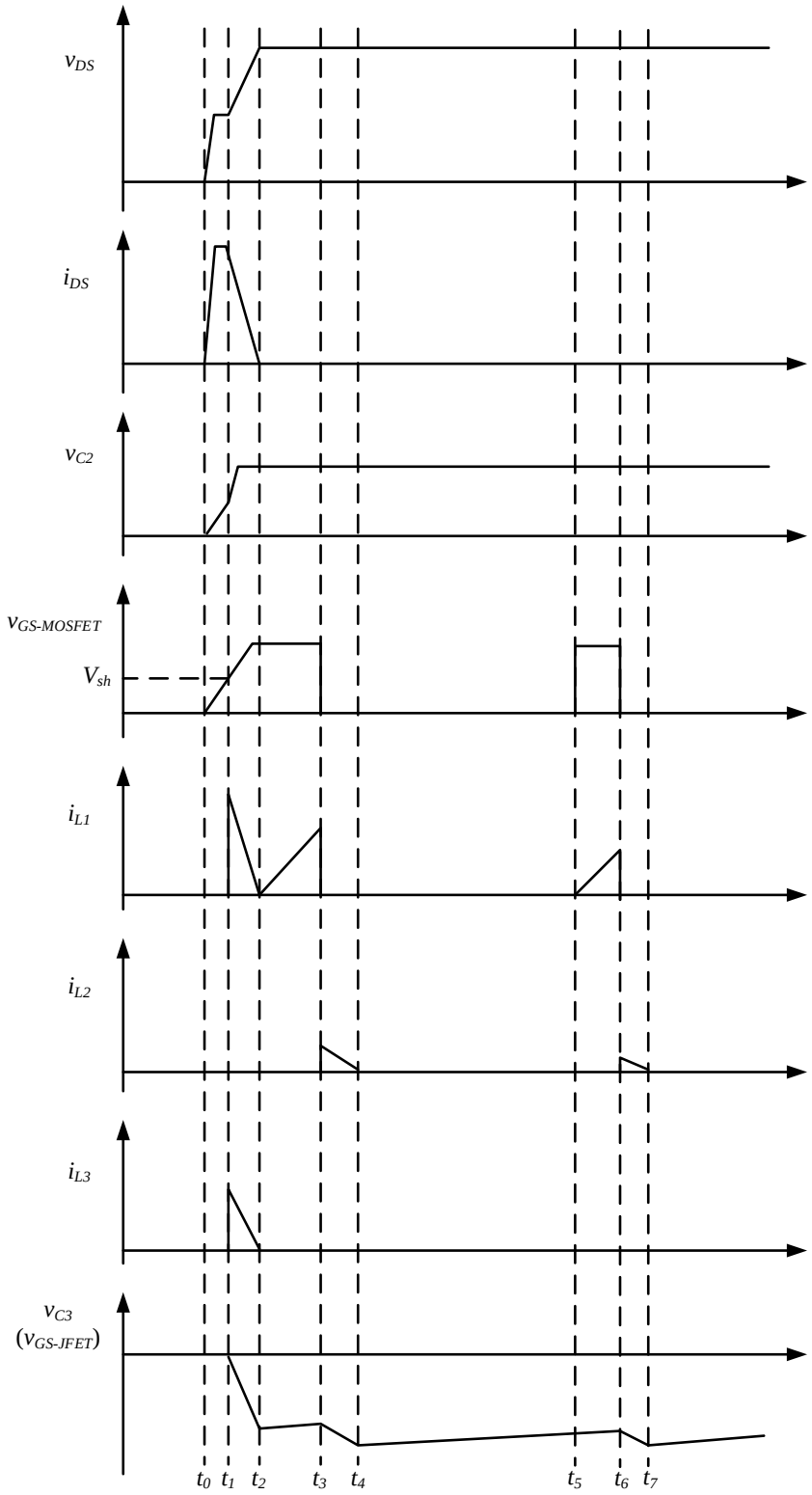

Figure 3-4 Switching waveforms of SSCB with a combined forward-flyback DC/DC converter

The switching waveforms of the SSCB implemented with a combined forward-flyback topology are shown in Figure 3-4. The operation of the combined forward-flyback DC/DC converter during the period of *t0* to *t1* is the same as the previously-mentioned flyback-only topology.

At *t1*, the C2 voltage v_{C2} first exceeds the threshold voltage (roughly 3V) of the gate drive chip TL494 and will activate MOSFET Q2. Q2 is turned on and the energy passes through R5, R6, and Q3. Voltage v_{C2} is directly dropped across the primary winding of the transformer and immediately transferred to the forward secondary winding L3. Current from L3 flows through D3 and R3 to charge C3 to provide a negative voltage between gate and source of SiC JFET. The voltage of C3 v_{C3} is given by

$$v_{C3}(t) = nV_{C2} * (1 - e^{-\frac{t}{R3C3}}) \qquad \text{Equation 3-7}$$

where *n* is the transformer turn ratio of L3/L1. At *t2*, C3 is charged to the induced voltage of L3 which is derived by

$$v_{C3}(t_2) = V_{L3} = n * V_{L1} = n * V_{C2} \qquad \text{Equation 3-8}$$

At *t2*, i_{L3} decreases to zero, and diode D3 turns off. The JFET is turned off by the negative voltage between its gate and source.

During the period of *t2* to *t3*, primary current i_{L1} of the transformer continues to ramp up like in a typical flyback transformer.

At *t3*, Q2 is turned off and the energy stored in the primary winding of transformer during the period of *t2* to *t3* will be transferred to secondary part through flyback secondary winding L3 and charge C3 to a voltage level more negative than the previous value established by the forward mode charging between *t1* and *t2*.

After *t3*, D3 will remain reversely biased and the forward winding L3 is no longer active. The flyback converter is now solely responsible for maintaining the negative JFET gate voltage, and repeatedly charges C3 until the short circuit fault is cleared.

3.3 The Coordination of SSCBs

Achievement of accurate and reliable fault discrimination in DC microgrids is a significant challenge given both the demanding speed of response and the dynamically changing configurations. Present day solutions rely upon relaying and communications between fault isolating devices (FIDs) and grid-feeding converters [22]- [29], but due to the demand for high speed of response of the FIDs, the success of accurately isolating a fault to its location is diminished by sensing and communications delays and increasing reliability involve increasing costs beyond what would be acceptable for residential distribution systems.

As shown in Figure 3-2 before, the SSCB can be divided in three part, voltage sensor network, PWM signal generator and isolated DC/DC converter. To fulfill coordination, the fault clearing time among the SSCBs in different locations should be different, so the design of the SSCBs need to be modified. The PWM signal generator part is realized by a commercial PWM control IC (Texas Instruments TL494 [30]) with a fixed frequency PWM control scheme. The PWM IC is configured to provide a pulse width of 2 microseconds and a PWM frequency of 60kHz during the steady state operation. The isolated DC/DC converter is actually a combined forward and flyback converter. The isolation function is fulfilled by a Q4436-BL flyback regulator transformer. The manufacturer for the transformer is Colicraft. It has two secondary windings, forward winding and flyback winding. Turns ratio between primary winding and secondary winding is 1: 2.5. These two parts are based on the packaged model and hard to be modified comparing to voltage sensor

network. The time-current trip coordination between upstream and downstream SSCBs can be accomplished through a simple resistor adjustment in the voltage sensing circuit.

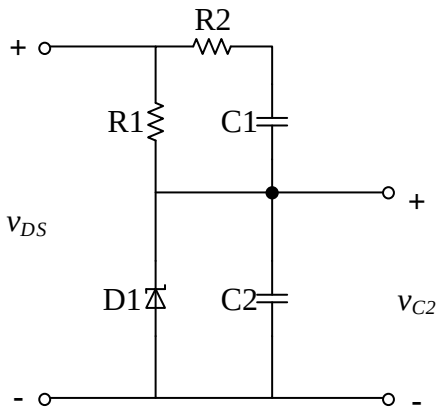

Figure 3-5 Voltage sensor network

The voltage sensor network is basically a RC network, shown in Figure 3-5. During the starting stage, the fault current will charge C2 through the RC network and different parameters for RC network will lead to different charging time. In order to find how does the voltage sensor network affect the charging time, the transfer function for RC network is given by

$$\frac{v_{C2}}{v_{DS}} = \frac{(R1+R2)C1\cdot s+1}{C1C2R1R2\cdot s^2+(C1R1+C1R2+C2R1)\cdot s+1} \qquad \text{Equation 3-9}$$

where V_{C2} is the voltage across C2, and V_{DS} is the voltage dropped between JFET drain and source terminals. Through this transfer function and aforementioned Equation 3-3, it clearly shows that the value of R2 has significant influence on the charging time. So, different values of R2 has been applied to test which one can achieve the best coordination.

Next step, a simulation model is built in MATLAB/ SIMULINK to verify the analytical work that has been done before. A real network was built together with a transfer function based network. According to the transfer function and experiences, different values for the R2 have been chosen which are 6.1 Ω, 20 Ω, 33 Ω, 47 Ω and 68 Ω respectively. The simulation results are shown in

Figure 3-6. The charging time of V_{C2} is increasing when the value of R2 is bigger.

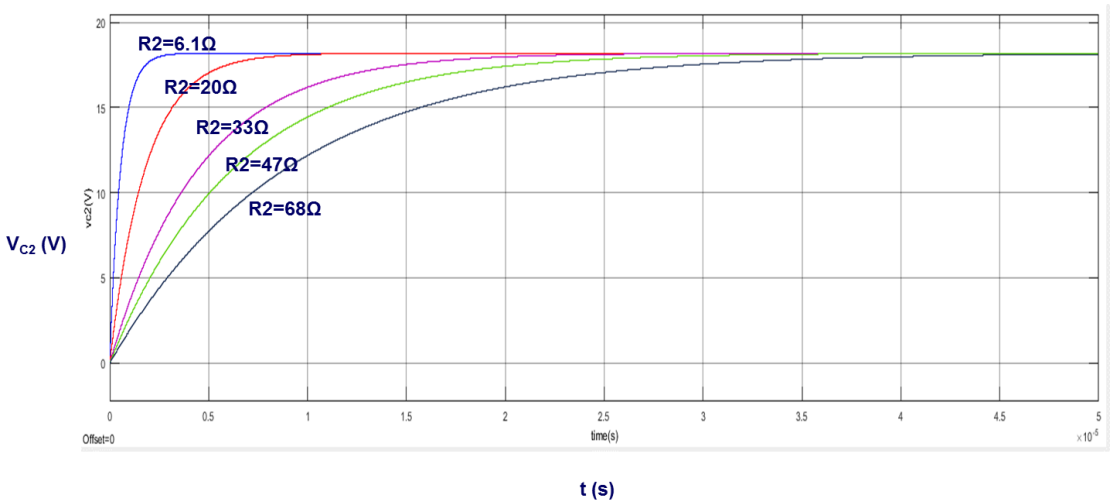

Figure 3-6 The simulation results of charging time of V_{C2} under different resistances

Chapter 4 Simulation Results and Analysis

In this chapter, the fault scenarios are simulated in both LTspice and PLECS. The simulation results have been analyzed to verify the coordination between SSCBs.

4.1 Description of the Simulation Model

In this thesis, a simulation model of SiC JFET based ultra-fast SSCB has been built in LTspice. The reason for choosing LTspice is that it can import SPICE component and the SiC JFET device can be modeled. The parameters for SiC JFET is imported from datasheet and the device is built into a subsystem. As shown in Figure 4-1 The Spice model for SiC JFET in LTspice VI, it is the SPICE model for SiC JFET built in LTspice. Table 4-1 shows the exact values of the typical performance of the SiC JFET.

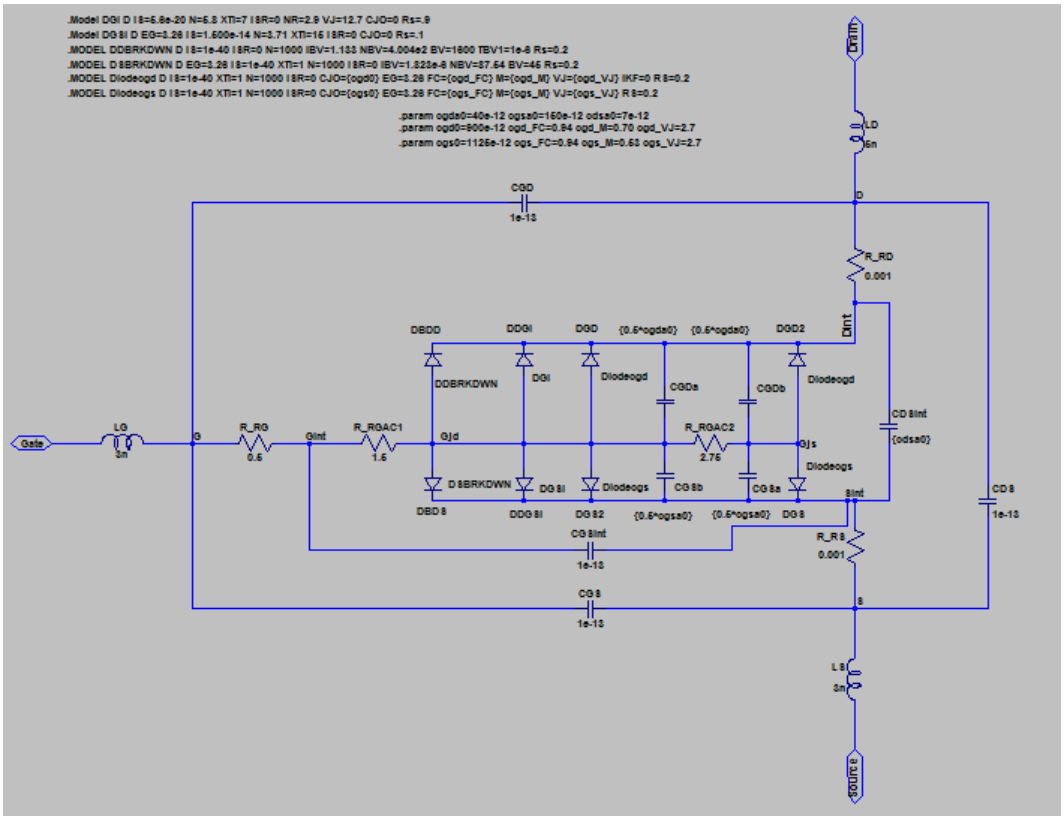

Figure 4-1 The Spice model for SiC JFET in LTspice VI

Table 4-1 Typical static performance of UJN1205K3

Parameter	Symbol	Test Conditions	Value	Units
Drain-Source Breakdown Voltage	BV_{DS}	V_{GS} = -20V, I_D = 1mA	1200	V
Total Drain Leakage Current	I_D	V_{DS} = 1200V, V_{GS} = -20V, T_j = 175 ℃	30	μA
Total Gate Leakage Current	I_G	V_{GS} = -20V, T_j = 175 ℃	10	μA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 2V, I_F = 30A, T_j = 175 ℃	105	mΩ
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5V, I_D = 70mA	-6	V
Gate Resistance	R_G	V_{GS} = 0V, f = 1MHz	5	Ω

Figure 4-2 shows the SSCB model built in PLECS. PLECS Blockset is a unique tool for the fast simulation of power electronic circuits within the MATLAB/Simulink environment as a toolbox. It allows combined simulations of electrical circuits modeled in PLECS with controls modeled in Simulink. For the reason that there is no JFET model in PLECS, an ideal IGBT with 45 mΩ conduction resistance has been used to replace the SiC JFET in SSCB. Also, PLECS doesn't have models for chips like PWM signal generator TL494 so the gate drive for JFET is replaced using the transfer function mentioned before to achieve the same purpose. The transfer function stands for the voltage sensing network and a delay block is basically representing the signal delays brought by PWM signal generator and isolated DC/DC converter (which is around 3 microseconds). This 3 μs response time is because the initial startup delay of the PWM control IC (the width of the first PWM pulse to drive the MOSFET Q2) and the delay of charging time of C3 connected between gate and source of SiC JFET.

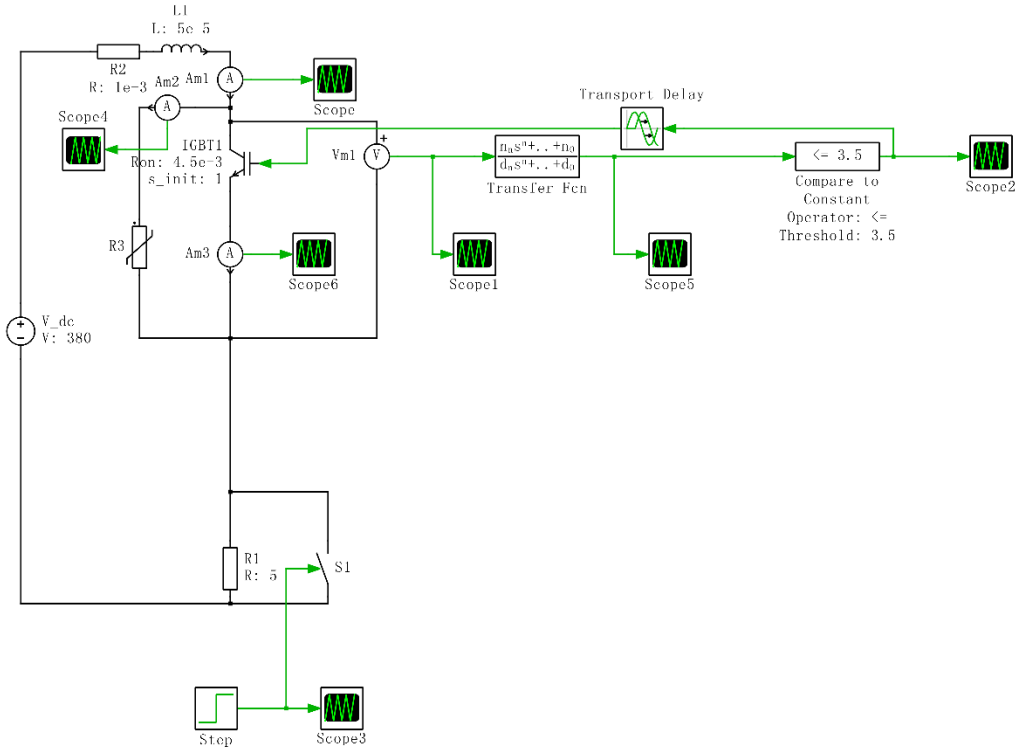

Figure 4-2 Simplified SSCB simulation model in PLECS

4.2 Fault Scenarios for Short Circuit in DC Community Microgrid

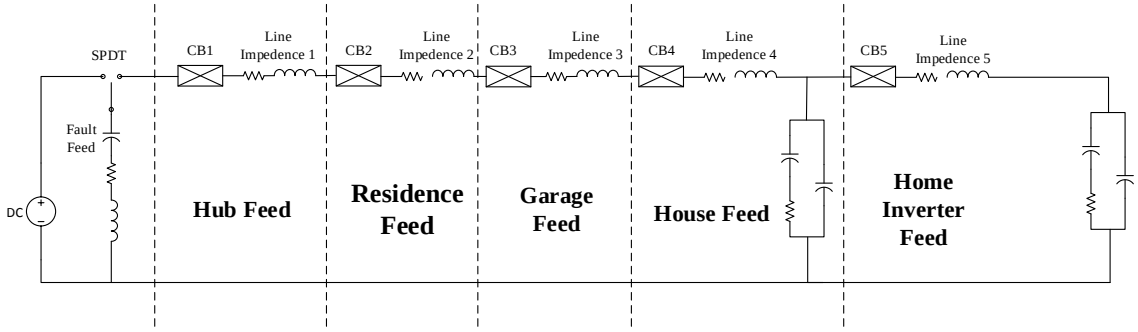

Figure 4-3 Simplified system overview of DC community microgrid

The proposed DC community microgrid has been simplified to a radial system shown in Figure 4-3. There are five SSCBs in the microgrid and they are connected in series. These five SSCBs are exactly the same except for the “R2” in their voltage sensor network. Five SSCBs divide the simplified model into five parts, which is hub, residence, garage, house and home inverter. Strictly

speaking, there are some other branches connected to the simplified radial system and when short circuit faults happen, fault current will feed from these branches as well (the fault current from branches are marked with yellow lines). Figure 4-4 exhibits the fault scenario with feeding from branches. However, in this thesis, this case will not be discussed due to the space limitation.

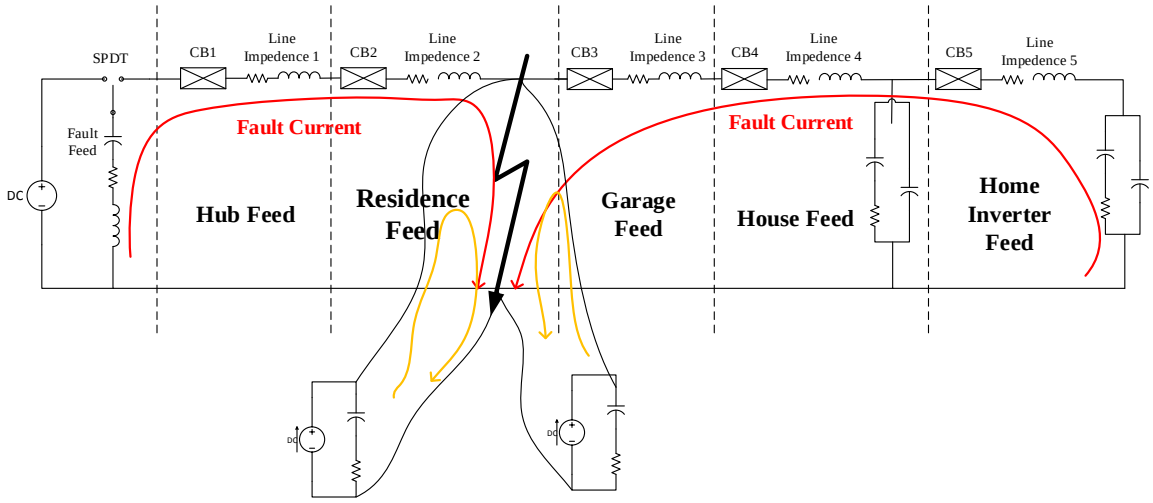

Figure 4-4 Fault scenario with feeding from paralleled branches

These five parts are connected through underground cables buried in the basements of the dwellings. The configurations of these underground cables are shown in Table 4-2.

Table 4-2 Line Configurations

	Inductance (μH)	Resistance (mΩ)	Length (m)
Line 1	0.33	0.35	20
Line 2	24.6	103	411
Line 3	6.28	16.9	15
Line 4	0.84	2.2	3
Line 5	1.67	20	6

In this DC community microgrid, short circuit fault can happen at five positions after the CB1, CB2, CB3, CB4 and CB5. Figure 4-5 to Figure 4-9 show the fault scenarios of the faults happen

in all these five positions. The red lightning mark in the pictures means the short circuit fault location and the red line shows the flow directions of fault currents.

Scenario A

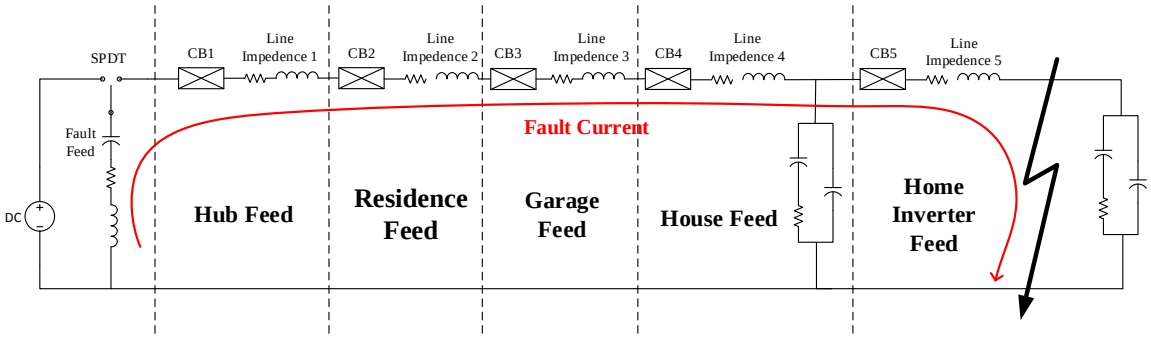

Figure 4-5 Fault scenario A

Scenario B

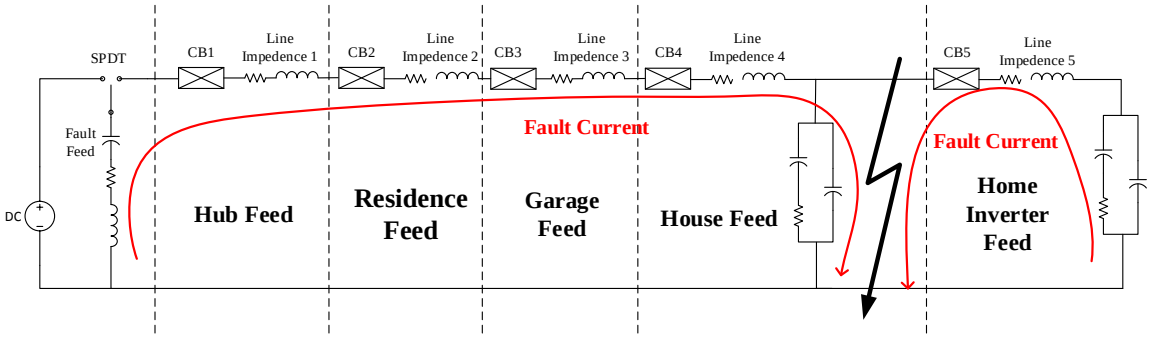

Figure 4-6 Fault scenario B

Scenario C

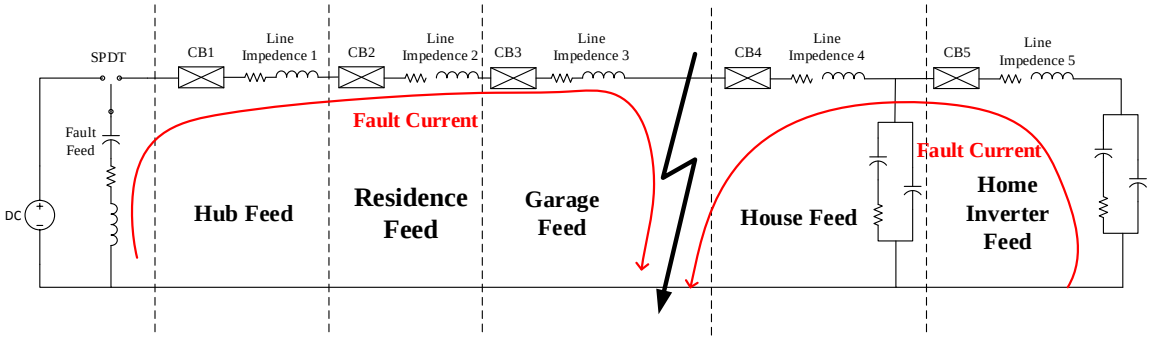

Figure 4-7 Fault scenario C

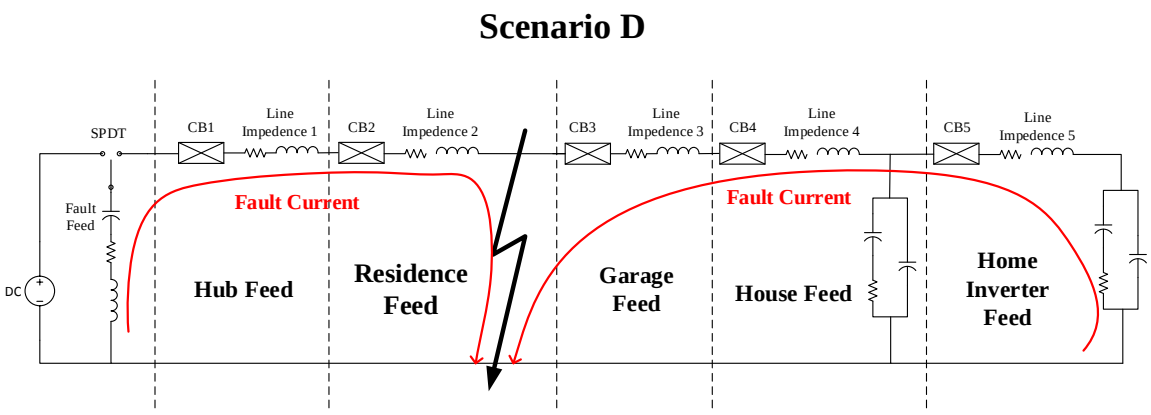

Figure 4-8 Fault scenario D

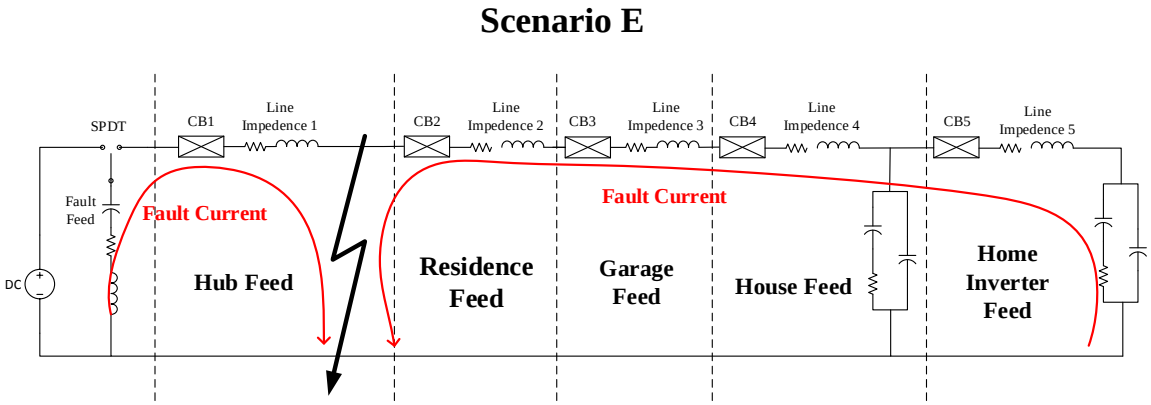

Figure 4-9 Fault scenario E

4.3 Simulation Results in LTspice

4.3.1 System Layout in LTspice

Figure 4-10 and Figure 4-11 show the overview of system layout and the SSCB model built in LTspice. It basically looks the same as the simplified radial system (schematic was shown before in this thesis), but there are two different parts I must make it clear.

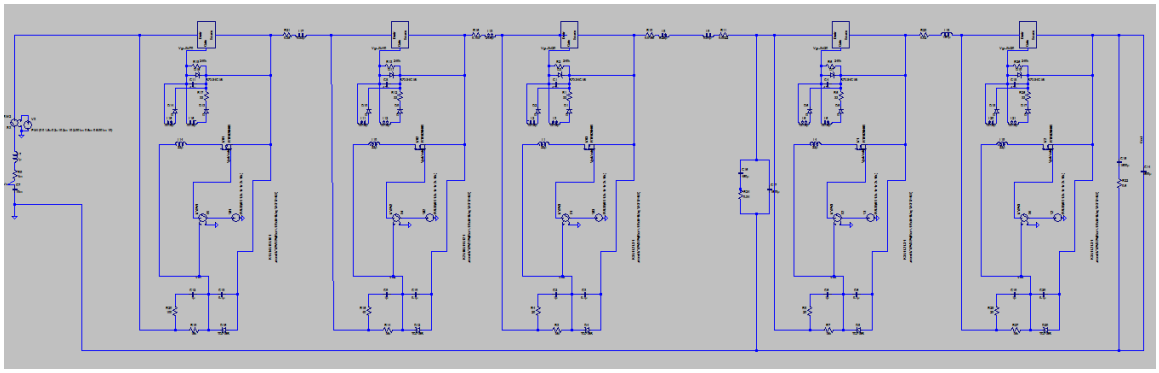

Figure 4-10 Overview of simulation model in LTspice

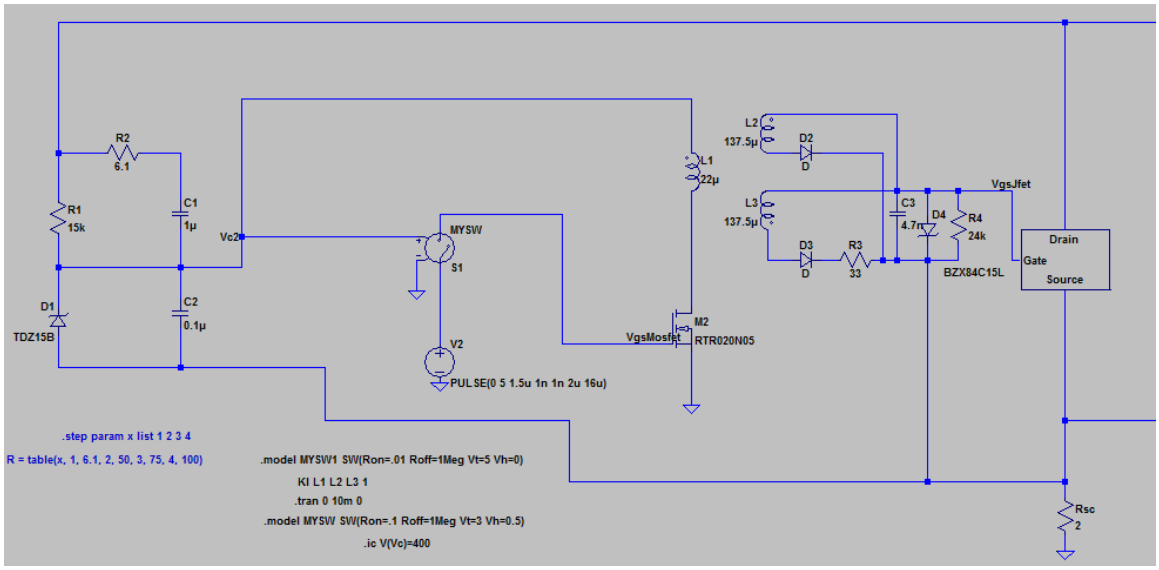

Figure 4-11 Detailed SSCB model in LTspice

First, as you can see from Figure 4-10, there is no Metal Oxide Varistor (MOV) in the system. MOV is not available in the component library in LTspice and customized component also has been proved cannot work together with SSCB model (the simulation steps are not matched between SSCB and customized MOV). In order to continue the simulations in LTspice, the MOV should be removed. Without MOV protecting the SiC JFET, voltage across the device will be go to very high level and this will be exhibited in the simulation results.

Second, LTspice doesn't have a component that has the function to perform like PWM signal generator chip TL494. To achieve the trigger mechanism discussed before, a simple comparator and a repeated sequence generator are put as a replacement in the circuit. When the voltage from the voltage sensor get from C2 is over 3.5V, the output of the comparator will change from 0 to 1 and activates the repeated sequence generator. Then the sequence generator will give out a repeated square wave signal with 12.5% fixed duty cycle to the gate of MOSFET Q2. It basically imitates the function of TL494.

4.3.2 Fault Scenario A

In fault scenario A, the short circuit fault happens at home and the fault current will feed both from DC source through CB1 to CB5. To achieve coordination, as discussed before, it should be CB5 to turn off and clear the short circuit fault to avoid unnecessary power cut. The simulation circuit of scenario A is illustrated in Figure 4-12.

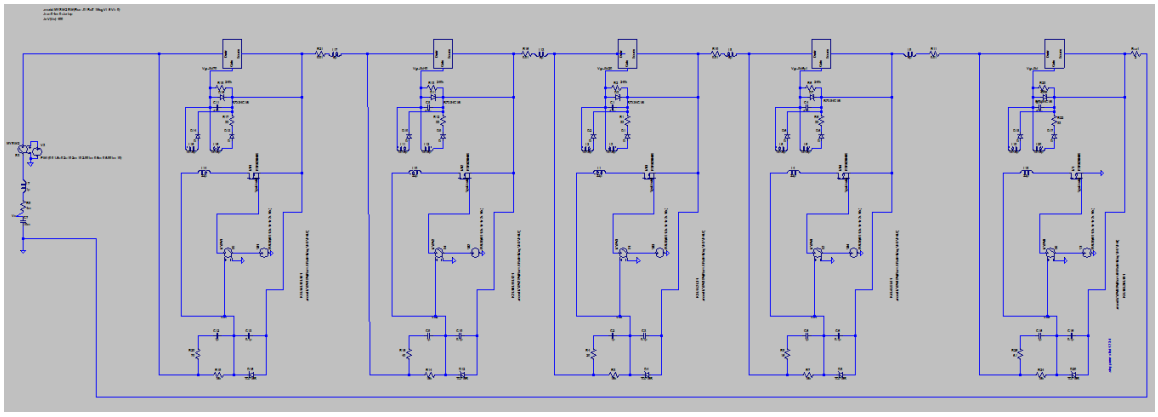

Figure 4-12 The simulation circuit of scenario A in LTspice

The traces in Figure 4-13 and Figure 4-14 show the V_{C2} and V_{GS} of all 5 SSCBs in scenario A. Among all the V_{C2} of all 5 SSCBs, all of them are showing an increasing trend (means all SSCBs are response to the fault), but only the V_{C2} of CB5 increases to over 3.5V, which is the threshold value that required for activating the PWM signal generator. For V_{GS}, all SSCBs are decreasing at

starting stage, but almost the same as V_{C2}, only the V_{GS} of CB5 goes to -16V and provide the essential reversed bias to turn off the SSCB. Therefore, the traces V_{C2} and V_{GS} for illustrates the coordination between SSCBs in scenario A.

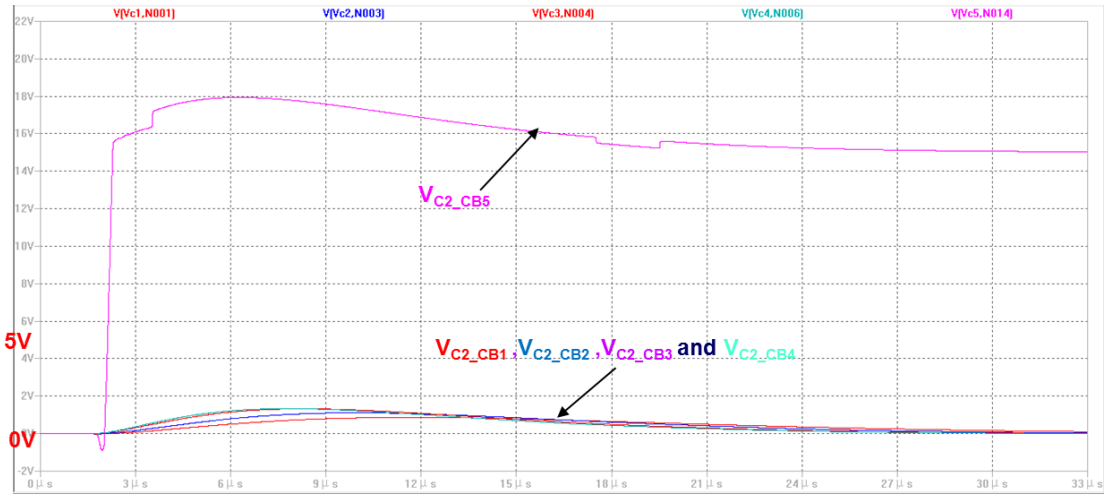

Figure 4-13 V_{C2} of all 5 SSCBs in scenario A

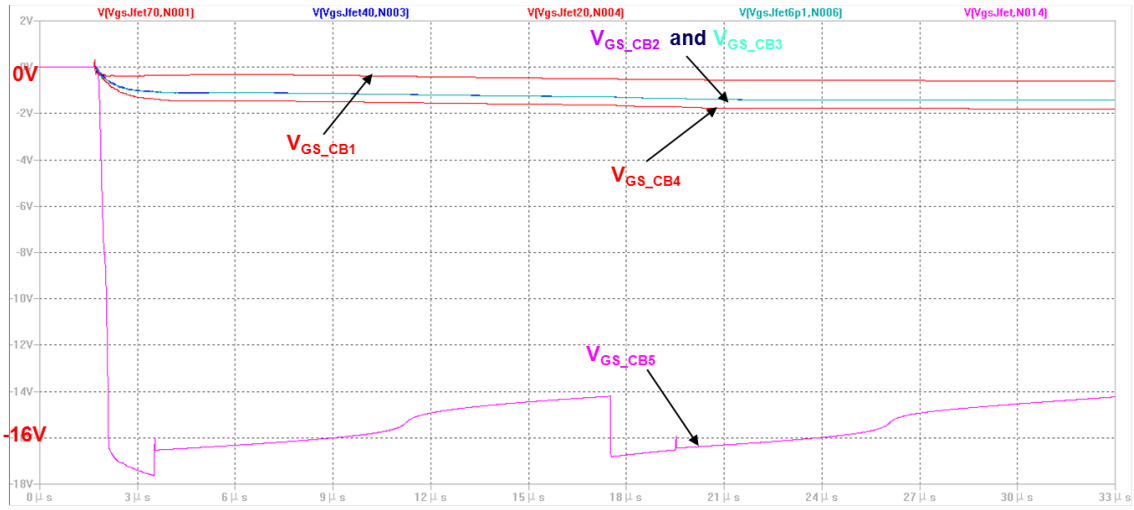

Figure 4-14 V_{GS} of all 5 SSCBs in scenario A

The voltages on SSCBs in scenario A are displayed in Figure 4-15. As you can see from the picture, the VCB5 is around 400V and the others are nearly 0V. It means CB5 has been turned off, takes all the voltage from DC source and isolates the fault.

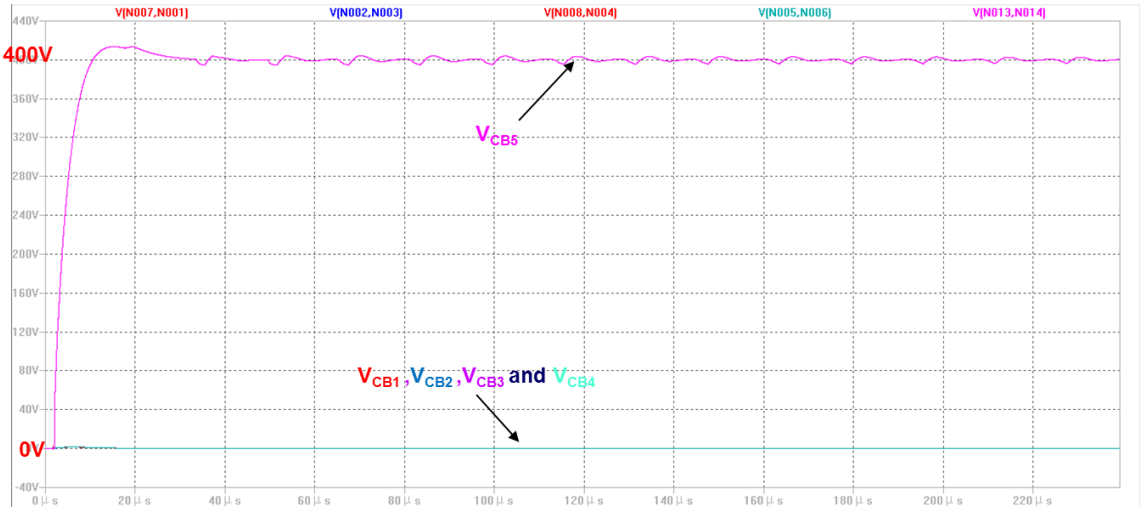

Figure 4-15 The voltage drop on SSCBs in scenario A

4.3.3 Fault Scenario B

For scenario B, the short circuit fault takes place at residence feed. Fault current will feed the fault location from DC source through CB1, CB2, CB3 and CB4 and also from home inverter. To achieve selection, CB4 need to discriminate the fault and CB1 to CB3 shouldn't be triggered. The LTspice simulation circuit of scenario B is illustrated in Figure 4-16.

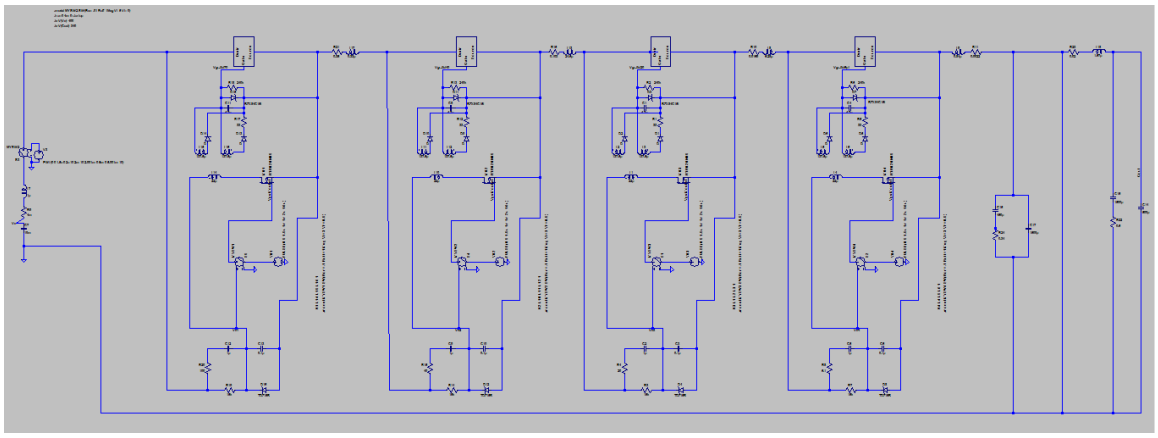

Figure 4-16 The simulation circuit of scenario B in LTspice

The traces in Figure 4-17 and Figure 4-18 show the V_{C2} and V_{GS} of all 4 SSCBs in scenario B (CB5 has been removed). Among all the V_{C2} of all SSCBs, similar with scenario A, only the V_{C2}

of CB4 increases the threshold value that can activate the PWM signal generator chip. For V_{GS}, all SSCBs are decreasing at starting stage, but almost the same as V_{C2}, only the V_{GS} of CB4 goes to -16V and provide the reversed bias to turn off the SiC JFET. The fault current shown in the picture is getting back to zero after the protective device turning off, which means the fault has been removed successfully.

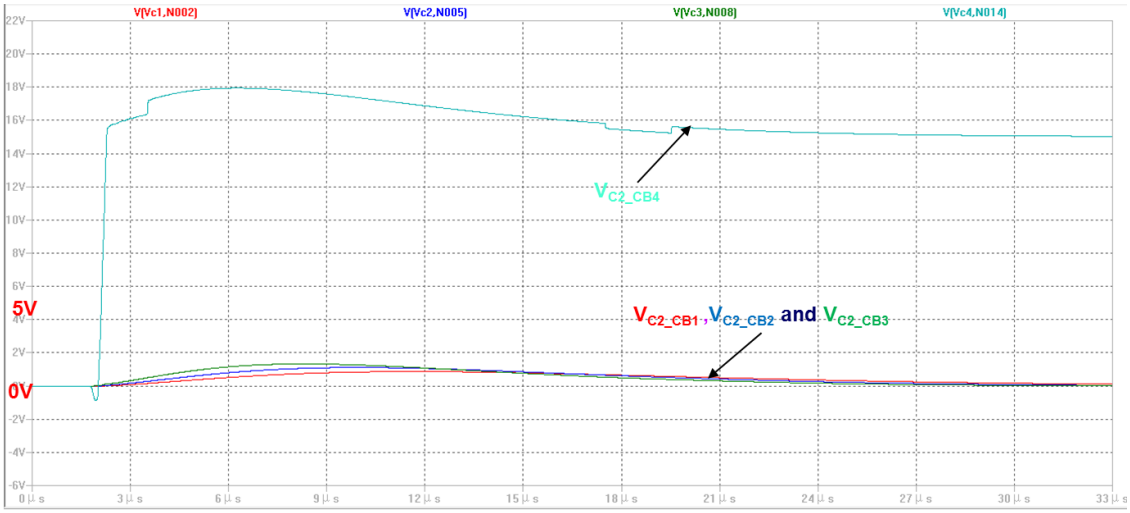

Figure 4-17 V_{C2} of all 5 SSCBs in scenario B

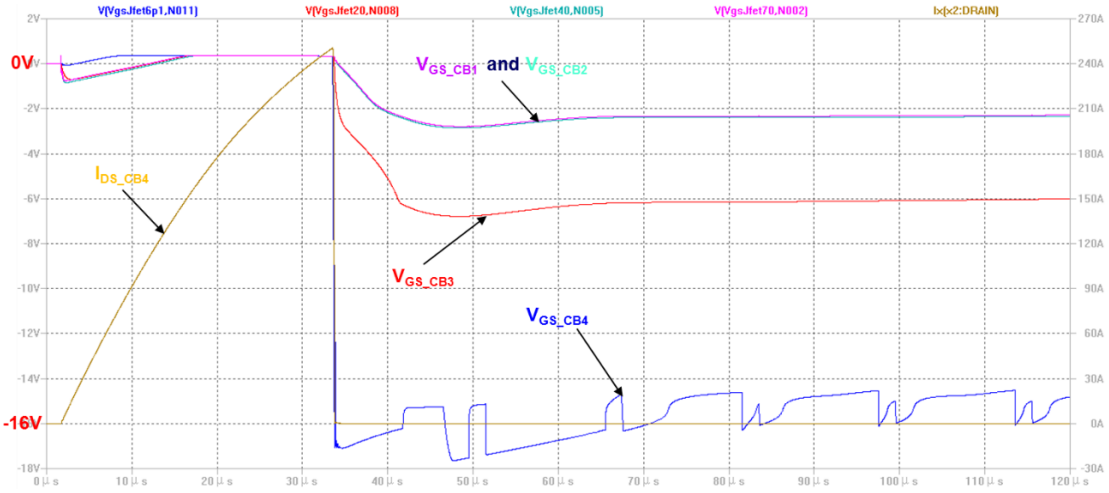

Figure 4-18 V_{GS} of all 5 SSCBs in scenario B

Next picture shows the voltages across the SSCBs. In Figure 4-19, you can see there is a high pulse about 1.6kV on CB4. The reason for this high pulse is discussed before, which is brought by the line inductance and short of effective MOV model in LTspice. After a very short time of high voltage, the V_{CB4} comes back to 400V and voltages of the other SSCBs are going back to zero after the SiC JFET turns off. So, CB4 clear the fault happens at house feed correctly.

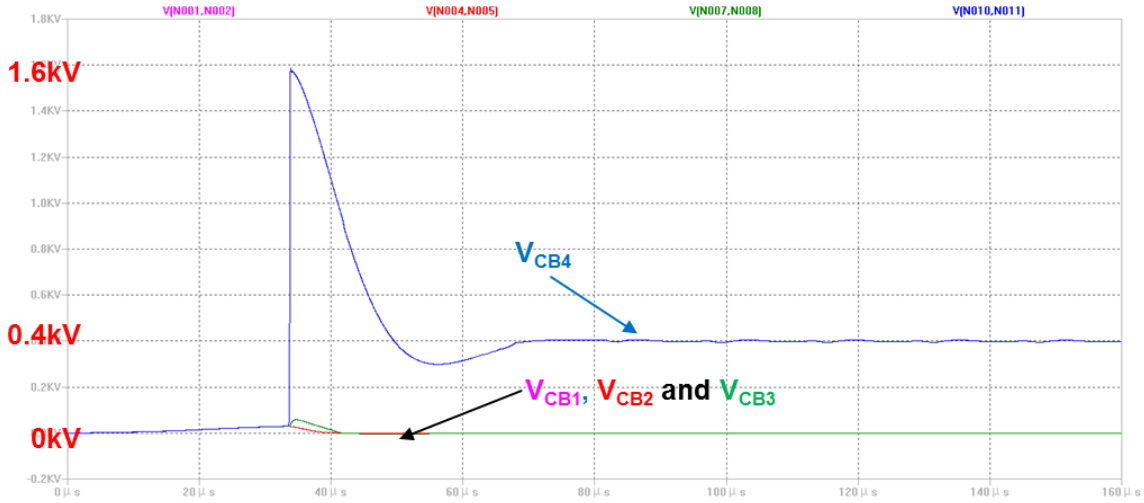

Figure 4-19 The voltage drop on SSCBs in scenario B

4.3.4 Fault Scenario C

In scenario C, the fault location is garage. In this case, it is the CB3 to clear the fault to avoid unnecessary loss of power supply. The LTspice simulation circuit of scenario C is exhibited in Figure 4-20.

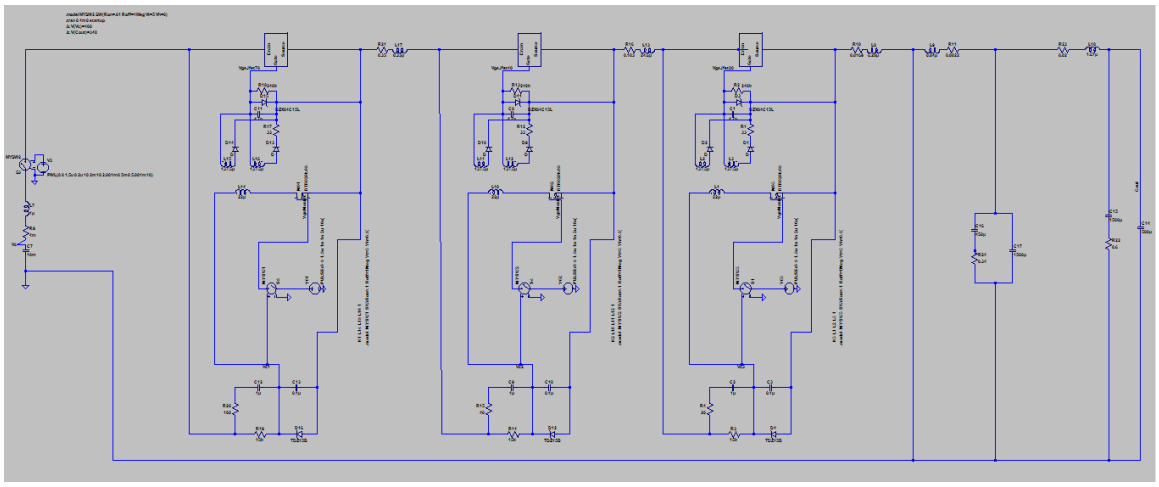

Figure 4-20 The simulation circuit of scenario C in LTspice

In Figure 4-21 to Figure 4-23, the traces for V_{C2}, V_{GS}, I_{DS} and V_{CB} has been shown just like scenario A and scenario B. It could be implied from the traces that CB3 turns off and clear the short circuit fault.

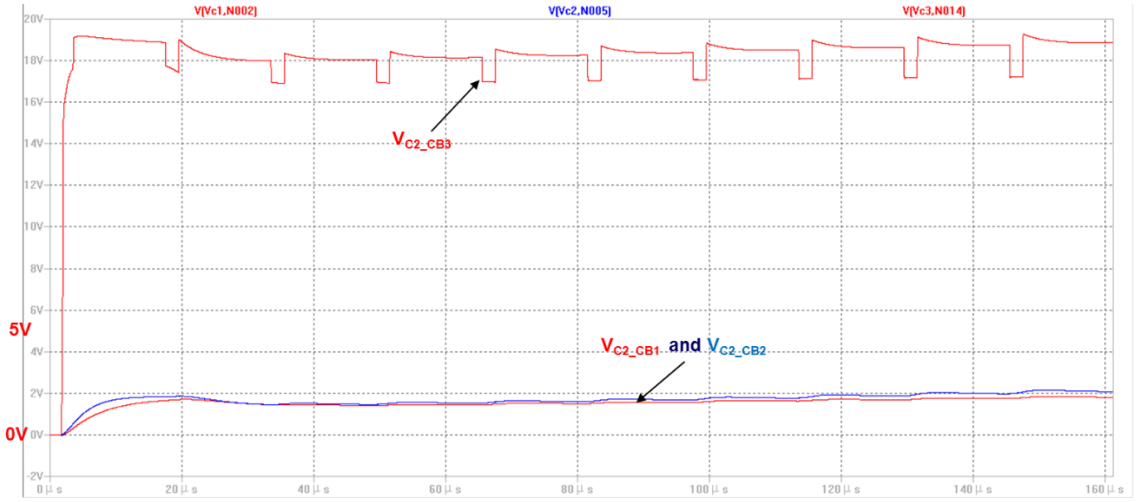

Figure 4-21 V_{C2} of all 5 SSCBs in scenario C

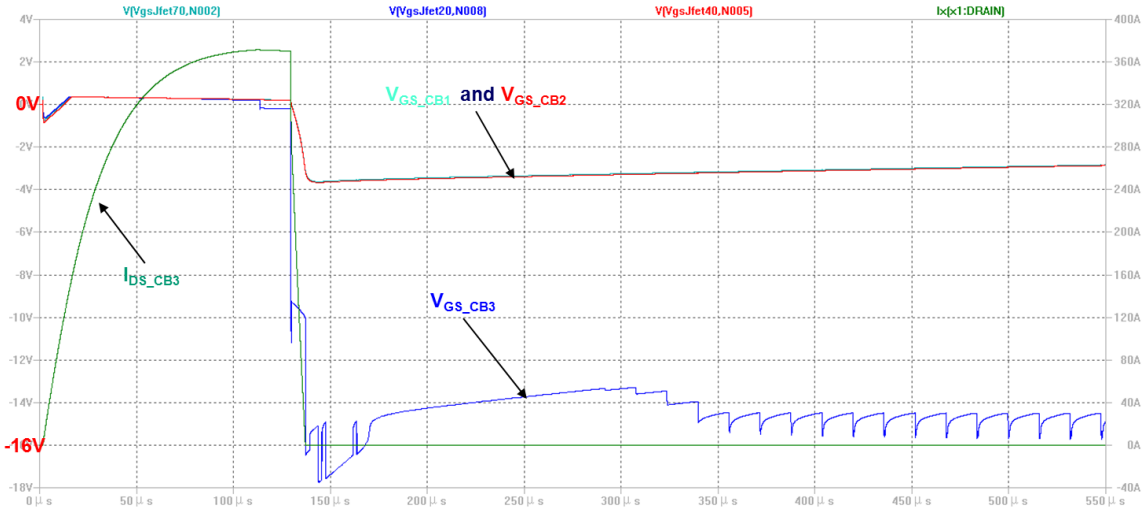

Figure 4-22 V_{GS} of all 5 SSCBs in scenario C

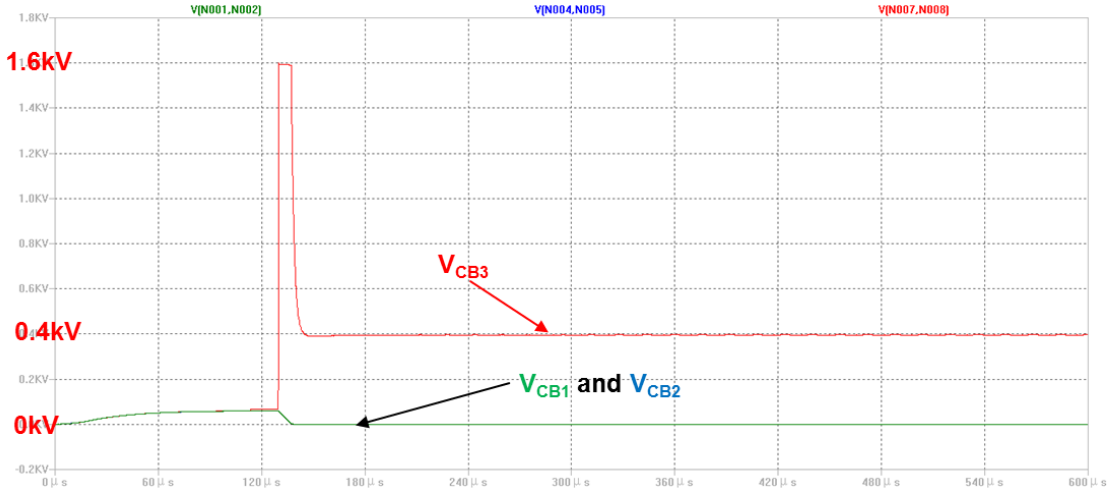

Figure 4-23 The voltage drop on SSCBs in scenario C

4.3.5 Fault Scenario D

In scenario D, the fault location is residence feed. CB2 is going to clear the fault in this case. The LTspice simulation circuit of scenario D is shown in Figure 4-24.

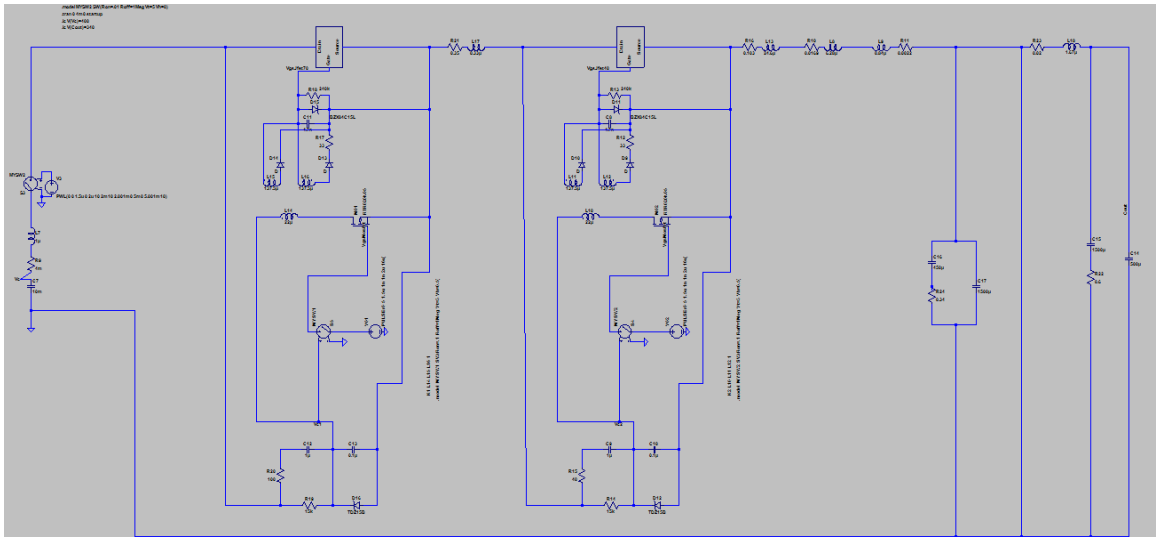

Figure 4-24 The simulation circuit of scenario D in LTspice

In Figure 4-25 to Figure 4-27, the traces for V_{C2}, V_{GS}, I_{DS} and V_{CB} has been shown just like scenario A, scenario B and scenario C. It could be implied from these traces that CB2 turns off and clear the short circuit fault as we expected.

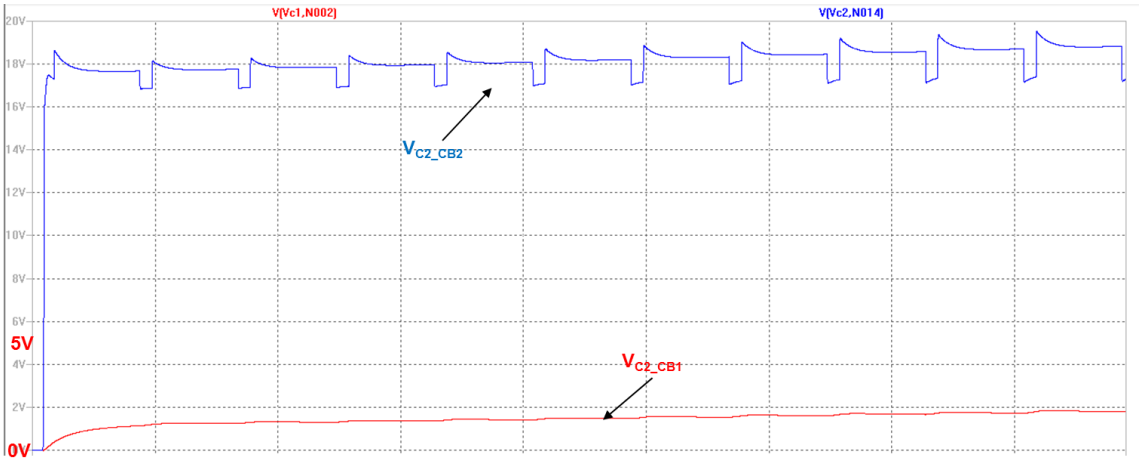

Figure 4-25 V_{C2} of all 5 SSCBs in scenario D

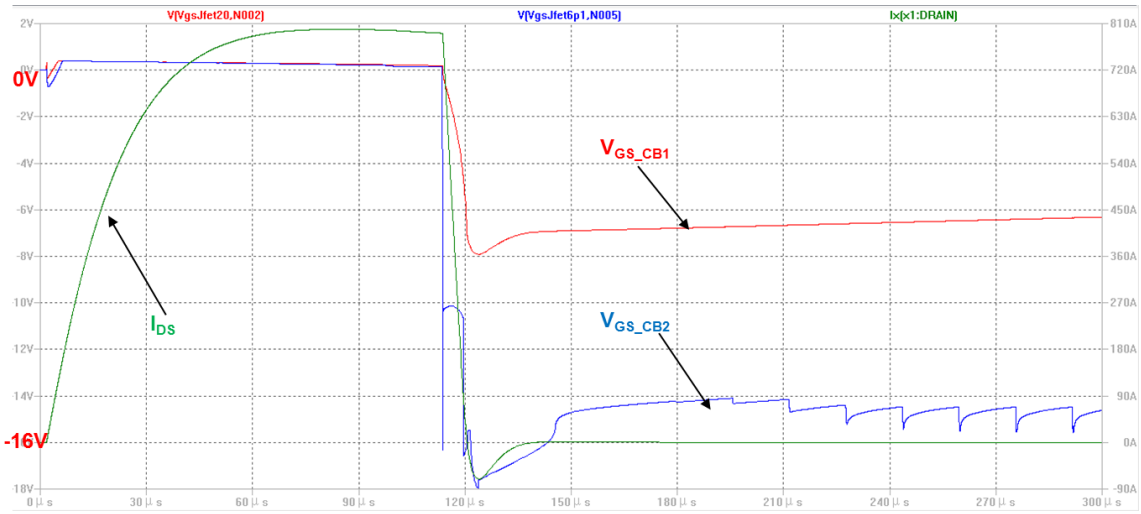

Figure 4-26 V_{GS} of all 5 SSCBs in scenario D

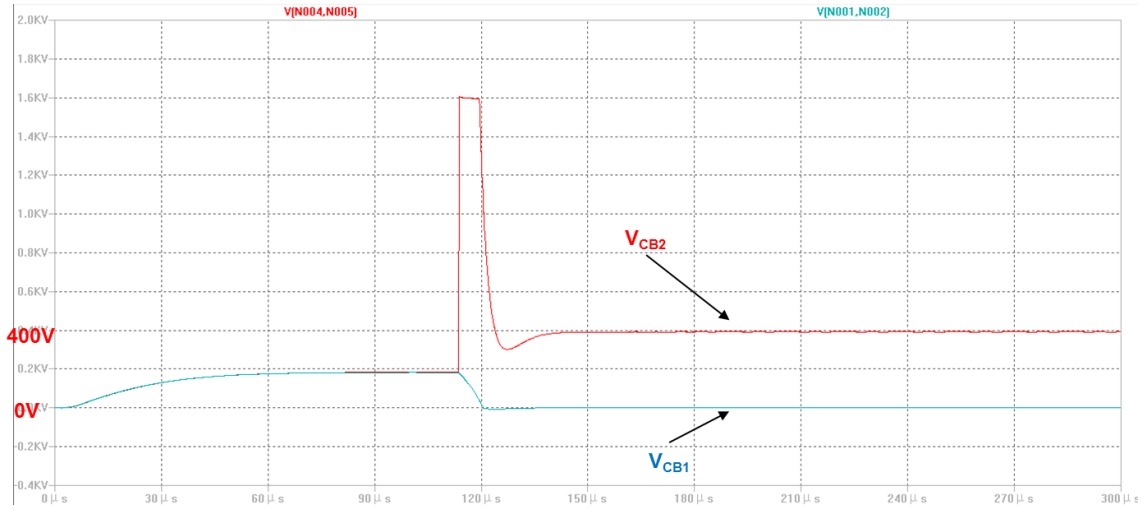

Figure 4-27 The voltage drop on SSCBs in scenario D

4.3.6 Fault Scenario E

In scenario E, it basically only one SSCB which is CB1 working in the system. Because the effectiveness of the proposed SSCB already been studied in previous section, the simulation results for scenario E are not shown in this chapter.

4.4 Simulation Results in PLECS

4.4.1 System Layout in PLECS

In Figure 4-28 and Figure 4-2, it shows the overview of the system and simplified SSCB model built in PLECS.

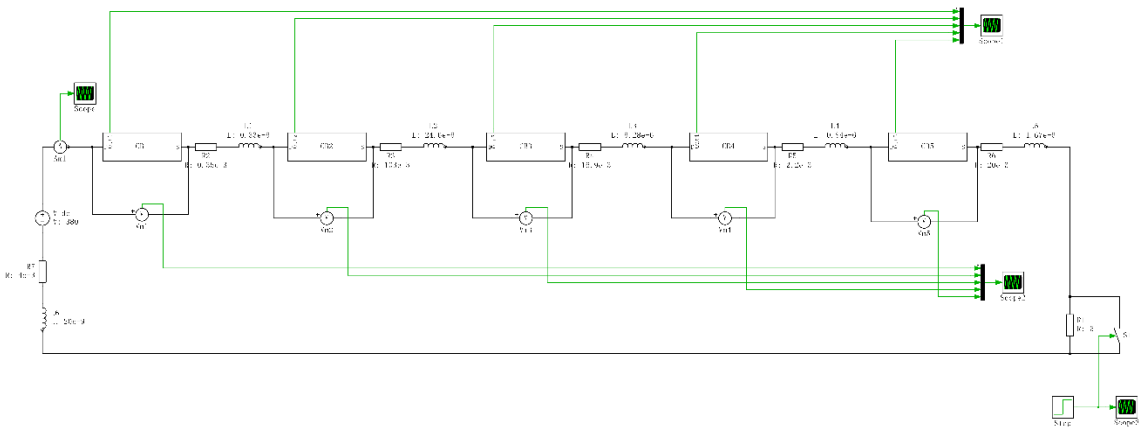

Figure 4-28 The overview of simulation model in PLECS

The SSCB model in PLECS has been simplified to an ideal IGBT with 45mΩ conduction resistance, a transfer function and a transport delay. Some statements about the simulation model have been made as following.

First, the main reason for repeating this simulation in PLECS is to bring this SSCB model into the whole DC community microgrid system which is built in PLECS. And PLECS also has the MOV model that can be modeling by mathematical equations to protect the SiC JFET.

Second, in PLECS, there is no JFET model so an ideal IGBT with conduction resistor has been chosen to replace the SiC JFET used in SSCB. The conduction resistor is used to sensor the voltage drop during the short circuit fault.

Third, in order to reduce the calculation time of simulation, a transfer function (shown in Equation 3-9) is derived previously and a transport delay has been used to simplified the gate driver of SiC JFET.

Last, the explanations for the model in PLECS will not be as detailed as in LTspice because the works are basically the same.

4.4.2 Fault Scenario A

In Figure 4-29, it shows the system model built in PLECS for scenario A. The short circuit fault is happening at home inverter. The simplified SSCB in Figure 4-2 is built into the subsystem.

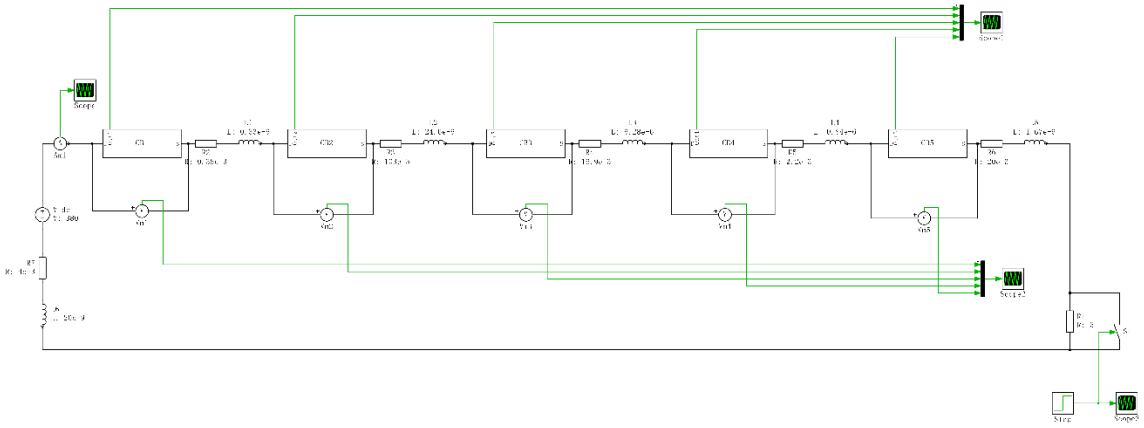

Figure 4-29 The simulation circuit for scenario A in PLECS

In Figure 4-30 and Figure 4-31, the voltages of all SSCBs V_{CB} and the voltages across C2 V_{C2} has been shown. The voltage from DC source is been applied between CB5 meaning that CB5 turns off and discriminate the fault. Furthermore, as shown in the picture, V_{CB} of CB5 has been successfully limited by MOV to 800V.

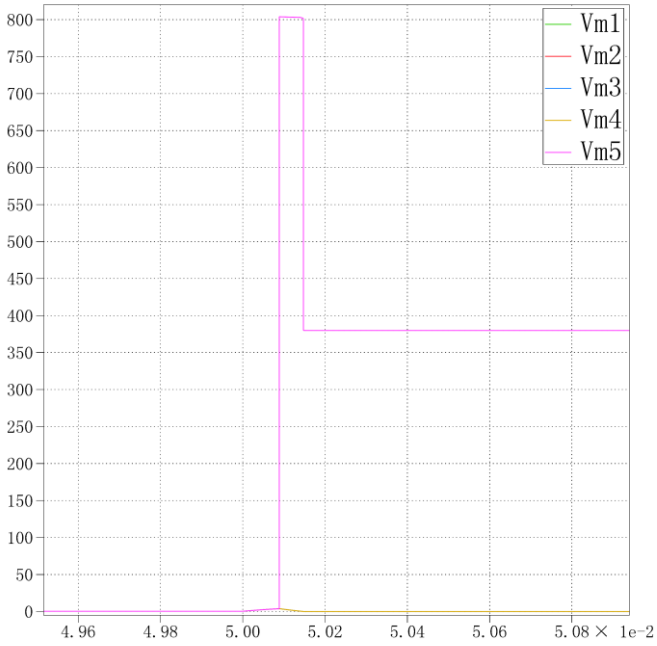

Figure 4-30 The V_{CB} of all SSCBs in scenario A

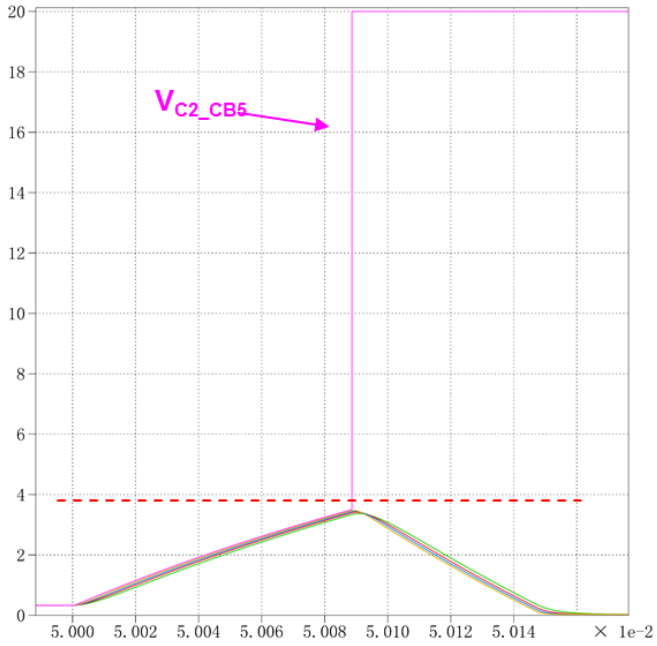

Figure 4-31 The V_{C2} of all SSCBs in scenario A

4.4.3 Fault Scenario B

In Figure 4-32, it shows the system model built in PLECS for scenario B. The short circuit fault is happening at house feed.

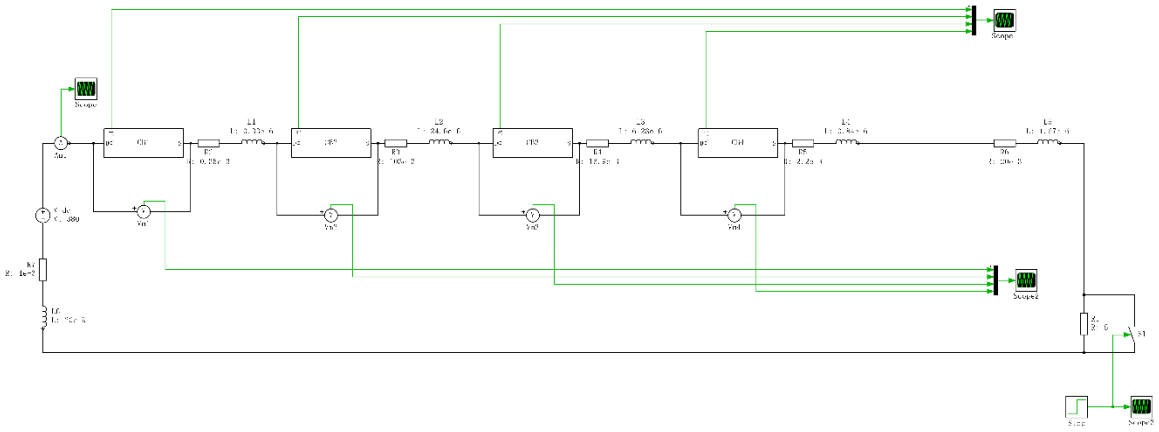

Figure 4-32 The simulation circuit for scenario B in PLECS

In Figure 4-33 and Figure 4-34, the voltages of all SSCBs V_{CB} and the voltages C2 V_{C2} has been shown. The voltage from DC source is been applied between CB4 meaning that CB4 turns off and discriminate the fault after house feed.

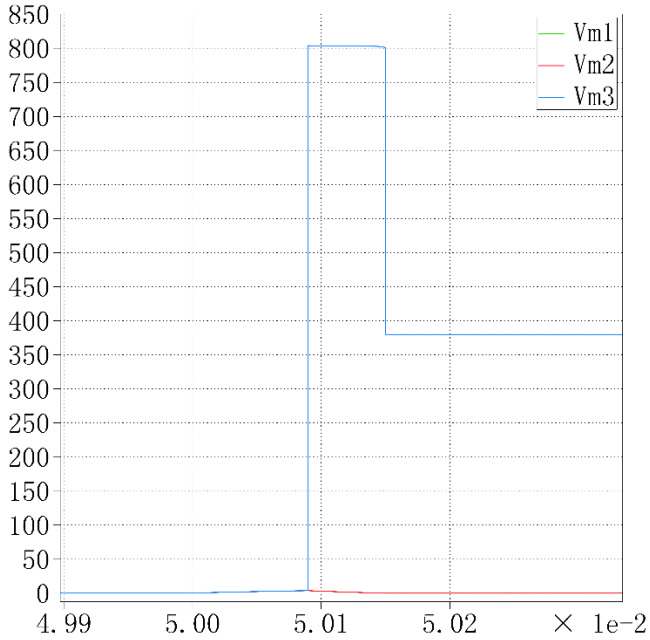

Figure 4-33 The V_{CB} of all SSCBs in scenario B

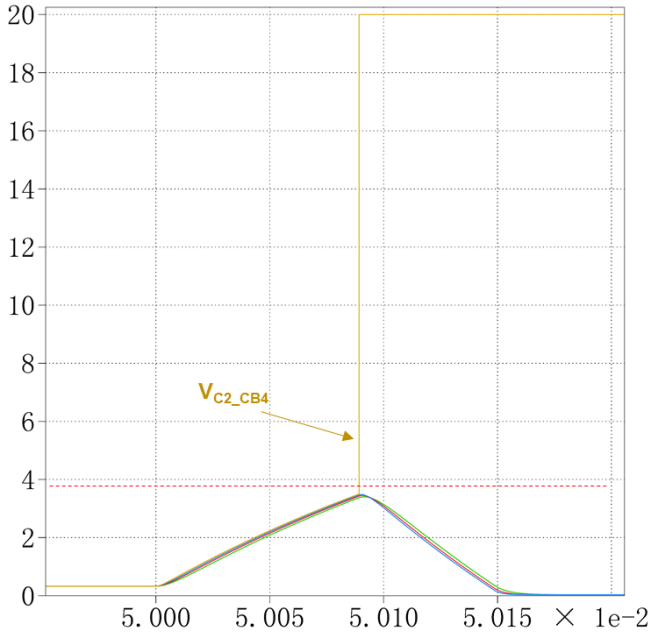

Figure 4-34 The V_{C2} of all SSCBs in scenario B

4.4.4 Fault Scenario C

In Figure 4-35, it shows the system model built in PLECS for scenario C. The short circuit fault is happening at garage feed.

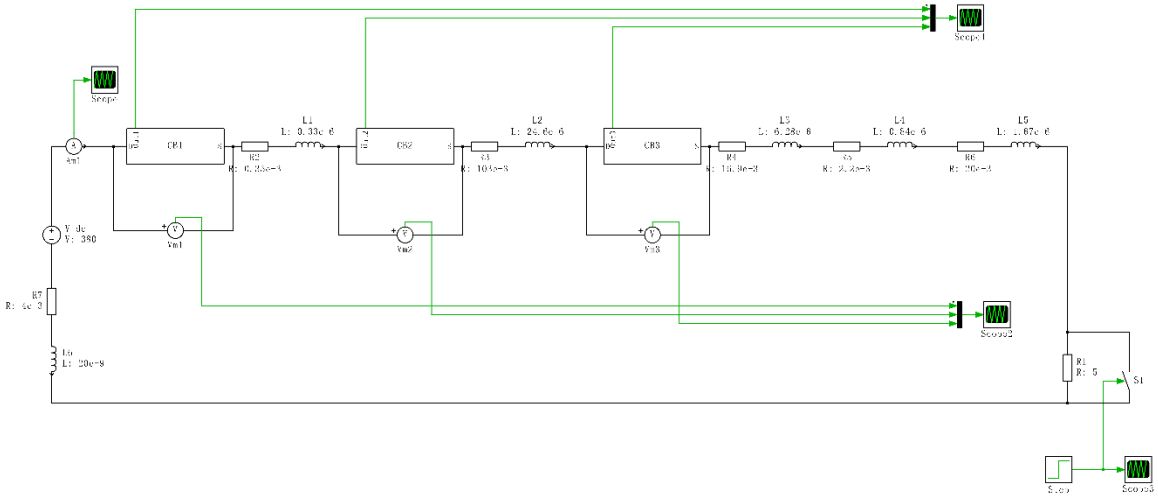

Figure 4-35 The simulation circuit for scenario C in PLECS

In Figure 4-36 and Figure 4-37, the voltages of all SSCBs V_{CB} and the voltages C2 V_{C2} has been shown. The voltage from DC source is been applied between CB3 meaning that CB3 turns off and discriminate the fault after garage feed.

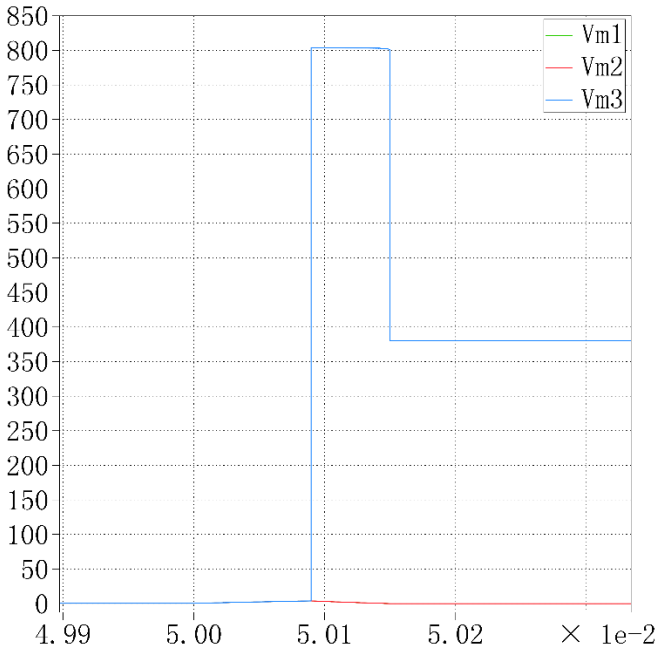

Figure 4-36 The V_{CB} of all SSCBs in scenario C

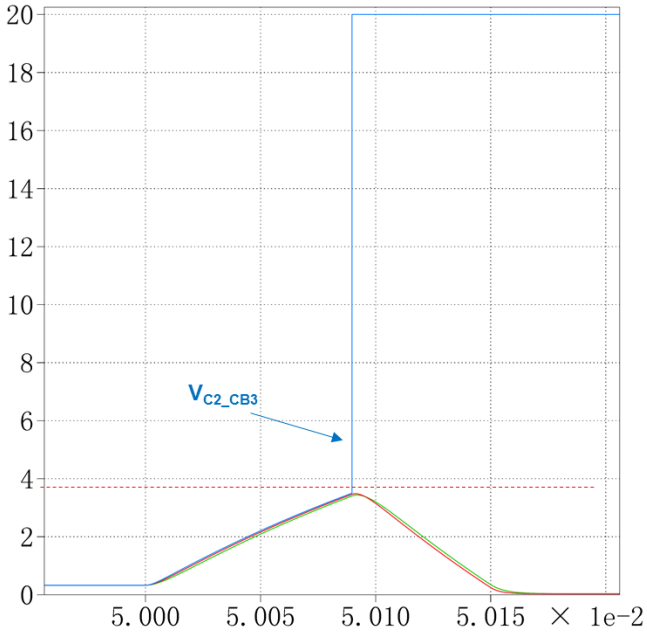

Figure 4-37 The V_{C2} of all SSCBs in scenario C

4.4.5 Fault Scenario D

In Figure 4-38, it shows the system model built in PLECS for scenario D. The short circuit fault is happening at residence feed.

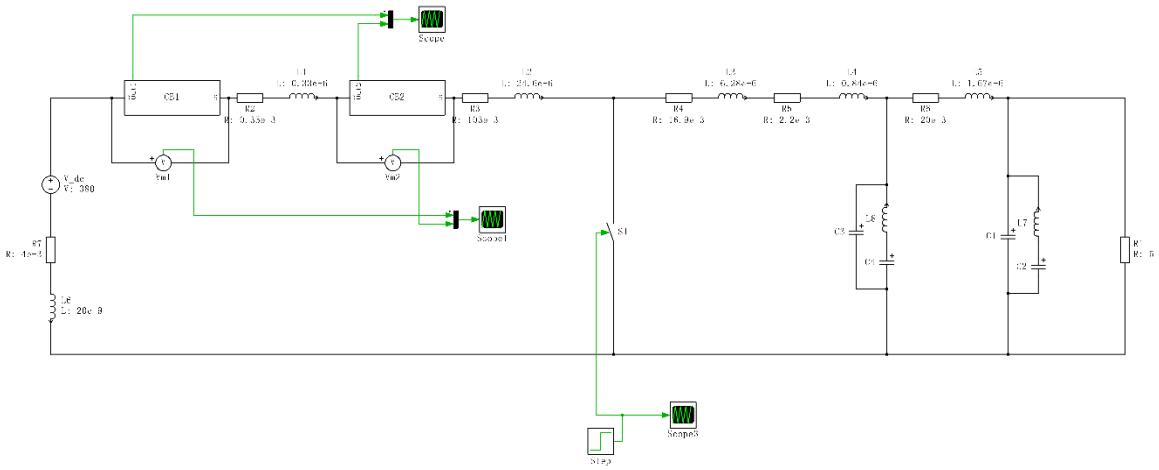

Figure 4-38 The simulation circuit for scenario D in PLECS

In Figure 4-39 and Figure 4-40, the voltages of all SSCBs V_{CB} and the voltages C2 V_{C2} has been shown. The voltage from DC source is been applied between CB2 meaning that CB2 turns off and discriminate the fault after residence feed.

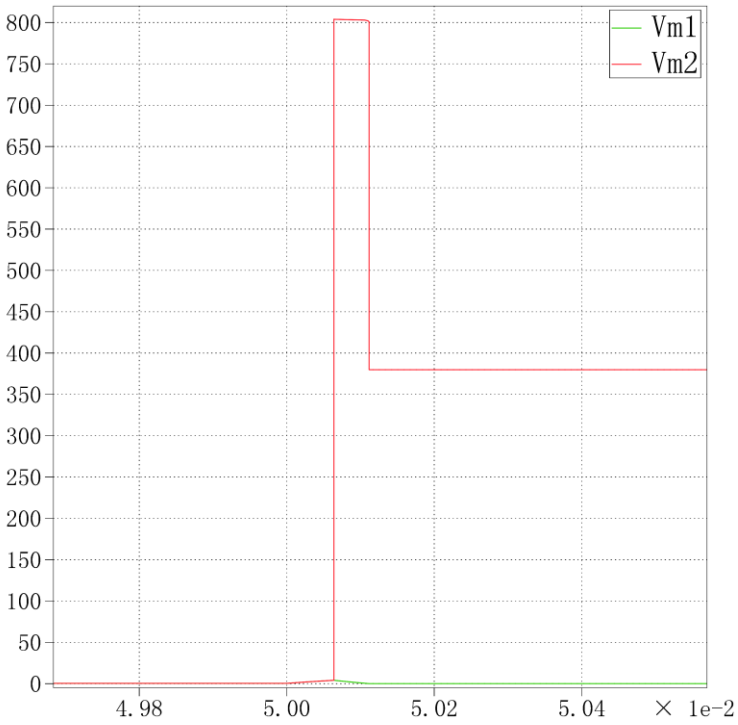

Figure 4-39 The V_{CB} of all SSCBs in scenario D

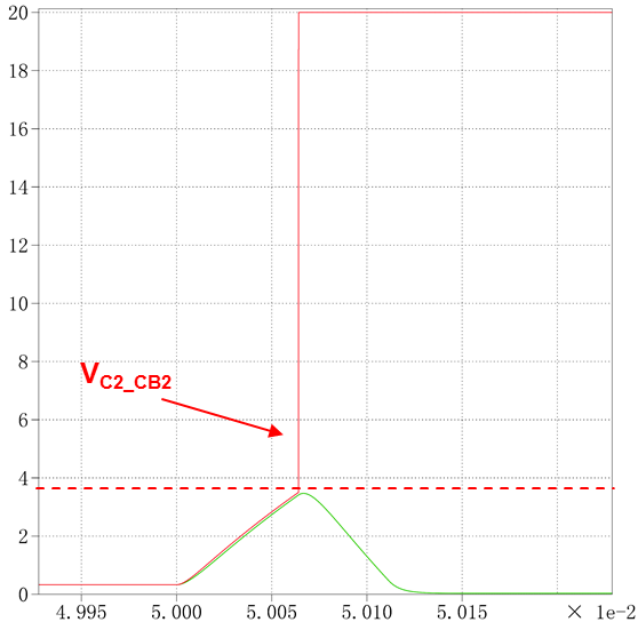

Figure 4-40 The V_{C2} of all SSCBs in scenario D

4.5 Summary

In this chapter, Section 4.3 discusses the simulation in LTspice under 5 different fault scenarios and Section 4.4 mainly talk about the same simulation been handled with PLECS. The simulation results from both software are verified the analytical work did in the previous chapters and prove that the changing of “R2” in proposed SSCB will successfully achieve the coordination between upstream and downstream devices in a DC community microgrid.

Chapter 5 Conclusion and Future Work

5.1 Conclusion

In this thesis, an ultra-fast normally-on SiC JFET based SSCB has been introduced. Then the basic working principles of the proposed SSCB has been illustrated in detail. The performance of that SSCB has been proved to be perfect for the overcurrent protection for DC system.

Next it analytically verifies the effectiveness protective device coordination to discriminate fault locations and to isolate faults in radial distribution systems with a little change in the design of proposed SSCB.

Finally, simulation models have been built in both LTspice IV and PLECS software. The simulation results prove the correction of previous theoretical coordination scheme and verify the implementation of SSCBs is suitable for the protection of DC system.

5.2 Future Work

More SSCB prototypes will be built to experimentally verify the proposed coordination.

A crowbar circuit can be added to the packaged SSCB assembly in order to enable a shunt trip mechanism.

A viable sensing and monitoring system to handle different types of faults and simple ladder relay logic circuitry that can be incorporated into the packaged SSCB.

References

[1] Wunder, B., Ott, L., Kaiser, J., Han, Y., Fersterra, F., & März, M. (2015, June). Overview of different topologies and control strategies for DC micro grids. In *DC Microgrids (ICDCM), 2015 IEEE First International Conference on* (pp. 349-354). IEEE.

[2] Sirsi, R., Prasad, S., Sonawane, A., & Lokhande, A. (2016, April). Efficiency comparison of AC distribution system and DC distribution system in microgrid. In *Energy Efficient Technologies for Sustainability (ICEETS), 2016 International Conference on* (pp. 325-329). IEEE.

[3] Manandhar, U., Ukil, A., & Jonathan, T. K. K. (2015, November). Efficiency comparison of DC and AC microgrid. In *Innovative Smart Grid Technologies-Asia (ISGT ASIA), 2015 IEEE* (pp. 1-6). IEEE.

[4] Nejabatkhah, F., & Li, Y. W. (2015). Overview of power management strategies of hybrid AC/DC microgrid. *IEEE Transactions on Power Electronics*, *30*(12), 7072-7089.

[5] Lonkar, M., & Ponnaluri, S. (2015, March). An overview of dc microgrid operation and control. In *Renewable Energy Congress (IREC), 2015 6th International* (pp. 1-6). IEEE.

[6] Dragičević, T., Lu, X., Vasquez, J. C., & Guerrero, J. M. (2016). DC Microgrids—Part II: A review of power architectures, applications, and standardization issues. *IEEE transactions on power electronics*, *31*(5), 3528-3549.

[7] Mane, S., Kadam, P., Lahoti, G., Kazi, F., & Singh, N. M. (2016, November). Optimal load balancing strategy for hybrid energy management system in DC microgrid with PV, fuel cell and battery storage. In *Renewable Energy Research and Applications (ICRERA), 2016 IEEE International Conference on* (pp. 851-856). IEEE.

[8] Che, L., Shahidehpour, M., Alabdulwahab, A., & Al-Turki, Y. (2015). Hierarchical coordination of a community microgrid with AC and DC microgrids. *IEEE Transactions on smart grid*, *6*(6), 3042-3051.

[9] Davies, R., Sumner, M., & Christopher, E. (2014). Energy storage control for a small community microgrid.

[10] Magdefrau, D., Taufik, T., Poshtan, M., & Muscarella, M. (2016, August). Analysis and review of DC microgrid implementations. In *Technology of Information and Communication (ISemantic), International Seminar on Application for* (pp. 241-246). IEEE.

[11] Cuzner, R. M., & Venkataramanan, G. (2008, October). The status of DC micro-grid protection. In *Industry Applications Society Annual Meeting, 2008. IAS'08. IEEE* (pp. 1-8). IEEE.

[12] Shen, Z. J., Roshandeh, A. M., Miao, Z., & Sabui, G. (2015, June). Ultrafast autonomous solid state circuit breakers for shipboard DC power distribution. In *Electric Ship Technologies Symposium (ESTS), 2015 IEEE* (pp. 299-305). IEEE.

[13] Sato, Y., Tanaka, Y., Fukui, A., Yamasaki, M., & Ohashi, H. (2014). SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems. *IEEE Transactions on Power Electronics*, *29*(5), 2597-2605.

[14] Handt, K., Griepentrog, G., & Maier, R. (2008, June). Intelligent, compact and robust semiconductor circuit breaker based on silicon carbide devices. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* (pp. 1586-1591). IEEE.

[15] Shen, Z. J., Miao, Z., Roshandeh, A. M., Moens, P., Devleeschouwer, H., Salih, A., ... & Jeon, W. (2016, June). First experimental demonstration of solid state circuit breaker (SSCB) using 650V GaN-based monolithic bidirectional switch. In *Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on* (pp. 79-82). IEEE.

[16] Hudgins, J. L., Simin, G. S., Santi, E., & Khan, M. A. (2003). An assessment of wide bandgap semiconductors for power devices. *IEEE Transactions on Power Electronics*, *18*(3), 907-914.

[17] Moutis, P., Skarvelis-Kazakos, S., Brucoli, M., Hung, J., & Wu, S. W. (2014, October). Planned communities as microgrid applications. In *Innovative Smart Grid Technologies Conference Europe (ISGT-Europe), 2014 IEEE PES* (pp. 1-7). IEEE.

[18] Jiao, Q., Hosseini, R., & Cuzner, R. M. (2016, November). A comparison between silicon carbide based current source rectifier and voltage source rectifier for applications in community DC microgrid. In *Renewable Energy Research and Applications (ICRERA), 2016 IEEE International Conference on* (pp. 544-549). IEEE.

[19] Ferrer, H. J. A., & Schweitzer, E. O. (Eds.). (2010). *Modern Solutions for Protection, Control, and Monitoring of Electric Power Systems*. Schweitzer Engineering Laboratories.

[20] Cuzner, R. M., Palaniappan, K., & Shen, Z. J. (2015, November). System specification for a DC community microgrid and living laboratory embedded in an urban environment. In *Renewable Energy Research and Applications (ICRERA), 2015 International Conference on* (pp. 1119-1125). IEEE.

[21] Shen, Z. J., Sabui, G., Miao, Z., & Shuai, Z. (2015). Wide-bandgap solid-state circuit breakers for DC power systems: Device and circuit considerations. *IEEE Transactions on Electron Devices*, *62*(2), 294-300.

[22] Miao, Z., Sabui, G., Chen, A., Li, Y., Shen, Z. J., Wang, J., ... & Jiang, M. (2015, March). A self-powered ultra-fast DC solid state circuit breaker using a normally-on SiC JFET. In *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE* (pp. 767-773). IEEE.

[23] United Silicon Carbide, Inc. Product Datasheet [Online]. Available: http://www.unitedsic.com/uploads/UJN1205K.pdf

[24] Huang, Z., Ma, J., Zeng, J., Gao, Y., Yuan, Z., Hu, Z., ... & Liu, G. (2014, September). Research status and prospect of control and protection technology for DC distribution network. In *Electricity Distribution (CICED), 2014 China International Conference on* (pp. 1488-1493). IEEE.

[25] Beheshtaein, S., Savaghebi, M., Vasquez, J. C., & Guerrero, J. M. (2015, November). Protection of AC and DC microgrids: Challenges, solutions and future trends. In *Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE* (pp. 005253-005260). IEEE.

[26] Satpathi, K., & Ukil, A. (2015, June). Protection strategies for lvdc distribution system. In *PowerTech, 2015 IEEE Eindhoven* (pp. 1-6). IEEE.

[27] Shen, Z. J., Miao, Z., & Roshandeh, A. M. (2015, June). Solid state circuit breakers for DC micrgrids: Current status and future trends. In *DC Microgrids (ICDCM), 2015 IEEE First International Conference on* (pp. 228-233). IEEE.

[28] Salomonsson, D., Soder, L., & Sannino, A. (2009). Protection of low-voltage DC microgrids. *IEEE Transactions on Power Delivery*, *24*(3), 1045-1053.

[29] Meghwani, A., Chakrabarti, S., & Srivastava, S. C. (2016, December). A fast scheme for fault detection in DC microgrid based on voltage prediction. In *Power Systems Conference (NPSC), 2016 National* (pp. 1-6). IEEE.

[30] Texas Instruments, Inc. Product Datasheet [Online]. Available: http://www.ti.com/product/tl494