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Theory, Simulation, and Implementation of Grid Connected Back to Back Converters Utilizing Voltage Oriented Control

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THEORY, SIMULATION, AND IMPLEMENTATION OF GRID CONNECTED BACK TO BACK CONVERTERS UTILIZING VOLTAGE ORIENTED CONTROL

by

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ABSTRACT

THEORY, SIMULATION, AND IMPLEMENTATION OF GRID CONNECTED BACK TO BACK CONVERTERS UTILIZING VOLTAGE ORIENTED CONTROL

by

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This work presents a back to back converter topology with the ability to connect two power systems of different voltages and frequencies for the exchange of power. By utilizing indirect AC/AC conversion decoupling is achieved between the power systems with one of the three-phase, two-level voltage source converters performing the AC/DC conversion that maintains the required DC bus voltage level at unity power factor while the other converter operates in all four quadrants supplying/consuming active and/or reactive power with the other power system. The prototype implementation resides at UW-Milwaukee's USR Building microgrid test bed facility. A possible application topology would be the converter that maintains the DC bus voltage to be connected to the microgrid's electrical bus of distributed energy sources while the other converter is connected to the utility in order to supply the required active and/or reactive power to support the needs of the grid.

To

my parents

and sister

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
VOC	Voltage Oriented Control
DSP	Digital Signal Processor
GP-DSP	General-Purpose Digital Signal Processor
GPIO	General-Purpose Inputs/Outputs
SVM	Space Vector Modulation
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
FFT	Fast Fourier Transform
DFT	Discrete Fourier Transform
VAC	Volts Alternating Current
VSC	Voltage Source Converter
DC	Direct Current
AC	Alternating Current
RMS	Root Mean Square
IGBT	Insulated Gate Bipolar Transistor
IIR	Infinite Impulse Response
FIR	Finite Impulse Response
PI	Proportional Integral
PU	Per-Unit
MFB	Multiple Feedback

LIST OF SYMBOLS

Abbreviation	*Variable*	*Unit*
C_{dc}	DC Capacitance	farad
$G_{cc,CL}$	Current Controller Closed Loop Transfer Function	
$G_{cc,OL}$	Current Controller Open Loop Transfer Function	
$G_{vc,CL}$	Voltage Controller Closed Loop Transfer Function	
$G_{vc,OL}$	Voltage Controller Open Loop Transfer Function	
$G_{converter}$	Converter Transfer Function	
$G_{feedback,i}$	Current Anti-Aliasing Filter Transfer Function	
$G_{feedback,v}$	Voltage Digital Low Pass Filter Transfer Function	
G_{pi}	Proportional Integral Controller Transfer Function	
$G_{system,C}$	System Capacitance Transfer Function	
$G_{system,L}$	System Inductance Transfer Function	
i_g	Instantaneous Grid Current	amp
K_{conv}	Converter Gain	
$K_{i,c}$	Current Controller Integrator Gain	
$K_{i,v}$	Voltage Controller Integrator Gain	
$K_{p,c}$	Current Controller Proportional Gain	
$K_{p,v}$	Voltage Controller Proportional Gain	
L	Grid Inductance	henry
m_a	Modulation Index	

P_g	Grid Active Power	watt
Q_g	Grid Reactive Power	VAR
R	Grid Resistance	ohm
T_a	Sum of Minor Current Controller Delays	sec
T_b	Sum of Minor Voltage Controller Delays	sec
T_{aaf}	Current Anti-Aliasing Filter Time Constant	sec
T_d	Sum of Processing Delay and PWM	sec
$T_{i,c}$	Current Controller Integral Time Constant	sec
$T_{i,v}$	Voltage Controller Integral Time Constant	sec
T_L	Reactor Time Constant	sec
T_{mp}	Processing Delay of Computational Device	sec
T_{PWM}	Delay of PWM Converter	sec
T_s	Computational Device Sample Time	sec
v_c	Instantaneous Converter Voltage	volt
V_{dc}	DC Bus Voltage	volt
v_g	Instantaneous Grid Voltage	volt
θ_g	Grid Voltage Angle	rad
ω_n	Undamped Natural Frequency	rad/sec
ζ	Damping Ratio	

1. Introduction

The purpose of this project is to connect two power systems of different voltages and frequencies for the exchange of power. An example of such an implementation could be the electric utility and a microgrid. The thesis project implementation resides at UW-Milwaukee's USR Building microgrid test bed facility. With indirect AC/AC conversion between the two power systems there is a DC bus that connects two converters that perform the AC/DC and DC/AC conversions. The benefit of indirect AC/AC conversion is the decoupling between the power systems while the disadvantage is the requirement of energy storage devices needed in the DC bus [1, p. 128]. One of the three-phase, two-level voltage source converters performing the AC/DC conversion maintains the required DC bus voltage level at unity power factor for the power system. The other two-level converter operates in all four quadrants supplying/consuming active and/or reactive power with the other power system. The designation of the converter type for the utility and microgrid is application specific. A possible topology would be the converter that maintains the DC bus voltage to be connected to microgrid's electrical bus of distributed energy sources while the other converter is connected to the utility in order to supply the required active and/or reactive power to support the needs of the grid.

2. Background and System Architecture

The AC/DC conversion that occurs between the power system and the two-level voltage source converter can be modeled as two AC voltage sources in Figure 1 by omitting the voltage harmonics produced by the converter other than the fundamental frequency of the power system. The amount and direction of active and reactive power can be controlled between two voltage sources by controlling the amplitude and phase angle of the voltage drop across the reactor. The leading voltage source will supply active power while the higher amplitude voltage source will supply reactive power [2, pp. 184-185].

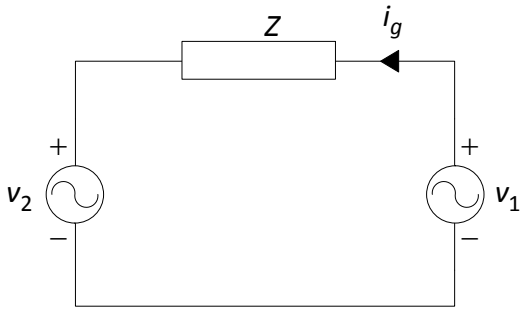

Figure 1 - Single-Phase Representation of Complex Power Flow

The converter operates in rectifier mode of operation when active power is supplied from the power system to the DC bus. By supplying active power from the power system to the DC bus the capacitor is charged and the DC bus voltage increases functioning like a boost converter. The converter operates in inverter mode of operation when power is supplied from the DC bus into the power system. By supplying power from the DC Bus to the power system the capacitor is discharged and the DC bus voltage decreases functioning like a buck converter [3, p. 225].

The "PQ" converter supplies/consumes active and/or reactive power by the use of open loop control by commanding the desired active and reactive power references. The "VDC" converter maintains the DC bus voltage with the use of a feedback control loop referred to as the voltage controller which measures the difference between the desired DC bus voltage and the voltage measured across the capacitors of the DC bus. In addition to the "VDC" converter controlling the direction of active power, unity power factor of the power system is also achieved by controlling the reactive power.

2.1. Space Vector Modulation

The linear region of sinusoidal PWM that can be achieved at the output of the converter for a modulation index when $m_a \leq 1$ would not allow the converter to deliver reactive power to the grid without going into overmodulation, the nonlinear region of sinusoidal PWM, unless the DC Bus level was raised to a substantially high level. Higher DC bus levels increase the stress on the converter's IGBTs due to the increase in the switching losses, so it is advantageous to keep the DC Bus voltage level as low as practicable [1, p. 348]. Operation in the overmodulation region of sinusoidal PWM is undesirable since it causes an increase in the sideband harmonics generated by PWM [4, p. 208] as well as the introduction of nonlinearity into the current controller [1, p. 336]. Double-edge symmetrical regular sampled space vector modulation was chosen so the converter operates in the linear region when reactive power is desired to be delivered from the converter to the grid making the best utilization of the DC Bus.

$$\begin{aligned} \textit{SPWM Converter Output Fundamental Line Voltage} &= \left(\frac{\sqrt{3}}{\sqrt{2}}\right)\left(m_a \frac{V_{dc}}{2}\right)[\textit{volts rms}] \\ &\approx 0.612 m_a V_{dc} \;\because m_a \leq 1.0 \end{aligned} \tag{1}$$

$$\begin{aligned} \textit{SVM Converter Output Fundamental Line Voltage} &= \left(\frac{\sqrt{3}}{\sqrt{2}}\right)\left(m_a \frac{V_{dc}}{\sqrt{3}}\right)[\text{volts rms}] \\ &\approx 0.707 m_a V_{dc} \;\because m_a \leq 1.0 \end{aligned} \tag{2}$$

2.2. Vector Control

In order for the voltage source converter to consume or supply active and reactive power as needed a control scheme with high dynamic performance must be implemented for control. Vector control methods are based on the system dynamic model rather than scalar control methods which are based on the system steady-state model [3, p. 931].

2.2.1. Voltage Oriented Control and the System Dynamic Model

The vector control scheme selected is known as Voltage Oriented Control. VOC was chosen for simplicity in the selection of the input filter due to a fixed switching frequency. The disadvantage of this scheme is that it requires coordinate transformation from the three-phase stationary frame (known as *abc* or natural frame) to the synchronous frame (known as *dq*, direct-quadrature rotating frame), an internal current feedback loop (known as the current controller), as well as the decoupling between the active and reactive components [5, p. 457].

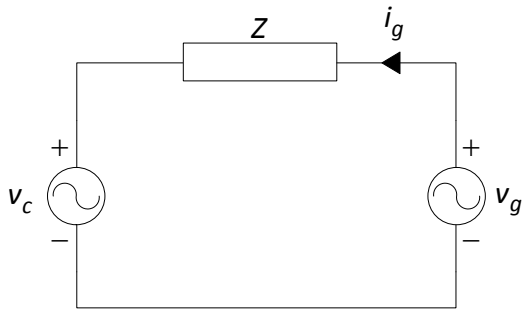

Figure 2 - One Line Diagram Representation of Converter, Impedance, and Grid

$$\begin{aligned} 0 &= v_g - v_Z - v_c \\ v_g - v_c &= v_R + v_L \end{aligned} \tag{3}$$

Figure 2 results from the substitution of an ideal voltage source converter in place of a voltage source from Figure 1. Equation (3) is the result of applying Kirchhoff's Voltage Law to Figure 2. Figure 3 is the representation of Figure 2 but represented in terms of resistance and inductance.

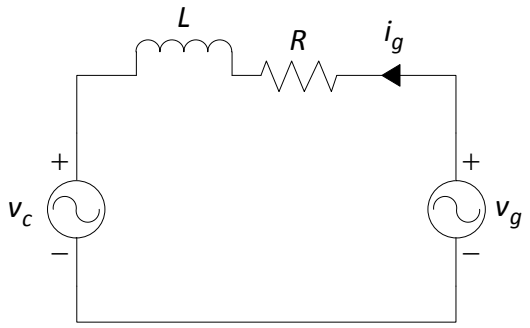

Figure 3 - One Line Diagram Representation of Converter, Impedance, and Grid

$$v_g - v_c = Ri_g + L\frac{di_g}{dt} \tag{4}$$

Equation(4) is the differential equation that represents Figure 3.

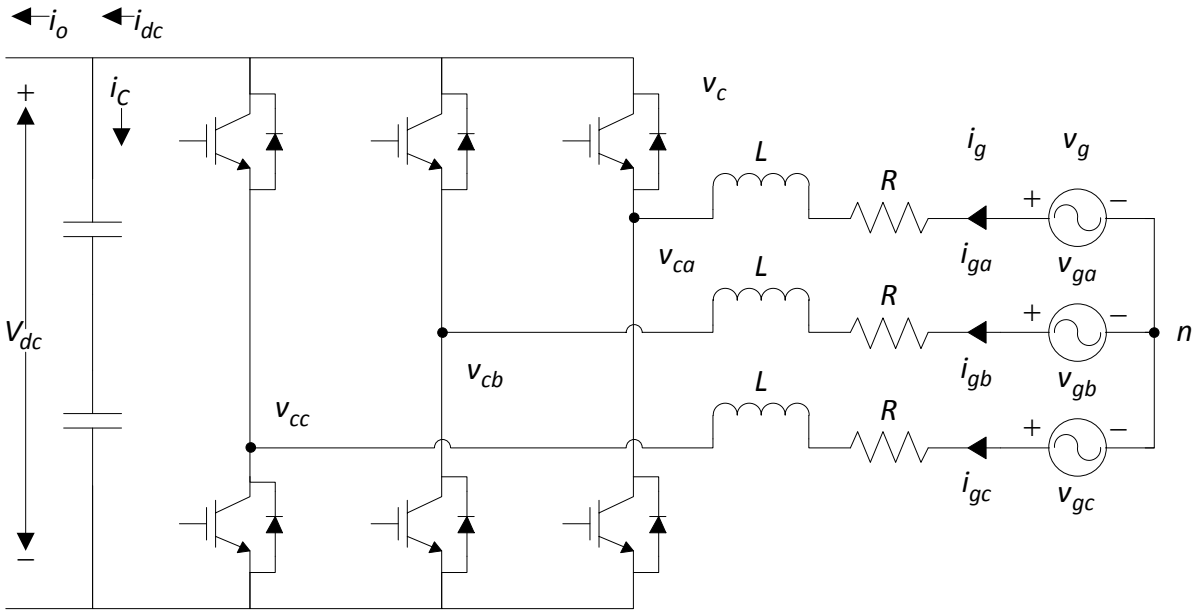

Figure 4 - Three-Phase Representation of Converter, Impedance, and Grid

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = R\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} \tag{5}$$

Equation(5) is the *abc* three-phase stationary frame representation of equation(4).

$$M_1\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - M_1\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = RM_1\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + L\frac{d}{dt}(M_1\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}) \tag{6}$$

$$\begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix} - \begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} = R\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} \tag{7}$$

Equations (6) and (7) are the result of the coordinate transformation from the *abc* three-phase stationary reference frame to the $\alpha\beta$ two-phase stationary reference frame. This is done by multiplying the voltages and currents by the matrix M_1 found in Appendix B: Coordinate Transformations.

$$M_2\begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix} - M_2\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} = RM_2\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} + LM_2\frac{d}{dt}\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} - \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = R\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} + L\omega\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} \tag{9}$$

Equations (8) and (9) are the result of the coordinate transformation from the $\alpha\beta$ two-phase stationary reference frame to the *dq* synchronous reference frame. The ωLi_g term is a result of the coordinate transformation due to the derivative term [6, p. 147] with the derivation found in Appendix B: Coordinate Transformations.

$$v_{gd} - v_{cd} = Ri_{gd} + L\frac{di_{gd}}{dt} - \omega Li_{gq} \tag{10}$$

$$v_{gq} - v_{cq} = Ri_{gq} + L\frac{di_{gq}}{dt} + \omega Li_{gd} \tag{11}$$

Equations (10) and (11) are the result of separating the *dq* synchronous reference frame equation into separate equations.

$$\frac{di_{gd}}{dt} = \left(v_{gd} - v_{cd} - Ri_{gd} + \omega Li_{gq}\right) / L \tag{12}$$

$$\frac{di_{gq}}{dt} = \left(v_{gq} - v_{cq} - Ri_{gq} - \omega Li_{gd}\right) / L \tag{13}$$

Rearrangement of equations (10) and (11) into equations (12) and (13) leads to the conclusion that the derivative of either axes current is cross-coupled with both the d-axis and q-axis

currents. To simplify the controller design decoupling between the d-axis and q-axis components must be achieved as unsatisfactory dynamic performance would otherwise result [6, p. 147].

$$v_{gd} - v_{cd} = \left(sL + R\right) i_{gd} - \omega L i_{gq} \tag{14}$$

$$v_{gq} - v_{cq} = \left(sL + R\right) i_{gq} + \omega L i_{gd} \tag{15}$$

Equations (14) and (15) represent the Laplace transformation of the synchronous frame equations (10) and (11) to move from the time domain to the frequency domain. Analysis in the time domain would present difficulties since the equations are non-linear.

$$i_{gd} = (v_{gd} - v_{cd} + \omega L i_{gq}) / \left(sL + R\right) \tag{16}$$

$$i_{gq} = (v_{gq} - v_{cq} - \omega L i_{gd}) / \left(sL + R\right) \tag{17}$$

Equations (16) and (17) represents the transfer functions of the system model that will be used in the inner current controllers.

2.3. Current Controllers

The current control methods for the voltage source converter can be generalized as either an on-off controller where the controller and modulation are combined or a controller with an open-loop PWM block. With an open-loop PWM block there are many different types of linear controllers that can be implemented such as proportional-integral, state feedback, resonant, and predictive as well as the additional benefit of utilizing many different types of open-loop modulators such as sinusoidal PWM, space vector PWM, and optimal PWM since the compensation for the current error feedback and the voltage modulation are separate parts [5, p. 116].

2.3.1. Proportional-Integral Controller Model

For the PI controller, the proportional gain provides the high-frequency response while the integral gain ensures the output corresponds to the set-point in steady-state [7, p. 67], [8, p. 37]. The conversion of the PI controllers from the time domain to the frequency domain are represented in (18) and(19). In order to account for the difference in the desired and actual current a voltage reference is requested for the voltage source converter to generate [5].

$$
\begin{aligned}
v_{cd}^{*} &= K_{p,c}\left(i_{gd}^{*}-i_{gd}\right)+K_{i,c}\int\left(i_{gd}^{*}-i_{gd}\right)dt \\
&= K_{p,c}\left(i_{gd}^{*}-i_{gd}\right)+\frac{K_{i,c}\left(i_{gd}^{*}-i_{gd}\right)}{s} \\
&= \left(i_{gd}^{*}-i_{gd}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right) \because T_{i,c}=\frac{K_{p,c}}{K_{i,c}}
\end{aligned} \tag{18}
$$

$$
\begin{aligned}
v_{cq}^{*} &= K_{p,c}\left(i_{gq}^{*}-i_{gq}\right)+K_{i,c}\int\left(i_{gq}^{*}-i_{gq}\right)dt \\
&= K_{p,c}\left(i_{gq}^{*}-i_{gq}\right)+\frac{K_{i,c}\left(i_{gq}^{*}-i_{gq}\right)}{s} \\
&= \left(i_{gq}^{*}-i_{gq}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right) \because T_{i,c}=\frac{K_{p,c}}{K_{i,c}}
\end{aligned} \tag{19}
$$

The transfer functions of PI controllers can be represented in the following forms in equation(20) and the derivation between the different forms can be found in Appendix D: Proportional-Integral Controller Forms.

$$
G_{pi}=K_p+\frac{K_i}{s}=K_p\frac{1+sT_i}{sT_i}=K_i\frac{\left(1+s\frac{K_p}{K_i}\right)}{s} \because T_i=\frac{K_p}{K_i} \tag{20}
$$

2.3.2. Converter Model

The worst case execution time of the voltage source converter's computational device is represented in (21) as the sample period. The statistical delay of the modulator for the voltage source converter is represented in (22) as the average time required for the ability to generate the desired voltage [1, pp. 317,351], [9, pp. 118-119].

$$
T_{mp}=T_s \tag{21}
$$

$$
T_{PWM}=0.5T_s \tag{22}
$$

$$
T_d=T_{mp}+T_{PWM}=1.5T_s \tag{23}
$$

The voltage source converter transfer function in (24),(25), and (26) is modeled as a first order low pass filter with a bandwidth determined by the sum of the delays in (23) and gain due to modulation technique chosen [5, p. 147], [8, p. 35].

$$G_{converter} = \frac{K_{conv}}{1+sT_d} \approx K_{conv} e^{-sT_d} \tag{24}$$

$$v_{cd} = \frac{K_{conv}}{1+sT_d} v_{cd}^* \tag{25}$$

$$v_{cq} = \frac{K_{conv}}{1+sT_d} v_{cq}^* \tag{26}$$

The cascaded representation [8, p. 17] of the PI Controller and voltage source converter transfer function is represented in (27) and(28).

$$v_{cd} = \frac{K_{conv}}{1+sT_d} \underbrace{\left(i_{gd}^* - i_{gd}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)}_{v_{cd}^*} \tag{27}$$

$$v_{cq} = \frac{K_{conv}}{1+sT_d} \underbrace{\left(i_{gq}^* - i_{gq}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)}_{v_{cq}^*} \tag{28}$$

2.3.3. Feedforward and Disturbance Decoupling

By rearranging (14) and (15) the system transfer function can be represented in (29) and(30). Using rules from the block diagram representation of cascaded transfer functions [8, p. 17] the negative unity gain (inversion) indicated in the leftmost part of (29) and (30) can then be rearranged to reside on the output of the PI Controller transfer function. To achieve a controller design with decoupling the unwanted the d-axis and q-axis current components in the system transfer function should be treated as disturbances with the inverted d-axis or q-axis component added to the output of the PI Controller transfer function. This cancels out the effect of the d-axis or q-axis current disturbance represented in the system transfer function which can be derived using Mason's signal flow rules [8, p. 134]. Since the d-axis and q-axis grid voltage components from the system transfer functions are known, the feed-forward technique can be used to add this information to improve the command response of the current controller [8, p. 145] thereby allowing the voltage source converter excitation to respond only to corrections required to meet the desired d-axis or q-axis current reference.

$$\underset{inv}{-}\left(v_{cd} - v_{gd} - \omega L i_{gq}\right) = \left(sL+R\right) i_{gd} \tag{29}$$

$$\underset{inv}{-}(v_{cq}-v_{gq}+\omega L i_{gd})=\left(sL+R\right)i_{gq} \tag{30}$$

$$v_{cd}^{*}=\underset{inv}{-}\underbrace{\left(i_{gd}^{*}-i_{gd}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)}_{PI\ Output}\underbrace{+\omega L i_{gq}+v_{gd}}_{\substack{Decoupling\ \&\\ Feedforward}} \tag{31}$$

$$v_{cq}^{*}=\underset{inv}{-}\underbrace{\left(i_{gq}^{*}-i_{gq}\right)\left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)}_{PI\ Output}\underbrace{-\omega L i_{gd}+v_{gq}}_{\substack{Decoupling\ \&\\ Feedforward}} \tag{32}$$

2.3.4. Anti-Aliasing Filter Feedback Model

For the feedback model in the non-unity closed loop transfer function of the current controller a multiple feedback 2nd order, low pass analog filter implemented on the current measurement is modeled as a 1st order low-pass filter using the cut-off frequency of the 2nd order MFB filter [8, p. 29]. The filter helps in reducing gain near and above the resonant frequency while the cost is the phase lag it introduces and subsequently the reduced phase margin.

$$G_{feedback,i}=\frac{1}{1+sT_{aaf}} \tag{33}$$

$$T_{aaf}=2\pi f_{cut-off} \tag{34}$$

2.3.5. Per-Unit Representation

For simplification in the controller tuning methodology and selection of components (35) and (36) show the conversion of the d-axis and q-axis system transfer functions (14) and (15) to per-unit representation using Appendix A: Per Unit Values.

$$\begin{aligned} V_b\left(v_{gd,pu}-v_{cd,pu}\right)&=\left(sL_{pu}L_b+R_{pu}Z_b\right)i_{gd,pu}I_b-\omega_{pu}\omega_b L_{pu}L_b i_{gq,pu}I_b \\ v_{gd,pu}-v_{cd,pu}&=Z_b\left(\frac{sL_{pu}}{\omega_b}+R_{pu}\right)i_{gd,pu}\frac{I_b}{V_b}-\left(\omega_{pu}\omega_b\right)\left(\frac{L_{pu}Z_b}{\omega_b}\right)i_{gq,pu}\frac{I_b}{V_b} \\ v_{gd,pu}-v_{cd,pu}&=\left(\frac{sL_{pu}}{\omega_b}+R_{pu}\right)i_{gd,pu}-L_{pu}i_{gq,pu} \end{aligned} \tag{35}$$

$$V_b\left(v_{gq,pu}-v_{cq,pu}\right)=\left(sL_{pu}L_b+R_{pu}Z_b\right)i_{gq,pu}I_b+\omega_{pu}\omega_b L_{pu}L_b i_{gd,pu}I_b$$

$$v_{gq,pu}-v_{cq,pu}=Z_b\left(\frac{sL_{pu}}{\omega_b}+R_{pu}\right)i_{gq,pu}\frac{I_b}{V_b}+\left(\omega_{pu}\omega_b\right)\left(\frac{L_{pu}Z_b}{\omega_b}\right)i_{gd,pu}\frac{I_b}{V_b} \tag{36}$$

$$v_{gq,pu}-v_{cq,pu}=\left(\frac{sL_{pu}}{\omega_b}+R_{pu}\right)i_{gq,pu}+L_{pu}i_{gd,pu}$$

Equations (37) and (38) represent the conversion of the converter transfer function gain to the per-unit representation dependent upon the applied modulation technique chosen for the voltage source converter.

$$\begin{aligned}K_{conv,spwm,pu}&=\frac{\left(\frac{\sqrt{2}}{\sqrt{3}}\right)\left(\left(\frac{\sqrt{3}}{\sqrt{2}}\right)m_a\frac{V_{dc}}{2}\right)}{V_b}\\&=\frac{\left(\frac{\sqrt{2}}{\sqrt{3}}\right)\left(\left(\frac{\sqrt{3}}{\sqrt{2}}\right)m_a\frac{2V_bV_{dc,pu}}{2}\right)}{V_b}\\&=1\because m_a=1,V_{dc,pu}=1\end{aligned} \tag{37}$$

$$\begin{aligned}K_{conv,pu}&=\frac{\left(\frac{\sqrt{2}}{\sqrt{3}}\right)\left(\frac{V_{dc}}{\sqrt{2}}\right)}{V_b}\\&=\frac{\left(\frac{\sqrt{2}}{\sqrt{3}}\right)\left(m_a\frac{2V_bV_{dc,pu}}{\sqrt{2}}\right)}{V_b}\\&=\frac{2}{\sqrt{3}}\because m_a=1,V_{dc,pu}=1\\&\approx 1.1547\end{aligned} \tag{38}$$

2.3.6. Block Diagram Representation of Transfer Functions

The combination of generic controller, converter, system, and feedback blocks is represented as a closed loop feedback diagram as shown in Figure 5. By substituting the respective d-axis and q-axis transfer functions for the controller, converter, system, and feedback into the blocks of Figure 5 the resultant Figure 6 and Figure 7 then represent the decoupled d-axis and q-axis current controllers for the voltage source converter. For development of the tuning method used on the current controllers Figure 6 and Figure 7 are

then simplified to Figure 8 and Figure 9 to represent the decoupled d-axis and q-axis current controllers in per-unit representation.

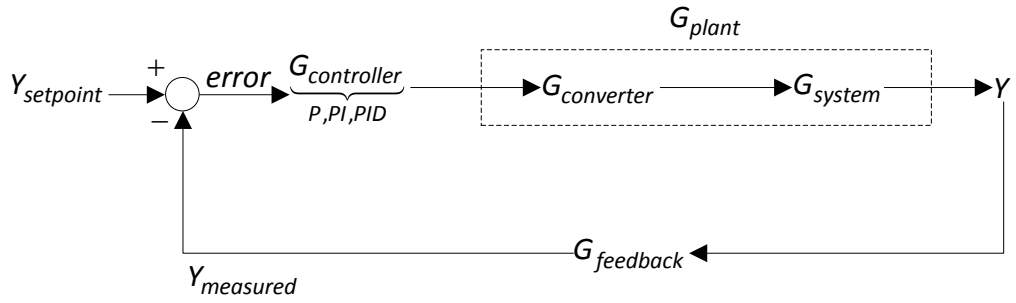

Figure 5 - Typical Closed-Loop Feedback System

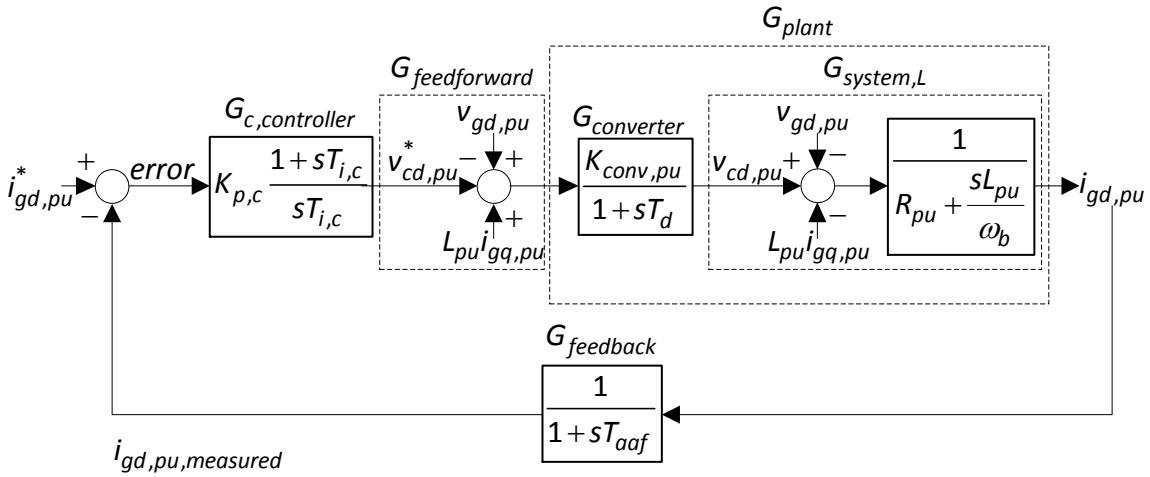

Figure 6 - Decoupled Current Controller (d-axis)

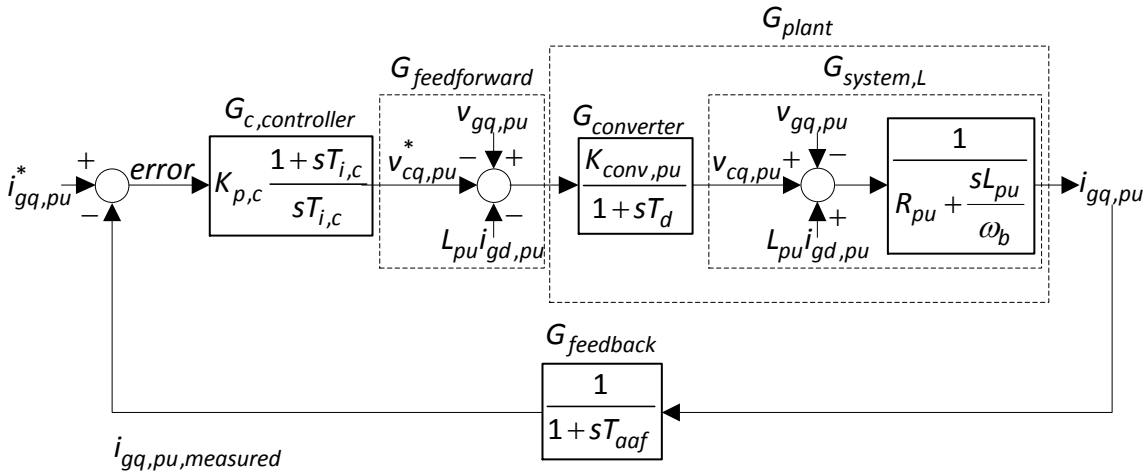

Figure 7 - Decoupled Current Controller (q-axis)

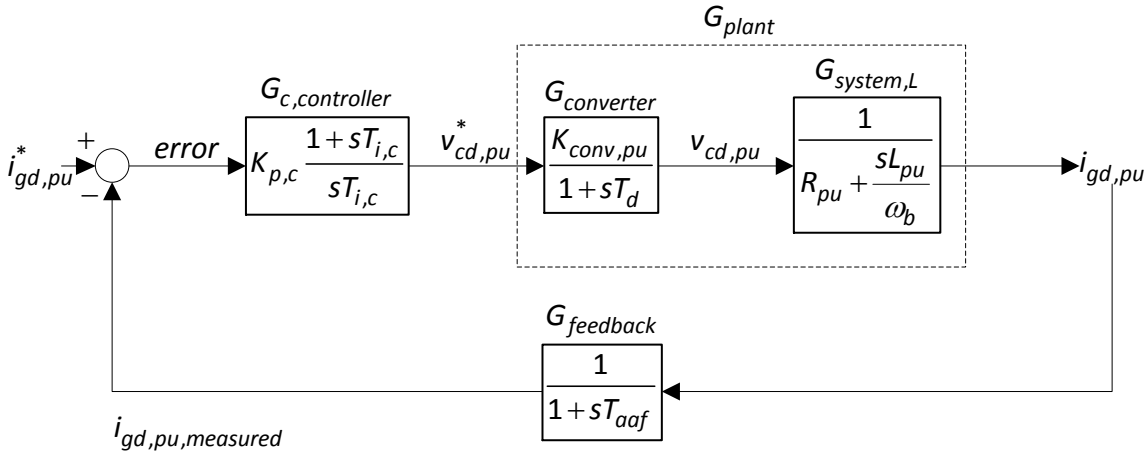

Figure 8 - Simplified Representation of the Decoupled Current Controller (d-axis)

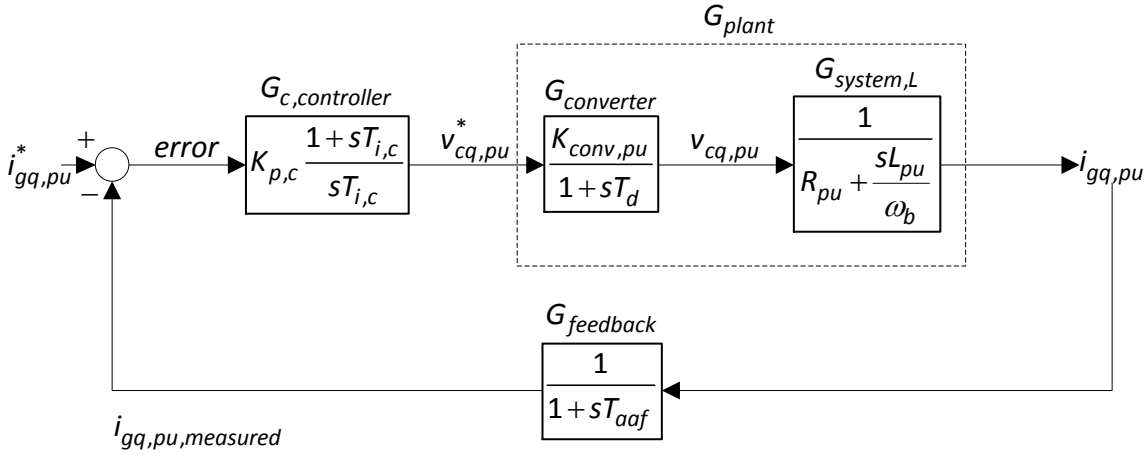

Figure 9 - Simplified Representation of the Decoupled Current Controller (q-axis)

2.3.7. Modulus Optimum Tuning of Current Controller

Each block in the closed loop current controller contributes phase lag and gain to the overall response. When 180 degrees of phase lag is introduced into the controller, positive feedback will result. With positive feedback and unity gain through the loop the control system is classified as unstable. Finding the optimal values for the PI Controller parameters will mitigate this and other unstable scenarios for the control system. An optimization method is a robust technique for determining PI controller parameters. By utilizing the magnitude optimum tuning technique a frequency response of the current controller's reference to actual output will be as close to unity as possible for low frequencies [7, p. 166].

By evaluating the product of the forward path and feedback transfer functions of Figure 8 or Figure 9 results in the current controller open loop transfer function as in (39) [10, p. 6.6].

$$\begin{aligned} G_{cc,OL} &= G_{pi,c}G_{converter}G_{system,L}G_{feedback,i} \\ &= \left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)\left(\frac{K_{conv,pu}}{1+sT_d}\right)\left(\frac{\frac{1}{R_{pu}}}{1+sT_L}\right)\left(\frac{1}{1+sT_{aaf}}\right) \\ &\approx \left(K_{p,c}\frac{1+sT_{i,c}}{sT_{i,c}}\right)\left(\frac{K_{conv,pu}}{1+s(T_d+T_{aaf})}\right)\left(\frac{\frac{1}{R_{pu}}}{1+sT_L}\right) \end{aligned} \tag{39}$$

The system inductance is dominant pole. The poles introduced by the converter and feedback transfer functions are considered minor and are therefore approximated in the open loop transfer function with(40).

$$T_a = T_d + T_{aaf} \because T_L \gg T_d \,\&\, T_{aaf} \tag{40}$$

The magnitude optimum utilizes the dominant pole cancellation technique to mitigate the effect of the pole introduced by the system inductance with the zero of the PI controller with(41).

$$T_{i,c} = T_L \because \textit{dominant pole cancellation} \tag{41}$$

Following the design procedure for magnitude optimum by evaluating the structure of (39) the proportional gain is specified in(42) [7, p. 171].

$$K_{p,c\ magnitude\ optimum} = \frac{R_{pu}T_L}{2T_aK_{conv,pu}} \tag{42}$$

Substituting (41) and (42) into (39) results in the simplified open loop current controller of(43).

$$G_{cc,OL} = \frac{\frac{1}{2T_a}}{s\left(1+sT_a\right)} \tag{43}$$

The closed loop current controller found in (44) when algebraically reduced can be recognized as the standard form of a second order transfer function depicted in (45) when ignoring the zero introduced by the feedback transfer function.

$$\begin{aligned} G_{cc,CL} &= \frac{G_{pi,c}G_{converter}G_{system,L}}{1+G_{pi,c}G_{converter}G_{system,L}G_{feedback,i}} \\ &= \left(\frac{K_{p,c}K_{conv,pu}}{T_aT_LR_{pu}}\right)\frac{1+sT_{aaf}}{s\left(\frac{1+sT_a}{T_a}\right)+\left(\frac{K_{p,c}K_{conv,pu}}{T_aT_LR_{pu}}\right)} \\ &= \underbrace{\left(\frac{K_{p,c}K_{conv,pu}}{T_aT_LR_{pu}}\right)}_{\omega_n^2}\frac{1+sT_{aaf}}{s^2+\underbrace{\left(\frac{1}{T_a}\right)}_{2\zeta\omega_n}s+\underbrace{\left(\frac{K_{p,c}K_{conv,pu}}{sT_aT_LR_{pu}}\right)}_{\omega_n^2}} \end{aligned} \tag{44}$$

$$\textit{Standard Form 2nd Order Transfer Function} = \frac{\omega_n^2}{s^2+2\zeta\omega_n+\omega_n^2} \tag{45}$$

The response of the standard form of a second order transfer function can be classified as overdamped, critically damped, and underdamped with ω_n referred to as the undamped natural frequency and ζ referred to as the damping ratio in (45) [10, p. 7.8]. A fast dynamic response for the current controller is desirable so (44) will reflect an underdamped second order transfer function. By using (46) a desirable phase margin and percent overshoot can be found for an underdamped second order transfer function.

$$\begin{aligned} &0 \le \zeta < 1, \textit{the resulting oscillatory system response is underdamped} \\ &k = \sqrt{(1-\zeta^2)} \\ &\textit{Phase Margin} = tan^{-1}\left(\zeta / k\right) \\ &\textit{Percent Overshoot} = e^{-\zeta\pi/\sqrt{1-\zeta^2}} \end{aligned} \tag{46}$$

By choosing the damping ratio defined in(47), as the modulus optimum method does, the underdamped response will provide the optimal rise and settling time for a low amount of

overshoot for the response of a second order transfer function. A larger damping ratio would negatively impact our settling and rise time, but reduce the overshoot. A smaller damping ratio would negatively impact the overshoot and settling time, but positively impact our rise time [10, p. 7.9].

$$\zeta = 0.707 \tag{47}$$

By rearranging the characteristic polynomial equation of (44) the relationships in (48) and (49) are found.

$$\omega_n = \frac{1}{2\zeta T_a} \tag{48}$$

$$\omega_n^2 = \frac{K_{p,c} K_{conv,pu}}{s T_a T_L R_{pu}} \tag{49}$$

By substituting (48) into (49) the relationship for the proportional gain is defined in (50) for a particular damping ratio and control system parameters.

$$K_{p,c} = \frac{R_{pu} T_L}{4\zeta^2 T_a K_{conv,pu}} \tag{50}$$

By substituting (50) into (44) the closed loop current controller can be further simplified to (51).

$$G_{cc,CL} = \frac{1 + sT_{aaf}}{4\zeta^2 T_a^2 s^2 + 4\zeta^2 T_a s + 1} \tag{51}$$

2.4. Voltage Controller

The voltage source converter that maintains the DC Bus level is designed with multiple loop control [11, p. 16.24]. The voltage controller is the outer loop with the tuned current controller residing within. From the perspective of the voltage controller the inner current loop acts as a low pass filter [8, p. 52].

2.4.1. Proportional-Integral Controller Model

The conversion of the PI controller from the time domain to the frequency domain is represented in(52). In order to account for the difference in the desired and actual dc bus voltage level a d-axis current reference is requested for the voltage source converter to generate [5].

$$
\begin{aligned}
i_{gd}^{*} &= K_{p,v}\left(V_{dc}^{*} - V_{dc}\right) + K_{i,v}\int\left(V_{dc}^{*} - V_{dc}\right)dt \\
&= K_{p,v}\left(V_{dc}^{*} - V_{dc}\right) + \frac{K_{i,v}\left(V_{dc}^{*} - V_{dc}\right)}{s} \\
&= \left(V_{dc}^{*} - V_{dc}\right)\left(K_{p,v}\frac{1 + sT_{i,v}}{sT_{i,v}}\right)
\end{aligned}
\tag{52}
$$

2.4.2. Approximation of Current Controller Model

The zero due to the feedback in the closed loop current controller of (51) can be ignored since it wouldn't negatively affect the system until well beyond the bandwidth of the current controller [12, p. 600]. Using the damping ratio in (47) the second order transfer function of the closed loop current controller is approximated in (54) as a first order low pass filter [7, p. 55], [5, p. 131]. If the total impact of the anti-aliasing filter in the current controller is ignored then the relationship between the computational device sample time and bandwidth of the current controller is defined in(55) [1, pp. 215, 351].

$$
G_{cc,CL} = \frac{1}{4\zeta^2 T_a^2 s^2 + 4\zeta^2 T_a s + 1} \approx \frac{1}{1 + s4\zeta^2 T_a} \tag{53}
$$

$$
G_{cc,1stOrdAppx} = \frac{1}{1 + s2T_a} \because \zeta = 0.707 \tag{54}
$$

$$
T_{cc} = 2T_a \approx 3T_s \because anti-aliasing\ filter\ is\ ignored \tag{55}
$$

2.4.3. Power Balance Model

To establish the power balance between the ac and dc side of the voltage source converter the relationship of dc voltage to d-axis current is required. Applying Kirchhoff's current law to Figure 4 the relationship between the phase currents, load current, and dc-link capacitor current is defined in (56) using the switch states of (57) [11, p. 11.7].

$$
i_C + i_o = i_{dc} = S_a i_{ga} + S_b i_{gb} + S_c i_{gc} \because (S_a = 1, S_b = 0, S_c = 0)\ is\ 1\ of\ 8\ possible\ states \tag{56}
$$

$$
\begin{aligned}
S_x &= 1\ the\ upper\ IGBT\ of\ one\ leg\ in\ the\ converter\ is\ switched\ ON\ (x = a,b,c) \\
S_x &= 0\ the\ lower\ IGBT\ of\ one\ leg\ in\ the\ converter\ is\ switched\ ON\ (x = a,b,c)
\end{aligned}
\tag{57}
$$

The instantaneous power balance for the voltage source converter in the synchronous rotating *dq* frame neglecting any losses is expressed in(58) since the ac-side active power is equal to the dc-side power [1, p. 213].

$$v_{dc}\underbrace{C_{dc}\frac{dv_{dc}}{dt}}_{i_c}+v_{dc}i_o=v_{dc}i_{dc}=\frac{3}{2}\left\{v_{gd}i_{gd}+v_{gq}i_{gq}\right\}\because P_{dc}=P_{ac} \tag{58}$$

Applying the small signal linearization to (58) leads to(59). The goal is to find the transfer function between the d-axis current and dc voltage so all perturbations including second-order signal perturbations are ignored resulting in (60) [1, p. 214].

$$(V_{dc}+\hat{v}_{dc})C_{dc}\frac{d(V_{dc}+\hat{v}_{dc})}{dt}+(V_{dc}+\hat{v}_{dc})(I_o+\hat{i}_o)=\frac{3}{2}\left\{(V_{gd}+\hat{v}_{gd})(I_{gd}+\hat{i}_{gd})+(V_{gq}+\hat{v}_{gq})(I_{gq}+\hat{i}_{gq})\right\} \tag{59}$$

$$V_{dc}C_{dc}\frac{d\hat{v}_{dc}}{dt}+\hat{v}_{dc}I_o+V_{dc}I_o=\frac{3}{2}\left\{V_{gd}I_{gd}+V_{gd}\hat{i}_{gd}+V_{gq}I_{gq}\right\} \tag{60}$$

Simplification of (60) considering (61) leads to(62).

$$V_{dc}I_o=\frac{3}{2}\left\{V_{gd}I_{gd}+V_{gq}I_{gq}\right\} \tag{61}$$

$$V_{dc}C_{dc}\frac{d\hat{v}_{dc}}{dt}+\hat{v}_{dc}I_o=\frac{3}{2}\left\{V_{gd}\hat{i}_{gd}\right\} \tag{62}$$

Applying algebraic manipulation to (62) leads to the relationship of dc voltage to d-axis current in(63).

$$\begin{aligned}
V_{dc}C_{dc}\frac{d\hat{v}_{dc}}{dt}+\hat{v}_{dc}I_o&=\frac{3}{2}\left\{V_{gd}\hat{i}_{gd}\right\}\\
V_{dc}(C_{dc}\frac{d\hat{v}_{dc}}{dt}+\hat{v}_{dc}I_o\frac{1}{V_{dc}})&=\frac{3}{2}\left\{V_{gd}\hat{i}_{gd}\right\}\\
\sqrt{3}V_{gd}(C_{dc}\frac{d\hat{v}_{dc}}{dt}+\hat{v}_{dc}I_o\frac{1}{R_oI_o})&=\frac{3}{2}\left\{V_{gd}\hat{i}_{gd}\right\}\because V_{dc}\geq\sqrt{3}V_{gd}\\
\hat{v}_{dc}(sC_{dc}+\frac{1}{R_o})&=\frac{\sqrt{3}}{2}\hat{i}_{gd}\\
\frac{\hat{v}_{dc}}{\hat{i}_{gd}}&=\frac{\sqrt{3}}{2}\frac{1}{sC_{dc}+\frac{1}{R_o}}
\end{aligned} \tag{63}$$

From a controller tuning perspective, the worst case stability standpoint of (63) simplifies to(64) during no load operation since the pole would reside on the imaginary axis [13, p. 711], [14, p. 103].

$$\frac{\hat{v}_{dc}}{\hat{i}_{gd}} = \frac{\sqrt{3}}{2}\frac{1}{sC_{dc}} \because R_o \to \infty \because I_o \to 0 \tag{64}$$

2.4.4. Digital Filter Feedback Model

To ensure that the inner current loop is at least 5 times faster than the outer voltage loop a digital low pass filter in (65) is used on the voltage feedback to slow the system response down [14, p. 375], [8, p. 52] but without the introduction of unnecessary filtering that would lead to sluggish control [8, p. 16]. By setting the frequency in (66) to half of the computational device's update rate and examining the scenario of a step function applied to (65) leads to a delay of 6 sample periods to reach 95% of the input [1, p. 218].

$$G_{feedback,v} = \frac{1}{1+sT_{lp}} \tag{65}$$

$$F_{lp} = 0.5F_s \tag{66}$$

2.4.5. Per-Unit Representation

For simplification in the controller tuning methodology (67) shows the conversion of the power balance transfer function (64) to per-unit representation using Appendix A: Per Unit Values.

$$V_{dc,pu}2V_b sC_{dc}\hat{v}_{dc,pu}2V_b + \underbrace{\hat{v}_{dc}I_o}_{no\ load} = \frac{3}{2}\left\{V_{gd}V_b\hat{i}_{gd}I_b\right\} \because V_{dc,b} = 2V_b$$

$$\underbrace{V_{dc,pu}}_{=1}\,4V_b^2 sC_{dc}\hat{v}_{dc,pu} = \frac{3}{2}\underbrace{V_{gd,pu}}_{=1 \because VOC}\,V_b\hat{i}_{gd,pu}I_b$$

$$sC_{dc}\hat{v}_{dc,pu} = \frac{3}{8}\frac{I_b}{V_b}\hat{i}_{gd,pu}$$

$$\frac{\hat{v}_{dc,pu}}{\hat{i}_{gd,pu}} = \frac{3}{8}\frac{1}{sC_{dc}Z_b}$$

$$\frac{\hat{v}_{dc,pu}}{\hat{i}_{gd,pu}} = \frac{3}{8}\frac{1}{sC_{dc,pu}C_{b,dc}Z_b} \because C_{dc} = C_{dc,pu}C_{b,dc}$$

$$\frac{\hat{v}_{dc,pu}}{\hat{i}_{gd,pu}} = \frac{3}{8}\frac{8}{3}\frac{1}{sC_{dc,pu}C_bZ_b} \because C_{b,dc} = \frac{3}{8}C_b$$

$$\frac{\hat{v}_{dc,pu}}{\hat{i}_{gd,pu}} = \frac{1}{sC_{dc,pu}\frac{1}{Z_b\omega_b}Z_b} \because C_b = \frac{1}{Z_b\omega_b}$$

$$G_{system,C} = \frac{\hat{v}_{dc,pu}}{\hat{i}_{gd,pu}} = \frac{1}{s\frac{C_{dc,pu}}{\omega_b}} \tag{67}$$

2.4.6. Block Diagram Representation of Transfer Functions

The non-unity closed loop feedback diagram for the per-unit representation of the voltage controller is shown in Figure 10. The 6 sample period delays introduced into the design of the voltage controller as a result of a step response with respect to the voltage feedback transfer function results in the desired slowdown of the system and Figure 10 can be further simplified to Figure 11 [15, pp. 758-759], [11, p. 16.26].

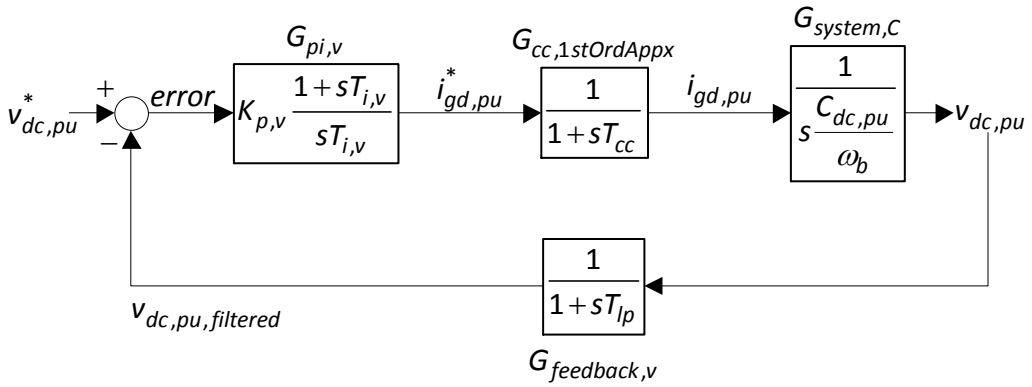

Figure 10 - Per Unit Voltage Controller

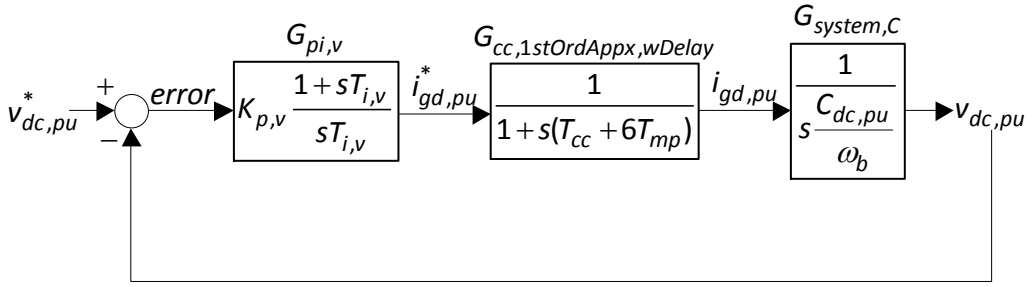

Figure 11 - Simplified Per Unit Voltage Controller

2.4.7. Symmetrical Optimum Tuning of Voltage Controller

By utilizing the symmetrical optimum tuning technique a cross-over frequency with the maximum amount of phase margin is obtained from the geometric mean between the approximated current controller with delay and PI controller frequencies that result in an optimum amount of damping for the voltage controller [16, pp. 85-87].

Evaluating the product of the forward path and feedback transfer functions of Figure 11 results in the voltage controller open loop transfer function as in(68) with the time constants simplified in (69) and (70).

$$G_{vc,OL} = G_{pi,v} G_{cc,1stOrdAppx,wDelay} G_{system,C}$$

$$= \left(K_{p,v} \frac{1+sT_{i,v}}{sT_{i,v}} \right) \left(\frac{1}{1+s(T_{cc}+6T_{mp})} \right) \left(\frac{1}{s\frac{C_{dc,pu}}{\omega_b}} \right) \tag{68}$$

$$= \left(K_{p,v} \frac{1+sT_{i,v}}{sT_{i,v}} \right) \left(\frac{1}{1+sT_b} \right) \left(\frac{1}{sT_{cap}} \right)$$

$$T_b = T_{cc} + 6T_{mp} \tag{69}$$

$$T_{cap} = \frac{C_{dc,pu}}{\omega_b} \tag{70}$$

By first determining the integral component of the PI controller in (71) the cross-over frequency can then be determined in(72).

$$T_{i,v} = a^2 T_b \,, \quad a > 1 \tag{71}$$

$$\omega_d = \frac{1}{\sqrt{T_b T_{i,v}}} = \frac{1}{aT_b} \tag{72}$$

By evaluating the cross-over condition of the open loop transfer function of the voltage controller in (73) the gain component of the PI controller can be determined in(74).

$$\left| G_{vc,OL}(j\omega_d) \right| = 1 \tag{73}$$

$$K_{p,v} = \frac{T_{cap}}{\sqrt{T_b T_{i,v}}} = \frac{T_{cap}}{aT_b} \tag{74}$$

The open loop voltage controller in (68) can be further simplified to (75) by substitution of PI controller parameters defined in (71) and (74).

$$G_{vc,OL} = \left(\frac{1}{s^2 a^3 T_b^2} \right) \left(\frac{1+sa^2 T_b}{1+sT_b} \right) \tag{75}$$

The unity feedback closed loop voltage controller simplifies to(76).

$$G_{vc,CL} = \frac{G_{pi,v}G_{cc,1stOrdAppx,wDelay}G_{system,C}}{1+G_{pi,v}G_{cc,1stOrdAppx,wDelay}G_{system,C}} = \frac{\left(1+sa^2T_b\right)}{s^3a^3T_b^3+s^2a^3T_b^2+sa^2T_b+1} \tag{76}$$

By evaluating the denominator of the closed loop voltage controller a pole exists at (77) [17, p. 29] and with that knowledge by applying long polynomial division leads to the simplification of the closed loop voltage controller in(78).

$$s_1 = -\frac{1}{aT_b} \tag{77}$$

$$G_{vc,CL} = \frac{\left(1+sa^2T_b\right)}{\left(1+saT_b\right)\left(s^2a^2T_b^2+sa^2T_b-saT_b+1\right)} = \frac{\left(1+sa^2T_b\right)}{\left(\underset{\frac{1}{\omega_n}}{1+saT_b}\right)\left(\underset{\frac{1}{\omega_n^2}\qquad\frac{1}{\omega_n}\quad 2\zeta}{s^2a^2T_b^2+saT_b(a-1)+1}\right)} \tag{78}$$

The poles of the standard form of a second order transfer function (45) are represented in(79).

$$Poles\ of\ \ Standard\ Form\ 2nd\ Order\ TF = -\zeta\omega_n \pm \sqrt{\zeta^2\omega_n^2-\omega_n^2} \tag{79}$$

The poles of the third order closed loop voltage controller (76) simplified to first and second order systems in (78) lead to the calculation of the poles in (80).

$$\begin{aligned} s_1 &= -\frac{1}{aT_b} \\ s_{2,3} &= -\underset{\zeta}{\frac{a-1}{2}}\underset{\omega_n}{\frac{1}{aT_b}} \pm \sqrt{\frac{(a-1)^2}{4}\frac{1}{a^2T_b^2}-\frac{1}{a^2T_b^2}} \\ &= \frac{1}{aT_b}\left[-\underset{\zeta}{\frac{a-1}{2}} \pm \sqrt{\frac{(a-1)^2}{4}-1}\right] \end{aligned} \tag{80}$$

Evaluating (80) provides insight for practical values of a following the criteria defined in (71) for the symmetrical optimum tuning. With $a > 1$ and $a < 3$ one real and two complex poles exist with the selection of a impacting the damping ratio (81) which in turn determines the oscillatory part of the response.

$$\zeta = \frac{a-1}{2} \tag{81}$$

When $a \geq 3$ the oscillatory response is removed since three real poles exist and the system can be further dampened by increasing a. Further evaluation of the open loop voltage controller of (75) identifies a double integrating term causing the step response of the closed loop voltage controller to exhibit significant overshoot. To eliminate this overshoot caused by the lead term of the PI Controller a corresponding low pass filter is inserted before the input to the closed loop voltage controller in Figure 12 [16, p. 87], [11, p. 16.26].

$$G_{prefilter} = \frac{1}{1+sT_{i,v}} \tag{82}$$

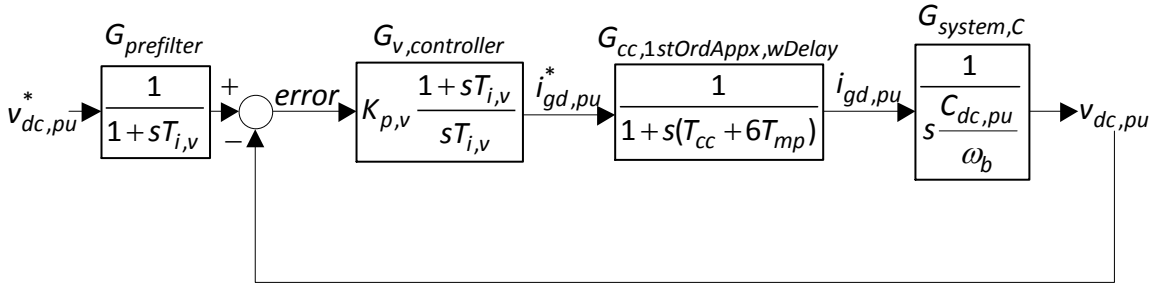

Figure 12 - Simplified Per Unit Voltage Controller with Prefilter

2.5. Active and Reactive Controller Models

The transfer of power between the grid and the voltage source converter in Figure 4 is represented with the *dq* synchronous reference frame active and reactive power equations of (83) and(84). In order for the voltage source converter to achieve the vector control method known as voltage oriented control the d-axis of the synchronous frame must be aligned to the grid voltage vector. With the d-axis of the synchronous frame aligned to the grid voltage vector the magnitudes will be equal to one another resulting in the q-axis of the synchronous frame equal to zero [6, p. 145]. Evaluation of (83) and (84) leads to the conclusion that the active power transferred is a result of controlling the d-axis of the synchronous frame current while the reactive power transferred is a result of controlling the q-axis of the synchronous frame current.

$$P_g = \frac{3}{2}\left(v_{gd}i_{gd} + v_{gq}i_{gq}\right) = \frac{3}{2}v_{gd}i_{gd} \because v_{gq} = 0 \tag{83}$$

$$Q_g = \frac{3}{2}\left(v_{gq}i_{gd} - v_{gd}i_{gq}\right) = -\frac{3}{2}v_{gd}i_{gq} \because v_{gq} = 0 \tag{84}$$

2.5.1. Open Loop Model

The voltage source converter that controls the power consumed and or supplied to the grid is designed with open loop control of the active and reactive power [18, p. 70]. In order for the PQ controllers to interface the *dq* current controllers (83) and (84) are simplified to per-unit representation in (85) and (86) using Appendix A: Per Unit Values.

$$\frac{3}{2}V_b I_b P_{g,pu} = \frac{3}{2}V_b v_{gd,pu} I_b i_{gd,pu} \quad P_{g,pu} = v_{gd,pu}i_{gd,pu} \tag{85}$$

$$\frac{3}{2}V_b I_b Q_{g,pu} = \frac{3}{2}V_b v_{gd,pu} I_b i_{gd,pu} \quad Q_{g,pu} = -v_{gd,pu}i_{gq,pu} \tag{86}$$

The per-unit open loop PQ controllers are represented in (87) and(88).

$$P^*_{g,pu} = v_{gd,pu}i^*_{gd,pu} \tag{87}$$

$$Q^*_{g,pu} = -v_{gd,pu}i^*_{gq,pu} \tag{88}$$

2.6. Phase-Locked Loop

For voltage oriented control of the voltage source converter the grid voltage angle must be detected in order to align the d-axis of the synchronous frame to the grid voltage vector. With the coordinate transformation of the grid voltage from the *abc* three-phase stationary reference frame to the $\alpha\beta$ two-phase stationary reference frame the grid voltage angle can then be detected in(89). However, any harmonic content present on the grid voltage may distort the measured angle so instead a phase locked loop is employed [6, pp. 144-145].

$$\theta_g = tan^{-1}\frac{v_{g\beta}}{v_{g\alpha}} \tag{89}$$

The general concept of the phase-locked loop is to use a PI Controller to establish the grid voltage angle from the grid voltage vector. With the actual grid voltage angle detected, the transformation of the grid voltage vector to the $\alpha\beta$ two-phase stationary reference frame is defined in (90) and (91) [19, p. 81].

$$v_{g\alpha} = v_g cos\theta_g \tag{90}$$

$$v_{g\beta} = v_g sin\theta_g \tag{91}$$

Substituting (90) and (91) into the coordinate transformation of the $\alpha\beta$ two-phase stationary reference frame to the *dq* synchronous reference frame in Appendix B: Coordinate Transformations results in (92) and (93). Evaluating (93) shows that when the grid voltage angle is established the q-axis of the synchronous frame grid voltage is zero.

$$\begin{aligned} v_{gd} &= cos\theta_g v_{g\alpha} + sin\theta_g v_{g\beta} \\ &= v_g\left(cos^2\theta_g + sin^2\theta_g\right) \\ &= v_g \because cos^2\theta_g + sin^2\theta_g = 1 \end{aligned} \tag{92}$$

$$\begin{aligned} v_{gq} &= -sin\theta_g v_{g\alpha} + cos\theta_g v_{g\beta} \\ &= v_g\left(-sin\theta_g cos\theta_g + cos\theta_g sin\theta_g\right) \\ &= 0 \end{aligned} \tag{93}$$

The output of a PI controller represents the deviation control signal. Since a correct detection of the grid voltage angle results in zero for the q-axis of the synchronous frame grid voltage, it is used as the input to the PI Controller. The addition of the steady-state term to the PI Controller output represents the actual control signal instead of simply the deviation control signal which would result without the addition of the steady-state term [19, p. 91]. By adding the base grid frequency as the bias signal to the PI controller output deviation control signal calculated from the q-axis of the synchronous frame grid voltage the grid frequency is established in(94).

$$\begin{aligned}\omega_g &= \underbrace{K_{p,pll}\left(v_{gq}-0\right)+K_{i,pll}\int\left(v_{gq}-0\right)dt}_{G_{pi,pll}} + \underbrace{2\pi f_b}_{\omega_b} \\ &= K_{p,pll}v_{gq}+\frac{K_{i,pll}v_{gq}}{s}+2\pi f_g \\ &= v_{gq}\left(K_{p,pll}\frac{1+sT_{i,pll}}{sT_{i,pll}}\right)+2\pi f_g \because T_{i,pll}=\frac{K_{p,pll}}{K_{i,pll}}\end{aligned} \tag{94}$$

The result of the integration of grid frequency leads to the grid voltage angle in(95).

$$\begin{aligned}\theta_g &= \int \omega_g dt \\ &= \frac{\omega_g}{s}\end{aligned} \tag{95}$$

The sampling delay of the computational device can be modeled as a first order low pass filter in (96) with a bandwidth determined by the sampling time of the computational device in (21) [20, p. 59].

$$G_{computational\ device} = \frac{1}{1+sT_{mp}} \tag{96}$$

With the transfer functions for the controller, computational device, and integrator known the resultant diagram for the detection of the grid voltage angle using a phase-locked loop is represented in Figure 13.

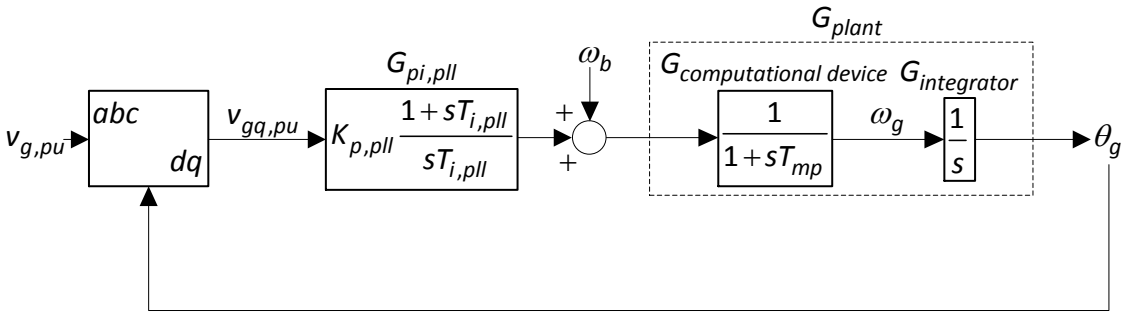

Figure 13 - Phase-Locked Loop for Grid Voltage Angle Detection

2.6.1. Symmetrical Optimum Tuning of Phase-Locked Loop

By utilizing the symmetrical optimum tuning technique a cross-over frequency with the maximum amount of phase margin is obtained from the geometric mean between the computational device and PI controller frequencies that result in an optimum amount of damping for the phase-locked loop.

Evaluating the product of the forward path of Figure 13 results in the phase-locked loop transfer function as in(97).

$$\begin{aligned} G_{pll} &= G_{pi,pll} G_{computational\ device} G_{integrator} \\ &= \left(K_{p,pll} \frac{1+sT_{i,pll}}{sT_{i,pll}} \right) \left(\frac{1}{1+sT_{mp}} \right) \left(\frac{1}{s} \right) \end{aligned} \tag{97}$$

Since the application of the phase-locked loop is for the electric grid the frequency should remain fairly constant which allows the bandwidth of the phase-locked loop to be designed with the maximum amount of phase margin in relation to the grid frequency in(98) [20, p. 60] to find the most robust phase-locked loop output. By establishing alpha in (99) the appropriate integral component of the PI controller is determined in(100).

$$\begin{aligned} \omega_{pll} &= \omega_b \\ &= \frac{1}{\sqrt{T_{mp} T_{i,pll}}} = \frac{1}{aT_{mp}} \end{aligned} \tag{98}$$

$$a = \frac{1}{T_{mp}\omega_b} \tag{99}$$

$$T_{i,pll} = a^2 T_{mp} \tag{100}$$

By evaluating the cross-over condition of the transfer function of the phase-locked loop in (101) the gain component of the PI controller can be determined in(102).

$$\left| G_{pll}(j\omega_d) \right| = 1 \tag{101}$$

$$K_{p,pll} = \frac{1}{\sqrt{T_{mp} T_{i,pll}}} = \frac{1}{aT_{mp}} \tag{102}$$

3. Project Implementation

The project installation resides at the University of Wisconsin – Milwaukee electrical engineering lab located on the second floor of the USR Building. Figure 14 is the one line diagram of the project installation while Figure 15, Figure 16, and Figure 17 are photos of the installation. The elements in Figure 14 refer to the channels on the Yokogawa power analyzer used to measure the system's phase voltages and currents.

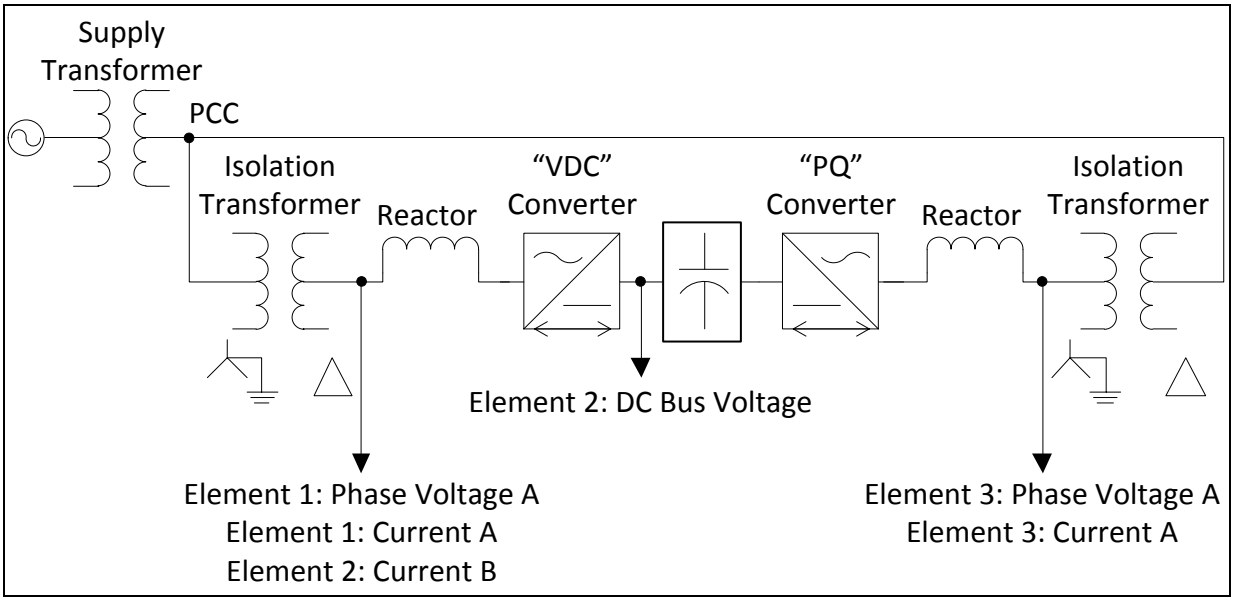

Figure 14 - Project Implementation & Yokogawa Measurements

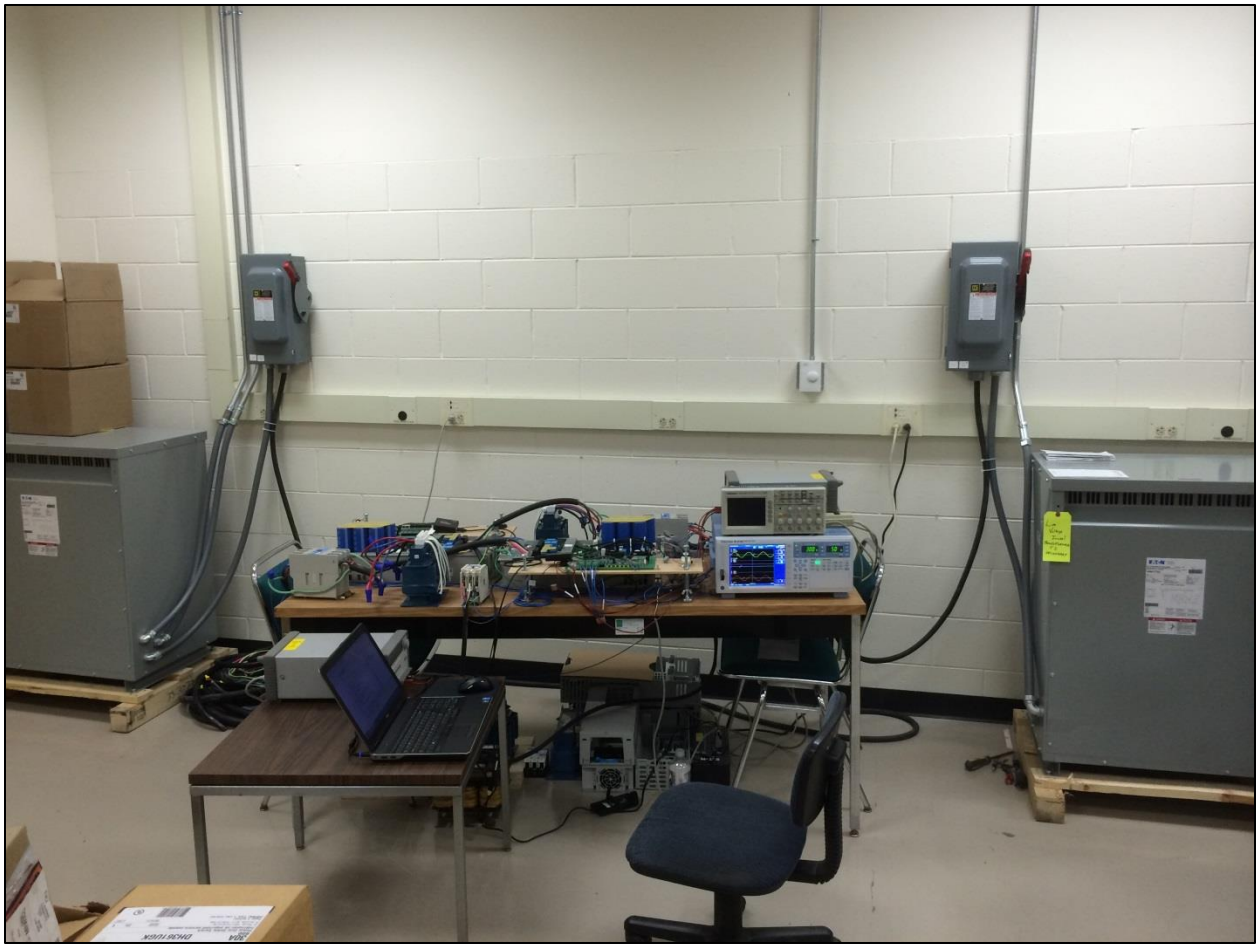

Figure 15 - Project Photo 1

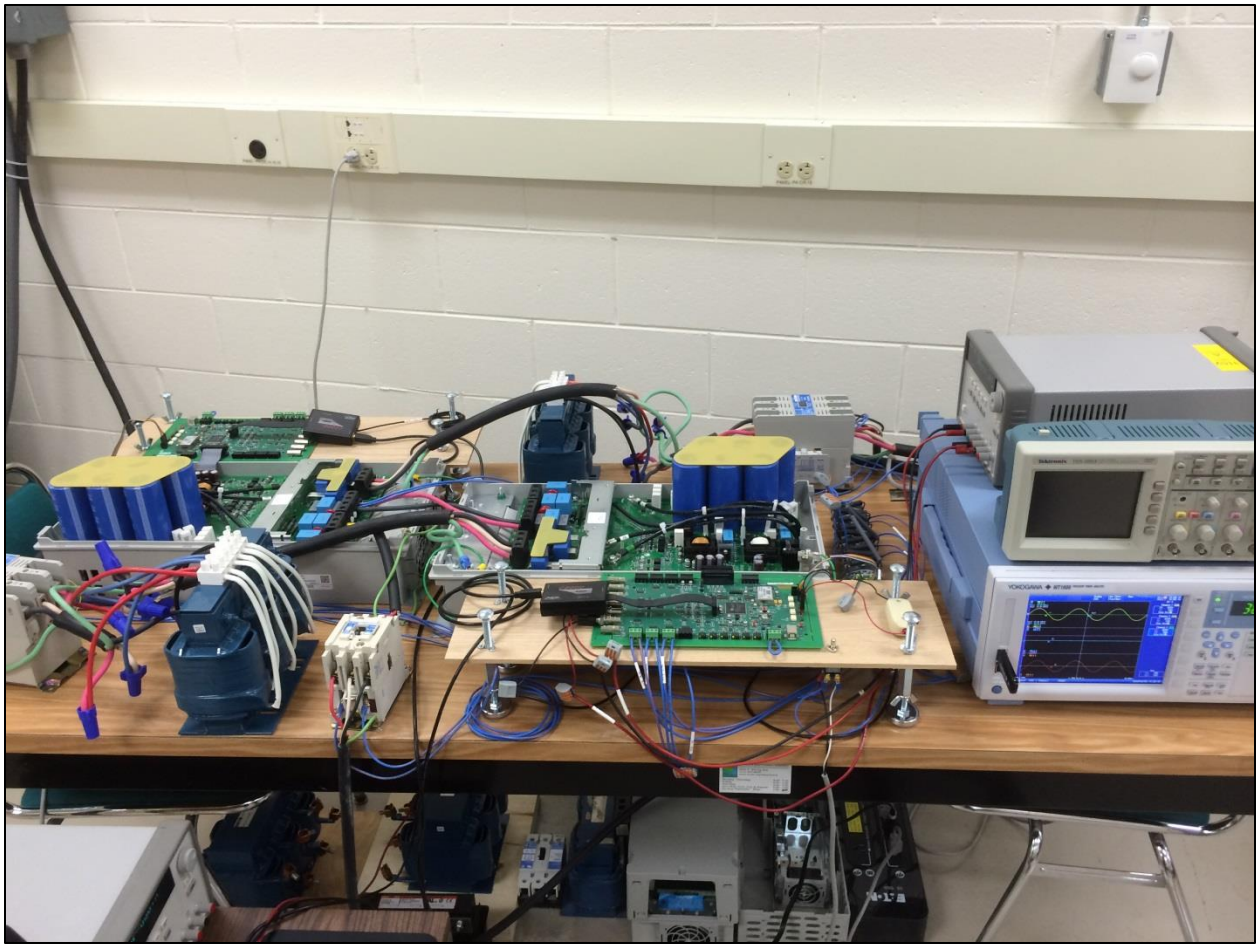

Figure 16 - Project Photo 2

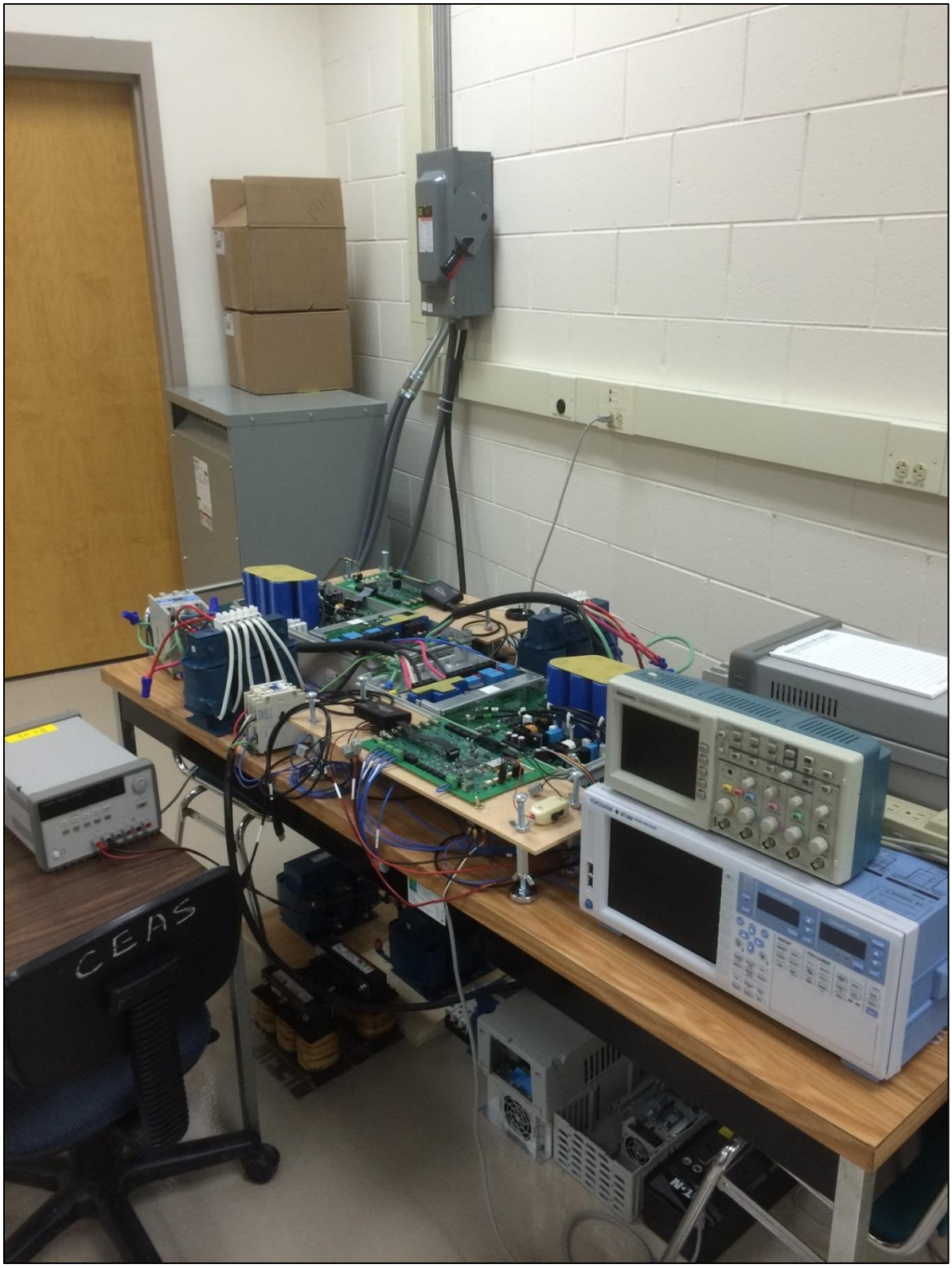

Figure 17 - Project Photo 3

3.1. Supply and Isolation Transformers

A delta-wye 500 kVA transformer configured for 4160VAC on the primary and 480VAC on the secondary supplies 480VAC at 60Hz to two fused electrical disconnects designated for this project in the electrical engineering laboratory. Each of the electrical disconnects feeds a single isolation transformer. The two delta-wye 75 kVA isolation transformers used in this project were donated by Eaton. Since an electrical installation from the supply transformer to the electrical engineering lab already existed, the 500 kVA transformer was chosen as the connection to the grid. Due to the age of the transformer typical performance data was unavailable from the manufacturer. The manufacturer provided modern day equivalent information [21, p. 7] and the equivalent circuit is derived using Appendix F: Delta/Wye Transformer Equivalent Circuit in Table 1.

Transformer Power Rating [kVA]	500
Transformer Impedance [%]	5.5
X/R Ratio	3.36
No Load Losses (Open-Circuit Test) [Watts]	1300
Full Load Losses (Short-Circuit Test) [Watts]	7840
Transformer Resistance [Per-Unit]	0.0157
Transformer Reactance [Per-Unit]	0.0527
Base Primary Winding Resistance [ohms]	103.8336
Base Primary Winding Reactance [ohms]	103.8336
Base Primary Winding Inductance [henries]	0.2754
Base Secondary Winding Resistance [ohms]	0.4608
Base Secondary Winding Reactance [ohms]	0.4608
Base Secondary Winding Inductance [henries]	0.0012
Primary Winding Resistance [ohms]	0.8151
Primary Winding Leakage Reactance [ohms]	2.7360
Primary Winding Leakage Inductance [henries]	0.007258
Secondary Winding Resistance [ohms]	0.003617
Secondary Winding Leakage Reactance [ohms]	0.0121
Secondary Winding Leakage Inductance [henries]	3.22e-5
Magnetization Resistance [ohms]	3.994e+04
Magnetization Resistance [per-unit]	384.6
Magnetization Inductance [henries]	28.52
Magnetization Inductance [per-unit]	103.6

Table 1 - 500 kVA Supply Transformer Performance Data

The high voltage connection for the isolation transformer is a delta winding and the low voltage connection is a wye winding. According to [22, p. 6] in a standard three phase transformer when the high-low voltage connection is wye-delta or delta-wye the low voltage winding lags the high voltage winding by 30 degrees. Installing the isolation transformer with

the primary delta-secondary wye between the point of common coupling and the “PQ” converter line reactor provides a phase shift with the primary leading the secondary by 30 degrees. Installing the isolation transformer with the primary wye-secondary delta between the point of common coupling and the ”VDC” converter line reactor provides a phase shift with the primary lagging the secondary by 30 degrees. This arrangement of the isolation transformers provides 60 degrees of angular displacement between the two outputs of the back-to-back converters since a common supply feeds both isolation transformers.

Without the isolation transformers of Figure 14 the back-to-back converters through their respective reactor would be connected directly to the point of common coupling defined for the system. With back-to-back converters the zero sequence voltages (3^{rd}, 6^{th}, 9^{th}, etc.) due to PWM can cause currents to circulate between the two converters [12, p. 609]. The addition of isolation transformers will mitigate the transfer of common-mode noise. Additionally the angular displacement of 60 degrees cancels out the 3^{rd} harmonic currents between the back-to-back converters.

Transformer Power Rating [kVA]	75
Transformer Impedance [%]	4.96
X/R Ratio	1.2371
No Load Losses (Open-Circuit Test) [Watts]	300
Full Load Losses (Short-Circuit Test) [Watts]	2617
Transformer Resistance [Per-Unit]	0.0312
Transformer Reactance [Per-Unit]	0.0386
Base Primary Winding Resistance [ohms]	9.216
Base Primary Winding Reactance [ohms]	9.216
Base Primary Winding Inductance [henries]	0.0244
Base Secondary Winding Resistance [ohms]	3.072
Base Secondary Winding Reactance [ohms]	3.072
Base Secondary Winding Inductance [henries]	0.00815
Primary Winding Resistance [ohms]	0.14377
Primary Winding Leakage Reactance [ohms]	0.177869
Primary Winding Leakage Inductance [henries]	4.718116e-04
Secondary Winding Resistance [ohms]	0.047923
Secondary Winding Leakage Reactance [ohms]	0.05929
Secondary Winding Leakage Inductance [henries]	1.572705e-04
Magnetization Resistance [ohms]	2304
Magnetization Resistance [per-unit]	250
Magnetization Inductance [henries]	1.36105
Magnetization Inductance [per-unit]	55.68

Table 2 - 75 kVA Isolation Transformer Performance Data

3.2. Converter

Two 60 kW three-phase two-level voltage source converters were donated by Rockwell Automation. The converters are connected chassis to ground with the PE-A and PE-B jumpers removed. The PE-A jumper is the circuit for the MOVs and AC EMI capacitors phase to ground connection. The PE-B jumper is the circuit for the common mode capacitors to ground connection. The removal of these jumpers creates an open-circuit to ground.

3.3. DC Bus Connection

The converters were placed as close as possible to one another to minimize the connection length of the DC Bus to reduce the parasitic inductance of the bus structure and thus provide lower peak bus voltages during transient operation, but yet still allow for sufficient operating area for the fans in the converter.

3.4. Pre-Charge

A method of pre-charging the DC bus is necessary as to not to damage the DC Bus capacitors in the power structure of the converter. In addition to the DC Bus capacitors and IGBT section each converter contains a diode rectifier with controllable pre-charge resistor circuit that can be optionally used to limit the inrush current during the pre-charge sequence. The converter that was chosen to maintain the constant DC Bus voltage level utilized these additional parts of the power structure during pre-charge.

3.5. Voltage Divider and Virtual Neutral

For voltage based control of the converter the phase voltages must be measured by the GP-DSP. The phase voltages are used for detecting the grid voltage angle and thus establishing the phase-locked loop for each converter. The GP-DSP board has the hardware capabilities to measure three voltage inputs up to approximately 120VAC rms. Since the grid's typical phase voltage measurement of 277VAC rms exceed the hardware capability of the GP-DSP board a voltage divider was needed. A virtual neutral circuit was used to measure each phase voltage opposed to converting line voltage measurements to phase voltages within the DSP software.

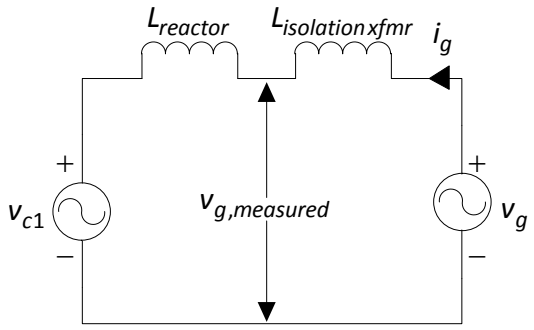

Figure 18 - One Line Diagram Representation of Converter, Impedance, and Grid

A multiple feedback 2nd order, low pass analog filter is implemented on the GP-DSP board layout for each voltage measurement circuit prior to the ADC. By measuring the phase voltages between the reactor and isolation transformer as depicted in Figure 18 the voltage harmonic spectrum produced by the converter is slightly attenuated by the ratio $Z_{isolation\,xfmr} \Big/ \left(Z_{isolation\,xfmr} + Z_{reactor} \right)$ which consist of the component impedances [23, p. 82]. Replacing the voltage measurement with a grid voltage estimator or virtual flux estimator [5, p. 453] was not considered since the measurement of the phase voltages by the GP-DSP board provided adequate filtering to firmly detect the grid voltage angle.

3.6. GP-DSP

The general purpose DSP board with a Texas Instruments TMS320F2812 was designed by Rockwell Automation in order to interface and control a converter's power structure. The ribbon cable between the Rockwell Automation converter and general purpose DSP board should be the same one supplied by Rockwell Automation that connects to the standard DSP provided with the converter.

3.7. Reactor Selection, DC Bus Level, and Converter Switching Frequency

There are multiple methods for the determining the actual component values of Figure 14. A typical method is to begin by determining the inductance of the reactor by selecting the range of current with emphasis on the nominal value the converter will need to handle (103), the grid voltage (104), and the maximum allowable total demand distortion [24, p. 487].

$$\begin{aligned} I_{nominal} &= 72.3\ [amps\ rms] \\ I_b &= 102.25\ [amps] \end{aligned} \tag{103}$$

$$\begin{aligned} V_{g,line-line} &= 480\ [volts\ rms] \\ V_b &= 391.92\ [volts] \end{aligned} \tag{104}$$

The worst case scenario for the harmonic current according to [25, p. 7] at the point of common coupling for Figure 14 is (105) where $I_{L,supply\,xfmr}$ represents the maximum demand load current and $I_{SC,supply\,xfmr}$ represents short-circuit current for the secondary of the supply transformer.

$$\begin{aligned} I_{limit,supply\,xfmr} &= 0.3\% \times I_{L,supply\,xfmr} \because \frac{I_{SC,supply\,xfmr}}{I_{L,supply\,xfmr}} < 20 \; and \; h \geq 35 \; and \; h = odd \\ &\approx 1.8\,[amps\ rms] \end{aligned} \tag{105}$$

The largest possible practical value of inductance is desired to provide the lowest current ripple [26, p. 54], [5, p. 435] since the current ripple is independent of the power being transferred [4, p. 232]. An estimate of current ripple for a converter utilizing space vector modulation connected to the grid through the system inductance is given in (106) [26, p. 56].

$$\Delta i_{\max} = \frac{V_{dc}}{24 f_s L} \tag{106}$$

To minimize the voltage drop across the reactor the maximum value of inductance is limited to 0.1 per unit [23, p. 56], [7, p. 142] with the voltage drop as a result of the resistance of the reactor considered negligible. The reactor purchased from MTE has a continuous current rating and inductance(107).

$$\begin{aligned} L_{reactor} &= 910\,[microhenries]\,(\pm 10\%) \\ I_{reactor} &= 83\,[amps] \end{aligned} \tag{107}$$

The per-unit value of inductance for the reactor is defined in (108) [2, p. 170].

$$L_{reactor,pu} = \frac{I_{nominal}\omega_b L_{reactor}\sqrt{3}}{V_{g,line-line}} \approx 0.09\,[pu] \tag{108}$$

In addition to the cancellation of harmonics generated by the converters the use of isolation transformers provides additional inductance to the system determined by(109) [27, p. 29].

$$\begin{aligned} L_{isolation\,xfmr} &= X_{pu}\frac{V_{g,line-line}{}^2}{\omega_b S_{isolation\,xfmr}} \because L_{pu} = X_{pu} \\ &\approx 314.54\,[microhenries] \end{aligned} \tag{109}$$

The maximum required bus voltage for (106) is chosen in order to find the worst case scenario of ripple current. Since the active (110) and reactive power (111) supplied or

consumed between the converter and grid is accomplished by controlling the phase angle θ and magnitude of the converter voltage with respect to the grid voltage [4, p. 496] the scenario where the converter needs to supply reactive power to the grid requires the highest bus voltage level (112).

$$P_g = V_g I_{g1} \cos\phi = \frac{V_g V_{c1} \sin\theta}{\omega_b L} \because \phi = \angle V_g - \angle I_{g1} \tag{110}$$

$$Q_g = V_g I_{g1} \sin\phi = \frac{V_g^2 - V_g V_{c1} \cos\theta}{\omega_b L} \because \phi = \angle V_g - \angle I_{g1} \tag{111}$$

$$\begin{aligned} V_{c1} &= \frac{V_{g,line-line}}{\sqrt{3}} + 2\pi f_g \left(L_{reactor} + L_{isolation\,xfmr} \right) I_{nominal} \cos\theta \\ &\approx 310.5 \text{ [volts rms]} \because \theta \approx 0 \end{aligned} \tag{112}$$

$$\begin{aligned} V_{c1} &= \frac{V_{g,line-line}}{\sqrt{3}} - 2\pi f_g \left(L_{reactor} + L_{isolation\,xfmr} \right) I_{nominal} \cos\theta \\ &\approx 255 \text{ [volts rms]} \because \theta \approx 0 \end{aligned} \tag{113}$$

By using (2) and assuming the maximum linear modulation index for SVM, the minimum DC bus voltage in order to meet the converter output phase voltage requirement when delivering reactive power to the grid is given in(114).

$$\begin{aligned} V_{dc,minimum} &= \hat{v}_{c1} \sqrt{3} \\ &\approx 760.6 \text{ [volts]} \end{aligned} \tag{114}$$

To account for variations in the grid voltage and simplification of the DC side base values in Appendix A: Per Unit Values, twice the base voltage was chosen for the DC bus voltage level(115).

$$\begin{aligned} V_{dc} &= 2V_b \\ &\approx 784 \text{ [volts]} \end{aligned} \tag{115}$$

To remain within the boundary determined by the total demand distortion of current the inductance of the system is given in (116) [28, p. 35], [29, p. 450].

$$L = \frac{V_{phase,h}}{h\omega_b I_{limit,supply\,xfmr}} \tag{116}$$

Since the inductance of the system and the maximum harmonic current are known, the worst case converter harmonic voltage magnitude $V_{phase,h}$ and order h must be determined for(116). The magnitudes of the voltage harmonic spectrum generated by the converter are dependent upon the pulse width modulation technique chosen while the order of the major sideband harmonics generated by the converter are determined by the converter switching frequency f_s and fundamental frequency f_o of the grid [30, pp. 289-290].

In order to minimize harmonic distortion and fully maximize the grid voltage supply for this installation synchronous double-edge symmetrical regular sampled space vector modulation was the technique chosen for the converter. The voltage harmonic spectrum in Figure 19 was calculated for space vector modulation single update, symmetrical, with a triangular carrier [30, pp. 276-290] at multiple converter switching frequencies using (117) and Table 3. The switching frequencies chosen were integer ratios of the fundamental frequency that would produce odd major sideband harmonics since even sideband harmonic currents are limited to 25% within their respective harmonic ranges [25, p. 7]. Double-edge asymmetrical regular sampled space vector modulation was only used for the model-in-the-loop simulation since difficulties arose in the actual implementation for the GP-DSP.

$$A_{mn} + jB_{mn} = \frac{V_{dc}}{\pi^2} \sum_{i=1}^{6} \int_{y_s(i)}^{y_e(i)} \int_{x_r(i)}^{x_f(i)} e^{j\left(\left[m+n\frac{\omega_o}{\omega_s}\right]x+ny'\right)} dx\,dy' \tag{117}$$

i	$y_s(i)$	$y_e(i)$	$x_r(i)$	$x_f(i)$
1	$\frac{2\pi}{3}$	π	$-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]$	$\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]$
2	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$-\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]$	$\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]$
3	0	$\frac{\pi}{3}$	$-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]$	$\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]$
4	$-\frac{\pi}{3}$	0	$-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]$	$\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y+\frac{\pi}{6}\right)\right]$
5	$-\frac{2\pi}{3}$	$-\frac{\pi}{3}$	$-\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]$	$\frac{\pi}{2}\left[1+\frac{3}{2}M\cos(y)\right]$
6	$-\pi$	$-\frac{2\pi}{3}$	$-\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]$	$\frac{\pi}{2}\left[1+\frac{\sqrt{3}}{2}M\cos\left(y-\frac{\pi}{6}\right)\right]$

Table 3 - Outer and Inner Double Fourier Integral Limits for SVM

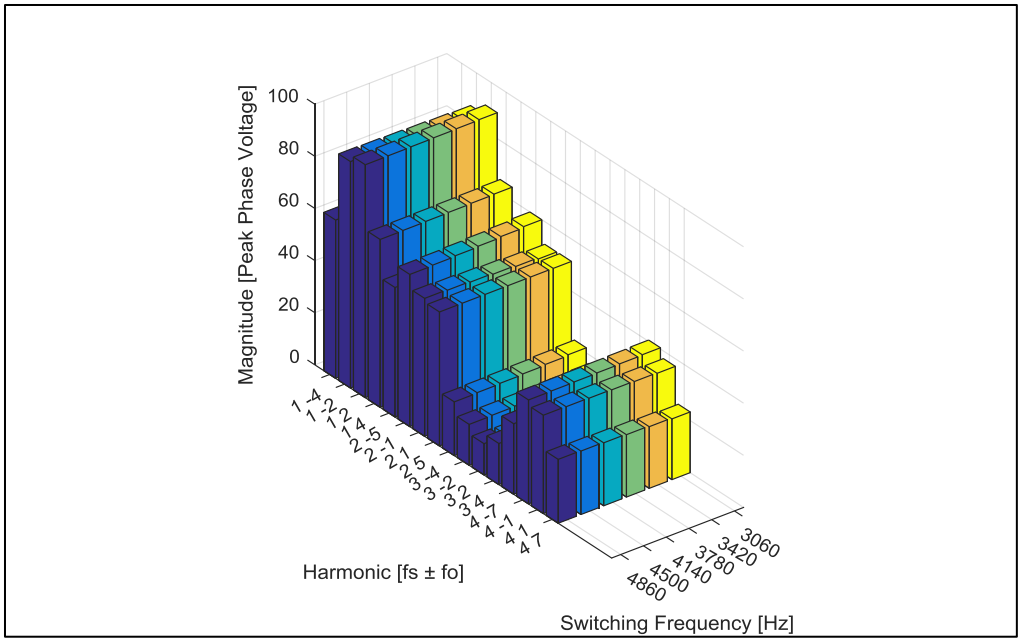

Figure 19 - Analytical Harmonic Voltage vs. Switching Frequency for Double-edge Symmetrical Regular Sampled SVM

With rearrangement of (116) the actual harmonic currents in Figure 20 can be calculated from the system inductance and converter harmonic voltage spectrum in Figure 19. Examination of the harmonic currents in Figure 20 show that the estimation in the minimum switching frequency falls on the border of 4500 or 4860 hertz in order to meet the harmonic current limits imposed at the secondary of the supply transformer for a single converter.

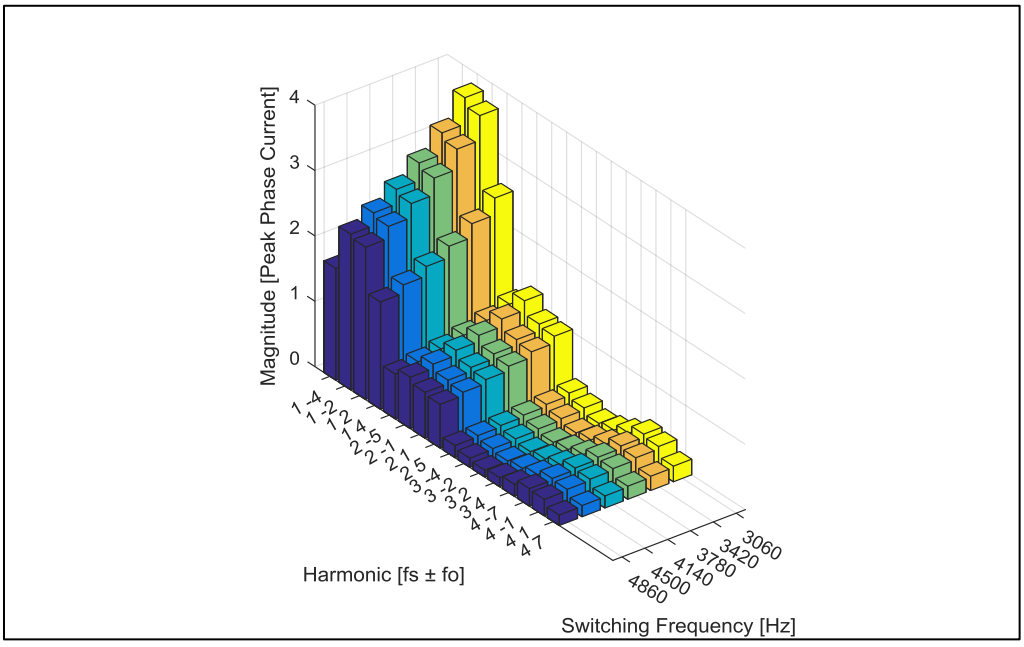

Figure 20 - Analytical Harmonic Current vs. Switching Frequency for Double-Edge Symmetrical Regular Sampled SVM

3.8. Control Overview

An overview of the power filtering topology and block diagram of the converter control schemes are shown in Figure 21.

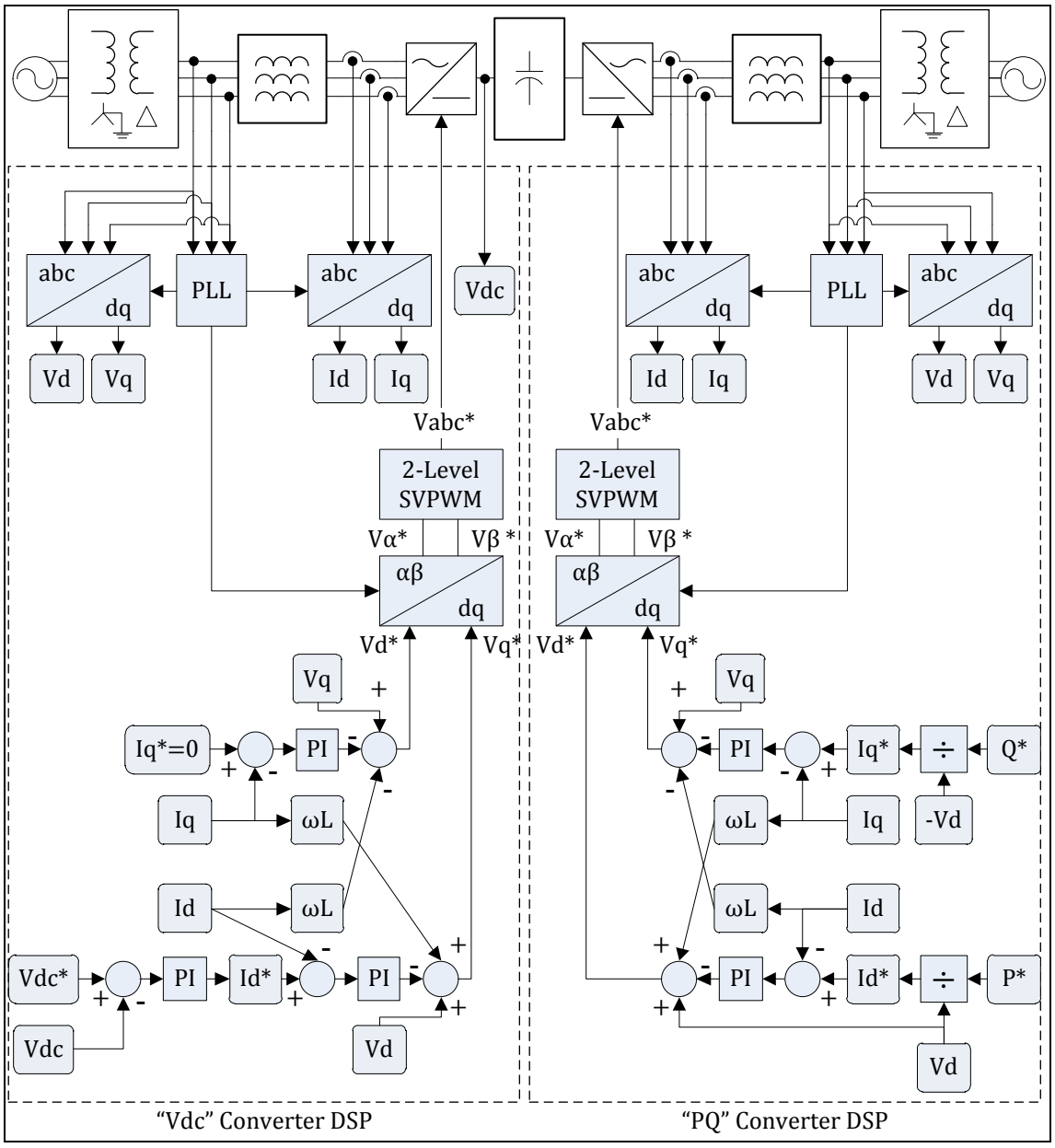

Figure 21 - Control Overview in Per-Unit

4. Simulation

The system parameters used for the frequency and time domain analysis of the current controller, voltage controller, and phase-locked loop as well as the continuous versus discrete controller implementations are listed in(118). The system parameters chosen are a result of the project implementation described in Chapter 3. The open loop response is used to evaluate the gain margin and phase margin, the closed loop response is used to determine the bandwidth and peaking, while the step response is used to measure the percent overshoot and rise time duration of the system [8, p. 42].

$$\begin{aligned} V_b &= 391.92\ [volts] \\ I_b &= 102.25\ [amps] \\ \omega_b &= 376.99\ [rad/sec] \\ L_{pu} &= 0.0895 \\ R_{pu} &= 0.0030 \\ C_{dc,pu} &= 34.68 \\ T_s &= 0.00020576\,[sec] \\ f_s &= 4860\,[Hz] \end{aligned} \tag{118}$$

4.1. Current Controller Frequency Domain Analysis

The optimization method modulus optimum described in Chapter 2.3.7 is used to derive the current controller proportional and integral gains as shown in the bold column of Table 4. The remaining proportional and integral gains listed in Table 4 are a result of substitutions for the damping ratio defined by modulus optimum. As can be seen in Figure 22 and Figure 23, increasing the switching frequency and processor update rate increases the proportional and integral gains at various damping ratios.

ζ	0.4	0.5	0.6	0.7	**0.707**	0.8	0.9	1
$K_{p,c}$	0.86288	0.55225	0.38350	0.28176	**0.27612**	0.21572	0.17045	0.13806
$K_{i,c\,discrete}$	0.00227	0.00145	0.00101	0.00074	**0.00073**	0.00057	0.00045	0.00036
$K_{c,c\,discrete}$	0.00263	0.00263	0.00263	0.00263	**0.00263**	0.00263	0.00263	0.00263
$T_{i,c}$	0.07836	0.07836	0.07836	0.07836	**0.07836**	0.07836	0.07836	0.07836
$K_{i,c}$	11.0115	7.0473	4.8940	3.5956	**3.5237**	2.7529	2.1751	1.7618

Table 4 - Current Controller Tuning Modulus Optimum at 4860 Hz Switching Frequency

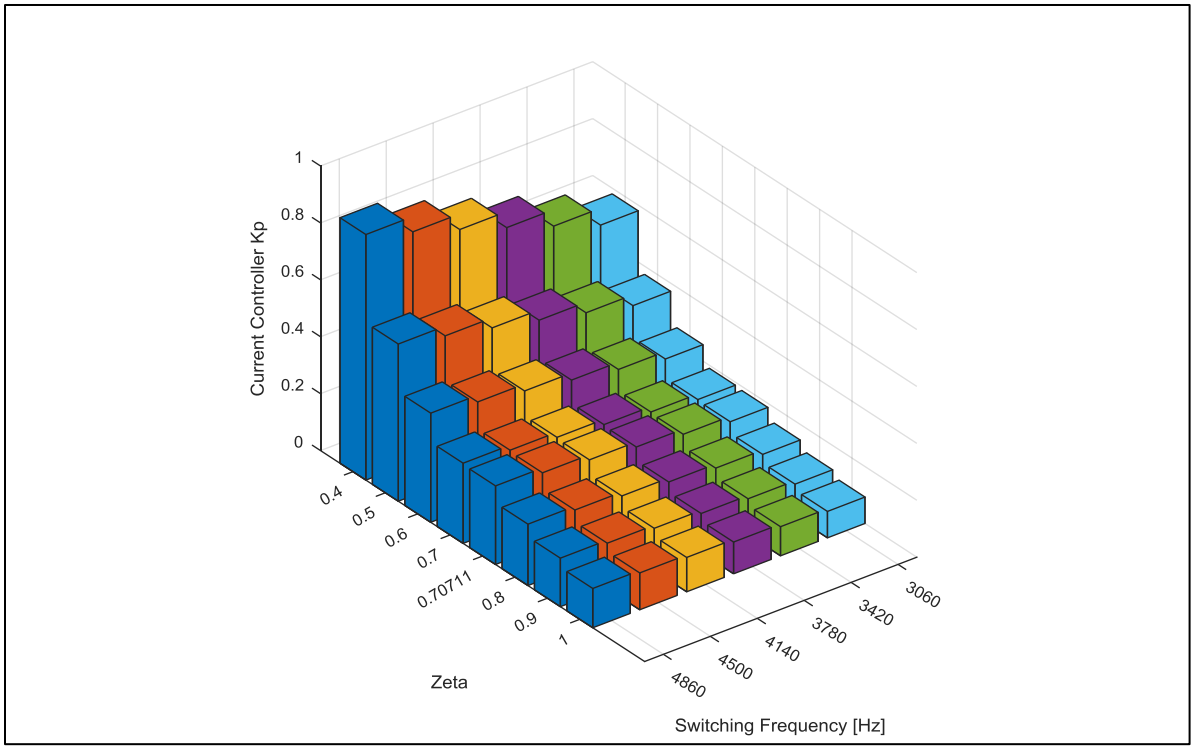

Figure 22 - Current Controller Proportional Gain versus Switching Frequency versus Damping Ratio

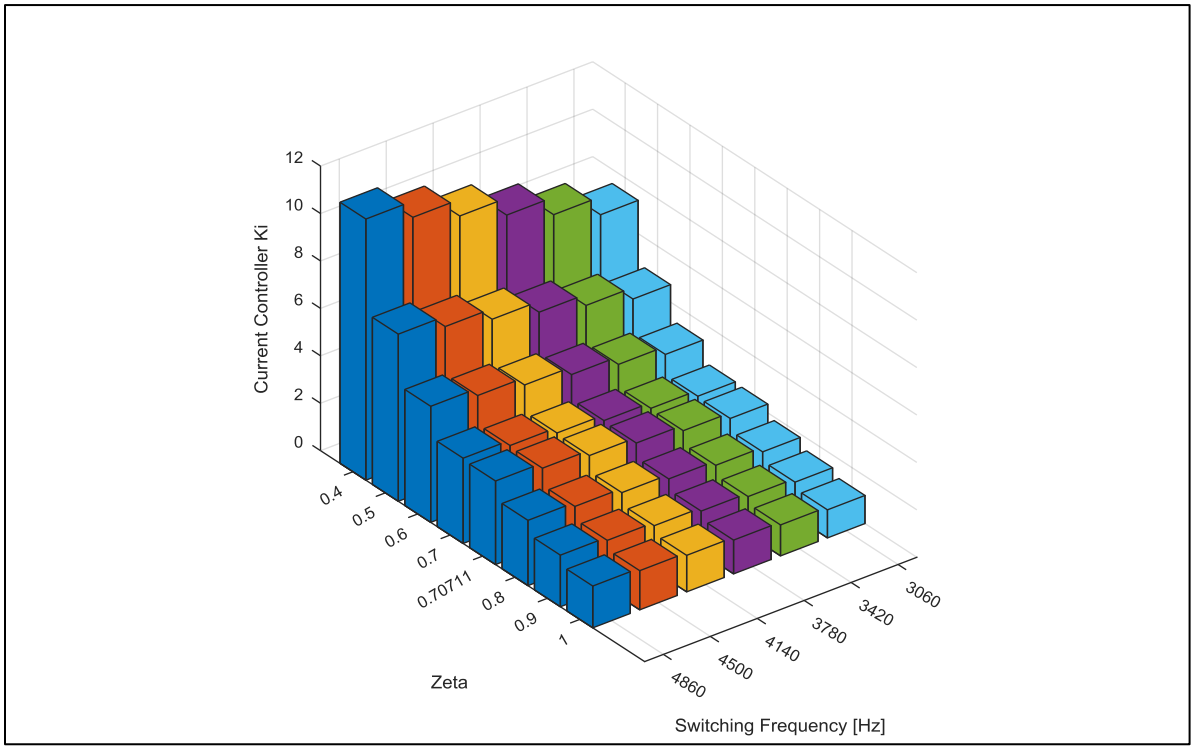

Figure 23 - Current Controller Integral Gain versus Switching Frequency versus Damping Ratio

The bode diagram of the current controller's open loop response to various damping ratios is used to determine the range of phase margin (Figure 24). The phase margin increases with an increase in the damping ratio as can be seen in Table 5. The current controller open loop transfer function (119) was derived with the modulus optimum proportional and integral gains.

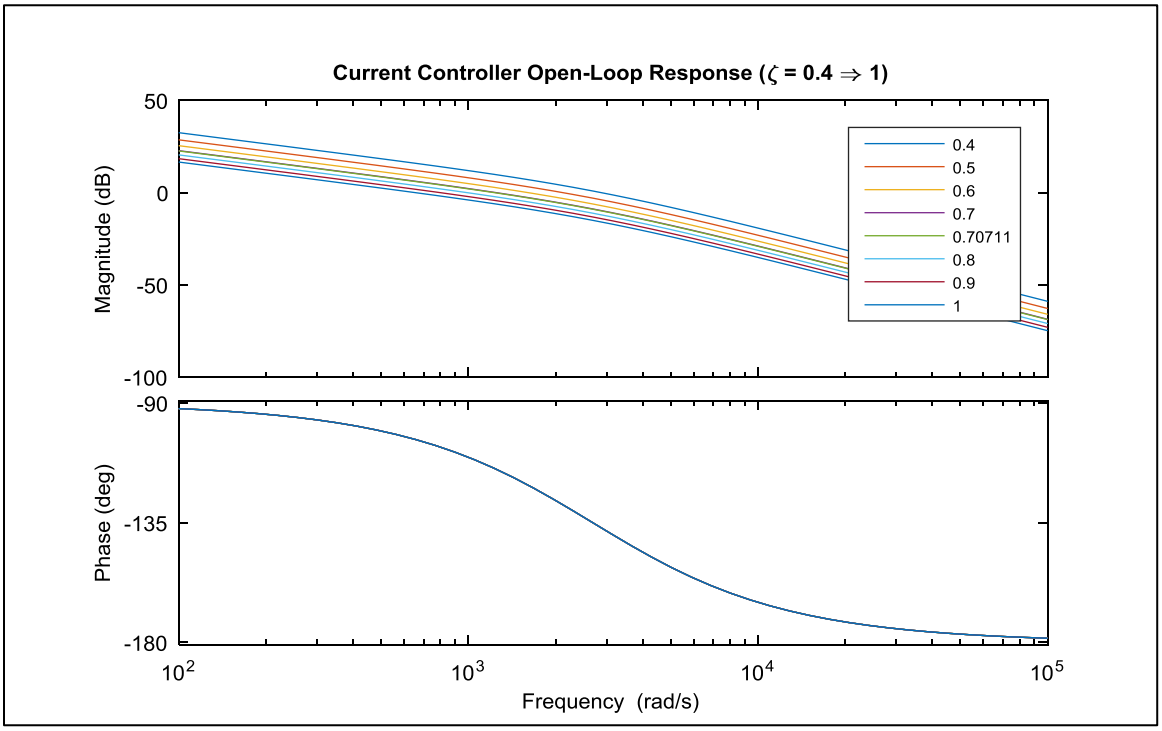

Figure 24 - Current Controller Open-Loop Response for Various Damping Ratios

ζ	0.4	0.5	0.6	0.7	**0.707**	0.8	0.9	1
Phase Margin [*degrees*]	43.14	51.83	59.19	65.16	**65.53**	69.86	73.51	76.35
Frequency @ Phase Margin [*rad / sec*]	2866.48	2111.58	1601.97	1243.58	**1222.36**	985.05	794.91	652.47

Table 5 - Current Controller Open-Loop Response for Various Damping Ratios

$$G_{cc,OL} = \frac{1343}{0.0003723s^2 + s} \because \zeta = 0.707$$
$$Phase\ Margin = 65.53\,[degrees]\,@\,1222.36\,[rad\,/\,sec] \quad (119)$$
$$Gain\ Margin = \infty$$

The bode diagram of the current controller's closed loop response to various damping ratios is used to determine the range of bandwidth (Figure 25). The bandwidth decreases with an increase in the damping ratio as can be seen in Table 6. The current controller closed loop transfer function (120) was derived with the modulus optimum proportional and integral gains.

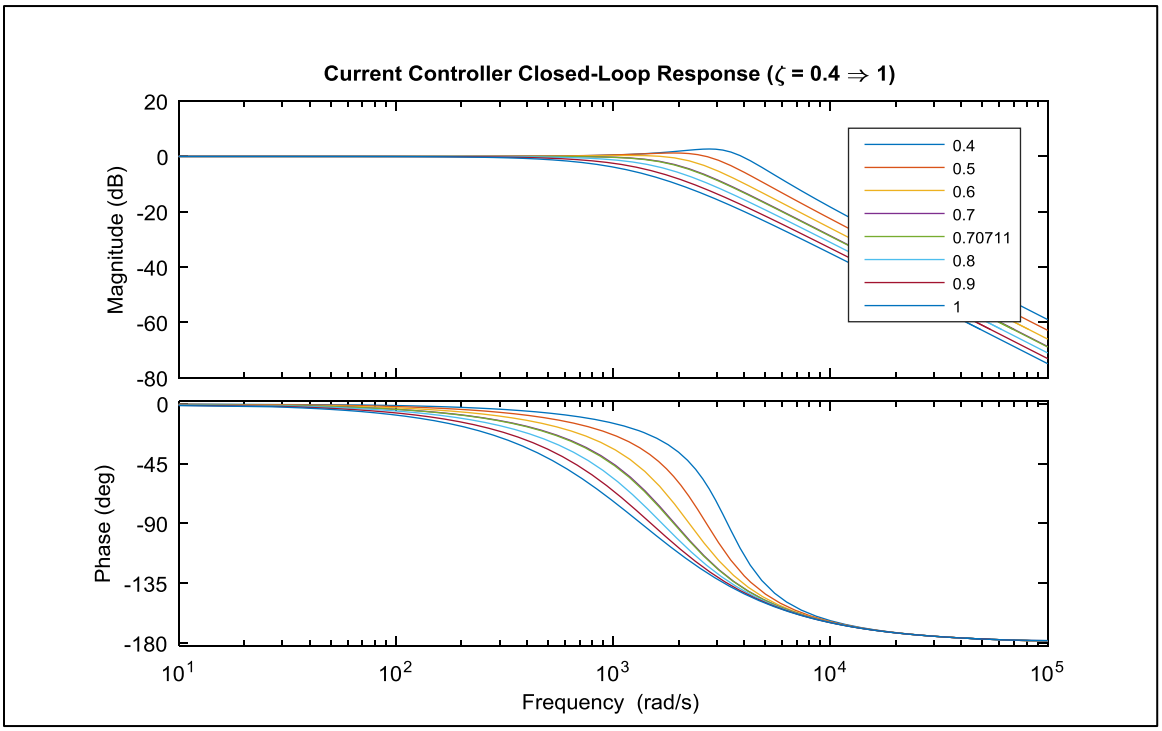

Figure 25 - Current Controller Closed-Loop Response for Various Damping Ratios

ζ	0.4	0.5	0.6	0.7	**0.707**	0.8	0.9	1
Bandwidth [*rad / sec*]	4612.51	3414.38	2567.90	1935.58	**1897.02**	1459.80	1111.26	862.59
Undamped Natural Frequency [*rad / sec*]	3357.47	2685.98	2238.31	1918.56	**1899.27**	1678.74	1492.21	1342.99
Damped Natural Frequency [*rad / sec*]	3077.17	2326.12	1790.65	1370.12	**1342.99**	1007.24	650.44	NA
Resonant Frequency [*rad / sec*]	2623.17	1896.58	1180.79	0	**0**	0	0	0
Resonant Peak [*dB*]	2.66	1.25	0.35	0	**0**	0	0	0

Table 6 - Current Controller Closed-Loop Response for Various Damping Ratios

$$G_{cc,CL} = \frac{1}{2.772\text{e-}7s^2 + 0.0007446s + 1} \because \zeta = 0.707$$

$$Bandwidth = \omega_n\left[\left(1-2\zeta^2\right)+\sqrt{4\zeta^4-4\zeta^2+2}\right]^{1/2} = 1897.02\,[rad/sec]$$

$$Undamped\ Natural\ Frequency\ (\omega_n) = 1899.27\,[rad/sec] \quad (120)$$

$$Resonant\ Frequency\ for\ \zeta \le 0.707 = \omega_n\sqrt{1-2\zeta^2} = 0\,[rad/sec]$$

$$Resonant\ Peak\ for\ \zeta \le 0.707 = \frac{1}{2\zeta\sqrt{1-\zeta^2}} = 0\,[dB]$$

4.2. Current Controller Time Domain Analysis

The plot of the current controller's step response to various damping ratios is used to determine the percent overshoot and rise time duration (Figure 26). The percent overshoot decreases and the rise time duration increases with an increase in the damping ratio as can be seen in Table 7.

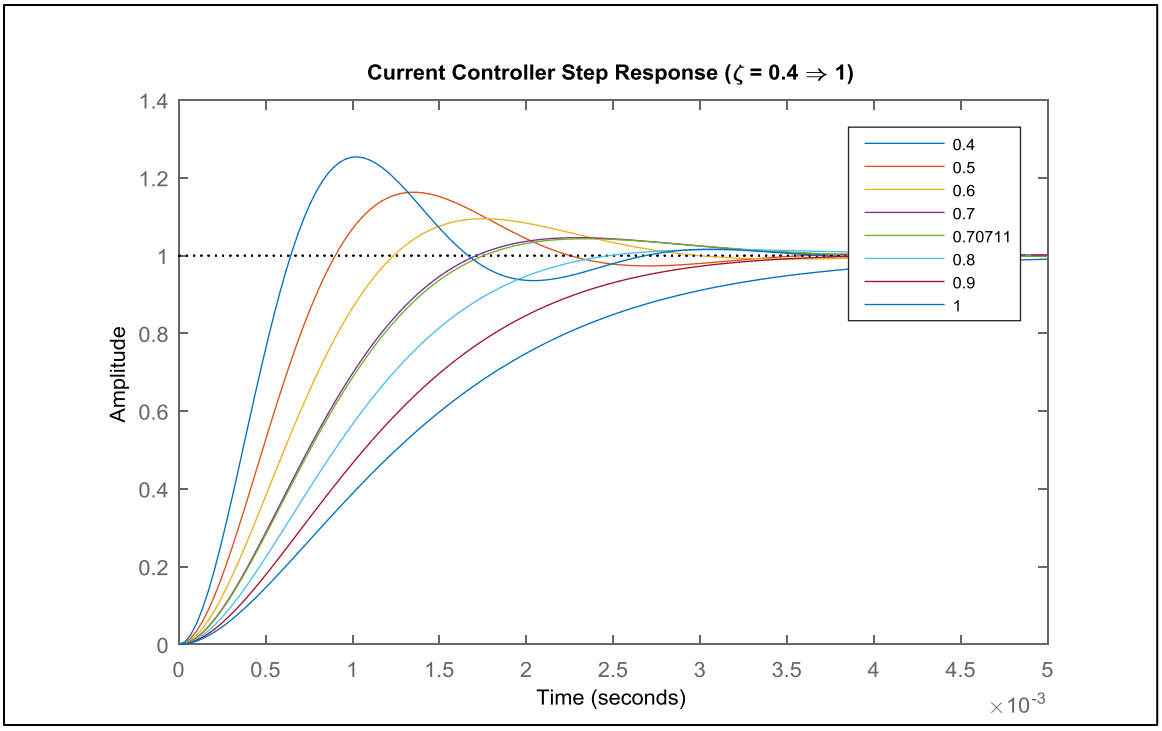

Figure 26 - Current Controller Step Response for Various Damping Ratios

ζ	0.4	0.5	0.6	0.7	**0.707**	0.8	0.9	1
Percent Overshoot [%]	25.37	16.29	9.48	4.60	**4.32**	1.52	0.15	0
Peak Time [*millisec*]	1.029	1.337	1.749	2.297	**2.332**	3.120	4.835	8.881
Settling Time (*Within* 2%) [*millisec*]	2.505	3.007	2.655	3.116	**3.139**	2.238	3.150	4.344
Rise Time Duration (10% *to* 90%) [*millisec*]	0.436	0.610	0.829	1.109	**1.131**	1.470	1.932	2.501

Table 7 - Current Controller Step Response for Various Damping Ratios

$$
\begin{aligned}
\textit{Percent Overshoot} &= 100e^{-\zeta\pi/\sqrt{1-\zeta^2}} = 4.321\,[\%] \because \zeta = 0.707 \\
\textit{Peak Time} &= \frac{\pi}{\omega_n\sqrt{1-\zeta^2}} = 2.339\,[\textit{millisec}] \\
\textit{Settling Time}\,(\textit{Within}\,2\%) &= \frac{4}{\zeta\omega_n} = 2.978\,[\textit{millisec}] \\
\textit{Rise Time Duration}\,(10\%\,\textit{to}\,90\%) &= \frac{1-0.4167\zeta+2.917\zeta^2}{\omega_n} = 1.139\,[\textit{millisec}]
\end{aligned}
\tag{121}
$$

4.3. Voltage Controller Frequency Domain Analysis

The optimization method symmetrical optimum described in Chapter 2.4.7 is used to derive the voltage controller proportional and integral gains as shown in the bold column of Table 8. The remaining proportional and integral gains listed in Table 8 are a result of substitutions for the normalizing factor α defined in part by symmetrical optimum. The normalizing factor defines the damping ratio for the second-order subsystem of the voltage controller. As can be seen in Figure 27 and Figure 28, increasing the switching frequency and processor update rate increases the proportional and integral gains at various normalizing factors.

α	$K_{p,c}$	$K_{i,c\,discrete}$	$K_{c,c\,discrete}$	$T_{i,c}$	$K_{i,c}$
2	**23.240**	**0.60403**	**0.02599**	**0.00792**	**2935.6**
2.2	21.127	0.45382	0.02148	0.00958	2205.5
2.414	19.253	0.34342	0.01784	0.01154	1669.0
2.5	18.592	0.30926	0.01663	0.01237	1503.0
2.6	17.877	0.27493	0.01538	0.01338	1336.2
2.7	17.215	0.24550	0.01426	0.01443	1193.1
2.8	16.600	0.22013	0.01326	0.01552	1069.8
2.9	16.028	0.19813	0.01236	0.01664	962.9
3.0	15.493	0.17897	0.01155	0.01781	869.8
3.5	13.280	0.11271	0.00849	0.02424	547.7
4.0	11.620	0.07550	0.00650	0.03167	366.9

Table 8 - Voltage Controller Tuning Symmetrical Optimum at 4860 Hz Switching Frequency

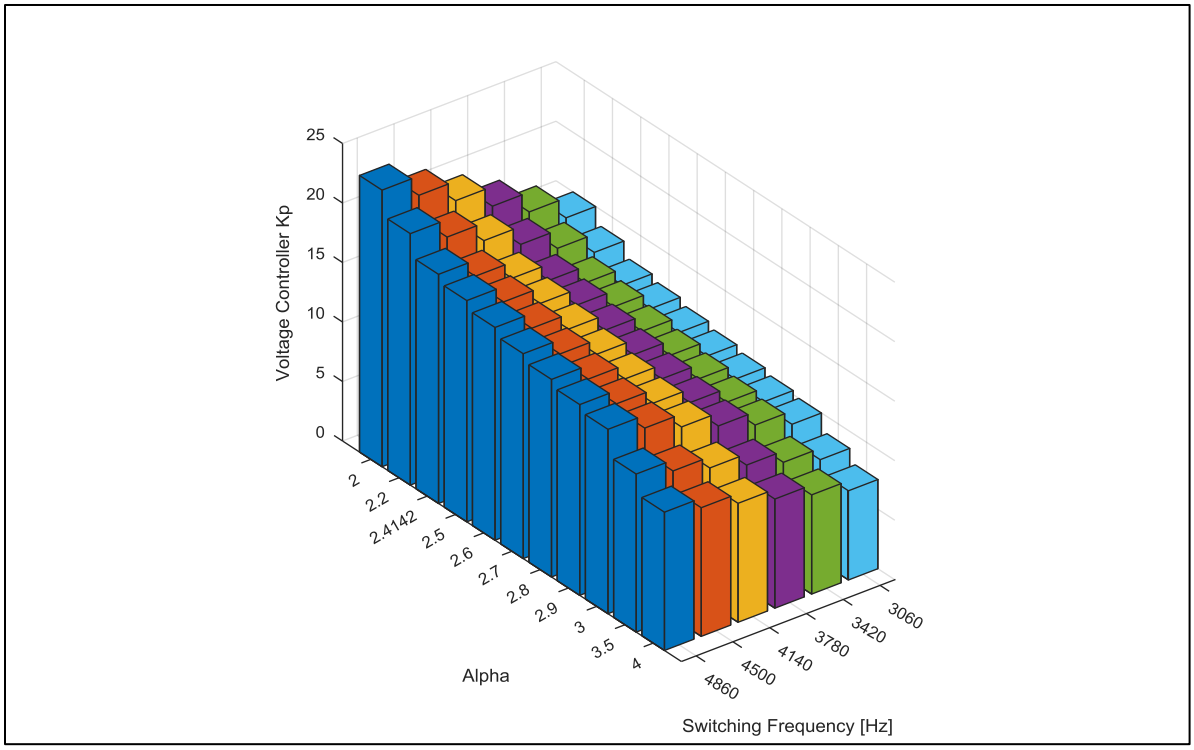

Figure 27 - Voltage Controller Proportional Gain versus Switching Frequency versus Normalizing Factor

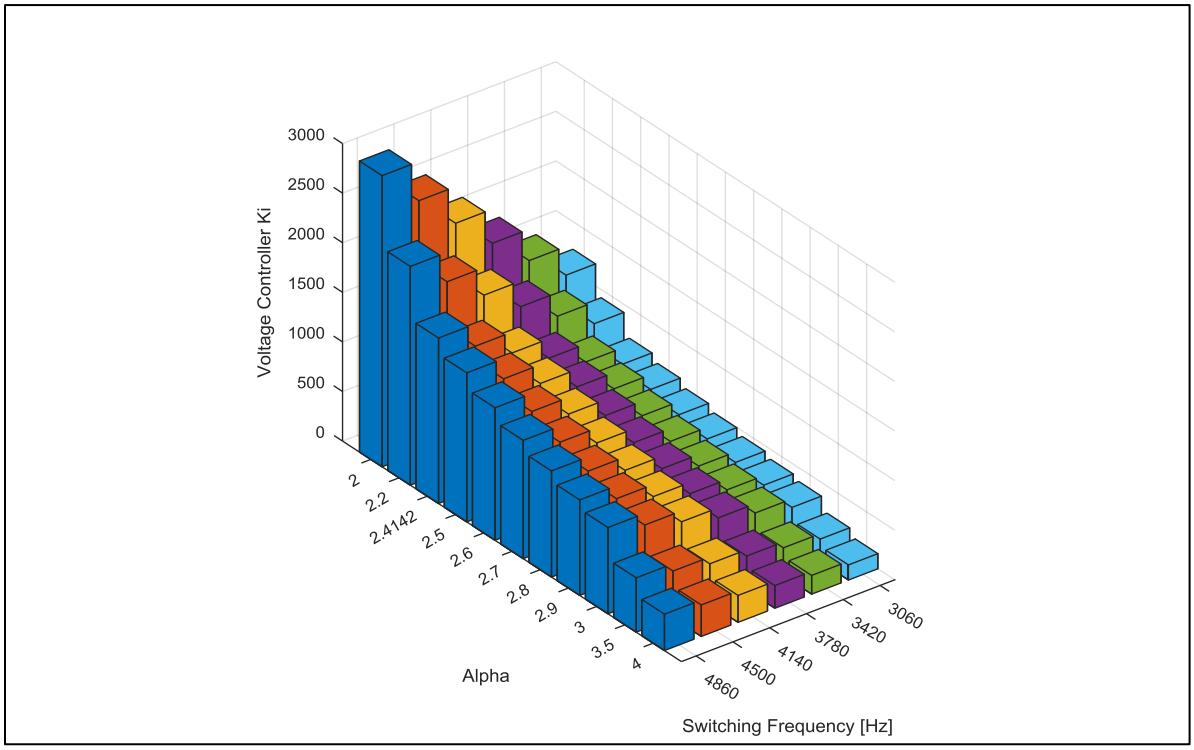

Figure 28 - Voltage Controller Integral Gain versus Switching Frequency versus Normalizing Factor

The bode diagram of the voltage controller's open loop response to various normalizing factors is used to determine the range of phase margin (Figure 29). The phase margin increases with an increase in the normalizing factor as can be seen in Table 9. The voltage controller open loop transfer function (122) was derived with the symmetrical optimum proportional and integral gains with a substitution of $\alpha = 4$ for the normalizing factor.

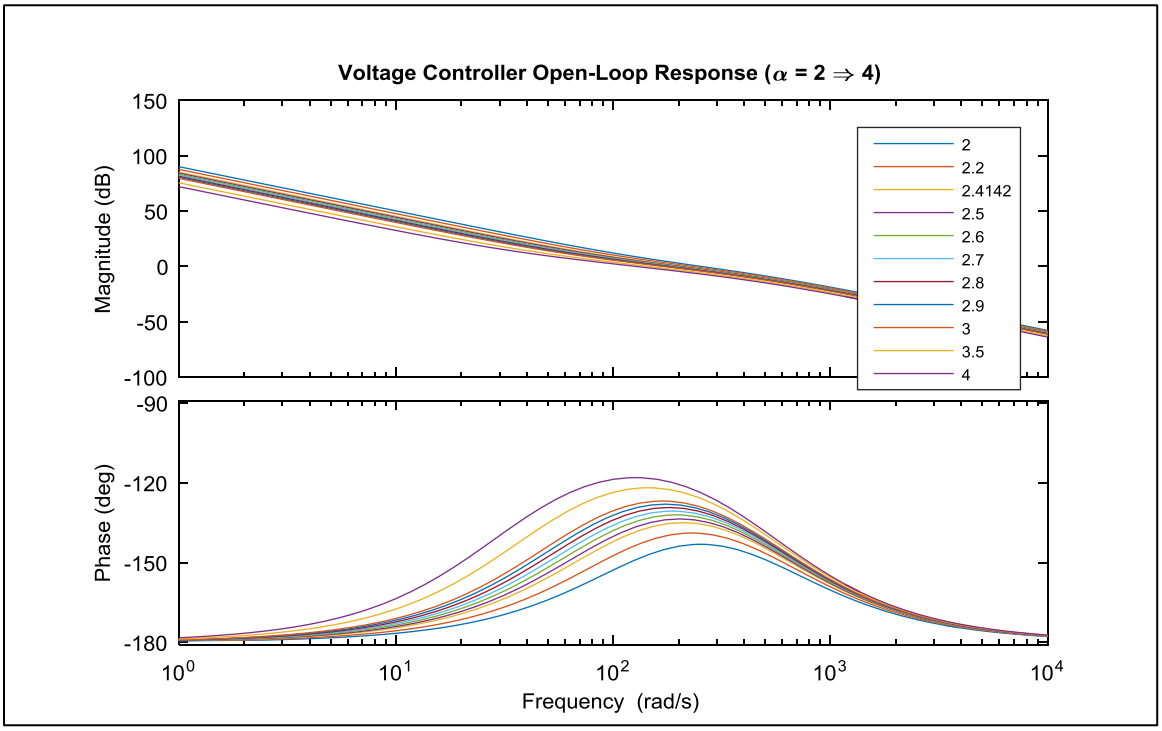

Figure 29 - Voltage Controller Open-Loop Response for Various Normalizing Factors

α	*Phase Margin* [*degrees*]	*Frequency@ Phase Margin* [*rad / sec*]
2	**36.870**	**252.630**
2.2	41.112	229.664
2.414	45.0	209.286
2.5	46.397	202.104
2.6	47.925	194.331
2.7	49.354	187.134
2.8	50.692	180.450
2.9	51.949	174.228
3.0	53.13	168.420
3.5	58.109	144.360
4.0	61.928	126.315

Table 9 - Voltage Controller Open-Loop Response for Various Alphas

$$G_{vc,OL} = \frac{0.03167s + 1}{4.962\text{e-}7s^3 + 0.0002507s^2} \because \alpha = 4.0 \qquad (122)$$
$$Phase\ Margin = 61.928\,[degrees]\,@\,126.315\,[rad\,/\,sec]$$

The bode diagram of the voltage controller's closed loop response to various normalizing factors is used to determine the range of bandwidth (Figure 30). The bandwidth decreases with an increase in the normalizing factor as can be seen in Table 10. The voltage controller closed loop transfer function (123) was derived with the symmetrical optimum proportional and integral gains. When the normalizing factor $\alpha \geq 3$ three real poles exist in Figure 31 and the oscillatory part of the response from the 2nd order subsystem is removed. By further increasing the normalizing factor to $\alpha = 4$ the bandwidth of the voltage controller in Table 10 is $\approx 1/10$ of the current controller bandwidth from Table 6. With the inner current controller 10 times faster than the outer voltage controller enough recommended margin is achieved for cascaded control [8, p. 52], [7, pp. 274-276].

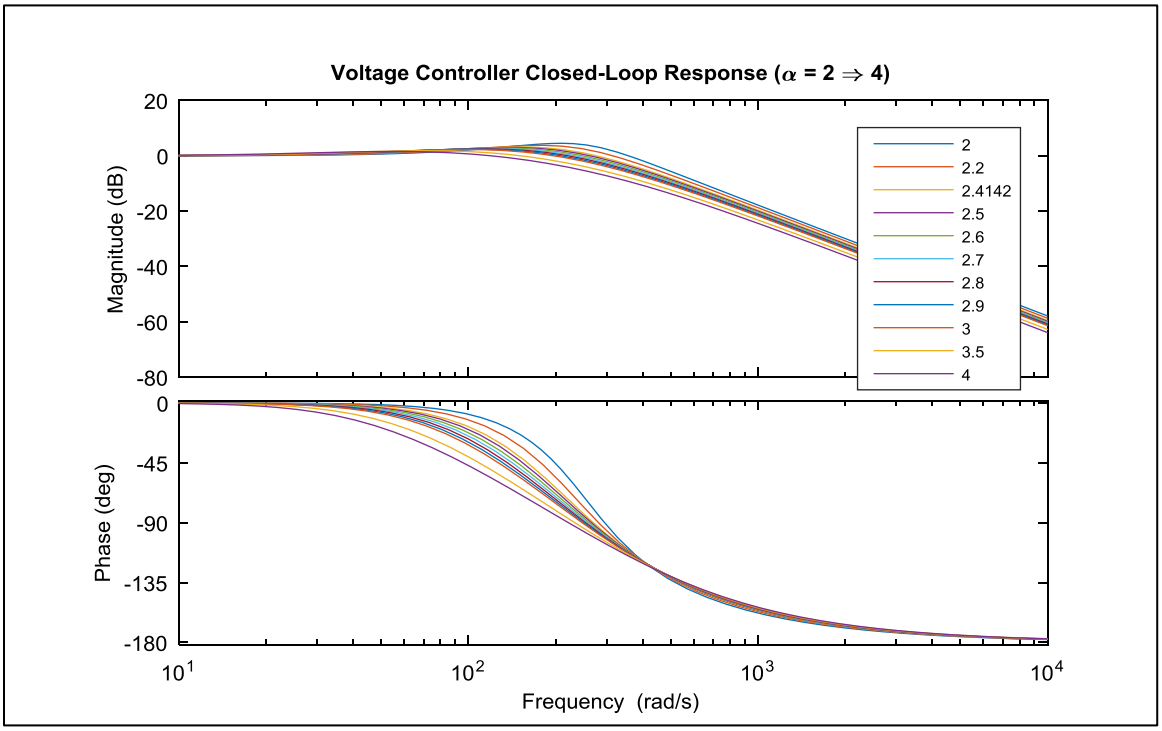

Figure 30 - Voltage Controller Closed-Loop Response for Various Normalizing Factors

α	*Bandwidth* [*rad / sec*]	*Resonant Frequency* [*rad / sec*]	*Resonant Peak* [*dB*]
2	**429.135**	**204.575**	**4.512**
2.2	389.764	170.028	3.757
2.414	353.369	139.269	3.170
2.5	340.211	128.609	2.981
2.6	325.778	117.253	2.784
2.7	312.243	106.939	2.610
2.8	299.535	97.546	2.453
2.9	287.592	88.955	2.310
3.0	276.358	97.154	2.272
3.5	229.193	72.180	1.845
4.0	193.718	48.248	1.537

Table 10 - Voltage Controller Closed-Loop Response for Various Alphas

$$G_{vc,CL} = \frac{0.03167s + 1}{4.962\text{e-}7s^3 + 0.0002507s^2 + 0.03167s + 1} \because \alpha = 4.0$$

$$Bandwidth = 193.718\,[rad / sec] \tag{123}$$

$$Resonant\ Frequency = 48.248\,[rad / sec]$$

$$Resonant\ Peak = 1.537\,[dB]$$

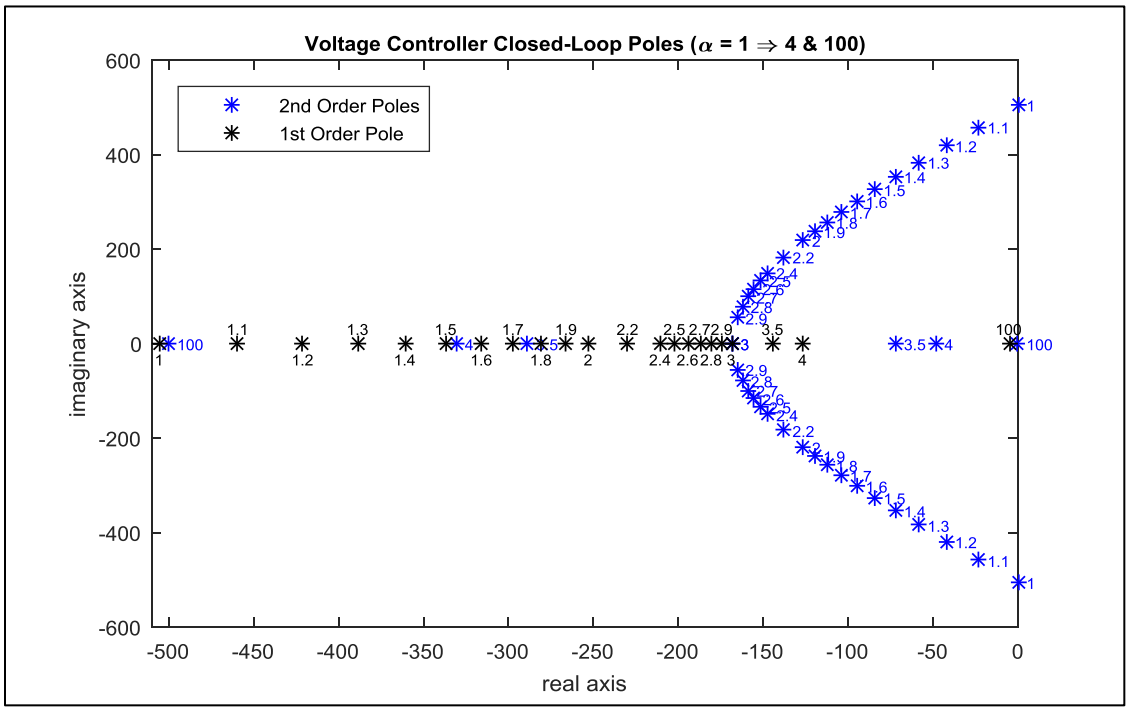

Figure 31 - Voltage Controller Closed-Loop Poles for Various Alphas

4.4. Voltage Controller Time Domain Analysis

The plot of the voltage controller's step response to various normalizing factors is used to determine the percent overshoot and rise time duration (Figure 32). The percent overshoot decreases and the rise time duration increases with an increase in the normalizing factor as can be seen in Table 11.

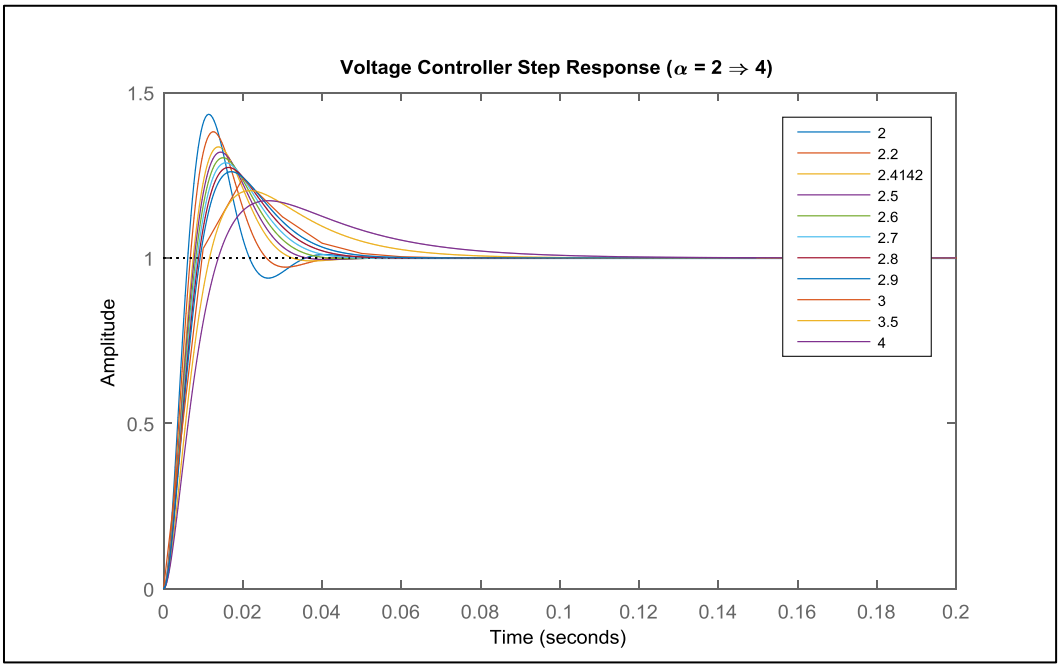

Figure 32 - Voltage Controller Step Response for Various Normalizing Factors

α	*Percent Overshoot* [%]	*Peak Time* [*millisec*]	*Settling Time* (*Within* 2%) [*millisec*]	*Rise Time Duration* (10% *to* 90%) [*millisec*]
2	**43.39**	**11.302**	**32.757**	**4.192**
2.2	38.13	12.699	34.811	4.656
2.414	33.55	13.692	29.478	5.167
2.5	31.97	14.279	31.691	5.378
2.6	30.29	15.107	34.466	5.629
2.7	28.75	15.634	37.411	5.881
2.8	27.34	16.447	40.481	6.137
2.9	26.06	16.972	43.633	6.397
3.0	24.58	20.000	47.925	7.780
3.5	20.34	21.692	63.441	8.045
4.0	17.31	26.459	80.970	9.529

Table 11 - Voltage Controller Step Response for Various Normalizing Factors

$$\begin{aligned} \textit{Percent Overshoot} &= 17.31\,[\%] \because \alpha = 4.0 \\ \textit{Peak Time} &= 26.459\,[\textit{millisec}] \\ \textit{Settling Time}\,(\textit{Within}\,2\%) &= 80.970\,[\textit{millisec}] \\ \textit{Rise Time Duration}\,(10\%\,\textit{to}\,90\%) &= 9.529\,[\textit{millisec}] \end{aligned} \tag{124}$$

4.5. Voltage Controller with Prefilter Time Domain Analysis

The plot of the voltage controller's step response with prefilter to various normalizing factors is used to determine the percent overshoot and rise time duration (Figure 33). The percent overshoot decreases and the rise time duration increases in comparison to Table 11 with the addition of the prefilter as can be seen in Table 12. Since the desired voltage controller characteristics were obtained during testing without the prefilter this technique was not part of the simulation, full system model, or the GP-DSP implementation.

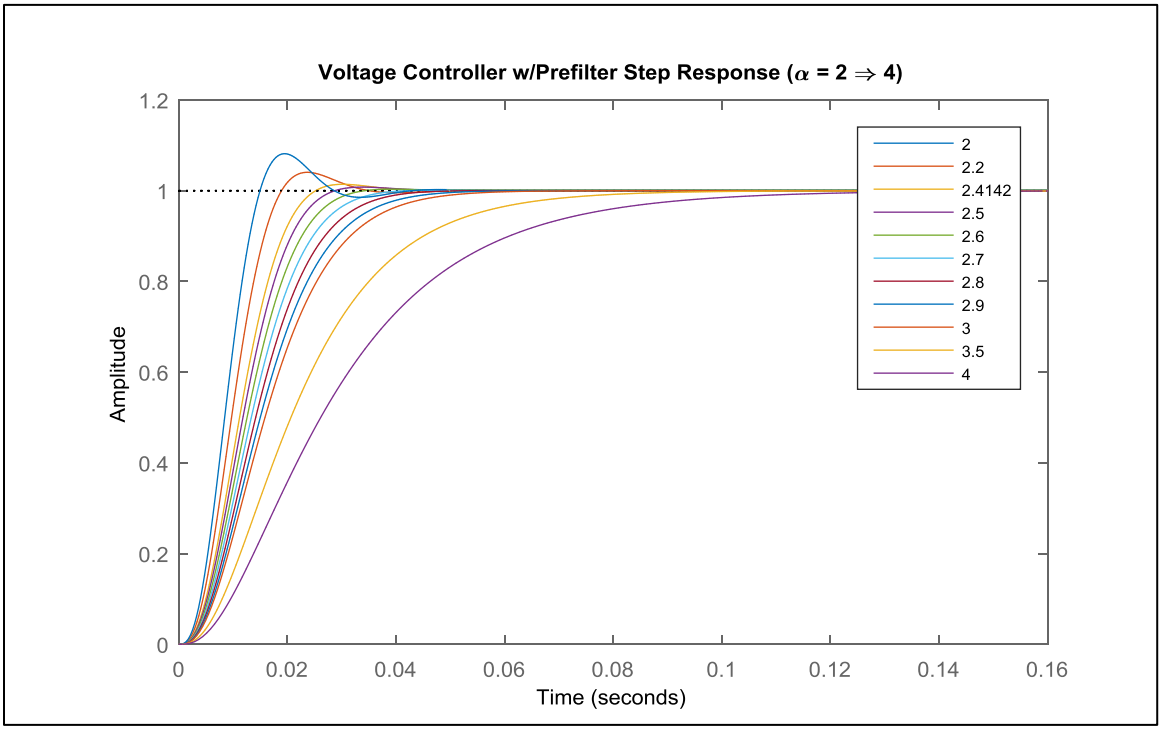

Figure 33 - Voltage Controller with Prefilter Step Response for Various Normalizing Factors

α	*Percent Overshoot* [%]	*Peak Time* [*millisec*]	*Settling Time* (*Within* 2%) [*millisec*]	*Rise Time Duration* (10% *to* 90%) [*millisec*]
2	**8.14**	**19.323**	**26.274**	**9.069**
2.2	4.04	23.728	29.352	11.289
2.414	1.40	30.185	23.147	14.197
2.5	0.77	33.723	25.641	15.528
2.6	0.31	39.397	28.897	17.201
2.7	0.08	47.481	32.491	18.996
2.8	0.00	56.429	36.355	20.908
2.9	0.00	83.191	40.417	22.932
3.0	0.00	92.420	44.634	25.061
3.5	0.00	111.333	67.709	37.091
4.0	0.00	174.268	94.320	51.317

Table 12 - Voltage Controller with Prefilter Step Response for Various Normalizing Factors

4.6. Phase-Locked Loop Frequency Domain Analysis

The optimization method symmetrical optimum described in Chapter 2.6.1 is used to derive the phase-locked loop proportional and integral gains in(125). The bode diagram of the PLL's open loop response is used to determine the phase margin (Figure 34). With stability the focus of the tuning for the PLL a normalizing factor of $\alpha = 10$ provided $\approx 80^\circ$ of phase margin.

$$
\begin{aligned}
G_{PLL} &= \frac{0.02058s + 1}{8.711\text{e-}9s^3 + 4.234\text{e-}5s^2} \because \alpha = 10.0 \\
K_{p,c} &= 486.0 \\
K_{i,c\,discrete} &= 4.86 \\
K_{c,c\,discrete} &= 0.01 \\
T_{i,c} &= 0.02058 \\
K_{i,c} &= 23619.60 \\
Phase\ Margin &= 78.6\,[degrees] @ 486\,[rad/sec]
\end{aligned}
\tag{125}
$$

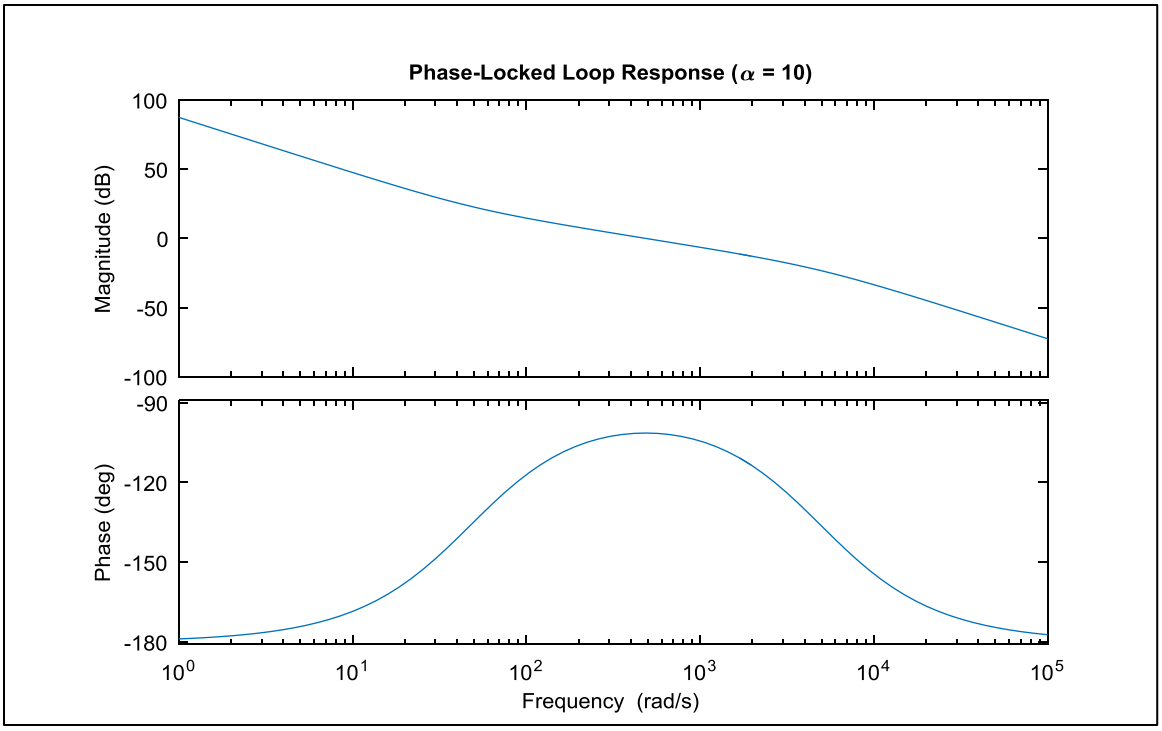

Figure 34 - Phase-Locked Loop Response for Normalizing Factor = 10.0

4.7. Continuous versus Discrete Time Domain Analysis

The current and voltage controllers as well as the PLL are defined in the continuous-time domain in Chapter 2. From the system parameters and the PI gains selected for the three control loops in Chapters 4 through 4.6, the simplified current and voltage controller models in Figure 8 and Figure 11 were then modeled in the continuous-time domain MathWorks Simulink environment as shown in Figure 35 and Figure 36.

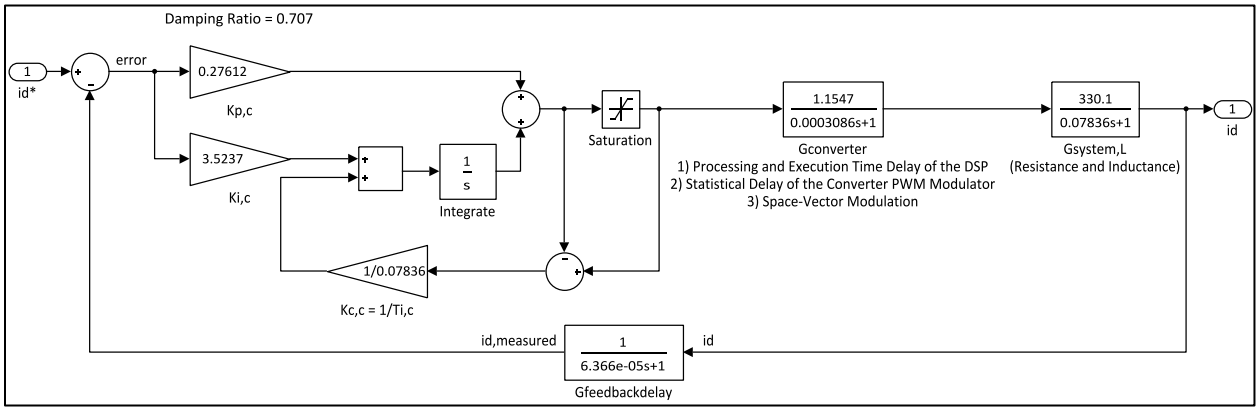

Figure 35 - Continuous Current Controller

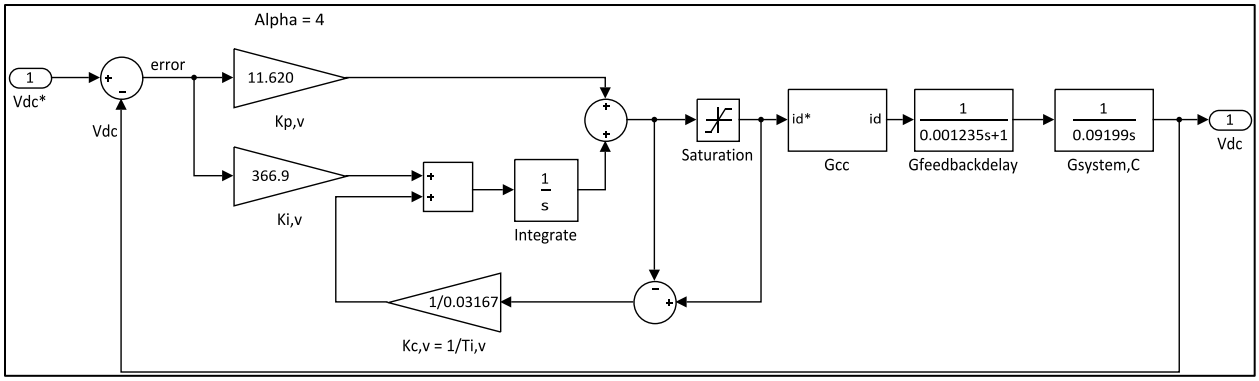

Figure 36 - Continuous Voltage Controller

To validate the control implementation for the GP-DSP board the discrete-time design of the three control loops is required. By using the appropriate discretization method, the transfer functions designed in the continuous-time domain can be transformed in the discrete-time domain. There are a number of discretization strategies to choose from; however, in this case a numerical integration method was selected. The numerical method known as trapezoidal (bilinear or Tustin) integration was chosen since replacement of the continuous-time computation of integrals with numerical approximations results in a 3% distortion limit as long as the ratio of sampling frequency to frequency of interest is greater than 10 [31, pp. 50-51]. The "c2d" function within the MathWorks MATLAB environment converts a continuous-time domain transfer function to the discrete-time domain equivalent. By using the "c2d" function and specifying the Tustin discretization method on the transfer functions of Figure 35 and Figure 36 two discrete control loops are realized as shown in Figure 37 and Figure 38.

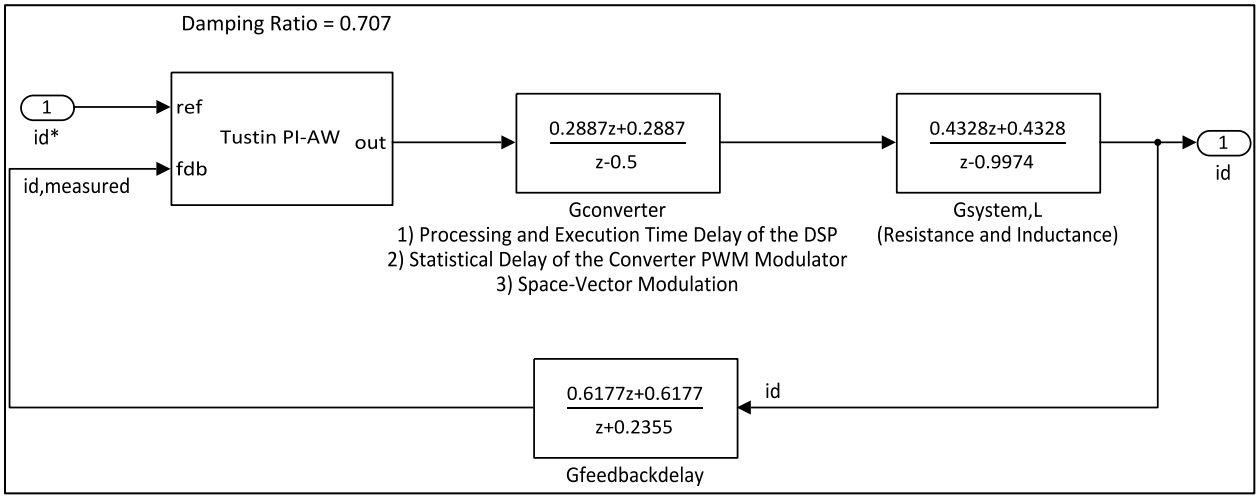

Figure 37 - Discrete Current Controller

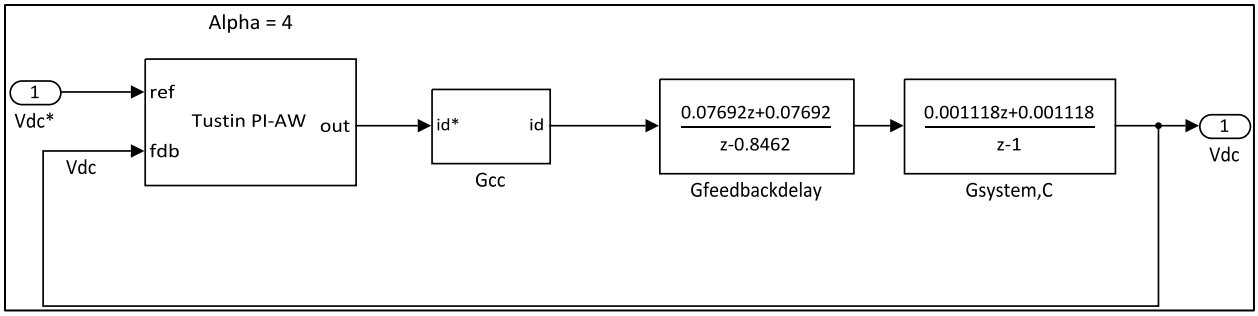

Figure 38 - Discrete Voltage Controller

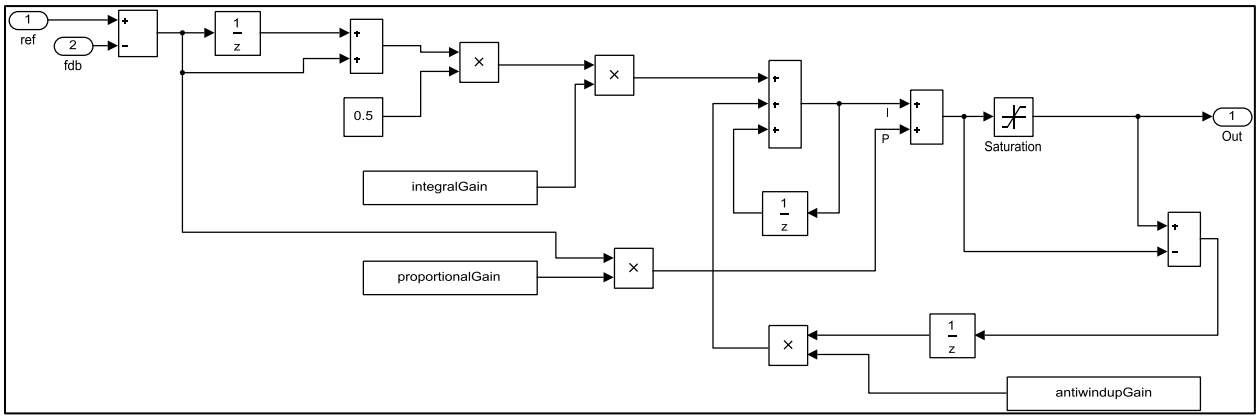

Figure 39 - Discrete Tustin PI Controller with Anti-Windup

The plot of the voltage controller's step response modeled in both the continuous and discrete-time domains with integrator anti-windup shows that the addition of a prefilter is unnecessary for the voltage controller (Figure 40).

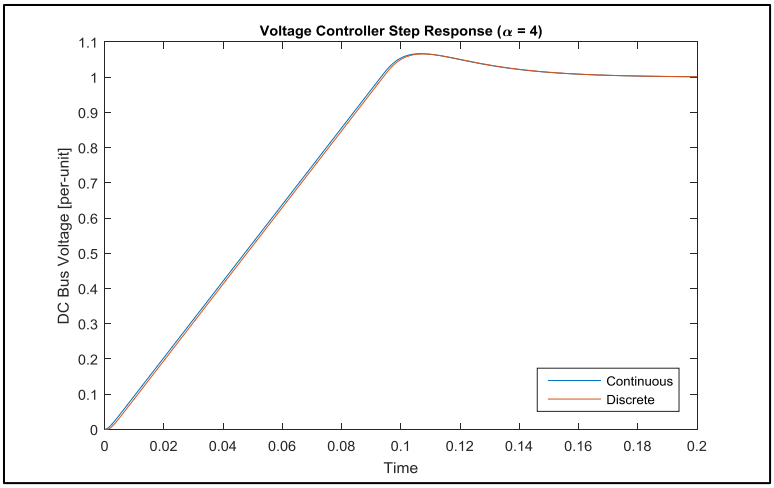

Figure 40 - Continuous vs. Discrete Voltage Controller Step Responses with Integrator Anti-Windup

5. TI C2000 Simulink Implementations and Testing

The control algorithms were developed for the “PQ” and “VDC” converters in the MathWorks Simulink 2014B environment. Along with the libraries MATLAB Coder, Simulink Coder, Embedded Coder with TI C2000 support package, and Fixed-Point Designer standalone C code is generated for the Texas Instruments C2000 processor family directly from Simulink. The TMS320F2812 is the fixed-point TI processor on the GP-DSP board. The standalone C code for the “PQ” and “VDC” converter is then downloaded to the TI processor with the Texas Instruments Code Composer version 5.5.0 software. The Spectrum Digital C2000 XDS510LC USB JTAG Emulator provides the connection between the GP-DSP board and the host computer. The JTAG emulation connection is used for debugging, downloading, and flashing the TI processor. Prior to deploying the “PQ” and “VDC” Simulink applications to standalone C code, model-in-the-loop testing was performed with the SimPowerSystems library. Development and testing the project’s system-level model was done to ensure proper operation and performance of the converters. Software-in-the-loop and processor-in-the-loop testing was omitted from this project.

5.1. “PQ” and “VDC” Converter Simulink Implementations

Both converter control implementations are detailed to show the minor differences between the “PQ” and “VDC” software.

5.1.1. Hardware Interrupt

The hardware interrupt is configured for the ADC in both the “PQ” and “VDC” control implementations. At the end of the GP-DSP’s analog to digital conversion, the ADC posts an interrupt that triggers the main subsystem to execute as shown in Figure 41 and Figure 42.

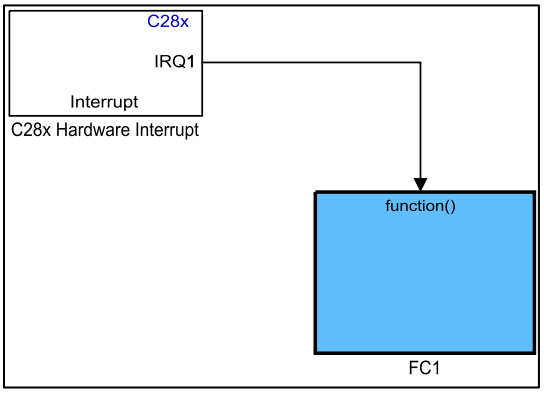

Figure 41 - “PQ” Converter Hardware Interrupt

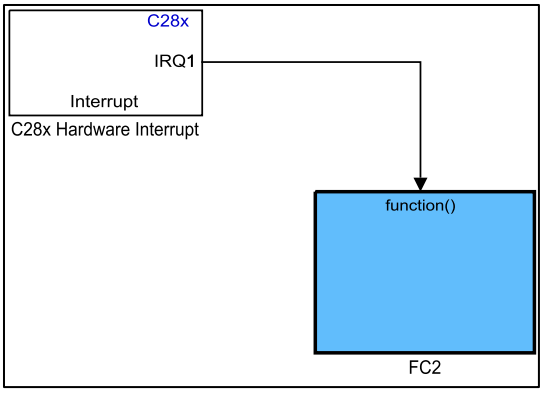

Figure 42 - "VDC" Converter Hardware Interrupt

5.1.2. Control Overview

The contents of the "FC1" main subsystem in Figure 41 provide the overview of the "PQ" converter control as shown in Figure 43 while the contents of the "FC2" main subsystem in Figure 42 provide the overview of the "VDC" converter control as shown in Figure 44. The "DiscreteInputs" subsystem configures the general-purpose I/O registers used to select the operation of shared pins for digital input. The purpose of the digital input associated with the "VDC" converter is to command the converter to charge the DC bus voltage to the desired level while the purpose of the digital input associated with the "PQ" converter is to command the converter to deliver and/or consume the desired amount of Active and/or Reactive power. Both the "PQ" and "VDC" digital inputs interface maintained switches located in the project installation.

Specifically, the digital input initiates the "Startup" subsystem and turns the converter fan on through the "DiscreteOutputs" subsystem. The "DiscreteOutputs" subsystem configures the general-purpose I/O registers used to select the operation of shared pins for digital output. The "Startup" subsystem provides a brief time delay prior to enabling the "Main" subsystem and disabling the "DisablePWM" subsystem which allows the converter to begin modulating. The "ADC" subsystem configures the 12-bit ADC to perform the analog-to-digital conversions on the signals representing the converter's phase voltages measured after the reactor and currents. The "PQ" GP-DSP board's ADC digitizes the analog signals associated with the Active and Reactive power references while the "VDC" GP-DSP board's ADC digitizes the analog signal associated with the DC bus voltage reference. The "Conversions" subsystem takes the digitized analog signals and converts the signals to per-unit representation. The "Main" subsystem provides the duty cycle reference to the pulse width modulator "PWM_A" block.

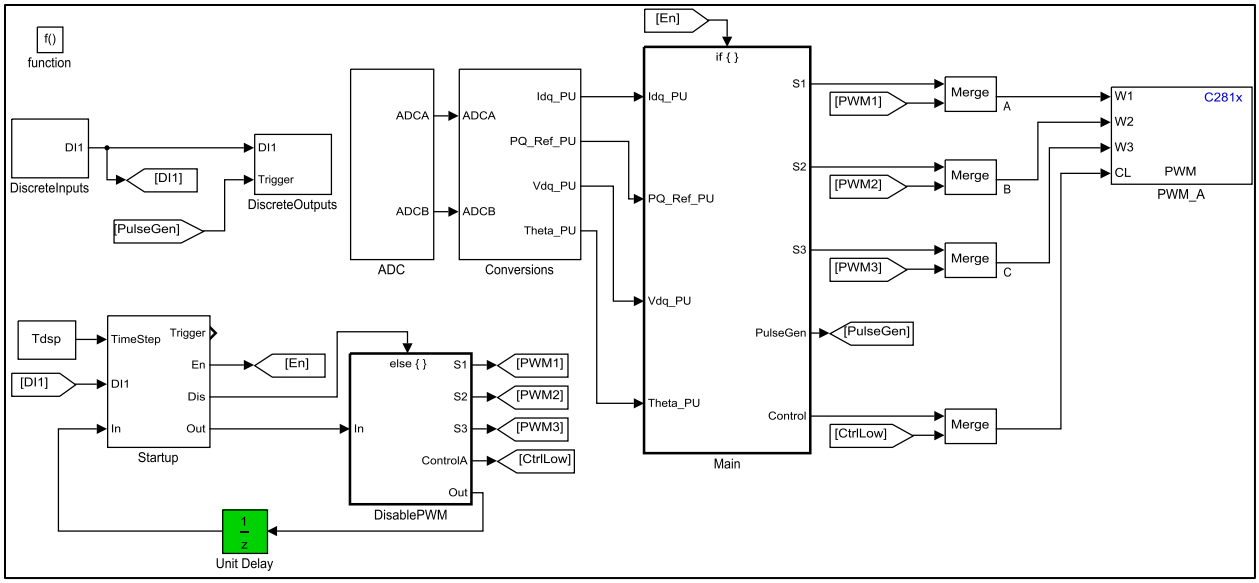

Figure 43 - "PQ" Converter Control Overview

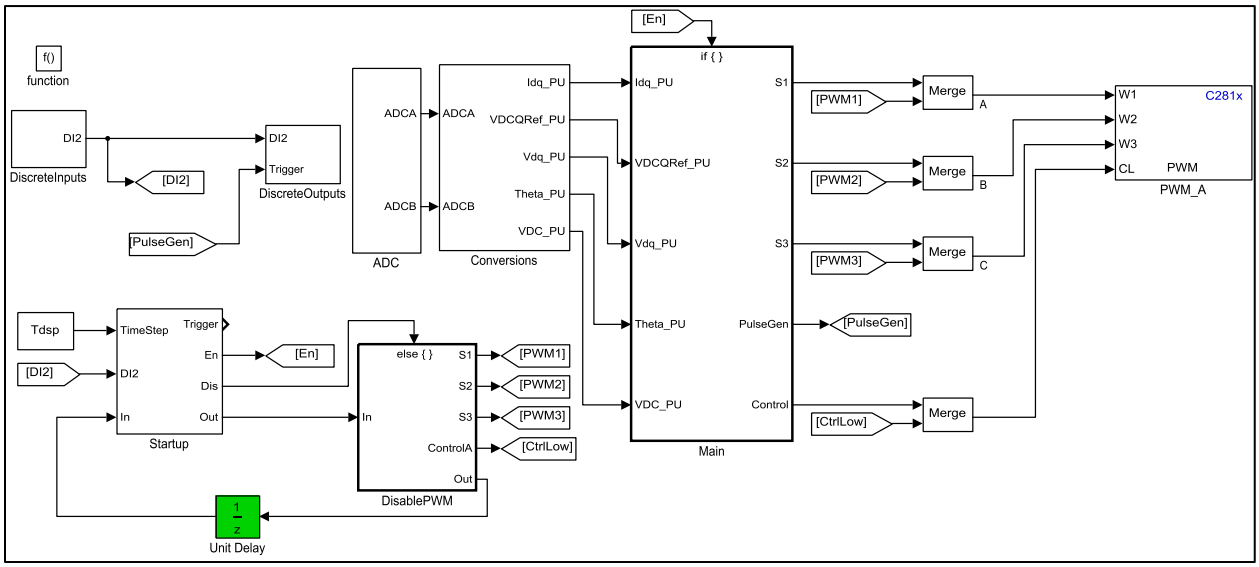

Figure 44 - "VDC" Converter Control Overview

5.1.3. Signal Conversions

The contents of the “Conversions” subsystem in Figure 43 show the digitized analog signals used for “PQ” converter control as shown in Figure 45 while the contents of the “Conversions” subsystem in Figure 44 show the digitized analog signals used for the “VDC” converter control as shown in Figure 46. Since the converter power structure was originally designed by the manufacturer for interfacing an induction motor when active power is flowing

from the converter to the motor the phase voltage and current are expected to be essentially aligned. Since the converters in this application are interfaced to the grid when active power is flowing from the converter to the grid the phase voltage and current are expected to be essentially 180° out of phase with one another. By adding the "Invert" subsystem the converter current sensing feedback is correctly applied to this application.

The "Convert4" and "Convert1" subsystems scale the digitized phase voltages and currents to per-unit representation. The "Convert5" and "Convert2" subsystems transform the per-unit phase voltage and currents from the *abc* stationary reference frame to the *dq* rotating reference frame. The "Convert6" subsystem is the phase-locked-loop which is used to detect the grid voltage angle. The "Convert3" subsystem scales the digitized Active and Reactive power references to per-unit representation as shown in Figure 45. The "Convert3" subsystem scales the digitized DC bus voltage reference to per-unit representation and the "Convert7" subsystem scales the digitized measured DC bus voltage to per-unit representation as shown in Figure 46.

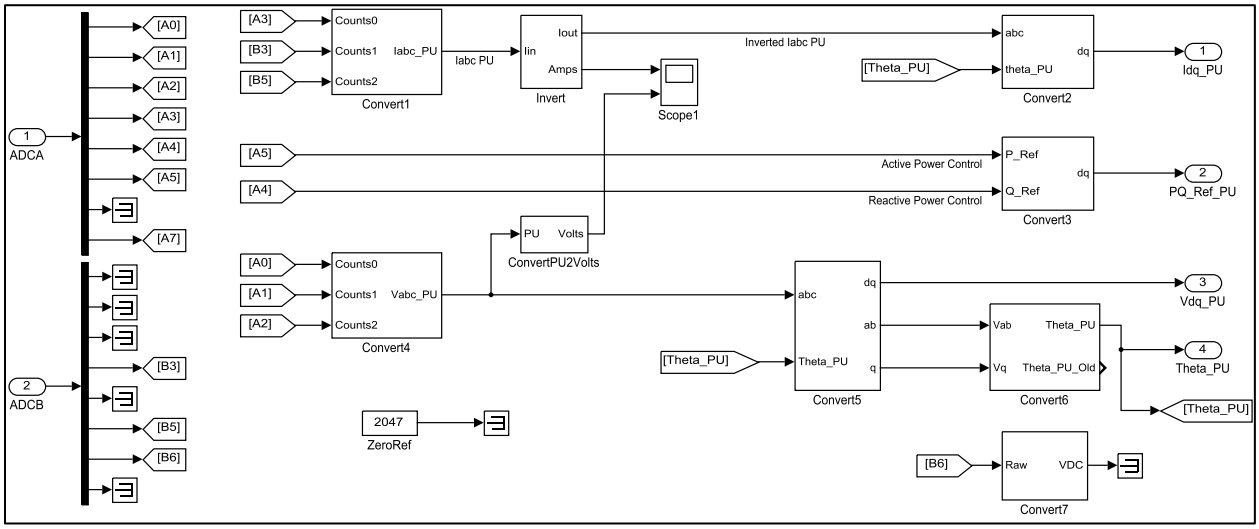

Figure 45 - "PQ" Converter Signal Conversions

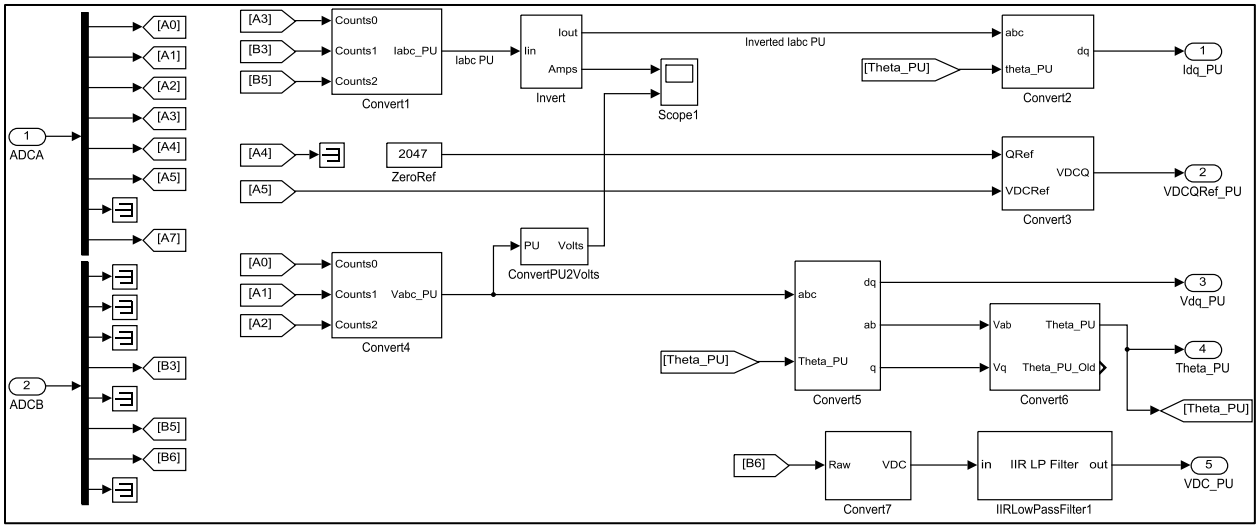

Figure 46 - "VDC" Converter Signal Conversions

The “IIRLowPassFilter1” subsystem filters the measured DC bus voltage. An IIR digital low pass filter in Figure 47 was chosen over an FIR digital low pass filter to conserve memory.

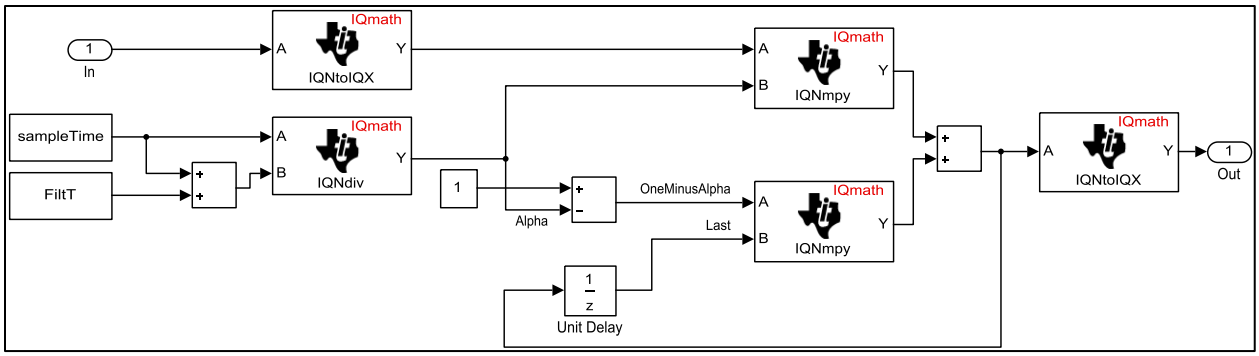

Figure 47 - “VDC" Converter IIR Low-Pass Filter for DC Bus Voltage

5.1.4. Decoupled Voltage Oriented Control and PWM References

The contents of the “DecoupledVOC” subsystem in Figure 48 represent the open loop Active and Reactive power references feeding the current controllers as shown in Figure 49.

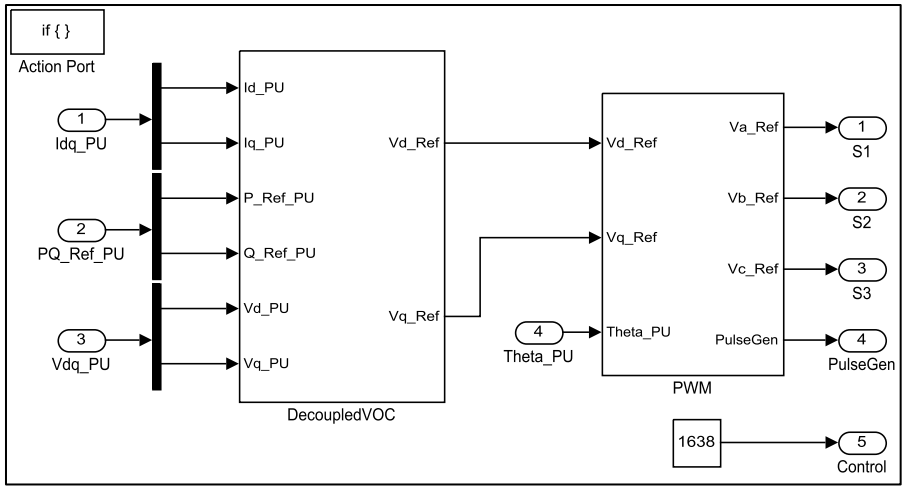

Figure 48 - "PQ" Converter Decoupled VOC and PWM References

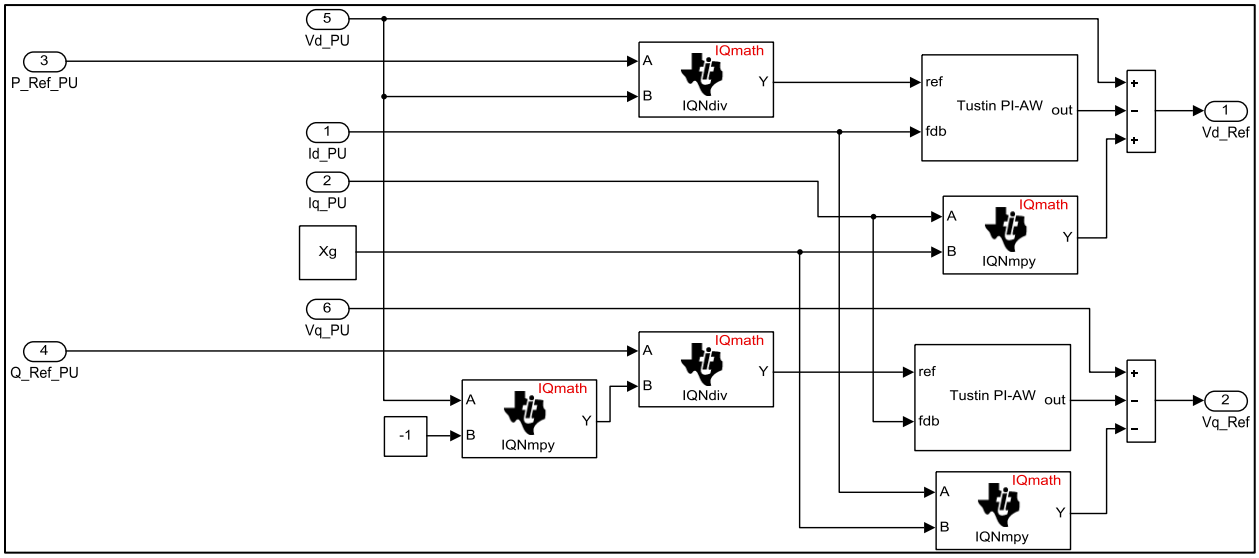

Figure 49 - "PQ" Converter Decoupled VOC

The contents of the “DecoupledVOC” subsystem in Figure 50 represent the outer voltage controller feeding the inner d-axis current controller as shown in Figure 51. The “IQsat” block in Figure 51 defines the minimum DC bus voltage reference as the peak of the line voltage.

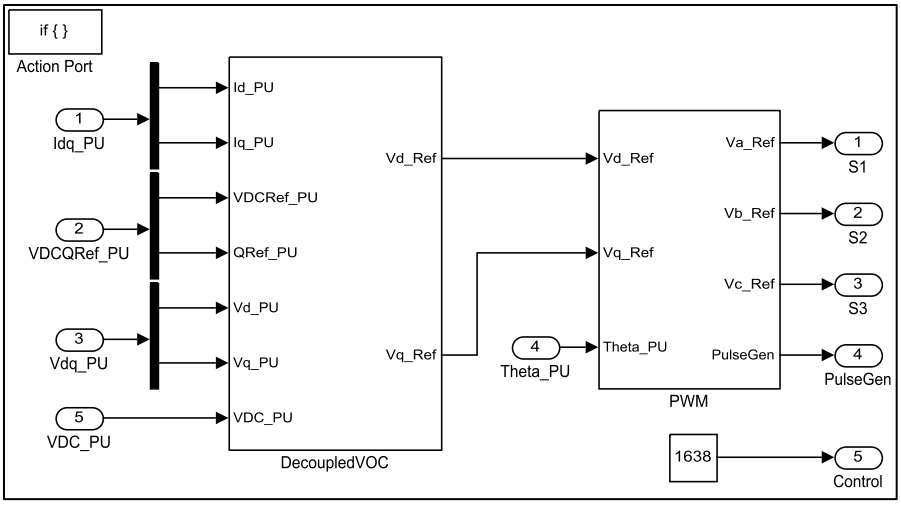

Figure 50 - "VDC" Converter Decoupled VOC and PWM References

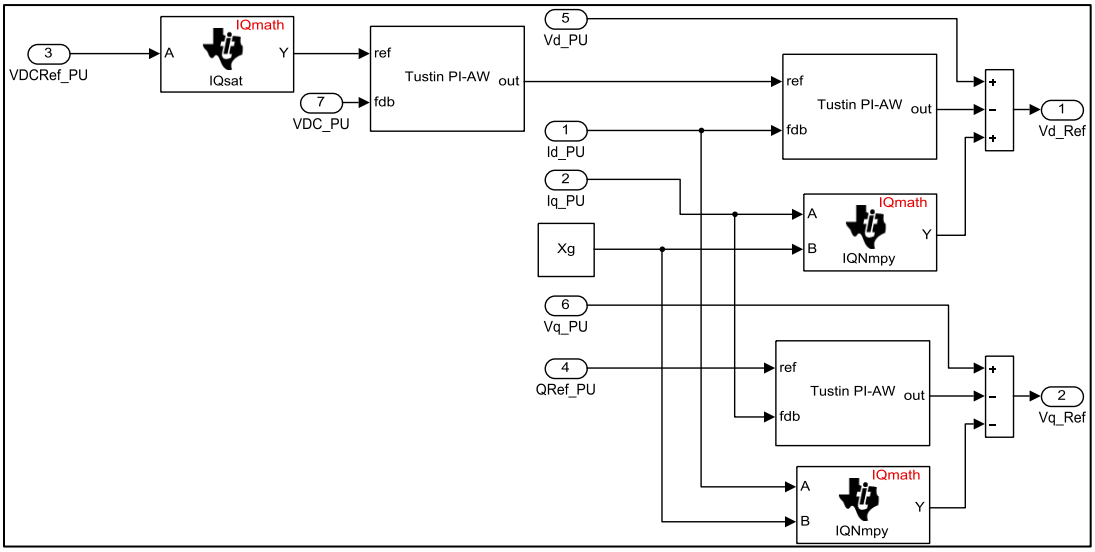

Figure 51 - "VDC" Converter Decoupled VOC

5.2. Common Functionality between "PQ" and "VDC" Simulink Implementations

The software common between the "PQ" and "VDC" converter control implementations is detailed in this section.

5.2.1. PWM References

The converter voltage reference is transformed from the *dq* rotating reference frame to the $\alpha\beta$ stationary reference frame with the inverse Park transformation "InvParkTrans" subsystem as shown in Figure 52. The space vector modulation "SVPWM" subsystem

transforms the converter voltage references from the $\alpha\beta$ stationary reference frame to the *abc* stationary reference frame. The remaining blocks and subsystems scale the *abc* stationary reference frame per-unit converter voltage reference to the TI C2000 PWM scaling requirements.

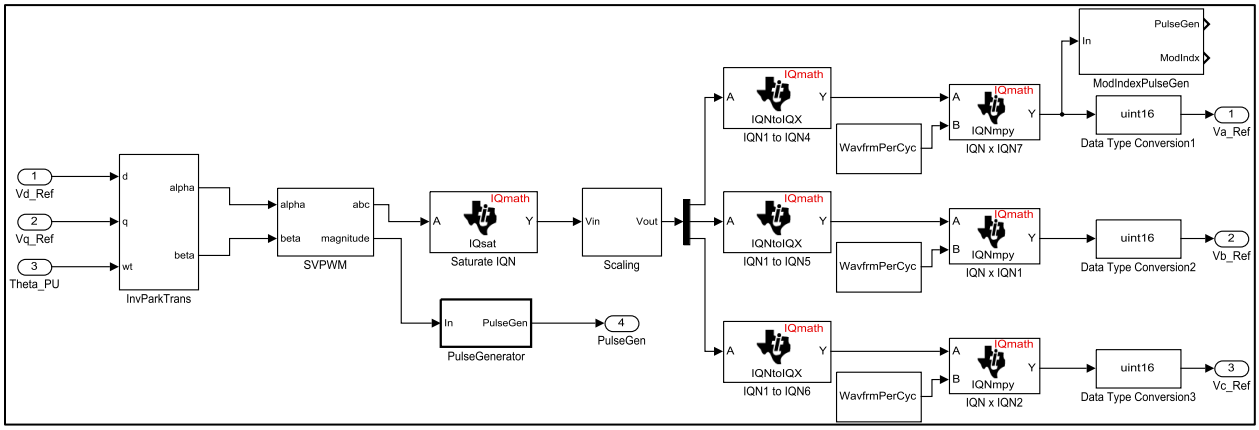

Figure 52 - Direct-Quadrature Voltage References to TI C2000 PWM References

5.2.2. PWM

The GP-DSP board interfaces the gate drivers in the converter's power structure through PWM module A. The "PWM_A" block in both Figure 43 and Figure 44 configure the module A Event Manager settings to generate the required waveforms. On the "Timer" tab of the "PWM_A" dialog box the "Waveform period" selects the switching frequency for the converter with the units "Waveform period units" defined in clock cycles (Figure 53). Clock cycles refer to the high-speed peripheral clock on the TMS320F2812 TI processor. The high-speed peripheral clock is 75MHz by default since the high-speed peripheral clock prescaler is set to 2 and the clock frequency is 150MHz. The "Timer prescaler" divides the clock input to produce the desired timer counting rate. Since "1/4" is selected from the pulldown menu the timer is set to 18.75MHz. Setting the "Waveform period" to 3,858 clock cycles defines a fixed switching frequency of essentially 4860 Hz. The "Waveform type (counting mode)" can be selected from the pulldown menu as either "Asymmetric (Up)" or "Symmetric (Up-down)" which produces a sawtooth or triangular carrier reference. A triangular carrier reference was selected since it is known to produce less harmonic distortion [30, pp. 223-225].

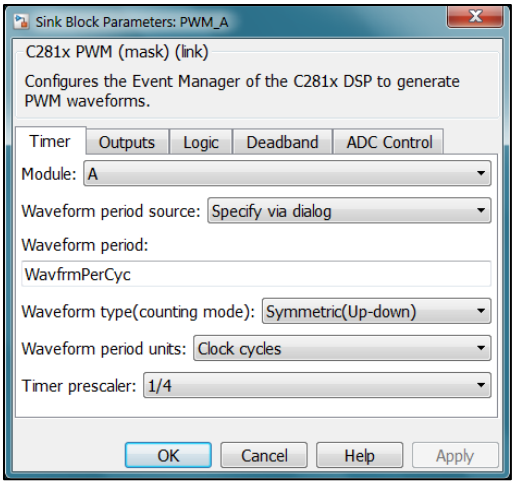

Figure 53 - PWM Switching Frequency

There is a short-circuit hazard associated with having both IGBTs of a single leg closed at the same time (Figure 54). To solve this only one IGBT in a leg is closed at a time. This is accomplished by feeding complementary PWM gating signals to each of the IGBTs in a leg so that when one IGBT is closed the other is open. When the converter is modulating the upper IGBTs 1, 3, and 5 are set to "Active High" which causes the pulse value to go from low to high while the lower IGBTs 2, 4, and 6 are set to "Active Low" which causes the pulse value to go from high to low. When the converter is not operational both IGBTs in a leg are set to "Active Low". On the "Logic" tab the pulldown menu selection for the "Control logic source" option is "Input port" since the state of the IGBT is based on the converter operational state (Figure 55).

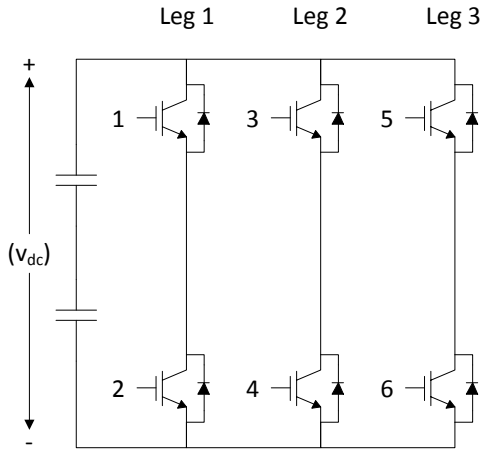

Figure 54 - Three Phase Full Bridge Converter

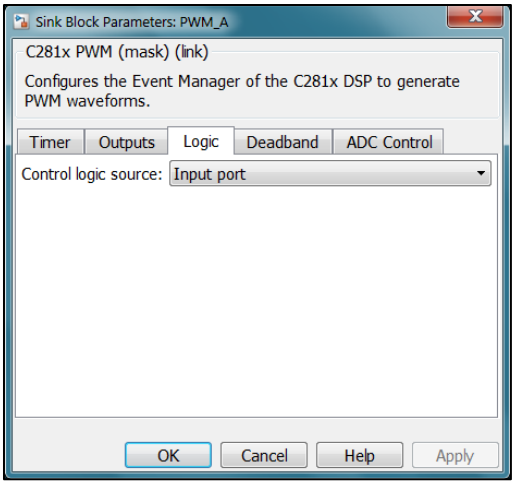

Figure 55 - PWM IGBT Control

To further avoid the short-circuit hazard of having both IGBTs on at the same time a time delay or deadband between the PWM signals is required in order to allow one of the IGBTs of a leg to fully turn "off" before the other IGBT in the leg is turned "on". The "Deadband prescaler" multiplied by the "Deadband period" sets the total deadband in clock cycles (Figure 56). Since the gate driver circuit and IGBT datasheet are unavailable the deadband was set to 2 microseconds. The "IGBT" datasheet would indicate the delay time and having an understanding of the propagation delay of the gate driver circuit would aide in determining a more appropriate deadband.

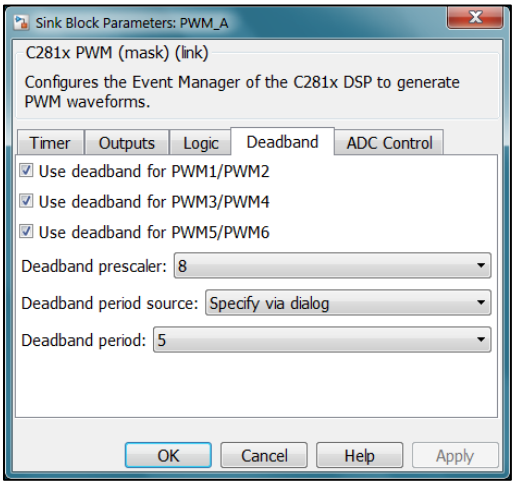

Figure 56 - PWM Deadband

5.2.3. ADC

The ADC cannot be synchronized with the PWM when it is in cascaded mode. Cascaded mode refers to the situation where a single ADC block is used for both modules A and B (Figure 57). However, asynchronous PWM is sufficient for this application since the ratio of the switching frequency to fundamental frequency is greater than 21 [4, pp. 208,226]. The "ADCA_PQ" and "ADCB_PQ" subsystems in Figure 57 improve the accuracy of the 12-bit analog-to-digital converter by correcting the ADC offset error.

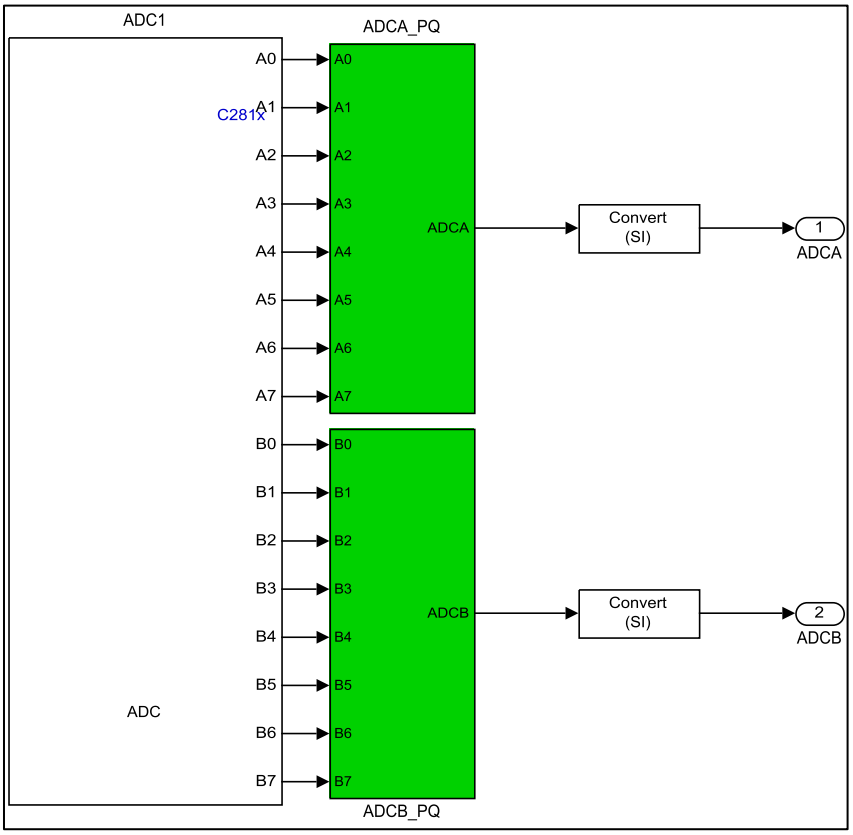

Figure 57 - "PQ" Converter ADC

5.2.4. Space Vector PWM

The contents of the "SVPWM" subsystem in Figure 52 provide the overview of the space vector modulation scheme as shown in Figure 58 [32].

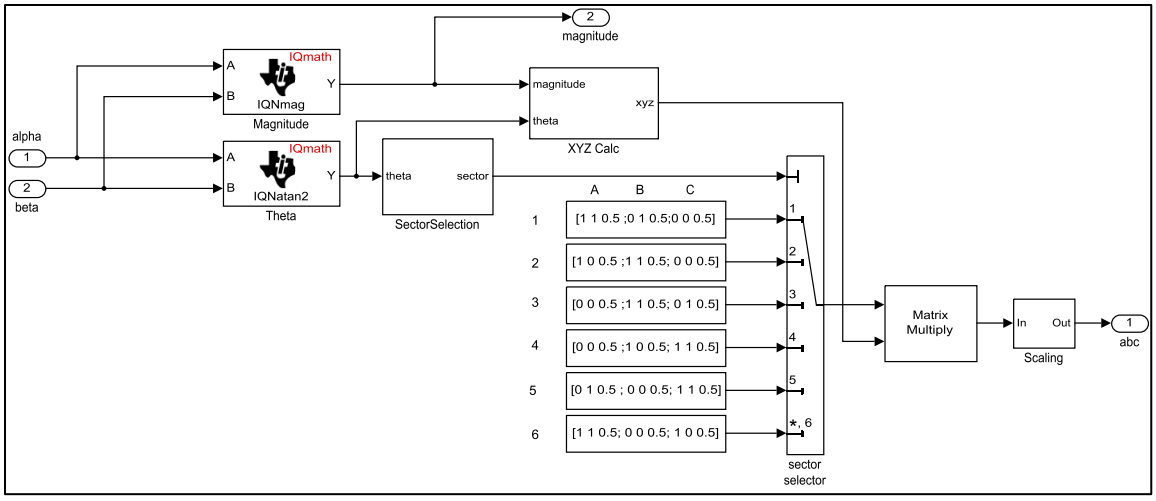

Figure 58 - Space Vector PWM

The converter voltage reference defined in the $\alpha\beta$ stationary reference frame is expressed as a space vector in (126) with magnitude (127) and angle (128) defining this voltage space vector.

$$\vec{v}_c^{\,*} = v_{c\alpha}^{*} + jv_{c\beta}^{*} \tag{126}$$

$$\left|v_c^{*}\right| = \sqrt{v_{c\alpha}^{*\,2} + v_{c\beta}^{*\,2}} \tag{127}$$

$$\theta = tan^{-1}\frac{v_{c\beta}^{*}}{v_{c\alpha}^{*}} \tag{128}$$

The “SectorSelection” subsystem in Figure 59 uses the angle of the voltage space vector to determine which of the 6 possible sectors from Table 13 in which the converter voltage reference could be located in. The “sector selector” multi-port switch defines the maximum duty time of the upper IGBT in each leg dependent upon the sector that is selected.

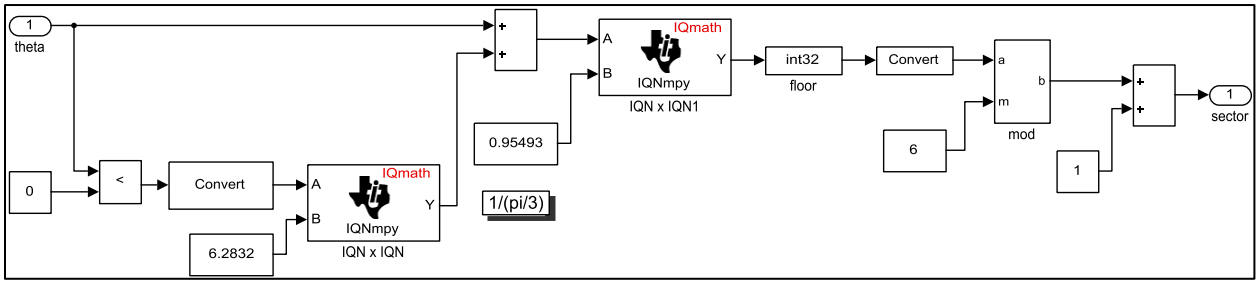

Figure 59 - SVPWM Sector Selection

Sector	Degrees	Radians
1	$0° < \theta \leq 60°$	$0 < \theta \leq \frac{\pi}{3}$
2	$60° < \theta \leq 120°$	$\frac{\pi}{3} < \theta \leq \frac{2\pi}{3}$
3	$120° < \theta \leq 180°$	$\frac{2\pi}{3} < \theta \leq \pi$
4	$180° < \theta \leq 240°$	$\pi < \theta \leq \frac{4\pi}{3}$
5	$240° < \theta \leq 300°$	$\frac{4\pi}{3} < \theta \leq \frac{5\pi}{3}$
6	$300° < \theta \leq 360°$	$\frac{5\pi}{3} < \theta \leq 2\pi$

Table 13 - SVPWM Sectors

For a two-level converter there are 8 possible switching states with 6 active stationary voltage vectors that establish the boundaries of the sectors in Table 13 along with 2 zero voltage vectors. In linear mode of operation the space vector representation of the converter voltage reference can be synthesized in each sector by using the two nearest active voltage vectors that serve as sector boundaries for where the space vector resides as well as a single zero voltage vector. The duration time for the two active voltage vectors and one zero voltage vector must be known in order to produce a vector sum that would equal the converter voltage reference. The duration times are calculated with the "XYZ Calc" subsystem as shown in Figure 60. The "X" and "Y" are the calculated duration times for the active voltage vectors with the remainder "Z" being the duration time of the zero voltage vector.

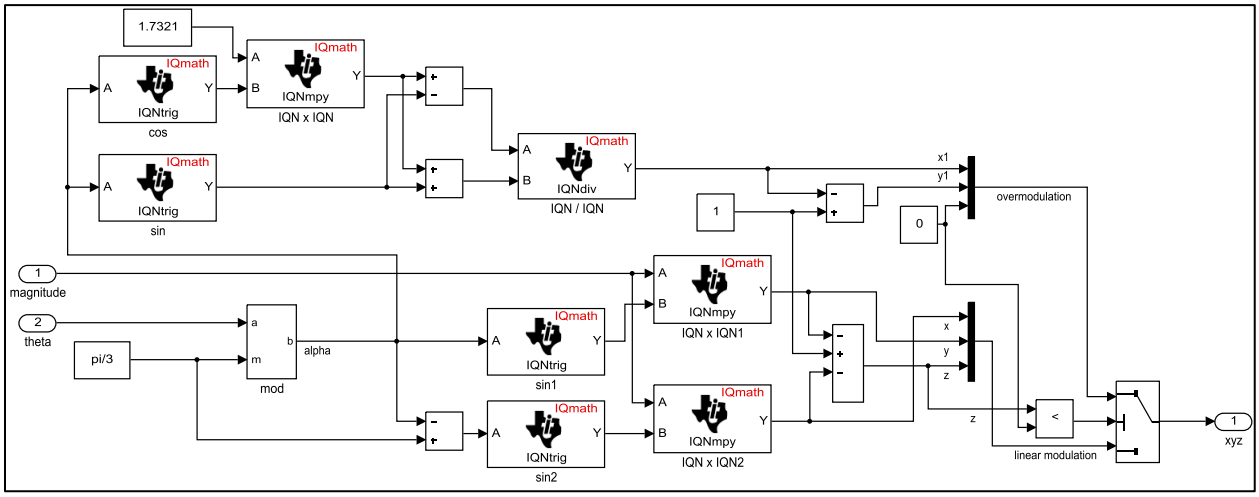

Figure 60 - SVPWM XYZ Calculation

5.2.5. Phase-Locked Loop

The PLL in Figure 61 establishes the estimated grid angle from the grid voltage as described in Chapter 2.6. The base grid frequency is the steady-state value of the control signal when added to the PI controller output deviation variable results in the actual control signal the estimated grid frequency.

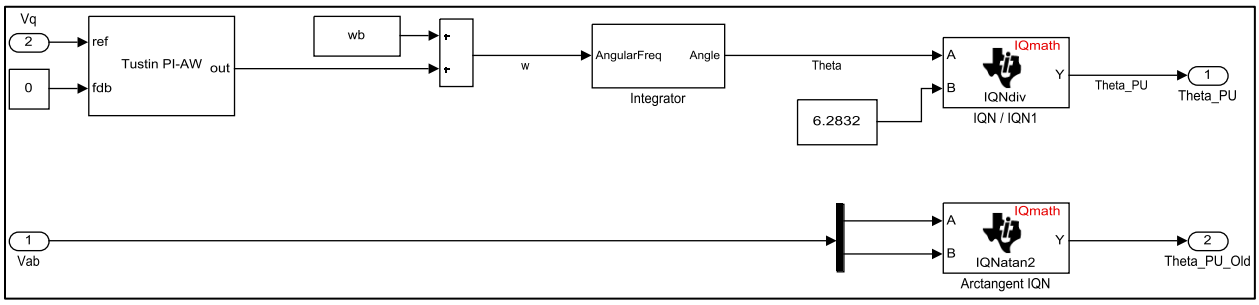

Figure 61 - Phase-Locked Loop

The "Integrator" subsystem in Figure 62 integrates the estimated grid frequency to determine the estimated grid angle.

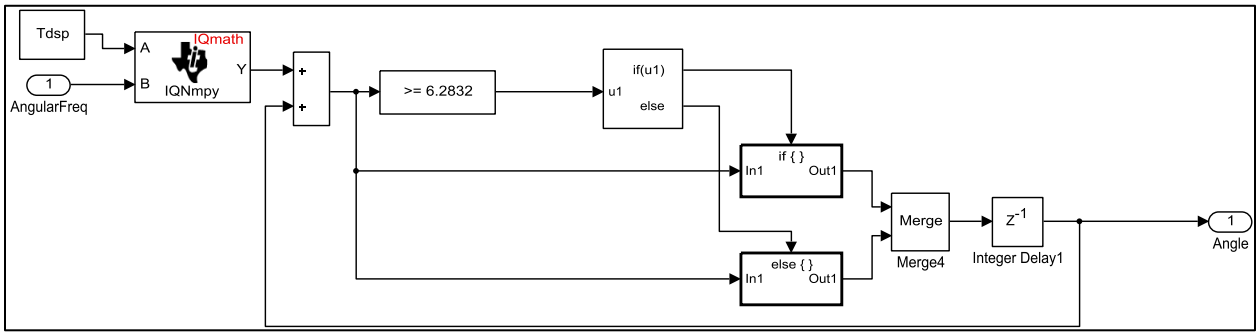

Figure 62 - Integrator for PLL

The if-else subsystems in Figure 63 are used to reset the estimated grid angle after each cycle.

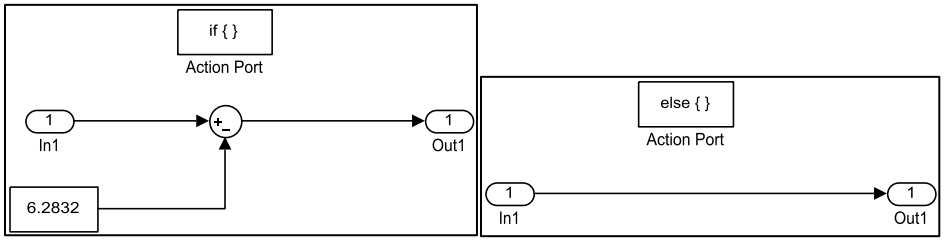

Figure 63 - PLL Integrator If Else Subsystems

5.2.6. Coordinate Transformations

Voltage oriented control requires the transformation of the voltages and currents from the *abc* stationary reference frame to the *dq* synchronous reference frame as described in Chapter 2.2.1(Figure 64).

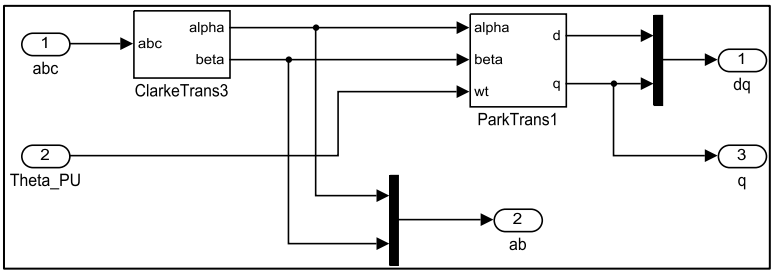

Figure 64 - Transformation from ABC to Alpha-Beta to Direct-Quadrature

Initially the three-phase quantities are adapted from the *abc* stationary reference frame to the $\alpha\beta$ stationary reference frame using the Clarke transformation as shown in Figure 65.

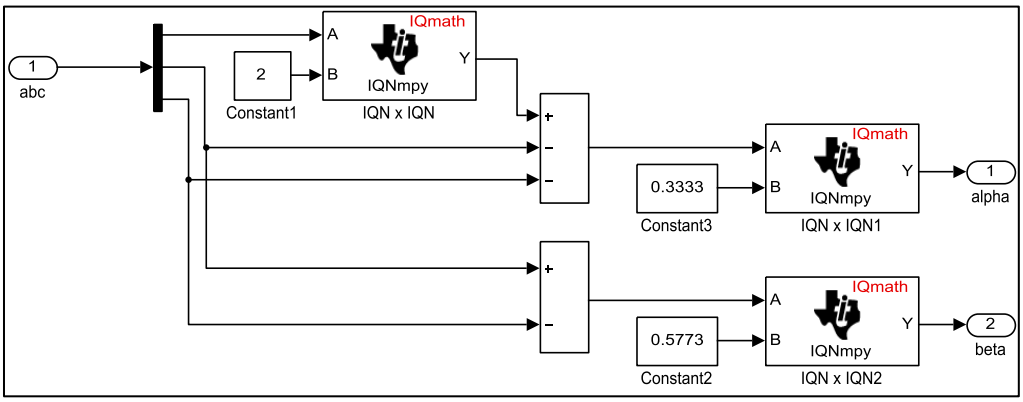

Figure 65 - Clarke Transformation

Then the two-phase quantities are converted from the $\alpha\beta$ stationary reference frame to the *dq* synchronous reference frame using the Park transformation as shown in Figure 66.

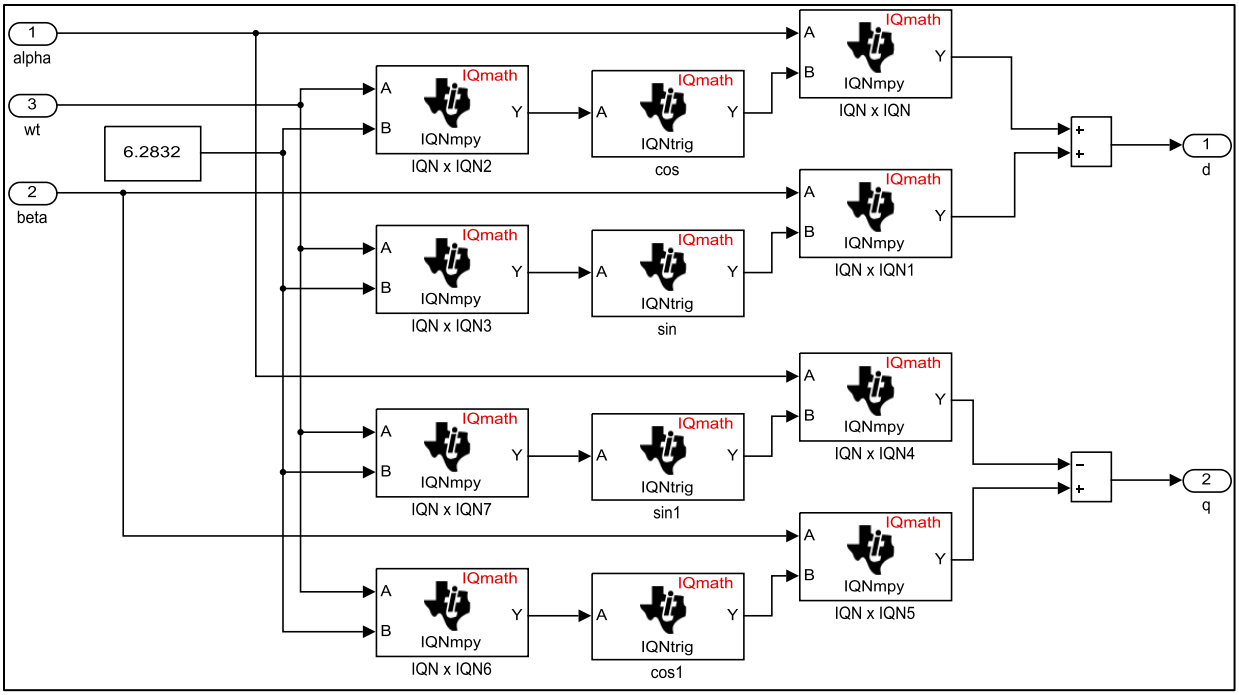

Figure 66 - Park Transformation

To realize space vector modulation the converter voltage reference in the *dq* synchronous reference frame must be transformed to the $\alpha\beta$ stationary reference frame using the inverse Park transformation (Figure 67).

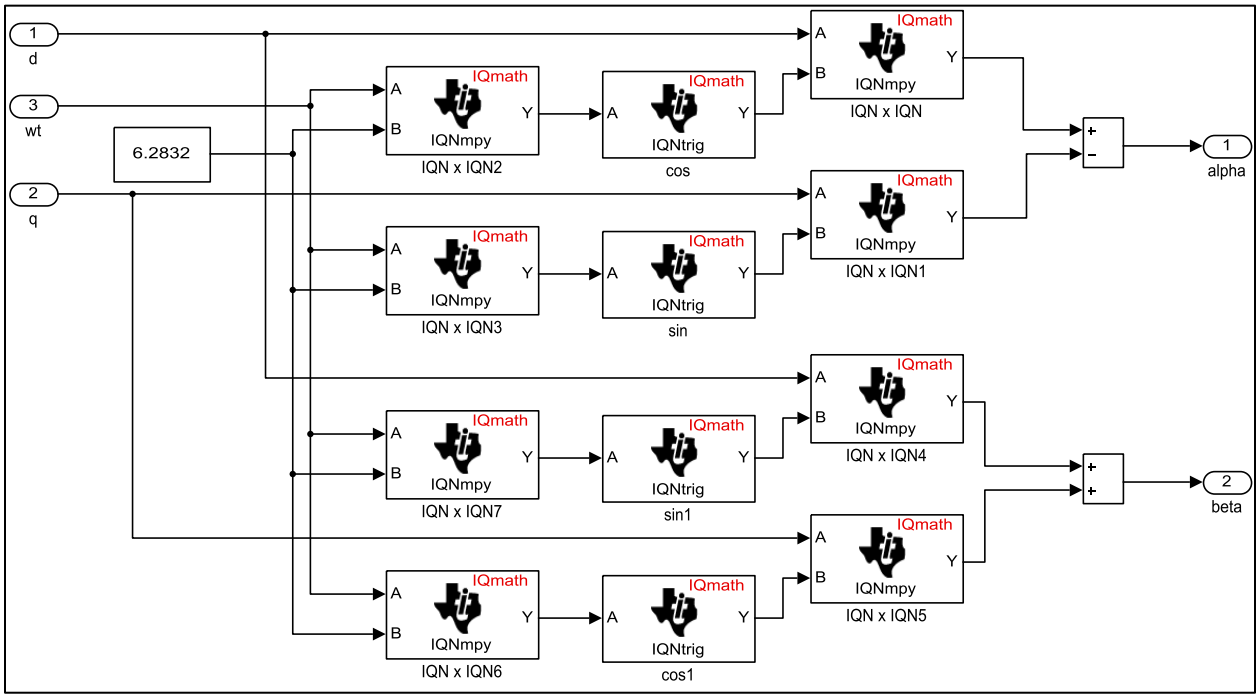

Figure 67 - Inverse Park Transformation

5.2.7. Tustin Proportional Integral Controller with Anti-Windup

Upper and lower thresholds are imposed on the continuous-time domain PI controller output with the addition of a limit block as shown in Figure 68. Integrator windup is avoided by calculating the error between the PI controller output and imposed limit. When the controller output has not reached the limit the anti-windup feedback has no effect on the controller. However, when the limit has been reached feeding this error back to the integrator through the anti-windup gain forces the error to approach zero which means the PI controller output is being kept close to the limit. The anti-windup gain determines how quickly the integrator windup is reset with a recommended value being the ratio of integral gain to proportional gain [33, p. 307].

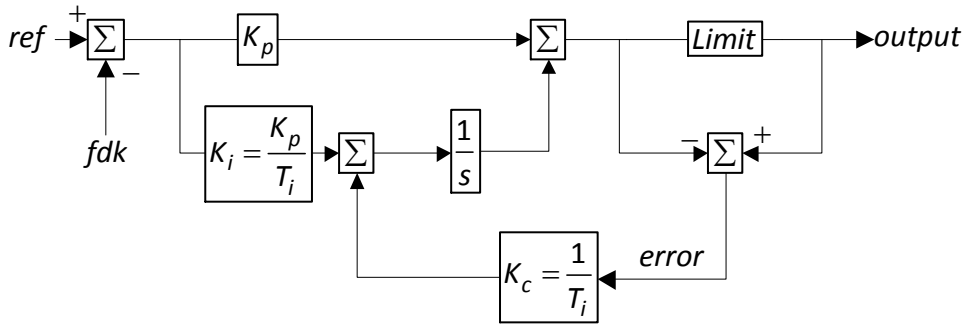

Figure 68 - Continuous PI Controller with Anti-Windup

By using the backward Euler discretization method, the block diagram representation in Figure 68 designed in the continuous-time domain can be transformed to the discrete-time domain as shown in Figure 69. As can be seen in Figure 68 and Figure 69 the proportional gain (129) is exactly the same between the continuous and discrete-time block diagrams. However, the integral (130) and the anti-windup (131) gains for the discrete-time domain are obtained by multiplying their respective continuous-time gain by the computational device's sample time.

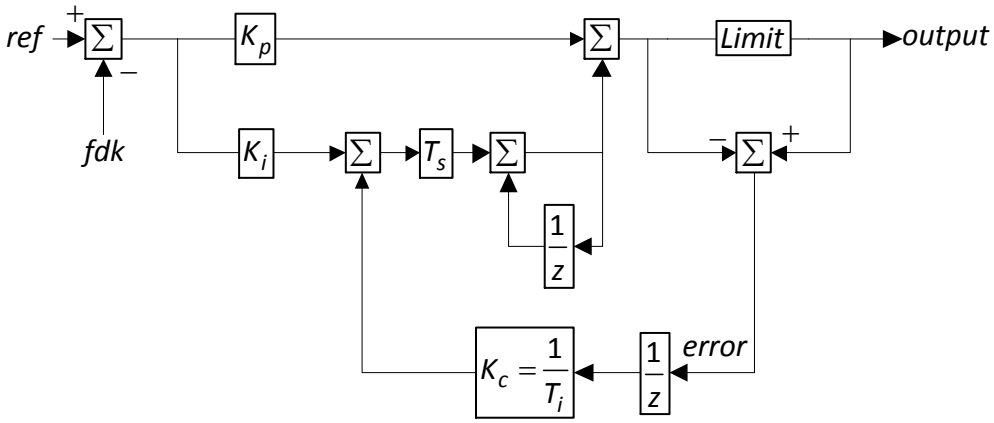

Figure 69 - Discrete PI Controller with Anti-Windup

$$K_{p,discrete} = K_p \tag{129}$$

$$K_{i,discrete} = K_i T_s \tag{130}$$

$$K_{c,discrete} = \frac{T_s}{T_i} \tag{131}$$

The MathWorks Simulink C2000 PID Controller is based on backward difference integration otherwise known as Euler's backward differential method which provides a 3% distortion limit as long as the ratio of sampling frequency to frequency of interest is greater than 20. Instead a PI controller based on Tustin integration with anti-windup as shown in Figure 70 provides a 3% distortion limit as long as the ratio of sampling frequency to frequency of interest is greater than 10.

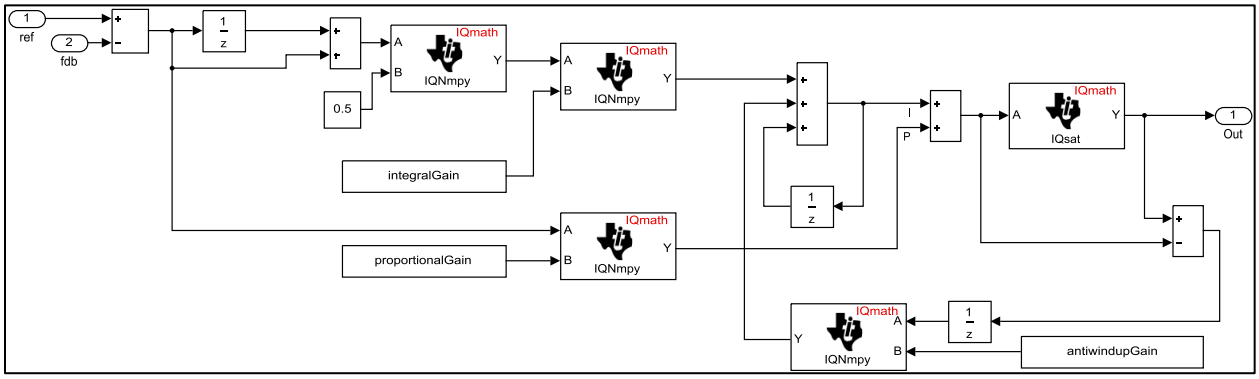

Figure 70 - "PQ" Converter Tustin PI Controller with Anti-Windup

By applying the Tustin discretization method to the PI controller the continuous-time domain representation (132) is transformed to the discrete-time domain(133).

$$G_{pi} = K_i \frac{\left(1 + s\frac{K_p}{K_i}\right)}{s} \tag{132}$$

$$G_{pi,discrete} = K_i \frac{\left(1 + \frac{2}{T_s}\frac{z-1}{z+1}\frac{K_p}{K_i}\right)}{\frac{2}{T_s}\frac{z-1}{z+1}} \tag{133}$$

5.3. Model-in-the-Loop Simulink Implementation and Testing

Model-in-the-loop testing was completed to ensure proper operation and performance of the converters prior to deploying the compiled code to the actual project installation. For the model-in-the-loop Simulink implementation a system-level representation of the actual project installation was developed with the SimPowerSystems library as shown in Figure 71, Figure 72, Figure 73, and Figure 74.

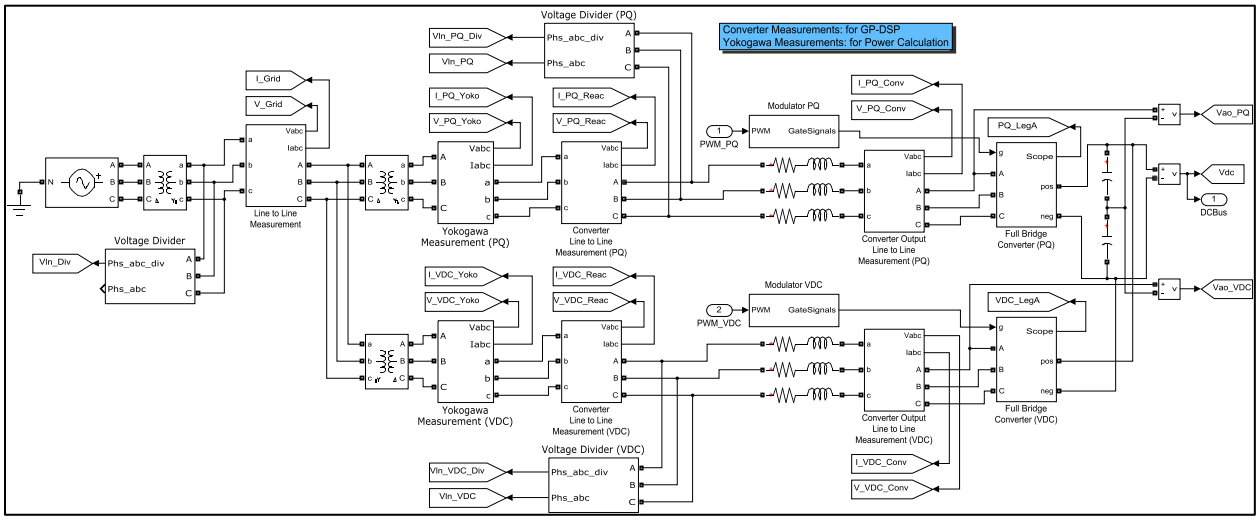

Figure 71 - System-Level Representation for Model-in-the-Loop Implementation

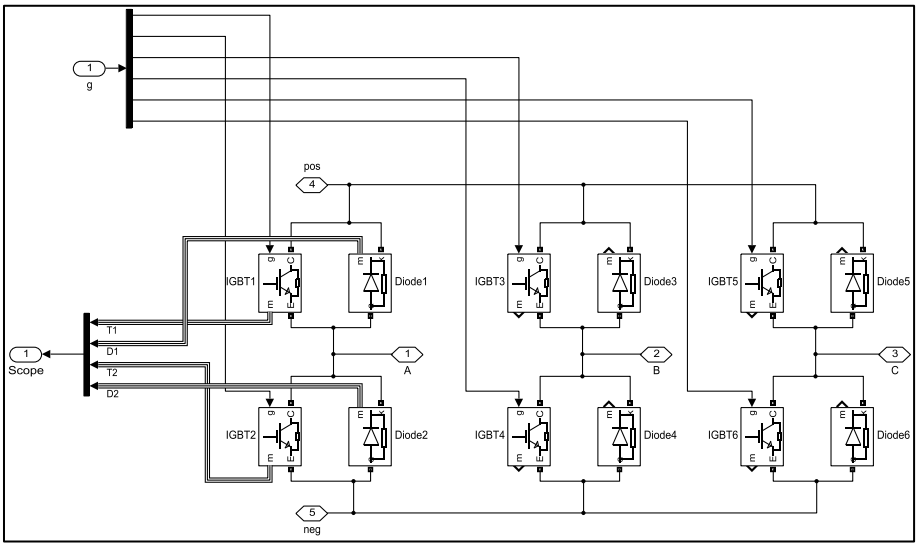

Figure 72 - Three-Phase Two-Level Converter for Model-in-the-Loop Implementation

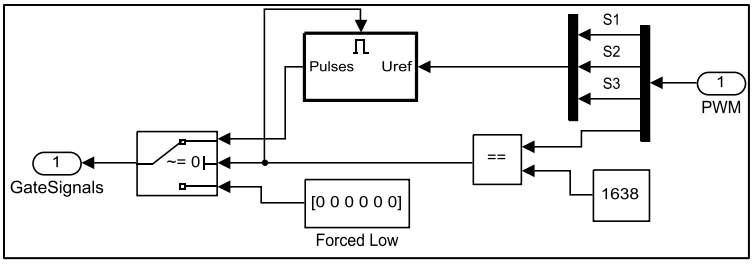

Figure 73 - Modulator for Model-in-the-Loop Implementation

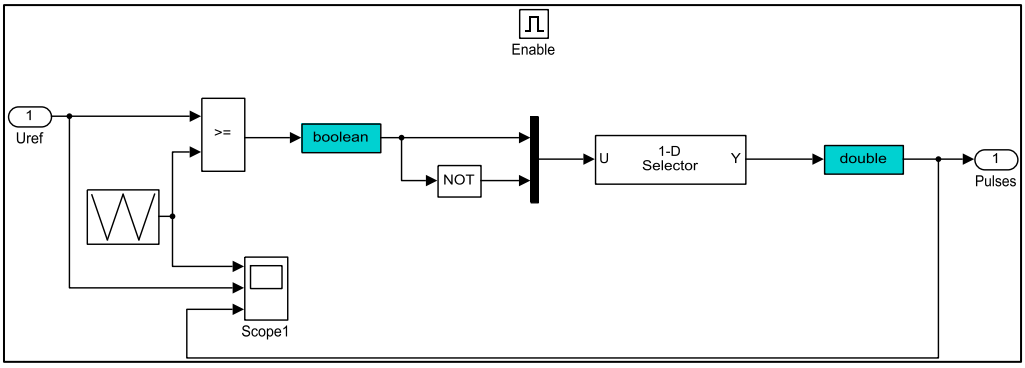

Figure 74 - Gate Driver Signal Generation for Model-in-the-Loop Implementation

The top level subsystem from the “PQ” and “VDC” Simulink implementations were added to the model-in-the-loop implementation for control of the converters (Figure 75).

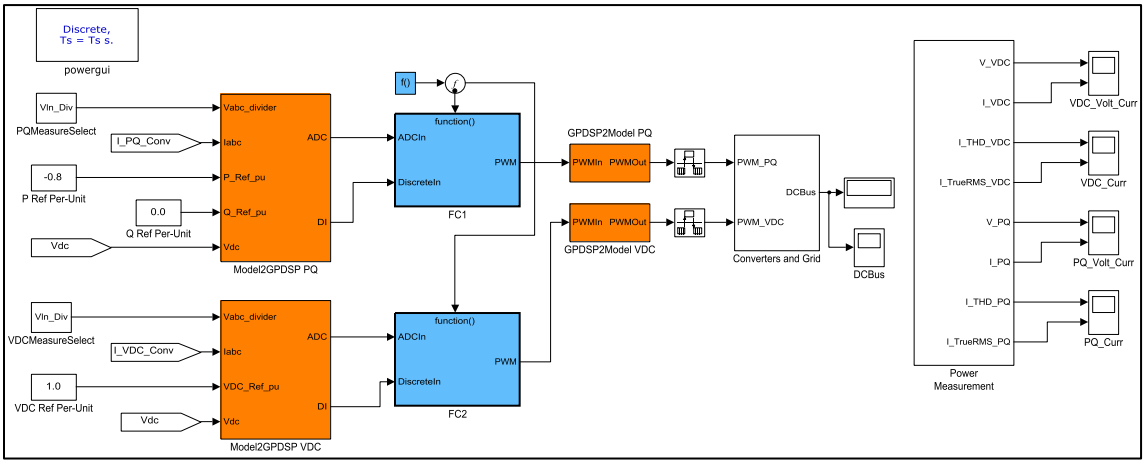

Figure 75 - Model-in-the-Loop Implementation

Since the “PQ” and “VDC” Simulink implementations were developed to interface the peripherals on the TI C2000 processor the inputs and outputs needed to be rerouted to interface the system-level model (Figure 76).

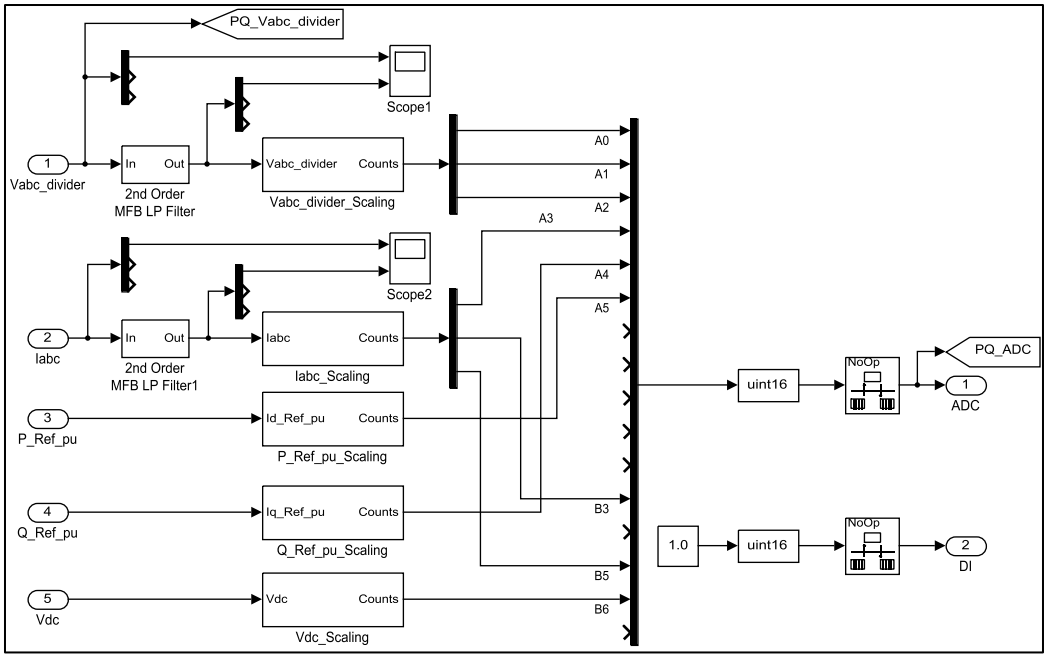

Figure 76 - Model-in-the-Loop Link to "PQ" Converter Simulink Implementation

Prior to running the model-in-the-loop simulation the blocks labeled “P Ref Per-Unit” and “Q Ref Per-Unit” must be initialized with the desired per-unit amount of Active and/or Reactive power for the “PQ” converter to deliver and/or consume during operation while the constant block labeled “VDC Ref Per-Unit” is the DC bus voltage set point for the “VDC” converter to maintain (Figure 75). After the user requests the model-in-the-loop simulation to run two dialog boxes will appear. The first dialog box determines if the model uses the three-phase voltage measurements after each reactor or a single three-phase voltage measurement between the supply transformer and the isolation transformers (Figure 71). The second dialog box determines if the model uses symmetrical or asymmetrical regular sampled SVM for the converters.

Both dynamic and steady-state operation of the converters was examined. The model-in-the-loop simulation was run with the three-phase voltage measurements after each reactor using asymmetrical regular sampled SVM for the converter modulation technique. The “PQ” converter active power reference was set to -0.8 per-unit at unity power factor while the “VDC” converter was set to maintain a DC bus voltage of 1 per-unit. The DC bus voltage is initialized in the model to the peak of the grid supply line voltage to simulate the pre-charge circuit. Due to the amount of inductance in the isolation transformer the harmonics generated by the converters are only slightly attenuated when measured between the reactor and isolation transformer. After a short time, the “VDC” converter receives the step command to maintain a DC bus voltage of 1 per-unit (Figure 77).

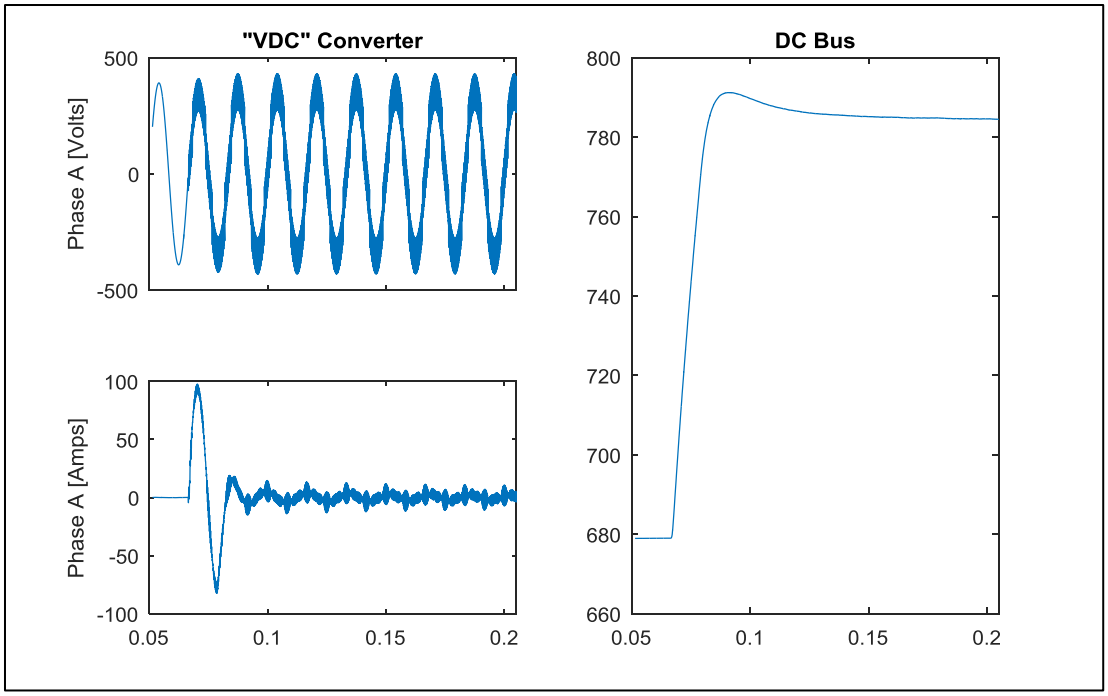

Figure 77 - "VDC" Converter Step at 4860Hz with Double-Edge Asymmetrical Regular Sampled SVM

Then shortly later, the "PQ" converter receives the step command to deliver –0.8 per-unit active power at unity power factor (Figure 78).

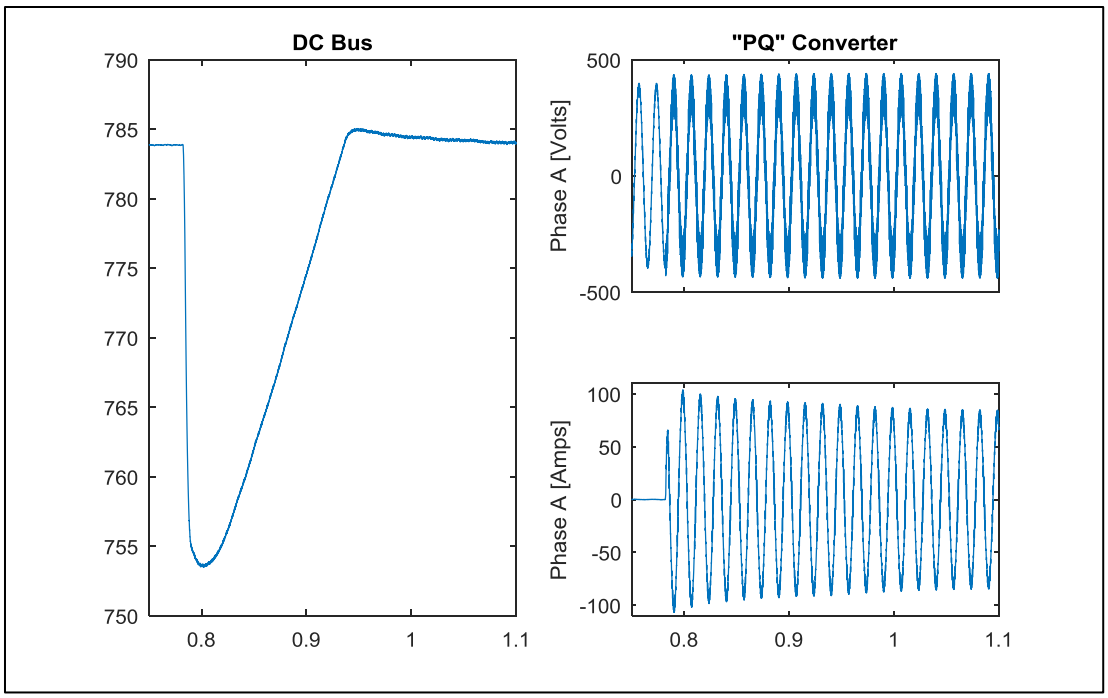

Figure 78 - "PQ" Supplying -0.8 pu Active Power Step at 4860Hz with Double-Edge Asymmetrical Regular Sampled SVM

Finally after a few seconds the steady-state operation of the converters is examined (Figure 79).

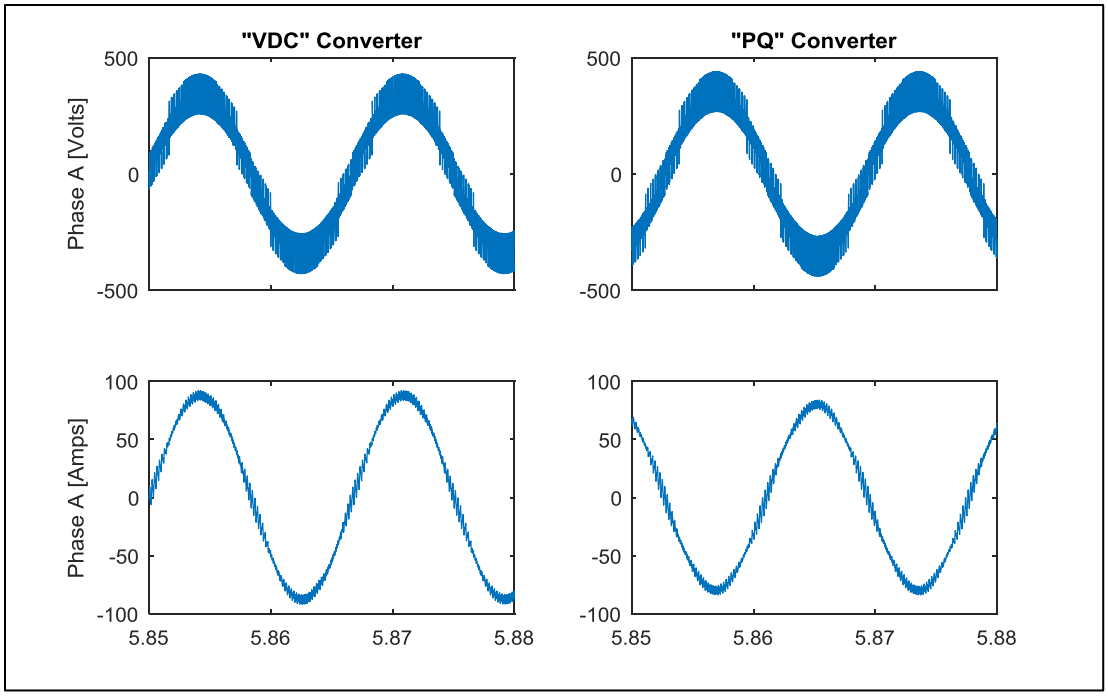

Figure 79 - "PQ" Supplying -0.8 pu Active Power at 4860Hz with Double-Edge Asymmetrical Regular Sampled SVM

For the second simulation the "PQ" converter reactive power reference was set to –0.8 per-unit at capacitor operation while the "VDC" converter was set to maintain a DC bus voltage of 1 per-unit. Shortly after the "VDC" converter maintains the DC bus voltage at 1 per-unit, the "PQ" converter receives the step command to deliver –0.8 per-unit reactive power (Figure 80).

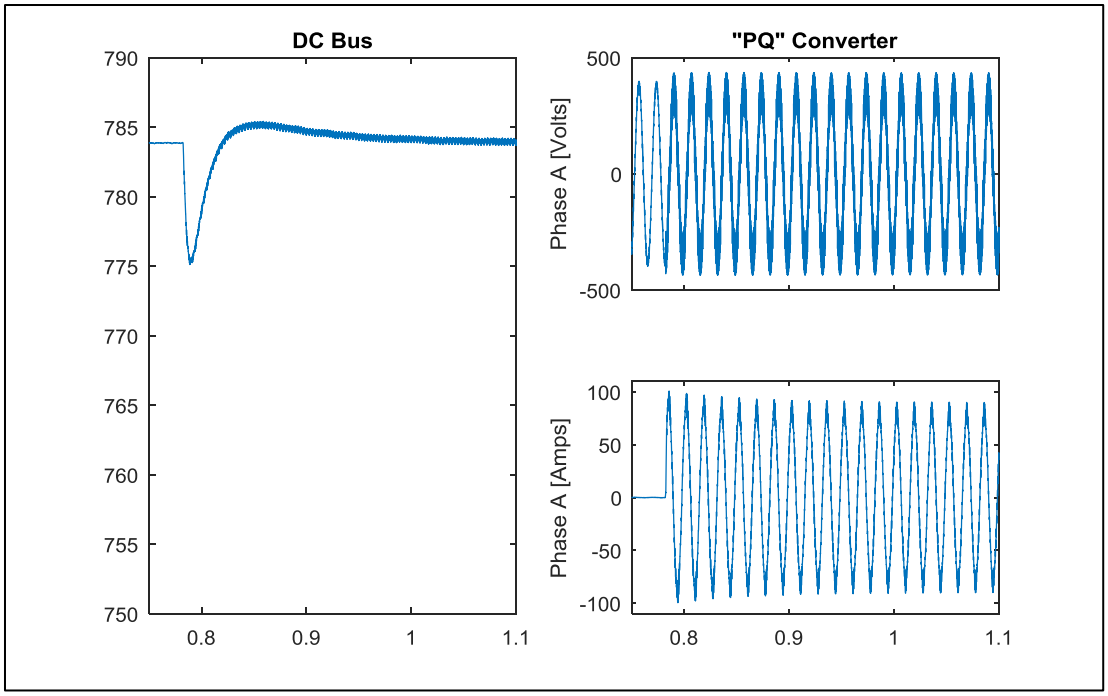

Figure 80 - "PQ" Supplying -0.8 pu Reactive Power Step at 4860Hz with Double-Edge Asymmetrical Regular Sampled SVM

Once again, after a few seconds the steady-state operation of the converters is examined (Figure 81).

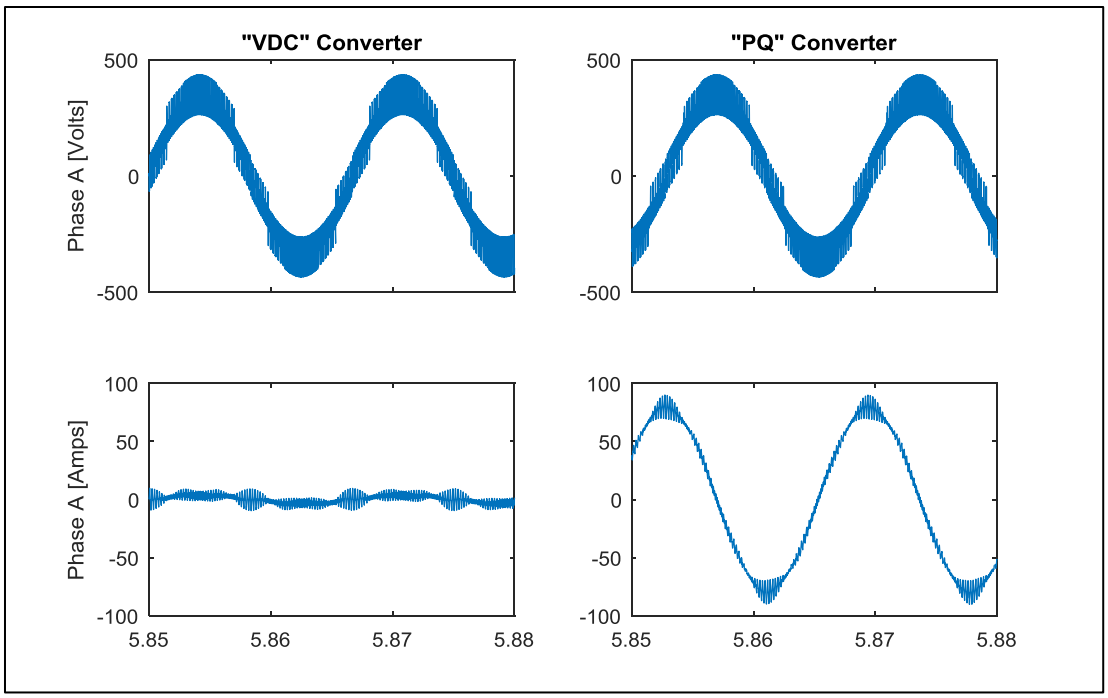

Figure 81 - "PQ" Supplying -0.8 pu Reactive Power at 4860Hz with Double-Edge Asymmetrical Regular Sampled SVM

5.4. Simulation vs. Analytical Harmonic Spectrum

The spectrum of harmonic voltages generated by the "PQ" converter was obtained using the FFT Analysis Tool from the MATLAB environment in Figure 82 and analytically as described in Chapter 3.7 using numerical integration in Figure 83. The model-in-the-loop simulation was run with the three-phase voltage measurements after each reactor using symmetrical regular sampled SVM for the converter modulation technique at a switching frequency of 4860Hz as determined in Chapter 3.7. Eight modes of operation were examined for the "PQ" converter, but as previously determined the highest magnitude harmonics with the lowest harmonic order were generated when delivering reactive power. The spectrum of harmonics obtained after the simulation by applying a Fourier transform on the signals of interest matched very closely to the harmonics predicted with the analytical technique approximated with a numerical method to solve the complicated integrals.

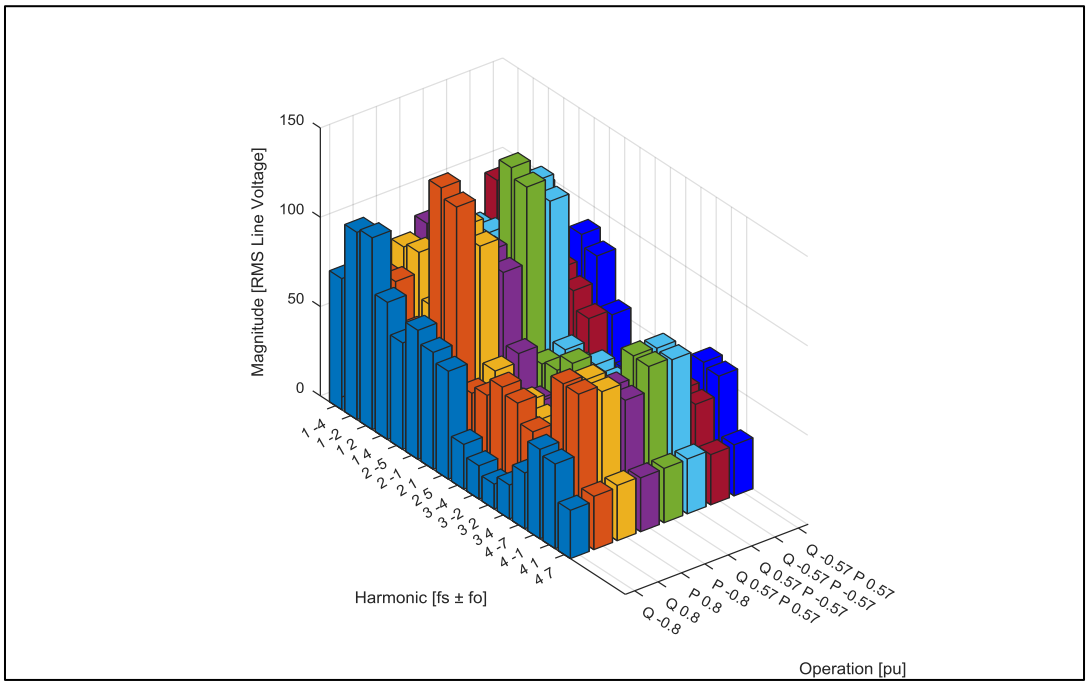

Figure 82 - Model-in-the-Loop Simulation Spectrum of "PQ" Converter Harmonic Voltages at 4860Hz

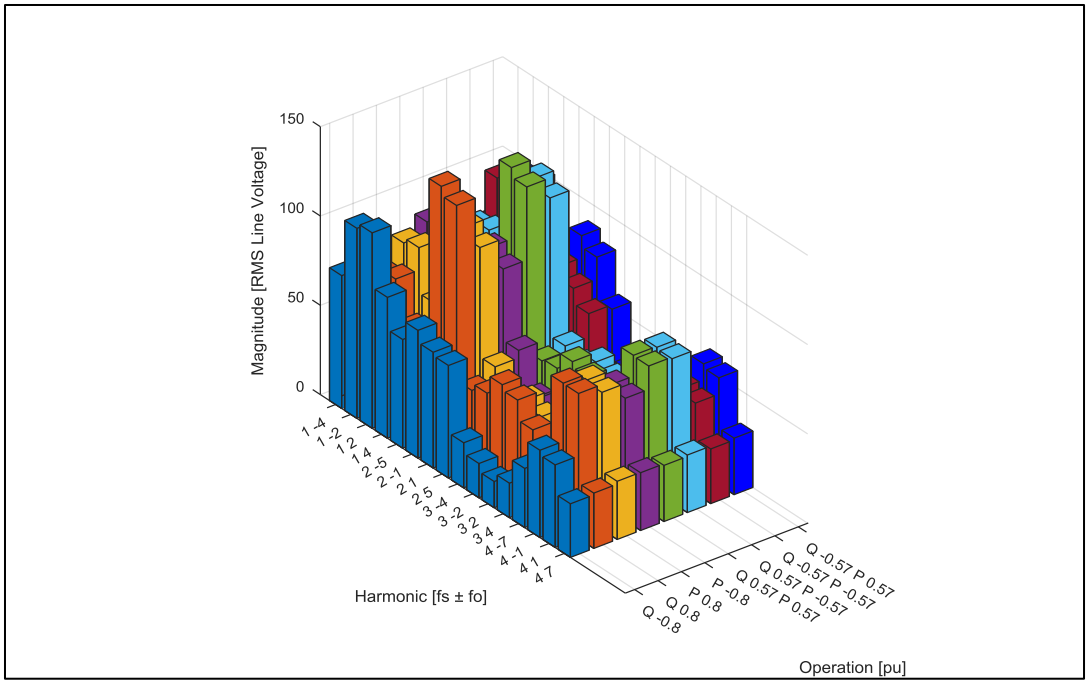

Figure 83 - Analytical Spectrum of "PQ" Converter Harmonic Voltages at 4860Hz

The spectrum of harmonic currents generated by the "PQ" converter was obtained using the FFT Analysis Tool from the MATLAB environment in Figure 84 and analytically using the rearranged form of (116) in Figure 85.

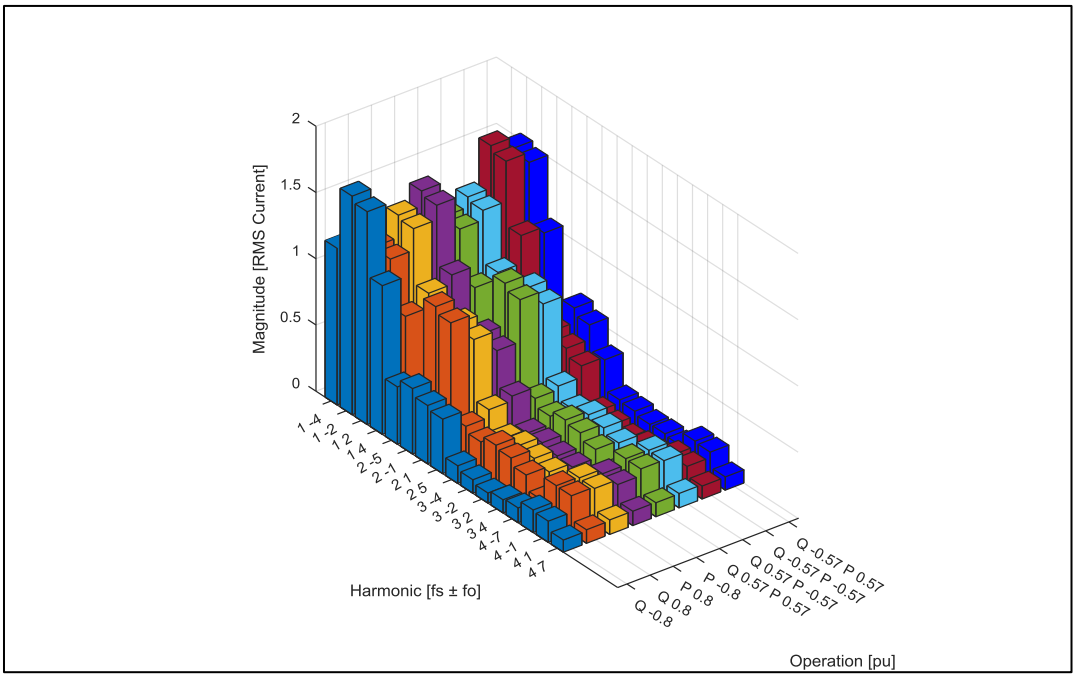

Figure 84 - Model-in-the-Loop Simulation Spectrum of "PQ" Converter Harmonic Currents at 4860Hz

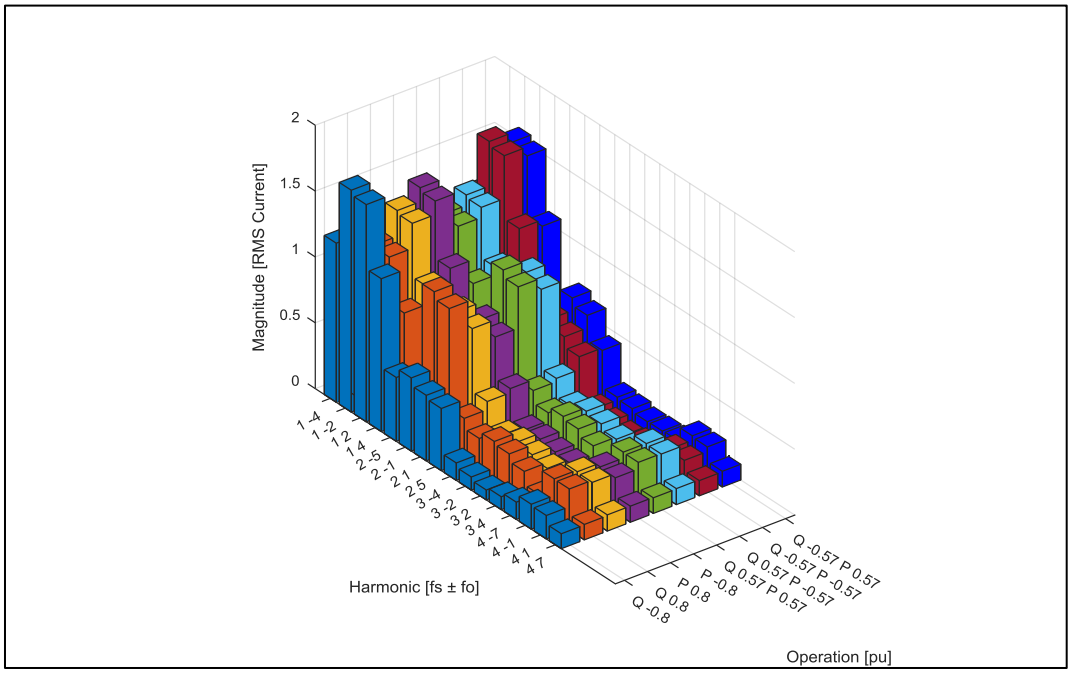

Figure 85 - Analytical Spectrum of "PQ" Converter Harmonic Currents at 4860Hz

6. Experimentation

After the model-in-the-loop testing showed the converter control schemes provided proper operation and performance, the compiled C code for the TI C2000 processors was downloaded to the GP-DSP boards for repeating the same tests with the project installation. The figures presented in Chapters 6.2 through 6.4 were captured with a Yokogawa WT1800 power analyzer with the harmonic measurement option installed (Figure 14). Up to the 500th harmonic can be digitally captured with the power analyzer; however the width of the measurement window for the Discrete Fourier Transform is limited to a single cycle of the grid. The figures in Chapter 6.3 with a converter switching frequency of 4860Hz were taken with the Yokogawa 300 kHz analog line filter enabled to prevent aliasing since the harmonics from these recordings were examined in Chapter 6.4. Symmetrical regular sampled SWM was utilized by the converters.

6.1. Converter Testing with TI CC Studio GUI Composer

To determine how to set the PWM channel settings for the converter, a TI CC Studio GUI Composer application in Figure 86 was developed and used to control the individual legs of the converter in real-time (Figure 87).

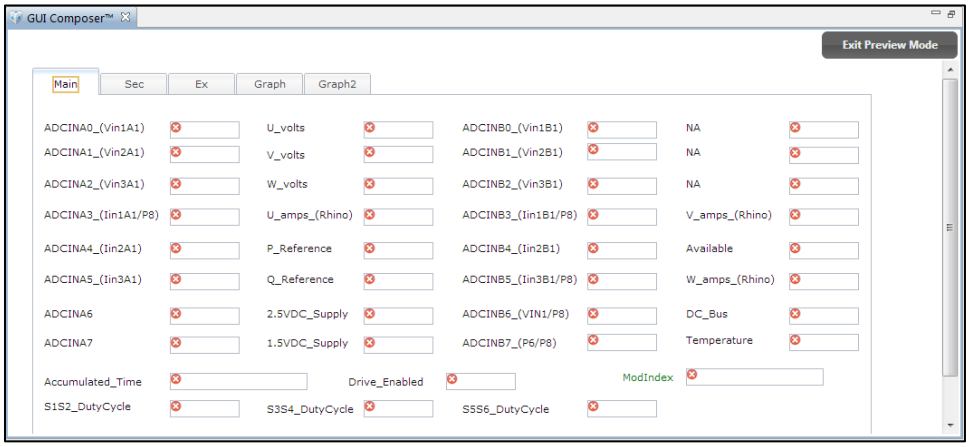

Figure 86 - TI CCStudio GUI Composer Application

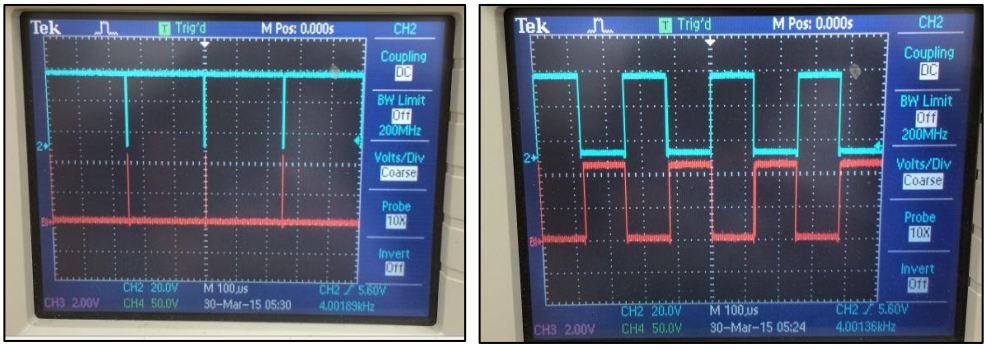

Figure 87 - 1% and 50% Reference to PWM Module A Leg 1

6.2. “VDC” Converter Steady-State and Dynamic Responses

The “VDC” converter maintains a constant DC bus voltage of 784 volts during no load operation at a switching frequency of 4500Hz (Figure 88). The “Element 2 V2” purple trace represents the DC bus voltage and the “Element 1 V1” yellow trace represents the phase A voltage measured between the “VDC” converter reactor and isolation transformer. The harmonics generated by “VDC” converter also appear on the “Element 3 V3” red trace representing the phase A voltage measured between the “PQ” converter reactor and isolation transformer.

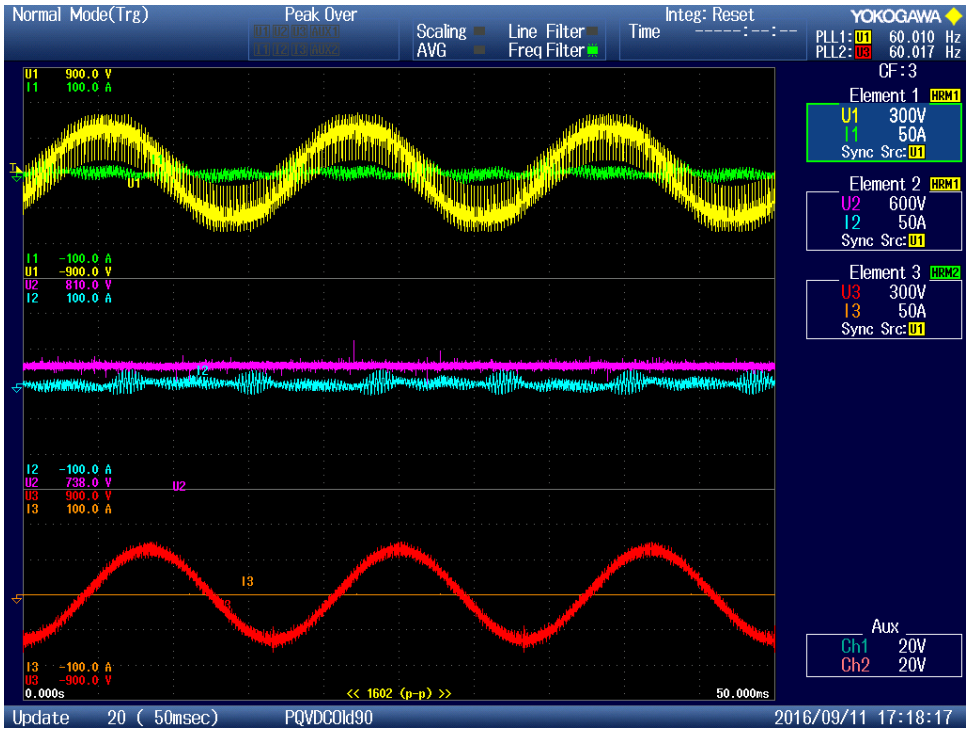

Figure 88 - "VDC" Converter Operating at No Load at 4500Hz

One cycle after the DC bus is pre-charged by the diode rectifier and current-limiting resistors; a 1 pu DC voltage step change is commanded and achieved by the “VDC” converter as shown in Figure 89 and Figure 90.

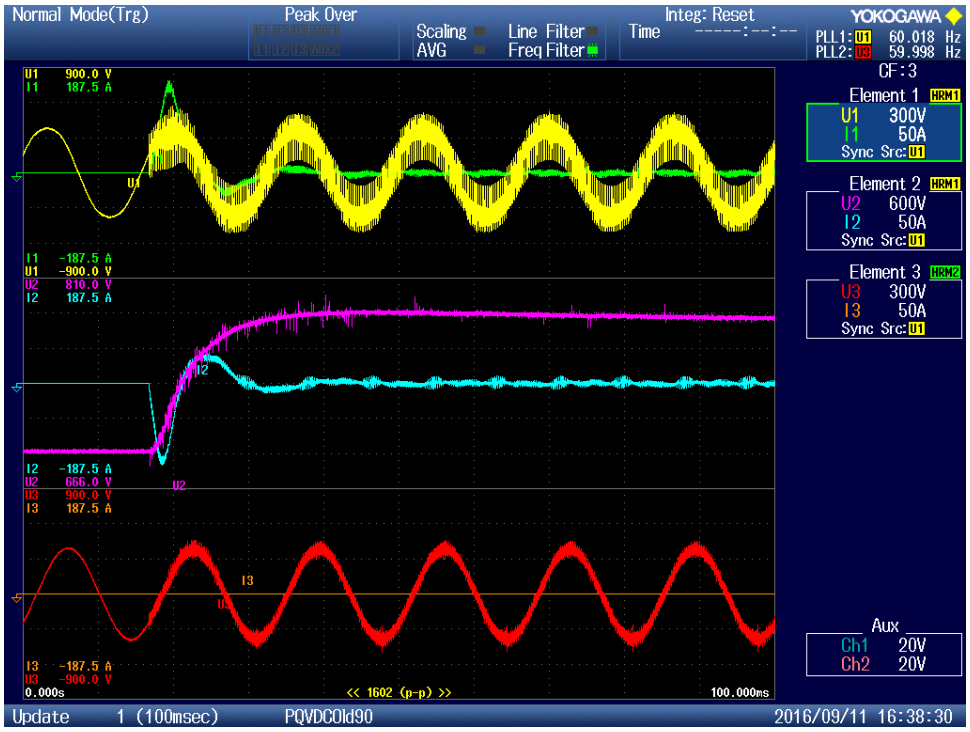

Figure 89 - "VDC" Converter Step Change at 4500Hz (100ms Window)

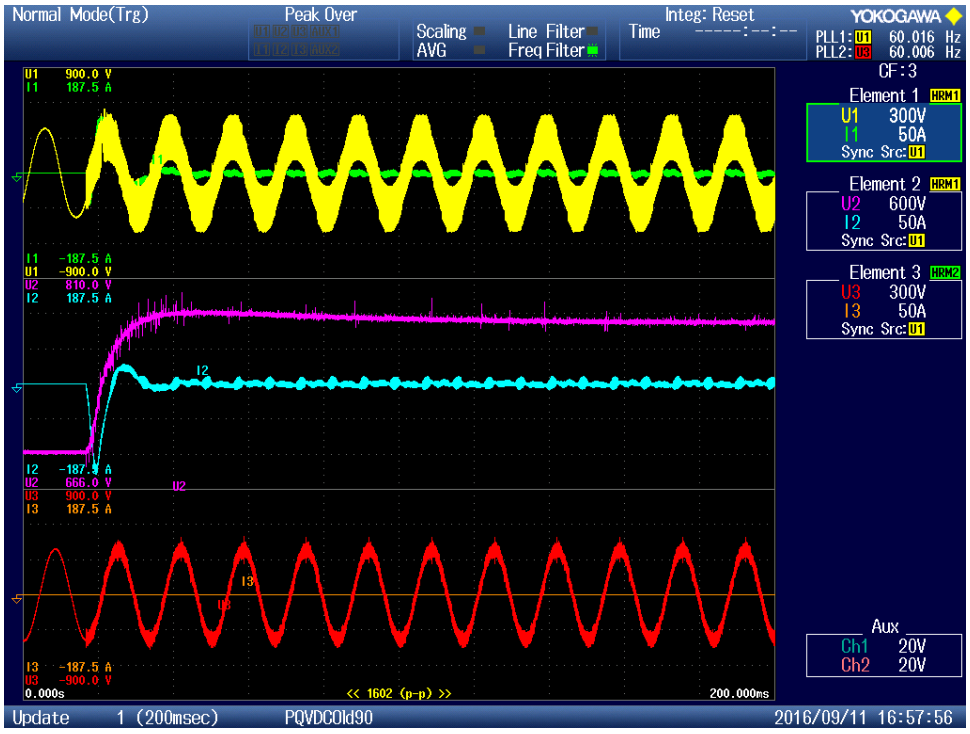

Figure 90 - "VDC" Converter Step Change at 4500Hz (200ms Window)

6.3. “PQ” Converter Steady-State and Dynamic Responses

The eight possible modes of steady-state operation for the “PQ” converter were examined with 0.8 pu of complex power flow introduced by the “PQ” converter in each case. For the Yokogawa recordings taken the “Element 2 V2” purple trace represents the DC bus voltage and the “Element 1 V1” yellow trace represents the line AB voltage measured at the output of the “VDC” converter. The “Element 1 I1” green trace and “Element 2 I2” blue trace represent the “VDC” converter phase A and B currents. The “Element 3 V3” red trace represents the line AB voltage measured at the output of the “PQ” converter and the “Element 3 I3” orange trace represents the “PQ” converter phase A current. Each recording has a duplicate figure with the line voltages removed for closer examination of the current. The switching frequency of the converters was fixed at 4860Hz during testing.

The “PQ” converter supplies -0.8 pu of active power at unity power factor as shown in Figure 91 and Figure 92. The “PQ” converter consumes 0.8 pu of active power at unity power as shown in Figure 93 and Figure 94. The “PQ” converter supplies -0.8 pu of reactive power at capacitor operation as shown in Figure 95 and Figure 96. The “PQ” converter consumes 0.8 pu of reactive power at inductor operation as shown in Figure 97 and Figure 98. The “PQ” converter consumes 0.57 pu of active power and 0.57 pu of reactive power as shown in Figure 99 and Figure 100. The “PQ” converter consumes 0.57 pu of active power and supplies -0.57 pu of reactive power as shown in Figure 101 and Figure 102. The “PQ” converter supplies -0.57 pu of active power and -0.57 pu of reactive power as shown in Figure 103 and Figure 104. The “PQ” converter supplies -0.57 pu of active power and consumes 0.57 pu of reactive power as shown in Figure 105 and Figure 106.

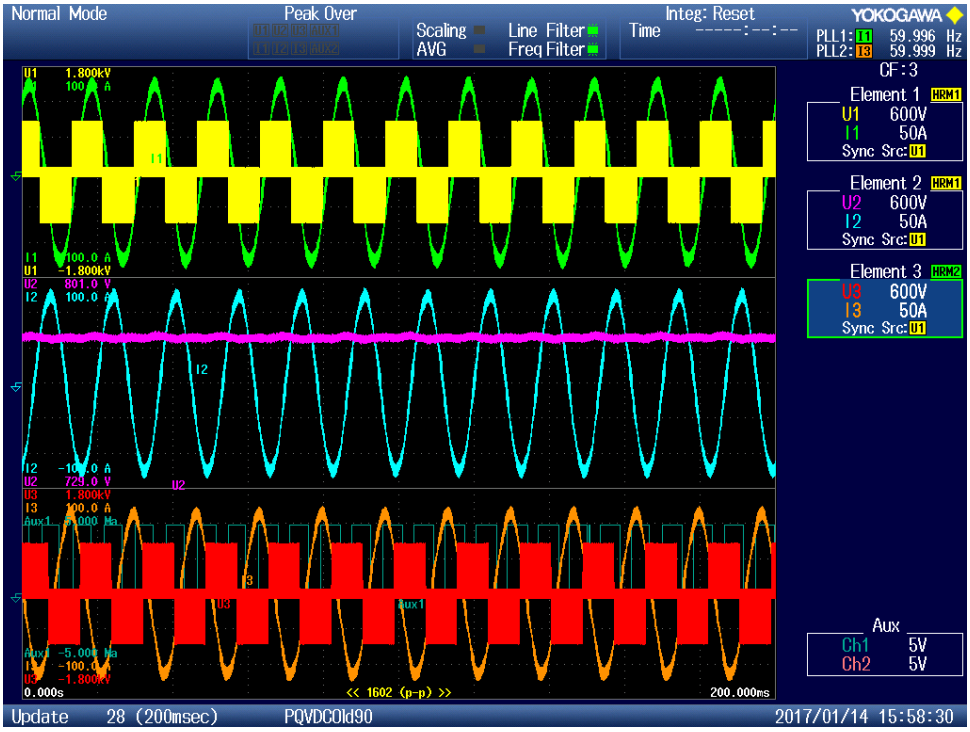

Figure 91 - "PQ" Supplying -0.8 pu Active Power at Unity Power Factor at 4860Hz

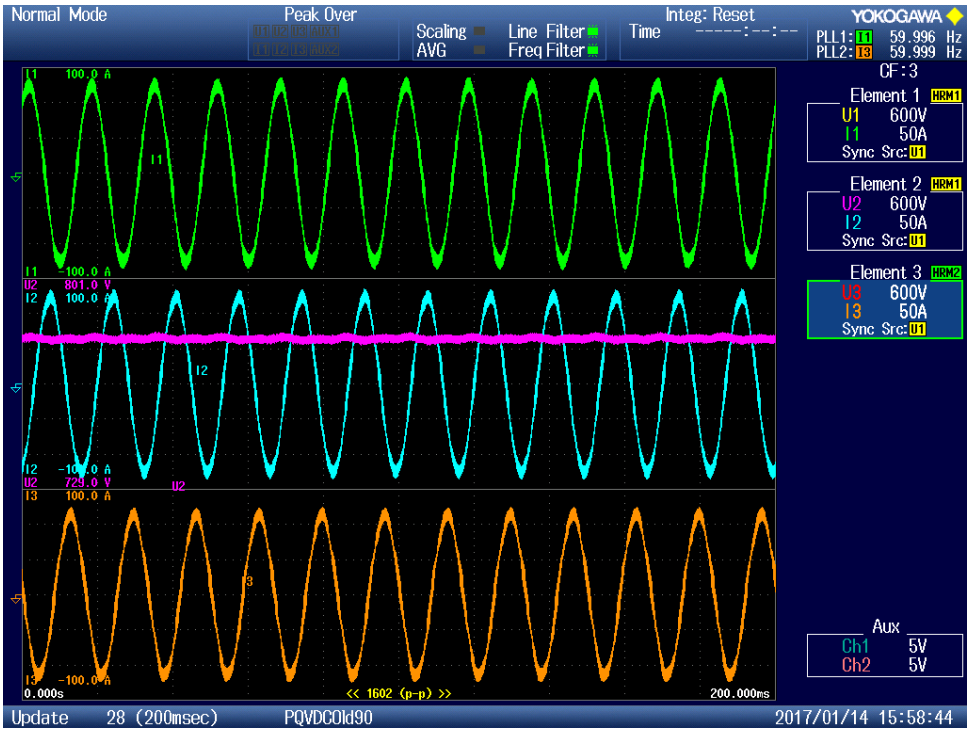

Figure 92 - "PQ" Supplying -0.8 pu Active Power at Unity Power Factor at 4860Hz without Line Voltages

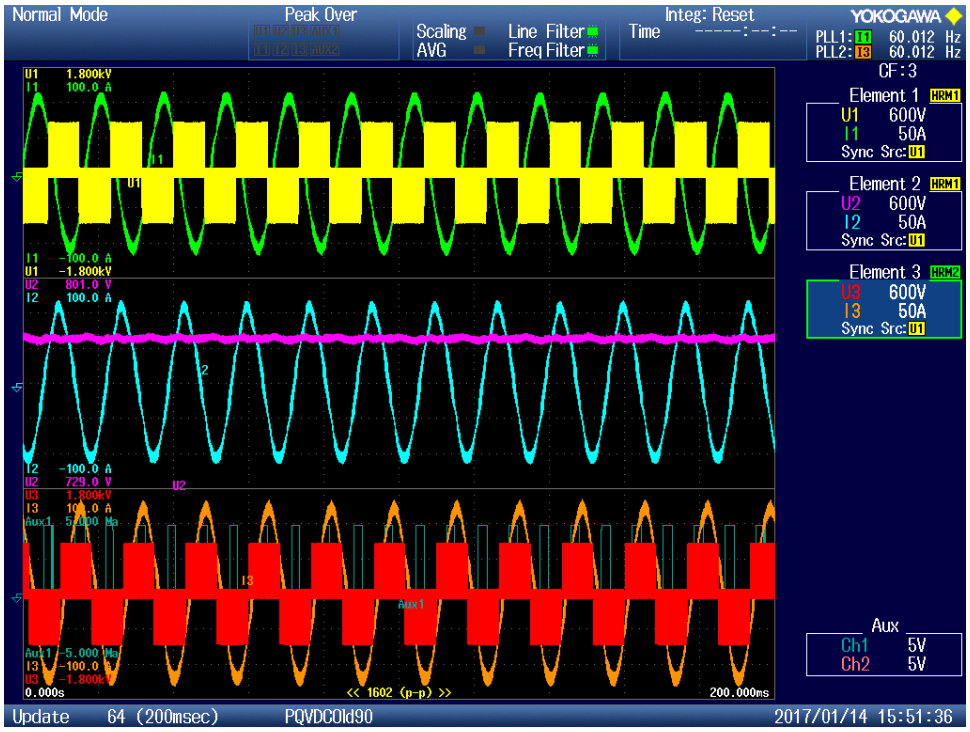

Figure 93 - "PQ" Consuming 0.8 pu Active Power at Unity Power Factor at 4860Hz

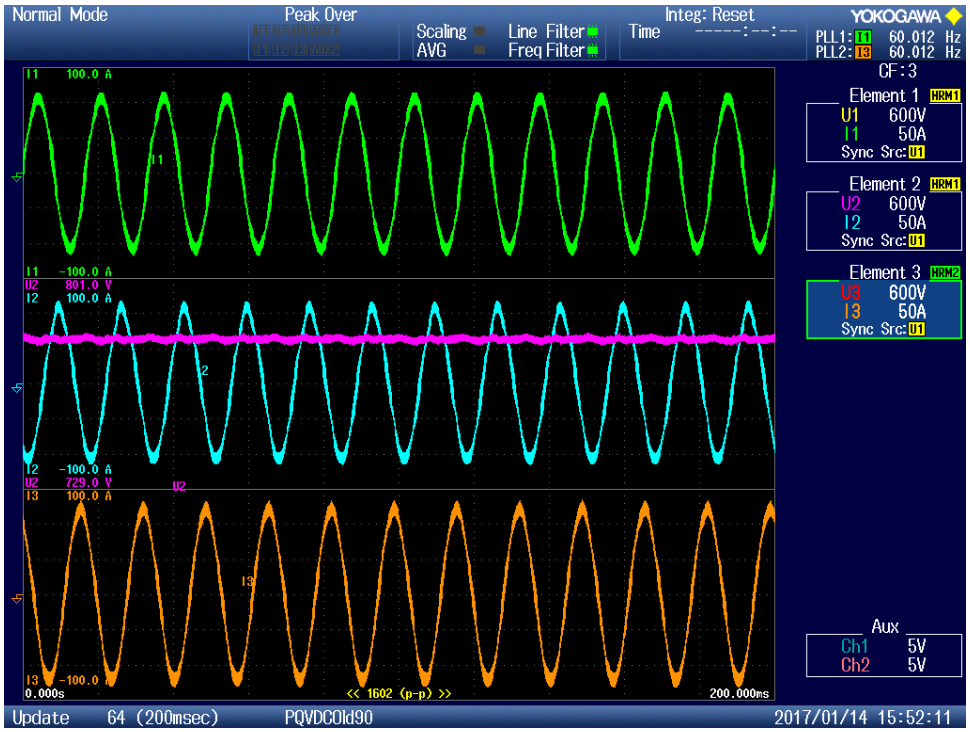

Figure 94 - "PQ" Consuming 0.8 pu Active Power at Unity Power Factor at 4860Hz without Line Voltages

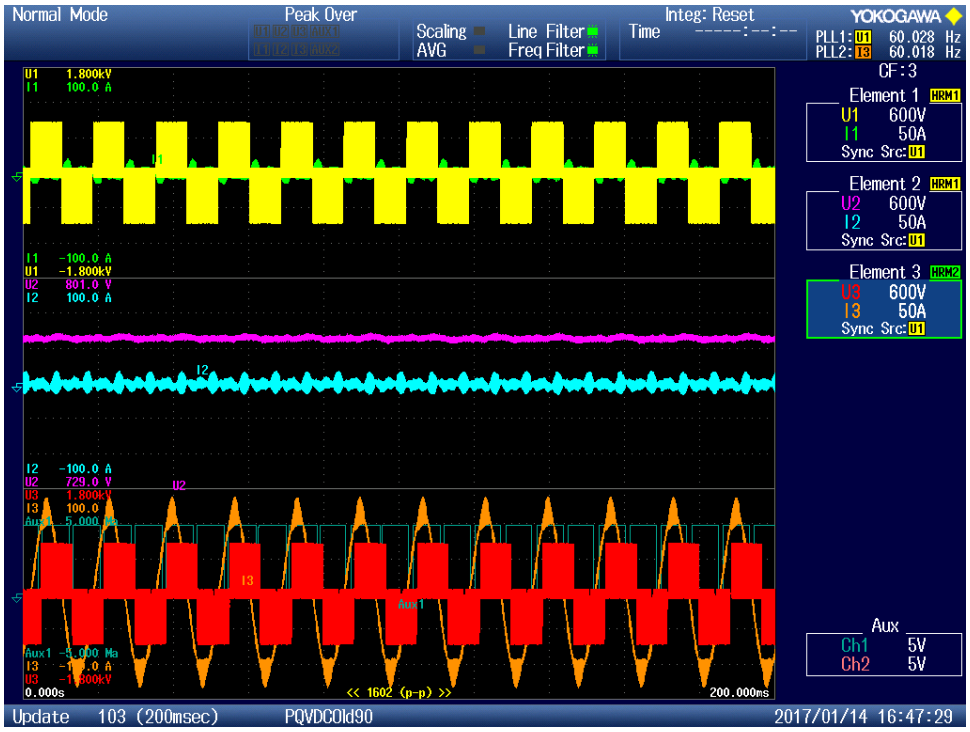

Figure 95 - "PQ" Supplying -0.8 pu Reactive Power at Capacitor Operation at 4860Hz

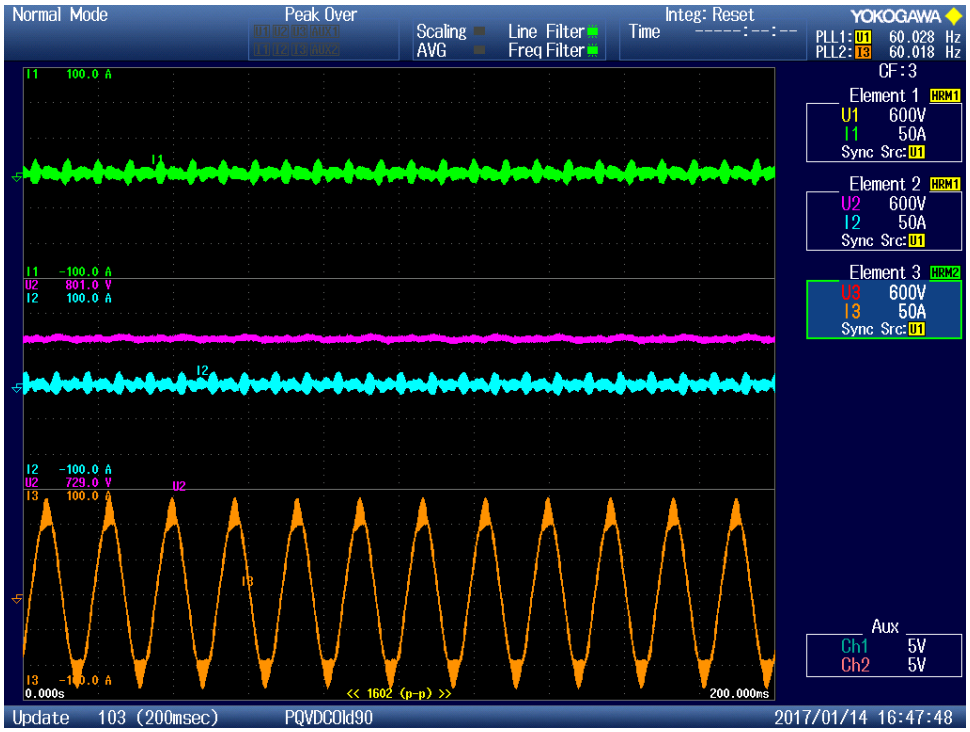

Figure 96 - "PQ" Supplying -0.8 pu Reactive Power at Capacitor Operation at 4860Hz without Line Voltages

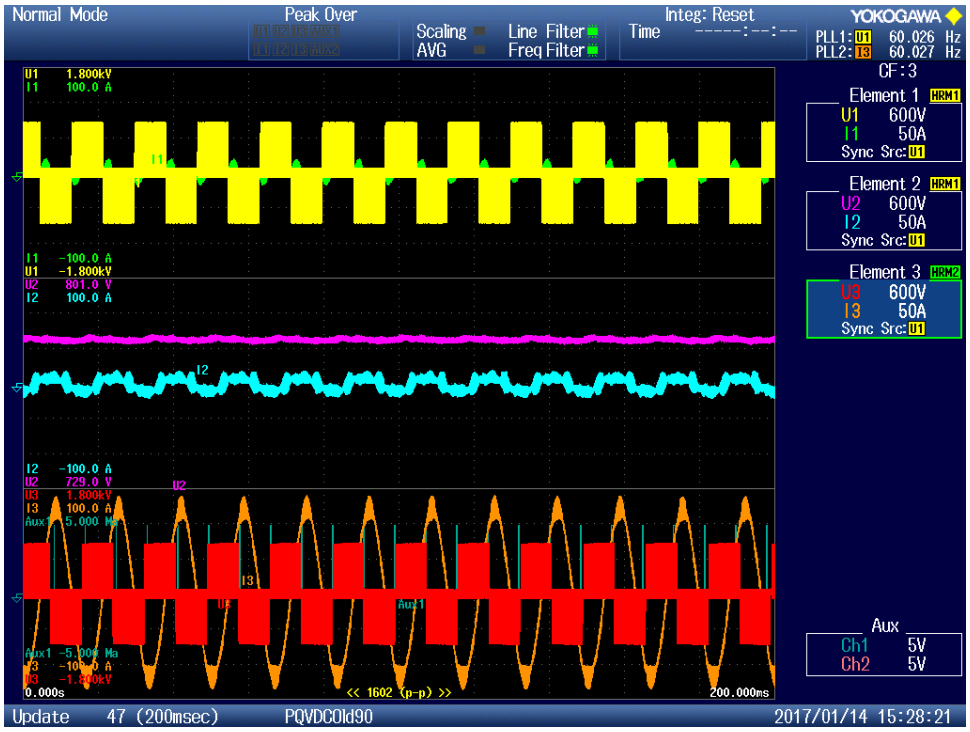

Figure 97 - "PQ" Consuming 0.8 pu Reactive Power at Inductor Operation at 4860Hz

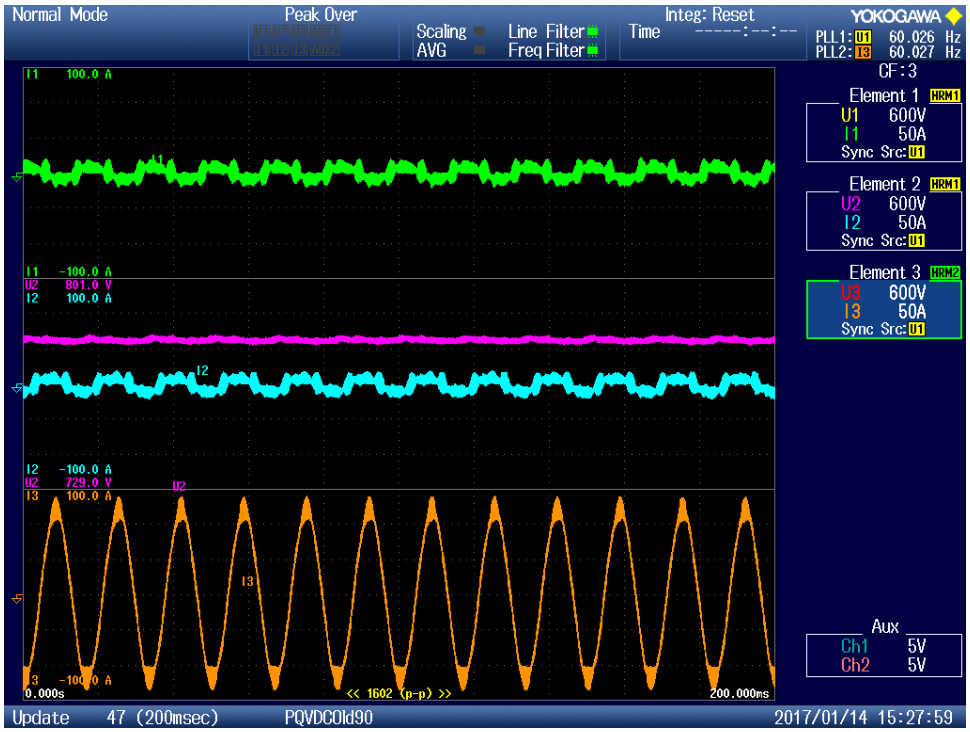

Figure 98 - "PQ" Consuming 0.8 pu Reactive Power at Inductor Operation at 4860Hz without Line Voltages

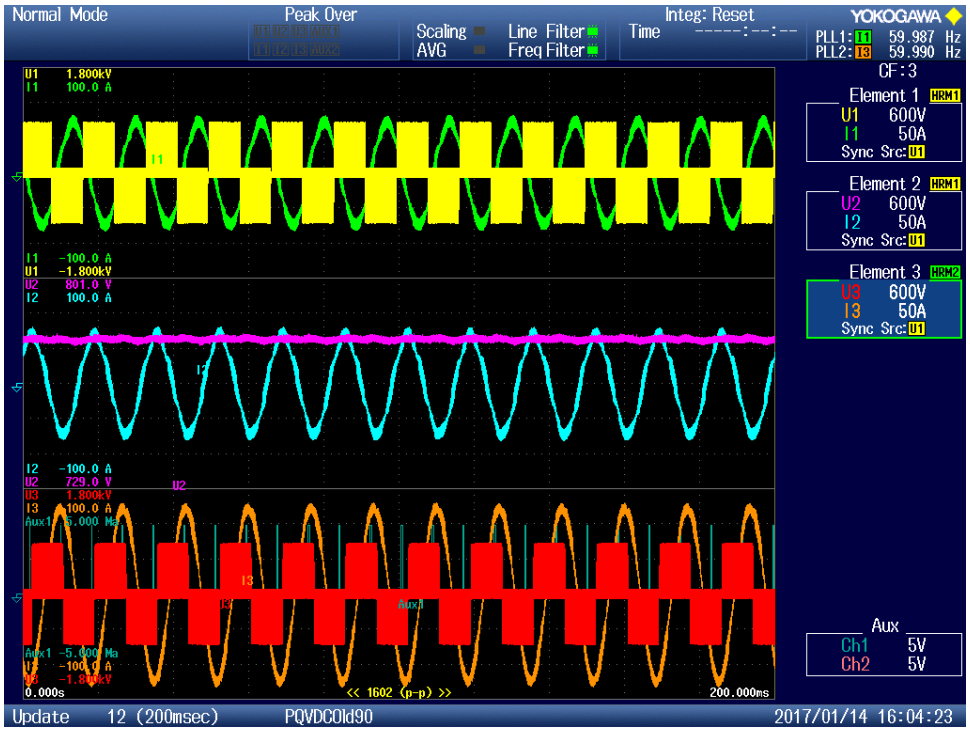

Figure 99 - "PQ" Consuming 0.57 pu Active and 0.57 pu Reactive Power at 4860Hz

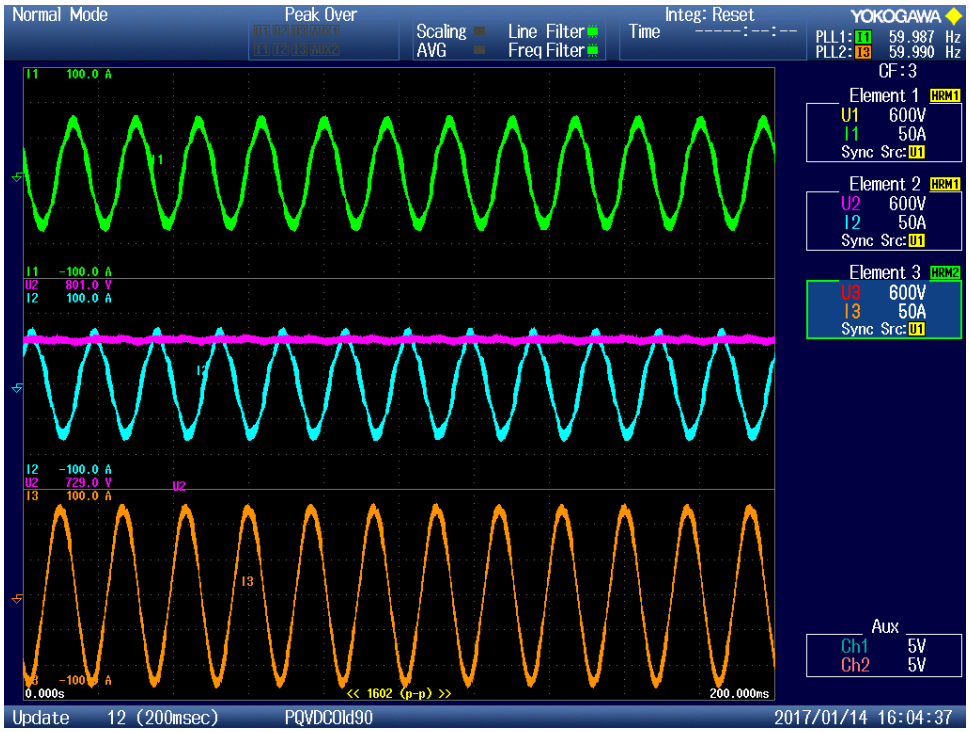

Figure 100 - "PQ" Consuming 0.57 pu Active and 0.57 pu Reactive Power at 4860Hz without Line Voltages

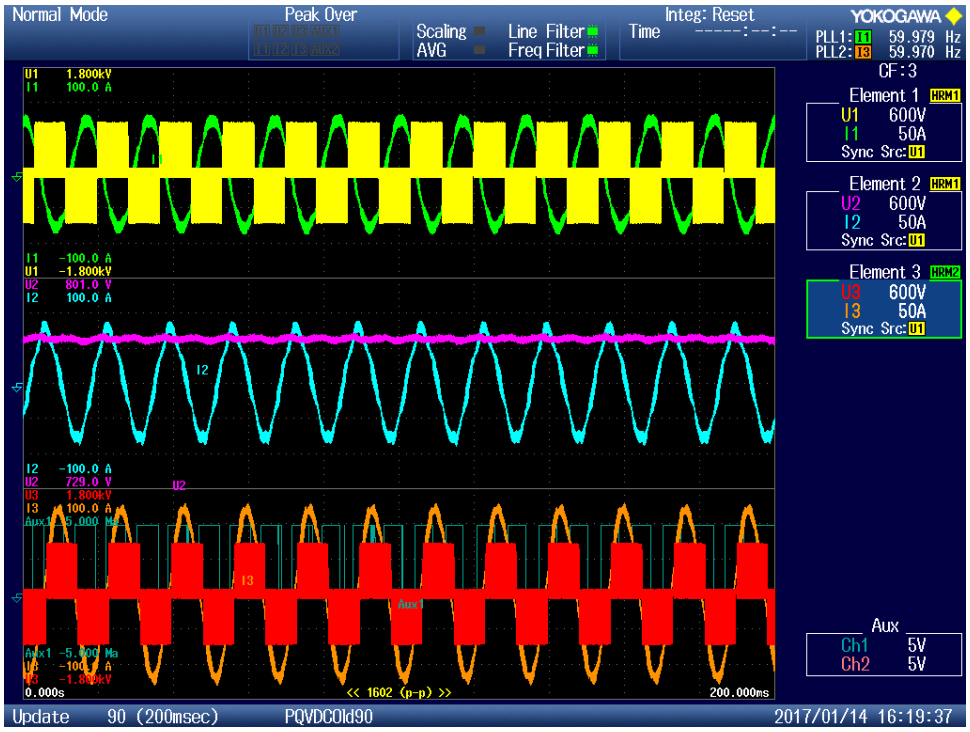

Figure 101 - "PQ" Consuming 0.57 pu Active and Supplying -0.57 pu Reactive Power at 4860Hz

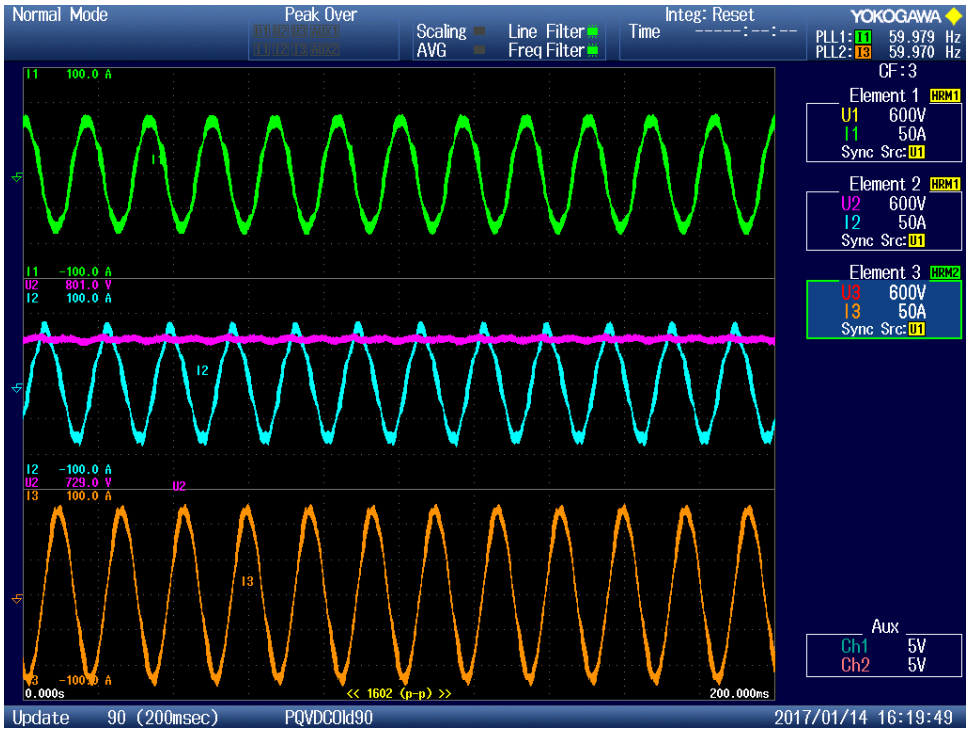

Figure 102 - "PQ" Consuming 0.57 pu Active and Supplying -0.57 pu Reactive Power at 4860Hz without Line Voltages

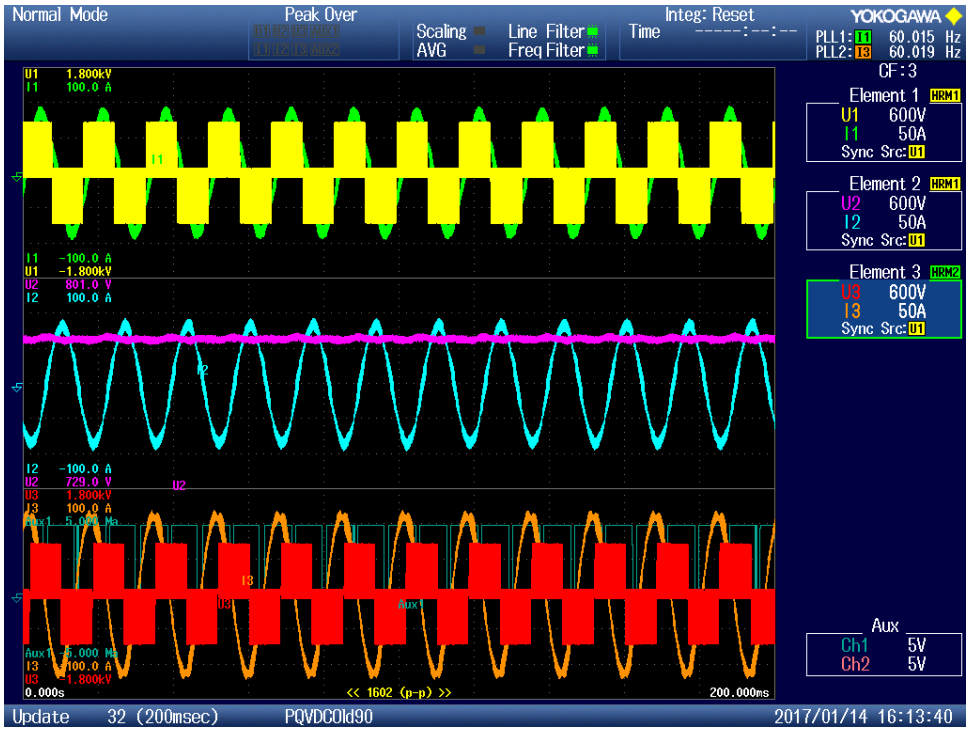

Figure 103 - "PQ" Supplying -0.57 pu Active and -0.57 pu Reactive Power at 4860Hz

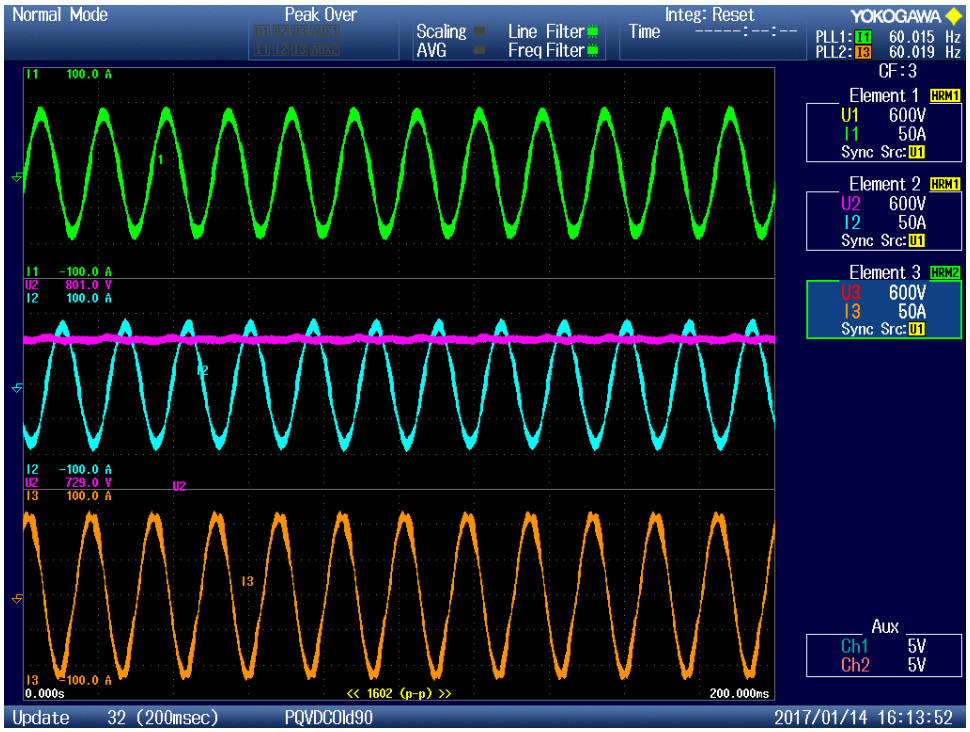

Figure 104 - "PQ" Supplying -0.57 pu Active and -0.57 pu Reactive Power at 4860Hz without Line Voltages

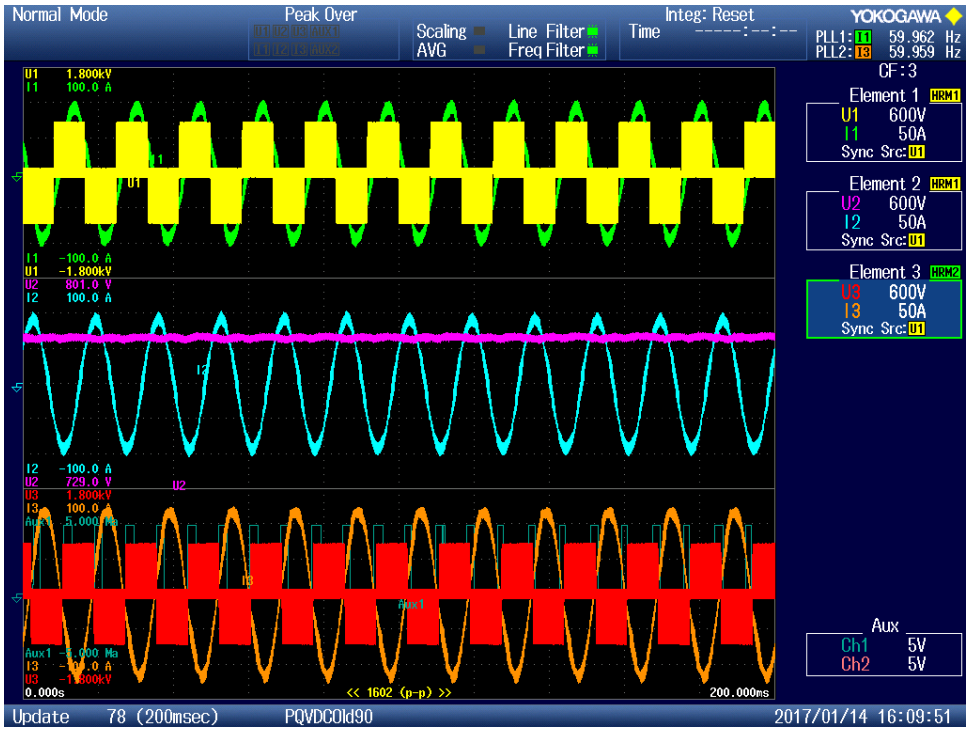

Figure 105 - "PQ" Supplying -0.57 pu Active and Consuming 0.57 pu Reactive Power at 4860Hz

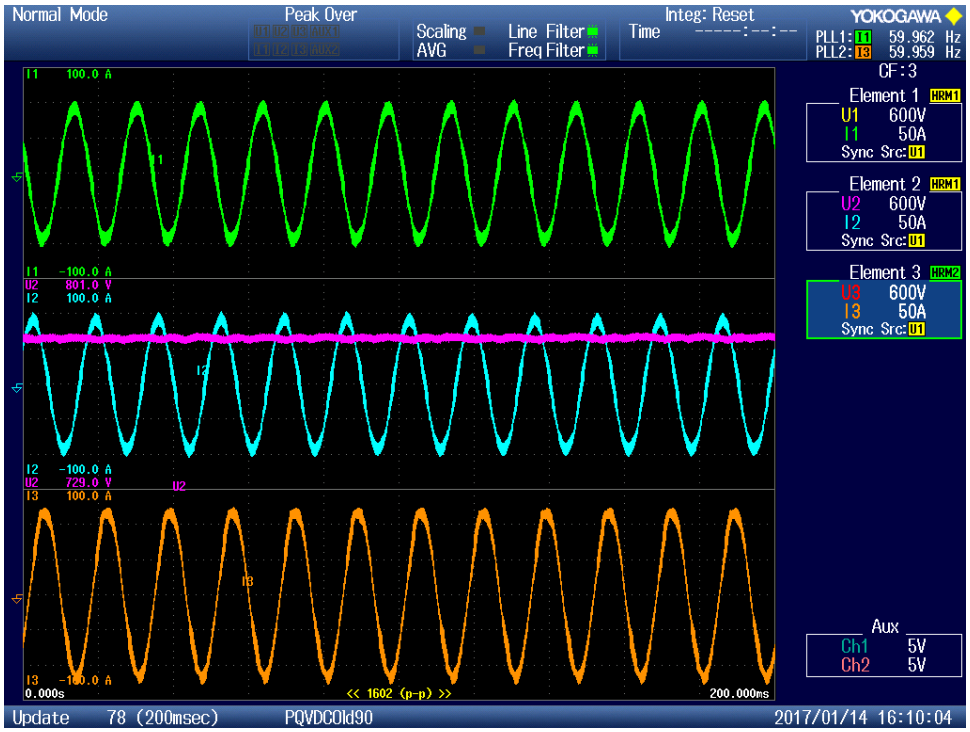

Figure 106 - "PQ" Supplying -0.57 pu Active and Consuming 0.57 pu Reactive Power at 4860Hz without Line Voltages

Once again, the eight possible modes of steady-state operation for the “PQ” converter were examined with 0.8 pu of complex power flow introduced by the “PQ” converter but with the switching frequency reduced to 4500Hz. For the Yokogawa recordings taken the “Element 2 V2” purple trace represents the DC bus voltage and the “Element 1 V1” yellow trace represents the phase A voltage measured between the “VDC” converter reactor and isolation transformer. The “Element 1 I1” green trace and “Element 2 I2” blue trace represent the “VDC” converter phase A and B currents. The “Element 3 V3” red trace represents the phase A voltage measured between the “PQ” converter reactor and isolation transformer while the “Element 3 I3” orange trace represents the “PQ” converter phase A current. Each recording is accompanied by a screen shot of the measurements screen on the Yokogawa. The harmonics that appear on the phase voltage measurements generated by the converters are only slightly attenuated since the measurement is between the reactor and isolation transformer.

The “PQ” converter supplies -0.8 pu of active power at unity power factor as shown in Figure 107 and Figure 108. The “PQ” converter consumes 0.8 pu of active power at unity power as shown in Figure 109 and Figure 110. The “PQ” converter supplies -0.8 pu of reactive power at capacitor operation as shown in Figure 111 and Figure 112. The “PQ” converter consumes 0.8 pu of reactive power at inductor operation as shown in Figure 113 and Figure 114. The “PQ” converter consumes 0.57 pu of active power and 0.57 pu of reactive power as shown in Figure 115 and Figure 116. The “PQ” converter consumes 0.57 pu of active power and supplies -0.57 pu of reactive power as shown in Figure 117 and Figure 118. The “PQ” converter supplies -0.57 pu of active power and -0.57 pu of reactive power as shown in Figure 119 and Figure 120. The “PQ” converter supplies -0.57 pu of active power and consumes 0.57 pu of reactive power as shown in Figure 121 and Figure 122.

The dynamic response to a step change commanded to the “PQ” converter to supply active power was examined. One cycle after the “VDC” converter maintains the DC bus voltage at 1 pu during no load operation; a -0.8 pu active power step change is commanded and achieved by the “PQ” converter as shown in Figure 123 and Figure 124.

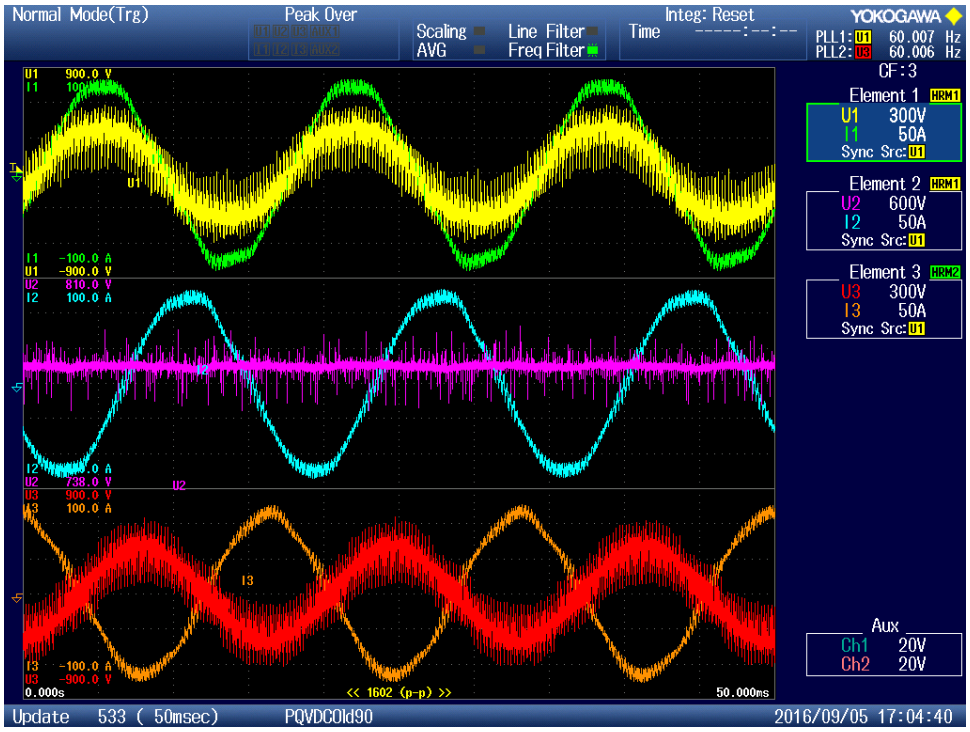

Figure 107 - "PQ" Supplying -0.8 pu Active Power at Unity Power Factor at 4500Hz

Figure 108 - Measurements of "PQ" Supplying -0.8 pu Active Power at Unity Power Factor at 4500Hz

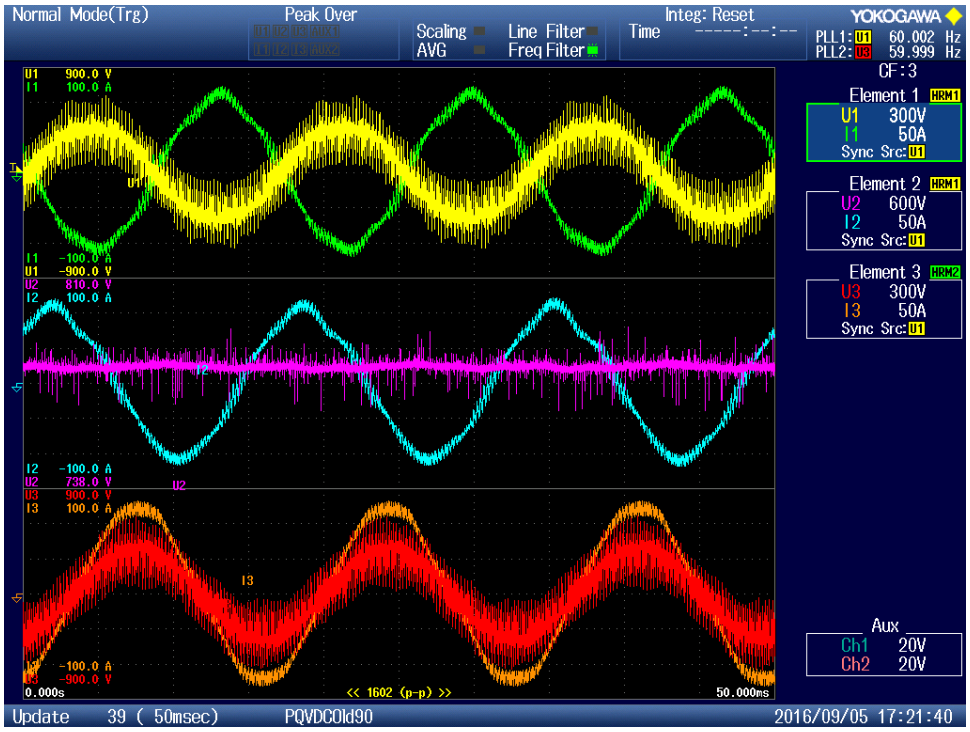

Figure 109 - "PQ" Consuming 0.8 pu Active Power at Unity Power Factor at 4500Hz

Figure 110 - Measurements of "PQ" Consuming 0.8 pu Active Power at Unity Power Factor at 4500Hz

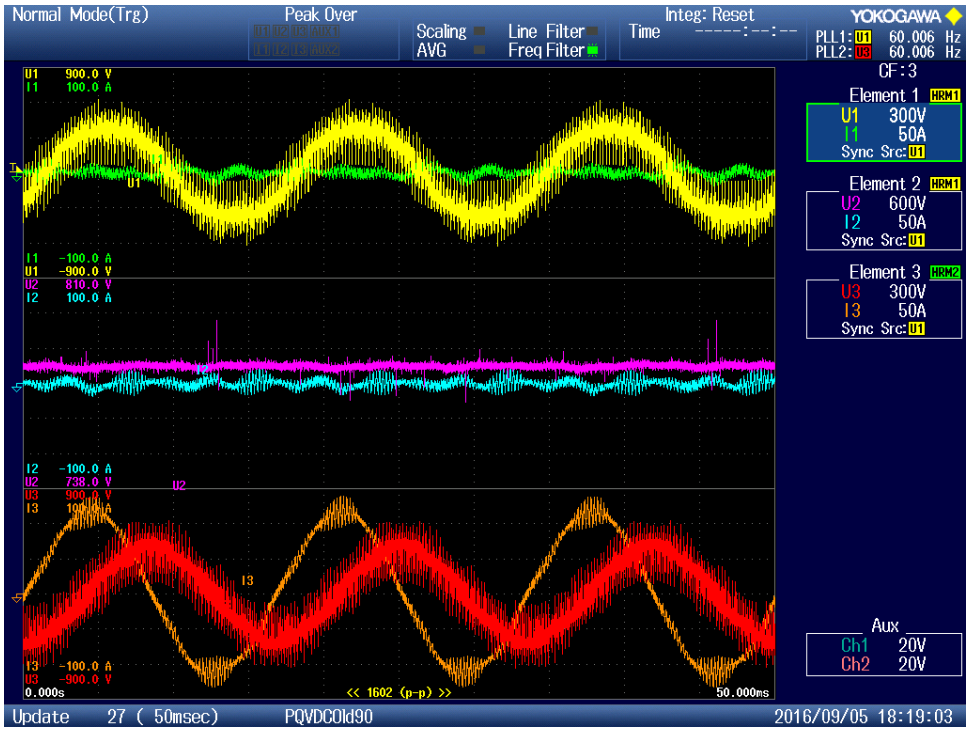

Figure 111 - "PQ" Supplying -0.8 pu Reactive Power at Capacitor Operation at 4500Hz

Figure 112 - Measurements of "PQ" Supplying -0.8 pu Reactive Power at Capacitor Operation at 4500Hz

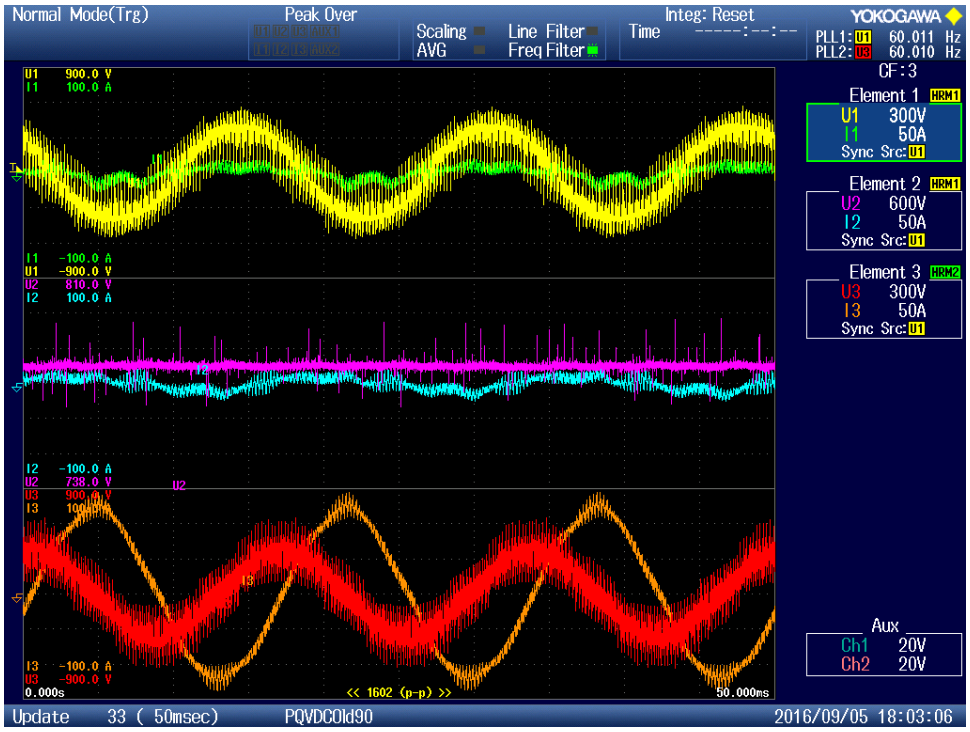

Figure 113 - "PQ" Consuming 0.8 pu Reactive Power at Inductor Operation at 4500Hz

Figure 114 - Measurements of "PQ" Consuming 0.8 pu Reactive Power at Inductor Operation at 4500Hz

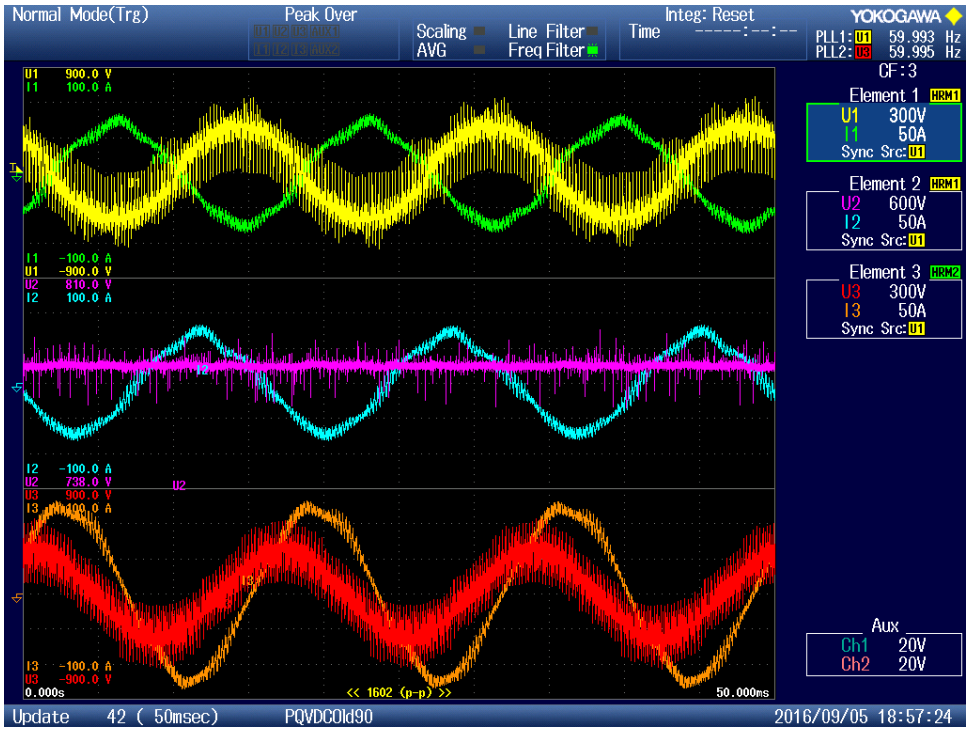

Figure 115 - "PQ" Consuming 0.57 pu Active and 0.57 pu Reactive Power at 4500Hz

Figure 116 - Measurements of "PQ" Consuming 0.57 pu Active and 0.57 pu Reactive Power at 4500Hz

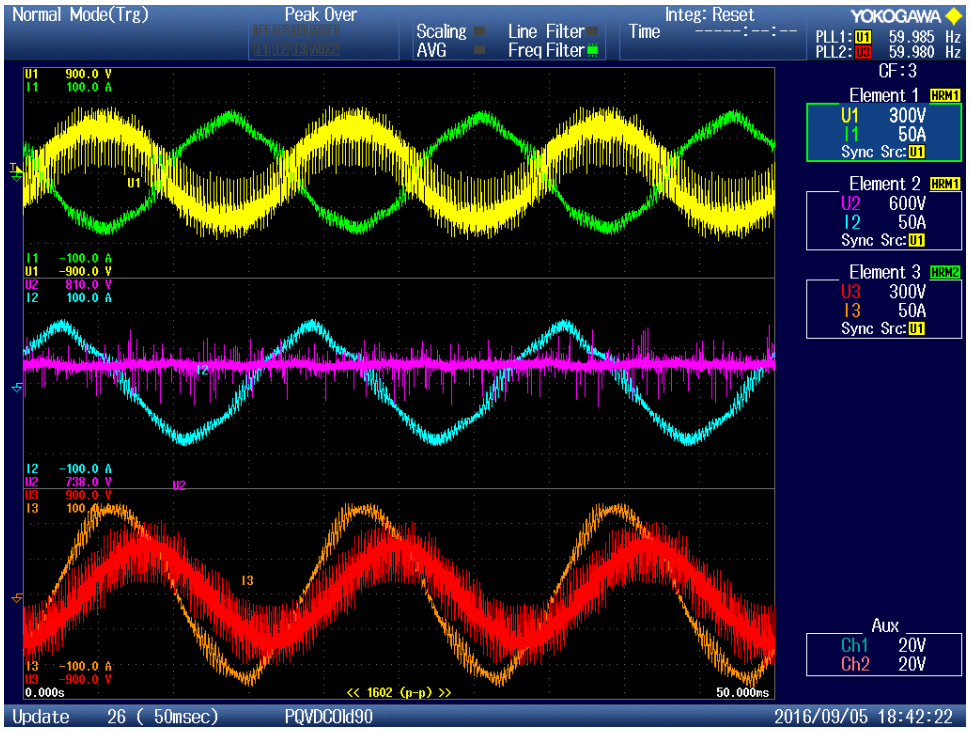

Figure 117 - "PQ" Consuming 0.57 pu Active and Supplying -0.57 pu Reactive Power at 4500Hz

Figure 118 - Measurements of "PQ" Consuming 0.57 pu Active and Supplying -0.57 pu Reactive Power at 4500Hz

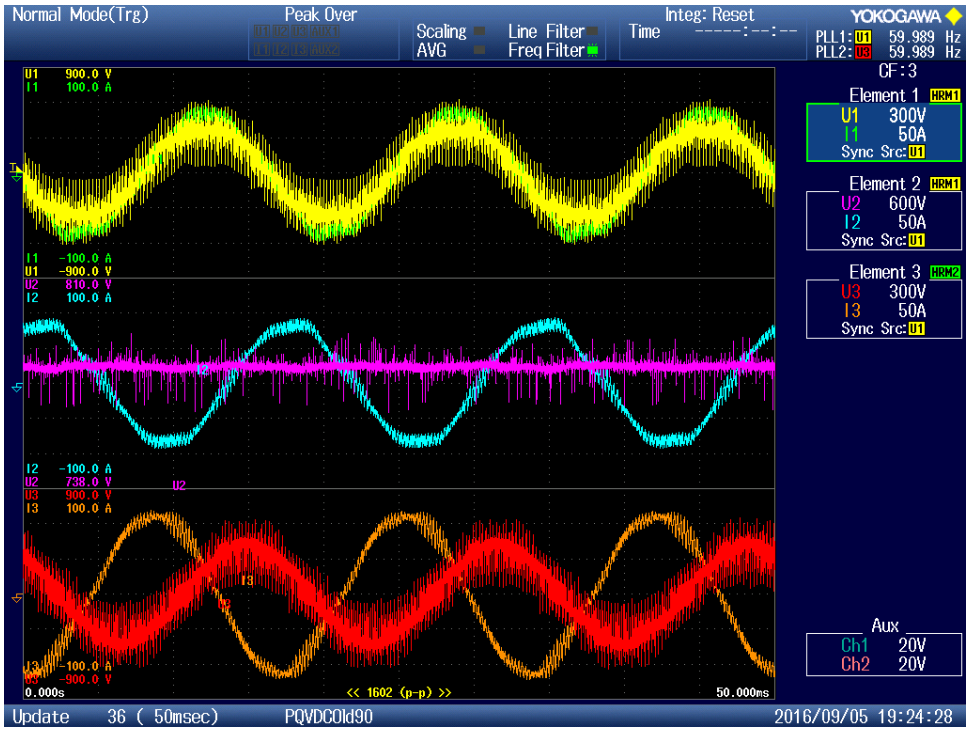

Figure 119 - "PQ" Supplying -0.57 pu Active and -0.57 pu Reactive Power at 4500Hz

Figure 120 - Measurements of "PQ" Supplying -0.57 pu Active and -0.57 pu Reactive Power at 4500Hz

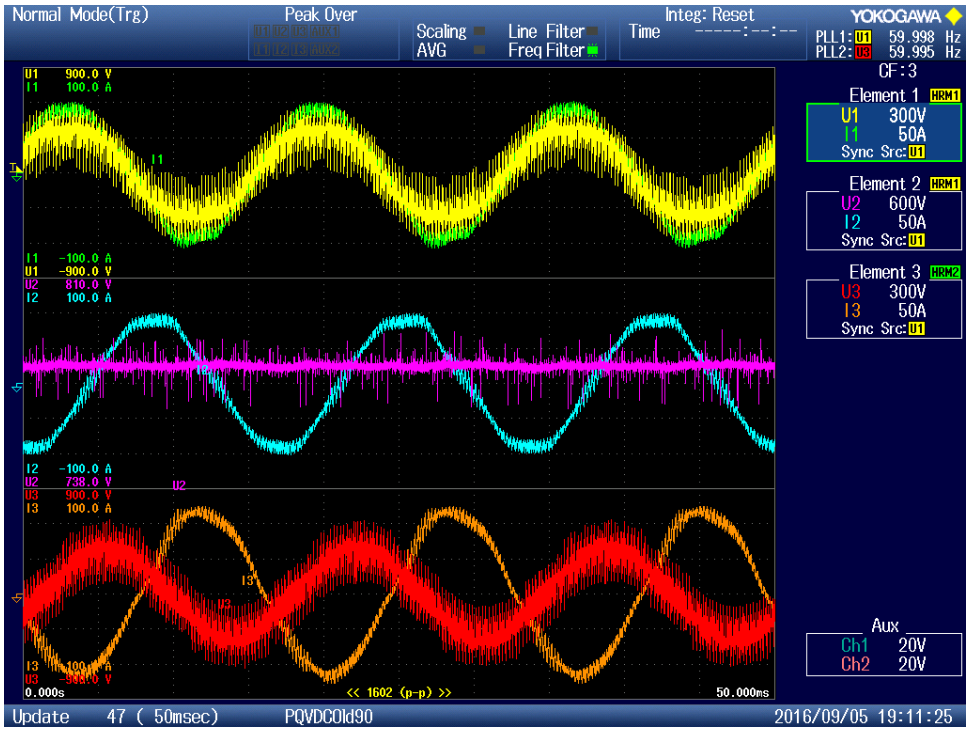

Figure 121 - "PQ" Supplying -0.57 pu Active and Consuming 0.57 pu Reactive Power at 4500Hz

Figure 122 - Measurements of "PQ" Supplying -0.57 pu Active and Consuming 0.57 pu Reactive Power at 4500Hz

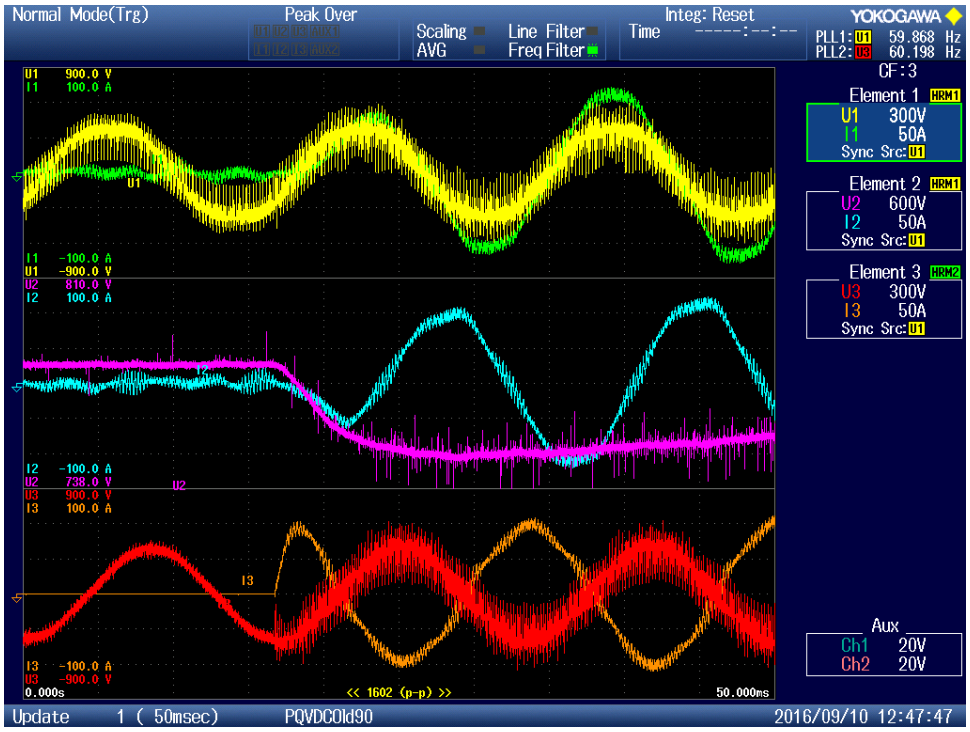

Figure 123 - "PQ" Supplying -0.8 pu Active Power Step at 4500Hz (50ms Window)

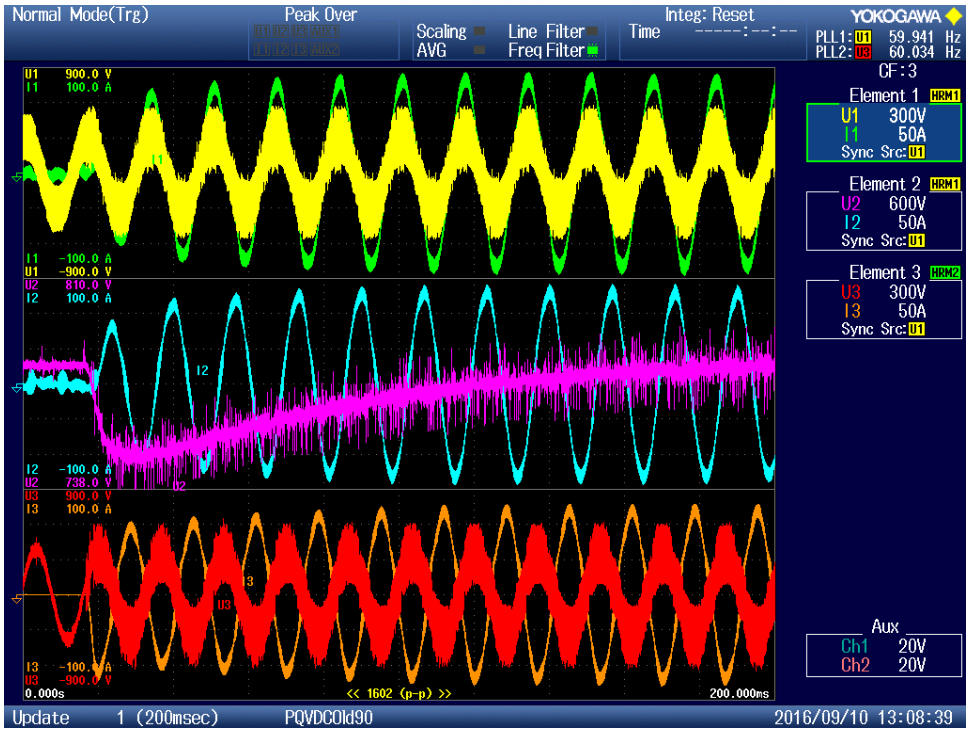

Figure 124 - "PQ" Supplying -0.8 pu Active Power Step at 4500Hz (200ms Window)

6.4. Measured vs. Analytical Harmonic Spectrum

Harmonics were measured during the steady-state operation of the "PQ" converter while operating at a switching frequency of 4860Hz. The harmonic voltages and currents generated by the converter were captured on the Yokogawa power analyzer with the major sideband harmonics shown in Figure 126 and Figure 128. The predicted voltage harmonic spectrum generated by the converter was obtained using (117), Table 3, and a numerical method to approximate the integrals with the major sideband harmonics shown in Figure 125. The predicted current harmonic spectrum generated by the converter was obtained using a rearranged form of (116) with the major sideband harmonics shown in Figure 127.

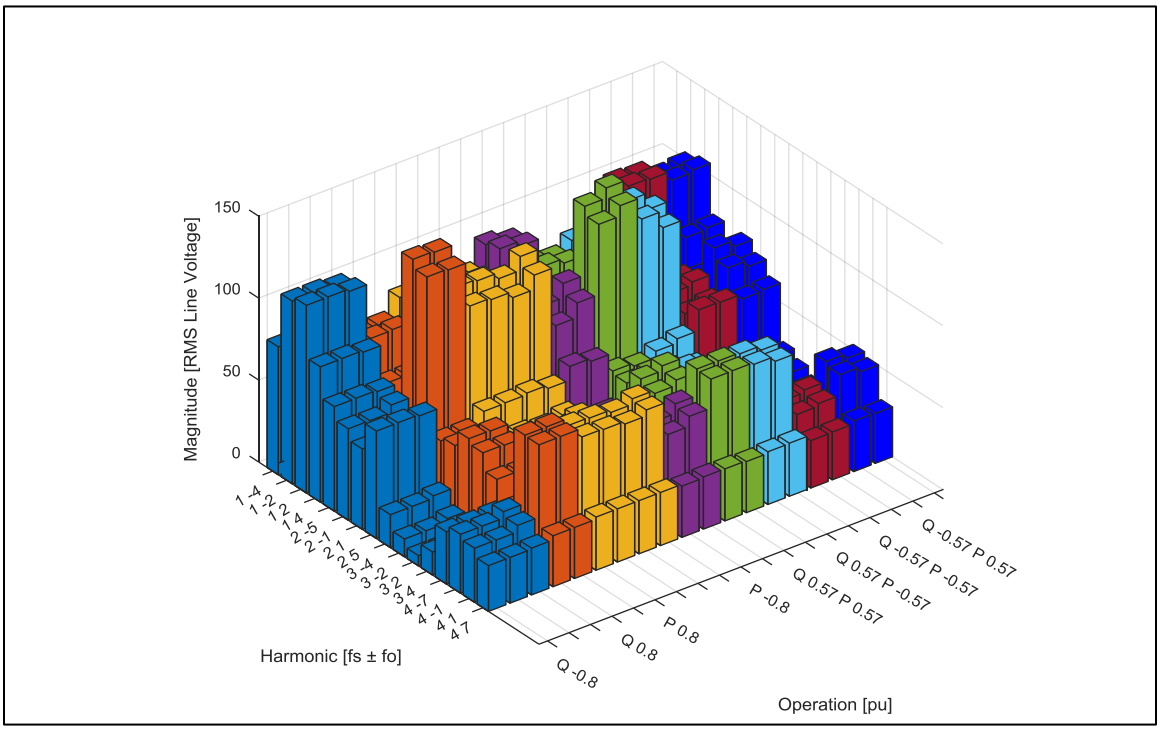

Figure 125 - Analytical "PQ" Converter Voltage Harmonic Spectrum at 4860Hz

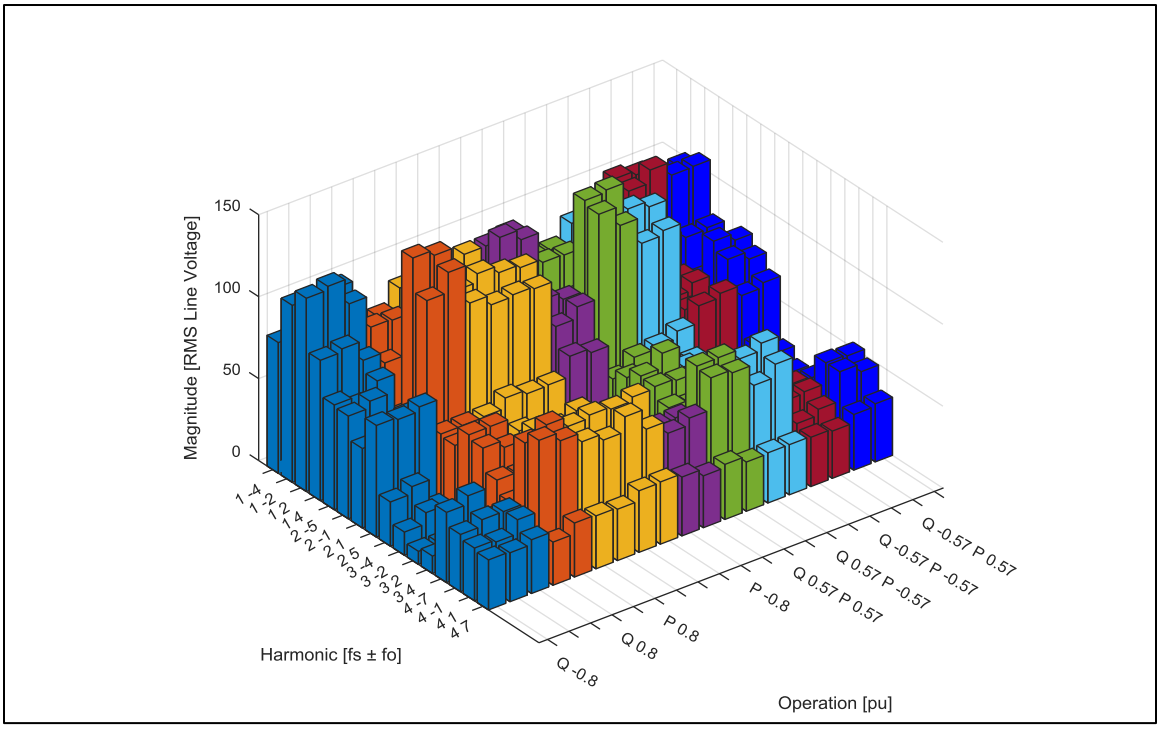

Figure 126 - Measured "PQ" Converter Voltage Harmonic Spectrum at 4860Hz

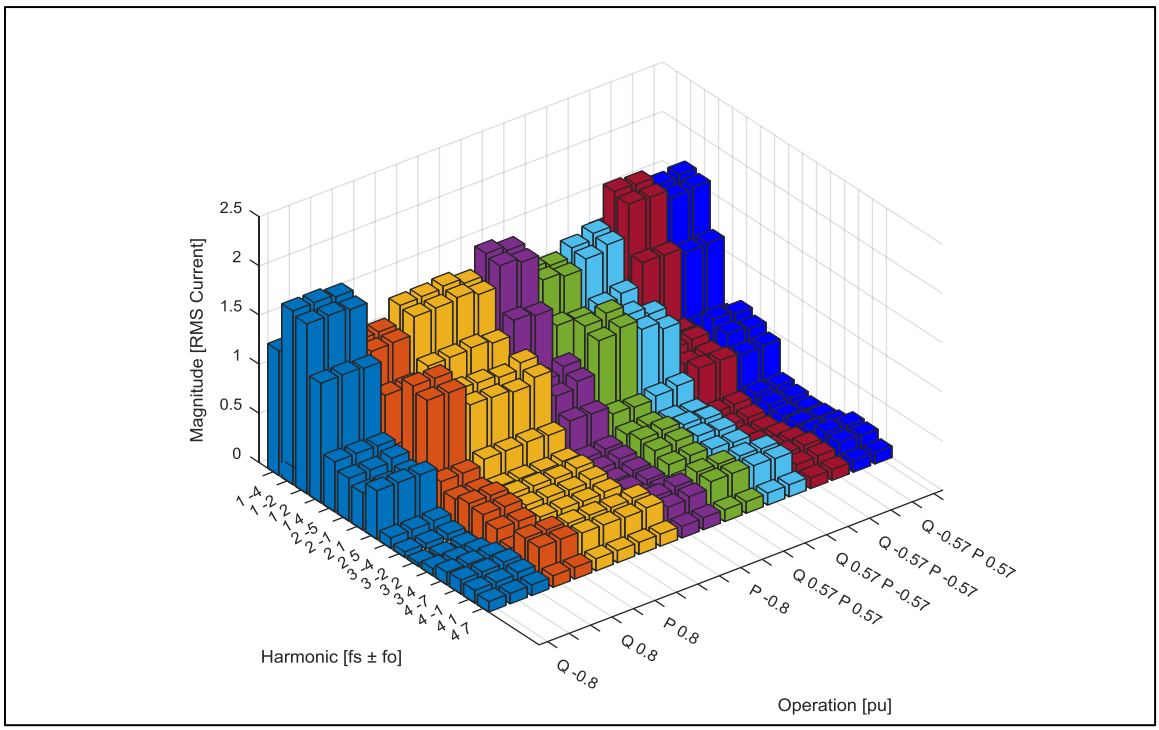

Figure 127 - Analytical "PQ" Converter Current Harmonic Spectrum at 4860Hz

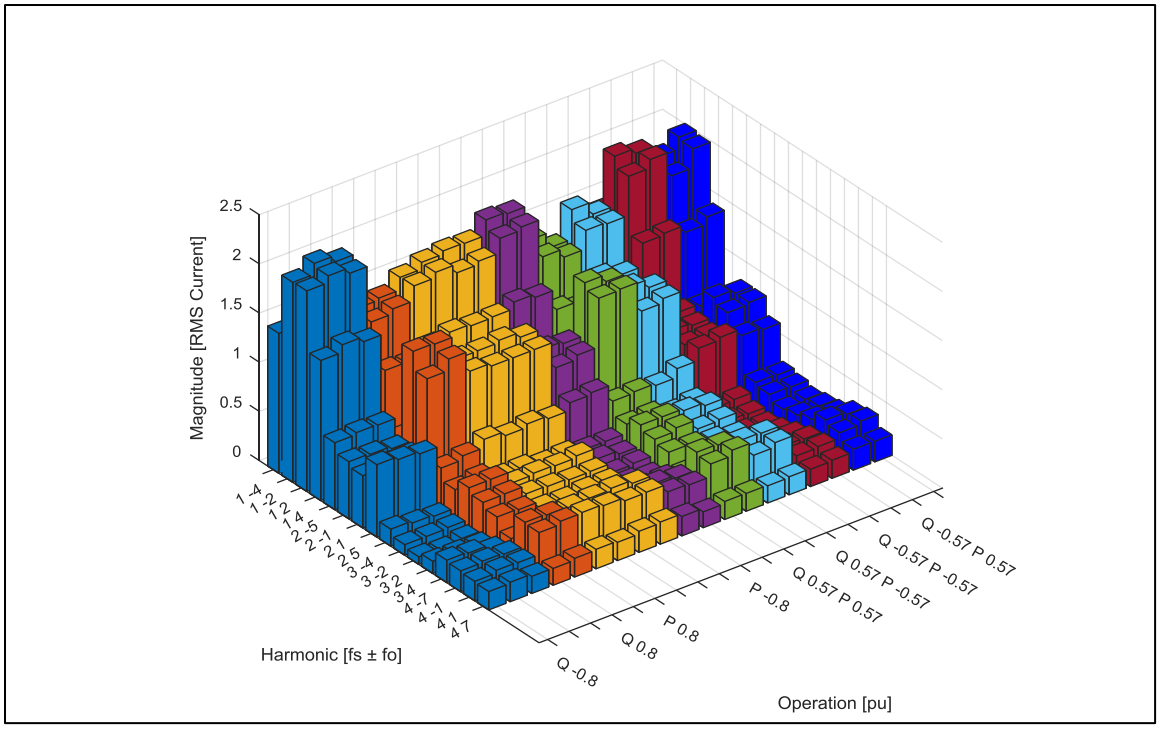

Figure 128 - Measured "PQ" Converter Current Harmonic Spectrum at 4860Hz

7. Conclusion

Examination of the harmonics showed consistent performance of the converters beginning with the analytical calculations, to the system-level model simulation, and finally with the project implementation. With the simplified models of the system transfer functions using the modulus and symmetrical optimum tuning techniques to establish baseline controller gains along with the substitution technique to determine the tradeoff between stability and bandwidth led to the proper selection of controller gains for the system. Detecting the grid voltage angle with the combination of the PLL and MFB analog filter for the voltage feedback measurement between the reactor and isolation transformer provides satisfactory performance even though the voltage harmonics are only slightly attenuated. Elimination of the AC capacitors by selecting the minimum required switching frequency to meet IEEE 519-2014 is an acceptable solution as long as the duty cycle of the converter is well understood as to not to exceed the thermal margins of the IGBTs. The analytical calculation for the voltage harmonic spectrum proved to be accurate in estimating the measured converter produced harmonics, however additional research and testing is required to accurately predict the current harmonic spectrum.

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Appendix A: Per Unit Values

[34, pp. 426-429]

Base Values for Converter AC-Side		
Quantity	Symbol & Equation	Description
Power	$P_b = \frac{3}{2} V_b I_b$	VA Rating of converter
Voltage	$V_b = \hat{V}_{phase}$	Amplitude of line-to-neutral nominal voltage
Current	$I_b = \frac{2P_b}{3V_b}$	Amplitude of nominal current selected
Impedance	$Z_b = \frac{V_b}{I_b}$	
Capacitance	$C_b = \frac{1}{Z_b \omega_b}$	
Inductance	$L_b = \frac{Z_b}{\omega_b}$	
Frequency	$\omega_b = \omega_o$	Grid frequency rad/sec.
Actual Values for Converter AC-Side		
Inductance	$L = L_b L_{pu}$	
Resistance	$R = Z_b R_{pu}$	
Grid Voltage, d-axis	$v_{gd} = V_b v_{gd,pu}$	
Grid Voltage, q-axis	$v_{gq} = V_b v_{gq,pu}$	
Converter Voltage, d-axis	$v_{cd} = V_b v_{cd,pu}$	
Converter Voltage, q-axis	$v_{cq} = V_b v_{cq,pu}$	
Grid Current, d-axis	$i_{gd} = I_b i_{gd,pu}$	
Grid Current, d-axis	$i_{gq} = I_b i_{gq,pu}$	
Frequency	$\omega = \omega_b \omega_{pu}$	

Base Values for Converter DC-Side		
Power	$P_{b,dc} = V_{b,dc} I_{b,dc} = P_b$	AC and DC Side Power are equal
Voltage	$V_{b,dc} = 2V_b$	
Current	$I_{b,dc} = \frac{3}{4} I_b$	
Impedance	$R_{b,dc} = \frac{8}{3} Z_b$	
Capacitance	$C_{b,dc} = \frac{3}{8} C_b$	
Inductance	$L_{b,dc} = \frac{8}{3} L_b$	
Actual Values for Converter DC-Side		
Capacitance	$C_{dc} = C_{b,dc} C_{b,pu}$	

Appendix B: Coordinate Transformations

[32]

$$\vec{f}_{\alpha\beta} = \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix}$$

$$\vec{f}_{dq} = \begin{bmatrix} f_d \\ f_q \end{bmatrix}$$

$$\begin{aligned}
\vec{g}_{\alpha\beta} &= \frac{d}{dt}\vec{f}_{\alpha\beta} \\
&= \frac{d}{dt}\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \\
&= \frac{d}{dt}\left\{\begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix}\begin{bmatrix} f_d \\ f_q \end{bmatrix}\right\} \\
&= \begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix}\vec{g}_{dq} \\
&= \begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix}\frac{d}{dt}\begin{bmatrix} f_d \\ f_q \end{bmatrix} + \left(\omega_{dq} - \omega_{\alpha\beta}\right)\begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix}\begin{bmatrix} \cos\frac{\pi}{2} & -\sin\frac{\pi}{2} \\ \sin\frac{\pi}{2} & \cos\frac{\pi}{2} \end{bmatrix}\begin{bmatrix} f_d \\ f_q \end{bmatrix}
\end{aligned}$$

$$\begin{aligned}
\vec{g}_{dq} &= \frac{d}{dt}\vec{f}_{dq} \\
&= \frac{d}{dt}\begin{bmatrix} f_d \\ f_q \end{bmatrix} + \left(\omega_{dq} - \omega_{\alpha\beta}\right)\begin{bmatrix} \cos\frac{\pi}{2} & -\sin\frac{\pi}{2} \\ \sin\frac{\pi}{2} & \cos\frac{\pi}{2} \end{bmatrix}\begin{bmatrix} f_d \\ f_q \end{bmatrix}
\end{aligned}$$

$$f_a + f_b + f_c = 0$$

$$\begin{aligned}
\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \\
&= M_1\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}
\end{aligned}$$

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos\varphi & \sin\varphi \\ -\sin\varphi & \cos\varphi \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix}$$
$$= M_2 \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix}$$

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix}$$
$$= M_2^t \begin{bmatrix} f_d \\ f_q \end{bmatrix}$$

Appendix C: Modulus Optimum

Magnitude Optimum [7, p. 166]

$$G_{BO} = \frac{K}{(1+sT_1)(1+sT_2)} where T_1 > T_2$$

$$K_p = \frac{T_1}{2KT_2}$$

$$T_i = T_1$$

Appendix D: Proportional-Integral Controller Forms

$$
\begin{aligned}
G_{pi,form1} &= K_p + \frac{K_i}{s} \\
&= K_p + \frac{K_p}{sT_i} \therefore T_i = \frac{K_p}{K_i} \\
&= \frac{sK_p}{s} + \frac{\frac{K_p}{T_i}}{s} \\
&= \frac{sK_pT_i + K_p}{sT_i} \\
G_{pi,form2} &= K_p \frac{1 + sT_i}{sT_i} \\
&= K_p \frac{1 + s\frac{K_p}{K_i}}{s\frac{K_p}{K_i}} \\
&= \frac{K_p + s\frac{K_p^2}{K_i}}{s\frac{K_p}{K_i}} \\
&= \frac{K_i + sK_p}{s} \\
G_{pi,form3} &= K_i \frac{\left(1 + s\frac{K_p}{K_i}\right)}{s}
\end{aligned}
\tag{134}
$$

Appendix E: Discretization Methods

[31, p. 51]

Method	Z-Form	3% Distortion Limit
Backward Euler	$s = \frac{z-1}{zT_s}$	$\frac{f_s}{f} > 20$
Forward Euler	$s = \frac{z-1}{T_s}$	$\frac{f_s}{f} > 20$
Tustin (Trapezoidal) (Bilinear)	$s = \frac{2}{T_s}\frac{z-1}{z+1}$	$\frac{f_s}{f} > 10$

Appendix F: Delta/Wye Transformer Equivalent Circuit

Primary and Secondary Winding Resistance [per-unit]	$R_{1,pu} = R_{2,pu} = \frac{R_{pu}}{2}$
Primary and Secondary Winding Reactance [per-unit]	$X_{1,pu} = X_{2,pu} = \frac{X_{pu}}{2}$
Primary and Secondary Winding Inductance [per-unit]	$L_{1,pu} = L_{2,pu} = \frac{X_{pu}}{2}$
Base Primary Winding Resistance and Reactance [ohms]	$R_{b,primary} = X_{b,primary} = \frac{3V_{b,primary\ xfmr}^2}{S_{b,xfmr}}$
Base Primary Winding Inductance [henries]	$L_{b,primary} = \frac{X_{b,primary}}{2\pi f}$
Base Secondary Winding Resistance and Reactance [ohms]	$R_{b,secondary} = X_{b,secondary} = \frac{V_{b,secondary\ xfmr}^2}{S_{b,xfmr}}$
Base Secondary Winding Inductance [henries]	$L_{b,secondary} = \frac{X_{b,secondary}}{2\pi f}$
Primary Winding Resistance [ohms]	$R_1 = R_{b,primary} R_{1,pu}$
Primary Winding Leakage Reactance [ohms]	$X_1 = X_{b,primary} X_{1,pu}$
Primary Winding Leakage Inductance [henries]	$L_1 = L_{b,primary} L_{1,pu}$
Secondary Winding Resistance [ohms]	$R_2 = R_{b,secondary} R_{2,pu}$
Secondary Winding Leakage Reactance [ohms]	$X_2 = X_{b,secondary} X_{2,pu}$
Secondary Winding Leakage Inductance [henries]	$L_2 = L_{b,secondary} L_{2,pu}$

Table 14 - Delta/Wye Primary and Secondary Transformer Equivalent Circuit Equations

Magnetization Series Resistance [ohms]	$R_{m,series} = \frac{P_{losses,\,no\,load} / 3}{I_{no\,load}^2}$
Magnetization Series Impedance [ohms]	$Z_{m,series} = \frac{V_b}{I_{no\,load}}$
Magnetization Series Reactance [ohms]	$X_{m,series} = \sqrt{Z_{m,series}^2 - R_{m,series}^2}$
Magnetization Resistance [ohms]	$R_m = \frac{\left(R_{m,series}^2 + X_{m,series}^2\right)}{R_{m,series}}$
Magnetization Reactance [ohms]	$X_m = \frac{\left(R_{m,series}^2 + X_{m,series}^2\right)}{X_{m,series}}$
Magnetization Inductance [henries]	$L_m = \frac{X_m}{2\pi f}$
Magnetization Resistance [per-unit]	$R_{m,pu} = \frac{R_m}{R_{b,primary}}$
Magnetization Reactance [per-unit]	$X_{m,pu} = \frac{X_m}{X_{b,primary}}$
Magnetization Inductance [per-unit]	$L_{m,pu} = \frac{L_m}{L_{b,primary}}$

Table 15 - Delta/Wye Transformer Magnetization Equivalent Circuit Equations