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# Solid State Protective Device Topological Trade-offs for Mvdc Systems

Vikas Singh

*University of Wisconsin-Milwaukee*

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SOLID STATE PROTECTIVE DEVICE TOPOLOGICAL TRADE-OFFS FOR MVDC  
SYSTEMS

by

Vikas Singh

A Thesis Submitted in  
Partial Fulfillment of the  
Requirements for the Degree of

Master of Science  
in Engineering

at

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December 2016

## ABSTRACT

### SOLID STATE PROTECTIVE DEVICE TOPOLOGICAL TRADE-OFFS FOR MVDC SYSTEMS

by

Vikas Singh

The University of Wisconsin-Milwaukee, 2016  
Under the Supervision of Professor Robert M. Cuzner

Presently accepted approaches to protection are “Unit-Based” which means the power converter(s) feeding the bus coordinate with no-load electromechanical switches to isolate faulted portions of the bus. However, “Breaker-Based” approaches, which rely upon solid state circuit breakers for fault mitigation can result in higher reliability of power and potentially higher survivability. The inherent speed of operation of solid state protective devices will also play a role in fault isolation, hence reducing stress level on all system components. A comparison study is performed of protective device topologies that are suitable for shipboard distribution systems rated between 4kVdc and 20kVdc from the perspectives of size and number of passive components required to manage the commutation energy during sudden fault events and packaging scalability to higher current and voltage systems. The implementation assumes a multi-chip Silicon Carbide 10kV, 240A MOSFET/JBS diode module. A static fault simulator device is proposed to characterize DC faults.

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When I look back at this two-year journey, I feel confident to say that I learned so much new about power electronics. This is just a start, learning process should never stop and I will always keep this spark alive in me.

## **Chapter 1 Introduction**

The main focus of this thesis is to assess the protection topologies for next generation “breaker” based DC distribution system. Increase in large scale integration of distributed energy resources and their bidirectional power flow requirements leads to application of DC or AC/DC hybrid micro grid, but instead of many advantages of dc systems there are still some issues which need attention for efficient and reliable performance of the system. Unavailability of zero crossing phenomenon in dc current has made the protection more challenging. Conventional approach of fault detection and protection may not work because of their dependence on voltage droop to ensure tripping of closest relay to trip of first. Also the fault current in upstream and downstream will same so it’s not suitable for convention relay coordination scheme. Current DC system still employ conventional devices such as AC side circuit breakers which are relatively slow and may result in interruption of power in major part of the grid. In present scenario there is a need of fast acting, high rated and smart protective devices in medium voltage DC (MVDC) protection system.

### **1.1 Background and motivation**

Conventional AC distribution protection relies upon the fact the further away a short circuit occurs from the utility feed, the higher the impedance and thus the lower the inherent short circuit fault impedance. This concept is aided by the fact that AC distribution systems consist of transformer feeds that look like a reactive impedance to upstream feeds. As a result, electromechanical protective devices can utilize time-trip settings to localize the effect of a fault. This is the principle of protective device coordination between upstream and downstream protective devices where the goal is to isolate a fault closest to the fault location with minimal impact to the surrounding unfaulted portions of the system.

Both AC and DC Micro grids present a special challenge for protection. Distributed energy resources (DERs) distributed along the grid can operate while connected to the main utility or in disconnected (islanded) configurations. Fault protection within the micro grid when it is islanded is particularly problematic because of the changing status of the DERs connected into the micro grid [1][2]. When the number of connected DER units change the fault current available to the grid changes as well as the potential fault current flow paths. Also, the micro grid topology may be looped, meshed, radial, or a mixture of multiple networks of different topologies. So, ensuring reliable fault protection in a micro grid is much more complex than conventional systems and most approaches must rely heavily upon both inter-device and central communications. These complications are further compounded by the fact that DERs interface to the micro grid through power converters that have capacitive filters on their outputs and that must current limit in order to self-protect. As a result, two problematic issues arise: (1) when a fault is suddenly applied the first few milliseconds of the fault characteristic are dictated by the total capacitance connected into the grid and the equivalent cable inductance and resistance to the fault. This fault characteristic will have a very high peak which will tend to trip the electromechanical devices on peak instantaneous trip functions that are in the path of the fault. There is no guarantee that the protective device closest to the fault will trip, especially because everything that is connected into the grid with a capacitive filter contributes to the fault current. (2) Once the initial capacitor discharge event is over, the power converter(s) will hard limit the output current to a level that may not be sufficient to provide margin between upstream and downstream protective devices for autonomous trip level based coordination or the converters may trip off altogether. The opposite problem may also occur: as more DERs are connected to the grid the available fault current increases. As a result, any protective scheme using conventional relaying approaches must be widely adaptable to changing

conditions. AC micro grid can build upon existing protective infrastructure but the above problems result in a high dependence upon inter-device communications and a difficult trade-off between system safety, cost and power continuity.

The approaches to protection in micro grids may be divided into two categories: “Unit-Based” and “Breaker-Based”. “Unit-Based” approaches apply to DC or hybrid AC/DC micro grids whereas AC micro grids almost without exception utilize “Non-Unit-Based” protective relaying, as is the standard practice for AC distribution. Still, “Non-Unit-Based” protection has some advantages for DC systems if it can be made to work. With “Unit-Based” protection, the power converter “Units” that interface DERs and energy sources to the grid are solely responsible for protective functions and may communicate with isolating no load switches for the purpose of isolating faults from the system. For “Breaker-Based” protection, the power converter “Units” play no role in protection and all protection is allocated to external current limiting and galvanic isolating devices. “Unit-Based” approaches [3] rely exclusively upon the fault-feeding power converters to limit fault currents when a fault occurs while, “Breaker-Based” approaches, rely exclusively upon circuit breakers, fuses, Solid State Protective Devices (SSPDs) or hybrid SSPDs (i.e. SSPDs with electromechanical bypass contactors for non-faulted conditions) to isolate the fault without participation of the power converters. “Breaker-Based” approaches acknowledge that power converter(s) feeding the fault must current limit in order to self-protect, so the breaker current limiting mechanism must act quickly enough mitigate fault effects or else widespread system loss of power occurs[4]-[6]. Therefore, only SSPDs, as opposed to electromechanical devices or hybrid SSPDs will have sufficient time response to mitigate current limiting of upstream converters if power interruption mitigation hardware is to be avoided. “Unit-Based” approaches deliberately utilize current limiting capabilities of the bus-feeding Power Generator Modules (PGM) to drive

the voltage to zero on the affected bus in order to eliminate fault current so that no load electromechanical DC disconnect switches can isolate the fault and work best when the power converter isolates faults in a branch it is feeding from a main distribution bus[7].

## **Chapter 2 DC Fault characterization (standards and experimental validation)**

### **2.1 Types of faults in DC**

In this thesis the term “fault” refers to a short circuit within the system, unless qualified in another way (i.e. high impedance fault refers to the unintended electrical connection between two points within the system through some non-zero impedance). A short circuit fault is considered a true short circuit. The analysis will usually specify the cable impedance between the two points where the fault is occurring.

In order to have better analysis, a different point of view for faults is suggested. In two-line AC systems, faults are typically divided into three categories: LL, LG and two Line to Ground (LLG). For the purposes of this study new definitions of these faults are developed for DC systems in the following sub-sections.

#### **2.1.1 Line to Line faults**

LL fault is represented in Figure 2-1. This figure shows also that a LL fault can occur from Positive to Negative (PN) or Negative to Positive (NP). This substitution will be more essential, when the DC distribution line includes diodes. Diodes prevent negative current; therefore, PN or NP faults that span positive and negative lines at different parts of the system have the potential of significantly increasing DC voltage stresses in the system. Figure 2-2 depicts faults where PN

faults occur in two separate branches. In these scenarios, the diode would not make any difference and the faults have the same effect as the faults depicted in Figure 2-1.

On the other hand, Figure 2-3 shows scenarios where the diode plays a role and faults in the worst case scenario can double the voltages between negative and positive lines [25]. If the PN fault in Figure 2-3 occurs between two lines on the anode sides of auctioneering diodes in the positive leg, this results in a voltage doubling effect and is hereafter referred to as a Positive Negative Double (PND) fault. PND faults need specific detection and very fast galvanic fault isolation means in order to mitigate potential damage to system components due to over-voltage (unless those components are significantly de-rated, which results in size/weight increases). The current change due to the PND fault likely will not be high enough to be detected as a fault.

A variation on the PND fault may occur in non-isolated systems where the path that the fault current follows includes at least one actively switching power semiconductor and a diode. If the power semiconductor and diode are arranged so that fault current builds up in the path connected to the diode anode when the switch is on and then discharges into the capacitor connected to diode cathode when the switch turns off, the capacitor voltage will build up. This will be referred to as a Positive Negative Charge Pump (PNCP) fault. This scenario is also undetectable until the voltage builds up to a point when the associate power converter shuts down on an over-voltage. At this point the capacitor voltage stops building up, but such scenarios can result in large portions of the system unaffected by the fault shutting down because their associated power converters are fed by the part of the same DC bus that is being pumped up by the PNCP fault.

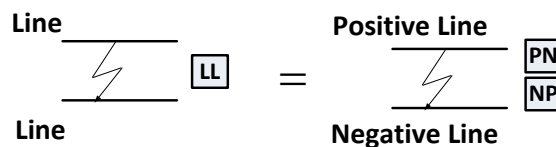


Figure 2-1 LL(PN or NP) faults in DC



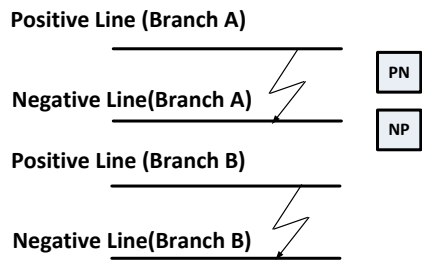


Figure 2-2 Multiple ground faults scenarios two branches without diode

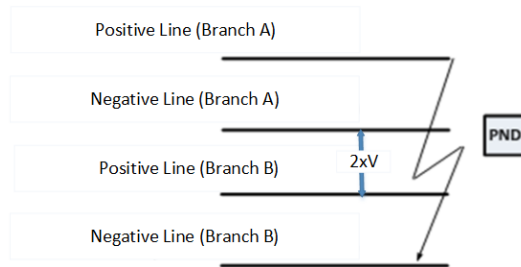


Figure 2-3 Multiple ground fault scenarios: two branches with diode

A similar response to the PNCP fault occurs when either the positive or negative leg has a LG fault and then a second LG fault occurs on an AC line (or vice versa) within the power system if the AC and DC parts of the system are not galvanically isolated from each other. These faults will also cause the affected AC power converter stage to fault off on an internal DC overvoltage, with a loss of power to all of its down-stream loads. This fault will be referred to as a Positive Negative AC (PNAC) fault.

### 2.1.2 Line to ground faults

LG faults are either between the positive line to ground (PG) or the negative line to ground (NG) as shown in Figure 2-4. In non-isolated DC systems, a NG fault will shift the PG voltage by one half of the PN voltage where the fault occurs. Alternatively, a PG fault will shift the NG voltage by one half the PN voltage. PN and NG faults occurring simultaneously, where a diode auctioneering circuitry having cathodes facing inward from the points where the faults occur will result in the PND scenario described by Figure 2-3

### 2.1.3 Line to line with ground fault

Fault characterization studies typically also include LLG faults. What is of particular interest in floating power systems is a sub-set of LLG faults where either two PG or two NG faults exist on either side of a protective device. These fault conditions are referred to as Positive-Positive Ground (PPG) or Negative-Negative Ground (NNG). In these scenarios the double ground fault condition is undetectable and, when a second LL fault or opposite bus NG or PG fault occurs the protective device is short circuited by the prior PPG or NNG fault and is therefore rendered ineffective. In conventional electromechanical circuit breaker implementations applied to LVDC systems, PPG and NNG faults is typically dealt with by adding circuit breaker poles in series in order to avoid the potential of arching, non-clearing faults[26]. This results in higher size/weight, over-designed systems.

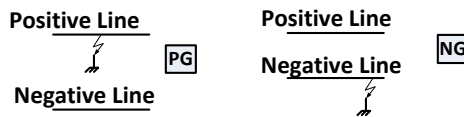


Figure 2-4 LG (PG and NG) faults

## 2.2 Mathematical Expression for short-circuit currents in DC-systems

IEC 61660-1 [8] is the only available standard document for the calculation of short-circuit currents in DC-systems. It has been developed to address the issue of calculating both the peak and steady state short-circuit currents in low voltage DC auxiliary installations in power plants and substations, thus proposing approximated analytical formulas. Nevertheless, the validation of the obtained results has not been done yet, through neither simulation nor testbed. In [30] authors have come up with theoretical approach to calculate DC transient short-circuit currents.

A six-pulse diode rectifier directly fed by a synchronous generator as shown in Figure 2-5 composes the power system configuration considered analysis. This case is typical of a DC distribution system equipping a ship, a car, a diesel-electric train or a truck. These particular applications are characterized by some peculiarities: first, there is no additional electric equipment interposed between generator and rectifier (such as transformers); second, the distance between generator and rectifier are short. Due to these facts, it is possible to consider only the parameters of the synchronous generator ( $r_d$  and  $x_d$ ) when defining the source system parameters. In fact, being the resistance in an electrical machine usually much smaller than the reactance it will be neglected in order to simplify the calculations. Obviously, this will lead to short-circuit currents higher than real ones. It is relevant to notice that the discussion presented hereafter is valid also in case of generator far from the rectifier, or in case of interposed impedances. Indeed, it is possible to include the additional impedances into the generator ones, without impairing the validity of the formulae provided in the following. The other hypotheses applied are the same as before, but in this case, the per-unit system will be used. This in order to simplify the generator parameters identification. It is relevant to notice that the analysis focuses on the first section of the short-circuit transient, which is the one mostly influenced by the generator's internal reactance variation. The dynamic evolution of such a transient is fast (tens of supply AC periods), due to the low longitudinal impedances of onboard power systems. This led to the possibility of ignoring both the prime mover internal dynamic (due to its inertia) and the control system's action (which respond with a higher time constant due to their common settings).

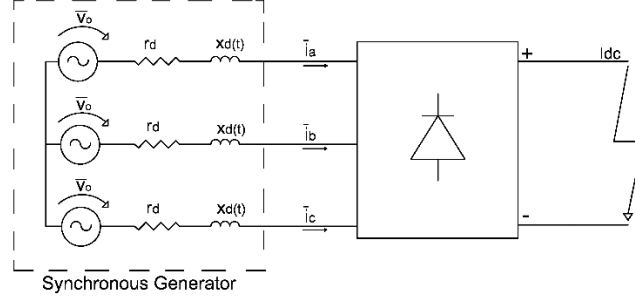


Figure 2-5 DC system fed by synchronous generator

The short-circuit currents transient can be expressed in DQ reference as follows, considering the well-known equations of synchronous generator dynamics [28][29]:

$$i_d = \sqrt{2} v_o \left[ \frac{1}{x_d} + \left( \frac{1}{x_d''} - \frac{1}{x_d'} \right) e^{-\frac{t}{T_d''}} + \left( \frac{1}{x_d'} - \frac{1}{x_d} \right) e^{-\frac{t}{T_d'}} - \left( \frac{1}{x_d''} \right) e^{-\frac{t}{T_{ac}}} \cdot \cos(\omega t) \right] \quad (1)$$

$$i_q = v_o \left( \frac{1}{x_q''} \right) e^{-\frac{t}{T_{ac}}} \cdot \sin(\omega t) \quad (2)$$

$$\bar{I}_{dq} = S_{dq} I_{dc} \quad ; \quad S_{dq} = \frac{2\sqrt{3}}{\pi} \quad (3)$$

where  $v_o$  is the constant internal *emf* rms value, set equal to 1 *p.u.*, and  $T_{ac} = x_d'' / (\omega \cdot r_d)$  is the synchronous generator armature short-circuit time constant. Using equation (3) in equation (1),

$$i_{dc} = \frac{1}{S_{dq}} \sqrt{2} v_o \left[ \frac{1}{x_d} + \left( \frac{1}{x_d''} - \frac{1}{x_d'} \right) e^{-\frac{t}{T_d''}} + \left( \frac{1}{x_d'} - \frac{1}{x_d} \right) e^{-\frac{t}{T_d'}} - \left( \frac{1}{x_d''} \right) e^{-\frac{t}{T_{ac}}} \cdot \cos(\omega t) \right] \quad (4)$$

### 2.3 Experimental validation of Expression for short-circuit currents in DC-systems

With the aim of experimental validation of equations discussed above and in [30], a three-phase, 480V, 75kVA synchronous generator with passive rectifier output has been used. The generator was driven by a variable frequency drive and a NEMA size 8 three-phase circuit breaker was configured as shown in Figure 2-6 in order to apply the three-phase fault to the generator output. The circuit breaker poles were connected in series so that if the circuit breaker were opened inadvertently with the dc short-circuit applied there would be sufficient arc voltage built up to drive short-circuit current to zero without causing damage. A constant DC voltage supply was

applied to the exciter field of the generator for the tests. Before performing the DC short-circuit tests, transient short-circuit tests were performed by applying a three-phase bolted fault to the generator without the diode rectifier in the circuit and parameters were extracted according to the procedures in IEEE Std. 115-2009. The synchronous machine parameters are given in Table 1.

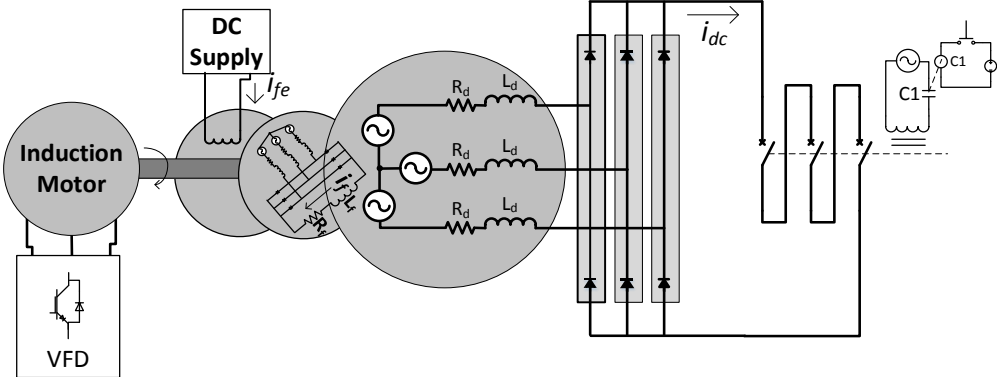


Figure 2-6 Short-circuit test set-up schematic and experimental setup

Table 1 Synchronous generator parameters

Parameter	Symbol	Value
Rated Volt-Amperes	$S_{rated}$	75 kVA
RMS Rated Voltage/Base Voltage	$V_{rated}/V_b$	480 V / 277 V
RMS Rated Current/Base Current	$I_{rated}/I_b$	90.2 A / 90.2 A
Operating frequency of tests	$f$	60 Hz
Base Impedance	$Z_{base}$	3.07 W
Stator resistance	$r_d$	0.026 p.u.
Unsaturated d-axis reactance	$x_{d(unsat)}$	1.656 p.u.
d-axis reactance at 408 Vrms	$x_d$	1.38 p.u.
d-axis transient reactance	$x'_d$	0.18 p.u.
d-axis sub-transient reactance	$x''_d$	0.072 p.u.
q-axis reactance	$x_q$	1.328 p.u.
q-axis sub-transient reactance	$x''_q$	0.072 p.u.
Armature short-circuit time constant	$T_{ac}$	0.00736 s
d-axis transient time constant	$T'_d$	0.088 s
d-axis sub-transient time constant	$T''_d$	0.016
q-axis sub-transient time constant	$T''_q$	0.0002

Figure 2-7 shows the experimental results for the 570V DC short circuit tests. Figure 2-8 shows a comparison between the measured DC short-circuit current transient and the calculated current using (4). The correlation is very good. As the initial voltage is increased, the sudden short-circuit application provides a higher torque load to the induction motor prime mover that causes the rotor speed to slow down. This introduces a variable that is not accounted for in (4). The comparison between the measured results and calculated results of (4) for this condition is shown in Figure 2-8. There is a small discrepancy attributable to the slowing down of frequency. As expected, the unsaturated d-axis reactance is required to achieve accurate results since  $x_d$  in (4) represents the resultant steady state short-circuit current which corresponds to low flux in the machine. Therefore,  $x_{d(unsat)}$  in Table 1 is used to calculate the transient short-circuit current characteristic using (4).

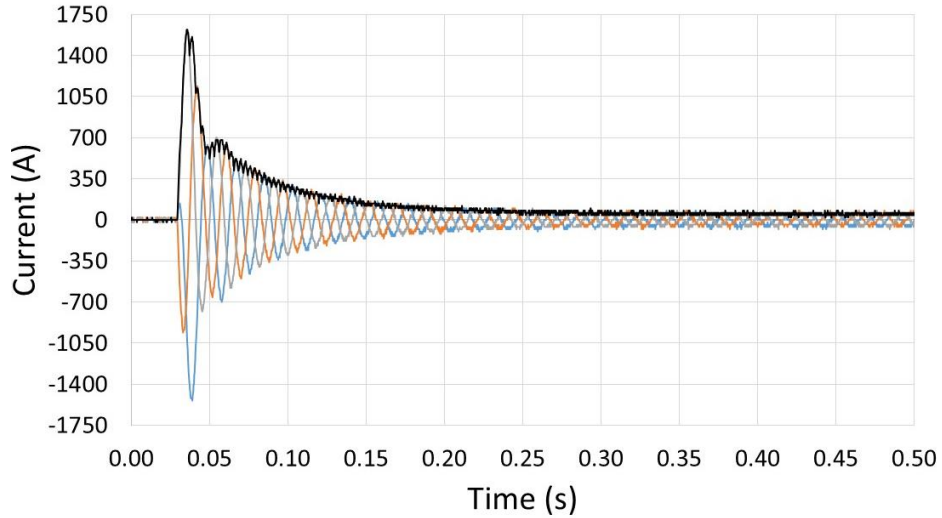


Figure 2-7 Test results with initial RMS dc output voltage of 570V ( $v_0=0.855$  p.u.)

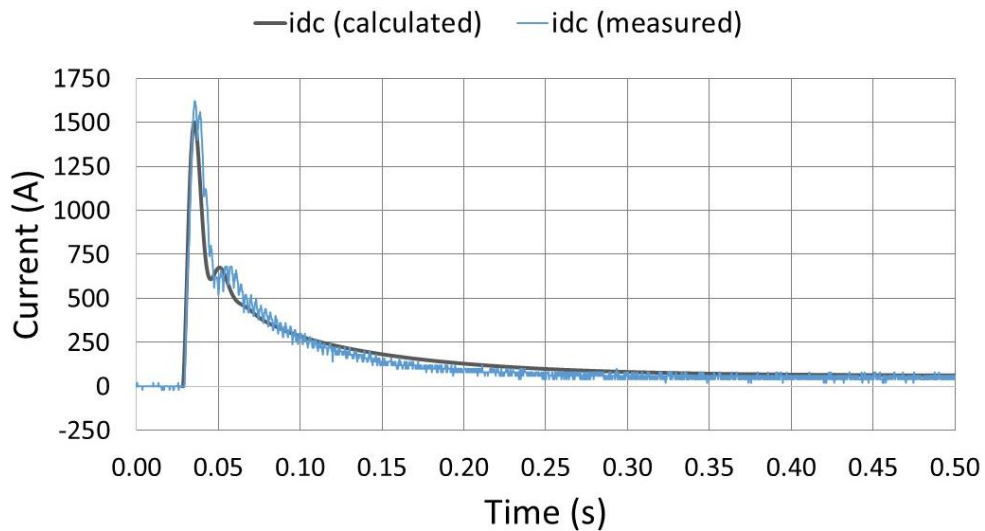


Figure 2-8 Comparison of test results with DC DQ transformation model for the RMS dc output voltage of 570V ( $v_0=0.855$  p.u.)

### Chapter 3 Review of state of the art

This chapter discusses the options for Protective Devices (PD) to be applied to the various MVDC and MVAC/DC architectures. PD is a general term that refers to both electromechanical and solid state devices that are used to separately from power conversion to isolate faults from the system. Solid State Protective Device (SSPD) refers to any component, sub-component or group of sub-components that plays a role in short circuit, low impedance and high impedance fault isolation

which uses solid state power semiconductor(s) to drive the fault current to zero so that the fault can be isolated. For the purpose of this study, SSPD, whose one-line diagram symbol is shown in Figure 3-1, provides both current limiting and air gap isolation capability, in addition to any control and communications capability associated with successful operation of the switch in a given architecture. The SSPD in Figure 3-1 can only block current in one direction. The SSPD in Figure 3-2 can block current in both directions. The air gap isolation will be accomplished with a Galvanic Isolating Switch (GIS). The GIS one-line diagram symbol is shown in Figure 3-3, The GIS is a set of purely electromechanically actuated no load contactors connected in series with the solid state part of the SSPD in both the positive and negative legs. A SSPD that is purely solid state, with no air gap isolation capability is represented in the one line diagrams by the symbol in Figure 3-4. This is generally referred to as the previously described SSCL but its function may be as simple as one or more series and paralleled power semiconductors that are commutated off when a fault occurs or as complex as utilizing Pulse Width Modulation (PWM) to actively limit the current. An additional symbol that is used in the one line diagrams of this study is the conventional AC circuit breaker. This symbol is shown in Figure 3-5. It is generally only applied to the AC parts of the system with exception of LVDC systems because conventional electromechanical AC circuit breakers can be configured so that they operate safely in LVDC systems.



Figure 3-1 Unidirectional SSPD one-line diagram



Figure 3-2 Bi directional SSPD one-line diagram



Figure 3-3 no load GIS one-line diagram





Figure 3-4 Solid state switch one-line diagram



Figure 3-5 Electromechanical circuit breaker one-line diagram

### 3.1 Solid state switch

In current DC systems where most of the part connects together through a common bus, if a fault occurs in any part of the system, the whole system will see the effects of fault inception. Significant power is lost for a large part of the system because of absence of well-coordinated protective devices which could detect and isolate faulted areas in a very fast and intelligent manner. Also, the uncontrolled amount of current flowing through the system can lead to equipment damage. Furthermore, the MVDC distribution will consist of active power electronic sources and leads, each having their own input and output filters. If a LL fault suddenly occurs the capacitors within these converters act as current sources discharging very high currents into the fault. These current surges will rise to very high peaks in a very short period of time. The AC distribution equivalent to this type of behavior is the discharge of surge current from connected induction motors into the fault. However, under the AC protective paradigm, the protective devices act slowly (over 10's of milliseconds), and the aim of the protective system design is to ride through the surges from connected induction motor loads. On the other hand, the new DC protective paradigm must actually coordinate its protective devices on the capacitor discharge current surges. These surges have potentially much higher peaks than the equivalent AC system surges and much shorter time constants. The requirement for SSPD is very fast detection and very fast current interruption. The early interruption of fault current will minimize the maximum fault current magnitude and allowing the current breaking capacity of the high speed circuit breakers to be reduced.

What is needed is a fast acting switch to isolate faults, one that inserts minimum loss into the distribution system, has reliability that would be requisite of a protective device within the context of the rest of the system and one that fits within ship spaces—at least in comparison with conventional AC switchgear but preferably even more power dense in order to make room for the power conversion equipment inherent to MVDC. If a system is designed by defining zones and providing some sort of fast and reliable protection mechanism which at occurrence of fault could immediately detect and isolate the faulty part of the system, power interruptions to non-faulted portions of the system can be minimized. A solid state protective device is a perfect proposal for this situation. SSPDs because of their fast action can limit faults in very short duration of time which may lead to less stresses on components of the system. The advent of SiC power semiconductors, with their inherent low loss and high speed of commutation, potentially addresses the attendant issues of efficiency and space claim.

SSPDs that are bidirectional and that are inserted in series with both the positive and negative legs of the bus add an additional compelling capability to mitigate PND, PNAC and PNCMP faults that occur in floating ground systems with a high power converter insertion level. It is possible that SSPDs, in coordination with other actively controlled power electronic systems, can detect and limit faults in specified zones with uninterrupted operation of other healthy parts of the system.

Survivability of the system in case of fault is a major factor for designing of a SSPD. Auctioneering diodes can also be included in the design of dc system to make it more reliable.

The current is the same upstream and downstream from the fault location. Therefore, conventional approaches to fault protection and coordination—which rely on voltage droop to ensure that protective devices closest to the fault trip off first—will not work. Because the solid state protective device(SSPD) limits the fault current to safe levels, which allows isolation in a time response on

the order of tens of microseconds (as opposed to several hundred milliseconds if the PCR limits the fault current).

### **3.2 Research status of available SSPD topologies**

A study was performed to identify the options for SSPD topologies that are currently in the literature. The SSPD topologies identified fall into one of four categories: (1) Current Interrupting; (2) Current Limiting, (3) Dissipating, or (4) Resonant. The main difference between an SSPD that falls into one of these categories is how it handles the stored inductive stored energy that inevitably exists in the system when the fault is being interrupted which, if not handled correctly, will destroy the power semiconductors within the SSPD by causing high  $L \cdot di/dt$  voltage stresses in excess of the device rating. A Current Interrupting SSPD will simply act as a switch to stop the flow of current into the fault and will rely upon a combination of significant device voltage de-rating, external snubber and surge arrester or Metal-Oxide Varistor (MOV) to handle the voltage stress. The design of Current Interrupting SSPD and external circuitry requires careful consideration of the switch turn-off commutation characteristic and addition of  $di/dt$  limiting inductance. A Current Limiting SSPD will actively current limit the fault current using PWM to predefined level (usually zero current) and requires a combination of additional diodes to provide a freewheeling path for inductive energy and capacitive voltage clamping to provide a relatively stiff voltage against which the power semiconductors can switch. A Dissipating SSPD utilizes additional active devices to divert energy into dissipative components. The Dissipating SSPD requires a pre-charged capacitor in parallel with the commutating devices and sufficient resistance to dissipate the energy under all potential scenarios. A Dissipating SSPD can be implemented without external inductance. Resonant SSPDs utilize resonant LC circuitry to force a zero crossing condition in the current directed into the fault, which can then accommodate either zero current turn-off of active switches

or turn-off of a load commutated switch, such as a Thyristor or SCR. Promising SSPD solutions representing all of the above categories are described in the following sub-sections. The following topologies are investigated:

- Solid state interrupter (Current Interrupting)
- Solid state limiter (Current Limiting)
- Dissipative AC/DC Switch (Dissipating)
- Z Source breaker (Resonant)
- Hybrid solid state/electromechanical circuit breaker (Current Interrupting)
- Hybrid HVDC circuit breaker (Current Interrupting)

In order to reliably mitigate fault behaviors in the system the “ideal” SSPD would embody three levels of protection:

- 1) Active current limit
- 2) Active current interruption at the switch level with minimal delay
- 3) Ability to fail to an open condition, for some reason, the power semiconductor itself fails

Levels (1) and (2) of protection can be accomplished with Current Limiting topologies. Only level (1) is accomplished with Current Interrupting topologies. A Current Interrupting topology could obtain some degree of Level (2) protection by pulsing energy into its external snubber and MOV. The Current Limiting topology will likely have an advantage in implementing protective coordination because cascaded topologies can actively limit the initial fault inrush event to different set points. Dissipating topologies accomplish (1) and (2) and, with can potentially accomplish level (3) of protection. More work is needed to demonstrate/verify this capability. Resonant topologies only accomplish Level (1) of protection.

### 3.2.1 Solid State Interrupter

The basic structure for a Solid State Interrupter is shown in Figure 3-7. The main active power circuit components to the Solid State Interrupter are first an actively controlled power semiconductor switch in each leg of the system that requires protection, second current limiting inductor and third snubber circuitry to dissipate the inductive stored energy between the source and the fault. If the system had a common reference (i.e. the negative leg was grounded) then only the top switch would be required and the SSPD would only be required to mitigate LL faults. However, in a floating system, switches are required in both the positive and negative legs in order to mitigate the possibility of two LG faults, or PND fault, as would occur at the LG fault positions in Figure 3-7. The single differential mode current sensor and common mode current sensor would probably be the best implementation for detecting the different types of faults. An alternative would be to sense current independently in the positive and negative currents but usually, in multiple LG fault scenarios, it is better to look for a small difference between the currents in the positive and negative legs in order to stop the fault before voltage stress builds up in a capacitor somewhere in the system. It will be more accurate to use a common mode sensor for this purpose because the overall continuous current rating of the differential mode sensors is high and the current that must be detected in, say, a PND fault, is at a level that is within the sensor error of the device. Energy into the fault during switch commutation is handled by the inductor (for the reasons explained in the introductory section), an RCD snubber across each active device to divert energy away from the device and keep device voltage within a safe region during off commutation and varistor to dissipate remaining inductive stored energy in the system while protecting the power semiconductor from over-voltage. The electromechanical contactors shown in Figure 3-7 are

opened only after it has been verified that the current through the inductor(s) in the associated faulted leg(s) is at zero.

This topology is based on series and parallel combination of IGBT switches to increase the current and voltage rating of the breaker. We can use an array of switches with careful synchronization of gate signals and snubbing of stray energy. Series and parallel combination of the switches can be used to meet the voltage and current requirements of the interrupter respectively[9].

Diversified Technologies Inc. (DTI) has introduced an 8MW IGBT-based solid state interrupter [9] as a potentially suitable SSPD for shipboard applications. This topology is based on series and parallel combination of IGBT switches to scale the SSPD to the voltage and current requirements of the system. An array of series/parallel IGBT are commutated off through careful synchronization of gate signals and snubbing of stray energy. The required voltage and current requirements for the SSPD can be met through the appropriate series and parallel combination of the IGBTs.

In the design described in[9], a unidirectional SSPD implementation is implemented with 6 series IGBT switches, each of 4.5kV rating, which would be sufficient for a 10kVdc system. An important characteristic of this type of SSPD implementation is the combination of a large inductor in series with the SSPD active devices to limit the di/dt voltages that will occur across the device during turn-off and slowing down the rate of device turn-off through with gate drive resistors in order to manage the inductive stored energy in the system. Even with these measures, it is still necessary to significantly de-rate the device voltage withstand capability. A suggested implementation of this topology, for a 20kVdc system, would utilize 4 of the 10kVdc SiC IGBTs of [27] in series in a bi-directional implementation, shown in Figure 3-9. Note also that the bi-directional SSPD is included in both the positive and negative legs. If bi-directional capability is

not required (this depends upon the placement of the SSPD in the system and the MVDC architecture as will be shown later) then the unidirectional implementation shown in Figure 3-7 is sufficient, which requires only half of the devices. As stated earlier, the symmetry of current interruption capability in the positive and negative legs is necessary due to the ungrounded nature of the MVDC bus. This also gives the SSPD the capability of independently interrupting current in the positive and negative legs and thus addresses the issues associated with PND, PNAC and PNCP faults. The implementations of Figure 3-9 and Figure 3-10 should have sufficient voltage de-rating to address  $di/dt$  voltage stresses when the devices commutate off during a fault (4:1 voltage margin).

One main challenge for any SSPD is in achieving sufficient continuous current carrying and current surge capacity. Given the current rating of present SiC devices, the multiple modules must be paralleled, each with associated snubber circuitry to mitigate the effects of interconnecting inductances. Also it should be ensured that all the gate drives perform in synchronized manner for opening of breaker in fault condition. The implementation seems impractical to parallel due to proliferation of hardware associated with each paralleled module. The complexity of such an implementation demonstrates the need for development of higher current SiC modules.

Proposed controller provides the gate drive signal for the switches in the interrupter which synchronously open and close. The fast inverse time controller receives commands from either a manual input, from other breakers in the network, or from fast sensors that detect local fault currents. The inverse-time controller provides inverse trip time control for over current states, and a fast instantaneous trip if the over current limit is reached. Basic control scheme of the interrupter is shown in Figure 3-6.

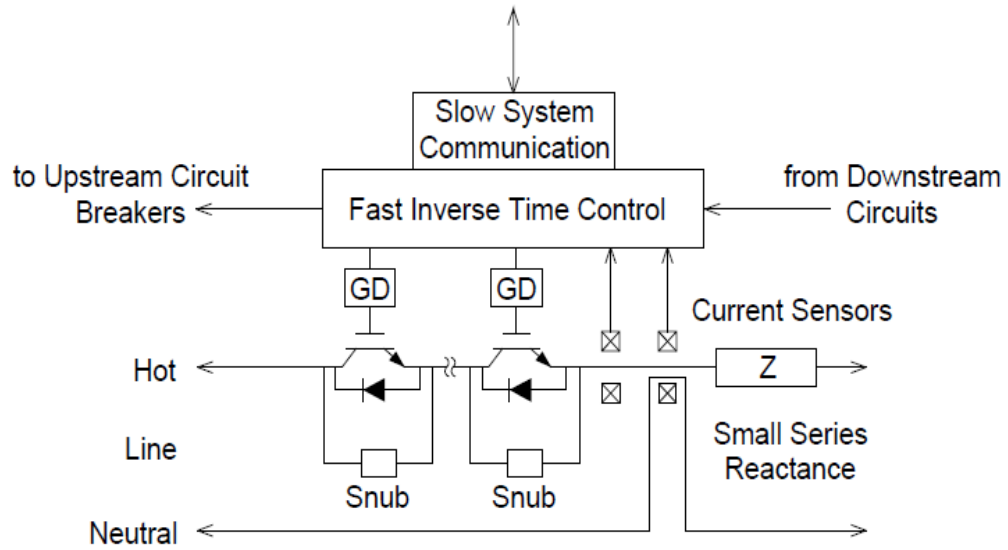


Figure 3-6 Control scheme for the proposed interrupter

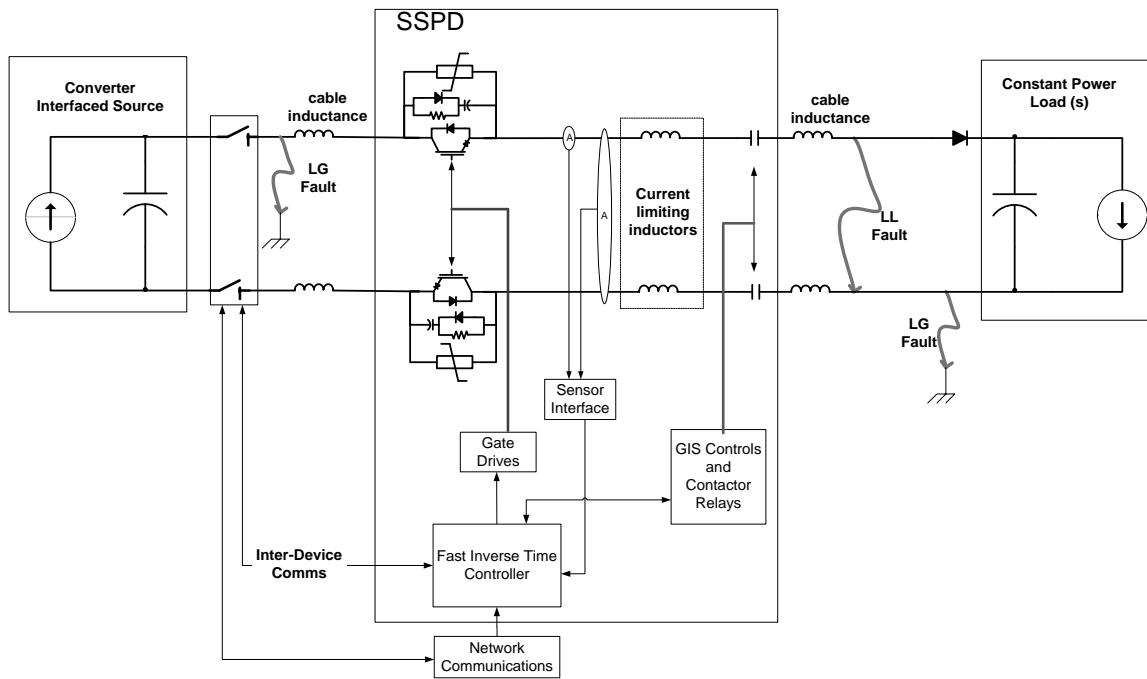


Figure 3-7 Basic unidirectional Solid State Interrupter implementation for notional floating system showing fault scenarios



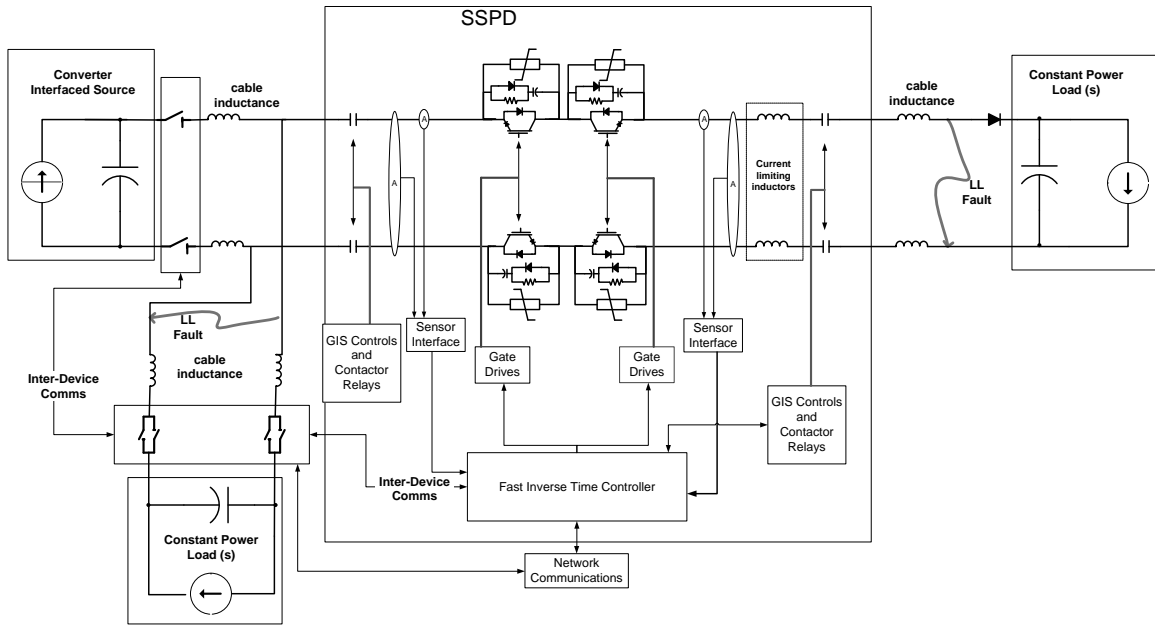


Figure 3-8 Basic bi-directional Solid State Interrupter implementation for notional floating system showing fault scenarios

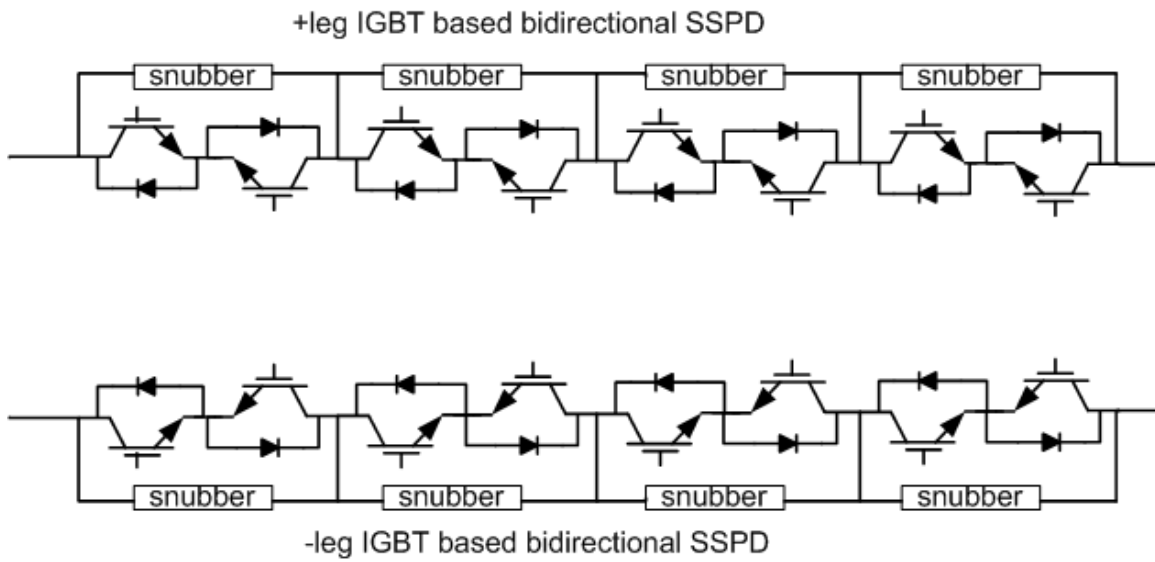


Figure 3-9 IGBT based Bidirectional SSPD for 20kv system

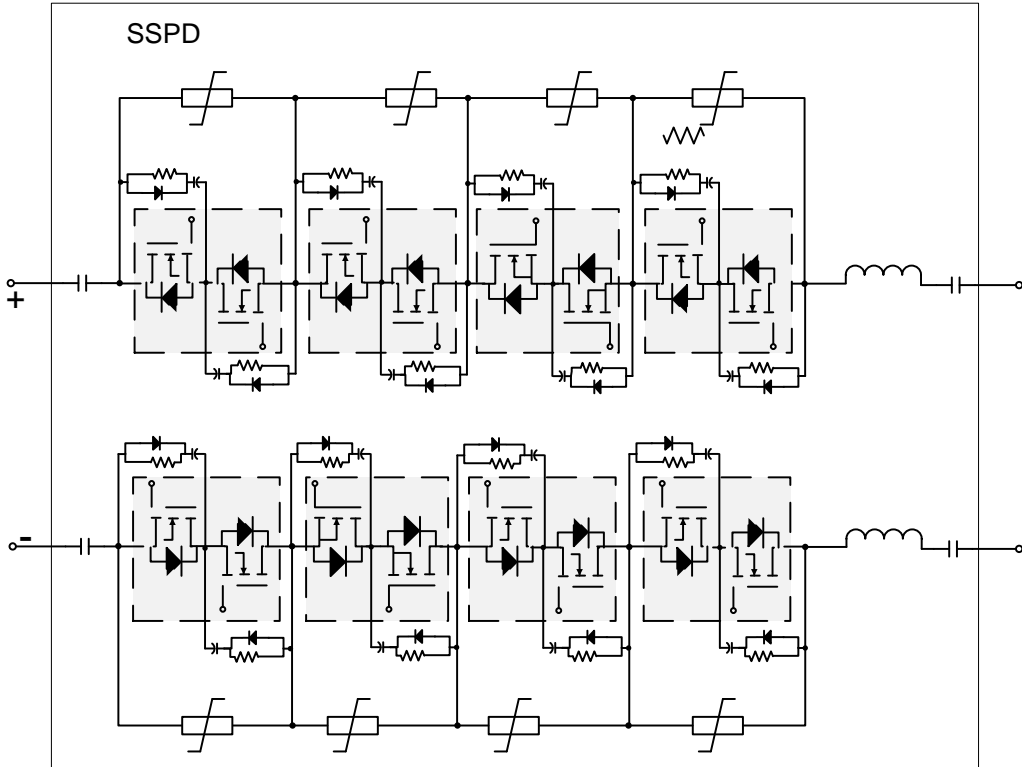


Figure 3-10 20kVdc SiC MOSFET based bidirectional SSPD implementation

### 3.2.2 Solid State Fault Isolation Device (SSFID) [10]

An alternative approach to a Solid State Interrupter is the Solid State Current Limiter shown in Figure 3-12. This topology has been proposed by various researchers for solid state protection and the topology of Figure 3-12 most closely matches that of [10]. The main active power circuit components to the Solid State Current Limiter are first an actively controlled power semiconductor switch in each leg of the system that requires protection, second current limiting inductor, third a freewheeling diode to provide a path for stored inductive energy when the power semiconductors are turned off, fourth a line to line RCD voltage clamp to provide “stiff” voltage to work against and fourth snubber circuitry to dissipate the inductive stored energy in the circuit interconnects. Again, if the system had a common reference (i.e. the negative leg was grounded) then only the top active switch would be required and the SSPD would only be required to mitigate LL faults and in the floating system, switches are required in both the positive and negative legs.

In [10] authors have proposed a prototype as shown in Figure 3-11 for 400V dc SSCB. It serves as basic design scheme of fast fault interruption and extended concept for 6.5kV silicon (Si) and 10kV silicon carbide (SiC) devices as solid state fault isolation devices (SSFID)

The main advantages can be listed as

- Low cost /size
- Simpler power circuit construction.
- Flexibility due to easy reprogramming capabilities.
- Fast interruption into tens of microseconds

The Solid State Current Limiter acts as in the same way as a simple DC-DC buck converter. When the fault occurs, active power semiconductors are operated in a PWM fashion to regulate the current in the inductor to zero or to some other pre-set limit. When the power semiconductor(s) are off, the downstream fault current freewheels through the freewheeling diode. The upstream RCD voltage clamp has its capacitor charged up to the bus voltage before the fault occurs. RCD diode blocks the flow of capacitor current into the fault. In this way, the Solid State Current Limiter works against a stiff voltage source. The advantages of the Solid State Current Limiter over the Solid State Current Interrupter are that current surges in the system can be completely controlled, the fault current limit is instantaneously controllable (within the timing latencies of the control circuit) and the snubbers and varistors only handle the interconnecting parasitic inductances between the RCD voltage clamp, the power semiconductors and the diode. Energy into the fault during switch commutation is handled in a controlled fashion through the freewheeling path and does not need to be absorbed by the power semiconductor(s) and associated snubbers and varistors.

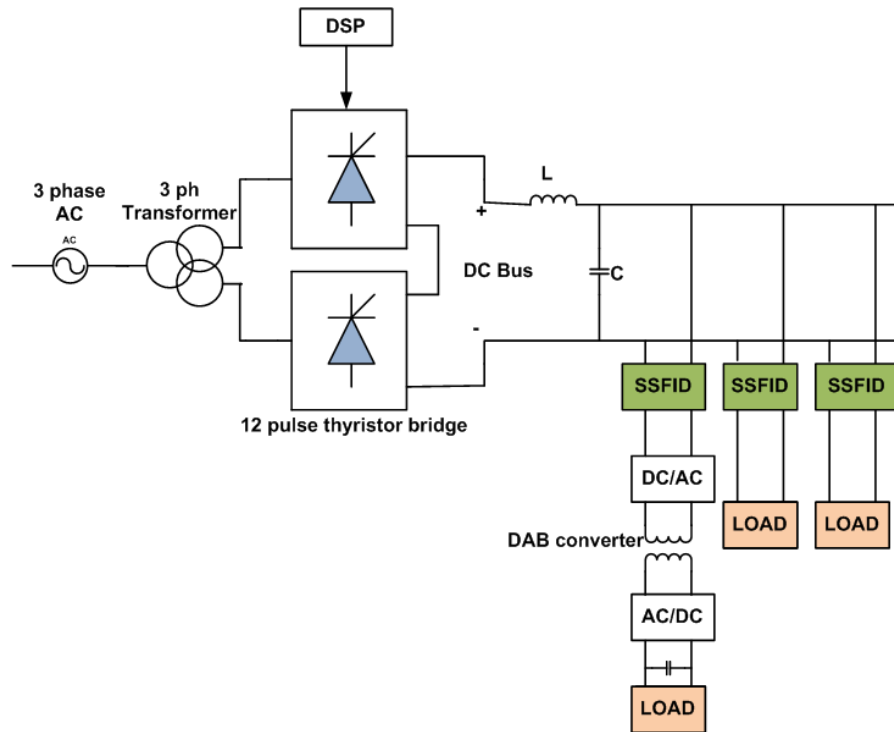


Figure 3-11 Typical scheme for application of SSFID

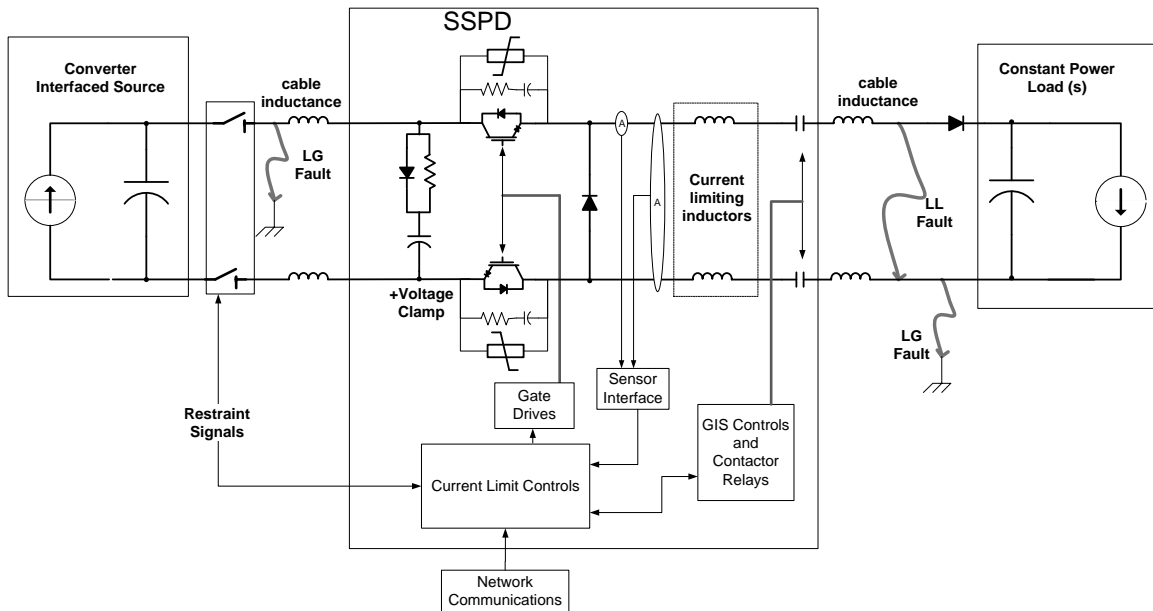


Figure 3-12 Basic unidirectional Solid State Limiter implementation for floating system

Inductor is proposed to limit  $di/dt$  of fault current and additional freewheeling path is provided at the time of interruption to limit the voltage stress on the semiconductor switch.

There is a tradeoff between the switch current rating and amount of inductance required to be put in power circuitry to limit  $di/dt$  of fault current. If a switch can interrupt fault current extremely fast, the fault current is not able to rise as high as it would otherwise. As a result, a faster switch allows to reduce size of external inductor. Any parasitic inductance in power circuit would only help to reduce  $di/dt$  of fault current

### **3.2.3 Z Source breaker**

In absence of zero crossing SCRs cannot be used directly in dc bus protection. So a design is proposed for application of SCRs in DC protection. As SCRs have lesser on state conduction losses it can be better option for SSPD. An SCR device cannot turn off unless the current in the device is at zero. Recognizing this limitation, Corzine invented the Z-Source Circuit Breaker, shown in Figure 3-13, which enables the use of SCR type devices in an SSPD [11][12]. Referring to Figure 3-13, the Z-Source Circuit Breaker utilizes an additional LC resonant interaction to naturally force SCR current to zero in response to application of a LL fault. If a LL fault is suddenly applied to the system, the fault current follows the paths shown through capacitors C into the fault and back through the supplying SCR. The inductor maintains the current value hence fault current through capacitor goes back to SCR and source. At a particular point of time capacitor current equalize the SCR current and net current going through SCR becomes zero, at this time gate can be removed from the SCR and therefore inhibit current from the upstream converter into the fault.

The z-source breaker as shown in Figure 3-13 has the advantage of automatically switching off in response to a local fault and without the need for fault detection. Furthermore, the z-source breaker isolates the generation source from the fault current.

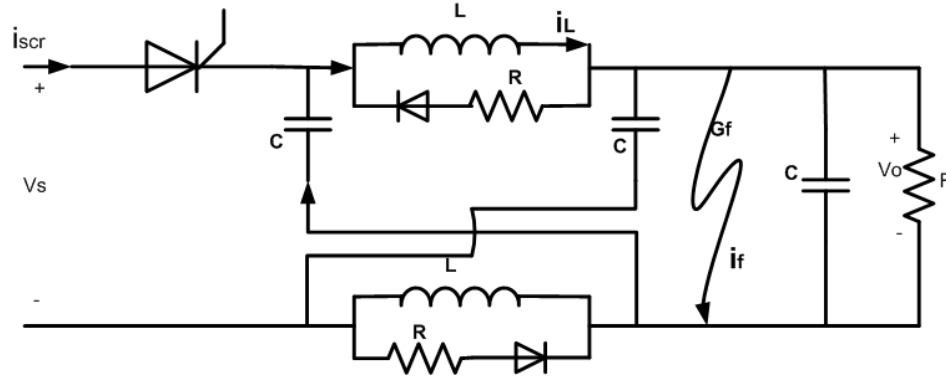


Figure 3-13 Z source breaker

This feature is adopted for fault handling in dc power systems. When the fault occurs in this system, there is no direct short of the z-source capacitor voltages, because of the inductors in the z-source circuit. The breaker components act together to quickly mitigate faults in a dc system. A portion of the fault current will come from the z-source breaker capacitances. In the transient state, the inductor keeps the current constant; the conduction path is then through the Z source capacitors and back to the source. At particular time cap current will match with inductor current making SCR current zero, at this time SCR will commutate off and gate voltage can be removed.

In this design we need to analyze the sizing of inductors and capacitors used. Proposed system specifications of the breaker are 6MW, 6kV with a  $20\text{m}\Omega$  fault ramped at a rate of  $K=5 \times 10^4 / \Omega\text{s}$ .  $C=125\mu\text{F}$  and  $L=200\mu\text{H}$  for the commutation time of  $100\mu\text{s}$ . The inductor current circulates in the diode and decays to zero in about 5ms (with a 100 resistor). Because of this large ratio of peak to nominal inductor current, an air-core inductor is recommended. Physically, the inductor would be a cylinder of 30cm diameter and approximately 30cm in length. For the capacitance, based on series combination of off-the shelf capacitors, a capacitance of  $125\mu\text{F}$  at 6kV with a peak current of 4.5kA is estimated to have dimensions of 21cm by 42cm by 19cm.

The Z-Source topology as shown in Figure 3-13 has several limitations. These include the following:

1. Fault mitigation requires sudden application of a LL short circuit fault or slow LL fault current inception only if the resultant current is 11 times the normal condition[13].
2. The Z-source circuit breaker cannot be commutated off at will, so, as a result, this topology is impractical for application to ring bus architectures
3. If radial bus architectures utilize the Z-source circuit breaker for coordination between upstream and downstream breakers, the LRC components will have to be different between them in order to achieve coordination
4. The topology can only handle LL faults and not the PND, PNAC and PNCP faults of the floating electrical system
5. The capacitance required is quite large, which will be an issue in 20kV systems. For example, for a 6MW, 6kV rated switch  $C=125\mu\text{F}$  and  $L=200\mu\text{H}$ .

### **3.2.4 SGTO based Implementation [14][15]**

Sic devices can be another area for selection of SSPD, due to increase in availability of high rating Sic devices, many topologies can be proposed based on different available Sic devices. Based on Sic mosfet SSFID has already been discussed in this thesis. Another topology is proposed in [14] based on combination of SGTO and Sic diode.

The higher band-gap leads to negligible junction leakage current at temperatures up to 600 °C, which allows for high temperature operation, which simplifies cooling system requirements. The higher electric field breakdown also yields higher voltage rated devices, which reduces the number of series connected devices in voltage blocking stacks. The higher breakdown electric field allows for the design of thinner and faster devices, which translates to 100 times improvement in the switching speed.

One of the limitations of SiC devices is that the chip sizes are small when compared to Silicon devices. This is due to the low wafer yield that is currently achievable. This small chip size is compensated for by the fact that the devices can operate at much higher temperatures—which is a reasonable strategy for power conversion—however this approach may not be advantageous for SSPDs. The main requirement for SSPDs is reliability, which would be enhanced with larger size chips or chips with higher current handling capability. Bipolar Junction Transistor (BJT) Alternatives to the unipolar MOSFET structure, such as SiC IGBT, SiC Emitter Turn-Off (SiC ETO), SiC GTO and SiC Super GTO (SGTO), can achieve higher current ratings at the cost of higher switching loss [16]. Since switching speed is not as significant of a requirement for SSPD than it is for power conversion, perhaps these alternative devices are a better alternative. Given the advantages of increased  $i_{2t}$  capability and larger chip volume associated with thyristor type devices, the SiC GTO and SGTO merit serious consideration. The fact that GTO and SGTO with series PiN Diode series combinations are being researched for medium voltage pulsed applications [17], AC SSCL [14][15] gives good reason to consider these devices applied to SSPD. The requirements for pulsed applications will be very similar to those for SSPDs. The SiC SGTO/PiN Diode based SSPDs may very well be a preferable choice for SSPD when compared to SiC MOSFET/JBS Diode for the following reasons:

- Lower voltage drop than SiC IGBT solutions
- Fully controllable 9kV SiC SGTOs with 2kA pulsed current have been tested [17]
- SGTO devices have larger surface area than SiC MOSFET and IGBT chips and, therefore, better inherent short circuit surge current capability
- High peak current (>12.8kA) measured with SGTO [17]



- SGTOs are unidirectional devices that can only block in the forward direction, so an appropriately rated Sic PiN diode is placed in series to block the reverse direction. The SGTO blocks the forward voltage during fault conditions, while the PiN Diode blocks the reverse voltage.

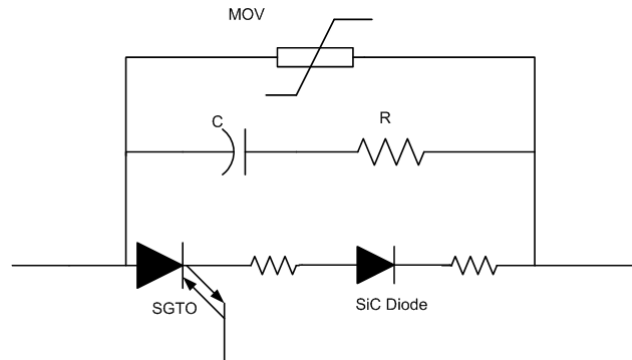


Figure 3-14 Basic SGTO based unidirectional current limiter

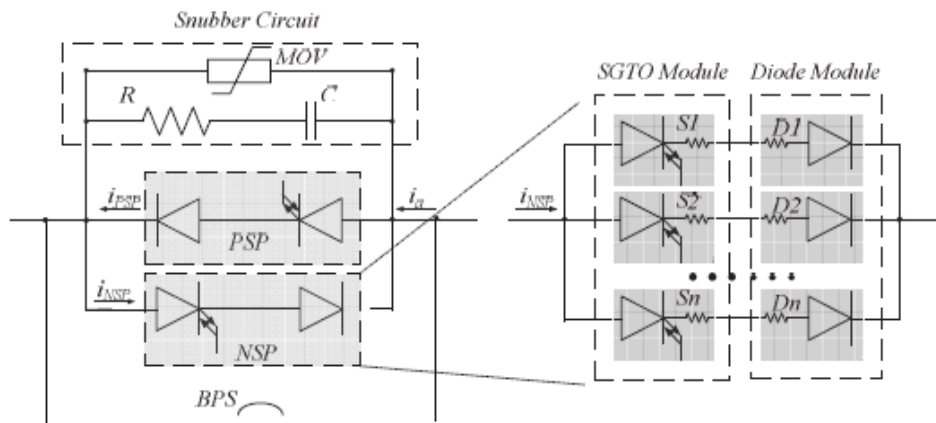


Figure 3-15 Basic design for solid state fault current limiter[14][15]

Figure 3-14 and Figure 3-15 shows the basic design of the limiter topology. Unlike other Sic devices, These Sic devices has negative temperature coefficient which can create problem in paralleling the devices. Because the current sharing by each device should be similar, so to maintain sharing equality a series resistor with positive temp coefficient is added.

SGTOs were selected since they are the highest voltage rated fully controllable SiC device available rated at 8 kV 50A.SGTOs have better short circuit capability than IGBT or MOSFET.

SGTOs are unidirectional devices that only block in the forward direction, so appropriately rated

Sic Pin diodes are placed in series to block the reverse direction. The SGTO blocks the forward voltage during fault conditions, while the diode blocks the reverse voltage. The MOV is employed to capture the initial sub-transient high voltage spike, while the snubber clamps the transient portion of the spike. A study was conducted that shows employing both types of protection dramatically increases the life time of the components. The value of the snubber capacitor was chosen to be 1  $\mu$ F and the snubber resistor is 30  $\Omega$ . One of the most challenging aspects of the SSFCL power module design is device paralleling and current sharing as current capability of the manufactured single SGTO die is around 50 A only. 8KV SIC SGTO, 10KV SIG PIN Diode current carrying capacity of 50A, JN Temp of 70°C at normal operating condition. Turn on delay is 200  $\mu$ S and turn off delay is 7. 68 $\mu$ S. Parallel combinations can be made to increase the current rating up to 1000Amps

### **3.2.5 Hybrid DC Circuit breaker for HVDC transmission**

HVDC transmission for long distance power transfer has become widely popular for large capacity power systems. Remote renewable power generation such as offshore wind or solar power can easily be integrated through HVDC technologies. Voltage source converters and Modular multilevel converters have been put to practical use for hvdc transmission but they have a drawback of losing control capability in case of short circuit faults in dc side circuits. Solid state circuit breakers could be a prominent option to interrupt the fault current without activating AC side breakers or forcing converters to bear fault current until AC side breakers opens.

The most advanced state of the art in SSPD is ABB's hybrid HVDC circuit breaker [18], which is currently being implemented in HVDC systems in Europe and is fast becoming a viable utility systems product [19]. The highest rating system to which the system has been applied is 320kV, 2kA and has the demonstrated capability of interrupting up to 9kA. A circuit schematic

implementation is shown in Figure 3-16 and a physical implementation of a modular 80kV cell is shown in Figure 3-17. Referring to Figure 3-16, ABB’s hybrid HVDC circuit breaker bypasses “Main DC Breaker” with a lower resistance series combination of mechanical switch (“Fast Disconnecter”) and power semiconductor (“Auxiliary DC Breaker” or Load Commutating Switch (LCS)). When a fault is detected the “Fast Disconnecter” begins to open and, as a result, the fault current follows the lower resistance path into the “Main DC Breaker. Once the “Main DC Breaker” is fully commutated of the remaining current due to stored energy in circuit inductance to the fault is diverted into the surge arrester or MOV. Current continues to flow until the energy is dissipated in the MOV until it is driven to zero.

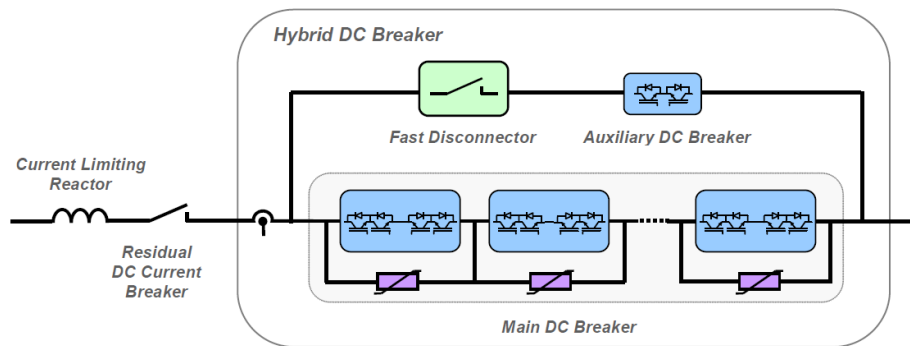


Figure 3-16 Circuit schematic for ABB’s hybrid HVDC circuit breaker[18]

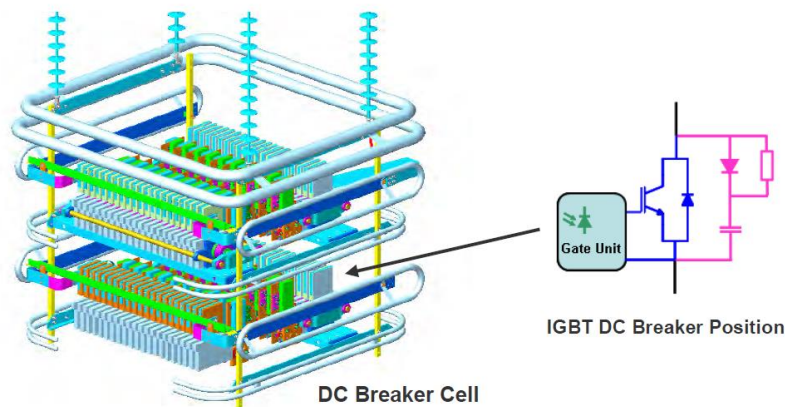


Figure 3-17 80kV hybrid HVDC circuit breaker cell implementation[18]

The power semiconductor device used for the SSPD is an IGBT in a Press-Pack module package. This packaging approach puts the IGBT Silicon into a compressible package similar to a “hockey-puck” thyristor and provides a much higher  $i_2t$  capability than the typical bond-wire connection of Silicon chips in a heat sink mountable module package—and is thus better suited for a protective device implementation. The hybrid HVDC circuit breaker can interrupt fault current in less than 5mseconds (followed by the longer opening time of the associated GIS). The significance of ABB’s achievement is the indication that SSPD at voltages even well in excess of the 20kV distribution voltage requirement can be a reality. However, the hybrid HVDC circuit breaker implementation will not meet the space constraints. Although ABB has not published the size of their hybrid HVDC circuit breaker module, in order to develop a viable SSPD for space constraints design like shipboard MVDC, the focus should be on the development of high voltage, low loss power semiconductors, i.e. >10kV SiC-based modules, and advanced packaging to achieve the desired power density and reliability.

### **3.2.6 Hybrid DC Circuit breaker topology [20]**

Before considering potential new developments in the area of SSPD, this study must consider the alternatives to a fully solid state solution to SSPD. Many topologies can be proposed for operation of solid state switches in combination with mechanical switch. Mechanical switch can be seen as a medium of galvanic isolation but in this case it has been used to reduce the on state losses. The conventional approach is to utilize a hybrid solid state/electromechanical circuit breaker where the SSPD handles commutation during the fault but during normal connected operation it is bypassed by a much lower loss electromechanical circuit breaker or no load contactor. The SSPD also mitigates the possibility of restriking across the mechanical breaker during the commutation process.

In order to better exploit the high turn-off current device capability, a hybrid DC circuit breaker is proposed. As presented in Figure 3-18, this circuit breaker is composed of a mechanical By-Pass Switch (BPS) paralleled to an IGCT static breaker.

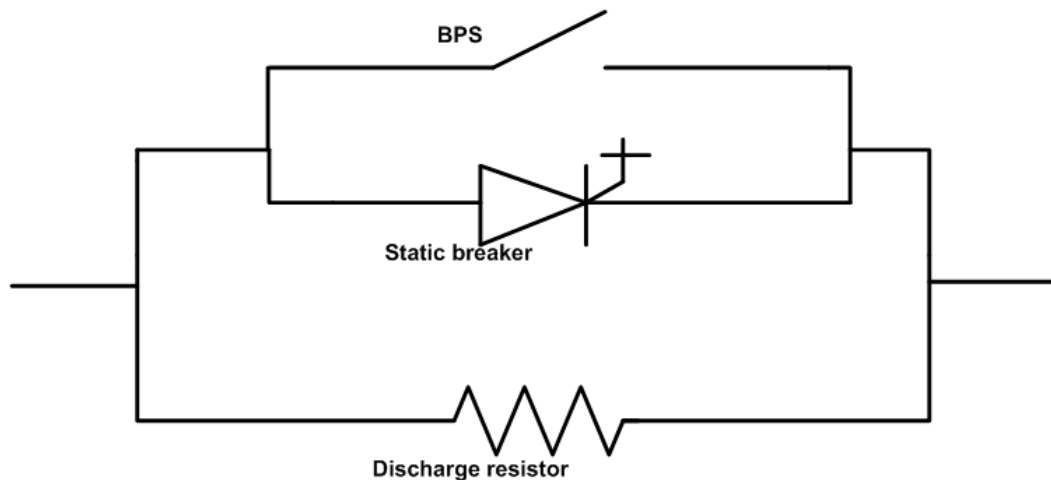


Figure 3-18 Typical hybrid DC breaker

In normal conditions the current flows through the BPS that generally has negligible resistance and capability to sustain high. At the BPS opening command time, after a delay due to mechanical switch inertia, an arc is formed across the BPS terminals, whose voltage allows current commutation into the static breaker. During commutation, the BPS is not subject to reapplied voltage that only appears when the IGCT is opened. This happens when the current commutation is over and the BPS is fully open, so that it is possible to interrupt the current in the static breaker without the risk of re-strike of the mechanical switch.

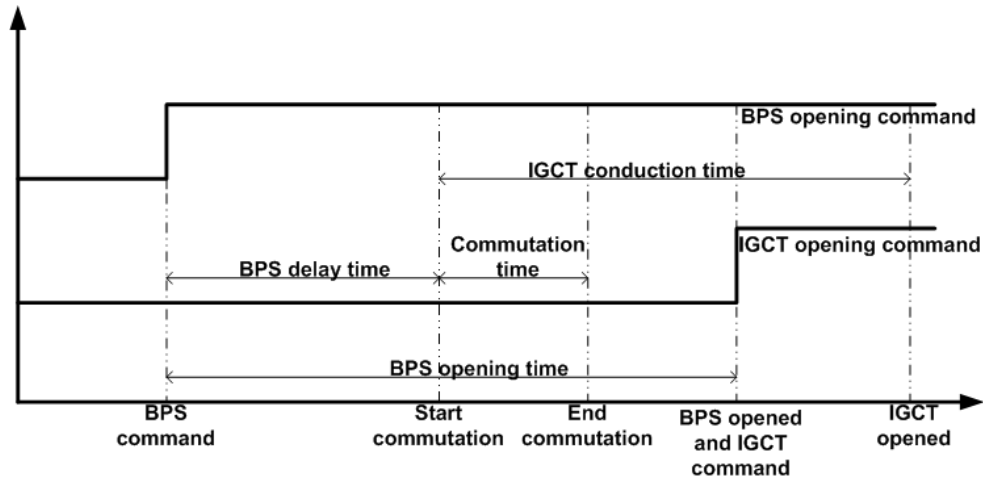


Figure 3-19 Scheme for BPS and IGCT opening command

As shown in Figure 3-19 we can see that the IGCT opening time is generally very short, of the order of few microseconds, while the BPS opening time, evaluated from the opening command time to the actual reaching of open position, depends on the switching technology and on the rated voltage and current values and can range from tens to hundreds of milliseconds. The IGCT carries current only for a limited time period, which depends on the BPS opening time and on the current commutation duration. The circuit involved in the current commutation between the BPS and the IGCTs has low impedance in order to limit the arcing time in BPS and the associated contact erosion. In this case the model can be simplified supposing that the current commutation happens with a current step. The dynamic behavior of the junction temperature can be studied considering the IGCT thermal impedance in transient conditions.

## **Chapter 4 Assessment and modelling of switching topologies for application in MVDC circuit breaker**

### **Classification of SSPDs based on fault mitigation techniques**

In this section three types of SSPD topologies are evaluated: (1) Interrupting; (2) Limiting and (3) Dissipating. The main difference between these topologies is how the SSPD handles the stored

inductive energy that inevitably exists in the system when the fault is being interrupted which, if not handled correctly, will destroy the power semiconductors.

#### **4.1 Interrupting topology**

A unidirectional Interrupting SSPD suitable for a floating system is shown in Figure 4-1 [19]. Assuming the use of 10kV device rated SiC MOSFET [8] in both PGM and SSPD, a PGM feeding a feeding a 30MW load on the 20kVDC bus through the Interrupting SSPD was simulated and a fault was applied to a branch off of the main bus. Results are shown in Figure 4-4. It was determined that four series devices are required per leg in order to keep peak stress per device below 8kV. The simulation shows that the main bus voltage is barely perturbed when the faulted branch is isolated. When the switch is opened, device current is diverted into the parallel RC snubber. The resistance is there to damp any ringing with circuit inductance that exists and a limiting inductor must be part of the assembly in order to ensure that response is critically damped in the presence of variable cable inductance between the PGM and the fault. A snubber capacitance of 100 $\mu$ F per device and a limiting inductance of 500 $\mu$ H is required, assuming worst case cable inductance is 40 $\mu$ H.

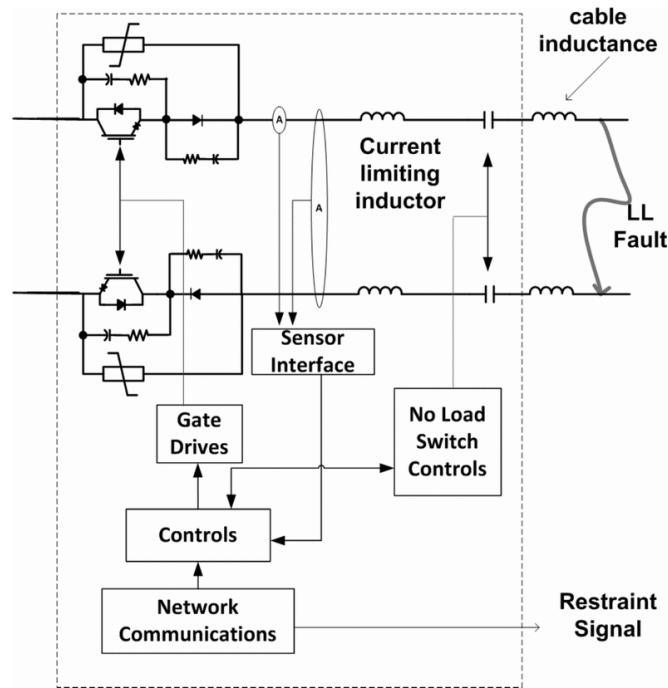


Figure 4-1 Interrupting SSPD

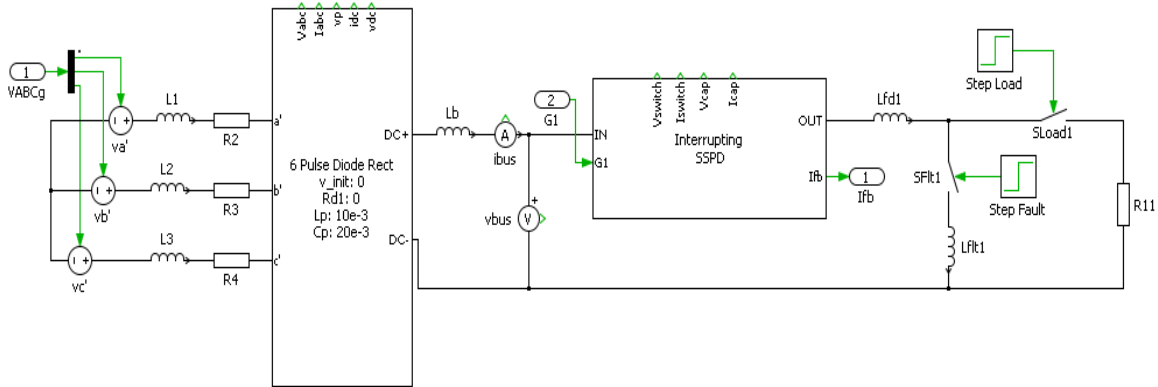


Figure 4-2 Simulation model for Interrupting topology

Figure 4-2 shows the PLECS model for simulating Interrupting topology, a dc voltage bus is being fed by 6 pulse diode rectifier. Cable inductance is shown as  $L_b$  on both the sides of the sspd. Step function is used to connect load and generate fault, Switch  $S_{load}$  is used to connect load and  $S_{fault}$  is used to generate fault.  $L_{flt}$  inductance is used to simulate fault inductance in the circuit. Bus current is measured using ammeters which in fact is giving a fault current signal to controls.AC



side Line inductances and resistances are shown as L1, L2, L3 and R1, R2, R3 respectively.  $V_{abc}$  shows the constant AC voltage supplied to the rectifier. Figure 4-3 shows the 4KV interrupter with MOV simulation schematics,  $L_p$  is the inductance needed to limit the current within specified limit for the duration of control to act and trigger the gate drive signal in case of fault is sensed. Minimum inductance is needed so save the switching devices from high current surges till the control sense and sends a gate drive turn off signal and gate drive turn off process happen.  $5\mu s$  of the delay is used to compensate for the actual practical delays in the circuit and hence  $10\mu H$  of inductance is used to limit the current surges during this delay.  $I_{fb}$  is the bus current feedback sent to control systems which compare this current with certain fixed limit and triggers the gate drive turn off operation once the bus current passed the given fault current level. In this simulation we have assumed two 4 KV 500A SiC mosfet device to be used in parallel to withstand a bus current level of 1000A. RC snubber is used to maintain a constant voltage across the device for smooth turn off. A 5kv MOV was designed and simulated in PLECS to analyze the path of the current, stress and energy recovery across the device. Understanding the fault energy management in the system is the key to design well behaved SSPD, studying the performance of inductance, snubber and MOV and the device controls will help is designing a better protective interrupting device.

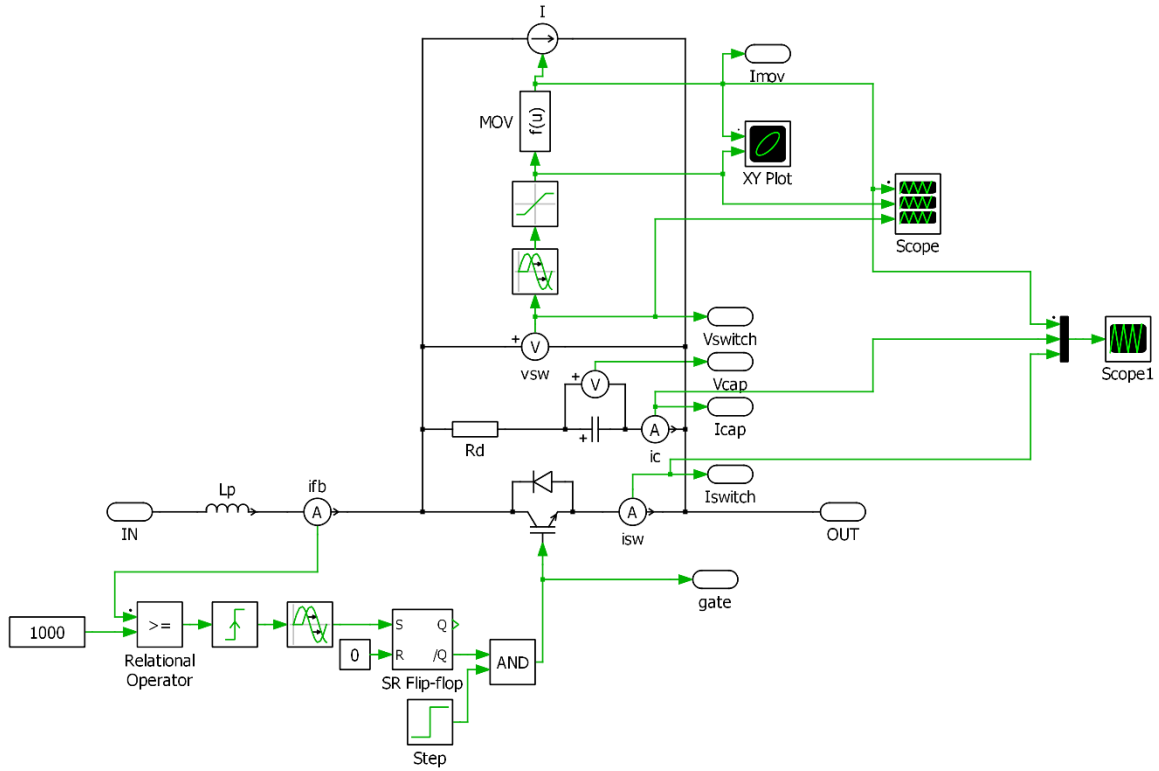


Figure 4-3 4kV Interrupter with MOV

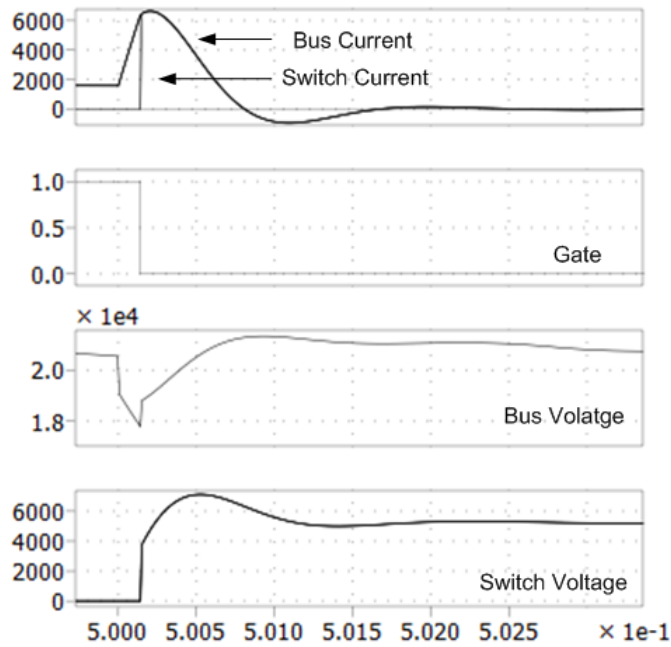


Figure 4-4 20kV Interrupting SSPD simulation results

#### 4.1.1 MOV Modelling:

In [22] authors have investigated the advantages of using RCD and MOV over using just MOV. Major limitation of using MOV is the parasitic inductance of connecting wire between switch and MOV, which leads to voltage spike in the system while commutation process. As we know that while commutation process of fault current any inductance in the path will lead to voltage surges in the system which should be avoided. If we use a snubber in addition to MOV, the constant voltage clamp developed by snubber capacitor will help in smooth transition of current paths. The breaker with MOV and RCD enlarge the paralleled capacitor between IGBT. During the commutation, the larger capacitor can reduce the slope of MOV current. Because of the existence of parasitic inductor in MOV loop, the lower slope rate means lower additional voltage spike.

In [23], to reduce the effect of parasitic inductance authors have tried to use two parallel MOVs in place of single MOV. The idea is to divide the voltage limitation from the energy absorption into two separate components to decrease the stress on the PE switch.  $MOV_E$  is used for energy absorption,  $MOV_{OV}$  is used to provide constant voltage across the switch which results in low voltage spike across the device. Basically characteristic of a single MOV has been divided into two separate MOVs. The MOV is characterized by its blocking voltage and energy absorption, the voltage rating of the MOV depends on the thickness of the component, and the energy rating is proportional to the volume of the component. There could be a tradeoff between amount of energy absorbed by  $MOV_E$  and level of voltage spikes across the device allowed by  $MOV_{OV}$ . Typically, the voltage level of  $MOV_E$  will be set by the system voltage and the energy of  $MOV_E$  is set by the magnetic energy that should be absorbed. Hence, it is the choice of  $MOV_{OV}$  and the voltage rating of the IGBT that is the trade-off that has to be done considering parasitic inductance in the system as well as the cost. [24] discuss about design aspects of series and parallel combination of varistors,

number of series MOV will decide voltage rating of the switch and number of parallel varistors will decide the amount of energy to be absorbed in the system. After the turn-off of the semiconductor branch, the current will be commutated to the varistor branch. Since the voltage level of the varistor in conducting state will be higher than the system voltage, the system current will decrease. The voltage level of the varistor will be a trade-off between how fast the system current decreases and the voltage stress applied to the semiconductor components. A high voltage level will rapidly decrease the current and hence limit the energy flowing through the system, but will require a higher voltage rating of the semiconductor branch resulting in higher costs. Naturally, the voltage level increases with increasing varistor voltage rating, but also decreases with increasing number of parallel components. The latter is due to that when the number of parallel components increase, the current in each device becomes lower which gives a lower effective voltage-current characteristic. Since galvanic isolation is not obtained by the varistors or the semiconductor switches, a disconnecter will be required in series with the breaker. Hence the varistor only has to withstand the system voltage until the disconnecter is opened and the opening time of the disconnecter will dictate the required energy absorption from the leakage current. However, if a fast disconnecter is used, this energy will be small compared to the inductive energy during the interruption of the current.

Figure 4-5 shows the simulation result for one of the mov used for 6KV rating, As we can see that in the graph, current through increased to a very high value once the voltage across the mov or the device reaches beyond the allowed value of 5.5KV. By allowing high amount of current through itself mov is providing a safe environment for the switching device in switching over voltage/surge condition.

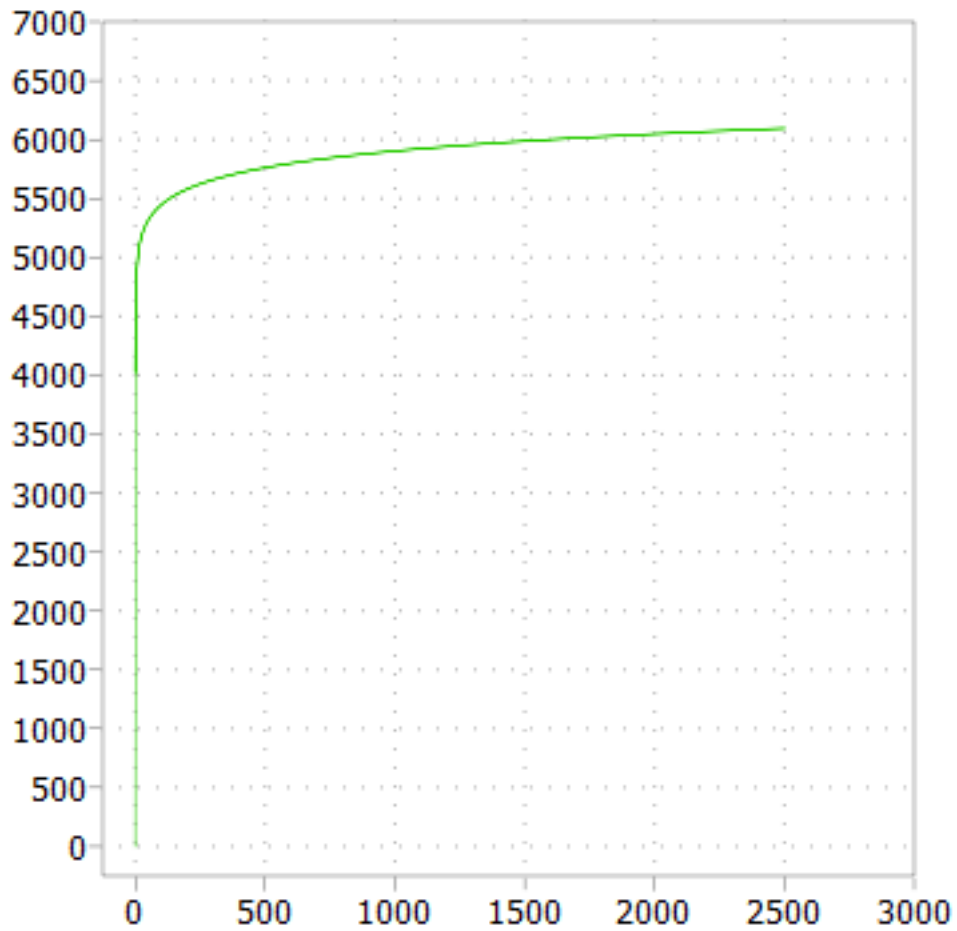


Figure 4-5 Simulation result of 6kV mov design

## 4.2 Limiting topology

A unidirectional Limiting SSPD actively limits the fault current using PWM to predefined level (usually zero current) and requires a combination of additional diodes to provide a freewheeling path for inductive energy and capacitive voltage clamping to provide a relatively stiff voltage against which the power semiconductors can switch as shown in Figure 4-6[20] [21] [22]. Figure 4-7 shows the limiting sspd model in plects to simulate the fault removal process for unidirectional dc system. Simulation results are provided in Figure 4-8 for the same system as in Figure 4-1 again

with four devices in series. A total bulk capacitance of  $4000\mu\text{F}$  was required with  $100\mu\text{H}$  of limiting inductance. For the  $20\text{kV}$  DC application these results indicate that only three devices are required in series. For limiting topology fault resistance and inductance plays role in defining the total time of fault current to free wheel to zero.

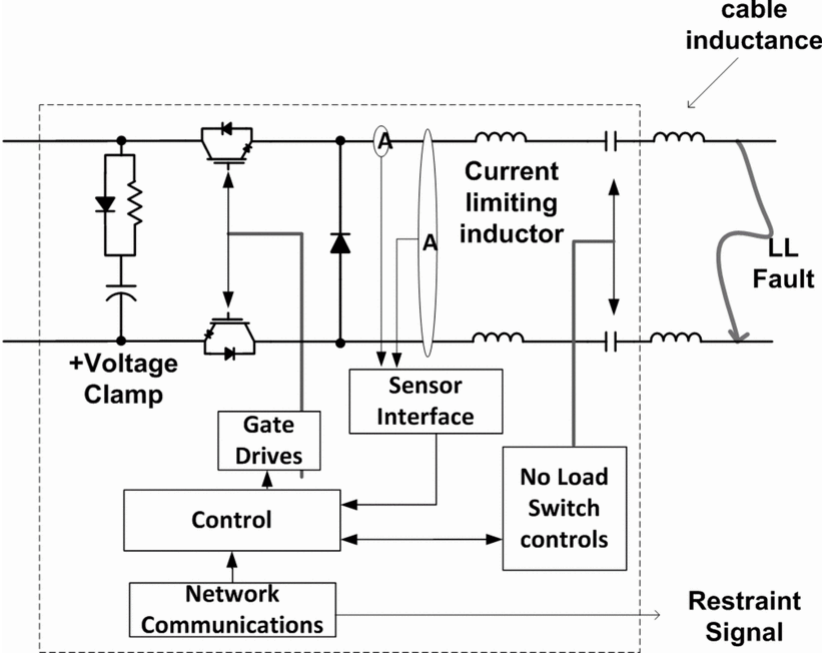


Figure 4-6 Limiting SSPD scheme for floating system

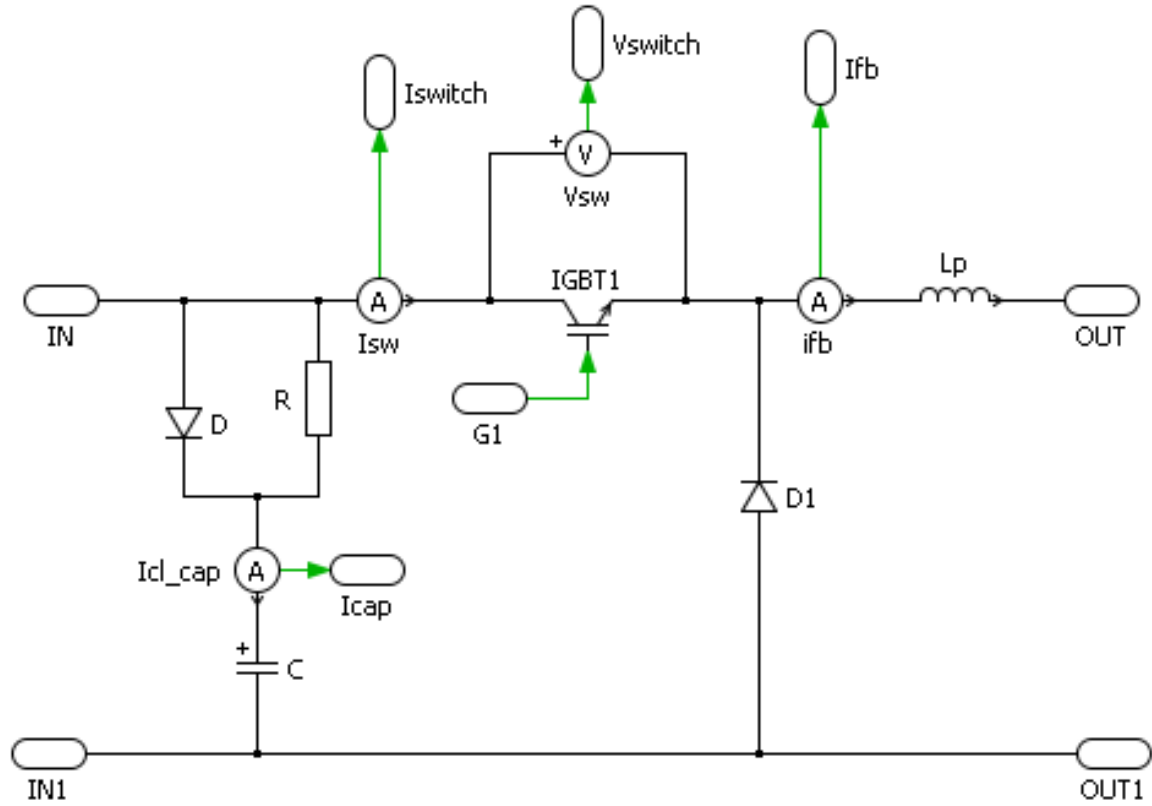


Figure 4-7 plects model for unidirectional limiting sspd

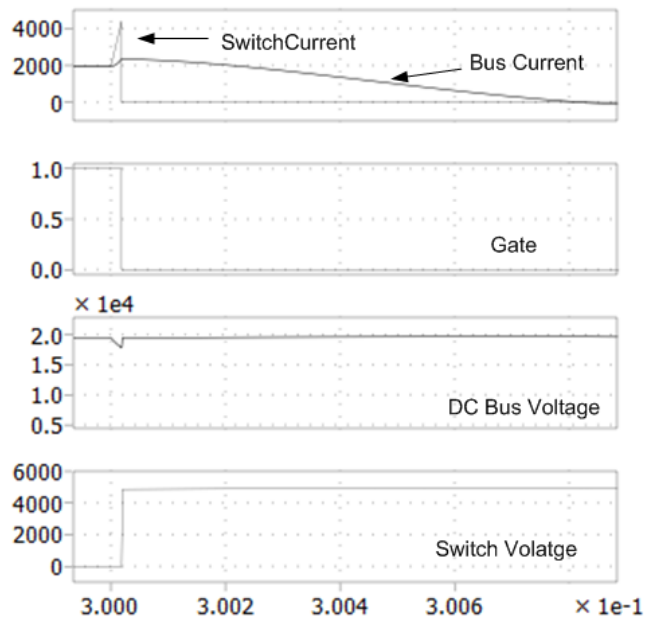


Figure 4-8 20kVLimiting SSPD simulation results

### 4.3 Dissipating topology

A unidirectional Dissipating SSPD, shown in Figure 4-9, utilizes additional active devices to divert energy into dissipative components [23]. The Dissipating SSPD requires a pre-charged capacitor in parallel with the commutating devices and sufficient resistance to dissipate the energy under all potential scenarios. One advantage of the Dissipating SSPD is that there is no need for current limiting inductance. The amount of cable inductance affects the energy that must be dissipated by the resistors and their resulting size.

Since cable length is limited in a shipboard application when compared to terrestrial systems, the size of resistors may be manageable for this application. Figure 4-10 shows the plects model to simulate the unidirectional dissipating sspd for DC bus faults. Simulation results for 20KV Dissipating SSPD are shown in Figure 4-11. In this implementation, each SSPD has a 400 $\mu$ F clamp storage capacitor. Here again, with this topology it may be possible to utilize only three series SSPDs per leg instead of four.

Dissipative has inherent quality of limiting the device voltage to very safe level by the use of hysteresis control of capacitor voltage across the devices, Also It does not need much higher inductance to limit the fault current because of its inherent design property.

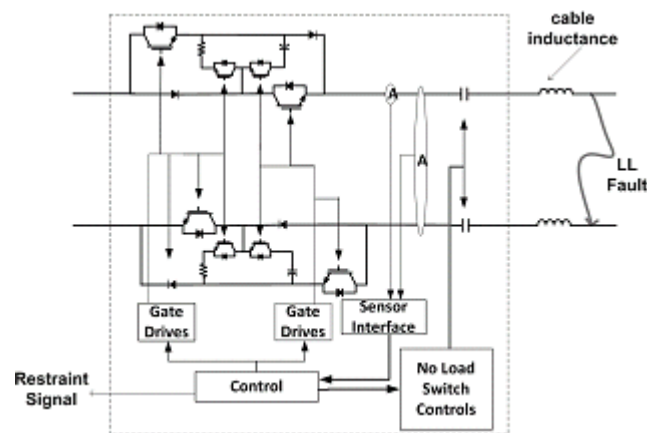


Figure 4-9 Dissipating SSPD for floating system



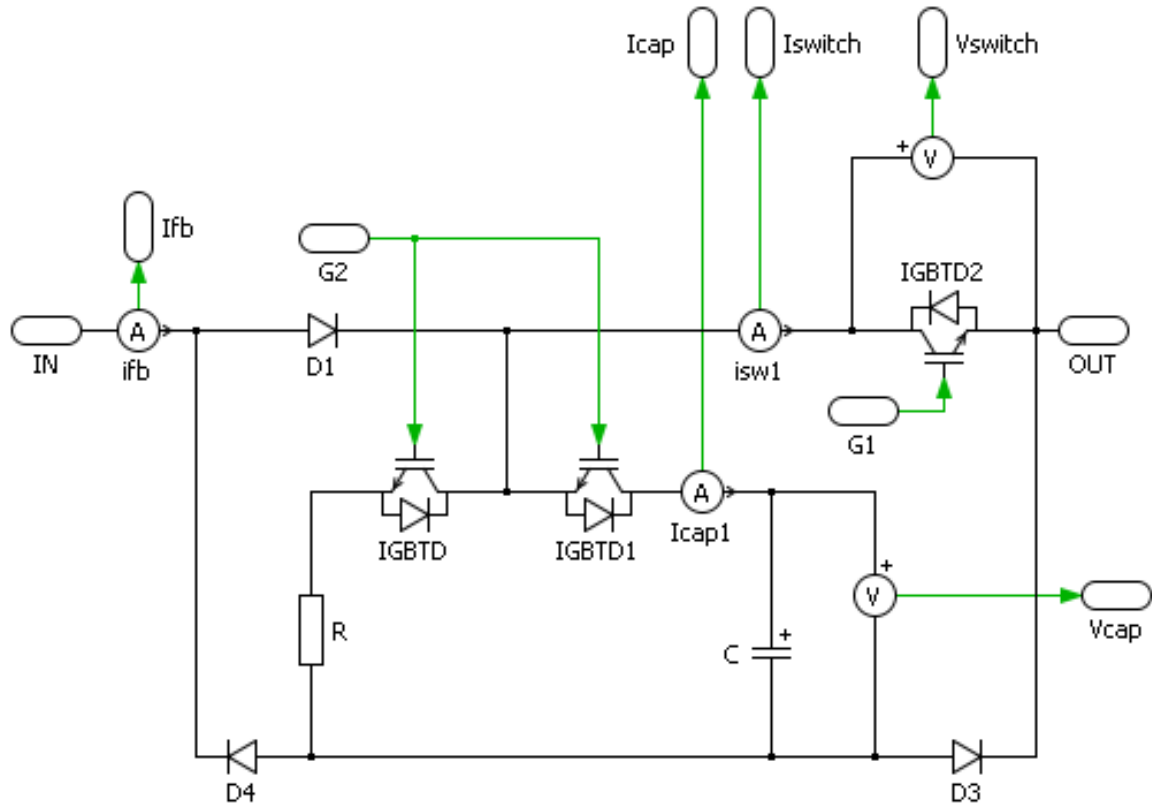


Figure 4-10 Plect model of unidirectional dissipative SSPD

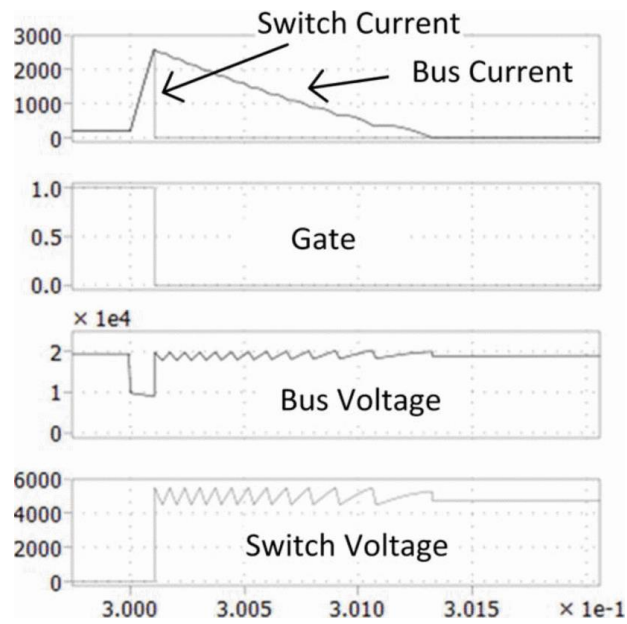


Figure 4-11 20kV Dissipating SSPD simulation results

## 4.4 Comparison and analysis of commutation stages of SSPD topologies through simulation for 4kV DC system

In order to make a valid comparison of the topologies, each was assumed to utilize a dual 10kV/240A SiC/JBS diode module in 10kV/240A SiC/JBS diode module in an appropriate configuration to the topology in order to minimize inter-connection minimize inter-connection inductance. A rated current of 500A was assumed which requires two parallel paths for continuous parallel paths for continuous current supply through-put. A 4kV system was simulated with the assumption that assemblies or assumption that assemblies or modules can be connected in series (depending upon the topology) in order to apply to higher in order to apply to higher voltage rated systems. The 4kVdc system was assumed with a constraint applied to the topologies that applied to the topologies that voltage during fault turn-off cannot exceed 6.5kV which is one of the drivers for required passive the drivers for required passive components to manage the commutation energy. Also, a total fault current sensing and gate drive current sensing and gate drive actuation delay of 5μseconds was assumed. Assuming a fault tripping level, a maximum allowable tripping level, a maximum allowable peak current of 3kA and a fault detection level of 1kA and sudden zero-ohm fault sudden zero-ohm fault application a di/dt limiting inductance of at least 13μH is required. In the shipboard IPS the cable shipboard IPS the cable inductance can be widely varying. It is assumed that the minimum cable inductance is 2μH and that the inductance is 2μH and that the maximum inductance to the fault is 50μH. The positive leg SSPD+ with the Interrupting SSPD is with the Interrupting SSPD is shown in

Figure 4-12 during three operating stages: (a.) Normal conduction to the load; (b.) Fault commutation through the snubber; (c.) Fault energy dissipation through the MOV. The Interrupting nomenclature was selected because the power semiconductors interrupt the flow of current to the fault and fault energy ultimately diverted to the MOV. The bidirectional Interrupting SSPD can be implemented with the 10kV/240A SiC/JBS diode module in a common source configuration. Assuming a continuous rating of 500A, two modules must be connected directly in parallel. It is assumed that some measures may be required in the gate drive design to ensure dynamic current sharing between devices. Care must also be taken to minimize the parasitic

inductance when paralleling the modules and connecting RC snubber and MOV components across the devices, otherwise, additional RC plus diode (RCD) voltage clamps would be required to mitigate the  $di/dt$  induced over-voltages during device turn-off. The purpose of the RC snubber across each paralleled set of devices is to provide an initial path through which fault current can pass when the MOSFET device(s) are commutated off. The resistive part of the RC snubber is required to dampen out ringing between any fault path inductance and the snubber capacitance,  $C_s$ , therefore some minimum inductance,  $L_p$ , is required to ensure that ring-up does not cause excessive voltage across the device or current through the device during fault commutation. The optimal values for  $L_p$ ,  $C_s$  and  $R_s$  are found by considering both low inductance cabling ( $2\mu\text{H}$ ) and high inductance cabling ( $50\mu\text{H}$ ). With low inductance the current stresses will be highest and with high inductance the commutating device(s) voltage stresses will be higher. In order to keep ringing from occurring and resultant increased current stress  $L_p=20\mu\text{H}$  is required. An MOV was selected with a clamping voltage of 4000V, modeled and included in the simulation. Simulation results are shown in Figure 4-13. After the time sensing and gate drive delay,  $t_d$ , the MOSFETs are commanded off and current diverts into the snubber capacitor ( $t_0 < t \leq t_1$ ). When the voltage across the device reaches 4000V ( $t_1 < t \leq t_2$ ) the MOV conducts. The remaining fault current is then diverted into the MOV where the remaining fault energy (a function of the system inductance between the source and fault) is dissipated ( $t_2 < t \leq t_3$ ). An important result of the simulation is how long it takes for bus current into the fault to be driven to zero, which indicates the delay required before the fault can be air gap isolated with a no load DC disconnect switch, which is 0.5mseconds ( $2\mu\text{H}$  cable inductance) and 1msecond ( $50\mu\text{H}$  cable inductance).

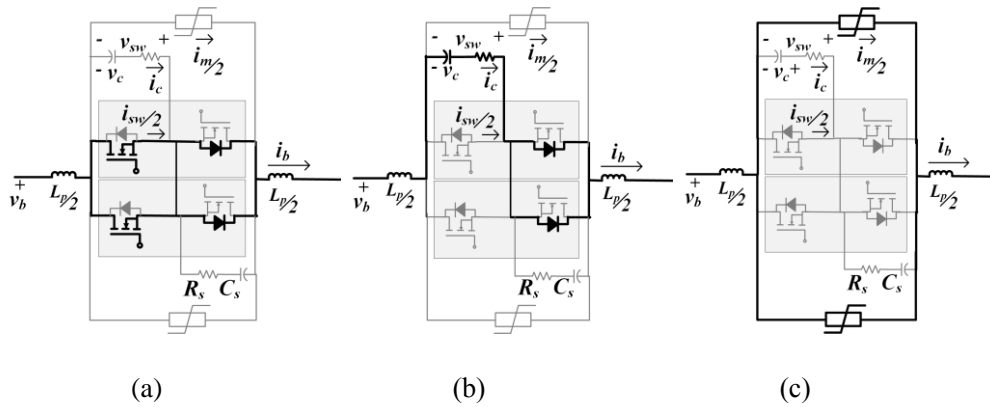


Figure 4-12 Interrupting SSPD and its commutation stages

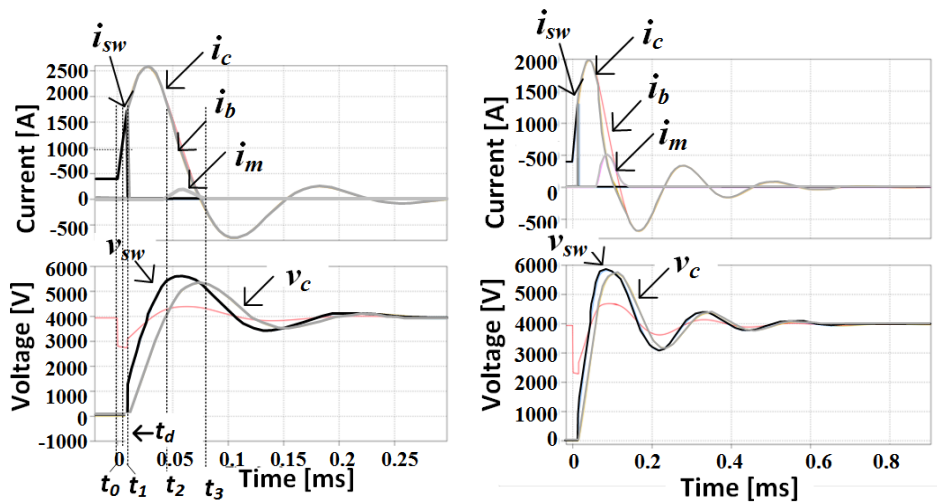
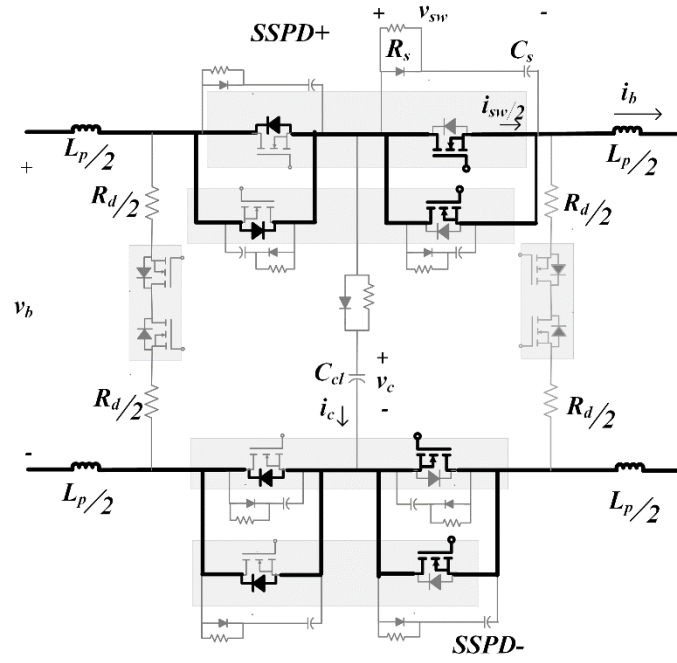


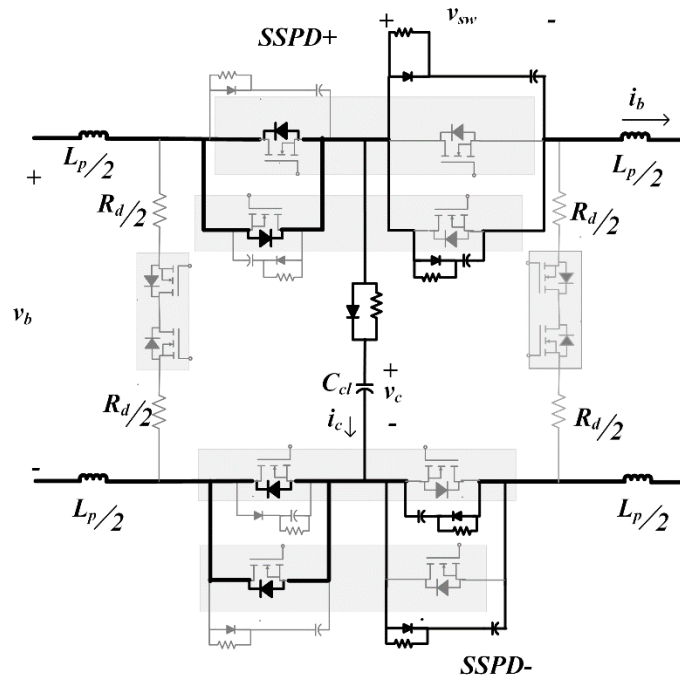
Figure 4-13 Interrupting SSPD simulation results for low cable and high cable inductances

A Limiting SSPD nomenclature implies that the fault current can be limited to predefined level by coordinated switching between the active power semiconductor(s) in series with fault and in a freewheeling path. The bidirectional topology of Figure 4-14 shows both the positive and negative legs (SSPD+ and SSPD-) and, like the Interrupting SSPD, can be implemented with common source of the SiC MOSFET modules. To drive fault current to zero the power semiconductor(s) are commanded off and a freewheeling path must be provided with a resistive component,  $R_d$ , to dissipate fault energy to zero. The three operating stages in Figure 4-14 are (a.) Normal conduction

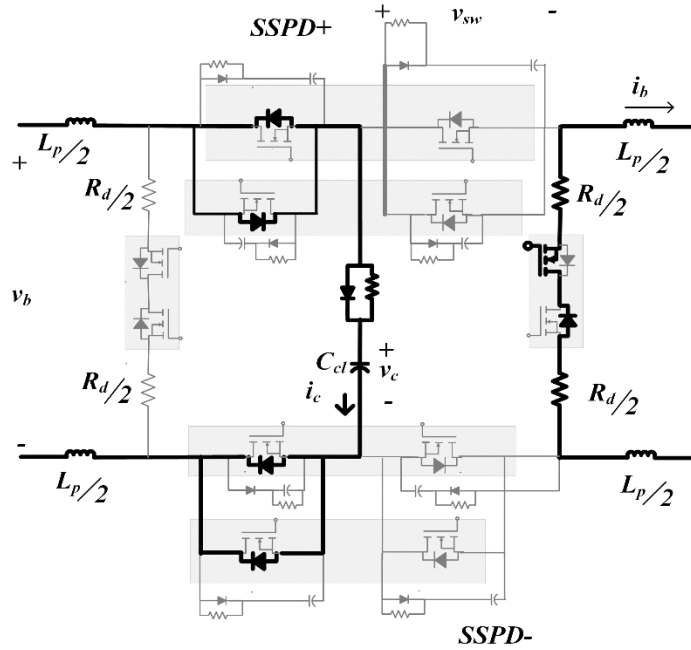
to the load; (b.) Fault commutation against the voltage clamping capacitor,  $C_{cl}$  and RCD snubber path and (c.) Fault energy dissipation by creating a freewheeling path that localizes the fault and decouples the fault path from the feed side of the SSPD. In a simple form, the bidirectional Limiting SSPD looks like two back-to-back dc-dc buck converters with devices that need to actively turn off being in the direction of the fault current flow with a diode freewheeling path to capture the inductive energy in the fault. The reason that active switches are added to the freewheeling path is to handle different kinds of fault paths. The bidirectional active switch in the freewheeling path provides flexibility to block current through a freewheeling path for such cases where unsymmetrical LG voltages might otherwise cause fault current to flow through diodes through an undesired path. Simulation results are shown in Figure 4-15 for a LL fault described by the commutation sequence of Figure 4-14. Comparing Figure 4-13 and Figure 4-15 the Limiting SSPD has tighter control of device voltage and current stresses but a commutation time that is less dependent on cable inductance than the Interrupting SSPD. This is due to the fact that the time to drive the current to zero is a function of the  $L/R$  time constant whereas for the Interrupting SSPD the time is influenced by damped resonance between inductance in the circuit and the snubber capacitor. The time to drive current can be reduced by reducing the value of  $R_d$ . There will be a trade-off between this time and the energy dissipated by the resistor.



(a)



(b)



(c)

Figure 4-14 Limiting topology and its commutation stages

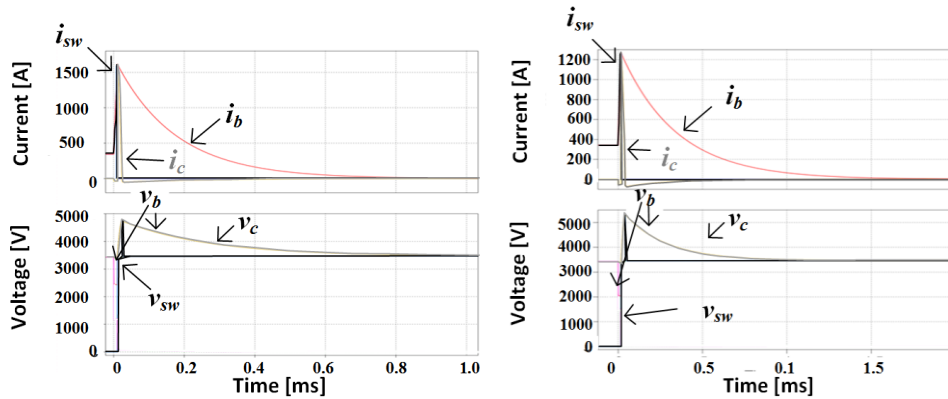


Figure 4-15 Limiting SSPD simulation results for low and high cable inductances

The Resistive SSPD and its commutation stage is shown in Figure 4-16. This topology is a derivative of SSPDs having an H-Bridge structure, introduced in [31]. Under the normal conduction, Figure 4-16(a), the current divides up between two parallel branches. When the main path devices are commutated off fault current is diverted through the forward diodes of devices in

the center path through a capacitor,  $C_{cl}$ , as shown in Figure 4-16(b). This capacitor is pre-charged to the nominal bus voltage level. When capacitor voltage,  $v_c$ , rises above a set-point level the center path devices are gated on, Figure 4-16(c), which diverts the fault energy through the  $R_d$  resistive path. When  $v_c$  has dropped to a set-point level that is below nominal by some difference the center path devices are gated off and the SSPD returns to the commutation state of Figure 4-16(b). This sequence is alternatively repeated until the fault current is driven to zero. The speed at which fault current is eliminated is a function of the pre-set hysteresis band around the nominal bus voltage, which controls voltage stresses, and the value of  $R_d$ , which controls peak instantaneous power. The simulated performance is shown in Figure 4-17. It should be noted that the total commutation time is much smaller than the other topologies. The amount of inductance in the fault path directly affects the energy that must be dissipated by resistor(s) in the SSPD so the amount of deliberate inductance added to the SSPD,  $L_p$ , should be kept to a minimum while keeping the switching device current stress within acceptable constraints given the need to limit  $di/dt$  caused by control and gate drive delays. For terrestrial applications this sensitivity to inductance. However, since cable length is relatively limited in shipboard applications resistor sizing may be manageable.



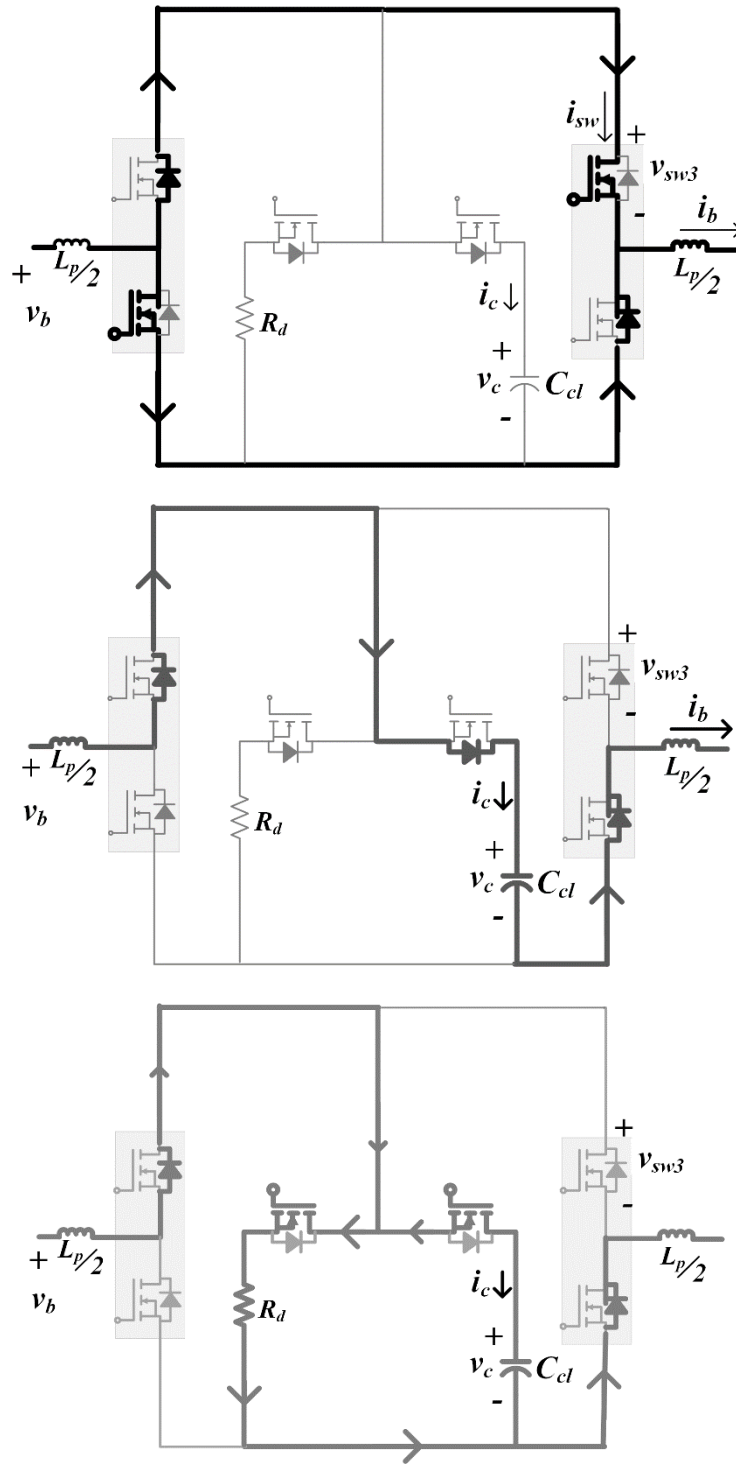


Figure 4-16 Dissipative topology commutation

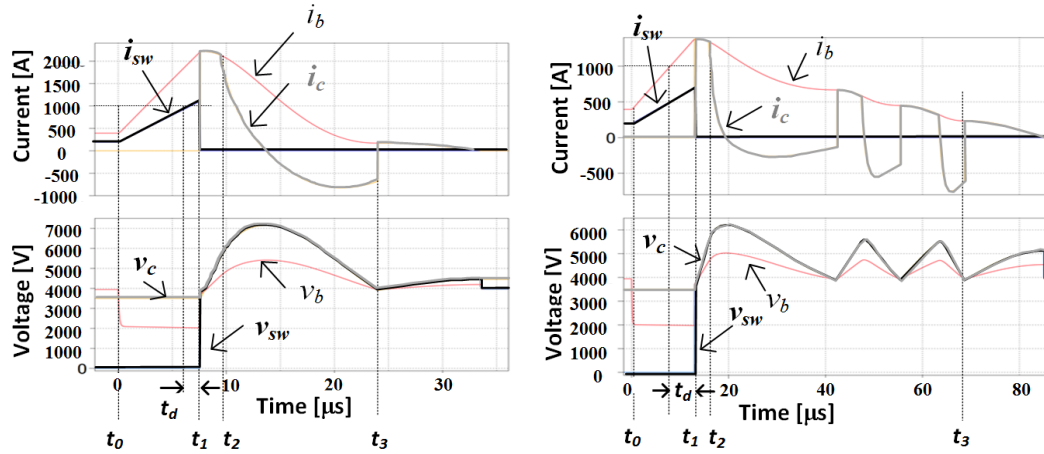


Figure 4-17 Dissipative topology commutation simulation for low and high cable inductances

Table 2 shows a summary comparison of the different SSPD topologies for a 4kVdc system. Considering only complexity as a criterion, the Interrupting SSPD is the most attractive because it requires the least number of gate drives and modules. The Resistive SSPD has complexity as the Limiting SSPD from an active component count. The Resistive SSPD is also attractive because it inherently divides the bus current into two well controlled paralleled current paths per assembly and the management of inter-connection inductance between paralleled modules is more easily achieved.

Table 2 Comparison of SSPD topologies for a 4kVdc system using SiC MOSFET dual modules

	$L_p$	$C_s$	$C_{cl}$	No. of Gate Drives per SSPD assembly	No. of Modules per SSPD assembly	Dissipative Components
<b>Interrupting</b>	20 $\mu$ H	20 $\mu$ F	N/A	8	4	LittleFuse V202BB60 with clamping voltage of 5200V
<b>Limiting</b>	20 $\mu$ H	0.5 $\mu$ F	10 $\mu$ F	12	6	HVR International Epoxy Coated Discs, 0.5 $\Omega$
<b>Resistive</b>	10 $\mu$ H	N/A	2 $\mu$ F	12	6	HVR International Aluminum Cooling Fins, 2 in series, 3 in parallel, 5 $\Omega$

## **Chapter 5 Proposed research instrument design for DC fault study and simulation results**

In order to update present DC protection standards (IEC 60909) there is a need of DC short circuit fault tester to perform fault characterization and develop protective system requirements. To achieve this, the short circuit tester must be developed that can (1) safely make and break DC current; (2) apply short circuits without impose additional  $di/dt$  limits that would not be present in the actual system; (3) remove short circuits without imposing required delays; (4) present a nearly zero impedance fault to the system; and (5) sustain long term fault currents.

Based on the principle of dissipative topology of protection, the proposed static fault simulator is designed to emulate all types of DC faults. By switching H bridge topologies in a manner to get +Vdc, -Vdc or 0 across each bridge we can simulate any kind of DC fault across the device. Switches and batteries in the device should be able to sustain the fault energy. That's why a proper heatsink design is needed. Resistor and capacitor plays an important role while turn off the device by dissipating inductive energy of the circuit into resistor bank and clamping voltage across the devices at a constant level.

### **5.1 Static fault simulator simulation analysis**

The Static Fault Simulator will be configurable to simulate any type of fault that can occur, including intermittent high resistance faults that can be tailored through intelligent controls to mimic the effect of arc faults. The Static Fault Simulator must be a solid state switch solution that has the same capabilities as a SSCBs—that is when the fault is removed there must be a capability to actively drive current to zero and there must be a way to divert the inductive energy in the fault to a place where it can be dissipated. Most solid state circuit breakers require a current limiting inductor and other passive devices to ensure safe commutation when the switch is opened.

However, the dissipating H-bridge topology, shown in Figure 5-1 as a means for applying a short circuit to a DC system, utilizes additional active switches to divert energy into dissipative components when it is commutated off and requires no additional inductor to limit the rate of rise of current. Instead, any existing system inductance affects the energy that must be dissipated by the resistors and resulting size. This characteristic makes this device foundation short circuit tester from the perspectives of requirements (1) -(5) stated above. This configuration enables application of sustained faults by sharing the load current between all eight switches and provides a multiple modular configuration that can be configured to apply any type of fault to the system. It is possible for the topology of the circuit in Figure 5-1 to be stacked and paralleled so that it can be scalable to use for testing of MVDC systems. Figure 5-5 shows the simulated electrical variables in the SSCB during a fault extinction. The fault current is diverted into the storage capacitor when the fault current is extinguished and then energy is alternatively traded between the capacitor and dissipating resistor, keeping capacitor voltage within safe limits using a hysteresis controller. Figure 5-6 shows how the circuit sustains faults during fault characterization by alternatively sharing currents between different halves of the H-bridge in order to mitigate internal device stresses.

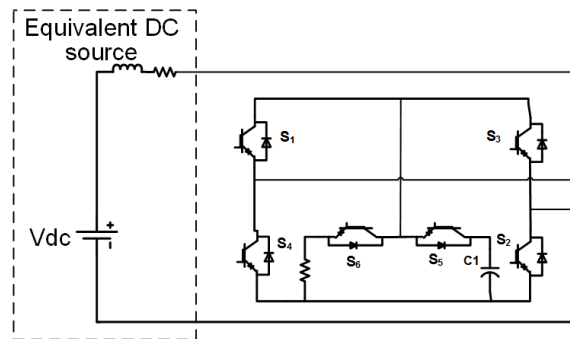


Figure 5-1 Basic fault simulator model

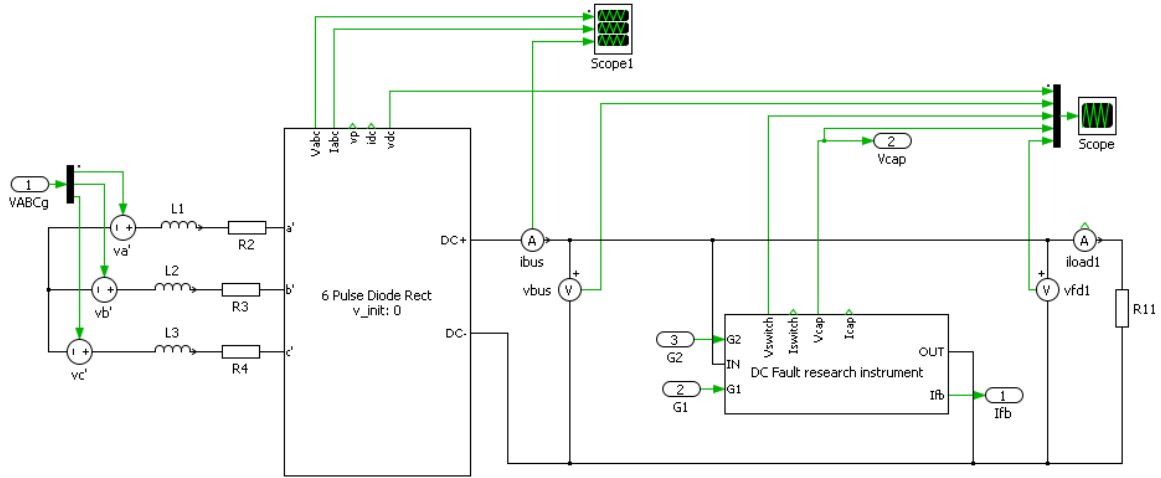


Figure 5-2 Basic outline of dc fault characterization system

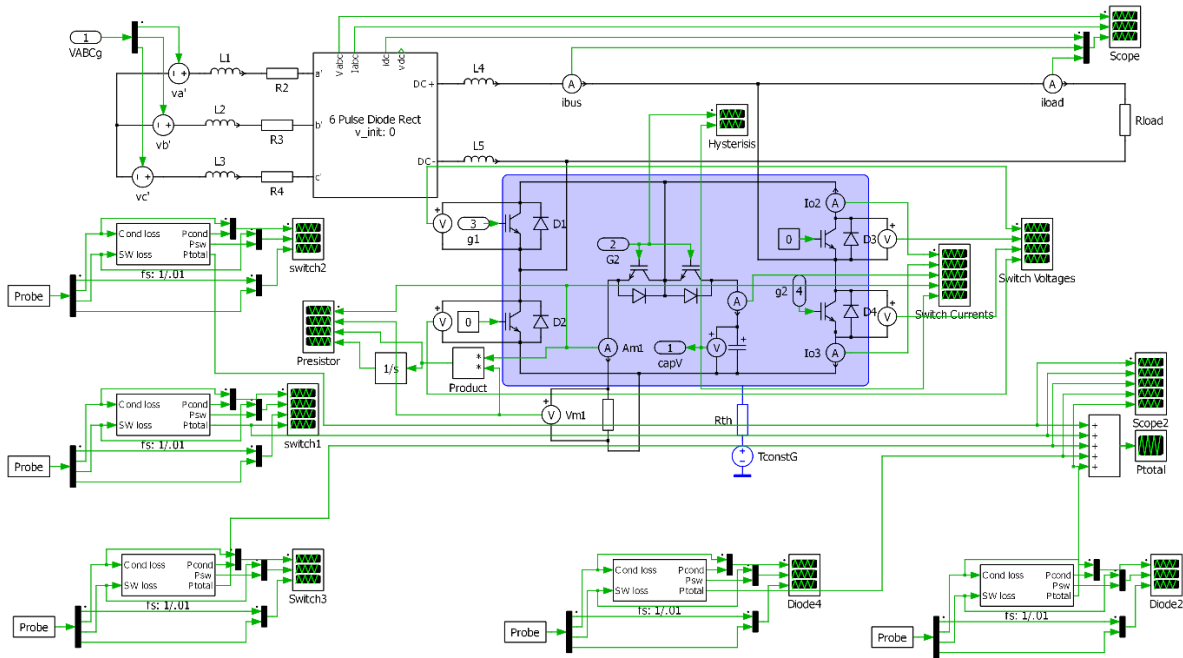


Figure 5-3 plects model for proposed fault characterization instrument

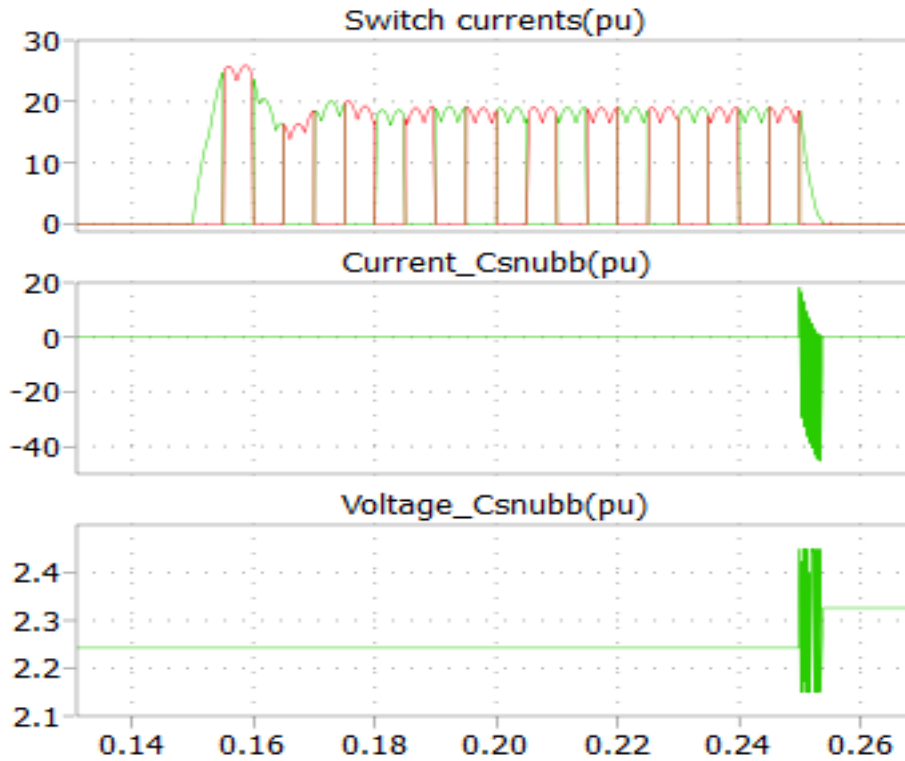


Figure 5-4 Simulation results for working of fault simulator instrument

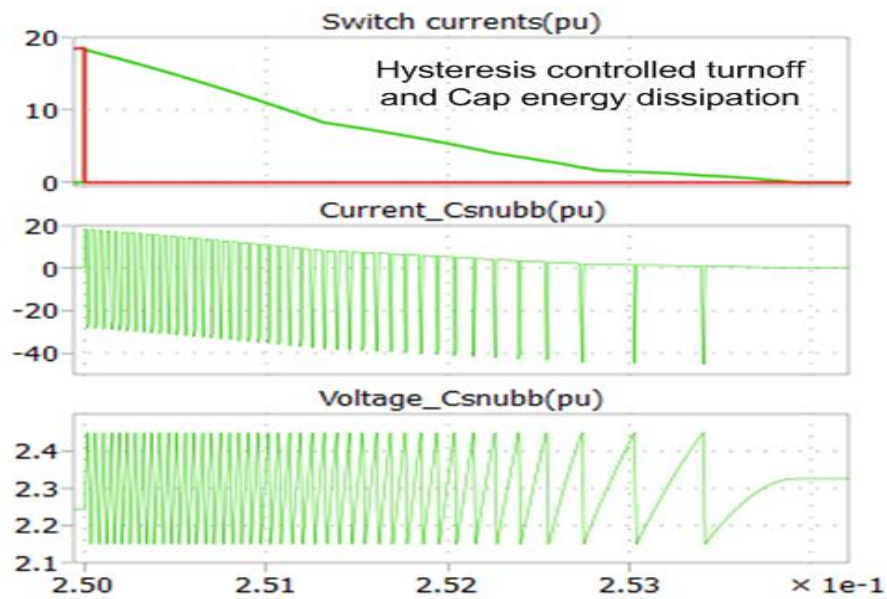


Figure 5-5 Simulation of fault extinction through hysteresis controlled cap energy dissipation

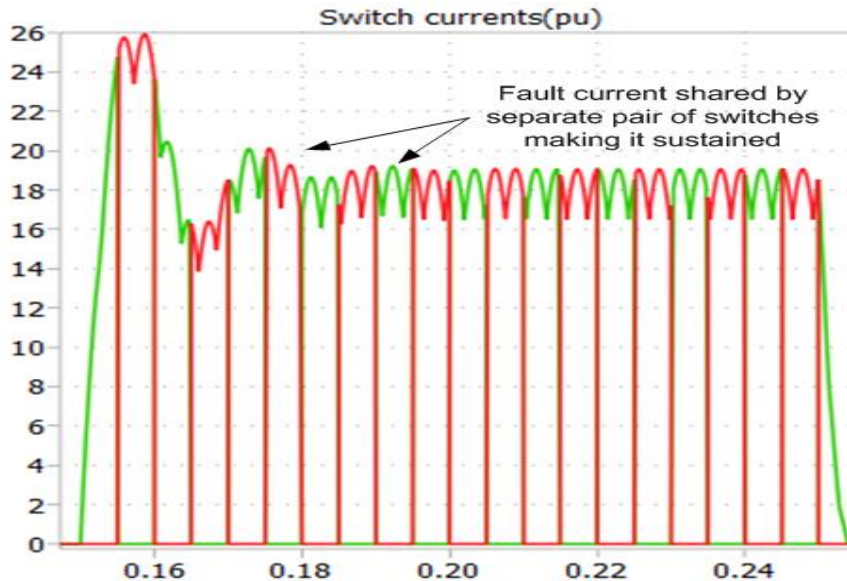


Figure 5-6 Simulation of H bridge currents during sustained fault

## 5.2 Heat sink design

### 5.2.1 Selection process of heat sink[21]

Heat sink design is very important component for complete design of any power electronic topology. Thermal heat management should be considered for all the power electronic topologies for proper functioning of the device. Temperature of the equipment have very strong impact on reliability, and life expectancy of the device. That means proper management of the temperature of the device will lead to higher performance of the device. So usually device manufacturers or design engineers suggest safe operating temperature of the device, by designing proper heat sink, we can maintain the device temperature within the allowed limit and ensures the reliability of the instrument being designed.

Heat sink dissipates heat from hot surface (the device base plate) to ambient cooler environment usually air. Heat sinks has high surface area for energy dissipation into ambient temperature environment which usually is air or liquid. Efficiency of the heat sink is defined as amount of heat dissipated for particular surface area. Using heat sink one can help the devices to cool down faster

and limit the device temperature within maximum allowable temperature limit as per manufacturer.

Optimization of heat sink performance is very important for the design of the overall system. For the design and optimization of the heat sink for our project we used the online tools available on the website of companies like Merson and C&H technology to get an idea of available product in the market. To design a heat sink you need to know amount of heat generated by solid state devices which needs to be dissipated, maximum allowable heat sink temperature, ambient coolant temperature, size of the heat sink, budget limit. You can play with fin height, fin length, fin spacing, number of fins, shape and thickness of base plate and heat sink materials to get your optimized heat sink design.

## **Chapter 6 Conclusions and future work**

This thesis has provided a detailed overview of the protection requirements for future MVDC systems. From the literature on SSPD topologies, this thesis has analyzed three topologies: Interrupting, Limiting and Resistive. WBG SiC power semiconductors will be necessary in order to achieve high system efficiency and to avoid growth of thermal management requirements. The Interrupting SSPD is the most popular approach and will be attractive as SiC p-GTOs, SGTOs and ETOs become commercially available. The Limiting SSPD is an inferior option because a scalable approach cannot be easily achieved. The Resistive SSPD is an attractive option because modular, scalable packaging can be achieved and voltage stresses in the Resistive SSPD can be well-controlled it is possible to reduce the number of series modules as the SSPD voltage rating increases. Hardware implementation and experimental validation of Dissipative topology is future work of this thesis.



## References

- [1] N. Hadjsaid, J. F. Canard and F. Dumas, "Dispersed generation impact on distribution networks," in *IEEE Computer Applications in Power*, vol. 12, no. 2, pp. 22-28, Apr 1999
- [2] N. Jayawarna, N. Jenkins, M. Barnes, M. Lorentzou, S. Papathanassiou, N. Hatziagyiou, "Safety Analysis of a MicroGrid," *International Conference on Future Power Systems*, 2005, vol., no., pp. 1-7, 16-18 Nov. 2005
- [3] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, P. Crolla and G. M. Burt, "Optimizing the Roles of Unit and Non-unit Protection Methods Within DC Microgrids," in *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2079-2087, Dec. 2012
- [4] M. Rose and R. M. Cuzner, "Fault Isolation and Reconfiguration in a Three-Zone System," *IEEE Electric Ship Technologies Symposium*, June 21-24, 2015, Washington DC
- [5] Baran, M.; Mahajan, N.R., "PEBB Based DC System Protection: Opportunities and Challenges," *Transmission and Distribution Conference and Exhibition, 2005/2006 IEEE PES* , pp.705-707, 21-24 May 2006
- [6] D. M. Bui, S. L. Chen, C. H. Wu, K. Y. Lien, C. H. Huang and K. K. Jen, "Review on protection coordination strategies and development of an effective protection coordination system for DC microgrid," *Power and Energy Engineering Conference (APPEEC), 2014 IEEE PES Asia-Pacific, Hong Kong, 2014*, pp. 1-10
- [7] D. Boroyevich, I. Cvetković, D. Dong, R. Burgos, F. Wang and F. Lee, "Future Electronic Power Distribution Systems A Contemplative View," *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on, Basov, 2010*, pp. 1369-1380.
- [8] IEC 61660-1, "Short-circuit currents in d.c. auxiliary installations in power plants and substations - Part 1: Calculation of short-circuit currents".
- [9] Kempkes, M.; Roth, I.; Gaudreau, M., "Solid-state circuit breakers for Medium Voltage DC power," *Electric Ship Technologies Symposium (ESTS), 2011 IEEE* , pp.254,257, 10-13 April 2011
- [10] Juvekar, S.; Compton, B.; Bhattacharya, S., "A fast acting DC solid state fault isolation device (FID) with Si and SiC devices for MVDC distribution system," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pp.2005,2010, 15-20 Sept. 2012
- [11] Corzine, K.A.; Ashton, R.W., "Structure and analysis of the Z-source MVDC breaker," *Electric Ship Technologies Symposium (ESTS), 2011 IEEE* , pp.334,338, 10-13 April 2011

- [12] Corzine, K., "Dc micro grid protection with the z-source breaker," Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE , pp.2197,2204, 10-13 Nov. 2013
- [13] Chang, A.H.; Avestruz, A.; Leeb, S.B.; Kirtley, J.L., "Design of DC system protection," Electric Ship Technologies Symposium (ESTS), 2013 IEEE , vol., no., pp.500,508, 22-24 April 2013
- [14] Liu, Yusi; Farnell, Chris; Zhang, Hao; Escobar-Mejia, Andres; Mantooh, H.Alan; Balda, Juan Carlos; Ang, Simon S., "A silicon carbide fault current limiter for distribution systems," Energy Conversion Congress and Exposition (ECCE), 2014 IEEE ,pp.4972,4977, 14-18 Sept. 2014
- [15] Zhang, H.; Ang, S.S.; Farnell, C.; Liu, Y.; Balda, J.C.; Mantooh, H.A., "A sic SGTO/PIN diode power electronic module for a fault current limiter," Power Electronics for Distributed Generation Systems (PEDG), 2013 4th IEEE International Symposium on, pp.1,7, 8-11 July 2013
- [16] Hefner, A., "Industry requirements and general trends for compound semiconductors", IEEE Applied Power Electronics Conference and Exposition (APEC), March 2015
- [17] Lawson, K.; Bayne, S.B.; Lacouture, S.; Lin Cheng; O'Brien, H.; Ogunniyi, A.; Scozzie, C., "Safe Operating Area and Long-Term Reliability of 9-kV Silicon Carbide PNP Super Gate Turn-Off Thyristors," Electron Device Letters, IEEE , vol.35, no.8, pp.862,864, Aug. 2014
- [18] J. Hafner, B. Jacobson, "Proactive hybrid HVDC breakers—a key innovation for reliable HVDC grids", Cigresymposium, Bologna, Italy, 13-15 Sept. 2011
- [19] <http://www.abb.com/cawp/seitp202/e84e6cf2b5200c57c1257aaf003cb9dd.aspx>
- [20] Piovan, R.; Gaio, E.; Novello, L., "Performance Analysis of a Hybrid IGCTs-Mechanical Dc Circuit Breaker for Quench Protection of Superconducting Magnets," Fusion Engineering, 2007. SOFE 2007. 2007 IEEE 22nd Symposium on, pp.1,4, 17-21 June 2007
- [21] S. Lee, "Optimum design and selection of heat sinks," in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A, vol. 18, no. 4, pp. 812-817, Dec 1995.doi: 10.1109/95.477468
- [22] H. Li, J. Zhou, Z. Liu and D. Xu, "Solid State DC Circuit Breaker for Super Uninterruptible Power Supply," 2014 International Power Electronics and Application Conference and Exposition, Shanghai, 2014, pp. 1230-1235
- [23] J. Magnusson, R. Saers, L. Liljestrang and G. Engdahl, "Separation of the Energy Absorption and Overvoltage Protection in Solid-State Breakers by the Use of Parallel Varistors," in IEEE Transactions on Power Electronics, vol. 29, no. 6, pp. 2715-2722, June 2014.
- [24] J. Magnusson, A. Bissal, G. Engdahl and J. A. Martinez-Velasco, "Design aspects of a medium voltage hybrid DC breaker," IEEE PES Innovative Smart Grid Technologies, Europe, Istanbul, 2014, pp. 1-6.

- [25] Cuzner, R.M.; Bendre, A.R.; Widmann, J.D.; Stonger, K.A.; Peshman, S.M.; Carlton, J.S.; Fischer, J.A., "Considerations when diode auctioneering multiple DC buses in a non-isolated DC distribution system," Electric Ship Technologies Symposium (ESTS), 2011 IEEE , vol., no., pp.277,282, 10-13 April 2011
- [26] Cuzner, R.; MacFarlin, D.; Clinger, D.; Rumney, M.; Castles, G., "Circuit breaker protection considerations in power converter-fed DC Systems," Electric Ship Technologies Symposium, 2009. ESTS 2009. IEEE , vol., no., pp.360,367, 20-22 April 2009
- [27] ONR ARC Proposal, "Silicon Carbide 2MW 10kV/240A High Power Modules for High Power Navy Shipboard Applications", FY14-F15
- [28] R. Marconato, "Electric Power Systems", CEI - Comitato Elettrotecnico Italiano, 2002.
- [29] Krause, P. C., Wasynczuk, O., and Sudhoff, S. D., "Analysis of Electric Machinery and Drive Systems", Wiley-IEEE Press, 2nd ed., New York 2002.
- [30] A. Vicenzutti, E. De Din and G. Sulligoi, "Transient short-circuit analysis in DC on-board distribution systems fed by synchronous generators through 6-pulse diode rectifiers," Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS), 2015 International Conference on, Aachen, 2015, pp. 1-6.
- [31] Kohlmann, M.; Kueper, T.; Staudt, V.; Steimel, A., "Combined Solid-state AC/DC switch for laboratory applications," PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of , pp.1-7, 20-22 May 2014