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MEDICAL GRADE HIGH FREQUENCY POWER DISTRIBUTION UNITS

by

Ezana T. Mekonnen

A Thesis Submitted in

Partial Fulfillment of

Requirements for the Degree of

Master of Science

in Engineering

at

The University of Wisconsin-Milwaukee

December, 2012

ABSTRACT

HIGH FREQUENCY POWER DISTRIBUTION UNITS

by

Ezana T. Mekonnen

The University of Wisconsin-Milwaukee, 2012

Under the Supervision of Professor Adel Nasiri, PhD

The focus of this thesis is to design, model, build, and test a series resonance converter that uses a high frequency isolation transformer, offering significant reduction in size and cost, for powering a Computed Tomography (CT) scanner. The design increases the power quality for the load by isolating the grid side disturbances, and providing regulated desired voltage. The proposed architecture also allows for an optimized point of integration with an UPS, a regulated DC bus to improve waveform fidelity of x-ray generator, and active monitoring and control of the power architecture. Conventional CT systems use a 60Hz transformer, which not only occupies large footprints but also uses large amounts of copper and iron with increasing cost trajectory. In comparison to the traditional Power Distribution Units (PDU), the medical grade high frequency PDU presented in this thesis provides higher power quality and performance at a lower cost.

The new CT systems possess unprecedented performance capability in terms of rotational speed and x-ray voltage modulation (“Ultra-Fast kV”) fidelity. In order to

achieve such capabilities, a tightly regulated high power DC bus (700VDC, 150kW) is required. The system implemented in this thesis satisfies these new requirements. Design requirements, proposed architecture and controls, modeling, implementation and test results of the proposed system, including thermal analysis and electromagnetic compatibility, are presented in details in this thesis.

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LIST OF ABBREVIATIONS

AC – Alternating Current

CCM – Continuous Conduction Mode

CFM – Cubic Feet per Minute

CT – Computed Tomography

DC – Direct Current

DCM – Discontinuous Conduction Mode

EMI – Electro Magnetic Interference

FPGA – Field Programmable Gate Array

HFPDU – High Frequency Power Distribution Unit

IGBT – Insulated Gate Bipolar Transistor

PDU – Power Distribution Units

PLR – Parallel-Loaded Resonant

PWM – Pulse Width Modulation

RMS – Root Mean Square

SLR – Series-Loaded Resonant

TTL – Transistor–transistor logic

UFKV – Ultra-Fast KV

CHAPTER I

1. INTRODUCTION

Medicine has been greatly advanced in large part to the discoveries related to imaging devices such as x-ray machines. Computed Tomography (CT) is medical imaging system that utilizes x-ray light to produce internal image of patients by rotating the x-ray source and detector, which are located 180 degree apart, around the patient.



Figure 1-1: A picture of GE's existing VCT660 CT scanner.

Some of the key components that result in not only competitive advantages, but also produces great clinical value for CT system are:

- Longer Z-axis coverage that can capture image of an entire organ in a scan
- Wider bore size capable of accommodating larger patients

- Faster rotational speed to reduce motion artifacts
- Robust Ultra-fast KV waveform fidelity for consistent result within views

Among other things, the aforementioned feature requires higher power for x-ray generation, and tighter output voltage regulation to the CT Power Distribution Unit (PDU) to support faster speed and improved UFKV waveform fidelity. This paper presents 150kW rated medical grade power distribution unit that provides system isolation, regulates output voltage, and reduces scan room footprint in an economically feasible method.

1.1 Background

Power supplies for medical devices fundamentally fall into strict sets of regulatory requirement in order to protect both patients and operators. This includes strict guidelines on leakage currents, conducted emissions, and whole set of immunity capabilities. Today's CT system contains a power distribution unit that provides galvanic isolation, taps for voltage adjustment, and high power unregulated DC voltage. The current power architecture, which is shown in figure 1-2 below, illustrates the power distribution unit and the major CT load. Some of these major loads are the x-ray Inverters, which require around 100 kW of peak power and gantry motor around 15 kW of peak power. The additional secondary winding, which accounts for roughly 10 kW of average power, provides power to all the electronics that are used to energize the system.

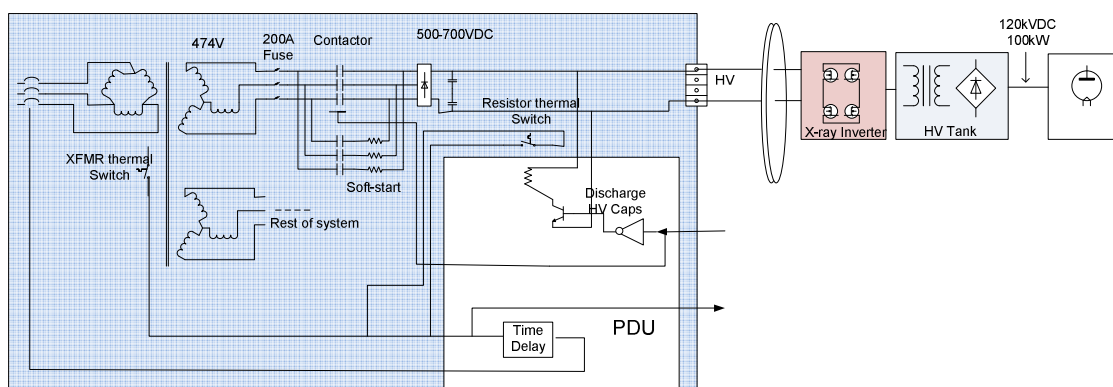


Figure 1-2: Block diagram illustrating current CT PDU architecture

From a close overview of the current CT PDU one would notice the possible variation with the unregulated high power DC bus voltage as a result of the high step load. In a typical setting, where the main power source is 3-phase 480VAC, the DC output can vary anywhere from 660VDC during no-load to 500VDC during 100kW x-ray generation. This variation puts lots of pressure on the x-ray generator controller to deliver continuous output voltage within the variation. In addition, an increase in the gantry speed puts tighter restriction on the DC bus voltage, which can be very difficult to achieve without some means of regulating the DC bus voltage.

The first approach to the DC bus voltage regulation was to introduce a DC/DC or AC/DC power supply that can be used as a buffer between the PDU and the major CT load, such as, the x-ray generator and gantry motor. This calls for a 100kw peak and 20kW average source power supply. Unfortunately, such a solution not only adds equipment to the already crowded scan room, but also lacks the economic merits for consideration. This paper presents an innovative and integrated solution that addresses the new requirements for the next generation of CT PDUs, while being cost-effective.

1.2 Thesis Goal and Objectives

The goal of this research is to design medical grade power distribution unit that has regulated high peak power DC voltage capable of handling step loads with the following specifications:

Table 1-1 lists show the new requirement for the next generation CT Power Distribution Unit.

TABLE 1-1: THE NEW CT PDU SPECIFICATION

Item	Rating	Unit
Input Voltage	480 +/- 30%	VAC
Output Voltage	700 +/- 5%	VDC
Peak Power	150	kW
Average Power	20	kW
Leakage Current	<5	mA
Efficiency	>90	%

To meet the aforementioned requirement, this research will investigate the use of resonance converter topology with integrated isolation transformer. This paper will discuss most of the critical point that are necessary to put the resonance converter topology concept into practice.

Chapter 2 will provide an overview of a couple of resonance convert topologies, and analysis their mode of operation.

Following the overview of resonance converter, Chapter 3 will discuss the specific resonance converter that was selected for this project. In addition, it will discuss the operational principle and mathematical overview of the selected topology.

Chapter 4 will briefly cover the isolation transformer that is used on this project, which is a key contributor to the overall cost and size advantages of the proposed HFPU.

In chapter 5, the discussion will focus on the selected control architecture, followed by analysis of the robustness of the control and performance.

In what seems to be the most important measurement parameter, when thinking about part selection and the implementation phase, chapter 6 will be fully dedicated toward thermal analysis and simulation of the proposed topology.

Chapter 7 will address the additional scrutiny that medical grade devices face, and what makes the propose topology particularly risky and its means of mitigation.

Chapter 8 presents a prototype of the proposed topology and discussed experimental results. In this chapter, the results have been evaluated to make sure that the above specifications have been met.

Finally, chapter 9 summarized the work performed for the thesis and the proposed solution before concluding with a recommendation that address the stated problems.

CHAPTER II

2. RESONANT POWER CONVERTERS

One of the drawbacks of most switch-mode converters is related to stress on the switching devices. The reason being, these power switches may have to turn on or off at the full power. This issue is even more problematic with the increase in power and switching frequency. This leads way to a topology that allows for zero-current or zero-volt switching by removing the energy from the switch to some form of LC resonance during the switch transition, known as resonance converts.

Resonant converters are defined as the combination of converter topologies and switching strategies that result in zero-voltage and/or zero-current switching [11]. One way of classifying resonance converter is based on the arrangement of the resonant circuitry to what is known as Series-Loaded resonant converters (SLR) and Parallel-Loaded resonant converters (PLR). The SLR and PLR topologies are limited to bridge-type converters that use an LC resonant tank to create conditions for lossless turn-on or turn-off of the semiconductor switches (13)

2.1 Series Resonant Converter

A series resonance converter gets its name from the series arrangement of the resonant inductor and capacitor. Figure 2-1, below, shows the main structure of a series

resonant DC-DC converter. One of the benefit of this topology is the presence of the resonant capacitor (C_r) on the primary side of the transformer that can block any DC component. This is particularly beneficial to help keep the transformer from saturating and/or being a safety concern in the event the switching device fails short. By the same token, one might consider the presence of capacitor in series a disadvantage due to the high current requirement on the resonant capacitor. An SLR operates in a current source mode, where a transformer might be needed if the desire output voltage has higher magnitude than the input.

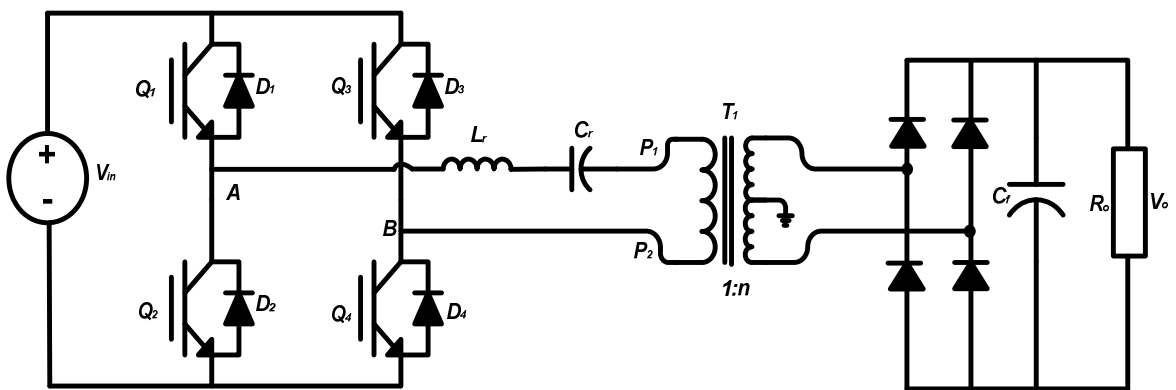


Figure 2-1: Series Resonant DC-DC converter Schematic

Assuming very large output filter capacitor (C_f), one can expect a ripple free DC voltage on the output. Considering transformer ratio of 1:1, the reflected voltage on the primary side of the transformer becomes (V_o) when inductor current is positive and it will become ($-V_o$) when inductor current is negative. Based on these assumptions, a simplified equivalent circuit of the above full-bridge series resonance converter can be represented as shown below in Figure 2-2.

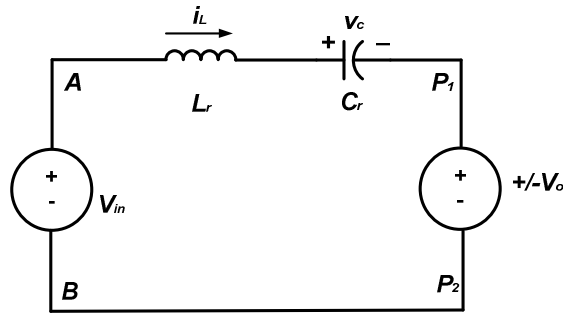


Figure 2-2: Series Resonant Converter Equivalent Circuit

The main characteristic of Full-bridge topology is the utilization of full input voltage. In a typical frequency based controller when i_L is positive, it flows through Q_1 and Q_4 if they are both on; otherwise, D_2 and D_3 will be conducting. During the negative cycle, where i_L is negative, the current flows through Q_3 and Q_2 if they are both on; otherwise, D_1 and D_4 will be conducting. Moreover when evaluating the waveform of the mentioned topology, there are three possible mode of operation that are specific to the ratio of the switching frequency with respect to the resonance frequency of the system. The derivation of the output waveform for basic undamped series-resonance can be found in the Appendix A.1. Equation A-5 shows the relationship between the resonance tank and its resonance frequency.

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{L_r C_r}} \quad (2.1)$$

2.1.2 Discontinuous Model

Discontinuous mode operation is when $\omega_s < \frac{1}{2}\omega_o$. The name refers to the discontinuity of the inductance current, which is also known as DCM mode. The DCM

mode benefit from lower switching frequency, and better control over no-load condition, by adjusting the off period. Another advantage of DCM is the natural commutation of all switching devices resulting in Zero-Current Switching (ZCS). This will have significant improvement in reducing stress on switching devices.

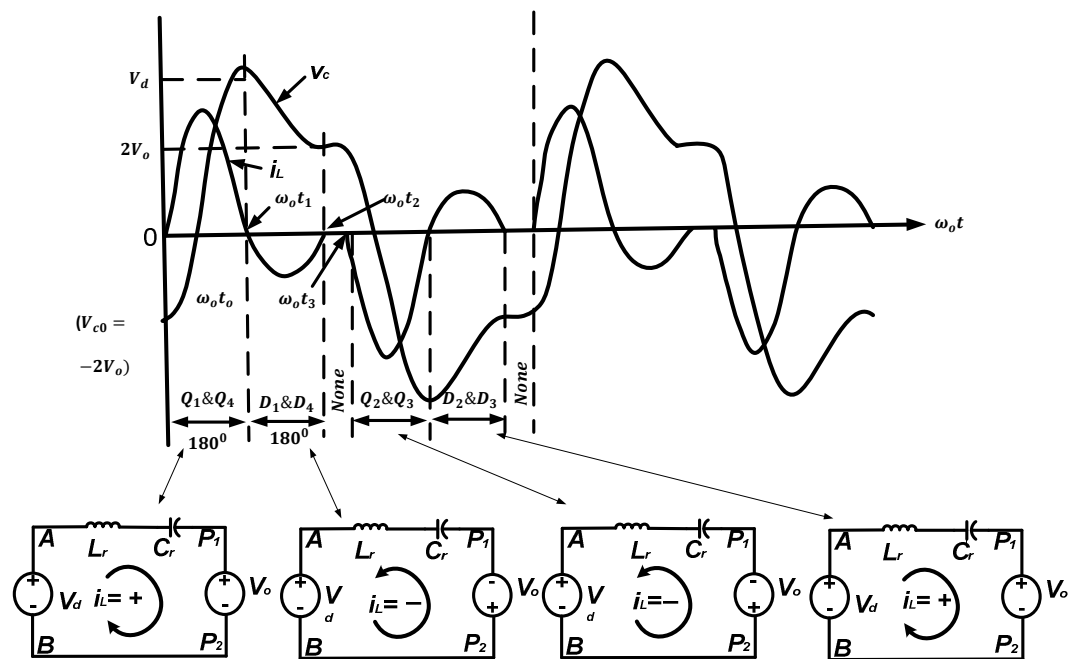


Figure 2-3: Discontinuous-conduction mode of operation for SLR [11]

2.1.2 Sub-Resonance Continuous Model

Sub-Resonance Continuous mode refers to the operation mode when the switching frequency is more than half of the resonance frequency, and less than the resonant frequency, i.e. when $\frac{1}{2}\omega_0 < \omega_s < \omega_0$. During this mode of operation, the transition to the opposite pair of switching devices happen at a finite current resulting in a

continuous inductance of AC current, as well as, turns on loss and diode recovery. However; the turn off happen naturally at Zero-current resulting in ZCS. This phenomental is also shown in the DCM where the voltage lags current due to the more capacitive nature of the operation. The CCM allow for higher power conversion than the DCM mode.

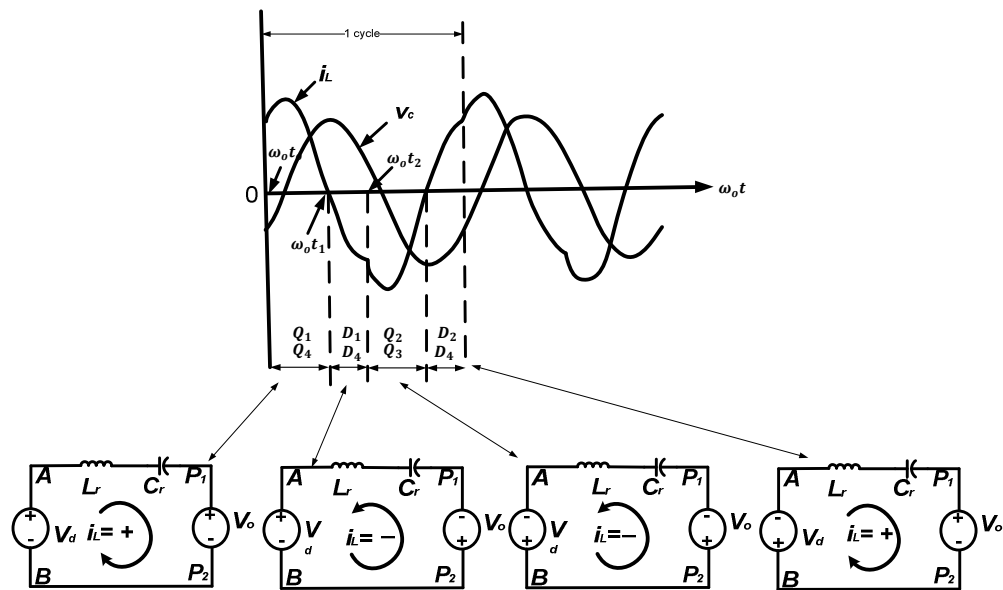


Figure 2-4: Sub-Resonance CCM operation for SLR [11]

2.1.2 Super-Resonance Continuous Model

Super-Resonance continuous current mode refers to the operation mode when the switching frequency is more than the resonance frequency, where $\omega_o < \omega_s$. Super-resonance mode is more inductive, and unlike the sub-resonance CCM or DCM, the current lags voltage, which result in no turn on loss due to ZCS. Another advantage of operating in this mode is the absence of diode recovery. This can be seen from the waveform below where the diode turn's off at zero-current. However; the switching still

have to turn on at current and voltage, and for that reason several techniques have been developed to minimize turn off loss.

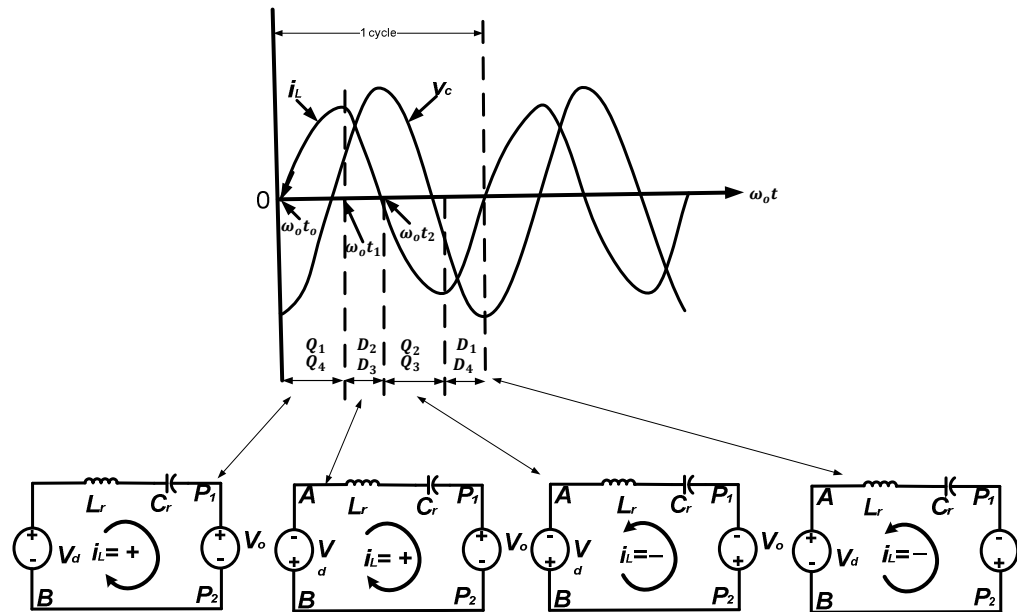


Figure 2-5: Super-Resonance CCM of operation for SLR [11]

2.2 Parallel-Loaded Resonant Converter

Parallel-Loaded Resonant Converter (PLR) is similar to the SLR in terms of operation, which employs a series-resonant LC tank circuit, except that the resonance capacitor (C_r) appears in parallel with the load [11]. As a result, the PLR converter operates as a voltage source, and would require a filter inductor (L_f) on the output after the diode bridges. One of the advantages of this topology is that, unlike SLR topology, PLR is able to step up or down the output voltage without the use of transformers. In addition, voltage source operation is suitable when multiple output voltage is required.

One shortcoming of the PLR topology, in comparison to SLR, is the lack of short circuit protection due to the resonant capacitor location.

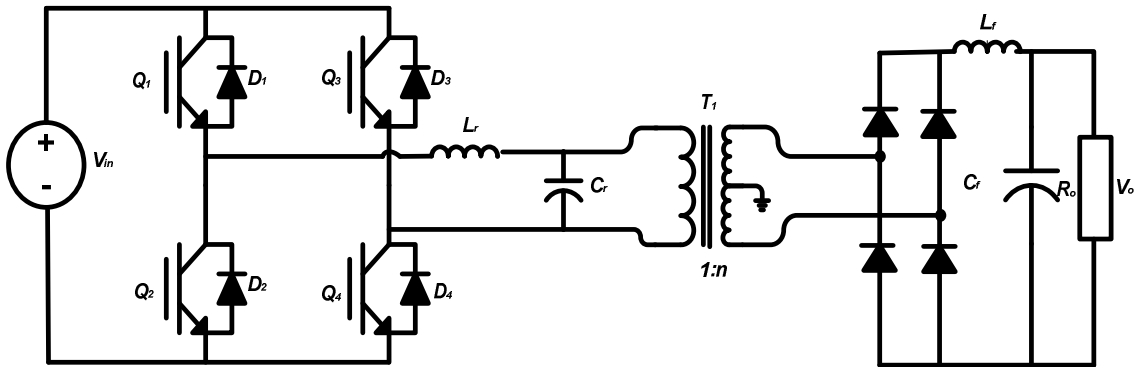


Figure 2-6: Parallel-Loaded resonant DC-DC converter [11]

Assuming a large output capacitor and inductor ripple free output DC current, (I_o) can be considered to develop an equivalent circuit. Similar to the SLR topology (mentioned above) the transformer is considered to be an ideal transformer with 1:1 turn ratio. Figure 2-7 (below) shows the equivalent circuit based on these assumptions. Unlike SLR, where the load is in series with the resonance tank, the PLR equivalent circuit shows parallel loaded capacitor.

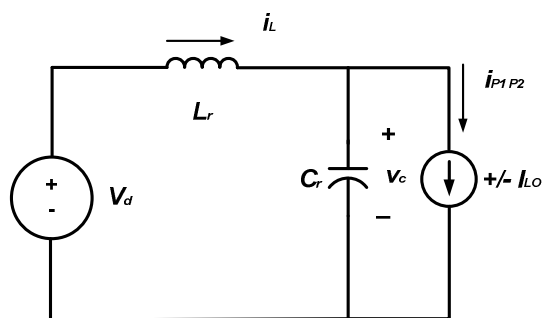


Figure 2-7: Series resonant converter with Parallel-Load equivalent circuit

Similar to the previous section, the relationship of the three modes of operation and the switching frequency will be discussed further.

2.1.2 Discontinuous Model

Similar to SLR discontinuous mode, PLR DCM has operating frequency of $\omega_s < \frac{1}{2} \omega_o$. One of the characteristics that are specific to the PLR DCM mode is that, unlike SLR DCM where only the current goes to discontinuous mode, both current and voltage briefly goes to discontinuous mode. This characteristic not only creates initial conditions that are consistent at every half-cycle, but also results in on turn on or off loss in either the switching device or diodes. Using an equation from Appendix A.2, the waveforms in Figure 2-8 demonstrates the state-state operation of the PLR DCM converter.

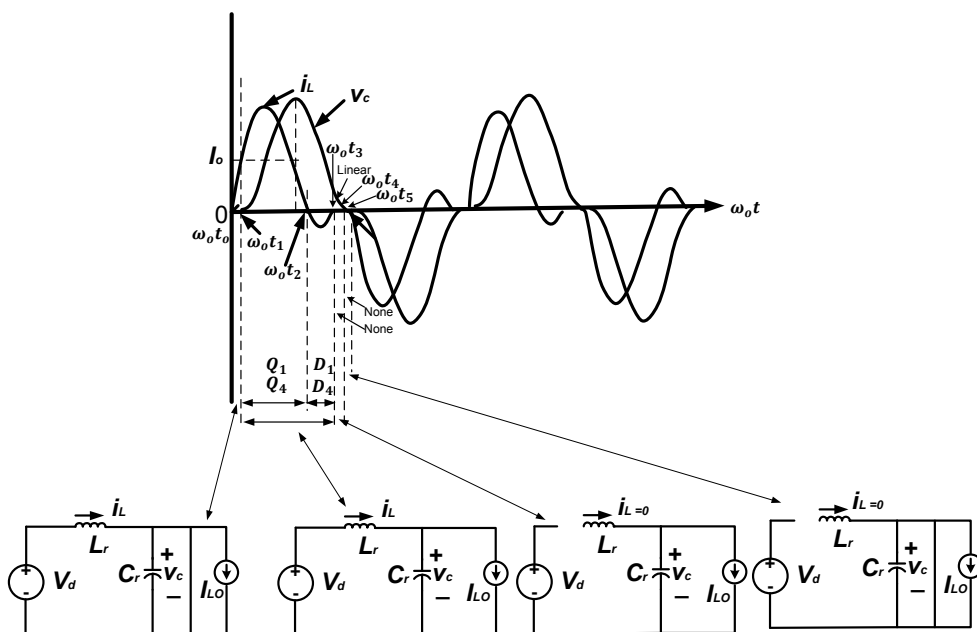


Figure 2-8: PLD DC-DC converter in discontinuous mode

From Figure 2-8, one will notice a rather peculiar state when $I_o > i_L$ during start-up. Essentially, all output diode becomes forward bias creating what appears to be a short circuit on the resonant capacitor (C_r) keeping it at zero voltage. Similar to other DCM mode, no-load operating condition can be easily achieved by adjusting the state where both the current and voltage are at Zero.

2.1.2 Sub-Resonance Continuous Model

Sub-resonance PLR continuous conduction mode (CCM) refers to the operating frequency between the resonance and half of the resonance frequency i.e. $\frac{1}{2}\omega_o < \omega_s < \omega_o$. While operating at the same condition, the sub-resonance PLR CCM and SLR are similar, when it comes to their advantages and shortcomings. Figure 2-9 demonstrates the steady-state waveform for this mode of operation. It can be seen from the waveforms that the switch turned on at finite voltage and current, and diode turn off at finite voltage and current. However, there is no turn off loss on the switch, which is consistent with more capacitive circuit where the voltage lags the current.

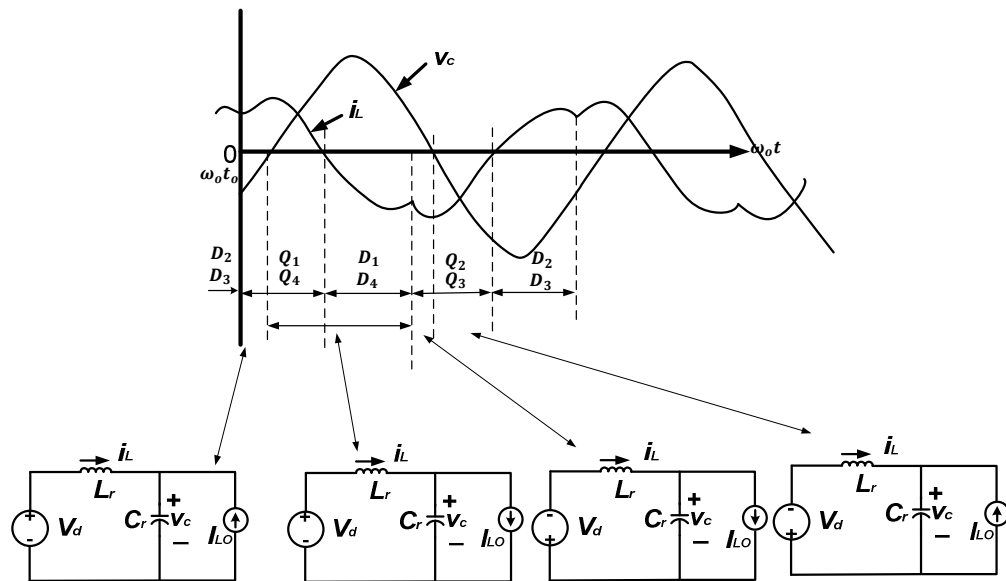


Figure 2-9: Sub-Resonance PLD DC-DC converter in CCM

2.1.2 Super-Resonance Continuous Model

Similar to what was previously stated for SLR, Super-Resonance continuous current mode refers to the mode operation where the switching frequency operates above resonance frequency or angular frequency, i.e. $\omega_o < \omega_s$. Super-resonance CCM mode of this PLR converter operates a lot like the SLR converter under similar operating points. Hence, similar behavior such as being more inductive, where the current lag the voltage, can be seen. This result in a no turn on loss on the switch, but the switch had to be turned off at finite voltage and current. Similar technique regarding the use of snubber capacitor can be employed for turn off loss reduction.

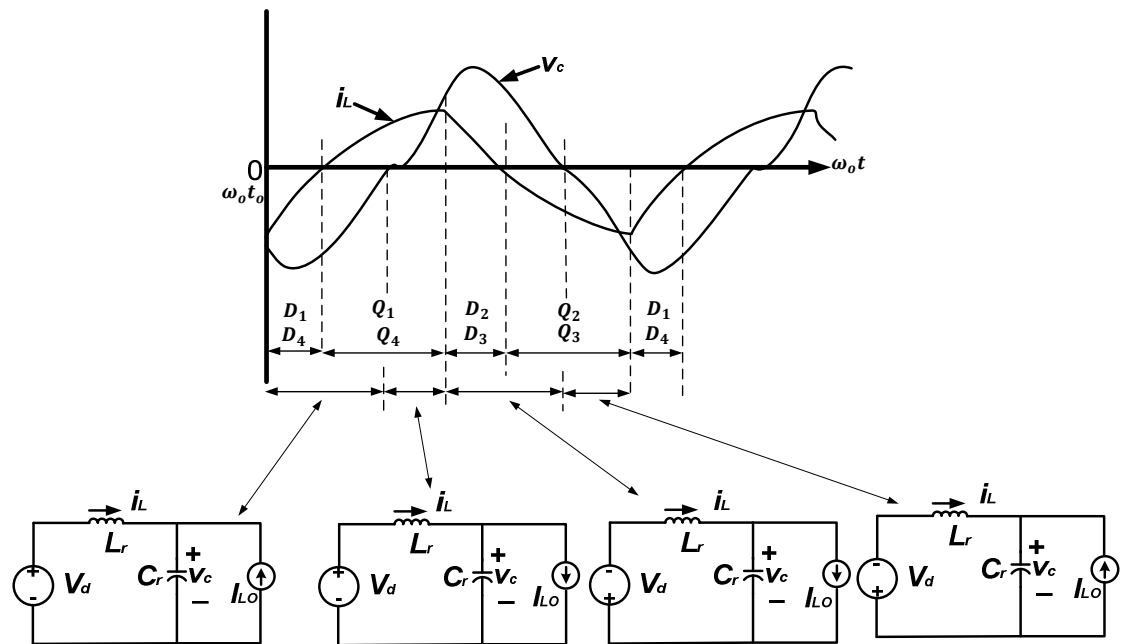


Figure 2-10: Super-Resonance PLD DC-DC converter in continuous mode

2.3 Thesis Research motivation

The main objective of this research thesis is to produce feasible topology for CT High Frequency Power Distribution Unit (HFPDU). There are several requirements for the new HFPDU, such as: (1) size reduction, (2) cost effective, (3) meet EMC requirement, (4) operate in wide load, and (5) low leakage current are just some to name a few. This research will identify the best topology that can meet all critical to quality specification for the HFPDU.

Section 2.1 and 2.2 discussed the operational principle of SLR and PLR converters. Also, the sections highlighted the advantages and shortcomings of this topology, as well as, presenting the different operating points. This leads us to a topology

that may offer the best of both worlds; by integrating SLR and PLR to form an LLC based series-parallel converter operating in super-resonance CCM mode.

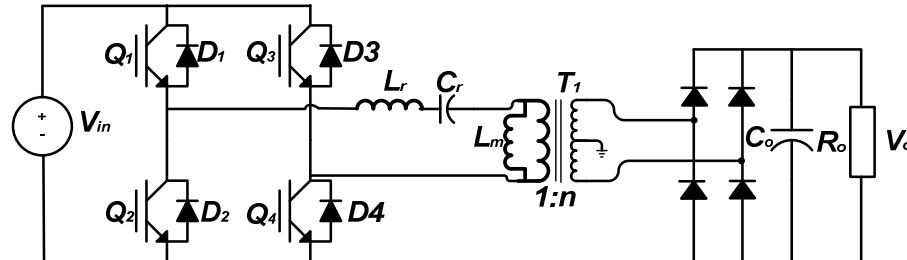


Figure 2-11: LLC Resonance Converter

LLC resonant is the most attractive option as switch's and rectifier diodes operates in ZVS. ZCS operating conditions are guaranteed over the entire operation range, dramatically reducing switching losses while improving EMI performance [5]. In addition, higher frequency operation allows for size advantage on the high frequency isolation transformer. The selected resonance topology will be further investigated for its merit and use in the CT HFPDU architecture.

CHAPTER III

3. LLC RESONANT CONVERTER FOR HFPDU

LLC resonant converters that are operated above the resonant frequency shows many advantages including, but not limited to inherent short-circuit protection, zero-voltage commutations, limited harmonics in the resonant current, maximum power transfer at minimum switching frequency, transformer leakage inductance included in the resonant link. [9] As a result, this thesis selects a series-parallel loaded resonance converter to implement for the CT High Frequency PDU. The proposed topology is expected to operate at a range of 100W of preload to 150kW of load. Moreover, the input voltage for the converter could vary by +/-30%. This presents a challenge to the topology because it requires have enough gains to operate across the full power range down to low or no-load condition. This will be further evaluated through the use of a phase-shift switching methodology.

Figure 3-1 shows the high level topology on the CT HFPDU, which takes in three-phase 480VAC. It includes AC line filters, three-phase full-bridge rectifier, and soft-start circuitry that create DC bus voltage for the H-bridge. For the sake of simplicity, the analysis begins with a DC voltage source and does not consider the effects from the input diode rectification. In contrast, the transformer used in the HFPDU will be further expanded to show the full characteristic since it is an integral part of the resonance circuitry.

A prototype was also developed, and results of the experiments performed are included in this paper. In building the prototype, PowerEx CM600DU-24NFH IGBTs was selected. This IGBT is capable of switching at up to 70 kHz during Soft-switching or at 30 kHz if the IGBTs are expected to operate in hard-switching mode. As previously mentioned, one of the shortcomings of the topology is the high current rating requirement on the resonant capacitor. And for that reason, a 4 μF AVX capacitor with 600 A rms current rating was selected. The output stage consists of high frequency rated capacitor together with few bulk capacitors, and a fast acting diode-bridge. Further discussion on the prototype and experimental will be presented at a later section in the paper.

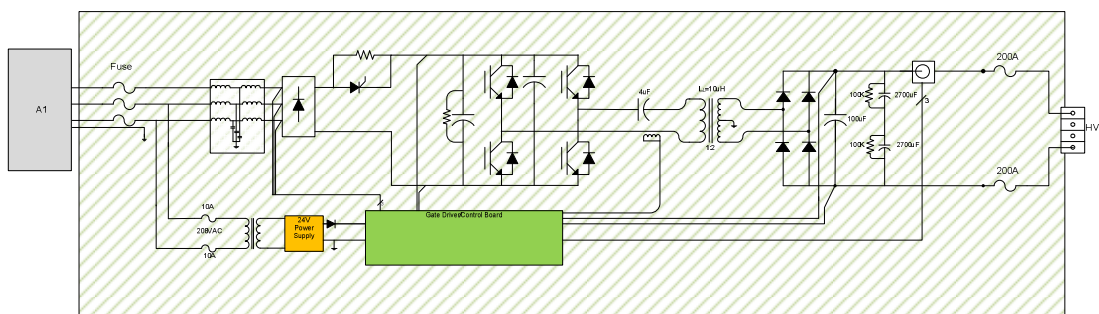


Figure 3-1: Topology of the proposed CT High Frequency Power Distribution Unit.

3.1 Equivalent Model Analysis

The resonant network results in the filtering of the square wave voltage output from the full-bridge converter, which results in sinusoidal current on the primary side of the transformer. From practicality stance, the LLC converter can be said to operate at or close to the series resonance frequency, and all higher order harmonic can be ignored for

calculating the transfer ratio. These assumptions allow for the use of first harmonic approximation (FHA) method.

The HF-PDU DC-DC converter section can be simplified into the circuit shown in Figure 3-2, where R_{AC} represent the output load and transformer turn ratio. Thus, the AC equivalent load resistance R_{AC} can be expressed as:

$$R_{ac} = \frac{8n^2}{\pi^2} R_o \quad (3.1)$$

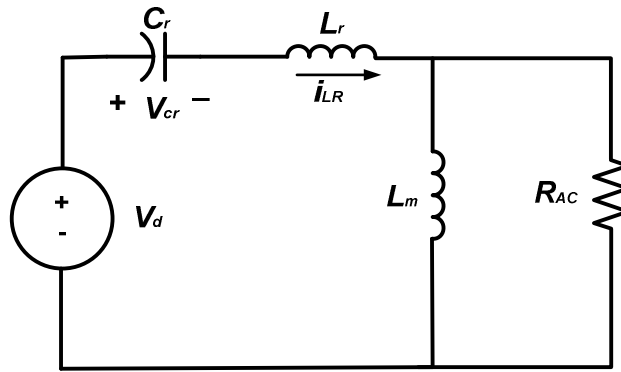


Figure 3-2: Equivalent circuit for the HFPDU DC-DC selected topology.

The input-output transfer ratio of the converter can be easily calculated from

$$M_g = \left| \frac{sL_m || R_{ac}}{sL_r + (sC_r)^{-1} + sL_m || R_{ac}} \right| \quad (3.2)$$

Eq. (3.2), and can be transferred to frequency domain by the equivalence of $s = j\omega$ as [7]

$$M_g = \left| \frac{j\omega L_m || R_{ac}}{(j\omega L_m) || R_{ac} + j\omega L_r + \frac{1}{j\omega C_r}} \right| \cong \frac{V_{Lm}}{V_{in}} \quad (3.3)$$

Where $j = \sqrt{-1}$

Based on equation (3.3), a relationship can be established between the input and the output voltage using the gain of the system and any transformer turn ratio.

$$V_o = M_g x \frac{1}{n} x V_{in} \quad (3.4)$$

In order to evaluate the DC gain characteristic of the LLC resonance converter under various load conditions, equation (3.3) is expressed in a normalized format for better readability. Starting from the operating frequency, the series resonance frequency (f_{r1}) can be used for normalization.

$$f_n = \frac{f_{sw}}{f_{r1}} \quad (3.5)$$

Where $f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}}$,

What is also true about LLC resonance converter is the presence of second resonance (f_{r2}) frequency that is the result of the combined inductances. The definition of (f_{r2}) is shown in equation (3.6), and the effect can be seen in figure 3-3.

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r+L_m)C_r}} \quad (3.6)$$

Furthermore, in order to combine two inductances into one, an inductance ratio can be defined as

$$L_n = \frac{L_m}{L_r} \quad (3.7)$$

The quality factor of the series resonant circuit is defined as

$$Q_{ac} = \frac{\sqrt{L_r/C_r}}{R_{AC}} \quad (3.8)$$

Notice that f_n , L_n , and Q_{ac} are no-unit variables. With the help of these definitions, the voltage gain function can then be normalized and expressed as:

$$M_g = \left| \frac{L_n x f_n^2}{[(L_n + 1) x f_n^2 - 1] + j[(f_n^2 - 1) x f_n x Q_{AC} x L_N]} \right| \quad (3.9)$$

Using equations (3.4) and (3.9), the relationship between the input and the output voltage is:

$$V_o = M_g(f_n, L_n, Q_{AC}) x \frac{1}{n} x V_{in} \quad (3.10)$$

The equivalent circuitry of the topology shown in Figure 3-2 and equation (3.9) form the basis for the design method and operating mechanism. In order to understand the design behavior, a plot of the voltage gain across the switching frequency at a different quality factors (Q_{AC}) is indispensable.

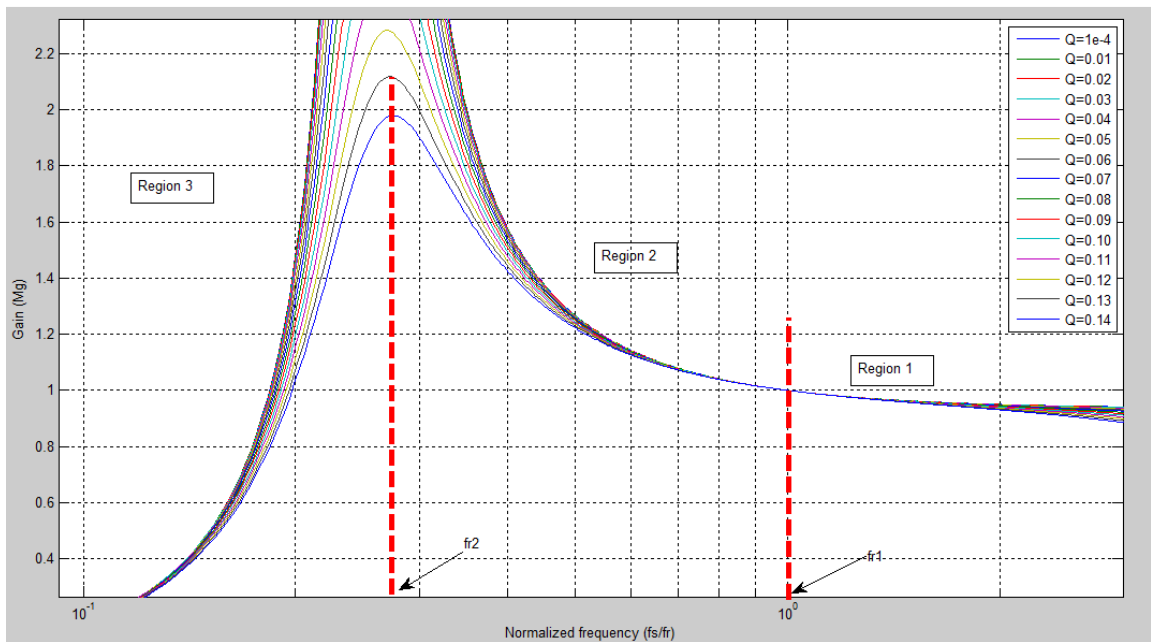


Figure 3-3: Voltage gain vs. normalized frequency for different Q factor.

In figure 3-3, the circuit response depends on the load consumption, which is represented in terms of quality factor (Q). The figure goes from 100 w or a no-load condition to 150kW of output load. As expected in LLC configuration, there are two

resonance frequencies. The first frequency (f_{r1}) is the effect of the series resonance, and the result is a voltage gain of $M_g = 1$, which in essence implies a short circuit. On the other hand, the second resonant (f_{r2}) is the combined effect of the two inductances together with the resonant capacitor. In the above figure (L_n), which is the ratio of the magnetizing inductance and resonance inductance represented in equation (3.7), stayed fixed. With constant L_r and C_r , a decrease in L_m would increase the reactive current in the switching devices that results in increased losses, while improving the gain margin in region 1 of Figure 3-3, as well as, moving the second resonance frequency (f_{r2}) more to the left.

Figure 3-3 shows three different operating regions across the frequency spectrum. The super-resonance region, which is labeled as region 1, operates at zero-voltage switching (ZVS) conditions. In this mode, the magnetizing inductance has minimum effect in terms of acting as a resonant. In fact, for the purposes of this research, the intended use of the magnetizing inductance is to maintain ZVS in phase-shift switching. The area between f_{r1} and f_{r2} , or Region 2, on the other hand shows significant effect as a result of changes in output load. This means that ZVS or ZCS operating condition would be dependent on the output load. Finally, in region 3, the converter goes to fully discontinuous conduction mode resulting in a ZCS mode of operation.

In any case, the focus for this research is operation at super-resonance and, looking at Figure 3-3, it can be seen that at light load the resonance circuit would need to switch above 100 kHz to maintain gain margin. In addition, the input voltage is allowed to vary by +/-30%. In order to maintain regulation and avoid going to frequency that exceed the device rating, a phase-shift modulation techniques have been proposed. This

technique adds phase-shifting competent to the frequency modulation that was initially proposed resulting in better no-load control.

3.2 Operation Principle

Phase-shift and frequency control full-bridge converter operates by turning off one set of the H-bridge leg earlier than the other sets of leg. Essentially, the leading and lagging leg firing signals are shifted. As a result, the excitation square wave can be modulated with three levels (V_i , $-V_i$, and 0). By controlling the shifting angle, the amount of energy sent to the resonant tank is controlled, which reduces the inverter frequency range significantly [14]. This type of operation creates discontinuity in the current every half period, which results in a DCM type of operation at super-resonance frequency. This is a key feature that helps mitigate the shortcoming of maintaining enough gain in a super-resonance to control no-load or low-load condition.

Figure 3-4 shows the theoretical waveform of a full-bridge LLC resonance converter operating in phase-shift control. The operating frequency of the converter is evaluated at super-resonance i.e. $f_{sw} > f_{r1}$. In order to maintain soft switching across the different loads, the converter also adjusts the frequency simultaneously with the change in phase angle. As a result the change in both phase and frequency there would be point of load that would have fewer operating mode than the 8 modes showing in Figure 17. The waveform in Figure 3-4 (a) shows the output voltage from the inverter switching devices (V_{inv}), magnetizing voltage (V_m), and resonant capacitor voltage (V_{cr}). While

Figure 3-4 (b) shows the current in the resonant inductor (i_{Lr}), magnetizing current (i_m), and output current through the diodes (i_d).

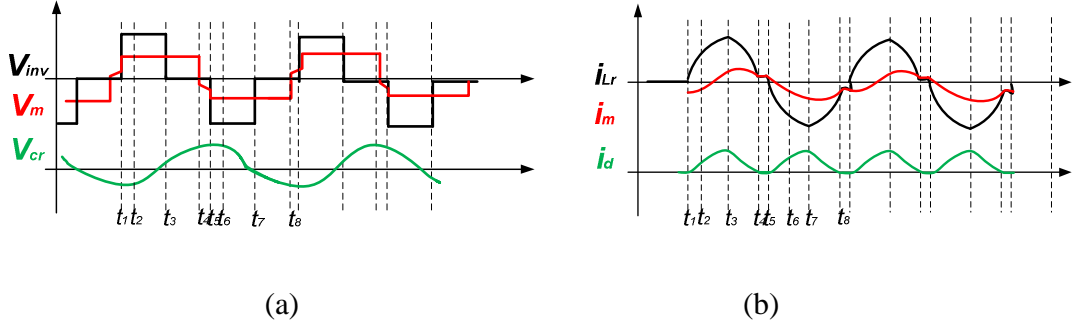


Figure 3-4: Theoretical waveform for phase-shift Operation.

Mode 1: This mode starts with Q_3 and Q_2 turning on. On this mode of operation, i_{Lr} and i_d begins to increase and causes the output voltage to reflect back to the primary side of the transformer. The presence of the output voltage on the magnetizing inductor (L_m), leads to a linear buildup of energy limiting its resonance operation during this period [7].

The equation for both i_{Lr} and v_{cr} is

$$i_{Lr}(t) = i_{Lr}(t_1) \cos(\omega_{r1}(t - t_1)) + (V_{dc} - \frac{1}{n}V_0 - v_{cr}(t_1)) \sqrt{\frac{C_r}{L_r}} \sin(\omega_{r1}(t - t_1)) \quad (3.11)$$

$$v_{cr}(t) = V_{dc} - \frac{V_0}{n} + \left(V_{dc} - \frac{V_0}{n} + v_{cr}(t_1) \right) \cos(\omega_{r1}(t - t_1)) + i_{Lr}(t_3) \sqrt{\frac{L_r}{C_r}} \sin(\omega_{r1}(t - t_1)) \quad (3.12)$$

Where $\omega_m = 1/\sqrt{L_m C_r}$, and $\omega_{r1} = 1/\sqrt{L_r C_r}$

Mode 2: This mode is known as Freewheel state where Q_2 turns off and the resonant current (i_{Lr}) is forced to go through D_1 and Q_3 . This sets the inverter full-bridge output voltage (V_{inv}) to become zero, providing a mode of operation that limits the output power

during low-load. However; the voltage at the magnetizing inductor remains $V_m = -\frac{v_o}{n}$, which would allow the output diode to be forward biased.

$$i_{Lr}(t) = i_{Lr}(t_3) \cos(\omega_{r1}(t - t_3)) + \left(\frac{1}{n}V_0 - V_{dc}\right) \sqrt{\frac{C_r}{L_r}} \sin(\omega_{r1}(t - t_3)) \quad (3.13)$$

$$v_{cr}(t) = -V_{dc} + \frac{V_o}{n} + \left(V_{dc} - \frac{V_o}{n}\right) \cos(\omega_{r1}(t - t_3)) + i_{Lr}(t_3) \sqrt{\frac{L_r}{C_r}} \sin(\omega_{r1}(t - t_3)) \quad (3.14)$$

Mode 2 operation ends when the resonant current (i_{Lr}) becomes equal to the current through the magnetizing inductor (i_m), and ($i_d = 0$) implying that the output diodes are turned off.

Mode 3: During this mode, the output will be separated from the transformer leaving the magnetizing inductor to take part in the resonant circuitry creating an LLC resonant tank [7].

$$i_{Lr}(t) = i_m(t) = i_{Lr}(t_5) \cos(\omega_{r2}(t - t_5)) - V_{cr}(t_5) \sqrt{\frac{C_r}{L_r + L_m}} \sin(\omega_{r2}(t - t_5)) \quad (3.15)$$

$$v_{cr}(t) = v_{cr}(t_5) \cos(\omega_{r2}(t - t_5)) + i_{Lr}(t_5) \sqrt{\frac{L_r + L_m}{C_r}} \sin(\omega_{r2}(t - t_5)) \quad (3.16)$$

Where $\omega_{r2} = \frac{1}{\sqrt{(L_m + L_r)C_r}}$

Mode 4: This mode consist of brief period known as “dead time” were all the switching device are in off state to guarantee safe operation when opposite pair of switching are ready to turn on.

Mode 5, 6, 7 & 8: Basically repeat the same principle that was discussed from *Mode 1* to *Mode 4* only this time the focus would be on Q_1 and Q_4 .

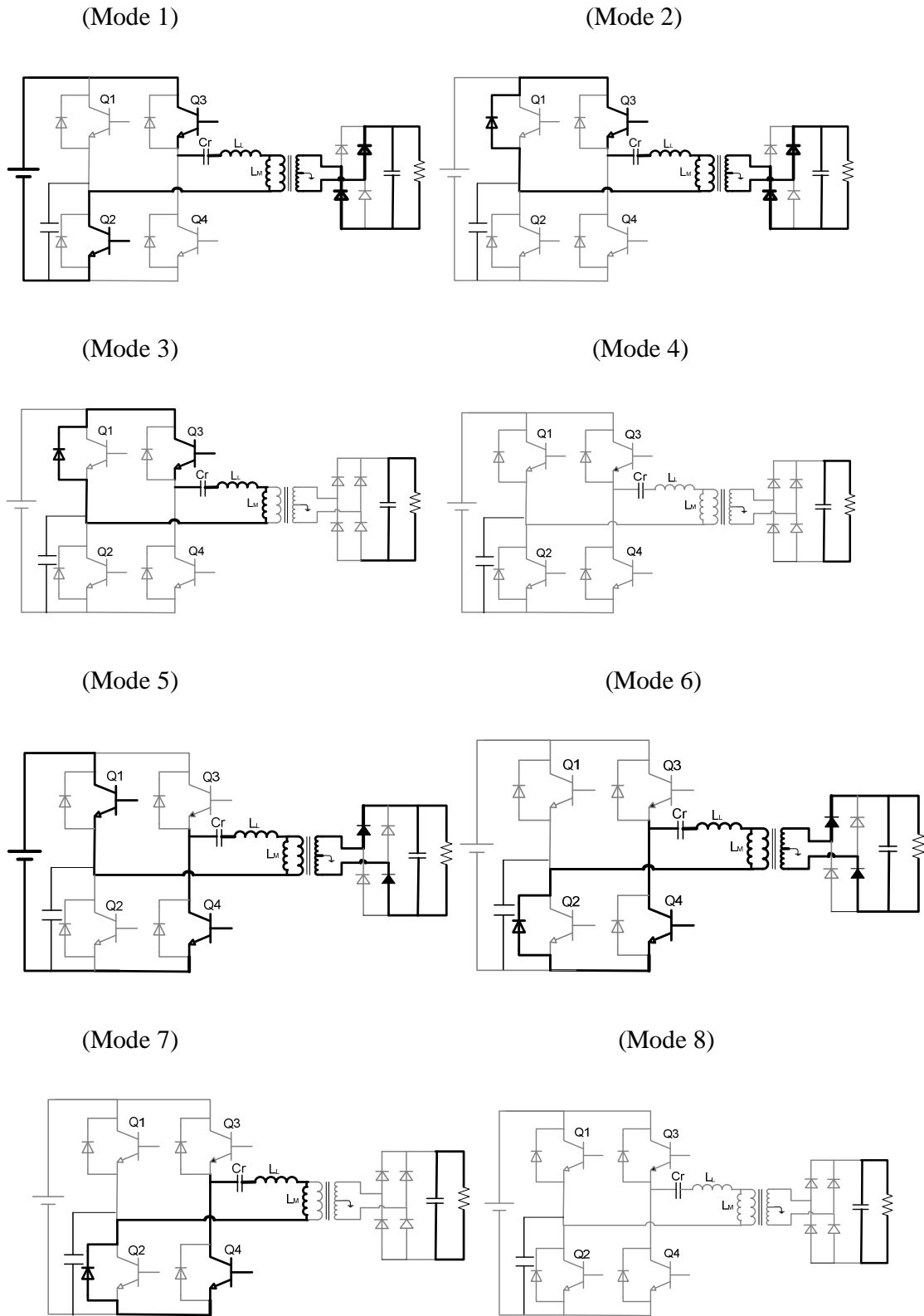


Figure 3-5: Phase-shift operating modes of LLC resonant converter.

3.2 Soft-Switching Techniques

Soft-switching refers to the technique used to minimize the loss or stress on switching devices during turn on or off transition. For instance, when a switch goes from blocking the full voltage to conducting the load current, there will be a finite amount of time where the switch is forced to conduct current at voltage leading to significant loss. Typically, an effective means of mitigation, in a resonant converter, is to remove the energy from the switches to the resonant circuit for a brief period; allowing enough time to let the transition to occur either during zero voltage or zero current switching. For this research, both ZCS and ZVS technique have been employed using what is known as asymmetric snubber circuits.

As previously discussed, operating the full-bridge converter at super-resonance benefit from natural commutation that results in no turn-on losses on the switching devices. This puts the focus on the turn off transition of these IGBTs. To help analyze the asymmetric snubber soft-switching technique, the full-bridge converter will be split into leading and lagging leg. In this case, the leading leg consists of one snubber capacitor between the output of the leading legs and either side of the DC bus. The use of one snubber capacitor for two switches in the leading leg was made possible through the use of superposition theorem, which replaces the DC voltage source with a short circuit for analysis. The result shows the true operation of the circuit that placed the snubber capacitor across both switches on the leading leg. The selection of this snubber capacitor is rather an art that involves the switching frequency, the size of the magnetizing inductance, and the output load.

The method first involve in specifying the maximum operating frequency, and the selected magnetizing inductance. On this case, the calculation would be to find the maximum possible capacitance that can be used at which the time constant for the capacitor discharge is less than the minimum half period at no load. This help limit from having the capacitor being short circuited during turn on.

$$C_{snubber_max} = \frac{1}{L_m(2\pi f)^2} \quad (3.17)$$

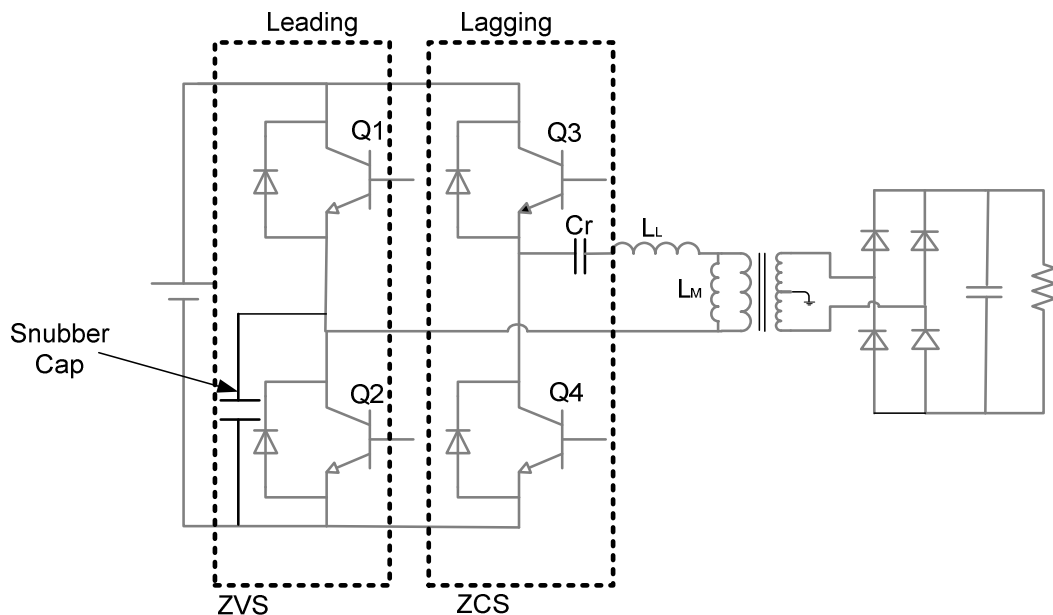


Figure 3-6: Asymmetric snubber soft switching technique.

The result is ZVS on the leading leg, as the snubber capacitor maintain the bus voltage during the turn off transition keeping the potential difference on the switch to zero.

However; the lagging leg benefits from the control varying frequency, which times the turn off transition to be at ZCS across the full load range.

CHAPTER IV

4. ISOLATION TRANSFORMER

One of the main requirements for the CT PDU is to provide galvanic isolation, which is accomplished through the use of an isolation transformer. In fact, the primary function of the current generation PDU is to provide isolation with the use of a bulky 60Hz transformer. Some of the reasons for using a transformer in CT PDU are:

- Achieve voltage step up/down through the use of taps in order to provide the required voltage to the system.
- Provides locally grounded neutral line, which greatly enhances the reliability of sensitive electronics by limiting the potential difference between the neutral and ground.
- Limits ground loop current due to poor infrastructure or multiple power sources.
- Reject stray common mode, DC voltage, and electromagnetic interference from being conducted through the power line.

In general, medical grade isolation transformer falls in strict safety rules. Some of these rules cover the construction process as well as, materials used for insulation, which has direct implication in meeting low leakage current and high isolation voltage requirement.

Figure 4-1 (below) shows the current generation CT PDU transformer. The figure shows that the input or primary is connected in “delta” configuration, while the secondary

side consists of two “wye” configurations, each with three phase power and a center or neutral point.

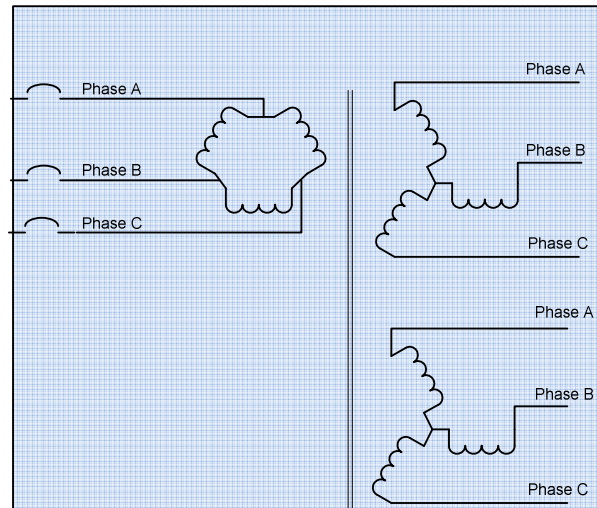


Figure 4-1: Current Generation CT PDU Isolation Transformer.

That being said, the bulky 60Hz transformer, which is currently in operation, was able to meet all performance expectations. However, this transformer not only takes up large footprints, but also uses large amounts of copper and iron with increasing cost trajectory. Therefore, the use of high frequency transformer, which is an integral part of the resonance converter, can significantly reduce the overall size and cost of the transformer.

4.1 High Frequency Transformer

As previously mentioned, the transformer used in the resonance converter is a component that holds key parameters, which dictate the characteristic of the converter. The inclusion of certain parasitic component in the transformer as part of the converter's

design has helped to reduce the part count and, ultimately, save on cost. This is highlighted through the use of the transformer leakage inductance to serve as the resonant inductor, while the magnetizing inductance becomes the parallel inductance in the LLC converter. In further clarification, this section will discuss the design methodology and go over some of the basics for the proper selection of this transformer.

Figure 4-2 (below) shows the major magnetic components that make up the high frequency transformer used in this research. Few items that are not shown in the figure below are:

- Series resistance due to the wire used to construct the transformer winding. This is an important factor when calculating the winding loss, and will have to be considered when determining the wire length and size used in the winding.
- The secondary leakage inductance is not shown in order to simplify the analysis. This was done because the converter only sees the primary side, and the leakage inductance on the secondary has minimal effect on the converter operating point.
- Parasitic capacitance between windings, as well as, between winding and ground. In general, this type of parasitic capacitance has minimum effect on the performance of resonance converter, but might provide common mode noise path to ground creating EMI concern.

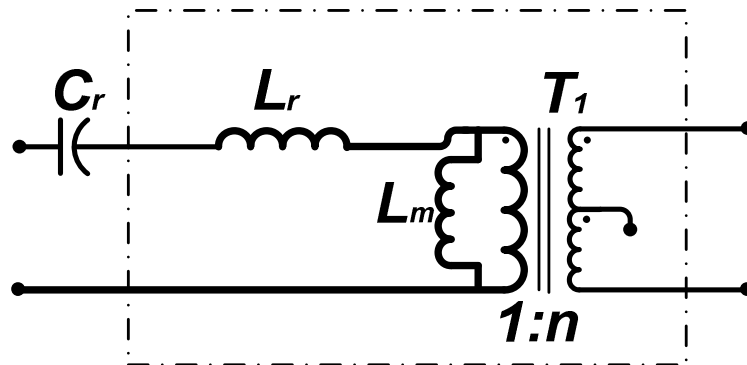


Figure 4-2: High frequency transformer equivalent magnetic component.

Unlike low frequency transformers that use steel lamination as its core material, a high frequency transformer uses ferrites material. This is due to the high eddy current losses due to the steel laminated core. However, for all its advantages in efficiency and size, ferrites come with lower saturation limits that cannot be surpassed at any point. Table 4-1 (below) shows some of the operating points that are used to design the high frequency transformer.

TABLE 4-1: HF TRANSFORMER OPERATING POINT

Item	Rating	Unit
Minimum Input Voltage	380	VAC
Output Voltage	700 +/- 5%	VDC
Max Current	500	A
Minimum Frequency	35	kHz
Nominal Input Voltage	500	VAC
Leakage Inductance	7	uH
Magnetizing Inductance	200-300	uH

4.1.1 High Frequency Transformer Design

Using equation of an ideal transformer, we can calculate the turn ratio (n) that can support an output of 700V from minimum voltage of 380V.

$$n = \frac{N_P}{N_S} = \frac{V_P}{V_S} \quad (4.1)$$

Therefore,

$$n = \frac{380}{700} = 0.54$$

The next important rating in designing high frequency transformer is determining the operating voltage, which is different from the input and output voltage due to the presence of leakage inductance. The especial consideration for this result is because this voltage determines the core size, core material, and number of turns of the transformer. Using value from Table 4-1, the voltage on the leakage inductance can be calculated using equation 4.2.

$$V_L = 2\pi f L_r i_r \quad (4.2)$$

The maximum voltage in the leakage inductance occurs during maximum power, which is when the resonance converter operates at its lowest frequency. The result is:

$$V_L = 2\pi * 35kHz * 7\mu H * 500A = 770V$$

Assuming nominal input voltage of 500V through the transformer, the magnetizing inductance V_m can also be assumed to be at this voltage. Therefore, the transformer operating voltage (V_T) will become the sum of the leakage and magnetizing inductance voltage.

$$V_T = V_m + V_L = 500V + 770V = 1270V$$

The next step is the selection of core material and core shape. This is an iterative process designed to make the best trade-off between the core losses vs., what is typically known as copper loss. Ferrites core comes in different shapes and characteristic. For this research, “U” shaped ferrites from Ferroxcube have been selected. These ferrites will be configured in a “UU” shape, where a set of core would have an effective area ($A_e = 0.00084m^2$). In addition, a ferrite material of “3C94”, which comes with specific core loss characteristic and maximum flux density, has been selected. Based on a review of the datasheet on the maximum flux density, which is $B_{max} = 0.2 T$, for this design a 30% margin was chosen as the new maximum flux density. (Below)

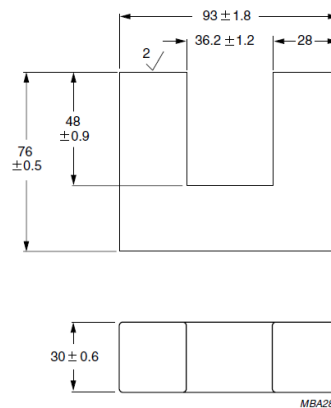


Figure 4-3: Ferroxcube’s U93/76/30 core dimension in mm.

With that in mind, given the size of each core and the intent to minimizing the number of turns, 5 set of core were selected to build the high frequency transformer in a “UU” configuration. This will increase the effective area of the transformer in five fold. Using

equation 4.3, we can calculate the maximum flux density (B_{max}) for a given number of turn on the primary. Another approach is to set a B_{max} , and calculate for minimum number of turns. An integer number of turns with a practical value for building the transformer were picked. As a result the flux density would have to be lower than the set maximum flux density at maximum power. For that reason, $N_p = 14$ was selected to give magnetic flux density of 0.14T using equation 4.3.

$$B_{max} = \frac{\sqrt{2} * V_T}{\omega * N_p * A_e} \quad (4.3)$$

Where

$$B_{max} = \frac{\sqrt{2} * 1270}{2\pi * 35kHz * 14 * (5 * 0.00084m^2)} = 0.138T$$

Based on the turn ratio that was set above, where $n = 0.57$, the number of turns for the secondary side of the transformer will be:

$$N_s = \frac{N_p}{n} = \frac{14}{0.54} = 25.9$$

Thus, setting the number turns to the nearest integer, $N_s = 26$ turns.

From Figure 4-2, we can see the presence of magnetizing inductance. This is set by adding air gap or non-magnetic spacer between the cores. The air gap causes a considerable decrease in the effective relative permeability. However, it produces a more stable effective permeability and reluctance, resulting in a more predictable and stable inductance [10]. The relationship between the air gap and the magnetizing inductance is shown in equation 4.4.

$$L_m = \frac{\mu_0 A_e N_p^2}{l_g} \quad (4.4)$$

Where $\mu_0 = 4\pi \times 10^{-7} \text{NA}^{-2}$ and (l_g) , is the air gap length, where its effective length would be twice the single air gap to account for both leg of the “U” shape ferrite. Using the values from Table 4-1, for maximum of 2mm air gap, where $l_g = 4\text{mm}$, the magnetizing inductance will be;

$$L_m = \frac{4\pi \times 10^{-7} * (5 * 0.00084\text{m}^2) * (14^2)}{0.004\text{m}} = 258.6\mu\text{H}$$

Finally, an important consideration during the designing phase of the high frequency transformer is losses. There are two types of losses that have significant effect on performance. These are core loss and copper loss. Information regarding core loss can be found in the manufacture’s datasheet as a function of peak flux density with frequency as a parameter. Therefore, the core loss of the selected core material can be calculated as follows.

$$P_c = \frac{20\text{kw}}{\text{m}^3} \times V_e = 20\text{kw}/\text{m}^3 * 0.00158\text{m}^3$$

$$P_c = 31.6\text{w}$$

Similarly, the copper losses, as it is commonly known, would be the loss on the wire, which may or may not be made out of copper. Based on the number of turns, and number of core used to construct the transformer, it is easy to calculate the total length of wire used. Once the length and the size of wire have been determined, a nominal RMS current can be used to calculate the losses on the wire. In order to determine the appropriate size of wire to be used in a high frequency transformer, the “skin effect” needs to be kept to a minimum. This is due to the tendency of an AC current to flow on the wire’s surface,

with the increase in frequency creates current crowding. Therefore, in order to fully utilize the wire, the skin depth (ε) needs to be calculated.

$$\varepsilon = \frac{0.0662}{\sqrt{f}} [m] \quad [1] \quad (4.5)$$

Where (ε) is defined as the distance below the surface, and the current density has fallen to 37 percent of its value at the surface [10]. Therefore, using equation 4.5, the skin depth for our maximum operating frequency, $f = 60kHz$ would be:

$$\varepsilon = \frac{0.0662}{\sqrt{60kHz}} = 2.7e^{-4} [m]$$

Therefore, a radius of equals to $\varepsilon = 2.7e^{-4}m$ would approximate the wire size of 30 AWG. Based on industry recommendation and additional consideration for design margin, 38 AWG size of wire was selected. Next step would be to determine the number of strands of 38 AWG wire needed to have in order to carry the full current without an excessive copper loss. With the intention of keeping the copper loss to no more than 3x of the core loss, or <100w of loss, a 4 AWG equivalent litz wire is assembled using approximately 2,625 number of strands. From the manufacturing datasheet, a 4 AWG equivalent litz using 38 AWG strands of wire have dc resistance of $R = 0.928\Omega/1000m$. The approximate required length of wire needed on the primary side of the transformer, based on the number of turn and core used is ~4.9m.

Therefore, the copper loss on the wire is:

$$P_w = \left(\frac{0.928\Omega}{1000m} \right) 4.9m * (150^2) = 102 W$$

However, for ease of manufacturing the transformer and a tighter control over the leakage inductance, two 8 AWG litz wire in parallel have been selected to replace the 4 AWG litz wire of the primary side of the transformer. With almost double the number of turns on the secondary, use of one 8 AWG litz wire could result in a similar performance as the primary side.

4.2 Transformer Simulation Analysis

Following the different design iterations, and calculations of section 4.1.1, the final specification of the high frequency transformer has been developed.

TABLE 4-2: HF TRANSFORMER SPECIFICATION

Item	Rating	Unit
Primary Turns	14	Turns
Secondary Turns	26	Turns
Primary winding	2x8	AWG
Secondary winding	1x8	AWG
Gap	2	Mm
Leakage Inductance	7	uH
Magnetizing Inductance	200-300	uH

Using the specifications in Table 4-2, a model of the high frequency transformer was developed using Ansoft® software tool. A 2mm spacer material was also been added to develop the expected leakage inductance result.

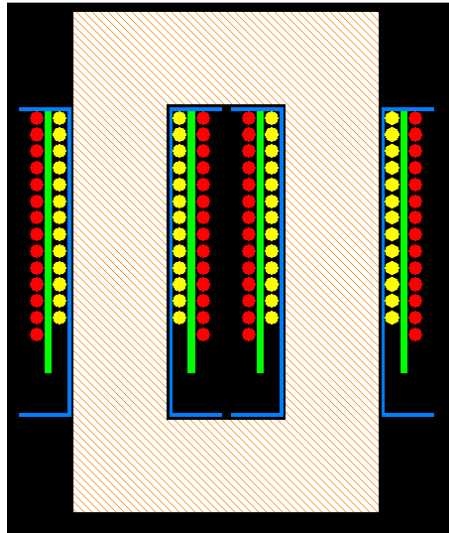


Figure 4-4: Ansoft high frequency transformer model using “UU” shape ferrites.

Simulation of the model was also done using PExpert® software, in order to compare the result with the expected value. Figure 4-5, shows a simulation of the magnetic flux density, which showed $B_{max} = 0.1371 T$. Similar result was found during calculation of B_{max} using equation 4.3 above.

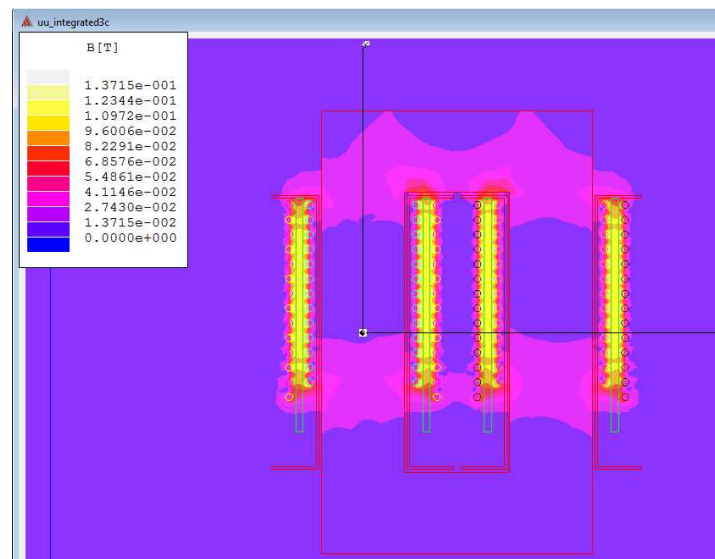


Figure 4-5: Magnetic field density model in high frequency transformer.

CHAPTER V

5. CONTROL ARCHITECTURE

One of the main requirements that initiated this research is the need for a regulated output voltage. Therefore, regardless of the topology or operating mode chosen, the high frequency power distribution unit needs to guarantee a regulated output voltage. This includes maintaining a specification of 700VDC +/-5% across the full output load range including 100 kW step load.

TABLE 5-1: HIGH FREQUENCY PDU SPECIFICATION

Item	Rating	Unit
Input Voltage	600 +/-30%	VDC
Output Voltage (including transit)	700 +/- 5%	VDC
Average Output Power	15	kW
Peak Output Power	150	kW
Minimum Output Power	100	W

5.1 HFPDU Control Scheme

The high frequency PDU controller is a classical voltage-current cascaded loop, where the error from the output voltage loop becomes a virtual current reference. The two loop concept shown in Figure 5-1 works by correcting the output voltage by way of adjusting the resonant current using proportional and integral (PI) controller. Since the current experiences less delay than the voltage, the two-loop approach tends to have better dynamics than voltage-mode control alone. [12] In addition, due to the extremely high step load requirement, output load current has been used to create a feed-forward

signal to improve HFPDU transient response. Reason being, the additional output current information gives early update on the output load before the effect is shown in the voltage feedback.

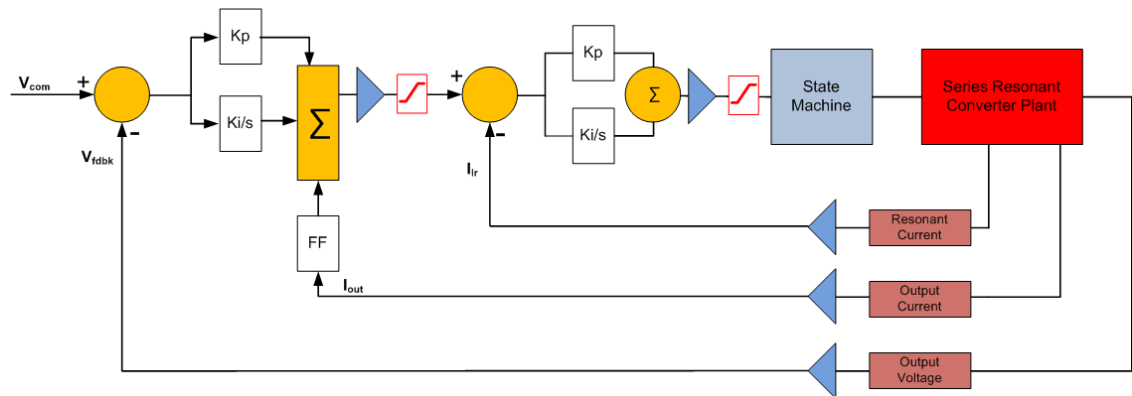


Figure 5-1: HFPDU control scheme using cascaded two-loop control.

5.2 HFPDU Control Modeling

Matlab/Simulink model was developed based on the above mentioned control scheme together with the LLC resonance converter that was discussed in Chapter III. Small output pre-load together with a switch controlled 135 kW resistive step load were used for simulation.

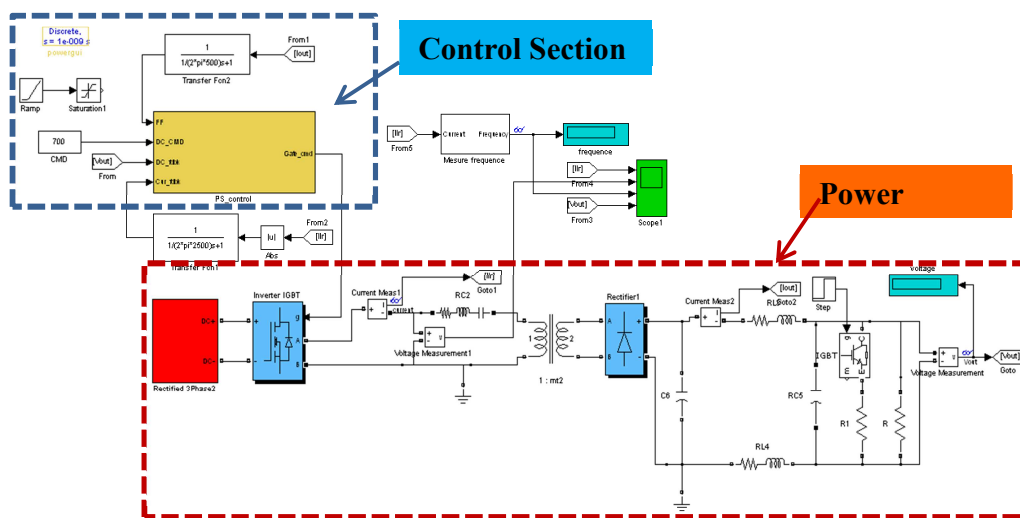


Figure 5-2: HFPDU Matlab/SIMULINK model of LLC topology and controller.

Figure 5-2 (below) shows the start-up waveform of the HFPDU. High gain is expected during start-up, due to the high voltage difference between the output and the input DC volt. Therefore, in order to provide soft start function, a controlled ramp has been incorporated in the input command. As a result, a good controlled ramp to the output voltage is shown in the figure below, followed by a controlled resonant current and inverter PWM voltage, respectively.

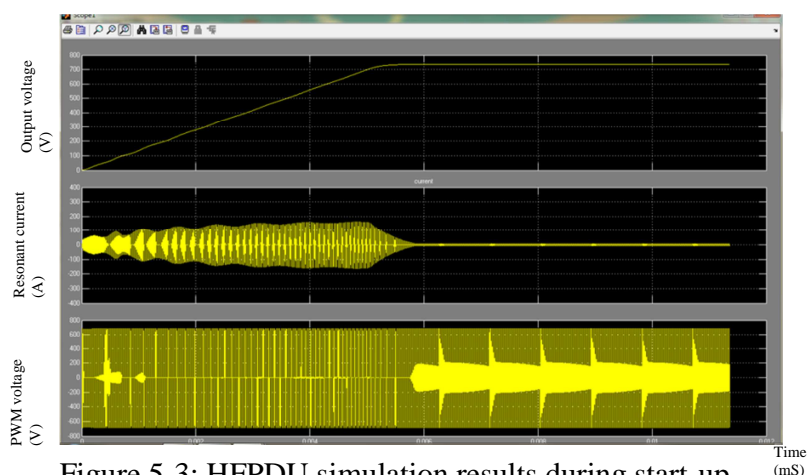


Figure 5-3: HFPDU simulation results during start-up.

Another important performance specification is transient response of output voltage. Figure 5-4 shows a converter starting from steady state running with an output load of 15 kW, and followed by additional 135 kW step load using only 2500 uF capacitor on the output. The waveform shows 2.1 % of its 700 VDC, and 2.2% over shoot when the 135kW load is finally removed, which is well within the expected specification of less than 5% regulation.

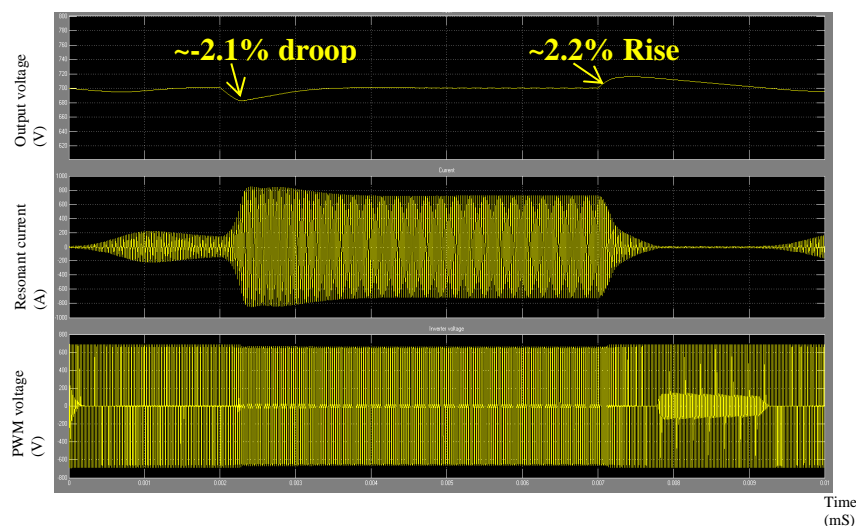


Figure 5-4: HFPDU Transient Response to 135kW step load.

5.3 Monte Carlo Analysis

On this section, Monte Carlo simulations were done to consider variation within components and disturbance to the resonance converter, while still guaranteeing performance. For this simulation, a Matlab script was develop to alter major component values and compute different combination of the adjusted disturbance. Finally, the results were aggregated to show the effect of the adjusted domain.

TABLE 5-2: SPEC FOR INPUT DOMAIN WITH DEGREE OF FREEDOM

Item	Value	Degree of Freedom	Unit
Input Voltage	600	+/-30%	VDC
Leakage Inductance	7	+/- 14%	uH
Resonant Capacitor	4	+/-10%	uF
Output Capacitor	10,000	-/+10%	uF

The items from Table 5-2 were set to vary within their degree of freedom, and a total of 81 different combinations of runs were performed. Figure 5-5 shows step load of 135kW, while the converter were at a steady state with the output loaded at 15kW. After completing the 81 runs, the maximum measured percentage droop values were aggregated, and 2.2% was determined as the maximum droop value.

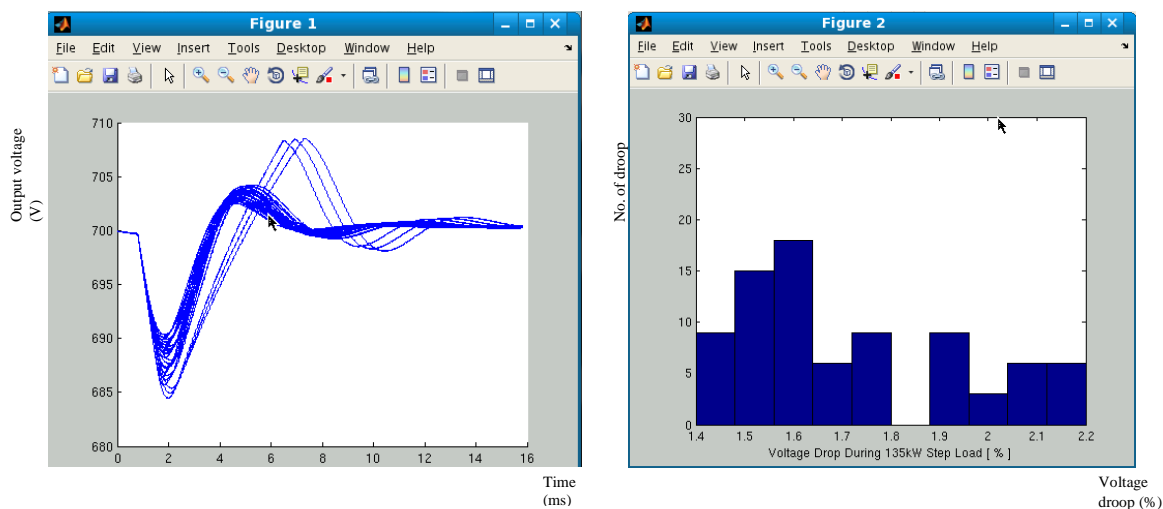


Figure 5-5: Monte Carlo Analysis of HF PDU Transient Response when 135 kW load were added, and droop measurement in percentage.

Similarly, once the converter is at steady state with the output loaded at 150kW load, any sudden removal of the load will result in some transient response. Using values from

Table 5-2, similar Monte Carlo result shows in Figure 5-6, the max rise on the output voltage was less than 2%.

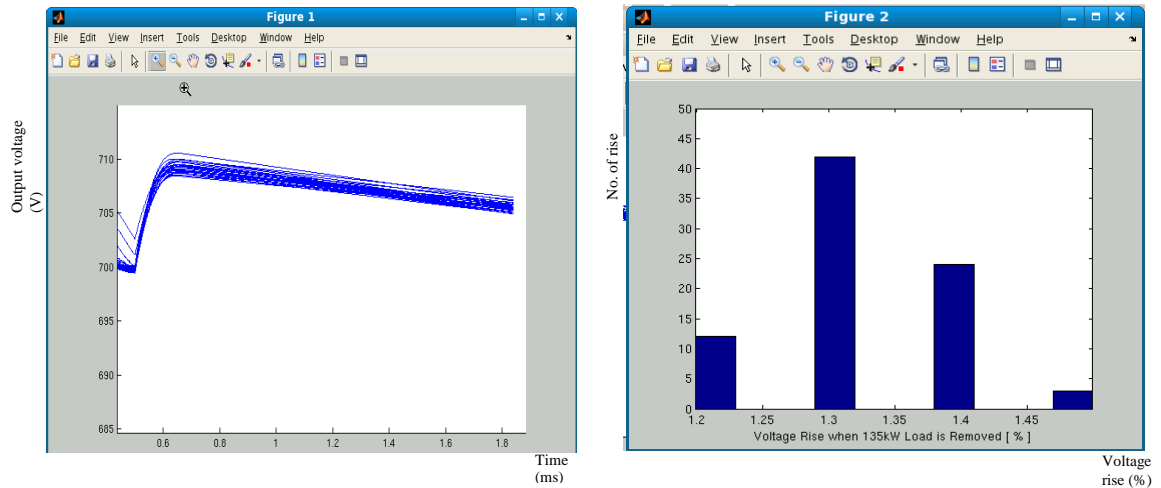


Figure 5-6: Monte Carlo Analysis of HF PDU Transient Response when 135kW load is removed and voltage rise measurement in percentage.

CHAPTER VI

6. THERMAL ANALYSIS

Thermal analysis is a fundamental issue in power converter design, since it is instrumental in determining the most convenient switching power device. The associated heatsink and choice of cooling method are strictly related to the basic requirement for keeping the junction temperature below the maximum admissible value [6]. In this chapter, we will identify the converter's source of losses, and discuss the simulation of the thermal performance for the selected heatsink.

6.1 Loss Calculations

There are primarily two sources of losses on the IGBT's used for the resonance converter. They are classified as switching losses and conduction losses. In setting up the experiment for thermal analysis of the converter, a single heatsink with a size of 150 mm x 380 mm was selected. The heatsink will be shared by two IGBT modules, with each consisting of 2 IGBTs, and two diode modules, which also consist of 2 diodes each.

As previously discussed, the selected LLC resonance converter will not have any turn on loss due to super-resonance operation. However, there will be some turn off losses. The section on softstart operation shows techniques for reducing or eliminating these turn off loss. Manufacturer of IGBTs or similar devices provides an energy turn on and turn off

estimate loss for corresponding current. Figure 6-1 shows both the turn on and turn off losses for PowerEx CM600DU-24FH IGBTs. To determine specific $E_{sw(off)}$ value, the resonant current will have to be determined through simulation of the model. Based on the difference in the operation of the leading and lagging sets of IGBTs, a separate analysis will be required.

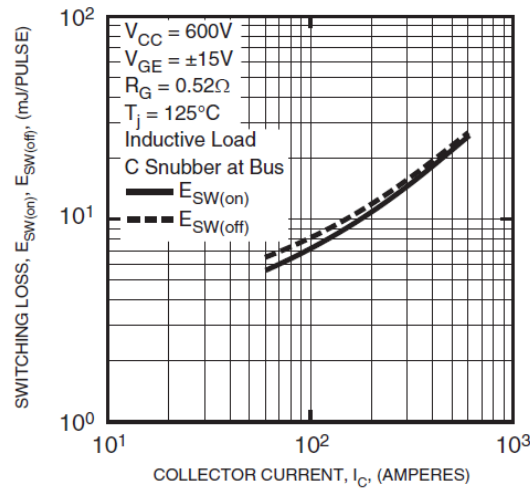


Figure 6-1: PowerEx CM600DU-24FH switching loss vs. collector current.

We begin with the leading leg, which uses a snubber capacitor to reduce the switching losses. In this case, in order to include the impact of the snubber capacitor, we apply a reduction factor ($K_{reduction1}$), which is a function of the snubber capacitor, the commutation current, the commutation voltage and switching characteristics of the devices [2].

$$P_{sw_lead} = K_{reduction1}(fxE_{offlead}) \quad (5.1)$$

While the conduction loss, also called the saturation loss, of the IGBTs can be calculated using the saturation voltage (V_{sat}) found in the manufacturing datasheet. Due to the nature of phase shifting, the leading leg will natural have lower saturation loss as a result

of freewheeling state. The leading leg uses the diode in the module, which has much lower order of conduction loss, to circulate current. As a result, the current on the leading leg can be considered roughly half. Similarly, this can be expressed in a reduction factor ($K_{reduction2}$)

$$P_{sat_lead} = K_{reduction2}(V_{sat} \times I_{mean}) \quad (5.2)$$

As previously mentioned the total losses on the IGBT will be the sum of the conduction and switching loss.

$$P_{IGBT_lead} = P_{sat_lead} + P_{sw_lead} \quad (5.3)$$

However, the loss in the IGBT module also includes the parallel diode, which is uncontrolled and consists of conduction losses only. The diode forward drop voltage (V_{CE}) is also found in the manufacturing datasheet.

$$P_{condDiode} = (V_{CE} \times I_{mean}) \quad (5.4)$$

Where $P_{condDiode} = P_{lead_Diode}$

Finally, the total loss of the IGBT module is the sum of the losses for two IGBTs and two freewheeling diodes. This provides the power loss value needed for heatsink thermal analysis.

$$P_{leading_IGBT_module} = P_{IGBT_lead} + P_{lead_Diode} \quad (5.5)$$

Similarly, we conducted analyses of the lagging leg, where the IGBT module benefits from ZCS or near ZCS operation.

Once losses from IGBTs and diode gets totaled, the thermal impedance would need to be analyzed to make sure junction temperature is still below the maximum allowable value.

Figure 6-2 shows a simple model of thermal interface from the junction temperature to ambient temperature. Where ($R_{th(j-c)}$), which is in $^{\circ}C/W$, is the thermal resistance between the junction and the module case. The manufacturer of the IGBT and diode, inside the module, provides this value. Series connection of thermal resistance of the thermal interface material ($R_{th(c-h)}$) and the thermal resistance of the heatsink ($R_{th(h-a)}$) can highlight the relationship between the ambient temperature and the virtual junction temperature.

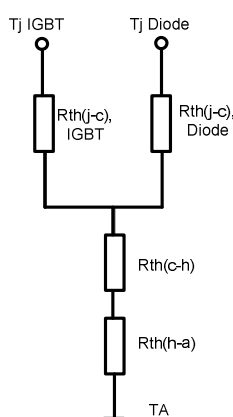


Figure 6-2: Simple model of the IGBT module thermal interface.

An excel file was developed based on the above equations at different operation points. Also included in the equation is the expected duty cycle from CT machine operation, which results in the heatsink temperature shown in Table 6-1.

TABLE 6-1: CALCULATED LOSS AND EXPECTED JUNCTION TEMPERATURE

Power	Frequency	Peak Current	Power leading	Power Lagging	Heatsink Temp	Junction Temp
15 kW	47 kHz	165 A	303.1 W	371.2 W	47.1 $^{\circ}C$	57.6 $^{\circ}C$
75 kW	41 kHz	470 A	733.7 W	1303.5 W	67.6 $^{\circ}C$	66.0 $^{\circ}C$
115 kW	39 kHz	600 A	995 W	1750 W	65.1 $^{\circ}C$	94.0 $^{\circ}C$

6.2 Heatsink Temperature Simulation

Using results from Table 6-1 above, a selected heatsink coupled with three fans each running at 150 CFM were thermally simulated. Figure 6-3 shows the steady state heatsink temperature with the converter running at 15 kW of load.

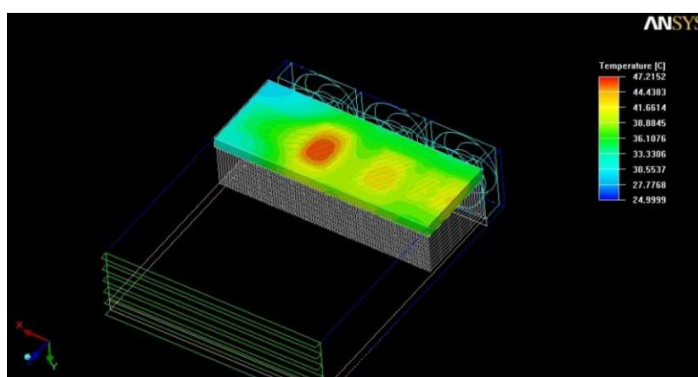


Figure 6-3: Simulation result from 15 kW average power of HFPDU.

Next, a thermal simulation of the heatsink was done for transient response. In this setup 60 kW load was introduced for 60 seconds, once the heatsink have reached steady state temperature on 15 kW average. The maximum measured heatsink temperature is found to be 67°C.

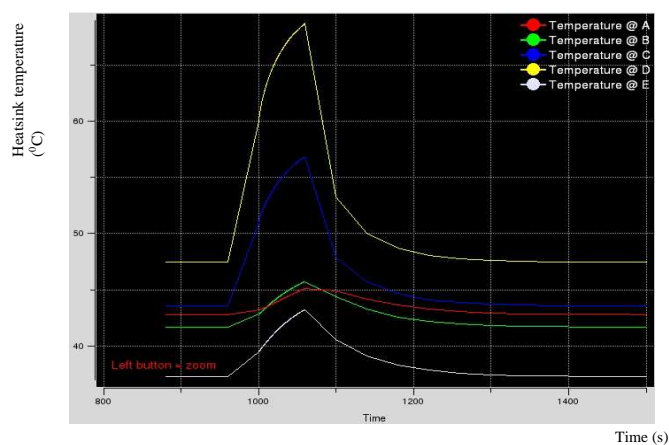


Figure 6-4: Simulation result from 15kW average plus 60kW for 1 minute.

Finally, 115 kW step load that has 5% duty cycle were simulated after the heatsink reached steady state running 15 kW average loads. The maximum heatsink temperature is found to be 65°C , which puts the junction temperature below 100°C leaving over 25°C of margin from maximum allowable junction temperature.

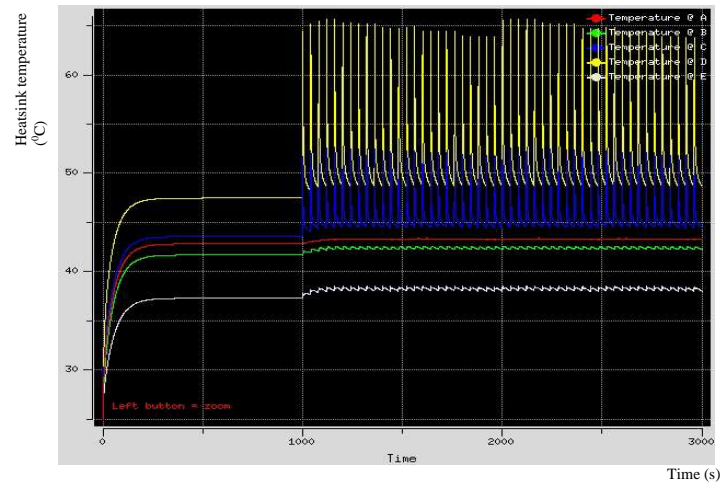


Figure 6-5: Simulation Result from 15kW Average plus 115kW for 2 seconds.

CHAPTER VII

7. ELECTROMAGNETIC COMPATIBILITY

One of the main concerns of replacing 60Hz transformer by high frequency transformer is the introduction of switching devices on the primary side of the transformer. These switching devices are the main enabler of this technology, yet are of potential concern for electromagnetic noise due to high d_v/d_t . The discipline of EMC has often been accused of being a "black art" wherein measures used to reduce the effect of a potential interference source are ineffectual [3]. This is typically due to lack of understanding on the source of noise, or the dominant effect to the overall conducted emission contributor. Figure 7-1, below shows the effect of differential-mode and common-mode current, and the frequency range where they are most dominant. This helps determine the potential source of noise, and means of mitigation.

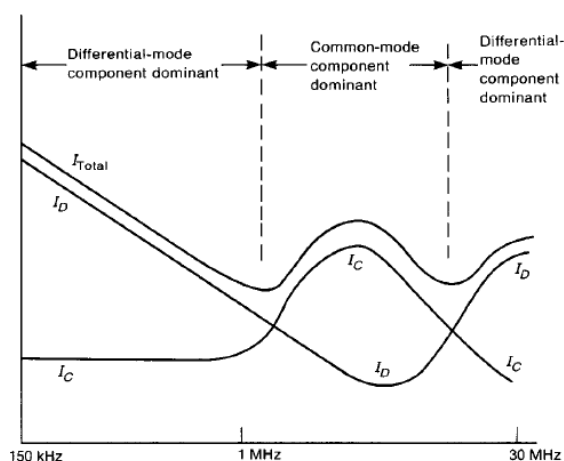


Figure 7-1: Illustration of the dominance of one conducted emission component over another in the contribution to the total emission [4].

7.1 Filter Design

To limit excess amount of conducted emission through the input power line, line filters possible on both the AC side and the rectified DC section, would be required. However; to make matter more challenging for this topology, medical grade power supply falls under strict leakage current requirements. This means that the filter design will be limited by the size of capacitance to ground it can use as part of the filter. Figure 7-2 (below) identify possible path of current to ground on the primary side of the transformer.

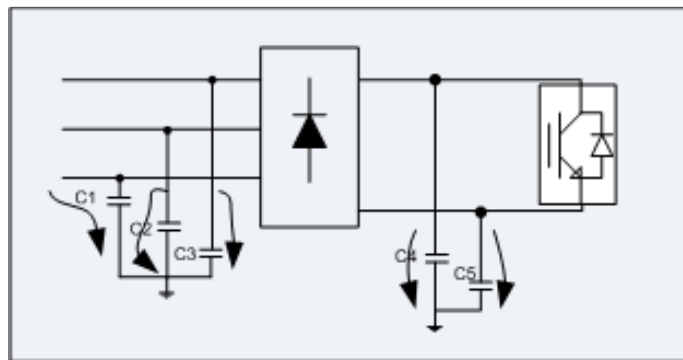


Figure 7-2: Primary Side Earth leakage Current Path.

The maximum allowed capacitor to ground on the AC side can be calculated using the line voltage, line frequency, and maximum earth leakage current.

$$I_{cap} = \frac{V_{in}}{z} = \frac{V_{in}}{2\pi f c} \quad (7.1)$$

Where $I_{rms_max} = 1mA$ per capacitor

$$\sim C_{max} = \frac{1mA}{277 * 2\pi * 60} = \mathbf{10nF}$$

Similarly the maximum allowed capacitor to ground on the DC side can be calculated using equation 7.1. However, due to 6-pulse rectification, the ripple frequency will be

360Hz, while the ripple voltage would be around 70V. Assuming $I_{rms_max} = 1.5mA$ per capacitor for the DC side

$$\sim C_{max} = \frac{1.5mA}{70 * 2\pi * 360} = \mathbf{9nF}$$

Therefore; this sets the precondition on any filter design to have a capacitor value no more than 10nF to ground on the primary side. Simulations were also conducted to check and see if the above calculation produces the expected leakage current. Figure 7-3 shows the current from each phase to ground = 1.5 mA, however the total current to ground becomes 0 mA. This is due to the assumption in the simulation were all the 3 phase are balanced, and the result would be zero due to phase cancellation.

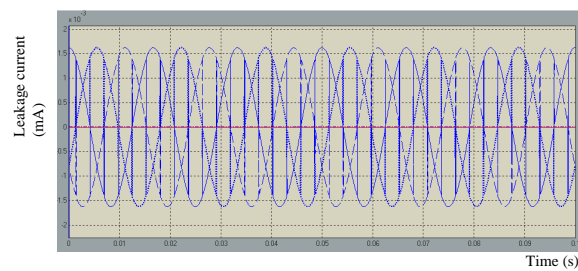


Figure 7-3: Leakage current on 3 phase AC line due to line frequency.

Followed by a simulation on the DC side, result in leakage current from line to ground =1.6mA

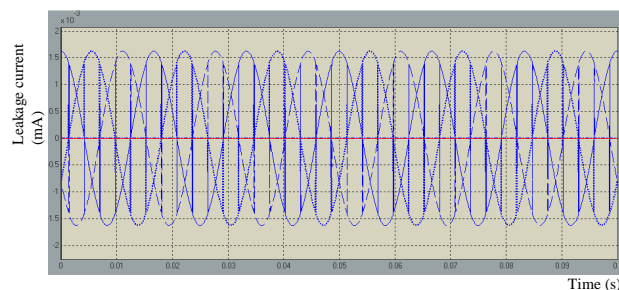


Figure 7-4: Leakage Current measurement on DC bus line due to line frequency.

Based on the precondition for the filter design, and information regarding the dominant source of noise, LTSpice simulation of EMC filter was conducted for both common-mode and differential mode noise.

Common-mode noise is when current flow out on all phase conductors and return on ground mostly through parasitic capacitors. Figure 7-5 below shows common-mode noise source together with common-mode noise filter or chock.

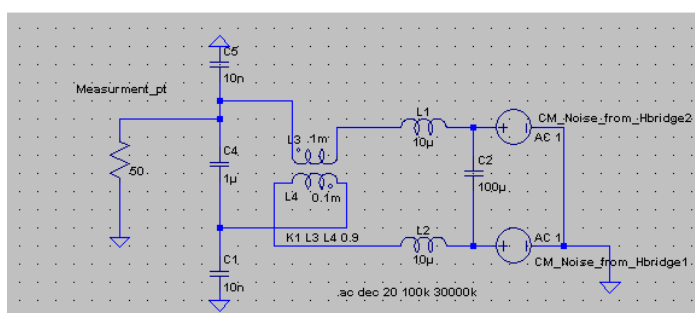


Figure 7-5: Common-mode noise simulation model using 10nF capacitor to ground.

The result from the common-mode filter model shows good insertion loss above 1 MHz frequency, which is greater than -36dB. Based figure 7-1 on the expected dominant noise contributor, the common-mode filter is expected to have significant contribution in reduce the overall EMI measurement in the frequency of interest for common-mode noise.

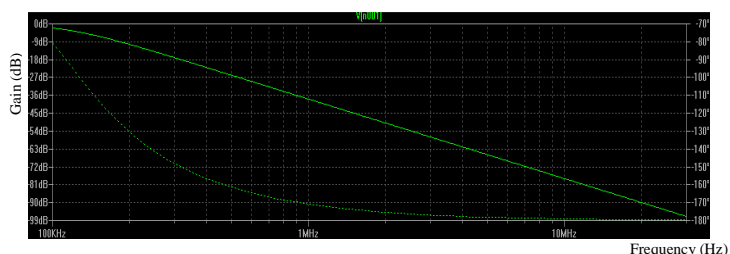


Figure 7-6: Insertion loss from the proposed LTSpice model of common-mode filter.

A similar filter model was also developed in LTSpice for the differential-mode noise, which is when current flows out of a phase conductor and returns on another phase.

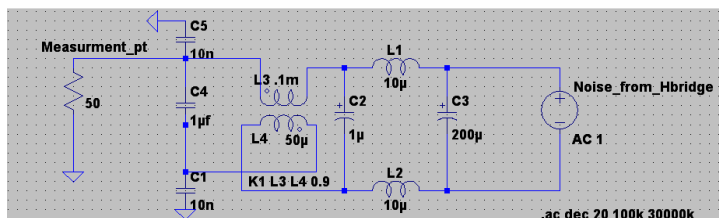


Figure 7-7: Differential-mode noise simulation model using 10nF capacitor to ground.

The result from the differential-mode filter model also shows good insertion loss across the full frequency range (100 KHz – 30 MHz) for conducted emission. With the minimum insertion loss of -40dB, this simulated filter contributes in great deal in minimizing the overall EMI measurement.

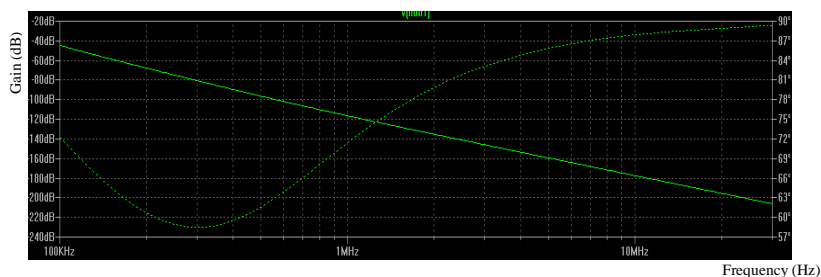


Figure 7-8: Insertion loss from the proposed LTSpice model of differential-mode filter.

7.2 Preliminary Conducted Emission Test

Conducted EMI from switching devices can be narrowband and broadband. The latter is caused by diode recovery, re-conducted radiated emissions and other, mostly parasitic phenomena, which are difficult, even impossible to predict theoretically. The

way to minimize the broadband noise is to follow good design practices, i.e. proper layout, grounding, switching etc. If these are followed, the broadband emissions are unlikely to exceed the standard limits [8]. For this thesis, a prototype was put together to get a preliminary result of conducted emission noise with a caveat that the result is very dependent on the specific packaging of prototype. This requires an understanding of the types of noise being produced, and the noise path as a result of parasitic of the package that need to be well understood.

A preliminary measurement of conducted EMI was done using line impedance stabilization network (LISN) in accordance to Comité International Spécial des Perturbations Radioélectriques (CISPR 11) specification. The above simulated line filter has been put to the test, and have shown promising resulting related to conducted emission of high frequency PDU architecture.

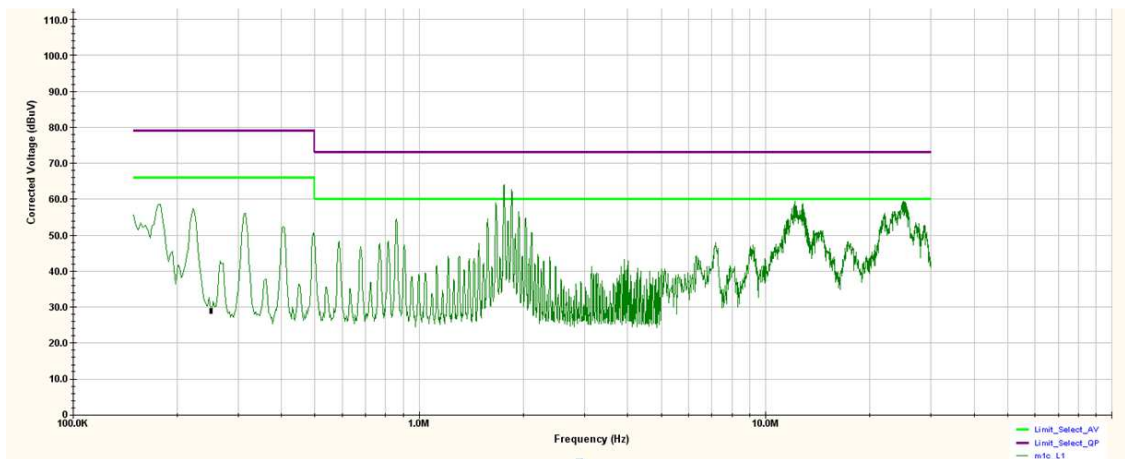


Figure 7-9: Preliminary quasi peak conducted emission measurement result of proposed topology shows -1 dB margin from quasi peak limit.

CHAPTER VIII

8. EXPERIMENTAL RESULT

To show the validity of the design procedure presented in this thesis, the proposed LLC resonant converter topology have been built and tested. This chapter presents the first HFPDU prototype, and test result of the prototype to demonstrate conformance of the design to the requirements and expected results from simulation. Figure 8-1 shows the overall package of the first HFPDU prototype with a shown significant reduction in size, with height less than 200 mm.

What was not discussed on this thesis report, but is of an important part contributor to the overall performance, is the design and implementation of control board. The first prototype uses an FPGA based control board that is not only used for monitoring but also control the resonance converter. In addition an isolated gate driver has been used to drive the gate signals from FPGA's TTL signals.



Figure 8-1: First HFPDU prototype built according to the proposed topology.

8.1 Measurement Setup

A picture of the major components on the first HFPDU prototype is shown in figure 8-2. It is mainly composed of FPGA control board, gate driver board, isolation transformer, 3-phase full bridge rectifier, full H-bridge configuration, output full bridge diodes, and fuses. This is consistent with the detail schematic shown in chapter III of this thesis report.

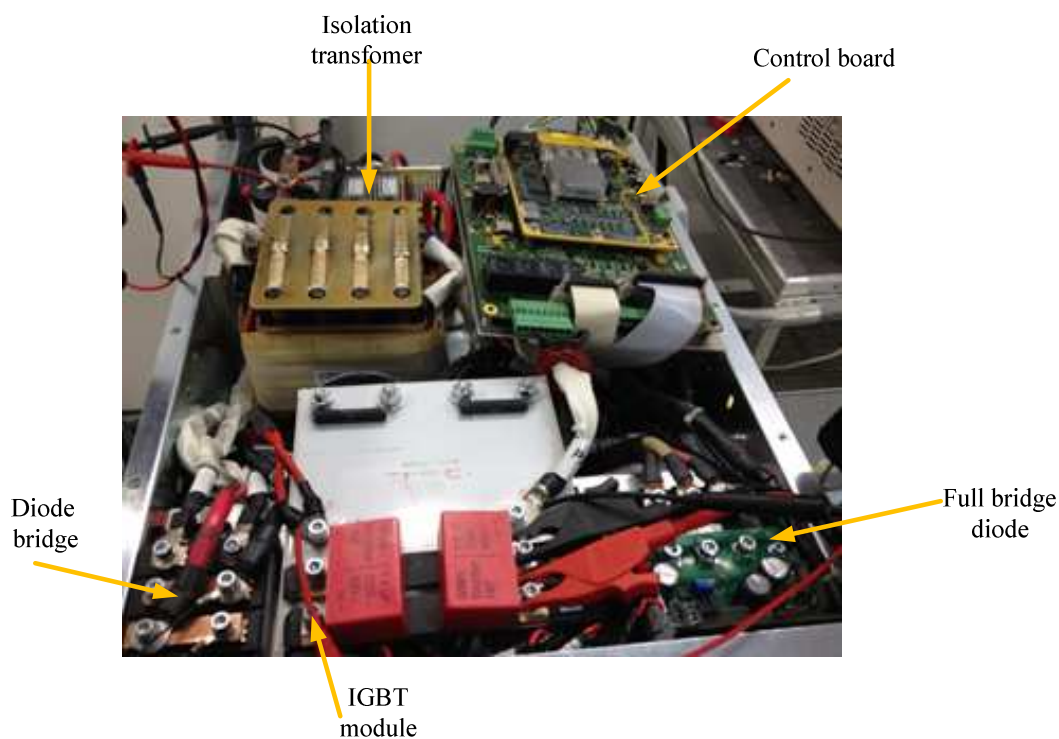


Figure 8-2: Overview of the main component of the first HFPDU prototype.

Before applying any power from the prototype, proper safety precaution must be taken due to the presence of lethal voltage. In order to collect both voltage and current measurement a Tektronic TDS5000 digital oscilloscope together with high voltage prop

were used. For the experiment result, PWM output voltage, resonant current, and output regulated voltage are presented.

8.2 Converter waveforms

Because of the difference in voltage between the input, and the output voltage at the beginning, the converter will see very high gain. As a result, given the same control law, the expectation is a very high inrush current during startup. Therefore; for this research a controlled ramp command were introduced to bring up the voltage in a controlled manner. Figure 8-3 and 8-4 show the measured result where starting from the top to bottom, a controlled output voltage ramp, PWM output voltage, and resonant current respectively. The initial start up waveform shows the output PWM being at maximum frequency, and minimum pulse width. As a result the output resonant current is very close to zero, thus limiting the output power.

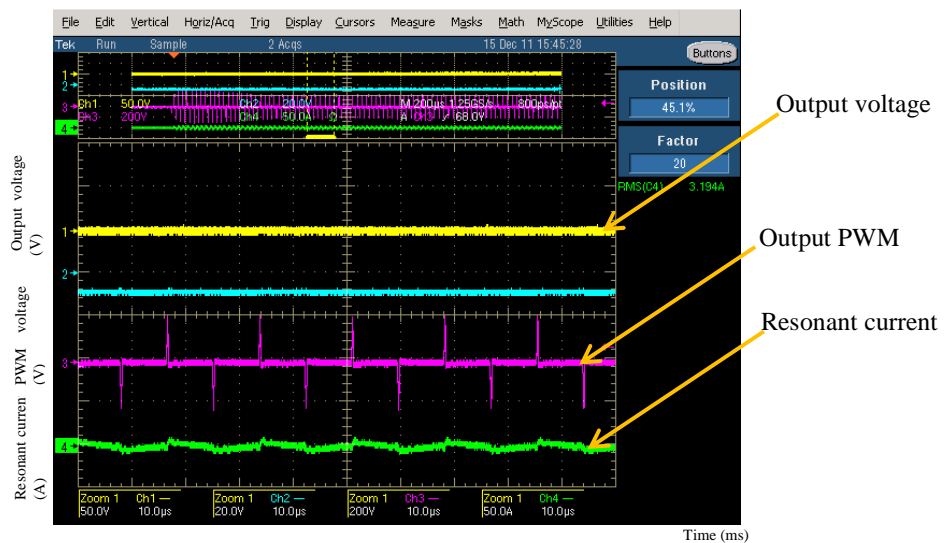


Figure 8-3: HFPDU initial pulse waveform during startup.

Figure 8-4 shows HFPDU during start up at 3 kW output load. The output voltage have followed the command ramp by limiting the resonant current in accordance to the output load.

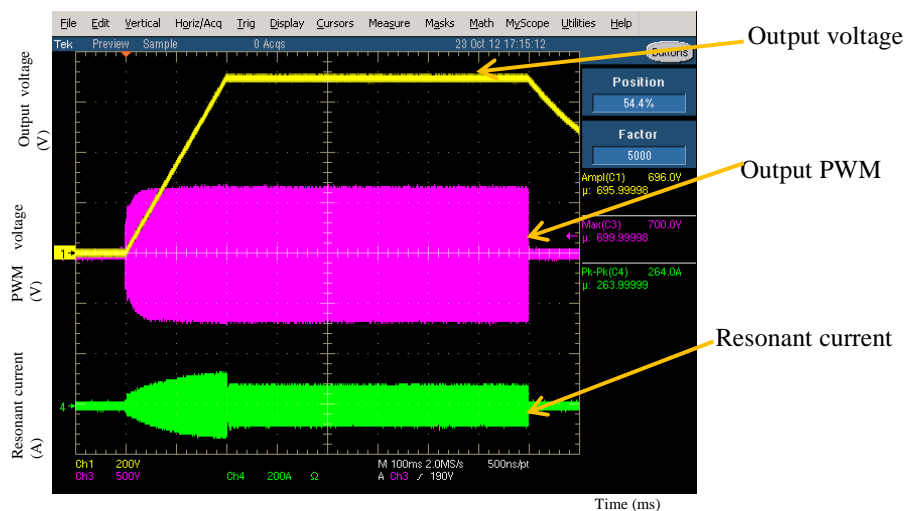


Figure 8-4: HFPDU startup waveform with a controlled ramp on the voltage.

Finally converter steady state waveform is presented in figure 8-5 below, where the output is connected to 15 kW of load. Similarly from top to bottom, figure 8-5 shows, the regulated 700 VDC voltages, PWM output voltage, and resonant current respectively.

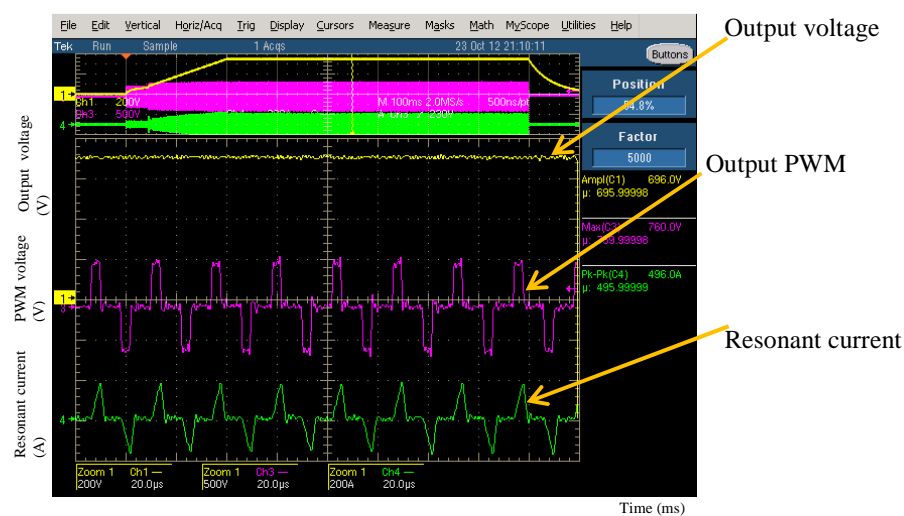


Figure 8-5: HFPDU steady state waveform with a 15 kW loads on the output.

CHAPTER IX

9. SUMMARY AND CONCLUSION

This thesis developed medical grade high frequency power distribution units using resonant converter to replace traditional CT power distribution units. Starting with the over view of resonance topology, and operating scheme, the paper have pointed out the benefits and shortcoming of different series resonant converter. Following in chapter 3, an LLC resonant converter topology, and super resonance operation has been selected in order to benefit from both the series and parallel load resonant converter. The selected topology provides inherent short circuit protection and lower part counts, particularly because of resonant converter capability of using leakage inductance, and magnetizing inductance of a transformer for its resonant tank.

Following the section of LLC resonant converter topology, a design model was developed using Matlab/Simulink, and control capability has been simulated. In order to account for variation in operating environment and part to part variation, Monte Carlo analysis were conducted to show conformance to the specification. Furthermore; simulation of the magnetics, filter design, and the thermal performance were conducted to set the stage for design implementation.

A prototype of the selected topology was built and result was evaluated. The measured result has been found to show an excellent correlation with the simulation result. This gave confidence in the accuracy of the model, and the results from the various simulations.

Finally, the technique and topology that were discussed here are by no means exclusive only to CT system, or even medical system. In fact, it can be used in many other applications that can benefit from isolating grid disturbance, regulated output voltage, and reduction in overall size in a cost effective manner.

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A. APPENDICES

A.1 UNDAMPED SERIES-RESONANT CIRCUIT

Figure A-1 shows an undamped series-resonant circuit where the input voltage is V_d at time t_o . The initial conditions are I_{L_o} and V_{C_o} . With the inductor current i_L and the capacitor voltage v_c as the state variables, the circuit equations are [11]

$$L_r \frac{di_L}{dt} + v_c = V_d \quad (\text{A-1})$$

and

$$C_r \frac{dv_c}{dt} = i_L \quad (\text{A-2})$$

For $t \geq t_o$, the solution is as follows:

$$i_L(t) = I_{L_o} \cos \omega_o(t - t_o) + \frac{V_d - V_{C_o}}{Z_o} \sin \omega_o(t - t_o) \quad (\text{A-3})$$

$$\text{and } V_c(t) = V_d - (V_d - V_{C_o}) \cos \omega_o(t - t_o) + Z_o I_{L_o} \sin \omega_o(t - t_o) \quad (\text{A-4})$$

$$\text{where } \text{angular resonance frequency} = \omega_o = 2\pi f_o = \frac{1}{\sqrt{L_r C_r}} \quad (\text{A-5})$$

$$\text{and } \text{Characteristic impedance} = Z_o = \sqrt{\frac{L_r}{C_r}} \quad (\text{A-6})$$

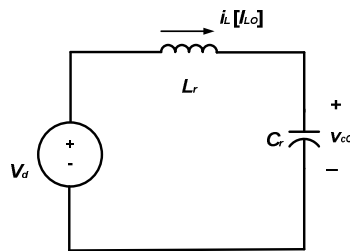


Figure A-1: Undamped series-resonant circuit [11].

A.2 SERIES-RESONANT CIRCUIT WITH A CAPACITOR-PARALLEL LOAD

Figure A-2 shows series resonant circuit, where the capacitor is loaded in parallel with I_o . In this circuit, V_d and, I_o are dc quantities. The initial conditions are I_{LO} and V_{CO} at time t_o [11]. Therefore

$$v_c = V_d - L_r \frac{di_L}{dt} \quad (\text{A-7})$$

and
$$i_L - i_c = I_o \quad (\text{A-8})$$

By differentiating Eq. A-7

$$i_c = C_r \frac{dv_c}{dt} = -L_r C_r \frac{d^2 i_L}{dt^2} \quad (\text{A-9})$$

Substituting i_c from Eq. A-9 into Eq. A-8 yields

$$\frac{d^2 i_L}{dt^2} + \omega_o^2 i_L = \omega_o^2 i_o \quad (\text{A-10})$$

Where angular resonance frequency ω_o is still the same as Eq. (A-5), solution for $t \geq t_o$ is as follow:

$$i_L(t) = I_o + (I_{LO} - I_o) \cos \omega_o(t - t_o) + \frac{V_d - V_{co}}{Z_o} \sin \omega_o(t - t_o) \quad (\text{A-11})$$

And

$$v_c(t) = V_d - (V_d - V_{co}) \cos \omega_o(t - t_o) + Z_o (I_{LO} - I_o) \sin \omega_o(t - t_o) \quad (\text{A-12})$$

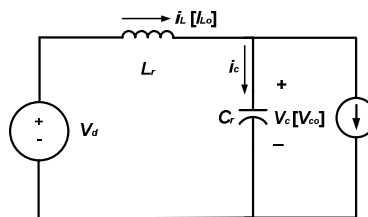


Figure A-2: Series-resonant circuit with capacitor-parallel load [11].