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Multi-Level Medium Voltage Inverter for Dc Distributed Wind Farm to Establish Grid Interface and Provide Ancillary Support

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MULTI-LEVEL MEDIUM VOLTAGE INVERTER FOR DC DISTRIBUTED WIND FARM TO ESTABLISH GRID INTERFACE AND PROVIDE ANCILLARY SUPPORT

by

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ABSTRACT
MULTI-LEVEL MEDIUM VOLTAGE INVERTER FOR DC DISTRIBUTED WIND FARM TO ESTABLISH GRID INTERFACE AND PROVIDE ANCILLARY SUPPORT

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Under the Supervision of Professor Dr. Adel Nasiri

Wind energy has gained in popularity in recent years due to cost, security and environmental concerns associated with conventional energy sources like fossil fuels. However, the utilization of wind energy in power systems creates many technical and non-technical challenges that need to be addressed for successful integrations. The main technical issues related to wind energy are its uncertainty and variability and their impacts on stability, reliability and quality of the electric power. In systems with high wind energy penetrations, unlike conventional generations, sudden changes in active and/or reactive power demand cannot be supported by wind energy. This lack of demand support may create unwanted voltage and frequency variations in the grid. On the hand, the existing AC distributed wind farms have several drawbacks including complexity, higher cost, and lower efficiency.

In this dissertation, a medium voltage direct current (MVDC) distribution system for wind farms is investigated. The proposed system offers higher reliability, lower cost,

higher efficiency and more importantly grid support. It also allows for easier integration of energy storage systems at DC level. Design, control, implementation, and testing of a three-level medium voltage inverter are presented. The inverter can provide active and reactive power support to the grid in case of frequency and voltage droops. Simulation and experimental results are presented to verify the viability of the proposed system and control techniques.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

DC – Direct Current

AC – Alternating Current

VSI – Voltage Source Inverter

VSC – Voltage Source Converter

CSC – Current Source Converter

LCL – Inductor – Capacitor – Inductor filter

NPC – Neutral Point Clamp

AGC – Automatic Generator Controller

PCC – Point of Common Coupling

MVDC – Medium Voltage Direct Current

HVDC – High Voltage Direct Current

LVRT – Low Voltage Ride Through

PMSG – Permanent Magnet Synchronous Generator

MPPT – Maximum Power Point Tracking

PLL – Phase Locked Loop

SVPWM – Space-Vector Pulse Width Modulation

DPWM – Discontinue Pulse Width Modulation

THIPWM – Third Harmonic Injection Pulse Width Modulation

ADC – Analog to Digital Converter

DFIG – Doubly Fed Induction Generator

PMSG – Permanent Magnet Synchronous Generator

1.1 Introduction

Renewable energy is increasingly popular over conventional energy. In particular, wind generation has become a substantial share of the total generation. As shown in figure 1.1, in the US alone 10GW wind power installation was added in 2009 with a cumulative capacity over 35GW. Figure 1.2 shows that world total wind power installation is over 190GW. Figure 1.3 shows the renewable energy installed capacity in 2009 is almost 40% of the total installed capacity [1].

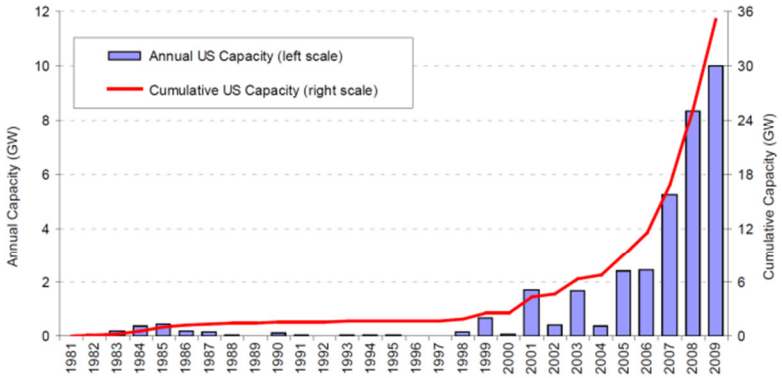

Figure 1.1 Annual / cumulative installed capacity of wind power (US), Source NREL

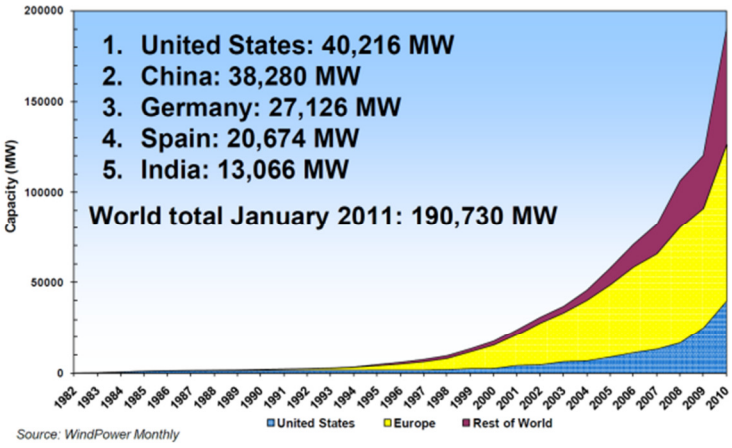

Figure 1.2 Total installed wind power capacity, source Wind power

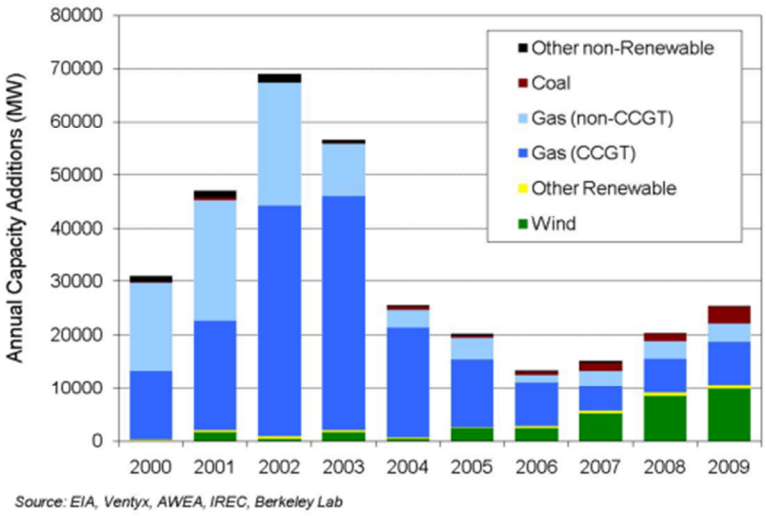

Figure 1.3 Wind power annual capacity addition, source EIA

The electric energy generation using wind turbines have been in the form of AC so far. This is because most of the wind turbine installations are land based. In addition existing machines, existing power conversion systems, control systems and protection scheme have been adapted in wind energy systems. Besides the onshore trend, offshore wind farms have also been continuing to grow rapidly. Some leading countries in the wind energy arena are focusing more on offshore technology. The main reasons for adopting offshore are lack of suitable onshore sites, installation of wind farms closer to load areas and the much better wind conditions of offshore sites. Sometimes, many of the large offshore wind farms are installed more than 50-60 miles away from the grid connection point. However, AC distribution through submarine cables seems to be less economical for distances about 50-60 miles due to issues related with high charging currents, reactive power and harmonics.

1.2 Problem with offshore wind farm and its distribution

The trend in the wind power industry is the off shore wind farms. Off shore wind farm has its own challenges in terms of cost-effective installation and energy efficient power transfer. Generally offshore wind farms have back to back converters and transfer energy from the wind farm to the grid using three phase AC system. If overhead three phase AC system is used to transfer power from the wind farm to grid, the cost of the installation is very high. In addition to ecological and aesthetic considerations, there are more overhead faults compared to underground faults. If underwater three phase AC system is used in this case, there are higher reactive power requirement as well as being difficult to locate the fault. It is necessary to have a viable economical solution for offshore wind power integration to the gird.

1.3Uncertain availability of wind power and effect on the grid

The grid is dominated by the synchronous machines. Synchronous machines have inertia. When there is sudden change in the active power demand, synchronous machine inertia will allow keeping the frequency of the grid within limits for short durations. It allows time for automatic generation system of the grid to react based on the change in demand. As more and more renewable energy resources are added to the grid, total inertial of the grid won't be dominated by the synchronous machines any more. Grid will be prone to frequency deviation by fluctuations of the load. The frequency deviation is severe enough and won't allow any time for automatic generation systems to react. It

severely impacts the power system stability and in some cases it leads to power outages. In addition, the reactive power of the grid is generally supported by synchronous generator, synchronous condenser, static VAR compensator or shunt capacitor. The reactive power effect is localized and reactive power generation must be close to where it requires voltage support. Generally the wind power unit is located remotely and does not support any reactive power generation. When there is a sudden fluctuations of the reactive power demand, the grid voltage may collapse and lead to brownout conditions. Both of these conditions affect grid stability, reliability and quality.

1.4.MVDC distribution for wind applications

The solution for reactive power support is provided in [2]. The reactive power support is based on combination of the STATECOM (static synchronous compensator) and wind power. It did not address the issue of frequency support. Various references [3], [4] discussed the optimized algorithm to provide reactive power using the DFIG (Doubly Fed Induction Generator) to keep the grid voltage constant. It is machine specific and won't provide a generic solution which includes PMSG (Permanent Magnet Synchronous Generator). In addition, it did not mention about frequency support for the grid. Reference [5]-[7] discussed frequency support, but it always requires the availability of the wind power. There is no back up energy storage system available to support the frequency during off peak wind. Reference [9] is used the VSC-HVDC (High Voltage Direct Current) connected wind farm to support the frequency of the grid without any energy storage unit. In addition, it is very expensive to integrate the energy storage unit

directly to the HVDC bus. The existing converter topologies and power modules easily support the MVDC system [8], [10], [13]. The bi-directional DC-DC converters are available [14] which allow integrating the energy storage systems with the MVDC bus. The MVDC power distribution systems offer several benefits over AC distribution system, such as lower losses and voltage drops, which allow to distribute power over longer distances and to interconnect remote offshore wind farms. With minor drawbacks there are many solutions for a cost effective control and protection of DC distribution system are presented in [13]. Particularly for offshore wind power applications, medium voltage direct current (MVDC) system is suitable from the size, cost and efficiency point of view over high voltage DC system (HVDC)[10]. MVDC distribution can be classified as monopole with ground return, monopole with metallic return or monopole with midpoint grounded. In the entire configuration there is significant cost advantage over the AC distribution. In addition there is no skin effect and minimum loss in the cables. Figures 1.4 to 1.6 show different DC distribution topologies. Added advantages of the DC distribution system are that PV can directly couple to the DC bus of the DC distribution system. Energy storage units and ultra-capacitor banks can be connected to the DC bus.

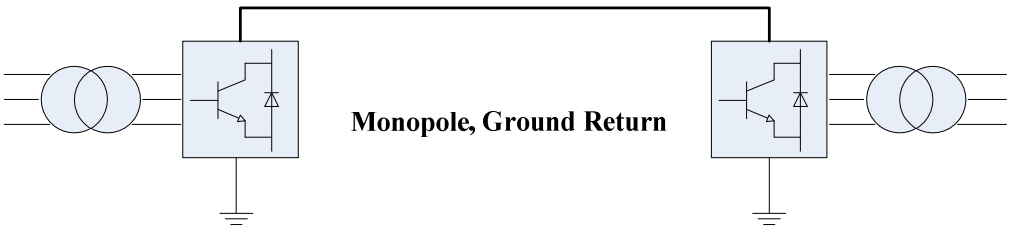

Figure 1.4 DC distribution with monopole and ground return

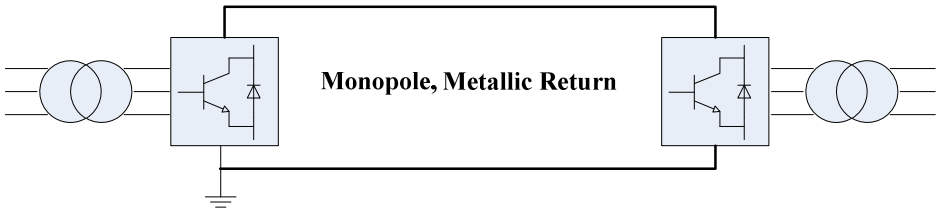

Figure 1.5 DC distribution with monopole and metallic return

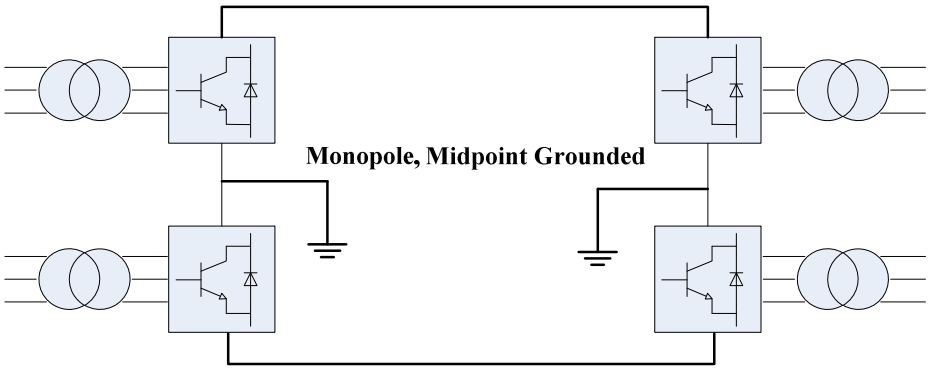

Figure 1.6 DC distribution with monopole and midpoint grounded

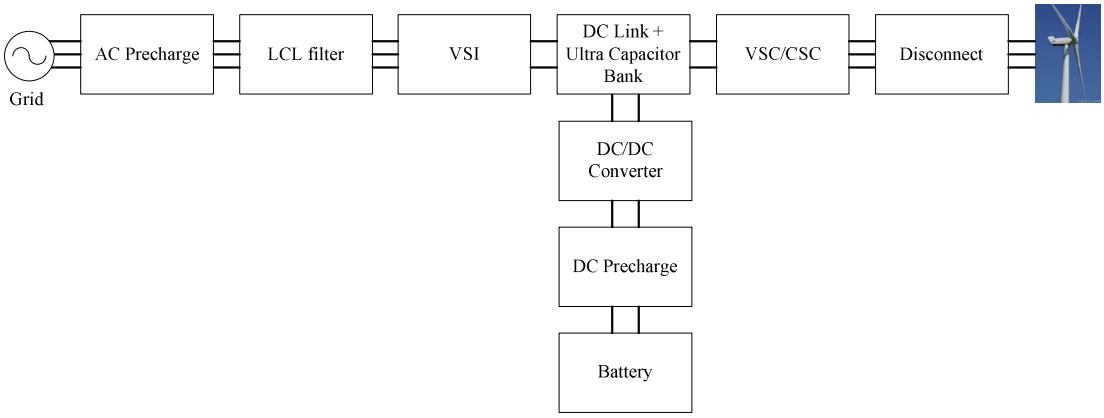

Figure 1.7 Block diagram of proposed MVDC distribution system

The block diagram of proposed DC distribution system for a wind farm is shown in figure 1.7. The wind farm connected to the MVDC link using CSC/VSC based converter and AC side disconnect switch. Energy storage, PV unit etc. can be interface with the

MVDC link using DC precharge and DC/DC converter. The MVDC link connects to the grid using VSI, LCL filter and AC precharge unit. The MVDC provides the cost effective distribution of the wind power. VSI based inverter can be controlled such a way that it provides frequency and voltage droop support to the grid.

In this thesis, a novel frequency and voltage droop support control strategy is presented which increases the stability and reliability of the grid. The VSI based 3L NPC topology to support the MVDC system is discussed in detail. An algorithm to provide optimized value of the LCL filter is discussed. It reduces the size, cost and power losses of the LCL filter. Novel precharge topologies (AC and DC) offer size and cost effective solutions. Energy efficient voltage source inverter with standby mode of operation during unavailability of wind is provided. The following chapter discusses the precharge for the voltage source inverter application.

2. Precharge

The precharge circuit is used to reduce high inrush current to the DC link capacitor during startup of the VSI. The typical precharge circuit includes precharge resistors in parallel with the contactor. The precharge circuit can either connected to the AC side of the VSI or the DC side of the VSI. Different types of the conventional precharge circuits commonly used for the power conversion systems will be discussed in this chapter. The novel AC and DC precharge circuits are presented and compared with conventional precharge circuits. Precharge control sequences will be discussed in detail and verified using simulation results.

2.1 Types of Precharge Circuits

One of the commonly used precharge circuit is shown in figure 2.1 and 2.2 as below [15][17]. The circuit breaker (CB) is used for to isolate the system from the grid. The precharge circuit is connected between the LCL filter and the VSC. The precharge circuit consists of the precharge contactor (PC) in parallel with the resistor(R). The precharge contactor is rated for the full load current of the system. During start up, first turn on the circuit barker. The precharge contactor is normally open and the DC capacitor bank is charged through the resistor. The precharge controller turns on the contactor when the DC capacitor bank charges up to 90% of the peak grid line to line voltage. Once the precharge contactor turns on, precharge resistors are bypassed. The precharge resistors need not to be rated for a higher wattage rating because it just precharges the DC capacitor bank and after that there is minimum current flow through the precharge

resistor. The disadvantages of this precharge are two full load rated components (circuit breaker and precharge contactor) are required. The LCL filter capacitor bank is not precharge through the precharge circuit and may be prone to damages from the inrush current.

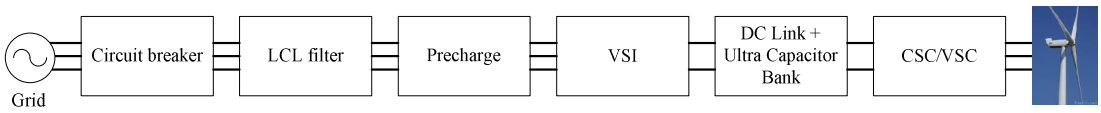

Figure 2.1 Block diagram system with conventional AC precharge

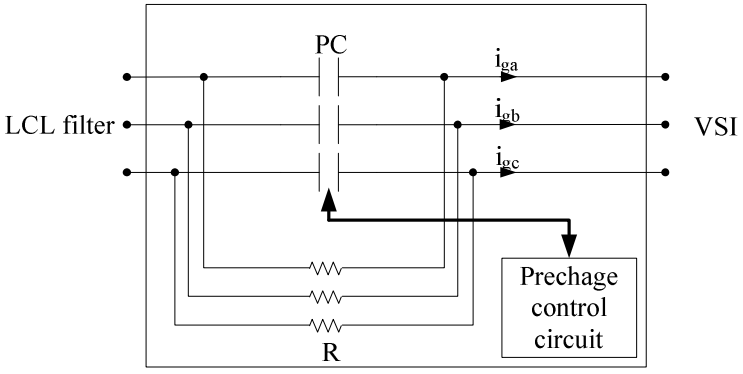

Figure 2.2 Detail of the AC side precharge circuit

Another commonly used precharge circuit is shown in figure 2.3 and 2.4 as below [17]. The circuit breaker is used to isolate the main power structure from the grid. During start up, the circuit breaker is normally off. The DC capacitor bank is charged through the precharge contactor, rectifier and resistor. The precharge controller will wait until the DC capacitor bank charge up to 90% of the peak line to line voltage and then it will issue a command to close the circuit breaker. After the circuit breaker turns on, the precharge control will turn off the precharge contactor. The precharge contactor is not rated for the

full load rating of the system. The only disadvantage of this precharge is that the LCL filter capacitor is not precharged.

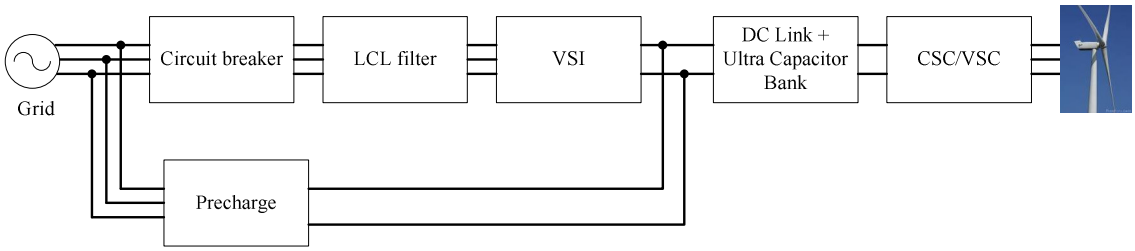

Figure 2.3 Block diagram system with conventional precharge (DC side)

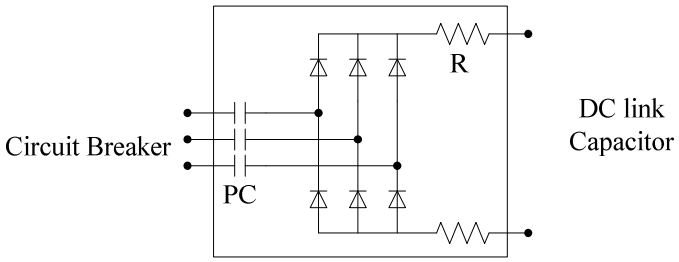

Figure 2.4 Detail of the DC side precharge circuit

A novel precharge circuit for the power conversion system is shown in figure 2.5 and 2.6. The precharge circuit is between the grid and the LCL filter [16][18]. The precharge circuit consist of a circuit breaker, fused disconnect (FD), fuses, precharge contactor and resistors. The fused disconnect and the precharge contactor is not rated for full load. Only the main circuit breaker is rated for full load current.

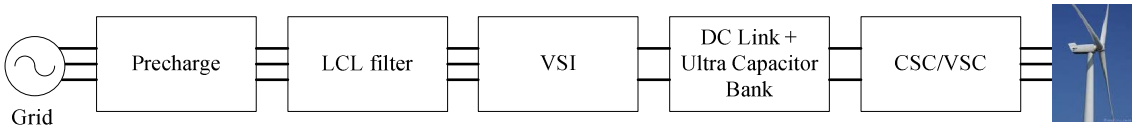

Figure 2.5 Block diagram of system with novel AC precharge

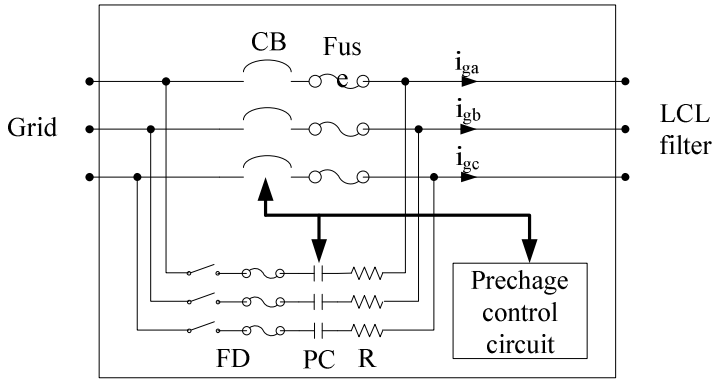

Figure 2.6 Detail of the novel AC precharge circuit

The precharge resistor need to be rated for higher power rating because during the precharge mode it will carry the current to charge the DC capacitor bank as well as the circulating current through the LCL filter. It is also necessary to make sure the precharge resistor is in the circuit for a very short duration, till the DC bus is precharged. Once DC bus reaches 90% of the grid line to line voltage, it must turn on the main circuit breaker to avoid the LCL circulating current passing though the precharge resistor. This indirectly imposes the requirement of automatic precharge circuit instead of manual precharge.

2.2Precharge sequence for propose novel AC precharge topology

Precharge turn on sequence:

- Manually turn on the fused disconnect.
- The precharge control circuit turn on the precharge contactor
- LCL filter capacitor bank and DC link capacitor start recharging through fused disconnect, precharge contactor and resistor.

- When the DC link voltage reaches 90% of the peak line to line grid voltage, the precharge controller will turn on the circuit breaker.
- After the circuit breaker turns on, the precharge controller will turn off the precharge contactor.
- The precharge contactor always turns off after the precharge complete or after fault occurred, which prevents circulating current through the LCL filter.

Precharge turn off sequence:

- Turn off the fused disconnect.
- Precharge controller detect the status of the fused disconnect.
- Precharge controller will turn off the VSC first and then open the circuit breaker.

2.3Advantages of novel precharge circuit

- Only one full rated current component is used, which leads to lower power loss and cost effective design.
- The precharge circuit serves dual purpose. 1) precharge 2) Means of disconnect of the power conversion unit from the grid and lockout / tagout operation.
- Precharge circuit precharge DC link capacitors as well as the LCL filter capacitors. It increases the life of the filter capacitors.
- In case of fault or normal turn off sequence, the precharge controller will turn off the inverter first and then issue an actuate command to turn of the circuit breaker.

These guarantees the no load makes and breaks operation of the circuit breaker. It reduces the maintenance and increases the life of the circuit breaker.

2.4Novel DC precharge circuit

The derivate of the novel AC precharge technique is used for the DC precharge applications as shown in figure 2.7. The battery is connected to the DC/DC converter using the DC precharge circuit. The DC/DC converter is used to charge the battery and delivers energy back to the grid to support the frequency and voltage droop control.

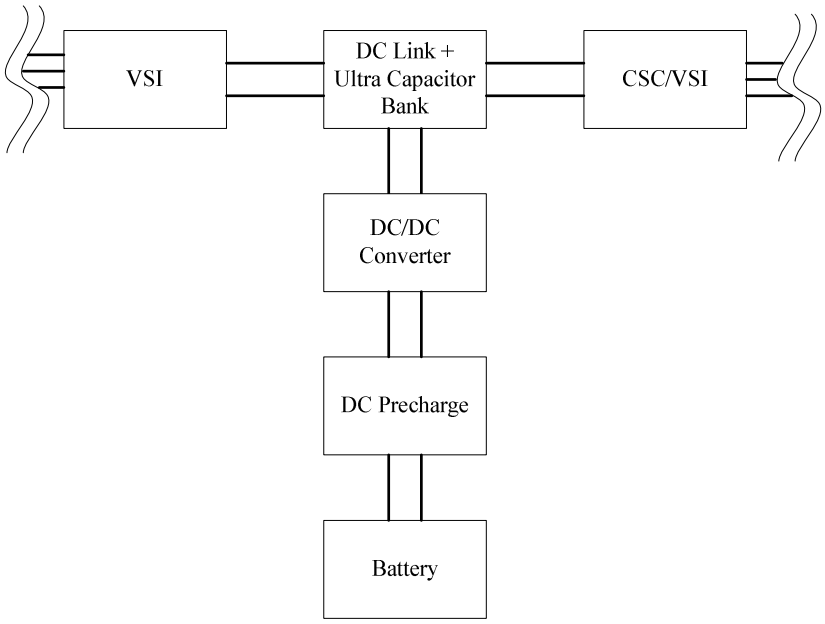

Figure 2.7 Block diagram of the power conversion system with DC precharge

The DC precharge circuit diagram is shown in figure 2.8. The DC precharge circuit is similar to AC precharge as shown in figure 2.6. The only differences are the precharge contactor is not required and the precharge resistor is not rated for a higher power [19].

The fused disconnect turns on manually. The DC bus on DC/DC converter starts pre-charging through FD and the resistors. When the DC link capacitors are completely charged, the precharge controller turns on the circuit breaker. The DC precharge works as a precharge as well as the disconnect means in case of the maintenance. Same as the AC precharge, the DC precharge controller algorithm make sure that the CB always turns on and turns off at no load. Which reduces the size of DC rated circuit breaker and provides potentially cost saving solution for the MVDC system.

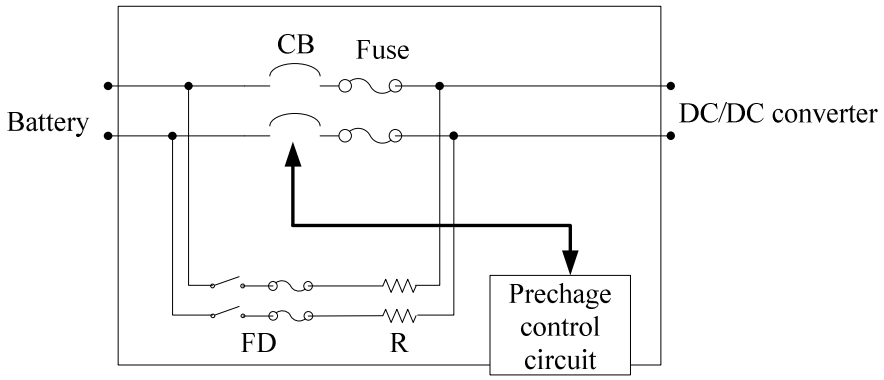

Figure 2.8 Detail of the DC precharge circuit

2.5Simulation results

The simulation study of the AC precharge is performed using Matlab Simulink software. Figure 2.9 shows the Simulink model of an AC precharge. The AC precharge controller controls the ON and OFF sequence of the precharge contactor and main circuit breaker during the precharge operation. The precharge model parameters are shown in table 2.1 as below:

AC precharge Parameters	
Input Voltage	480Vac
Total Power	200kW
Bus Capacitance	60mF
3% Inductor	84uH
9% Inductor	254uH
5% Capacitor	415uF
Precharge Resistor	2.5ohm

Table 2.1. AC precharge parameter use for simulation

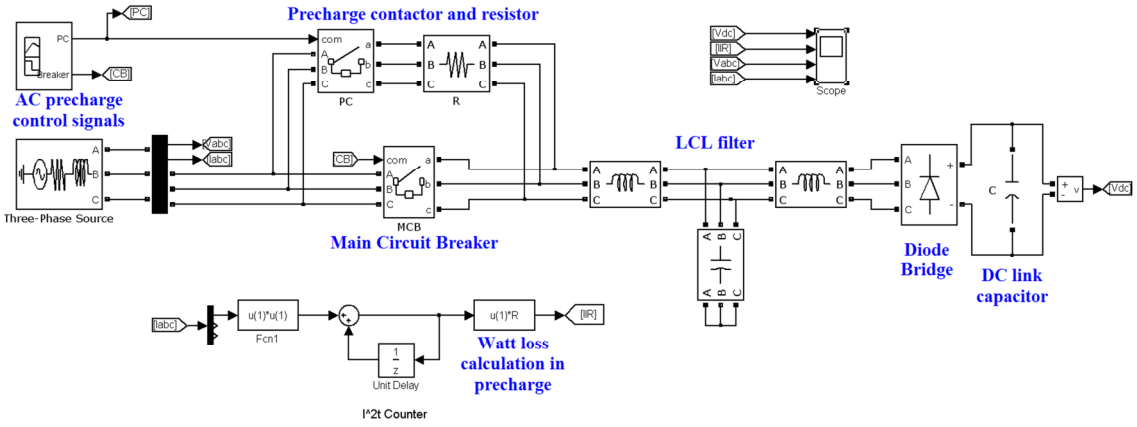

Figure 2.9 Matlab Simulink model of AC precharge circuit

The simulation result of an AC precharge is shown in figure 2.10. The first waveform shows the DC bus capacitor charge up to 90% of the peak line voltage within 2 sec. Second waveform shows the i^2tR counter for the precharge resistor, which determines the rating of the resistor. The line current waveform shows that when MCB is close, the capacitor bank will charge remaining 10% rapidly and around 1000A peak current pass through the circuit breaker.

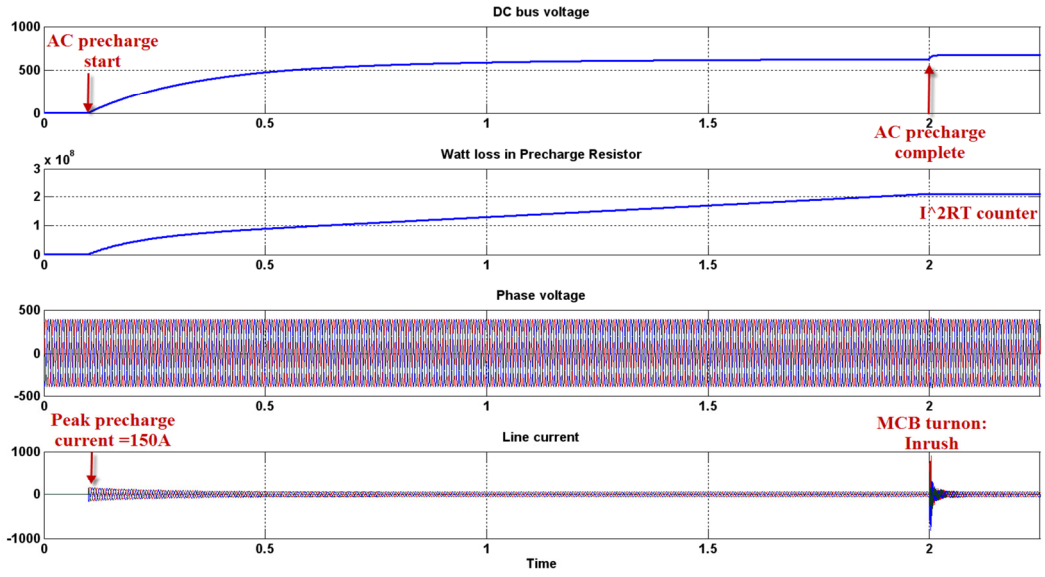

Figure 2.10 Simulation result of AC precharge

Figure 2.11 shows the Simulink model for DC precharge circuit. The Precharge contactor is not required in the DC precharge circuit. For the DC precharge application, one can select a higher precharge resistor value. The parameter for the DC precharge circuit is shown in table 2.2. Figure 2.12 shows the dc precharge simulation result.

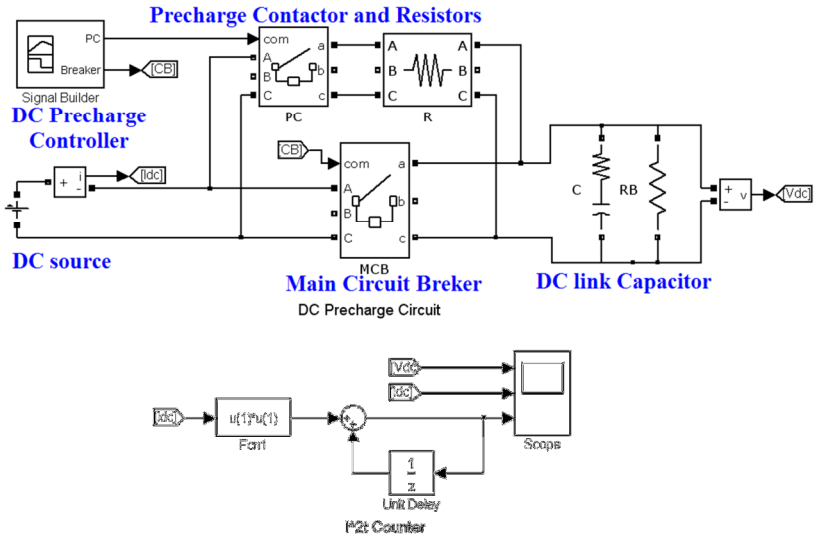

Figure 2.11 Matlab Simulink model of DC precharge

DC precharge parameters	
DC bus voltage	678Vdc
Bus Capacitance	15mF
Cap ESR	0.0104ohm
Balancing Resistor	5000ohm
Precharge Resistor	50ohm

Table 2.2. DC precharge parameter for Simulink model

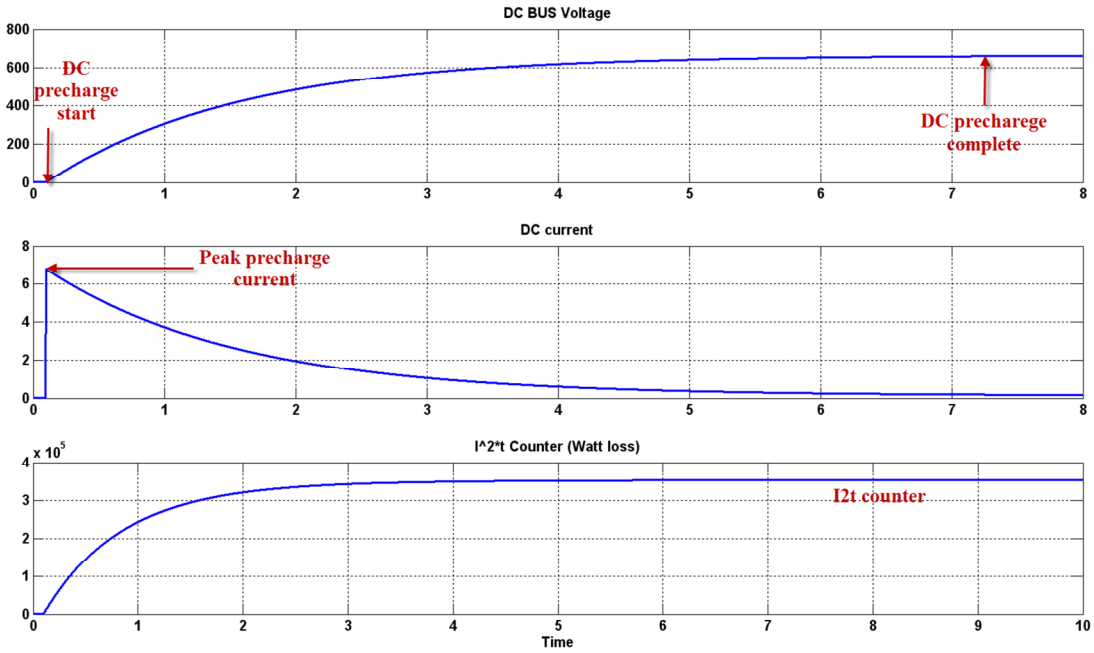

Figure 2.12 Simulation result of DC precharge

2.6Conclusion

The novel AC and DC precharge topologies are presented in this chapter. The proposed AC precharge topology precharges the DC link capacitor as well as LCL filter. Both AC and DC precharge have size and cost advantages. It reduces the maintenance and increase life of the switch gear. An automated AC and/or DC precharge topology

enables standby mode of operation when wind is not available. In next chapter, the LCL and the Trap filter for VSI are discussed in detail including optimum design algorithm, effect of grid impedance and passive damping technique to reduce the resonance in the filters.

3. LCL and Trap filter for VSI

This chapter presents two main filters widely used in industry for the three phase voltage source inverters. The filters are the Trap and the LCL. These filters are primarily used to reduce the switching frequency ripple and to meet the IEEE 519 THD requirements. The algorithms presented in this chapter provide optimized values of the inductors and capacitors for the Trap and LCL filters. The source impedance has significant effect on the resonance of the filters. The passive resonance damping techniques are presented in this chapter. The Trap and LCL filters for a 125kW voltage source inverter are designed using algorithm. The simulation and experimental results reveal the performance of the Trap and LCL filter. This chapter also compares the Trap and LCL filter results.

3.1. Low harmonics requirements

Voltage source inverter connection to the grid contributes to harmonic distortion proliferating throughout the system. The IEEE Standard 519 established a basis for limits on system distortion. The IEEE 519 specifications for voltage and current harmonics are shown in Table 3.1 and 3.2. In many specifications the lowest number in table is used for all situations and little attention is paid to the I_{SC}/I_L ratio at PCC (point of common coupling). For a soft source (I_{SC}/I_L<20) the current distortion is less than 5% whereas for a stiff source (I_{SC}/I_L= 100-1000) the current distortion is less than 15%. Voltage source are connected to the grid using the reactors or filters and isolation transformers. The size

of the isolation transformer defines the allowable distortion as per IEEE 519 as presented in [20]. Generally for medium to higher power applications, lower converter switching frequencies are selected to reduce switching losses. This results in smaller heat sinks and cooling fans. As a result, active converter size will be reduced and efficiency will be higher. The lower switching frequency requires a higher value of the input reactors to reduce the switching frequency ripple, which is very expensive and gives poor dynamic response. In addition, a reactor alone is not sufficient to meet the IEEE 519 requirements. Alternative solutions to these problems are to use either a Trap or a LCL filter instead of the line reactors as suggested in [20]-[22]. Trap and LCL filters are specifically design to reduce switching frequency ripple and provide lower total harmonic distortion.

Bus Voltage at PCC	**Individual Harmonic (%)**	**Total Harmonic Distortion THD%**
1.0kV and below	5.0	8.0
1.001kV through 69kV	3.0	5.0
69.001kV through 161kV	1.5	2.5
161.001kV and above	1.0	1.5

Table 3.1 IEEE 519 Voltage Distortion Limit

Maximum Harmonic Current Distortion in Percentage of IL						
Individual Harmonic Order (Odd Harmonics)						
Isc/IL	<11	11<=h<17	17<=h<23	23<=h<35	35<=h	TDD
<20	4.0	2.0	1.5	0.6	0.3	0.5
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Isc =max short circuit current at PCC. IL=max demand load current at PCC						

Table 3.2 IEEE 519 Current Distortion Limit

3.2 Trap filter analytical model and design algorithm

3.2.1 Trap filter configuration

A Trap filter based 3L VSI is shown in figure 3.1. The filter name is based on its ability to trap the switching frequency components. L_g and L_c are grid side and VSI side inductances. $L_g=L_t+L_1$, where L_t is the inductance of the isolation transformer and L_1 is inductance of the line side inductor. L_t is not required unless the application requires two converters connected in parallel on the same isolation transformer. In paralleling, L_t is used to reduce the circulating current between the two parallel units. The inductor L_f and the capacitor C_f are conned in Y configuration. The damping resistor R can be connected in series with the L_f and the C_f to damp the resonance. The resonance study and the novel techniques to mitigate the resonance are discussed later in this chapter.

The goal of the Trap filter is to reduce the switching frequency ripple and meet the IEEE 519, total harmonic distortion requirements. The L_f and C_f are tuned to the switching frequency of the 3L VSI [23]. The design of the Trap filter is critical because poor design results in lower attenuation of switching frequency components, resonant issues, higher cost, higher power losses, lower efficiency and inductor saturation. The Trap filter design limitations are the switching frequency of VSI, line frequency and the power rating of VSI. The isolation transformer to which the VSI is connected also plays an important role. It is necessary to consider the isolation transformer impedance in the Trap filter design.

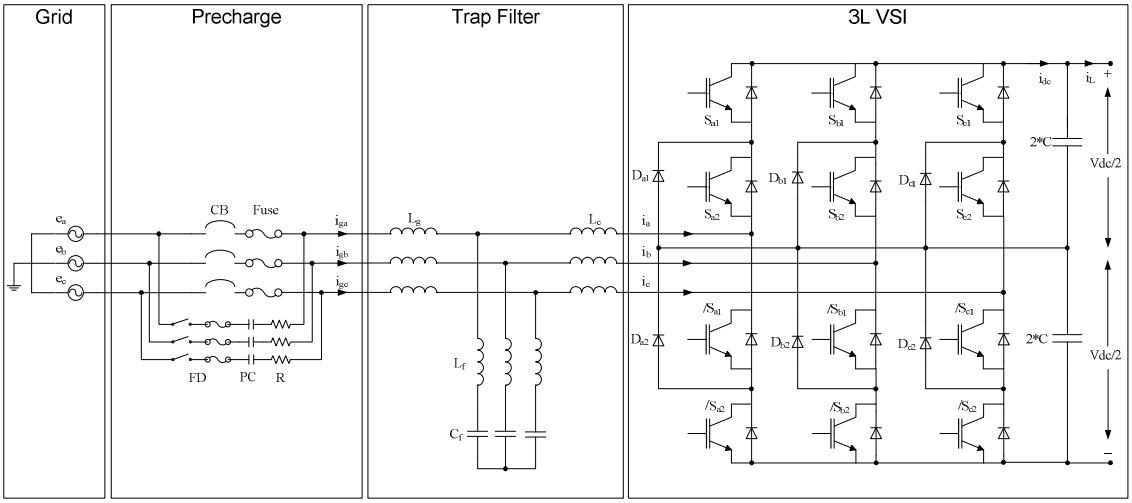

Figure 3.1 3L NPC VSI with Trap filter

The higher the power rating of VSI, the lower the switching frequency used to reduce the switching losses. Usually the switching frequency for 100kW to 1MW VSC varies from 2 kHz to 6 kHz. It is very difficult to design the Trap filter with very low switching frequency because the resonance frequency of the filter must not approach the fundamental frequency as well as the switching frequency. In addition, the size and the cost of L_c will be higher. Isolation transformer impedance also contributes to the resonance frequency of the Trap filter. VSIs are connected to isolation transformers up to a maximum of 20 times rating, providing a wide bandwidth of resonance frequency. Also, the tolerance of L_c contributes to the bandwidth of resonance frequency. The cost of L_c is inversely proportional to allowable tolerances in the inductance value [26]-[28]. The single phase equivalent circuit of the Trap filter is shown in figure 3.2. The damping resistor is ignored in mathematical model.

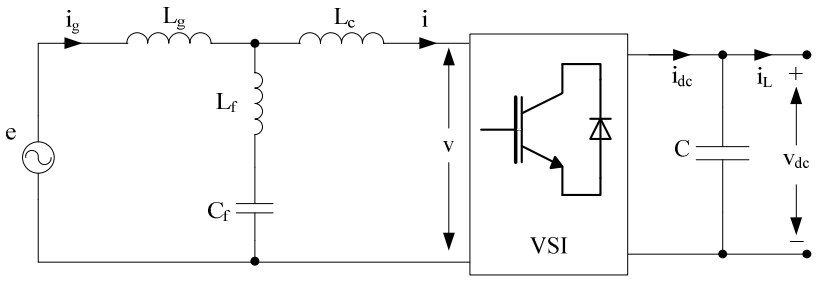

Figure 3.2 Single phase equivalent circuit of VSI with TRAP filter

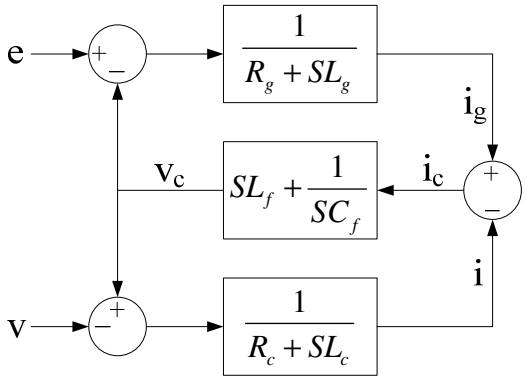

Figure 3.3 Block diagram of TRAP filter

$$\frac{i_g(s)}{e(s)} = \frac{S^2(L_fC_f + L_cC_f) + 1}{S^3(L_gL_2C + L_gL_fC_f + L_cL_fC_f) + S(L_g + L_c)} \tag{1}$$

$$\frac{i(s)}{v(s)} = \frac{S^2(L_fC_f + L_gC_f) + 1}{S^3(L_gL_2C + L_gL_fC_f + L_cL_fC_f) + S(L_g + L_c)} \tag{2}$$

The resonance frequency of the Trap filter with effect of isolation transformer impedance is given by:

$$\omega_{res} = \frac{1}{\sqrt{\dfrac{L_g + L_c}{L_gL_cC + L_gL_fC + L_cL_fC_f}}} \tag{3}$$

The capacitor C_f and the inductor L_f are tuned such that the trap resonant frequency is equal to the switching frequency of the VSI.

$$\omega_{Trap} = \frac{1}{\sqrt{(L_f C_f}} \tag{4}$$

The base impedance of the active converter system can be calculated as $Z_{base} = \frac{V^2}{P}$ and base inductance is $L_{base} = \frac{Z_{base}}{2\pi f}$ and base capacitance is $C_{base} = \frac{1}{2\pi f Z_{base}}$, where P is power rating of active converter, V is line to line voltage and the f is fundamental frequency.

3.2.2 Trap filter design

The Trap filter design algorithm is based on keeping the resonant frequency of the Trap filter including the isolation transformer away from fundamental as well as switching frequency. The L_f and C_f are tuned to the switching frequency. Considering the variation in isolation transformer impedance and the tolerance of the inductor, the Trap filter algorithm is given as below.

- Switching frequency, fundamental frequency, active converter ratings are the input arguments.
- Calculate base impedance, base inductance and base capacitance.
- Based on ripple current requirements, design the converter side inductor L_c, which is usually between 6-9% of base impedance as per [28][29].
- Select the inductor L_f which is small percentage of L_c and calculate the capacitor C_f based on the switching frequency requirements.

- Based on applications, consider the minimum and maximum rating of the isolation transformer to be used for the active converter, and find its impedance and inductance in terms of percentage of the base impedance and inductance.
- Vary the isolation transformer inductance in small steps from minimum to maximum and find the resonance frequency. The resonance frequency must fall between limit lines set per design requirements, which is usually $13f < \omega_{res} < 0.6f_{sw}$, in order to reduce the resonance issue because of the low frequency or switching frequency harmonics. The f is fundamental frequency and F_{sw} is the switching frequency.
- If the above condition does not satisfy, increase L_f in small steps and repeat steps 4-6 until it fulfills the above requirement.
- If there are multiple options available, select the option which gives highest attenuation to the switching frequency component.

It is important to keep low tolerance of L_f and C_f, which provides more predictable filtering for switching frequency components. The above algorithm is implemented in Matlab with rated power of 125kW, line voltage of 480Vrms, fundamental frequency f=60Hz, and switching frequency 4 kHz. The Trap filter component values are calculated in terms of base inductance and base capacitance. In this design we consider the size of the isolation transformer to vary from 125kVA to 3MVA. Typically isolation transformer impedance is 6%, which means if we connect 125kVA active converter to 3MVA transformer, then effective inductance in series with Trap filter is 0.6% of base inductance of the VSI. The program based on the above algorithm provides optimum

value of inductors and capacitors. The transfer function of the Trap filter without damping resistor is given by

$$\frac{i_{(s)}}{e_{(S)}} = \frac{S^2 L_f C_f + 1}{S^3(L_g L_2 C + L_g L_f C_f + L_c L_f C_f) + S(L_g + L_c)} \tag{5}$$

Figure 3.4 shows bode plot of the transfer function (TF) for minimum and maximum value of the isolation transformer inductance. For a minimum inductance equal to 0.6% of base inductance of active converter, the corresponding maximum resonance frequency is 2048Hz and gain is around 122dB, whereas for maximum inductance 6% of base inductance, corresponding minimum resonance frequency is 1633Hz and gain is around 122dB. Attenuation to switching frequency components (4 kHz) is around 180dB.

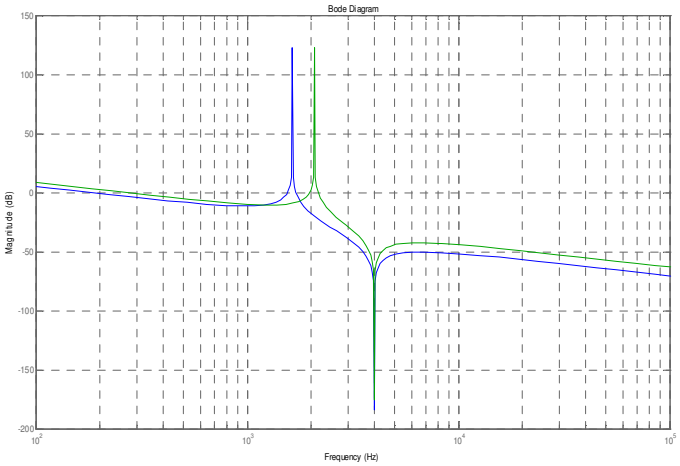

Figure 3.4 Bode plot of TF of Trap filter without damping

Transfer function of the Trap filter with damping resistor is as below.

$$\frac{i_{(s)}}{e_{(S)}} = \frac{S^2 L_f C_f + SC_f R + 1}{S^3(L_g L_c C_f + L_g L_f C_f + L_c L_f C_f) + S^2(L_g + L_c)C_f R + S(L_g + L_c)} \tag{6}$$

Minimum and maximum resonance frequencies of Trap filter and attenuation for switching frequency components are shown in table 3.3 for R=0.01ohm resistor which is good approximation for ESR of capacitors and connection resistance. The corresponding bode plot for transfer function (6) is shown in figure 3.5. Various methods are proposed to damp the resonance in literature [28]-[29]. Table 3.3 shows the trap filter design parameters. It should be noted that with 6% source impedance, Trap filter provides 81dB attenuation to switching frequency components.

125kVA, 480Vrms, 60Hz Active converter with 4kHz switching frequency Trap filter design with R=0.01ohm damping resistor							
Isolation transformer base inductance				Ls min=0.6%	Ls Max=6%	Ls min=0.6%	Lsmax =6%
%L2	%L1	%Lt	%C	Fres max Hz	Fres Min Hz	Atten max dB	Atten min dB
9.0	3.0	0.9	2.5	2048	1633	-73.0	-81.0

Table 3.3. Trap filter parameters

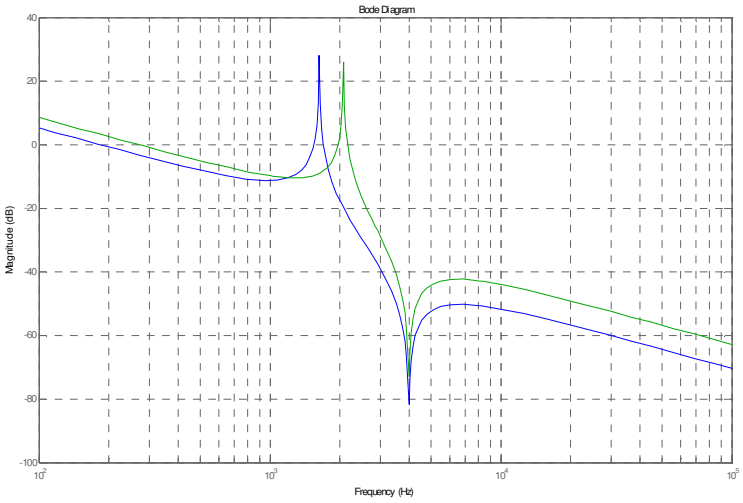

Figure 3.5 Bode plot of Trap filter with damping

3.3 LCL filter analytical model and design algorithm

3.3.1 LCL filter configuration

The LCL filter based 3L VSI is shown in figure 3.6. The L_g and L_c are grid side and VSI side inductances. $Lg=L_t+L_1$, where L_t is the inductance of the isolation transformer and L_1 is inductance of the line side inductor. The capacitor C_f is connected in Y configuration.

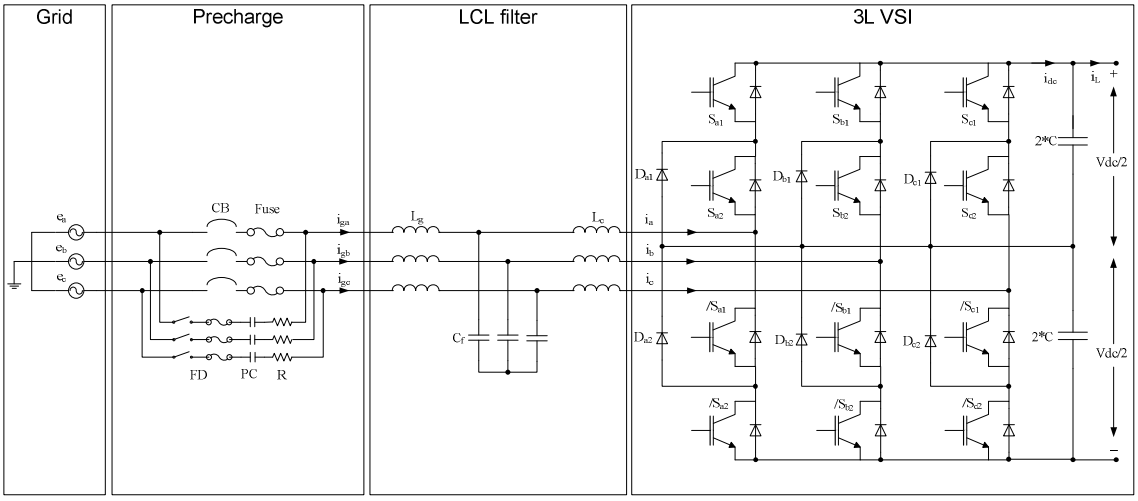

Figure 3.6 3L NPC VSI with LCL filter

The Single phase equivalent circuit of the LCL filter is shown in figure 3.7. The damping resistor is ignored in mathematical model.

$$\frac{i_{g(s)}}{e_{(S)}} = \frac{S^2 L_c C_f + 1}{S[S^2 L_g L_c C_f + (L_g + L_c)]} \tag{7}$$

$$\frac{i_{(s)}}{v_{(S)}} = \frac{S^2 L_g C_f + 1}{S[S^2 L_g L_c C_f + (L_g + L_c)]} \tag{8}$$

The resonance frequency of LCL filter is given by

$$\omega_{res} = \sqrt{\frac{L_g + L_c}{L_g L_c C_f}} \tag{9}$$

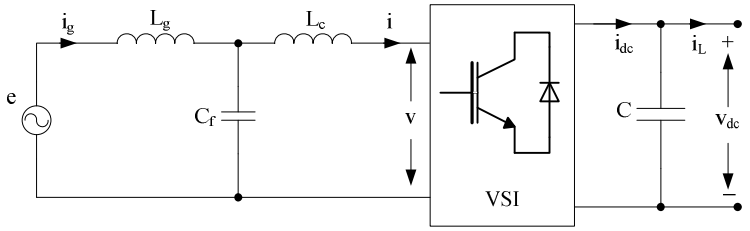

Figure 3.7 Single phase equivalent circuit for VSI with LCL filter

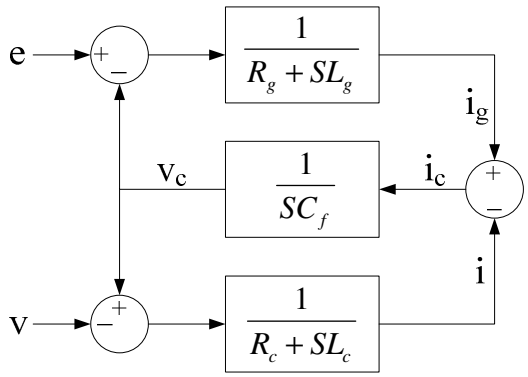

Figure 3.8 Block diagram for the LCL filter

3.3.2 LCL filter design algorithm

The LCL filter design algorithm is also based on keeping the resonance frequency away from fundamental and switching frequency considering the variation in isolation transformer impedance and tolerance of the inductor. The algorithm is given as below:

- Switching frequency, fundamental frequency, VSI ratings are input arguments.
- Calculate base impedance, base inductance and base capacitance.

- Based on the ripple current requirement, design the converter side inductor, which is usually between 6-9% of base impedance as per [28][29].
- Select inductor L_1, which is some percentage of L_c. Total inductance should be less than 12% of base inductance in order to reduce the voltage drop across it. Also the cost of the inductor should be taken into consideration. Start with L_c/L_1 ratio =3, as a good approximation.
- The capacitor decreases power factor. Generally, the maximum desired capacitor is around 5-6% of base capacitance [24]. Start the capacitance at 3% of base capacitance.
- Based on applications, consider the minimum and maximum rating of isolation transformers used for the active converter and find its impedance and inductance in terms of percentage of base impedance and inductance.
- Vary the isolation transformer inductance in small step from minimum to maximum and find the resonance frequency. Resonance frequency must fall between limit lines set as per design requirements which is $13 f < \omega_{res} < 0.6 f_{sw}$.
- If the above condition does not meet the requirements, then increase C_f in small steps and repeat steps 6-7. If necessary reduce the L_c/L_1 ratio and repeat steps 4-7.
- If there are multiple options available, select the option which gives highest attenuation to switching frequency component.

The above algorithm is implemented in Matlab. Using the same power rating as in the Trap filter section, the program gives us three different combinations. The values of highlighted row in table 3.4 are used for simulation and experiment purpose. Cost will be the driving factor for the selection of one of the combinations.

125kVA, 480Vrms, 60Hz Active converter with 4kHz switching frequency LCL filter Design with R=0.01ohm damping resistor						
Isolation transformer base inductance			Ls min=0.6%	Ls Max=6%	Ls min=0.6%	Lsmax =6%
%L2	%L1	%C	Fres max Hz	Fres Min Hz	Atten max dB	Atten min dB
8	3	6	1732	1201	-35	-46
9	3	5	1789	1265	-35	-46
9	3	6	1633	1155	-37	-47

Table 3.4. LCL filter parameters

3.4 Effect of the source impedance

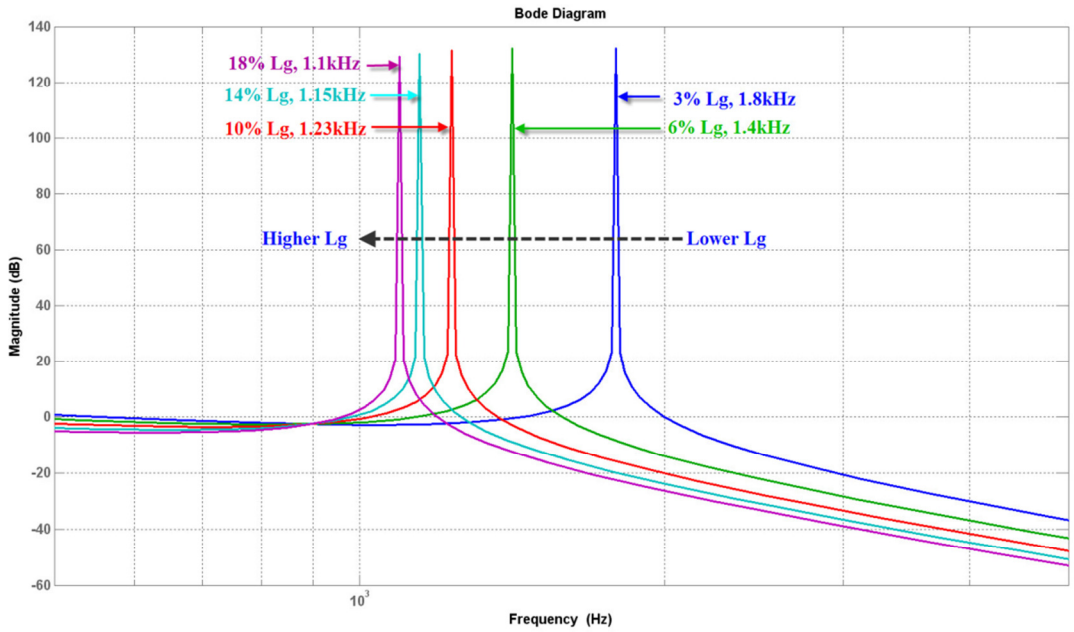

Figure 3.9 Bode plot of LCL filter with different source impedance

The source impedance has significant effects on the behavior of the Trap and LCL filter response. Bode plot of the LCL filter transfer function with different source impedance is shown in figure 3.9. It includes the source impedance as well as grid side inductance (3% L) of the LCL filter. One can observe that as source impedance increases, resonance frequency reduces [25]. If source is more than 20 times VSI rating then source

impedance is negligible compare to the grid side inductance. In this case the resonance frequency is 1.8 kHz. In contrary, if the VSI is connected to generator, in this case the source impedance is almost 5 times the grid side inductor of the LCL filter. The resonance frequency may drop to 1.1 kHz and the effective bandwidth of the control loop reduces significantly. If the control loop parameter is tuned based on just LCL filter without considering the source impedance, for any step change in load, VSI may go to the unstable mode. The information about source impedance is required for better tuning of the VSI control loop [30]-[32].

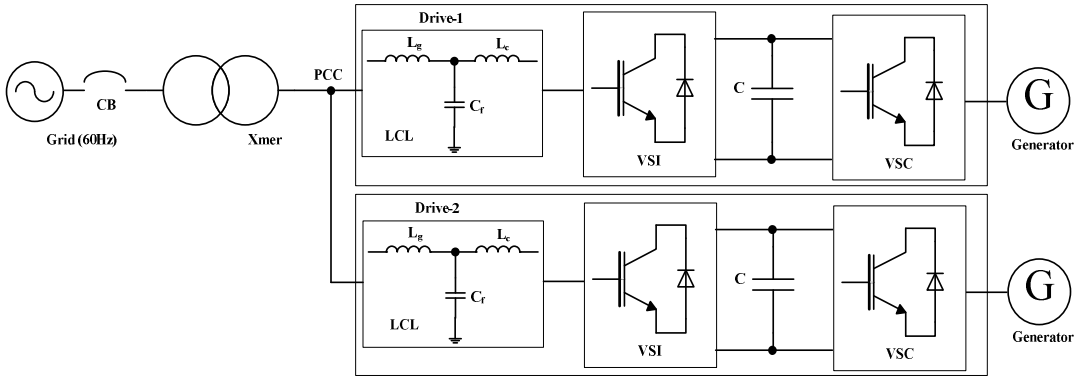

Figure 3.10 VSI's connected at same PCC

Even after considering the source impedance and tune the control loop of the VSI, there are some cases where the VSI control can't avoid resonance. One of the scenarios is shown in figure 3.10 where two drives are connected to the same PCC. One drive's switching frequency is overlapping to other drive's LCL resonance frequency. Active damping control techniques can be used to damp the resonance [33][34][40][41]. The active damping control algorithm is complex; it may pose additional issues if is not implemented properly. The only easy way to alleviate the problem is by adding passive

damping circuit to the unit when a resonance is detected in the system. Passive damping of the LCL filter is discussed in detail later in this chapter.

3.5 Passive damping for LCL filters

The resonance of the LCL filter can be avoided by either an active damping or a passive damping technique. Passive damping is simple, easy to implement and guarantee work for all the time. Heat dissipation and space for the resistors are the only issues when dealing with the passive damping. Active damping requires complex control algorithm with higher sampling rate. Doesn't always guarantee work with all possible scenarios. Sometime active damping has adverse effects on overall control of the VSI. In this section, we will discuss possible topologies for the passive damping, its mathematical model and comparative result of the passive damping technique in terms of bode plot.

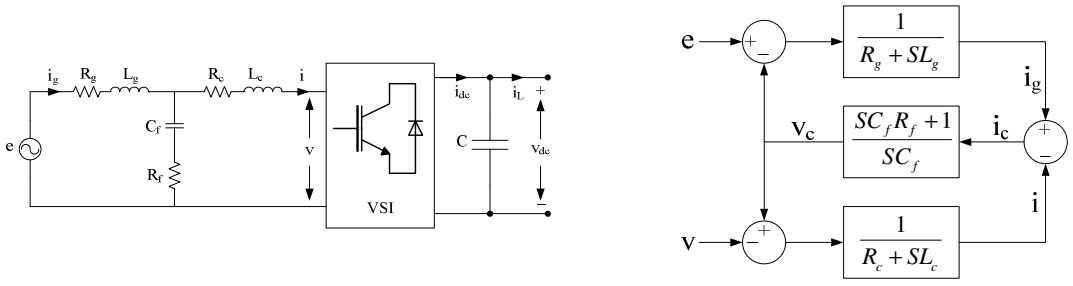

Figure 3.11Block diagram of LCL filter with series damping resistor

The simplest topology for the passive damping is series connected resistor R_f with filter capacitor C_f. The topology and a block diagram of LCL filter with series connected

resistor is shown in figure 3.11. The input and output admittances and transfer function are given by equations (10)-(12).

$$\frac{i_{g(s)}}{e_{(S)}} = \frac{S^2 L_c C_f + S C_f R_f + 1}{S[S^2 L_g L_c C_f + S C_f R_f (L_g + L_c) + (L_g + L_c)]} \tag{10}$$

$$\frac{i_{(s)}}{v_{(S)}} = \frac{S^2 L_g C_f + S C_f R_f + 1}{S[S^2 L_g L_c C_f + S C_f R_f (L_g + L_c) + (L_g + L_c)]} \tag{11}$$

$$\frac{i_{(s)}}{e_{(S)}} = \frac{S C_f R_f + 1}{S[S^2 L_g L_c C_f + S C_f R_f (L_g + L_c) + (L_g + L_c)]} \tag{12}$$

In order to reduce the heat dissipation in series connected resistor, another proposed topology is shown in figure 3.12. The filter capacitors are split in to two different capacitor banks. The C_{f1} is 4% capacitor bank and the C_{f2} is 1% capacitor bank. The damping resistor R_{f2} is connected in series with the C_{f2} capacitor bank. The block diagram of the passive damping technique is shown in figure 3.12. The mathematical model of the admittances and transfer function are given by equations (13)-(15).

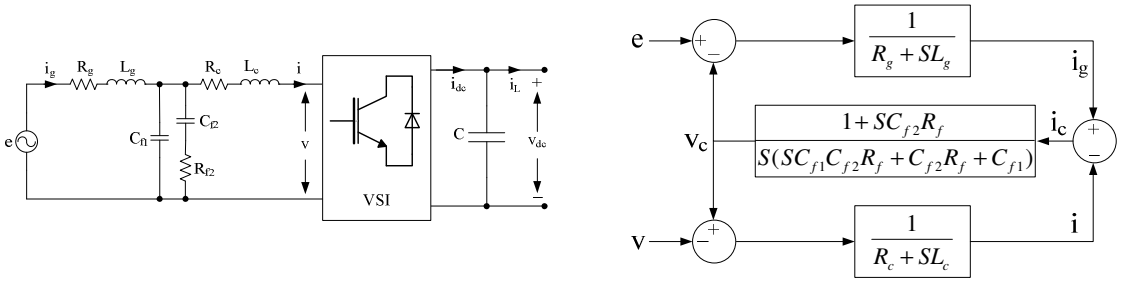

Figure 3.12 Block diagram of LCL filter with Cf1 || [Cf2+Rf] damping

$$\frac{i_{g(s)}}{e_{(S)}} = \frac{S^3 L_c C_{f1} C_{f2} R_f + S^2 L_c (C_{f2} R_f + C_{f1}) + S C_{f2} R_f + 1}{S[S^3 L_g L_c C_{f1} C_{f2} R_f + S^2 L_g L_c (C_{f2} R_f + C_{f1}) + S C_{f2} R_f (L_g + L_c) + (L_g + L_c)]} \tag{13}$$

$$\frac{i_{(s)}}{v_{(S)}} = \frac{S^3 L_g C_{f1} C_{f2} R_f + S^2 L_g (C_{f2} R_f + C_{f1}) + S C_{f2} R_f + 1}{S[S^3 L_g L_c C_{f1} C_{f2} R_f + S^2 L_g L_c (C_{f2} R_f + C_{f1}) + S C_{f2} R_f (L_g + L_c) + (L_g + L_c)]} \quad (14)$$

$$\frac{i_{(s)}}{e_{(S)}} = \frac{S C_{f1} C_{f2} R_f + (C_{f2} R_f + C_{f1})}{S^3 L_g L_c C_{f1} C_{f2} R_f + S^2 L_g L_c (C_{f2} R_f + C_{f1}) + S C_{f2} R_f (L_g + L_c) + (L_g + L_c)} \quad (15)$$

Another possible solution to reduce the heat dissipation in series connected resistor is shown in figure 3.13. The filter capacitor is series connected to parallel combination of a resistor and an inductor. The block diagram of this passive damping technique is shown in figure 3.13. The mathematical model of the transfer function and admittances are given by equations (16)-(18).

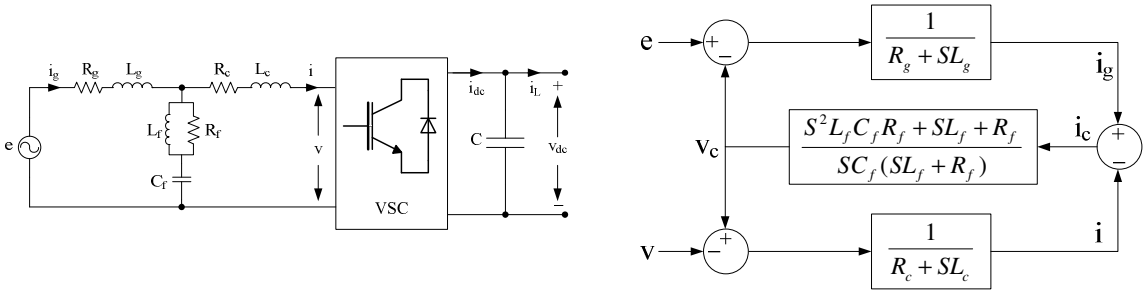

Figure 3.13 Block diagram of LCL filter with Cf+ [Lf || Rf] damping

$$\frac{i_{g(s)}}{e_{(S)}} = \frac{S^3 L_c L_f C_f + S^2 C_f R_f (L_c + L_f) + S L_f + R_f}{S[S^3 L_g L_c L_f C_f + S^2 C_f R_f (L_g L_c + L_g L_f + L_c L_f) + S L_f (L_g + L_c) + R_f (L_g + L_c)]} \quad (16)$$

$$\frac{i_{(s)}}{v_{(S)}} = \frac{S^3 L_g L_f C_f + S^2 C_f R_f (L_g + L_f) + S L_f + R_f}{S[S^3 L_g L_c L_f C_f + S^2 C_f R_f (L_g L_c + L_g L_f + L_c L_f) + S L_f (L_g + L_c) + R_f (L_g + L_c)]} \quad (17)$$

$$\frac{i_{(s)}}{e_{(S)}} = \frac{S^2 L_f C_f R_f + S L_f + R_f}{S[S^3 L_g L_c L_f C_f + S^2 C_f R_f (L_g L_c + L_g L_f + L_c L_f) + S L_f (L_g + L_c) + R_f (L_g + L_c)]} \quad (18)$$

For all the above topologies, bode plots analysis are performed. Figure 3.14 shows the bode plots of the different passive damping techniques with its configuration, resonance frequency and effective damping. It's quite obvious that without damping the LCL resonance peak can go as high as 132dB. With the series connected resistor (C-R), the resonance peak reduces to 30dB and attenuation at switching frequency component (4kHz) is maximum, For (C1||C2+R) and (C+L||R) topologies, the resonance peak remain same -0.2dB. The attenuation of switching frequency component is reduces significantly for (C1||C2+R) topology. The watt loss calculation table is shown below for 125kVA system. Table 3.5 shows that for configurations 1 and 3 the watt losses are very similar but very expensive to implement the configuration 3. The 2nd configuration provides lowest watt loss solution but implementation for delta configuration capacitor bank is very difficult from packaging point of view. Based on resonance damping, attenuation of switching frequency component, cost of implementation and packaging point of view topology 1 provides the best solution except heat dissipation, which can be easily solve by the energy efficient solution provided in next section.

Result for 125kVA system						
Configuration / Value		R	C1	C2 / L	IR (Amp)	Watt
1	C+R	0.4	5%	-	15	90
2	C1||C2+R	8	4%	1% (C2)	2	32
3	L||R +C	0.5	5%	2% (L)	13	84.5

Table 3.5. LCL passive damping technique comparison in terms of watt loss

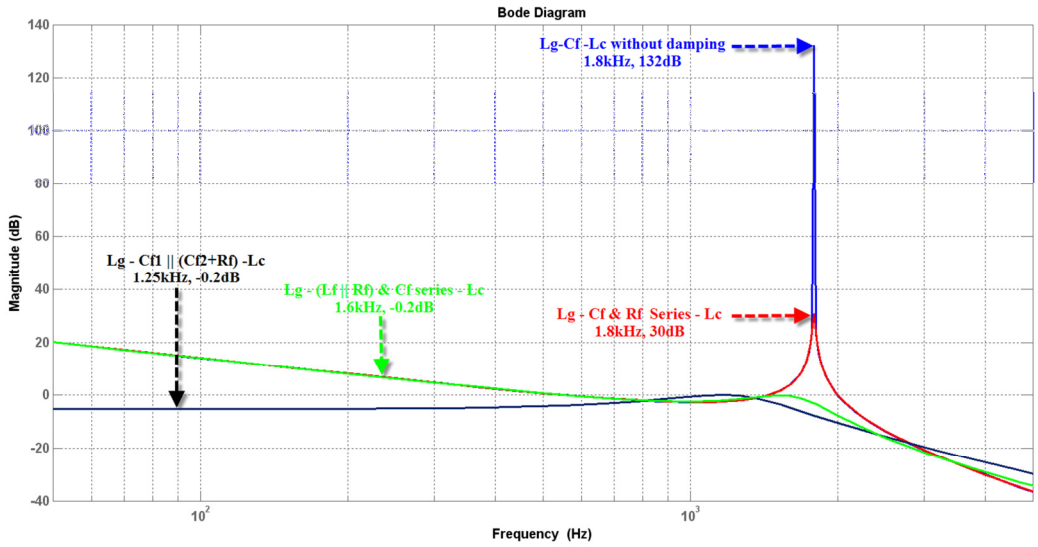

Figure 3.14 LCL passive damping techniques comparison using bode plot

The energy efficient solution is shown in figure 3.15. The SW1 is in normally ON when there is no resonance, connects the filter capacitors in Y configuration without damping resistor. There is no additional watt loss across the resistor. When control system detects the resonance, SW1 allows putting the resistor in series with filter capacitor to help damping the LCL resonance.

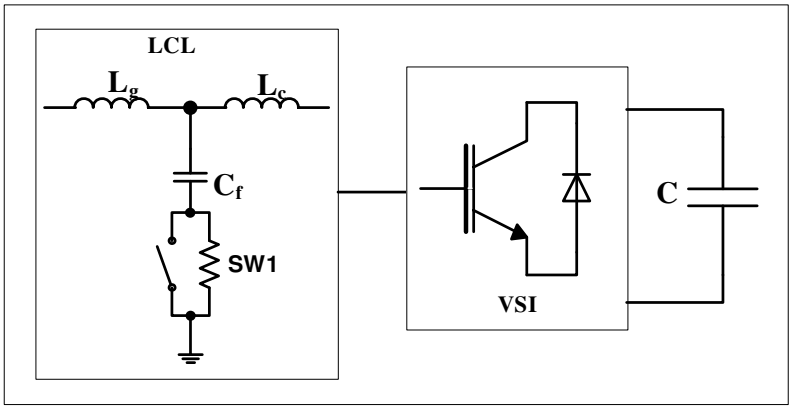

Figure 3.15 LCL damping resistor switching circuit

3.6 Simulation and Experimental results

3.6.1 Simulation result of Trap filter

Voltage source inverter (125kW) connected to 2.5MVA 6% isolation transformer system is simulated using Simplorer software. The Trap filter inductors; capacitor and resistor values are shown in Table 3.3. Input phase to phase voltage and current waveforms are shown in figures 3.16 and 3.17.

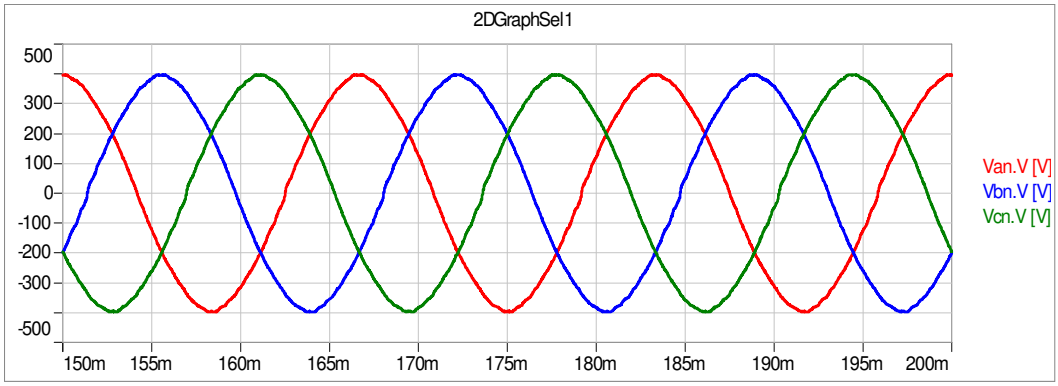

Figure 3.16 Simulation result of Trap filter phase voltage

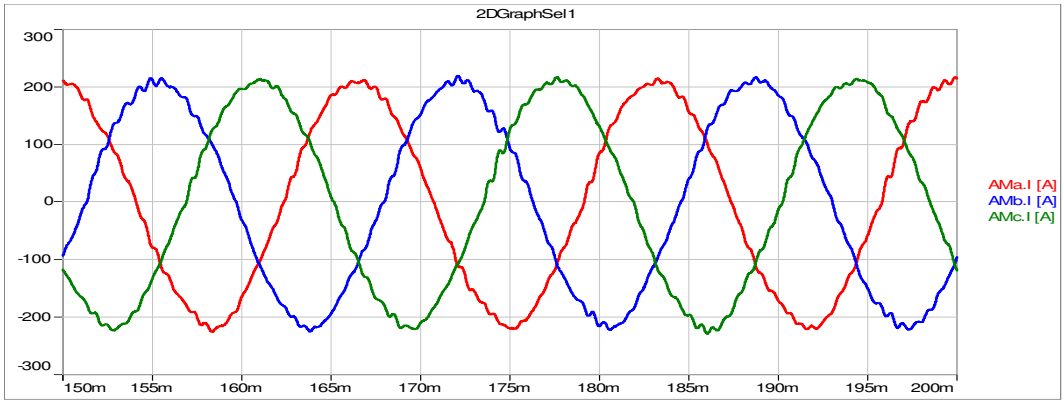

Figure 3.17 Simulation result of Trap filter phase currents

Phase to neutral voltage and phase current FFT are shown in figure 3.18. The THD of phase to neutral voltage is 1.4746% and the TDD is 3.5707%. There is minimum switching frequency component (4kHz) are observed in current FFT compare to 2nd order of switching frequency component (8kHz), this is because Trap filter is tuned for the 4kHz. Trap filter has minimum attenuation effect on 2nd and higher order harmonics of switching frequency components.

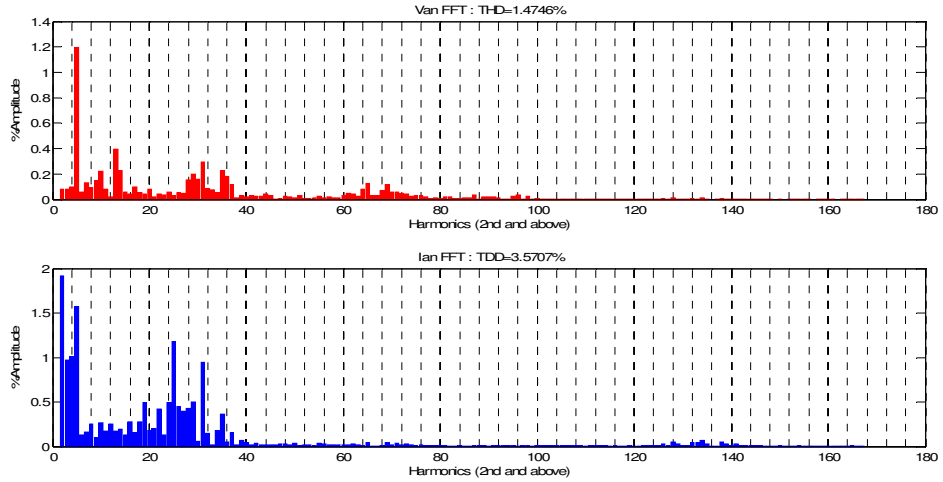

Figure 3.18 Simulation result of Trap voltage and currents FFT

3.6.2 Simulation result of LCL filter

With the same setup as TRAP filter, the LCL system is simulated using Simplorer software. LCL filters inductors, capacitor and resistor values are shown in table 3.4. Input phase to phase voltage and current waveforms are shown in figure 3.19 and 3.20.

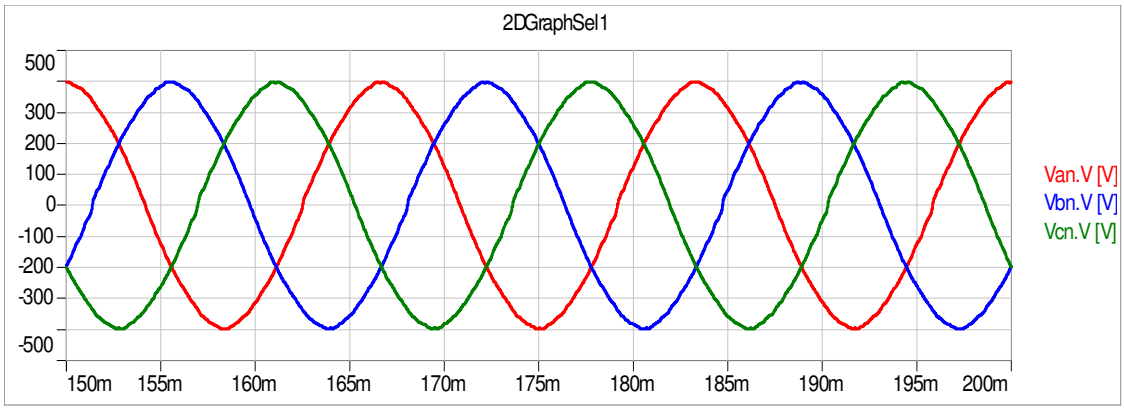

Figure 3.19 Simulation result of LCL filter phase voltage

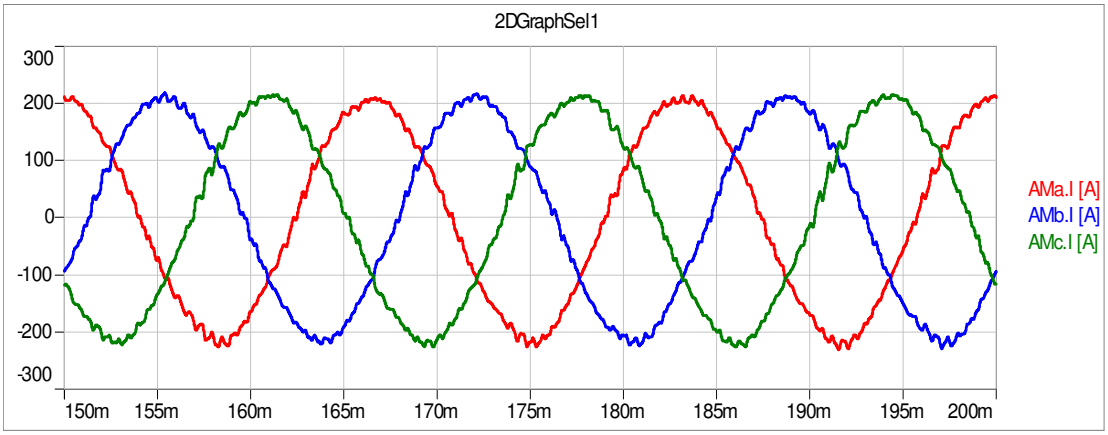

Figure 3.20 Simulation result of LCL filter phase currents

The phase to neutral voltage and phase current FFT are shown in figure 3.21. The THD of phase to neutral voltage is 1.4746% and the TDD is 4.0119%. In phase current FFT graph, switching frequency components (4kHz) is very high compare to Trap filter. The 2^{nd} and higher order harmonic components are attenuated significantly compare to Trap filter. It shows that LCL filter provides better attenuation for electro-magnetic interference at low frequency range (<500 kHz).

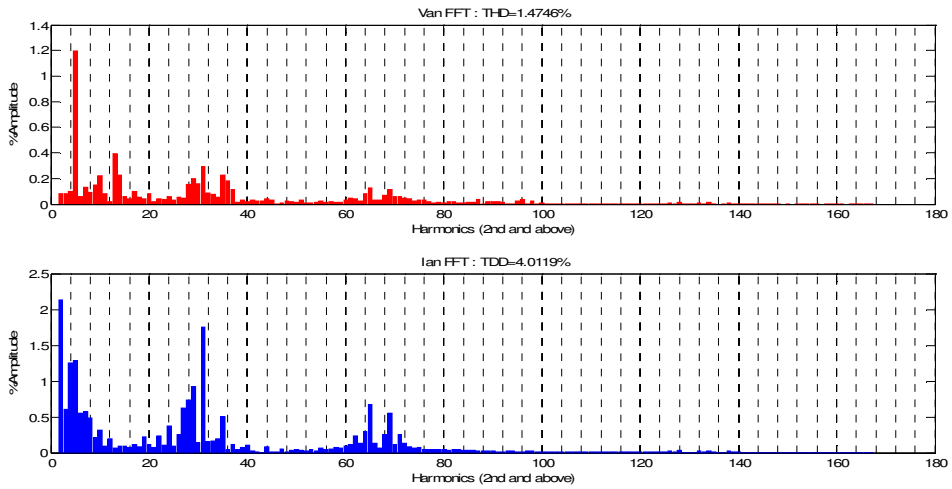

Figure 3.21 Simulation result of LCL filter voltage and currents FFT

3.6.3 Experimental result of Trap filter

Figure 3.22 and 3.23 shows the experimental result of the 125kW active converter with Trap filter ran at full load and FFT analysis of phase voltage and line current of phase R. The measured voltage THD is 1.812% and the current TDD is 5.262%.

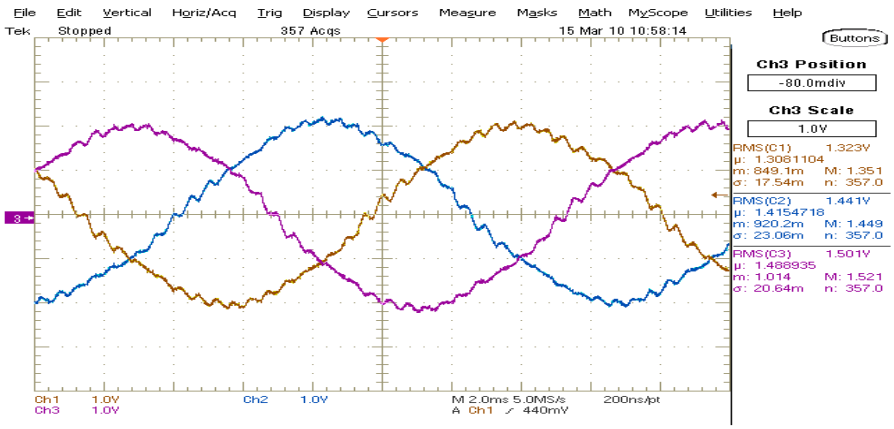

Figure 3.22 Trap filter full load phase currents

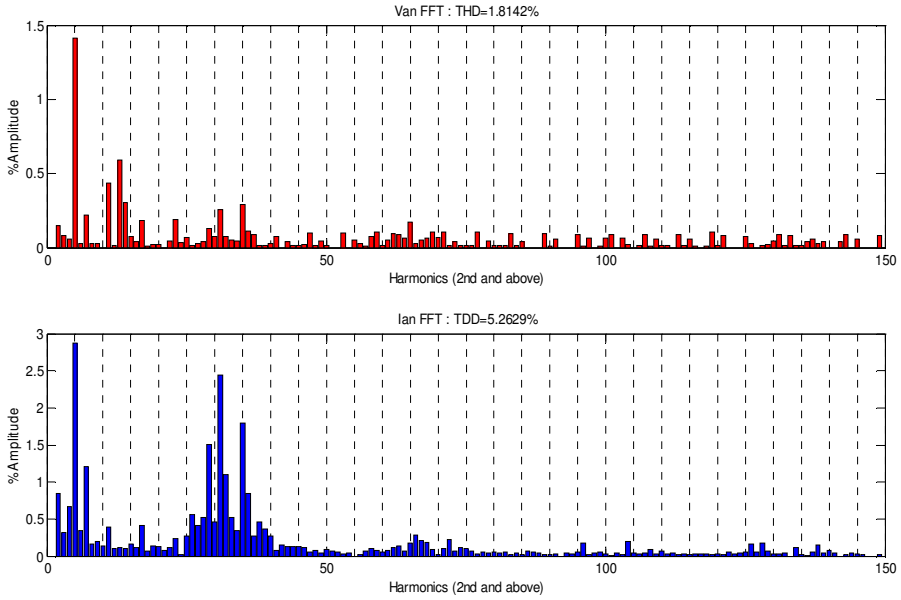

Figure 3.23 Trap filter FFT of phase R voltage and phase current

3.6.4 Experimental result LCL filter

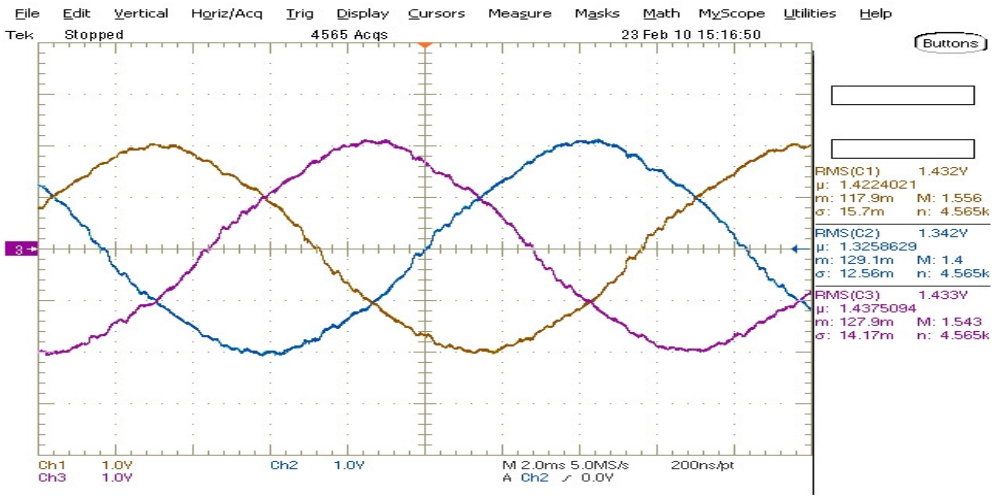

Figure 3.24 LCL filter full load measurement of phase currents

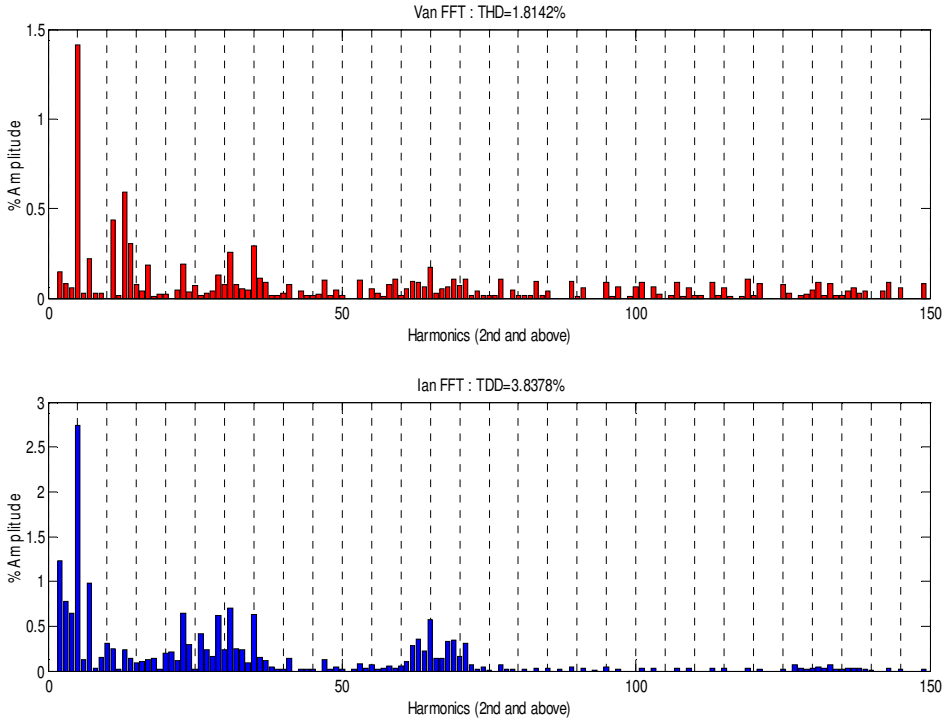

Figure 3.25 LCL filter FFT of phase R voltage and phase current

Figure 3.24 and 3.25 shows the experimental result of the 125kW active converter with LCL filter ran at full load and FFT analysis of phase voltage and the line current of phase R. The measured voltage THD is 1.814% and the current TDD is 3.837%. The attenuation of the switching frequency component (4 kHz) is not as high as Trap filter but the higher attenuation of the 2nd order switching frequency component (8 kHz) is achieved compare to Trap filter. The drive is connected to a 2.5MV transformer in both cases. The I_{SC}/I_L ratio is 139 which means it requires less than 15% current TDD to meet the IEEE standard 519 specification. The THD and the TDD results are higher than simulation results because the base line voltage measurements had higher fifth harmonic

components. The experimental results of TRAP and LCL filters show that both filters pass IEEE 519 requirements.

3.7 Comparison of Trap and LCL filters

The Trap filter provides better attenuation of the switching frequency components. It provides better performance for a generator as a source and during line dip conditions. The Trap filter is effective for audible noise reduction when it is connected to an isolation transformer. A 3% reactor could be optional depending upon application. The Trap filter has less attenuation at higher frequency. The Trap filter required very tight tolerance of the *LC* tuned circuit to effectively filter the switching frequency component. The cost of the *LC* tuned circuit will be higher. The LCL provides higher attenuation at higher frequency and will be effective in electromagnetic compliance. Higher L and C tolerance will be acceptable. The LCL is not as effective as Trap filter for switching frequency component filtering.

3.8 Conclusion

In this chapter the TRAP and the LCL filters mathematical models are discussed in detail. The optimum design algorithms for the TRAP and the LCL filters are presented. The effects of the grid impedance or isolation transformer are discussed in detail and used the information to design the TRAP and the LCL filters. The algorithms are implemented in MATLAB. The resonance issues with LCL filter are discussed in depth and different topologies for the passive resonance damping for the LCL filter are presented. The pros

and cons of each passive damping topology are compared. The TRAP and the LCL filters for 125kW converters are designed using optimum design algorithm. The design has been tested in simulation and with an experimental setup. Simulation result as well as experimental result shows that both filters meet the IEEE 519 voltage THD and current TDD limits. In next chapter we will discussed the VSI for the MVDC application. Selection of a topology and the control algorithm is presented in detail.

4. Voltage source inverter

4.1 Introduction

With advancement in silicon technology, the higher voltage self-commutated switching devices are available in market, which enables to supports higher power medium voltage converters for the MVDC system. Depending up on the dc-link energy storage component, the medium voltage converters are classified into a current-source and voltage-source topologies. The voltage source inverters (VSI) are increasingly popular for the MVDC application. The VSI can be further classified in multiple topologies like multi-level converters, flying capacitors and cascade H-bridge [37]-[39]. The VSI operates with higher switching frequencies generally in range of 2 kHz – 4 kHz, reduces the input LCL filter size. This leads to reduce the overall size of the power conversion unit.

4.2 Selection of topology

The high power converter classification is shown in figure 4.1. The cycloconverter is fall under the bi-direction conversion without DC link. The indirect conversion have DC link between the inverter and the converter. The current source converters have more harmonics and lower power factor compare to voltage source inverters. The voltage source inverters are further classified in to multi-level inverters and high power 2-Level inverters. The multi-level voltage source converters are classified

into three different categories like 3-level neutral point clamp (NPC), cascade H-bridge (CHB) and Flying capacitors. The control for the flying capacitor topology is complex compare to 3-level NPC converter. In addition, it's more expensive because low switching frequency makes clamping capacitor large and an excessive number of capacitors used for the clamping.

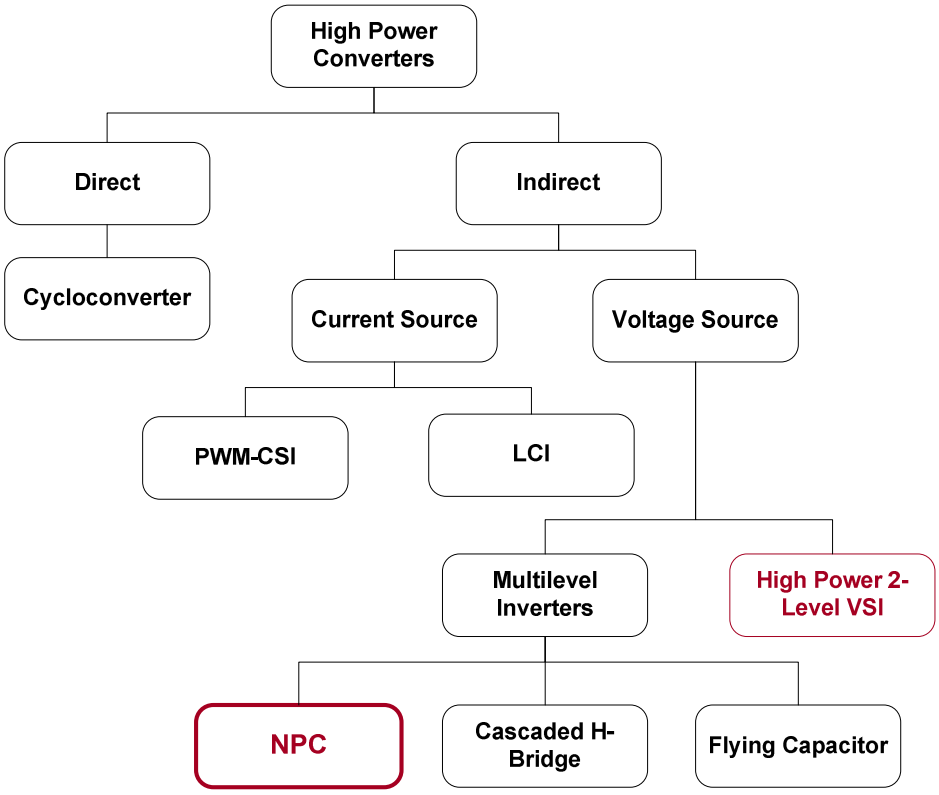

Figure 4.1 Classification for high power converters

The disadvantages of the cascade H-bridge are the separate dc sources and a nonstandard transformer. The 3-level NPC provides higher quality output voltage and current waveform results in reduced output filter size and cost compare to two level inverter. Only half of the DC bus voltage has to be switched leads to reduced switching losses

compare to 2-level inverter. The control loop is easy to implement. With the availability of IGBT modules of 3.3kV, 4.5kV and 6.6kV rating makes the 3-Level NPC topology very popular for MVDC (2.3kV-4.6kV) applications [37].

Summary of the advantages of the 3L NPC as below:

- **No dynamic voltage sharing problem.** Each of the switches in the NPC inverter withstands only half of the total dc voltage during commutation.
- **Static voltage equalization without using additional components.** The static voltage equalization can be achieved when the leakage current of the top and bottom switches in an inverter leg is selected to be lower than that of the inner switches.
- **Low THD and *dv/dt*.** The waveform of the line-to-line voltages is composed of five voltage levels, which leads to lower THD and *dv/dt* in comparison to the two-level inverter operating at the same voltage rating and device switching frequency.

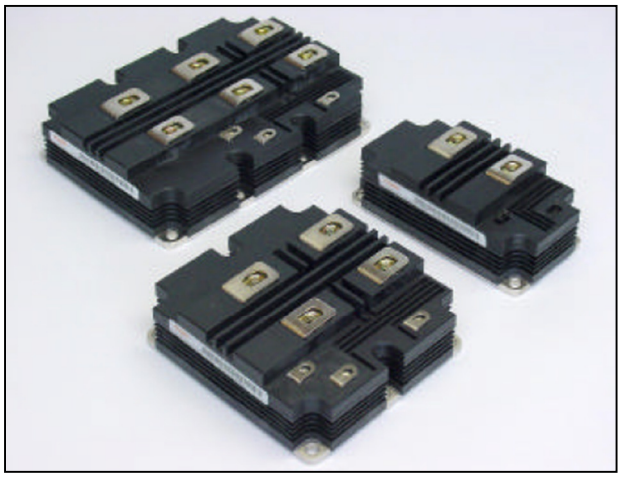

Figure 4.2 2.2kV- 6.6kV rated IGBT from ABB

4.3 Three level NPC voltage source inverter

The 3-level NPC topology is shown in figure 4.3. There are four switches per leg. There are two additional diodes per leg, which link the midpoint of the indirect series connection of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point N and enables the three level characteristic of the topology.

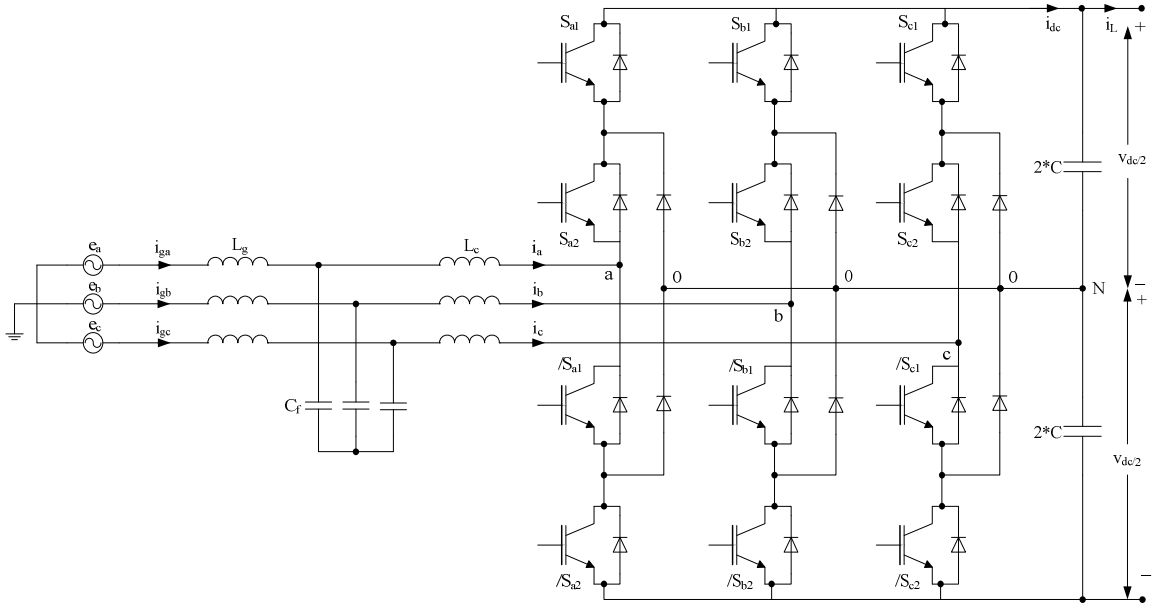

Figure 4.3 3-Level NPC topology for VSC/VSI with LCL filter

Output voltage (V_{aN})	Gate signal S_{a1}	Gate signal S_{a2}	Switching States (S_a)
$+V_{dc}/2$	1	1	+
0	0	1	0
$-V_{dc}/2$	0	0	-

Table 4.1. 3-Level NPC switching states (Phase a)

The two pairs of switches of one leg receive inverted gate signals S_{ak} and $/S_{ak}$ (k=1,2). Table 4.1 shows the switching states of one phase leg. There are there different switching state per phase which is related to +Vdc/2, 0 and –Vdc/2 voltage across switches. Combining the states of all three phases, the 3L NPC-VSI features total number of switching state equals to $L^3 = 3^3 = 27$ switch states, where *L* is the number of voltage levels of $V_{xN}(x = a, b, c)$. The different switch states can be represented in the complex $\alpha-\beta$ frame, simply by calculating the space vector ($\mathbf{V}_s$) associated to each switching state is given by the equation below. Detail description of all possible 27 switching states and voltage space vector are presented in [38]-[39]. Note that some switching states have redundant space-vector representations. Generally, modulation methods used for the 3-level NPC are either carrier based sine-triangular modulation or space vector modulation. The voltage space vector for 3L NPC is given by equation (2)

$$V_s = \frac{2}{3}\left(V_{aN} + aV_{bN} + a^2 V_{cN}\right) \tag{1}$$

$$V_s = \frac{2}{3}\left(S_a \frac{V_{dc}}{2} + aS_b \frac{V_{dc}}{2} + a^2 S_c \frac{V_{dc}}{2}\right) \tag{2}$$

Where $a = e^{\frac{2\pi}{3}i}$

The fundamental component of the inverter phase voltages satisfies

$$V_{aN} = V_{bN} = V_{cN} = m_a \frac{V_{dc}}{2} \qquad 0 \le m_a \le 1 \tag{3}$$

And thus the line voltages satisfy

$$V_{ab1} = V_{bc1} = V_{ca1} = m_a \sqrt{3} \frac{V_{dc}}{2} \qquad 0 \le m_a \le 1 \tag{4}$$

Where $0 < m_a \leq 1$, is the linear operating region. To further increase the amplitude of the load voltages, the over modulation operating region can be used by further increasing the modulating signal amplitudes ($m_a > 1$), where the line voltages range in

$$\sqrt{3}\frac{V_{dc}}{2} < V_{ab1} = V_{bc1} = V_{ca1} = \frac{4}{\pi}\sqrt{3}\frac{V_{dc}}{2} \qquad m_a > 1 \tag{5}$$

In addition, modulating signals could be improved by adding a third harmonic (zero sequence), which will increase the linear region up to $m_a = 1.15$.

$$0 \leq m_a = \frac{V_{aN}}{\frac{V_{dc}}{2}} \leq 1.15 \tag{6}$$

4.3.1 Gate pulse generation for 3L NPC voltage source inverter

Figure 4.4 shows the simulation model in Matlab Simulink which generates the 3L NPC gate pulses. The gate pulse pattern chart is also provided in the figure 4.4. The SPWM in three-level inverters uses a sinusoidal set of modulating signals (*vca*, *vcb*, and *vcc* for phases *a*, *b*, and *c*, respectively) and $N - 1 = 2$ triangular type of carrier signals ($v1$ and $v2$) as illustrated in figure 4.5. According to figure 4.5, switch $S1a$ is either turned on if $vca > v1$ or off if $vca < v1$, and switch $S1b$ is either turned on if $vca > v2$ or off if $vca < v2$. Additionally, the switch $/S1a$ status is obtained as the opposite to switch $S1a$, and the switch $/S1b$ status is obtained as the opposite to switch $S1b$.

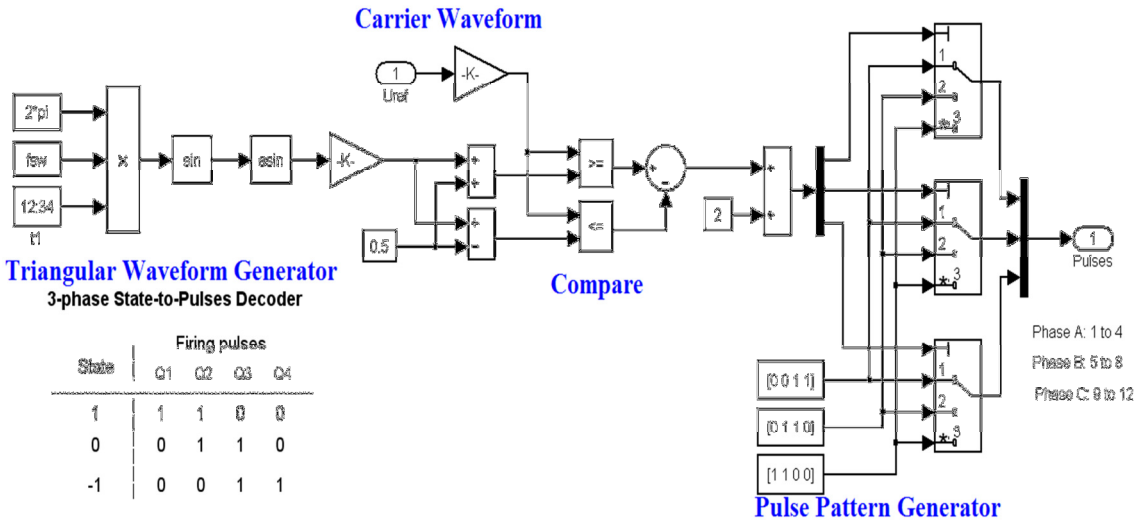

Figure 4.4 Simulation model of 3L NPC gate pulse generator

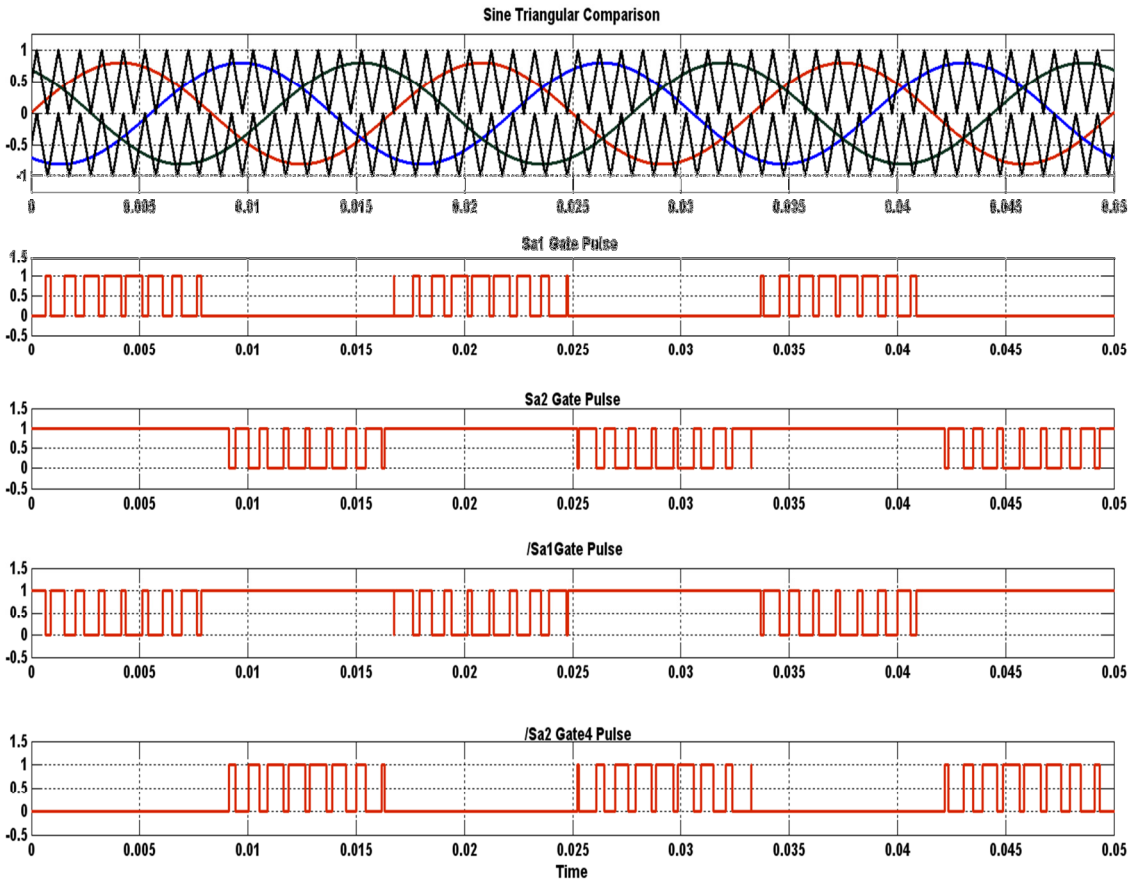

Figure 4.5 Simulation result of carrier Vs control & pulse generation

For the MVDC application, 3-level NPC power devices are switched at frequency between 2-3 kHz. It will introduce higher order harmonics when directly connect to grid without filter leads to power quality issues. Either LCL or Trap filter is used to avoid power quality issue. Both filters are able to meet the IEEE 519 low harmonic solution. Trap filter is series L-C tuned circuit designed to filter out the switching frequency and 2^{nd} order switching frequency of the VSI. The LCL filter is shown in figure 4.3 has VSI side inductor, capacitor and grid side inductor. It is designed to filter all higher order harmonics, not only the switching frequency and the 2^{nd} order switching frequency. The VSI side inductor value is selected based on the ripple current requirements. The capacitor is selected based on % reactive power absorb under rated condition. The grid side inductor value is selected based on how much attenuation required at switching frequency. The step by step design algorithm as well as pros and cons for both LCL and Trap filters are presented [40] and discussed in previous chapter. Figure 4.6 shows single phase equivalent 3L NPC topology with LCL filter without damping.

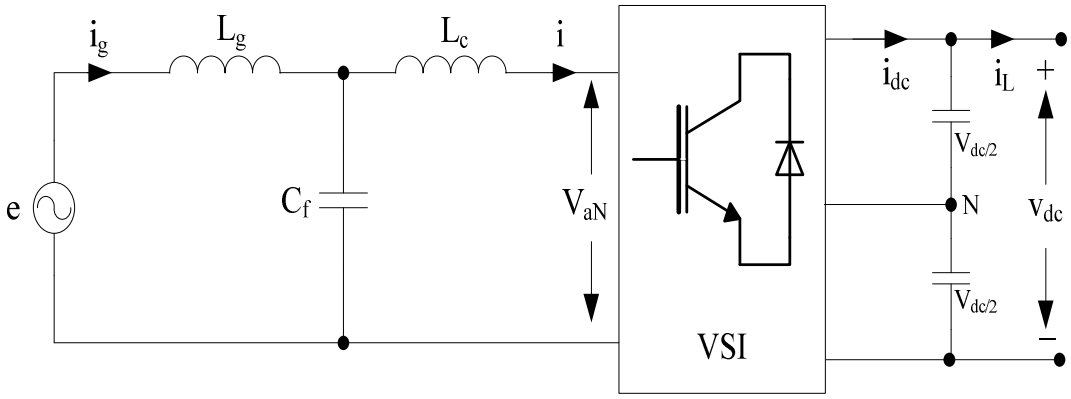

Figure 4.6 Single phase equivalent of 3L VSI with LCL filter

4.4 Control technique for 3L NPC VSI

4.4.1 Constant DC bus voltage control

The VSI's in proposed MVDC system shown in figure 4.3 can be control with different strategies. The VSI can either control the DC bus of the system or direct active and reactive power control to the grid. The VSI's also can be control such that it provides the frequency droop support and voltage droop support. For all the different control techniques, mathematical model of balanced three-phase VSI system can be defined using following equations, where the filter capacitor is neglected and L represent the total inductor ($L=L_g+L_c$) and R represent the total equivalent series resistance of the inductors ($R=R_g+R_c$) [41][42].

$$e_a = L\frac{di_a}{dt} + Ri_a + v_a \tag{7}$$

$$e_b = L\frac{di_b}{dt} + Ri_b + v_b \tag{8}$$

$$e_c = L\frac{di_c}{dt} + Ri_c + v_c \tag{9}$$

For DC output side of the VSI, current equation is written as

$$C\frac{dV_{dc}}{dt} = i_{dc} - i_L \tag{10}$$

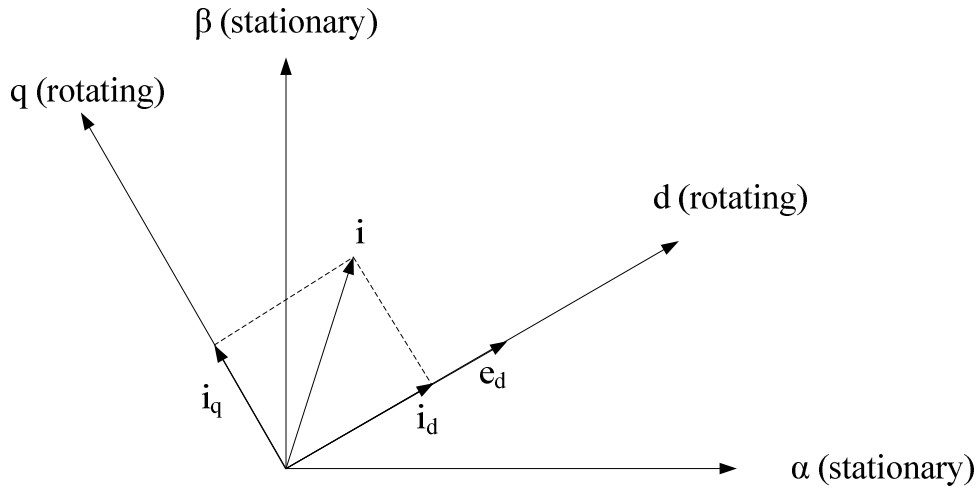

Figure 4.7 Vector diagram of VSI system

With application of Clarke and Park transformation, equation (7) – (9) can be represented with d-q components in the synchronous d-q coordinates rotating at constant angular speed of the grid voltage as (11)-(12):

$$e_d = L\frac{di_d}{dt} - \omega L i_q + R i_d + v_d \tag{11}$$

$$e_q = L\frac{di_q}{dt} + \omega L i_d + R i_q + v_q \tag{12}$$

For the reference frame synchronized to the mains supply leads to e_q=0, the equations (11) and (12) can be written as below

$$v_d = -L\frac{di_d}{dt} - R i_d + \omega L i_q + e_d \tag{13}$$

$$v_q = -L\frac{di_q}{dt} - R i_q - \omega L i_d \tag{14}$$

Equations (13) and (14) coupled with each other. The PI type current controller equation (13) and (14) can be given as below. The current control forms the inner loop where as the voltage control will form the outer loop.

$$v_d = -\left(K_p + \frac{K_i}{S}\right)(i_{dref} + i_d) + \omega L i_q + e_d \tag{15}$$

$$v_q = -\left(K_p + \frac{K_i}{S}\right)(i_{qref} + i_q) - \omega L i_d \tag{16}$$

$$i_{dc} = i_L + C\frac{dV_{dc}}{dt} \tag{17}$$

The DC bus voltage is controlled using the VSI side dc current. For the voltage control loop the equation (17) can be shown as in equation (18)

$$i_{dref} \approx i_{dc} - i_L = \left(K_p + \frac{K_i}{S}\right)\left(V_{dc\,ref} - V_{dc}\right) \tag{18}$$

The analysis of a control loop is easy if equations (15) and (16) are assume decoupled and consider single phase control loop of VSI with LCL filter is shown in figure 4.8. In this figure, $K_p \frac{1+sT_i}{sT_i}$ is the transfer function of current loop PI regulator, $\frac{K_{pwm}}{1+s\frac{T_s}{2}}$ is the transfer function of PWM module. In figure 4.8 filter with R-C series passive damping technique is considered [31]-[34].

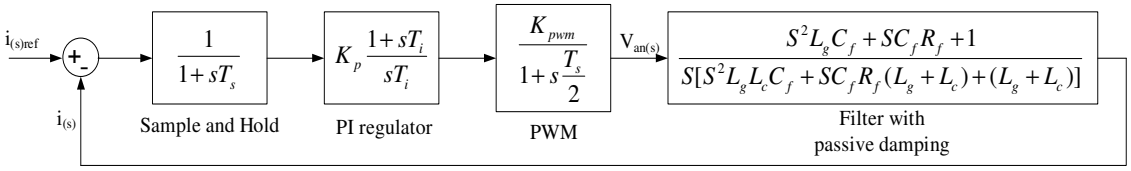

Figure 4.8 Block diagram of VSI with LCL filter current control

Analysis of single phase equivalent control loop is performed using Matlab Simulink control design tool as shown in figure 4.9. With tuned PI regulator, the step response of the system and the bode plot are shown in figure 4.10 and figure 4.11. Analysis shows that the steady state error is less than 2% and settling time is 3.4 msec. The system is stable with the passive damping used for LCL filter. The approximate minimum gain margin of the system is about 20dB whereas; minimum phase margin of the system is about 120 degree.

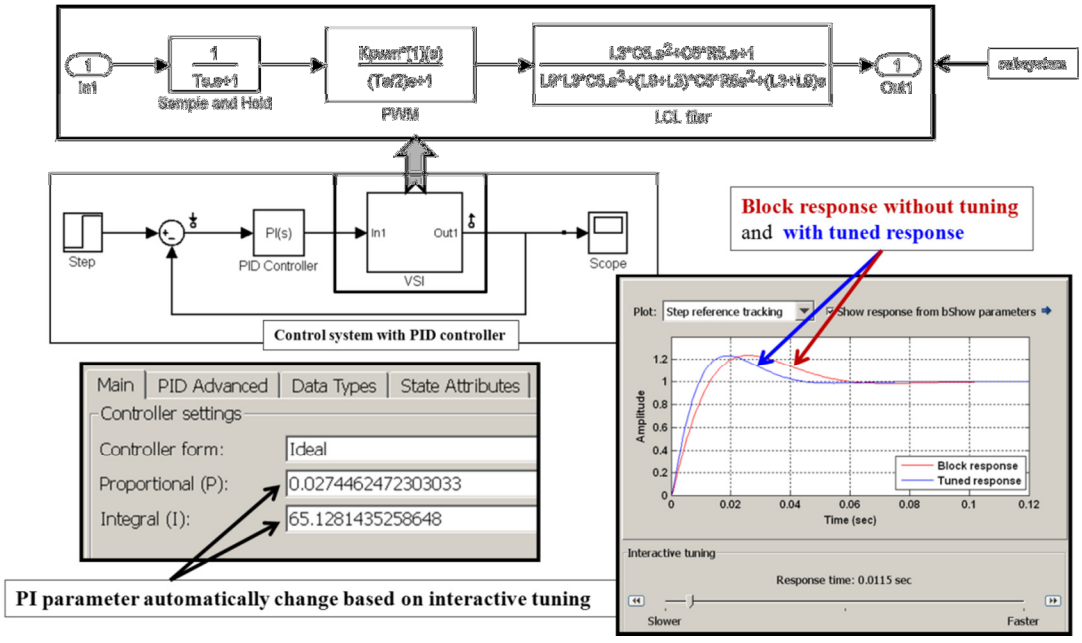

Figure 4.9 Control loop analysis using control design toolbox

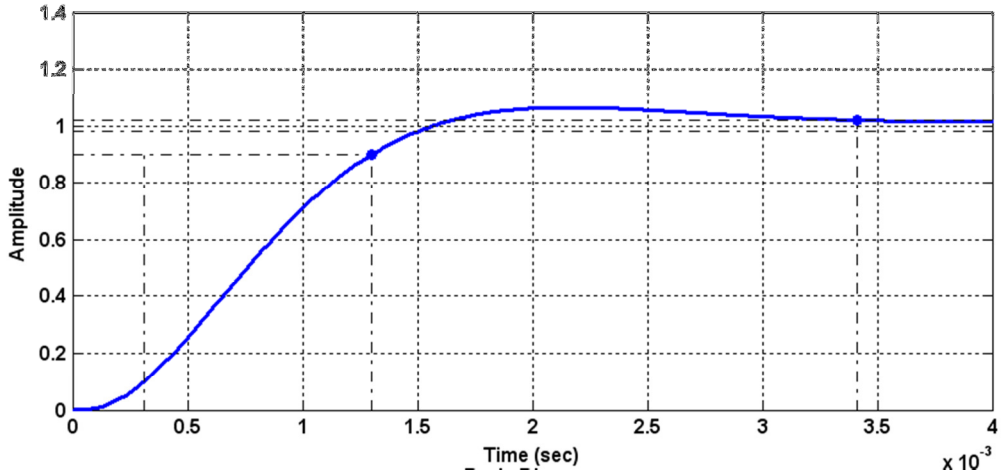

Figure 4.10 Step response of VSI current control loop

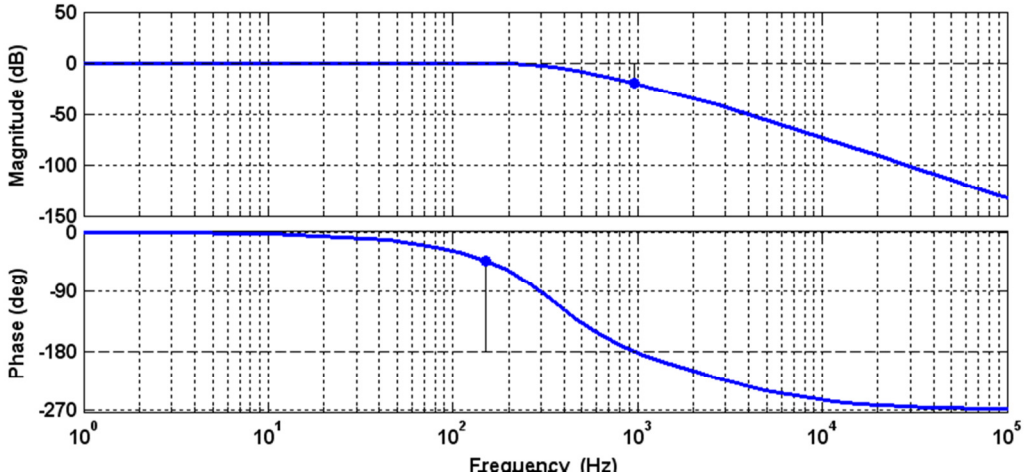

Figure 4.11 Bode plot of the of VSI with LCL filter current control

Figure 4.12 shows the control diagram of the VSI with constant DC bus voltage control. The reference angle is generated from the three phase line voltage using PLL circuit. The transformation block converts the three phase voltages and currents into synchronous reference frame voltages and currents. I_{dref} current command is generated using PI voltage regulator, which regulate the DC bus voltage. Generally for unity power factor

I_{qref} is set to zero. The current controller is implemented using equations (15) and (16). The output of the current control regulator is feed to DQ-ABC transformation block and space vector modulation block respectively. The gate signals are feed to the IGBT of the VSI. Simulation and experimental results are provided in section 4.5 and 4.6.

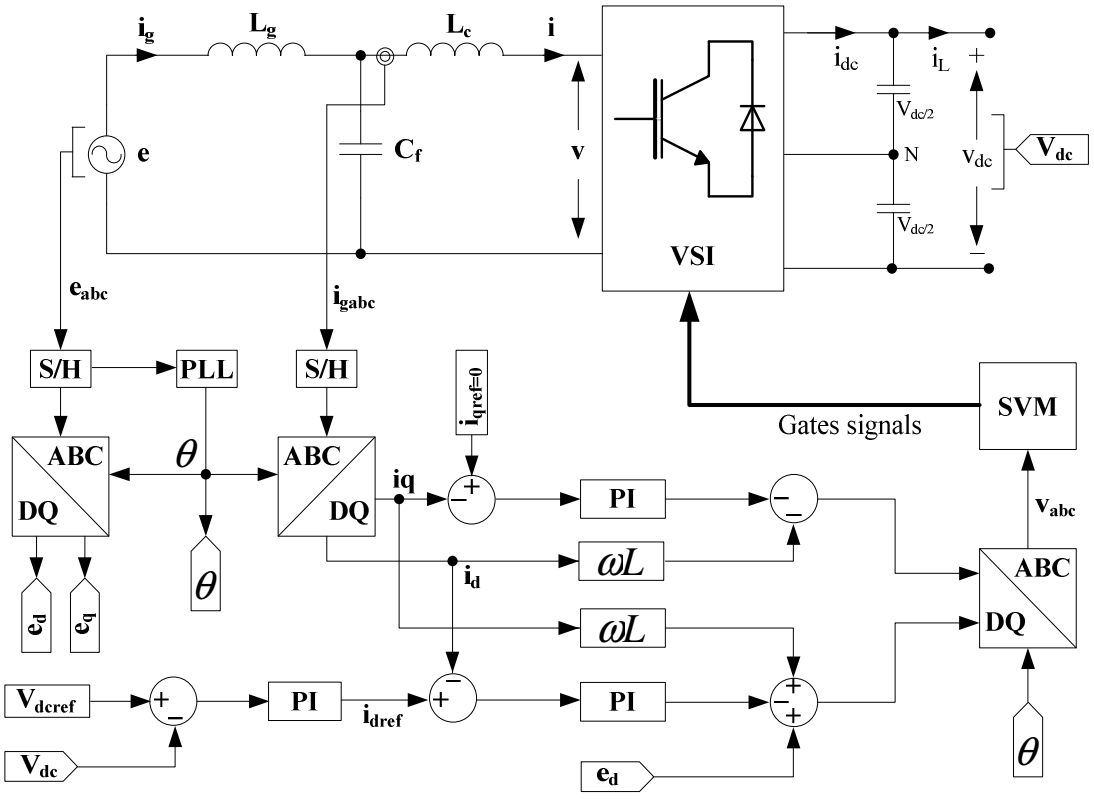

Figure 4.12 Control diagram of constant DC bus voltage control

4.4.2 Active and reactive power control

In VSI based MVDC system, direct control of active and reactive power can be easily implement by decouple of active and reactive power component. The total power of the system is given by equation (19).

$$S = e_s I_s^* \tag{19}$$

$$S = (e_d + je_q)(i_d + ji_q) \tag{20}$$

For reference frame synchronized to mains supply e_q =0, the equation (20) can be shown as below.

$$P = re(S) = e_d i_d \tag{21}$$

$$Q = im(S) = -je_d i_q \tag{22}$$

The direct power control equations derived from the current controller equations (15)-(16) as below.

$$v_d = -\left(K_p + \frac{K_i}{S}\right)(p_{ref} + p) - \omega L q + e_d \tag{22}$$

$$v_q = \left(K_p + \frac{K_i}{S}\right)(q_{ref} + q) - \omega L p \tag{23}$$

Figure 4.13 shows the control diagram of VSI with direct active and reactive power control. The control is very similar to the constant DC bus voltage control except use of active and reactive power reference. The direct active reactive power control in conjunction with constant DC bus voltage control is widely used in the DC distribution system. The constant DC bus voltage control try to keep the system bus voltage constant

whereas the direct active reactive power control will determine the power flow based on the supply and demand matrix [29].

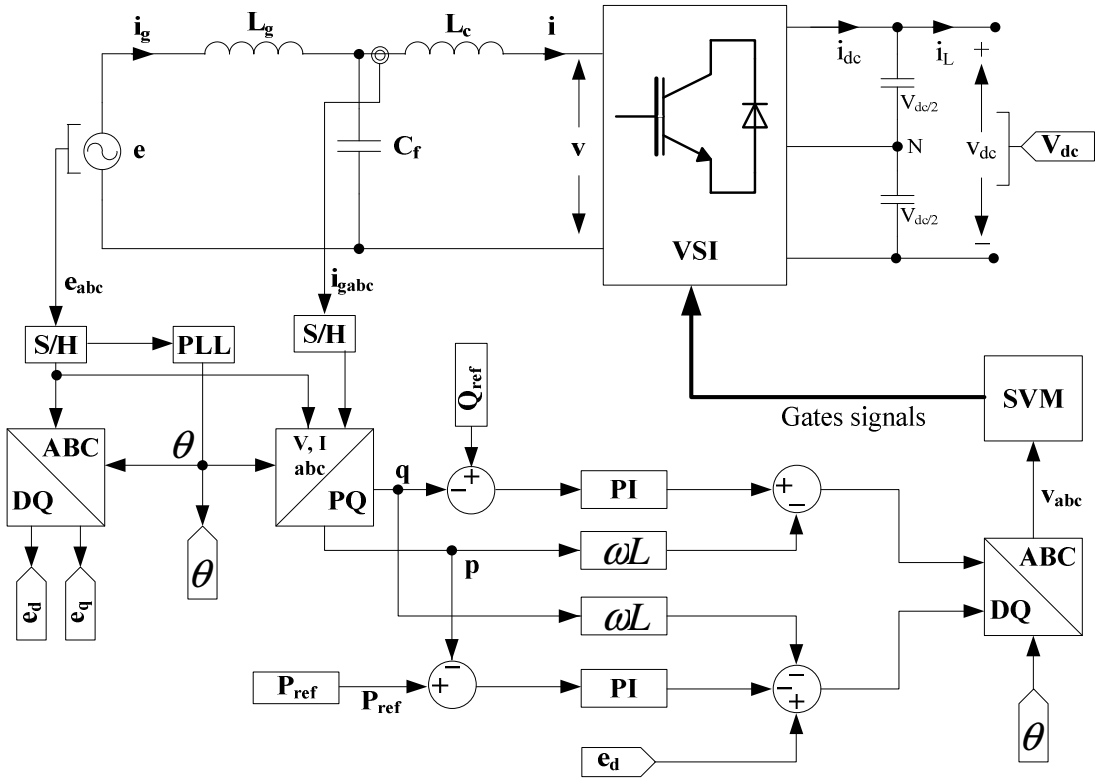

Figure 4.13 Control diagram of direct active/reactive power control

4.5. Simulation result

The simulation is performed for the VSI with a LCL filter using Matlab Simulink for different control techniques. Power block simulation model is shown in figure 4.14 and control block is shown in figure 4.15. All the simulations were performed for 600kW system. All the simulation results are displayed in per unit bases. For constant Vdc voltage control, simulations are performed for both, LCL filter without passive damping

and with passive damping. Figure 4.16 shows the simulation results for constant Vdc voltage with passive filter in motoring mode. The observed steady state error in the DC bus control was around 2%. Step change in load from 0.5pu to 0.9pu has minimum effect on the DC bus voltage. Similar results were observed for regenerative mode.

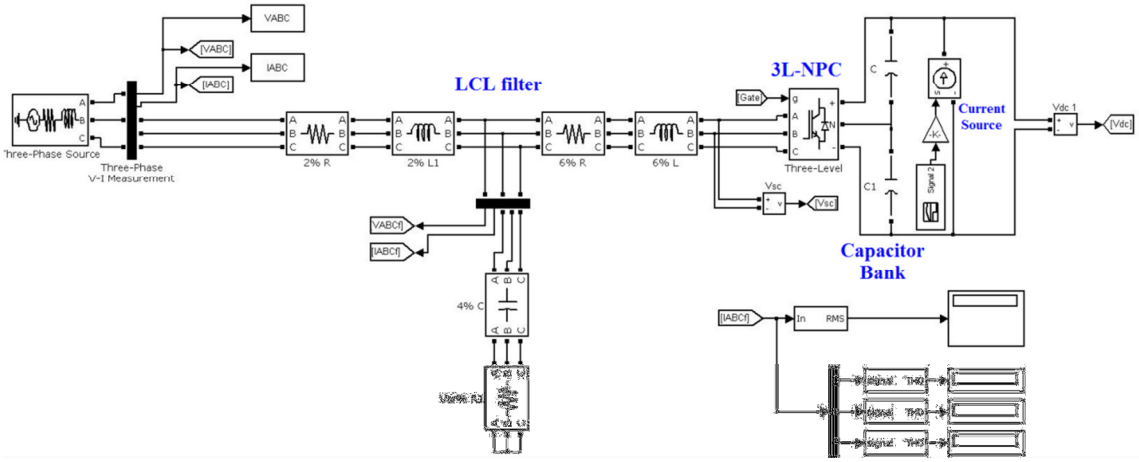

Figure 4.14 3L NPC VSI with LCL filter model in Simulink

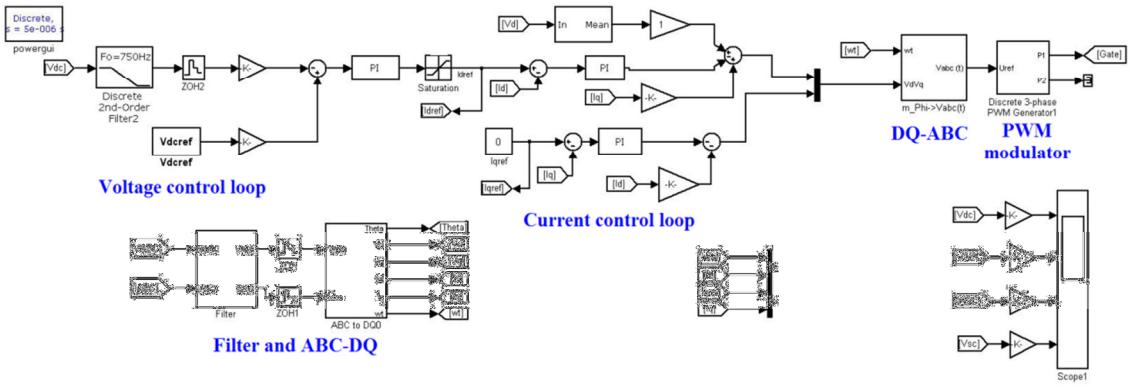

Figure 4.15 Constant DC bus control for 3L NPC VSI in Simulink

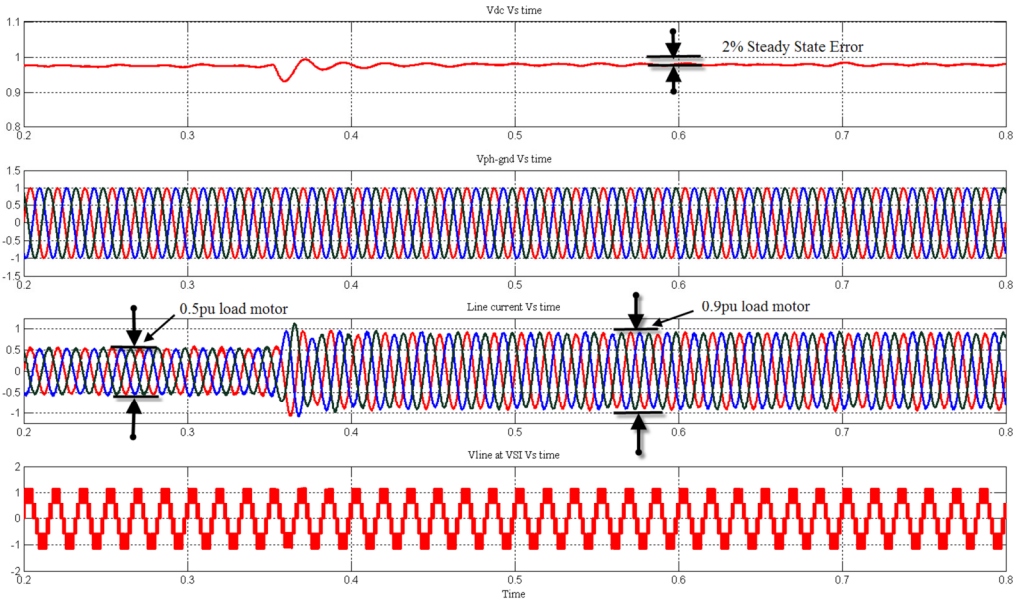

Figure 4.16 Simulation result of constant DC bus control

Figure 4.17 shows the reference and actual I_d and I_q. In simulation $I_{q\text{-}ref}$ set to zero, means reactive power reference set to zero. $I_{d\text{-}ref}$ is set by the voltage control loop to keep the DC bus constant. Simulation results shows that actual I_d and I_q are closely follow the reference signals.

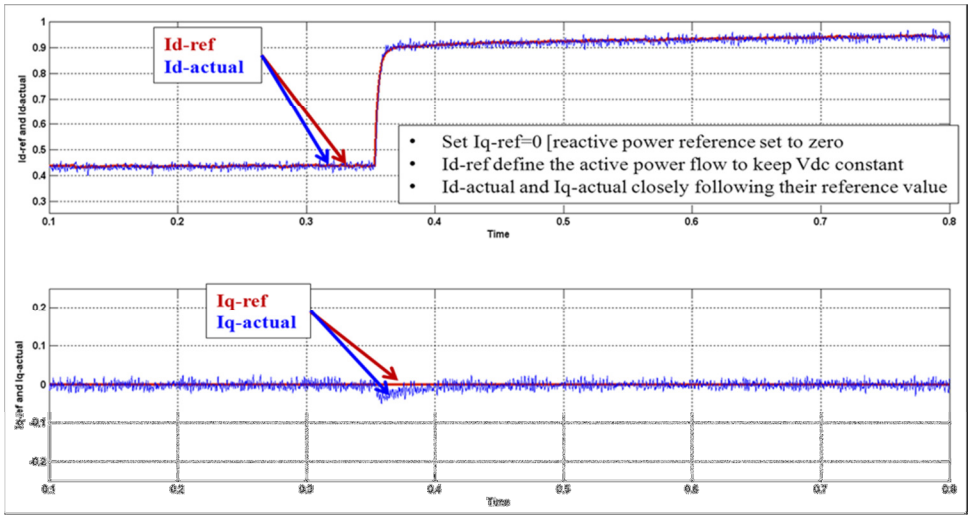

Figure 4.17 Simulation result of reference and actual I_d and I_q

Figure 4.18 shows the simulation results of constant DC bus control in the motor mode and regenerative mode. In the motor mode the phase voltage and line current are in phase, whereas in the regenerative mode they are 180' phase shift. The step responses for both modes are identical.

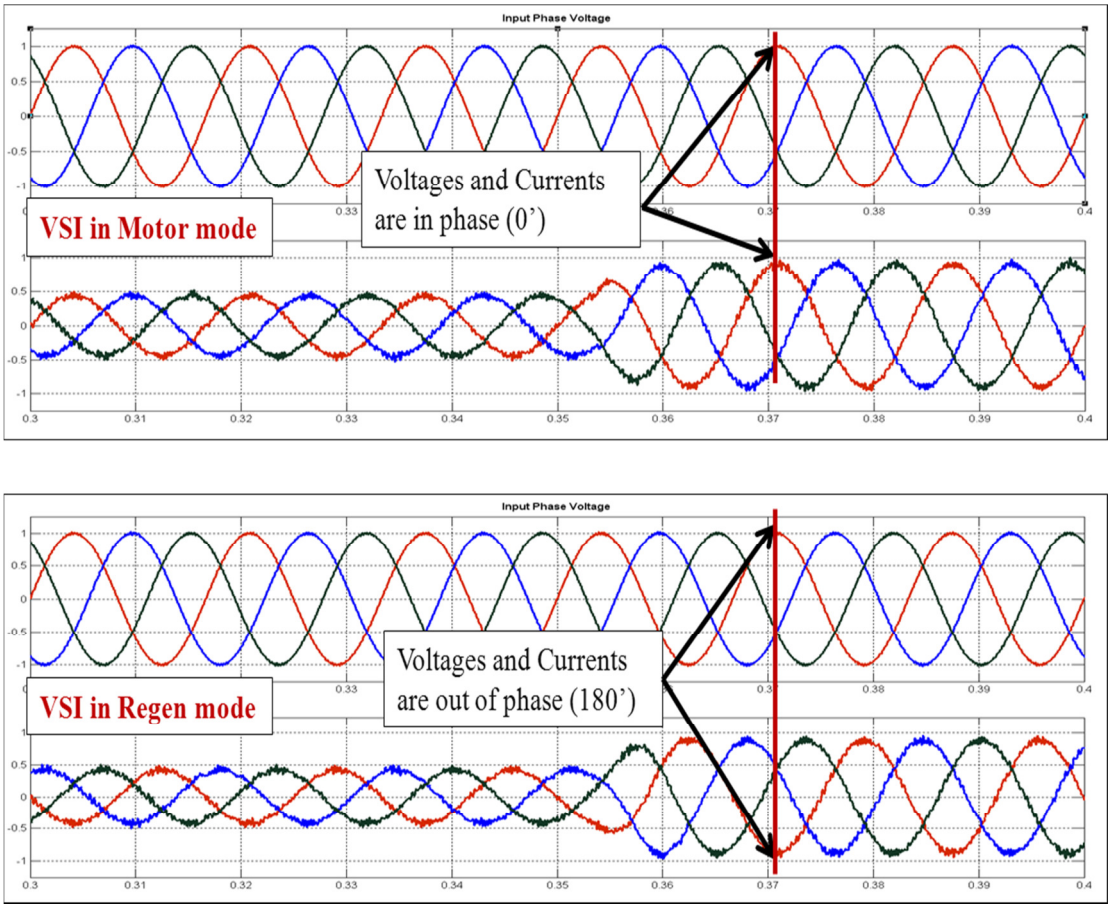

Figure 4.18 Simulation result of Motor and Regen mode of operation

Figure 4.19 shows the line voltage and line current of filter capacitor of LCL filter. Filter capacitor filter out most of the switching frequency components. The grid side inductor observes minimum switching frequency component in line currents.

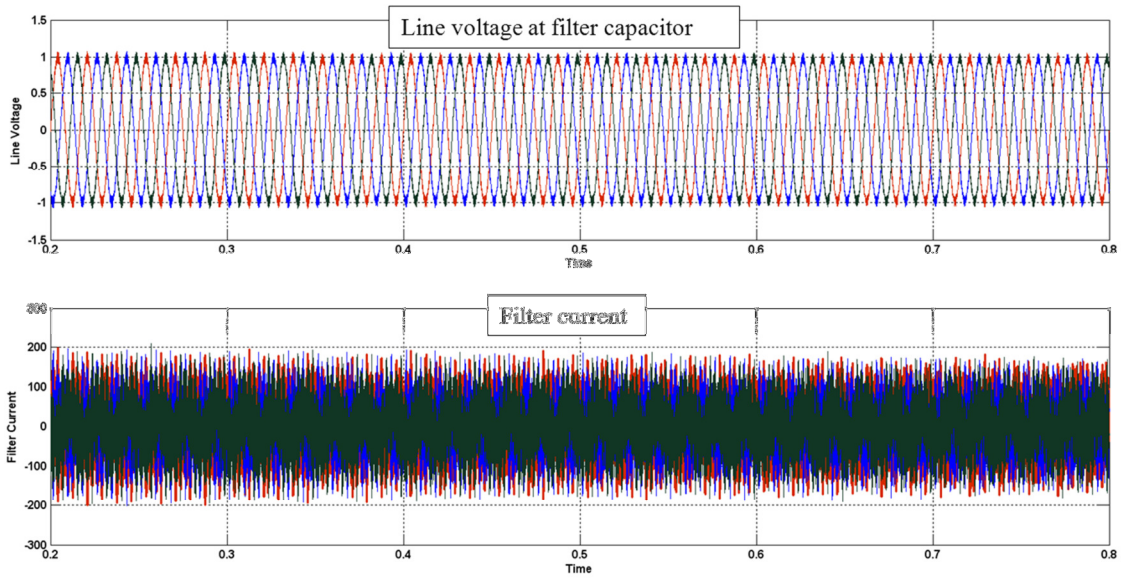

Figure 4.19 Simulation result of filter capacitor line voltage and current

Figure 4.20 shows the FFT of the input current of the system without passive damping. The resonance frequency components (around 2.2kHz) are significantly higher than with passive filter as shown in figure 4.21.

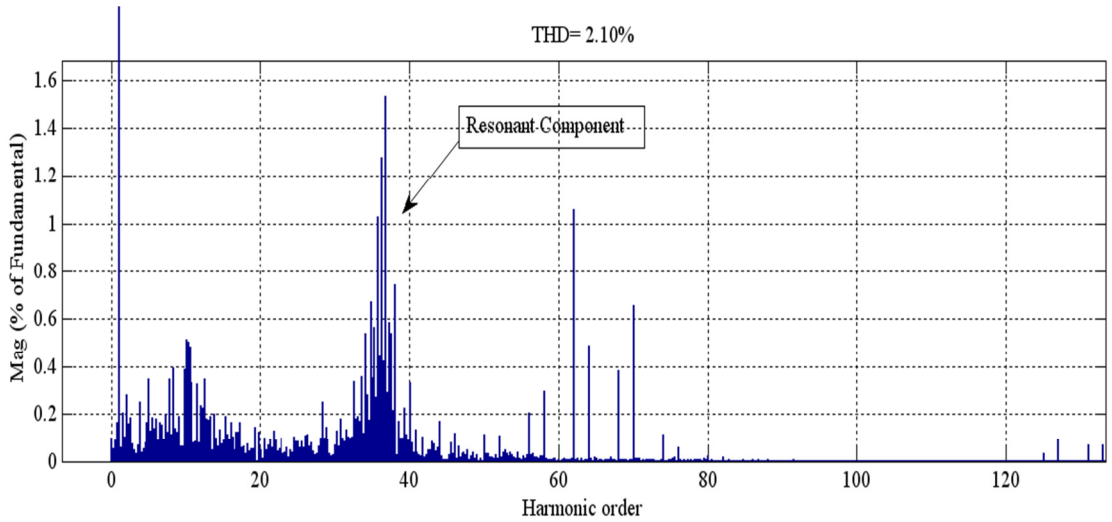

Figure 4.20 FFT of the VSI line current without passive damping

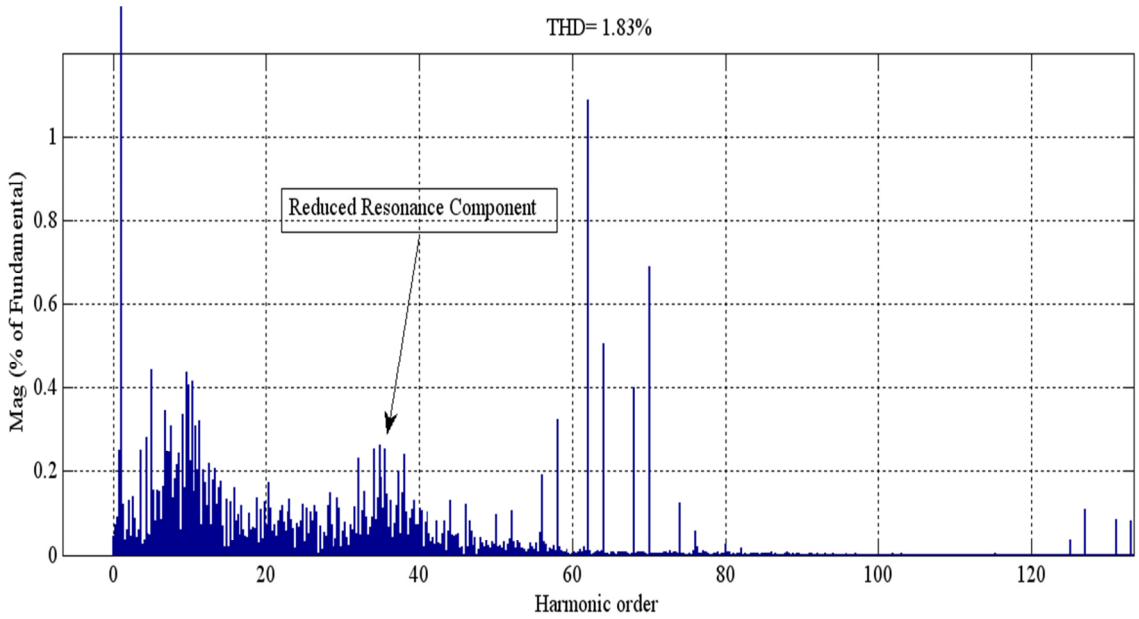

Figure 4.21 FFT of the VSI input current with passive damping

Figure 4.22 shows the simulation results of the active power control of the system. In first simulation, the reactive power reference set to zero. Simulation results show the response with ramp change and step change in the reference signals of the active power. The measured power P_{actual} are closely follow the reference power P_{ref}. To simplify the simulation, Vdc bus kept constant with means of infinite DC source. It can be kept constant by mean of constant DC bus control as mention before using second VSI. Figure 4.23 shows the simulation results with both active and reactive power step change. The control is robust enough that actual active and reactive powers signals are closely follow the reference signals. These active and reactive power controls allow supporting the frequency and voltage droop control of the grid.

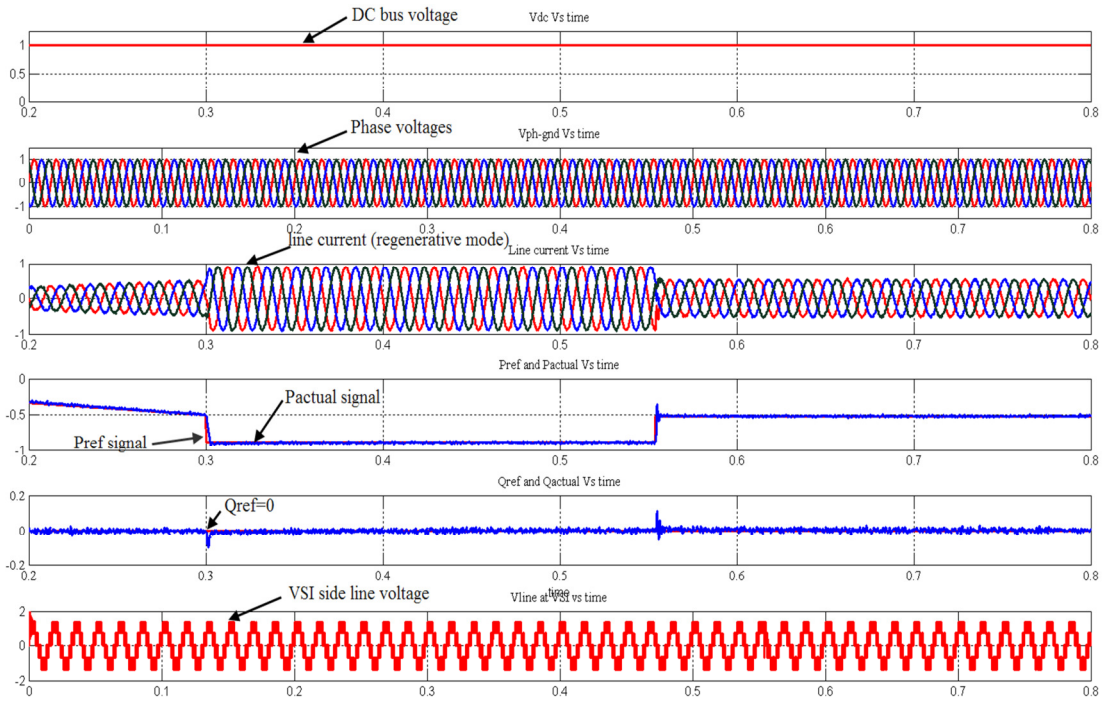

Figure 4.22 Simulation result of active power control

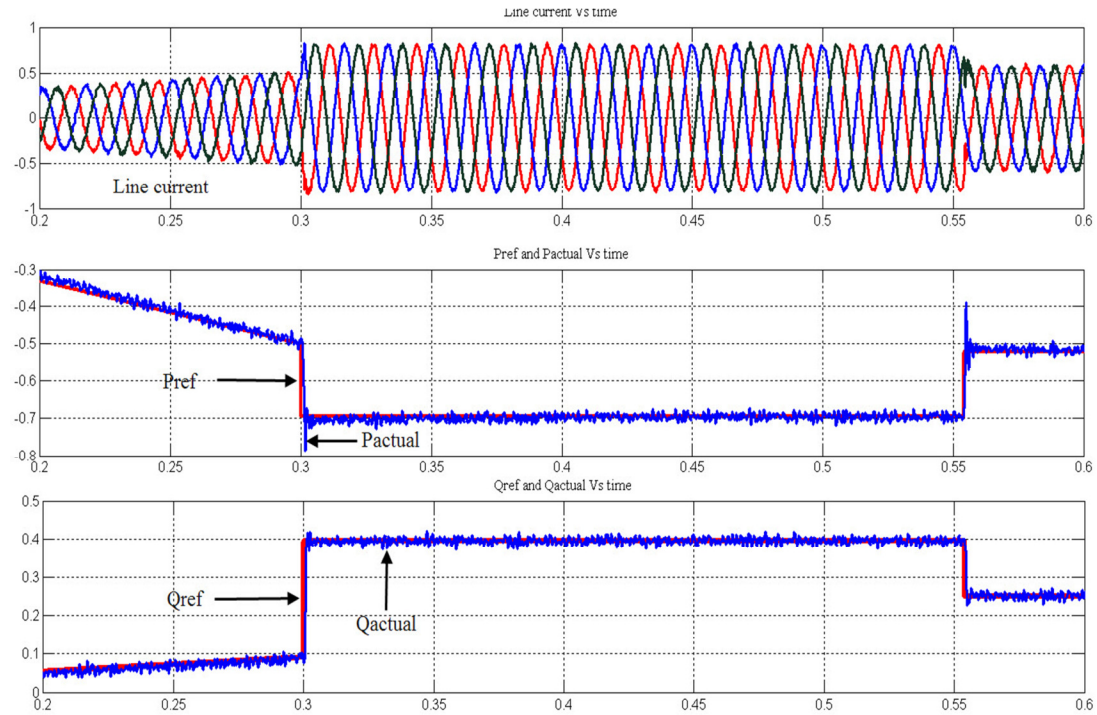

Figure 4.23 Reference and actual active and reactive power

4.6. Experimental setup and control implementation

4.6.1 Experimental result

This section describes the experimental setup built for the purpose of experimentally verifying the behavior of the wind power system in case of the frequency and voltage droop conditions. The setup consists of inverter with inductor connected to grid. The DC link is connected to the regulated DC source to inject the active and reactive power to support the frequency and voltage droop control. The inverter is designed for 10kW, 400-480Vac with 2 Level and 3-Level NPC VSI topologies. The components used for both 2L and 3L NPC VSI are discussed as below. The control is based on GPDSP (General Purpose Digital Signal Process) board, which used the Texas Instrument Fixed Point DSP TMS320F2812. The GPDSP board has 3 current sensors, 3 voltage sensors, DC bus voltage sensor and up to 12 PWM output channels. The GPDSP board has built-in features such as over voltage and over current protection. GPDSP 50 pins interfacing connector can be directly connect to the Power Flex 755 Frame-2 power structure. GPDSP board is shown in figure 4.24. GPDSP board can communicate to the Matlab Simulink through the XDS510USB emulator. Figure 4.25 shows the spectrum digital emulator. Real time embedded coder, Simulink Coder, DSP toolbox, Fixed point toolbox and Simpower system toolbox are required for control implementation in Matlab. Texas Instrument Code Composer Studio Ver 3.3 is used to communicate and program the GPDSP board. Matlab real time embedded coder interface with Code Composer Studio to convert the Simulink model in to the assembly code for DSP.

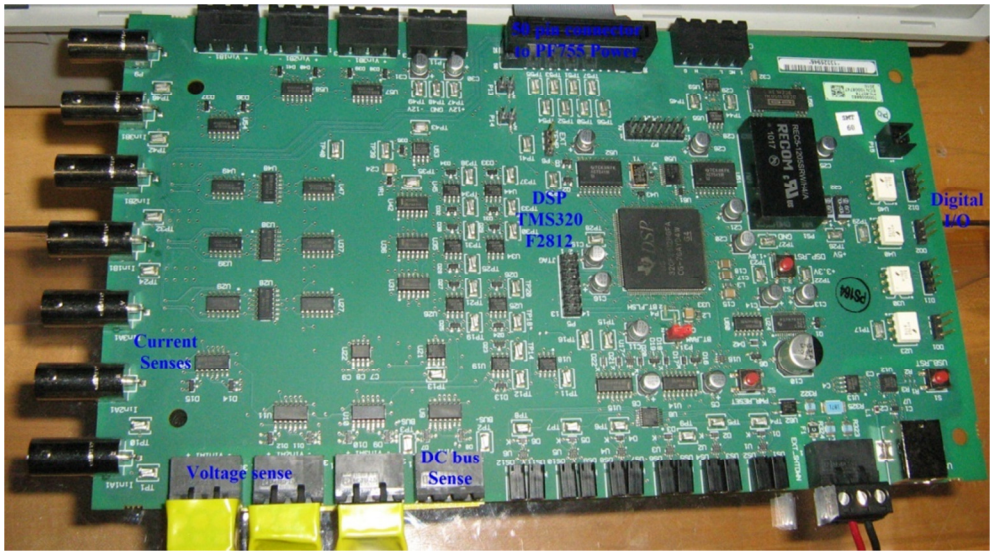

Figure 4.24 GPDSP board with DSP TMS320F2812

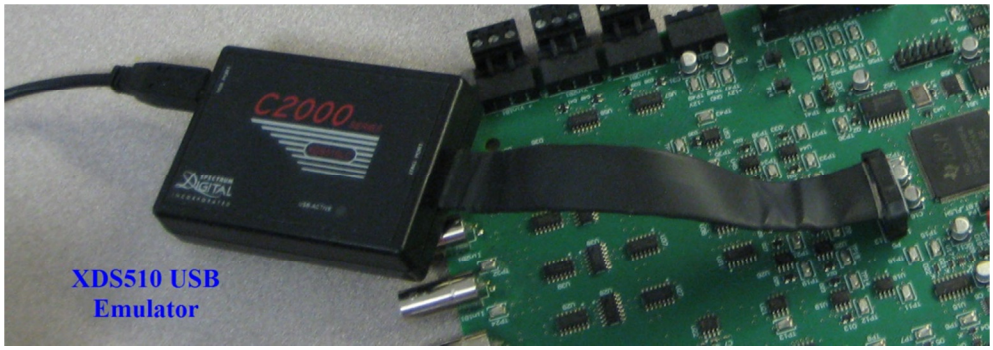

Figure 4.25 Spectrum digital XDS510 USB emulator

Power Flex 755 Frame-2 power unit includes 2 level inverter, gate drive board, current sensors, PCB for voltage and current sense, fan and heat sink. The power structure includes the over current protection, over voltage protection and ground fault protection. All mentions critical faults have hardware interface with PWM inhibit signal that allows shutting down the IGBTs instantly when any of the mention fault detected by the circuit. Power Flex 755 Frame-2 power structure is shown in figure 4.26.

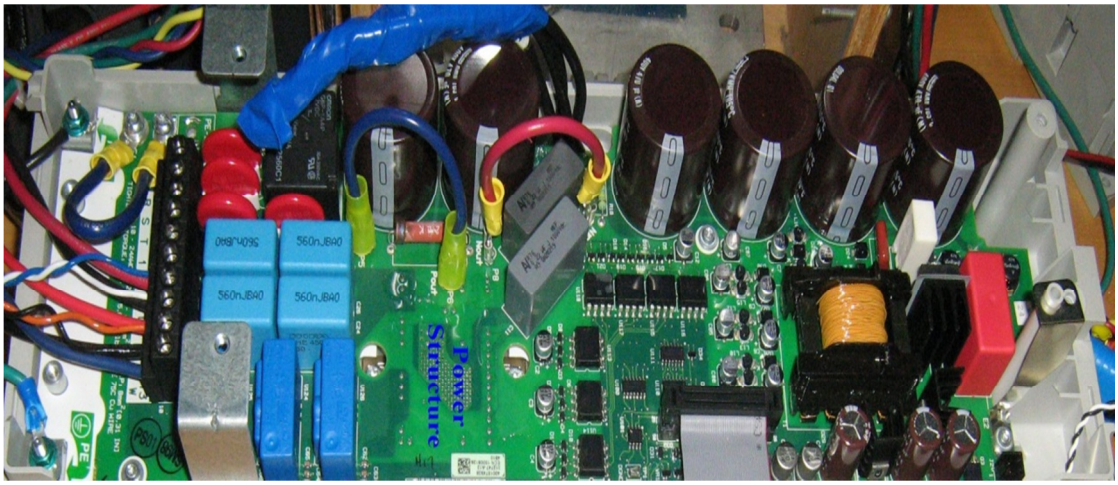

Figure 4.26 Power Flex Frame-2 power structure

The control for the 2L and 3L inverter power structure is same except 3L provides higher voltage capability and requires 12 PWM channels Vs 6 PWM channels for 2L inverter. The IGBT used for the 3L NPC inverter is shown in figure 4.27 (Infineon part # F3L75R07W2E3_B11) [64]. The one leg of the 3L IGBT is shown in figure 4.28.

Figure 4.27 IGBT leg for 3L NPC VSI

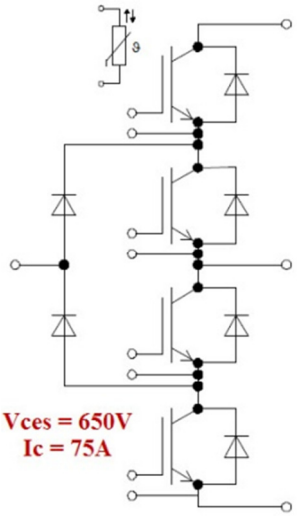

Figure 4.28 IGBT leg for 3L NPC VSI

The gate drive board used to drive the 3L IGBT is shown in figure 4.29. The gate drive board is from Infineon (part # F3L030E07-F-W2_EVAL). The gate drive board snaps on the IGBT modules and provides low inductance structure [64].

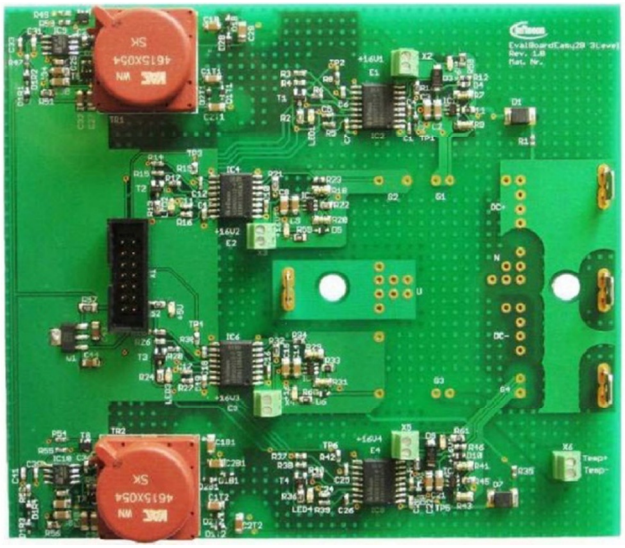

Figure 4.29 Gate drive board for 3L NPC VSI

The 3L NPC VSI power structure is shown in figure 4.30. The IGBTs are mounted on heat sink and gate drive boards are snap on the IGBTs. The laminated DC bus structure is connected to DC link capacitors as well as IGBTs. Balancing resistors are connected to the DC bus. The gate drive boards interface with the GPDSP board using three 14pins ribbon cables.

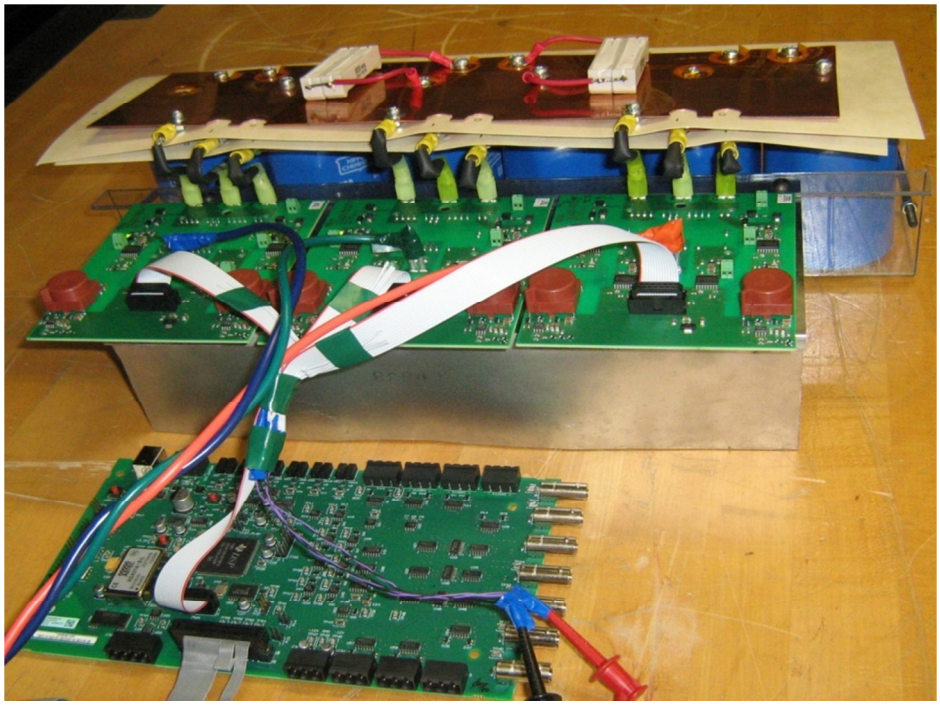

Figure 4.30 3L NPC VSI with DC bus structure

The block diagram of an experimental setup of the 2L inverter is shown in figure 4.31. The source is connected to 19% inductor using delta to Y connected transformer. In order to reduce the common mode circulating current, the neutral of the Y connected winding is not grounded. Output of the inductor is connected to Power Flex 755 Frame 2 structure. Siemens active interface module is used as regulated DC bus supply. GPDSP board gets is three phase voltage feedbacks from input of the inductor and current sense

signals from PF755 power structure. GPDSP board interface with Matlab Simulation using emulator.

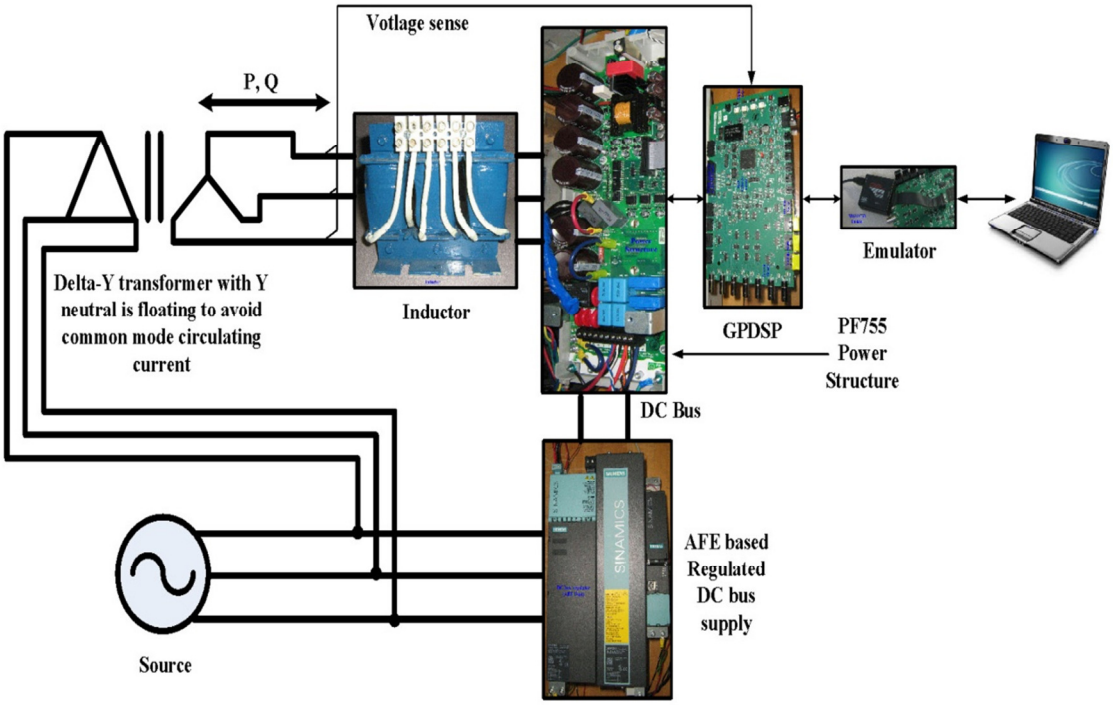

Figure 4.31 Block diagram of 2L inverter setup

The actual setup for 2L inverter is shown in figure 4.32 and figure 4.33. The figure 4.32 show the PF755 frame 2 power structure interface with the GPDSP board. The 24V power supply is used to power up the GPDSP board and the PF755 frame 2 fan. The first fuse-disconnect is used to provide voltage sense to the GPDSP board without actually applying power to the unit. It allows scaling of the voltage sense circuit as well as the PLL synchronization to line voltage before modulation of the VSI unit. The second fuse disconnect will be only turn on when it is required to modulate the VSI. The setup including measurement instrumentation for voltage and current is shown in figure 4.33.

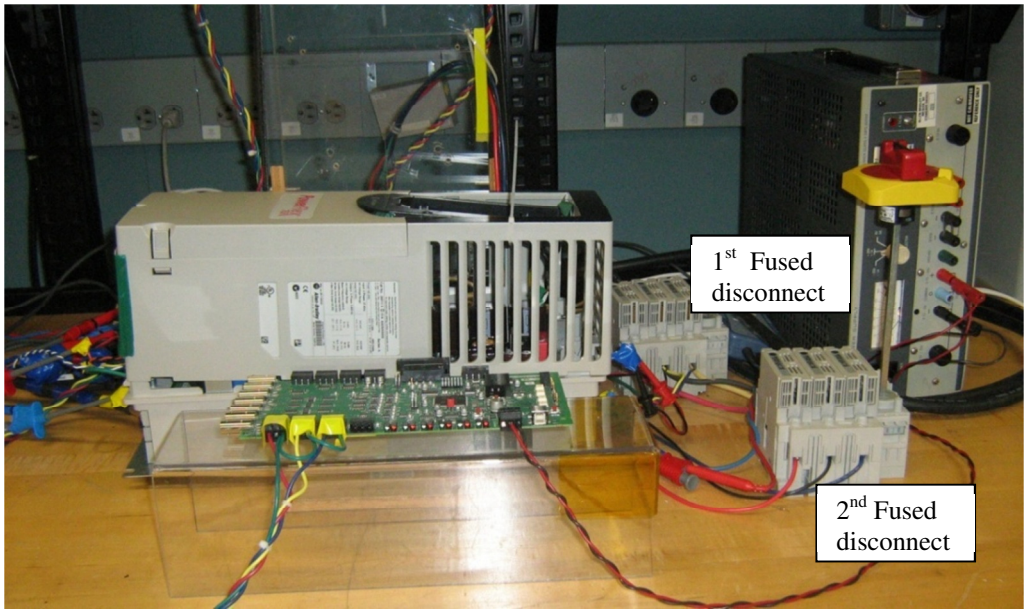

Figure 4.32 Actual 2L inverter test setup

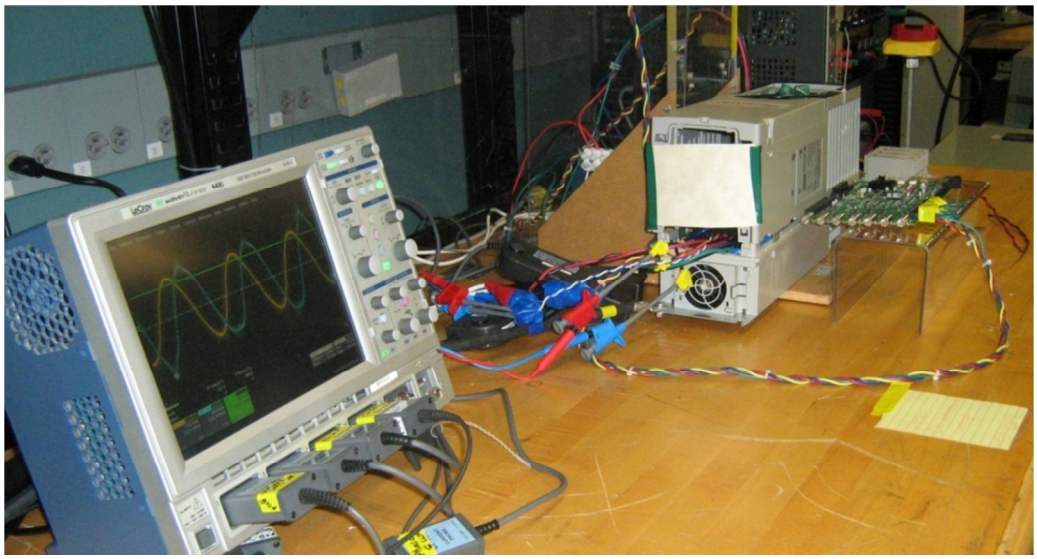

Figure 4.33Voltage and current measurement setup

Figure 4.34 shows the 3L NPC VSI power structure interface with GPDSP board and drive simulator. The bench level setup is used to generate the 12 PWM pulses to control the IGBTs. Figure 4.35 shows the gate pulses measurement of one of the leg of the 3L NPC VSI IGBTs.

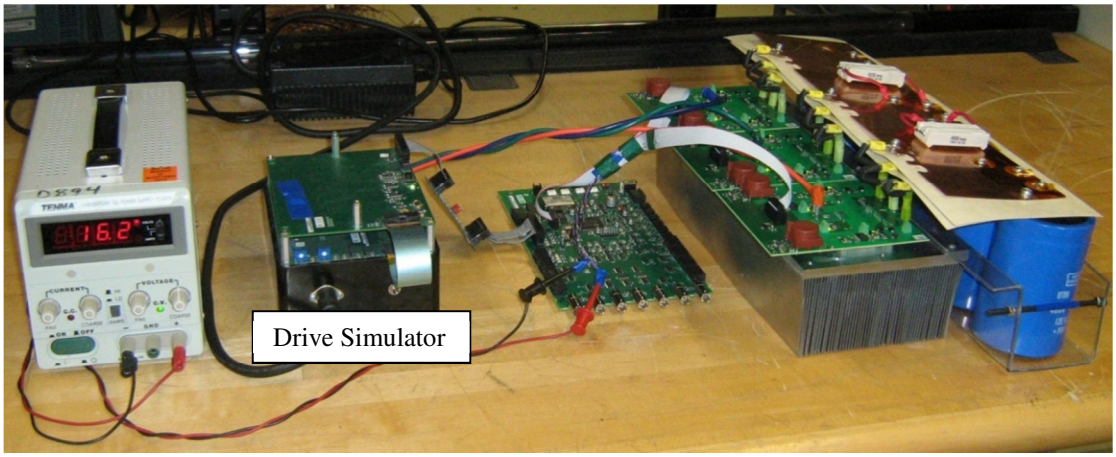

Figure 4.34 3L NPC VSI interface with GPDSP and drive simulator

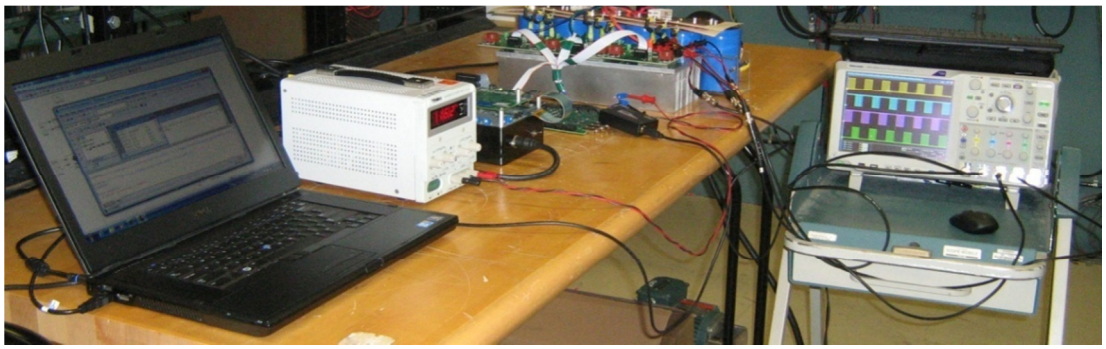

Figure 4.35 3L NPC VSI setup for gate pulse measurement

The control is implemented in Matlab Simulink. The control includes ADC for voltage and current sense, PLL, current control regulator with cross coupling effect and feed forward term and PWM modulators for the 2L and 3L NPC.

4.6.2. Control Implementation using Matlab Simulink RTE coding

Three phase input voltages are sense using a voltage resistor divider network. The input voltage range to ADC converter is 0-3V. The voltage sense circuit scaling and

calibration is required in order to avoid DC offset in measurement and to keep the symmetry of three phase waveform. The current is sense by Hall Effect current sensor. The burden resistance is selected such that 0-3V scales the full load current of the power structure. Sometime scaling of current sensor includes the 150% overload factor. In this case 3V relates to 150% over load. The trip level for the over current is set to 5V. The ground current fault is set based on sum of the all three phase instantaneous current is more than 25% of rated current of the unit. The voltage and current sense signals are feed to the inbuilt 12 bit ADC of the DSP. The outputs of the ADC signals are compensate for the offsets and convert to either 16 bit integer or 32 bit unsigned integer signals. Finally the voltage or current signals are converted to pu (per unit) with fixed data type (1, 32, 20) format using shift and data converser operation as shown in figure 4.36.

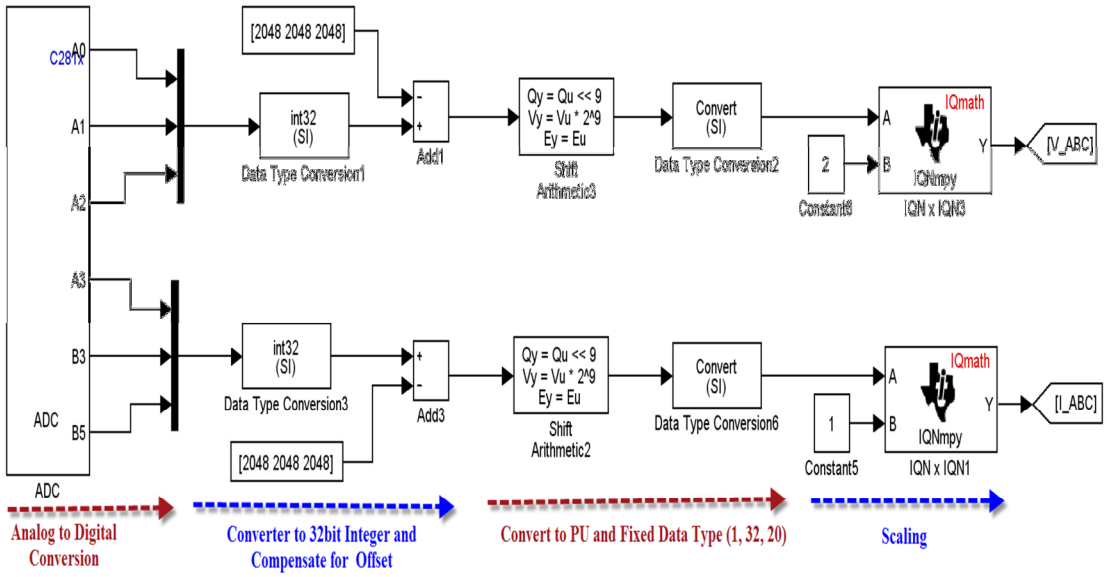

Figure 4.36 ADC, data type conversion / scaling of voltage and current signals

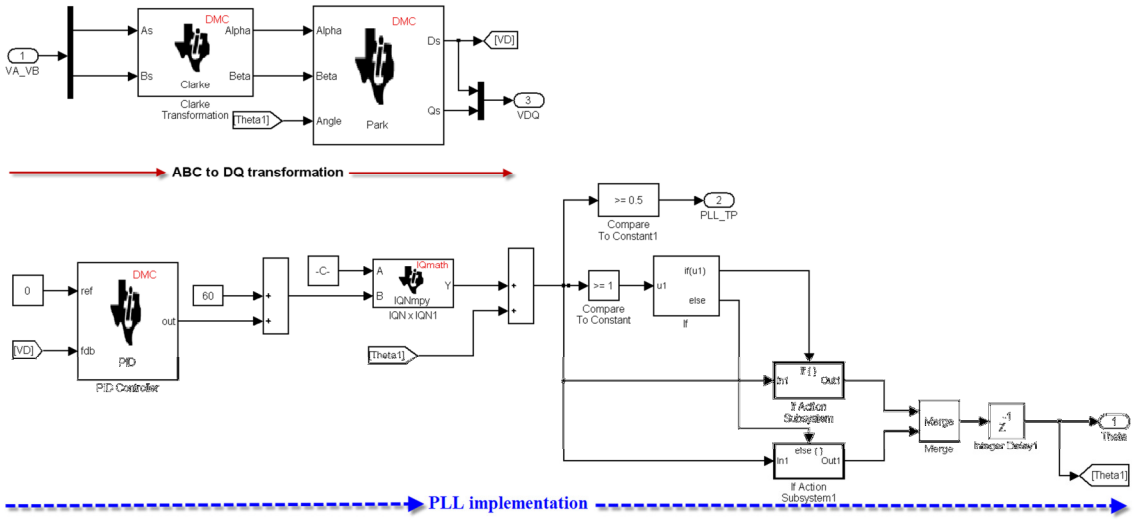

Figure 4.37 PLL implementation in DSP TMS320F2812

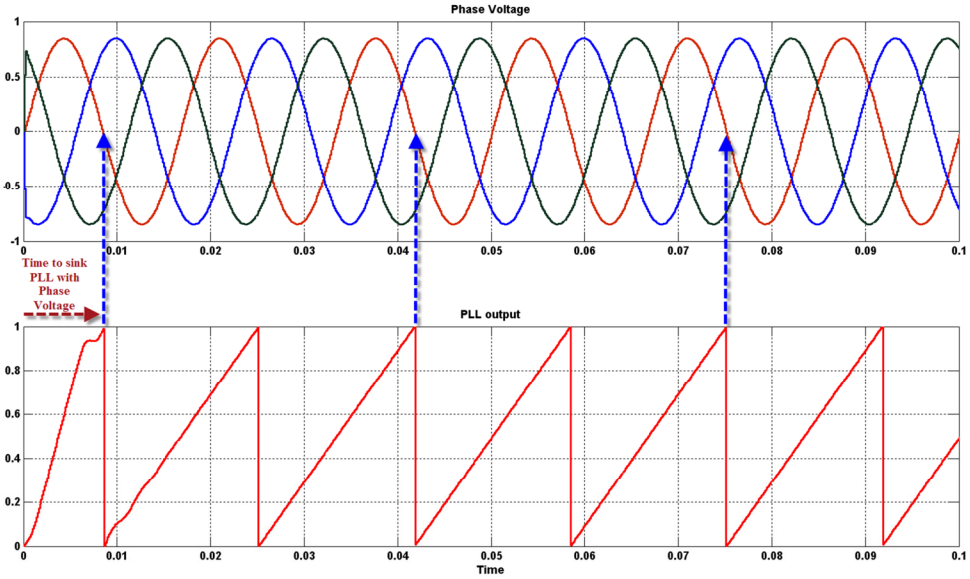

Figure 4.38 PLL signal synchronized with phase voltage

The PLL is based on the synchronous reference frame. The PLL implementation is shown in figure 4.37. Three phase voltages are converted to V_d and V_q using Clark Park transformation. The V_d is compare with the reference signal (0V) and feed to the PI

regulator. Output of the PI regulator is scaled and added to the feed forward angle theta. Simulation result in figure 4.38 shows that PLL synchronization with the phase voltage takes at least half cycle of the input voltage. It is required to delay the PWM modulator at least one cycle, such that it guarantees synchronization of PLL with line before PWM start modulating.

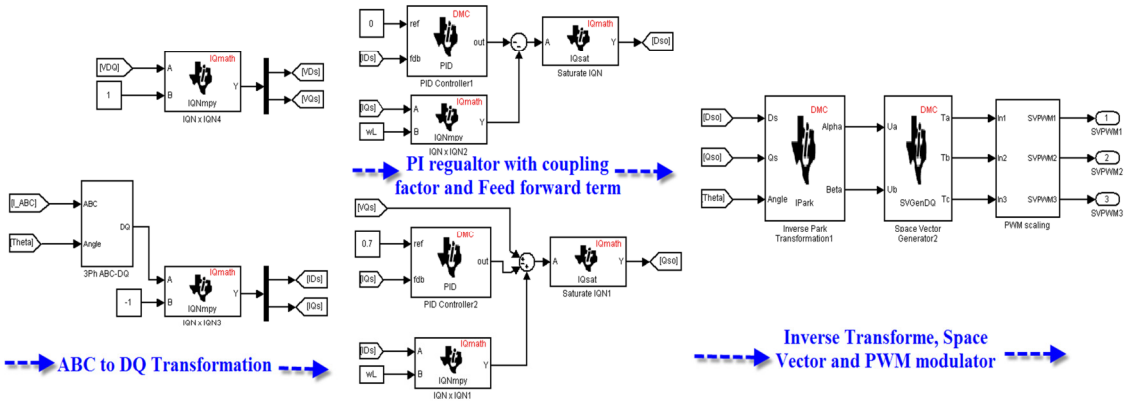

Figure 4.39 Current regulator in DSP TMS320F2812

The current control loop implementation is shown figure 4.39. The pu three phase voltages and currents are transformed to D-Q axis using Clark-Park transformation. The D-Q voltages and currents are feed to the PI regulator. Current control loop includes cross coupling and feed forward term. Output of the PI regulator goes to the limit block. Using the inverse transformation and Space Vector PWM technique, converts the D-Q signals of the limit block to the ABC. The standard PWM modulator generates the 3 pulse which feed to the PWM generator to generate 6 pulses to drive the gates of the 6 IGBTs for the 2L VSI. All the calculations of the current control loop are based on the fixed point data types. PWM switching frequency is set to either 4 kHz or 8 kHz. The dead time of the PWM set to 1.2uS.

As shown in figure 4.5, there are two reference triangular carrier signals compared with 3 sinusoidal control signals to generate 12 pulses for the 3L NPC VSI. The TMS320F2812 fixed point DSP has no such features available to generate two triangular carrier signals. The new algorithm is implemented in Matlab Simulink, which generates 6 control signals from the three SVPWM signals and compare with only one reference triangular carrier signal to generate 12 pulses for the 3L NPC topology. The Matlab Simulink model is shown in figure 4.40.

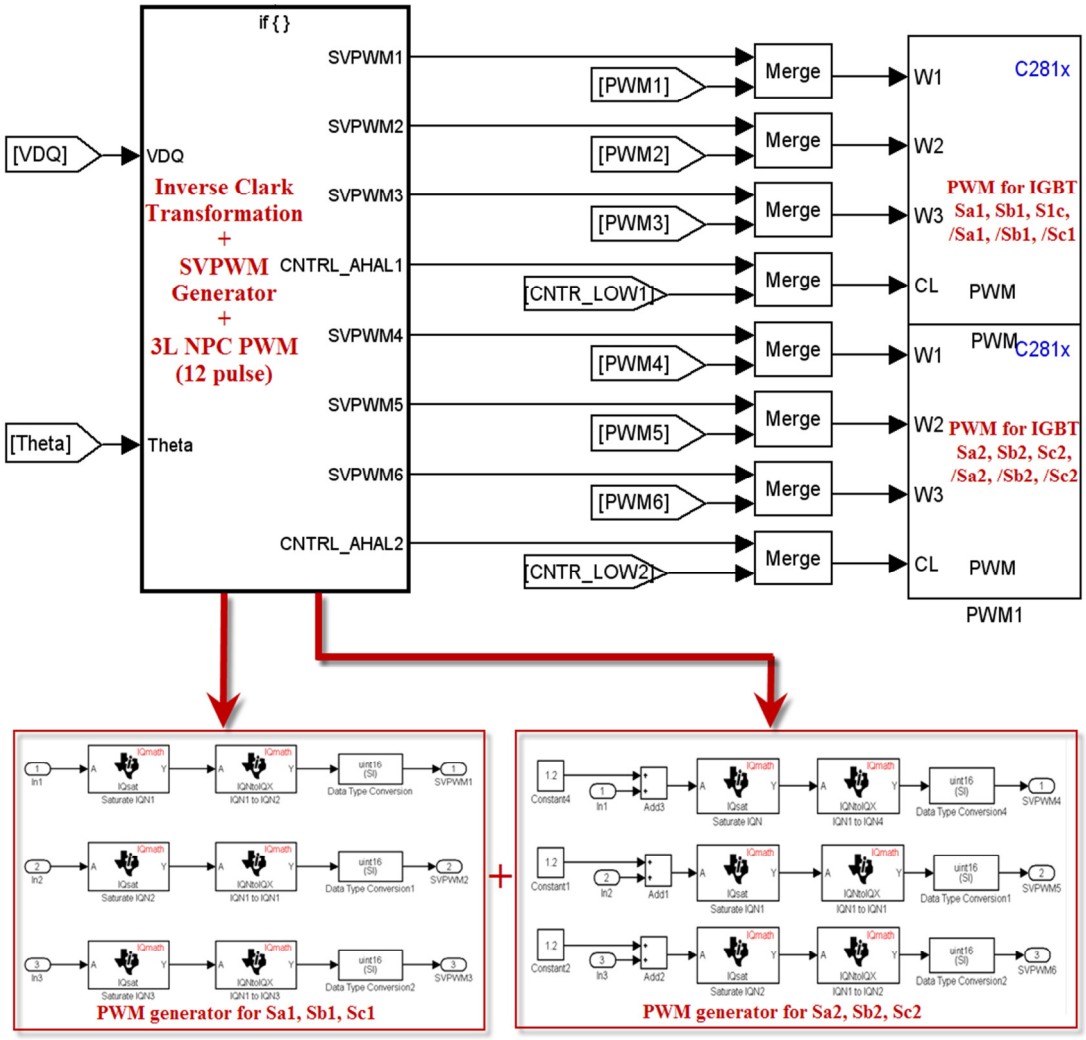

Figure 4.40 6 pulse generators in Matlab for 3L NPC VSI

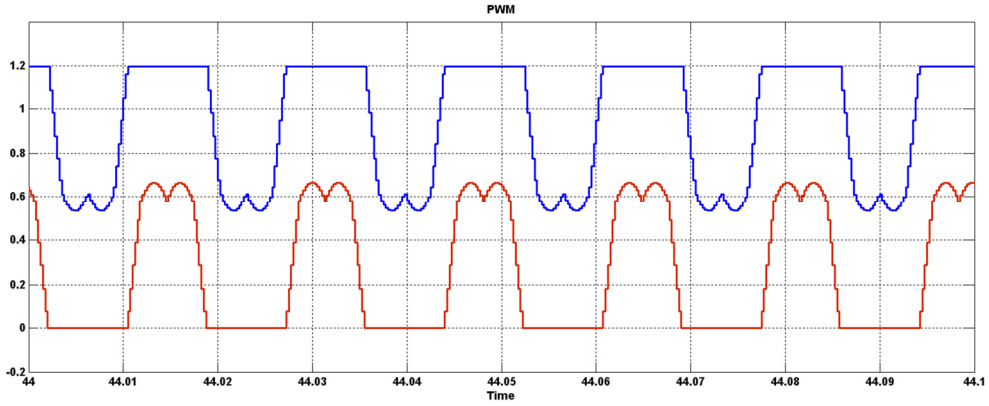

Figure 4.41 Modified 2 pulses per phase for 3L NPC gate pulse generator

Figure 4.41 shows the split SVPWM waveforms for one phase. Similarly another four split SVPWM waveforms are generated for remaining two phases. The total 6 waveforms are compared with the single triangular carrier signal and generate 12 pulses to drive 12 IGBTs for 3L NPC topology.

4.6.3 Experimental result

The experimental result of the PLL synchronization with line voltage is shown in figure 4.42. The PLL synchronized with the phase voltage, which is 30 degree lags the line voltage. The 4 kHz sample rate (250uS sample time) is used for the PLL implementation. The delay in synchronization is about 250uS which is translated to 5.4 electrical degrees. The error in angle measurement by PLL is 5.4 electrical degrees for 4 kHz sampling frequency and 2.7 electrical degrees for 8 kHz sampling frequency. Higher the sampling frequency, betters the result of PLL synchronization.

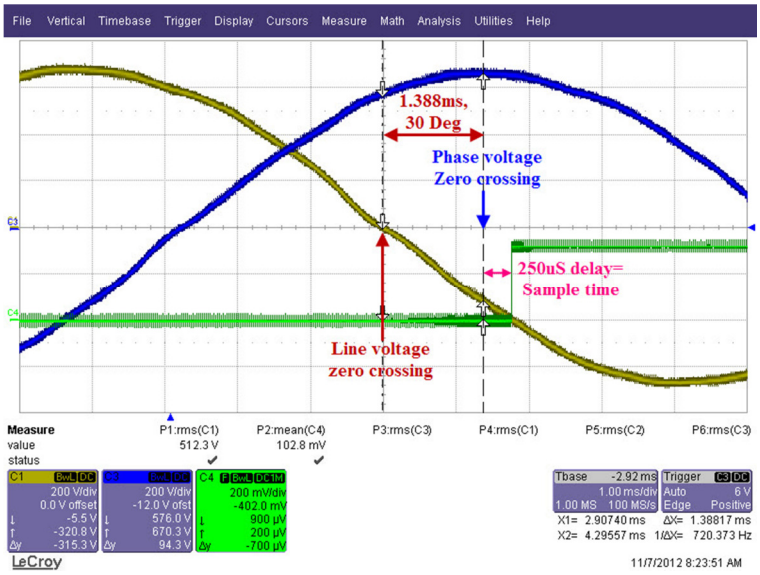

Figure 4.42 Experimental result of PLL sync with phase voltage

Figure 4.43 shows the line voltage has significant amount of common mode noise. The PLL is immune to the noise on the line voltages. The robust PLL is required to interface the inverter with the grid. If there are any transient conditions, PLL allows inverter to continue its operation without drop out.

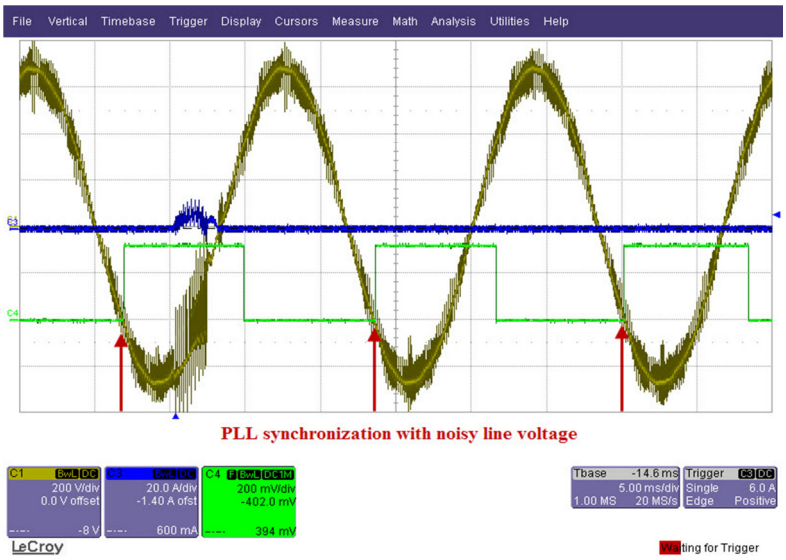

Figure 4.43 PLL synchronization with noisy line voltage

The 2L VSI ran at 400Vac input voltage, full load (14A). The VSI unit ran in motor mode as well as regenerative mode. The line to line voltage (V_{RS}: channel 1, Yellow), line current (R: channel 3, Blue) and DC bus voltage (Vdc: channel 4, Green) for motor mode are shown in figure 4.44. The measured line to line voltage VRS= 391Vrms, line current = 14.01 Arms and DC bus voltage = 765.4Vdc.

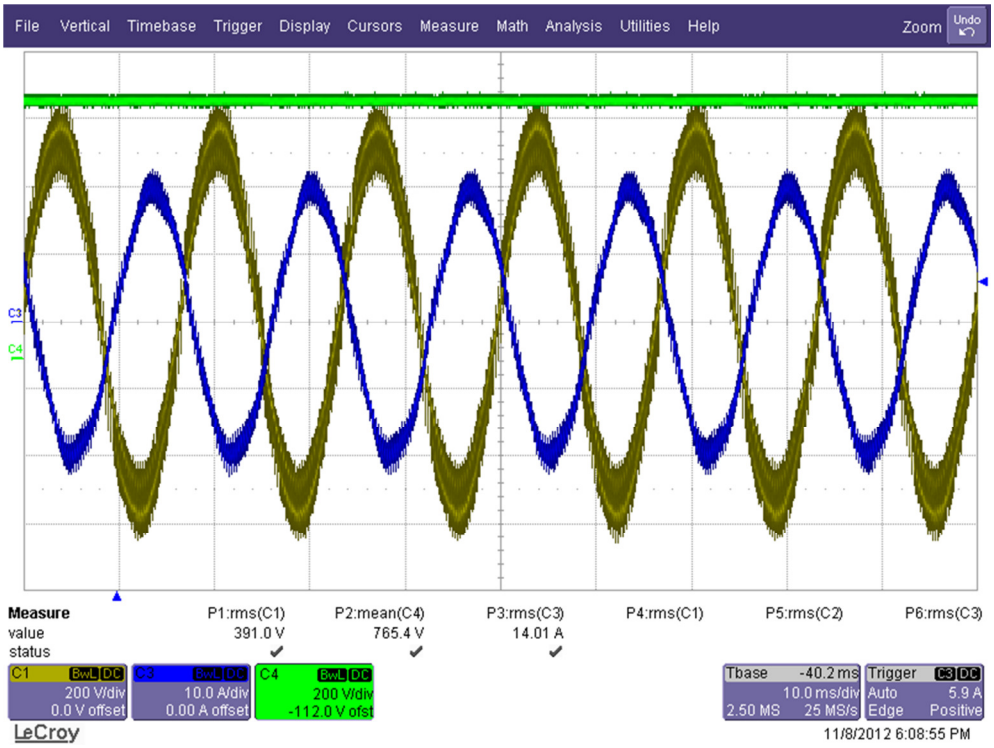

Figure 4.44 Experimental result of 2L VSI in motor mode at full load

The 2L VSI in regenerative mode is shown in figure 4.45. The channel descriptions are same as in figure 4.44. It should be noted that the direction of currents are reverse for the regenerative mode of operation.

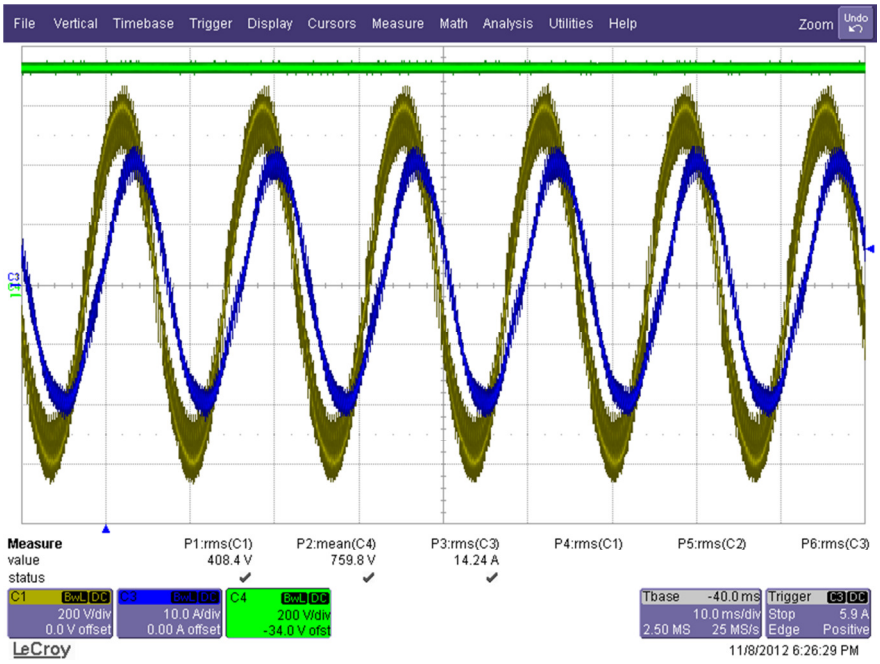

Figure 4.45 Experimental result of 2L VSI in Regen mode at full load

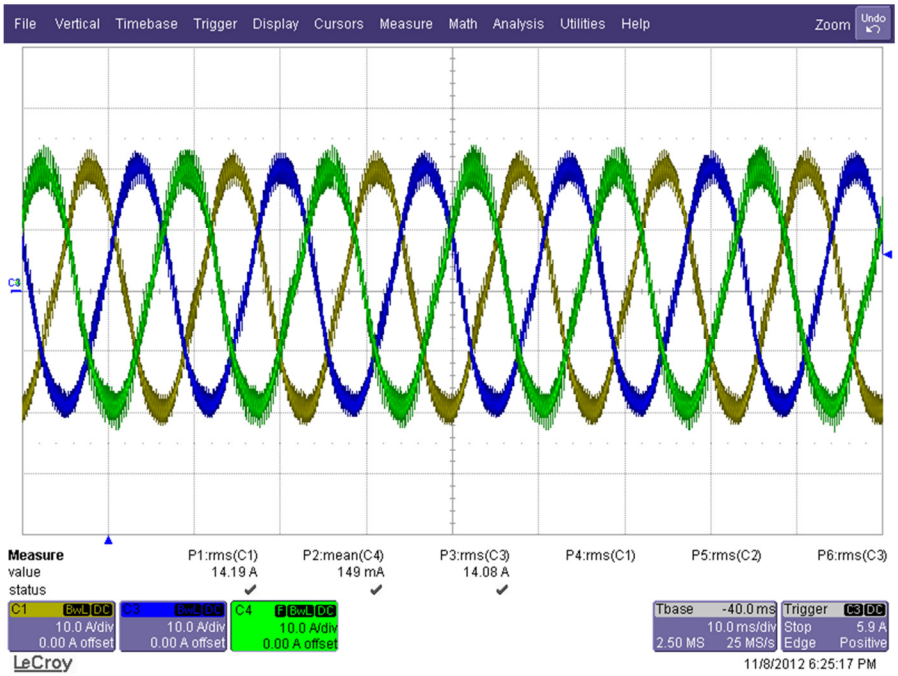

Figure 4.46 3-phase current waveform in Regen mode at full load

The three phase current waveforms of the VSI in regenerative mode at full load are shown in figure 4.46. The current waveforms are symmetric without any DC offset. Generally, if there is any offset in the scaling of the voltage sense circuit, it will introduce the DC offset in phase current. The waveforms in figure 4.44 and 4.45 are saved as text file and post processed the FFT analysis using the Matlab Simulink. The voltage and current FFT are shown in figure 4.47 and figure 4.48 respectively. The VSI under test is running at 4 kHz switching frequency but in voltage and current FFT the 8kHz switching frequency components are significantly higher because of the Siemens unit which is regulating the DC bus is running at 8kHz switching frequency. Its resonance frequency may close to the switching frequency of the PF755 FR2 unit. The total harmonic distortion for line voltage is 11% and the total demand distortion for line current is 6.82%.

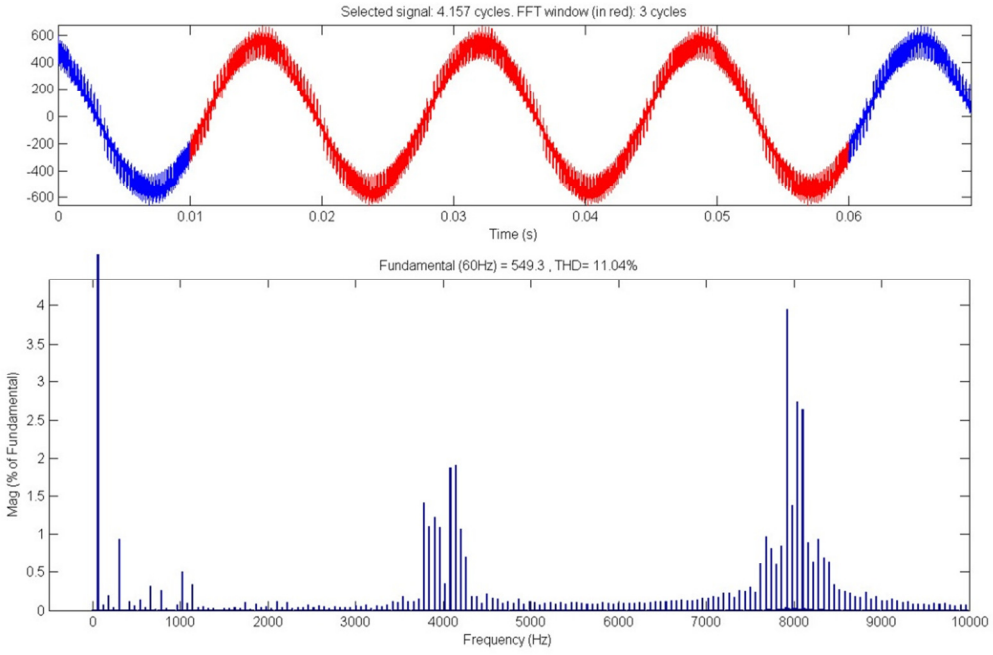

Figure 4.47 FFT analysis of line voltage for 2L VSI

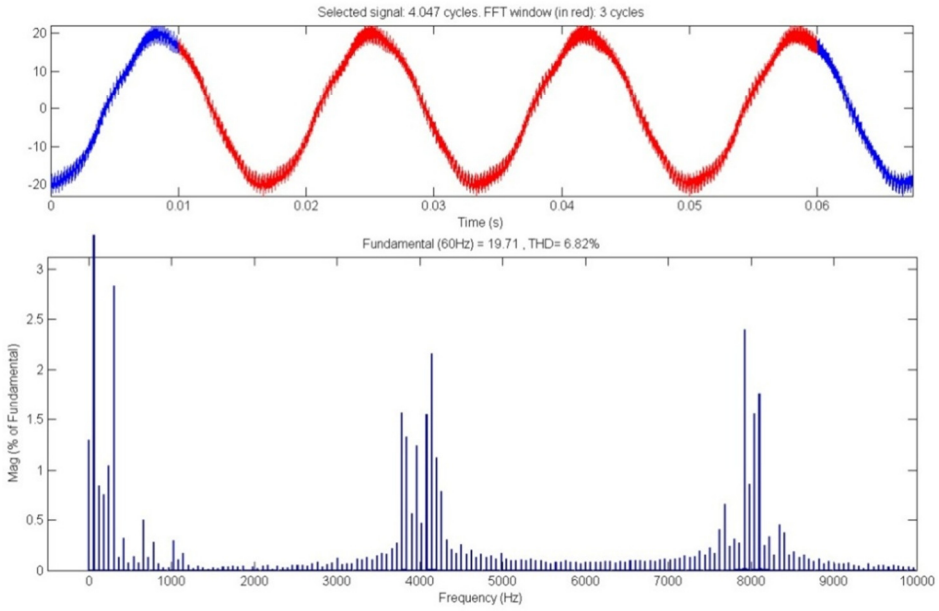

Figure 4.48 FFT analysis of line current for 2L VSI

The 3L NPC gate pulses are generated using GPDSP board and algorithm discussed in previous section. The figure 4.49 has shown the gate pulses pattern for the one leg of the VSI. Channel 1 is IGBT 1 gate pulse, Channel 2 is IGBT 2 gate pulse and so on.

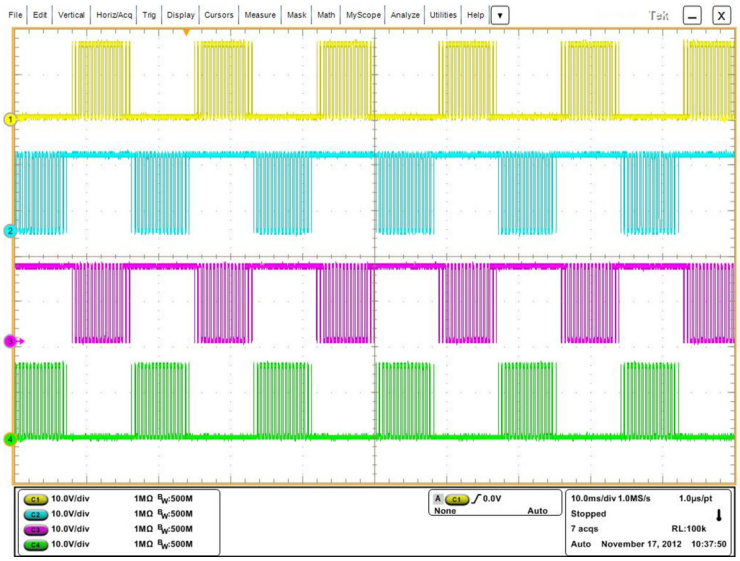

Figure 4.49 Gate drive pulse pattern of one leg for 3L NPC

IGBT 1 and IGBT 3 are complementary pulse patterns and IGBT 2 and 4 are complementary pulse patterns. The maximum delay in IGBT1 and IGBT 2 pulses are 800nS. The dead time for complementary (IGBT1 and IGBT3, IGBT2 and IGBT 4) pairs is set to 1.2uS. Figure 4.50 shows the waveform of the gate pulses of second IGBT in phases R, S and T legs. The gate pulse patterns are 120 degree apart.

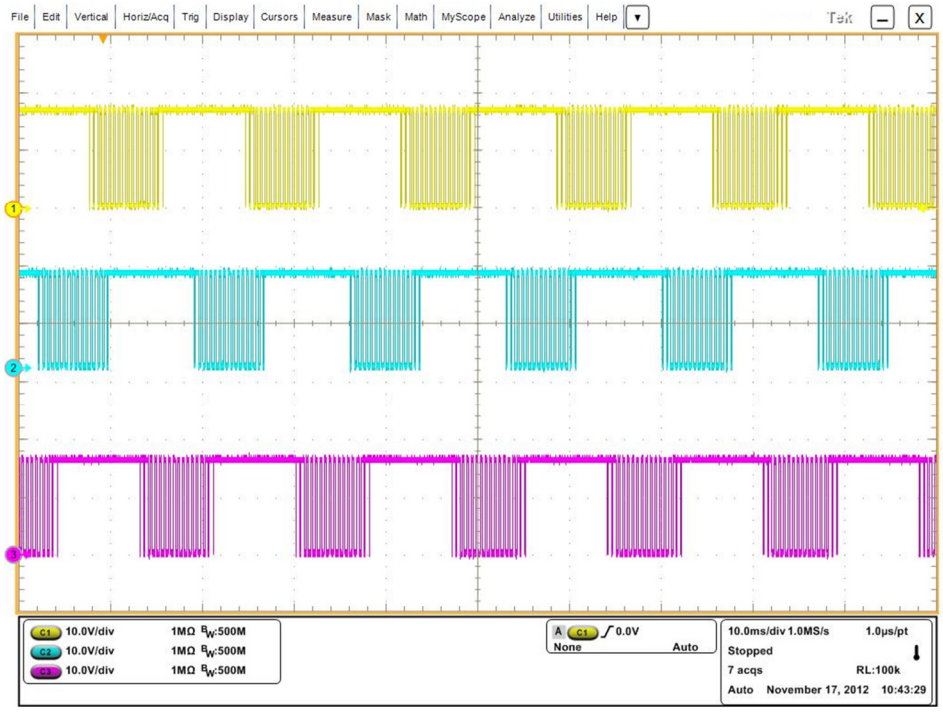

Figure 4.50 Gate pulse pattern of 2nd IGBT of Phase R, S, & T

The experimental is performed using 3L NPC power structure in motor mode with low DC link voltage. This is because the gate drives do not provide negative bias to the IGBT. The DC link voltage is provided by unregulated DC power supply. Three phase line to line voltage measurement is shown in figure 4.51. The voltage measurement is performed at output of the converter which shows the five steps in a waveform which match the

simulation results. Channel 1 is line voltage R to S (yellow) , channel 2 is line voltage S to T (blue) and channel 3 is line voltage S to R (pink) and channel 4 is the DC bus voltage (green).

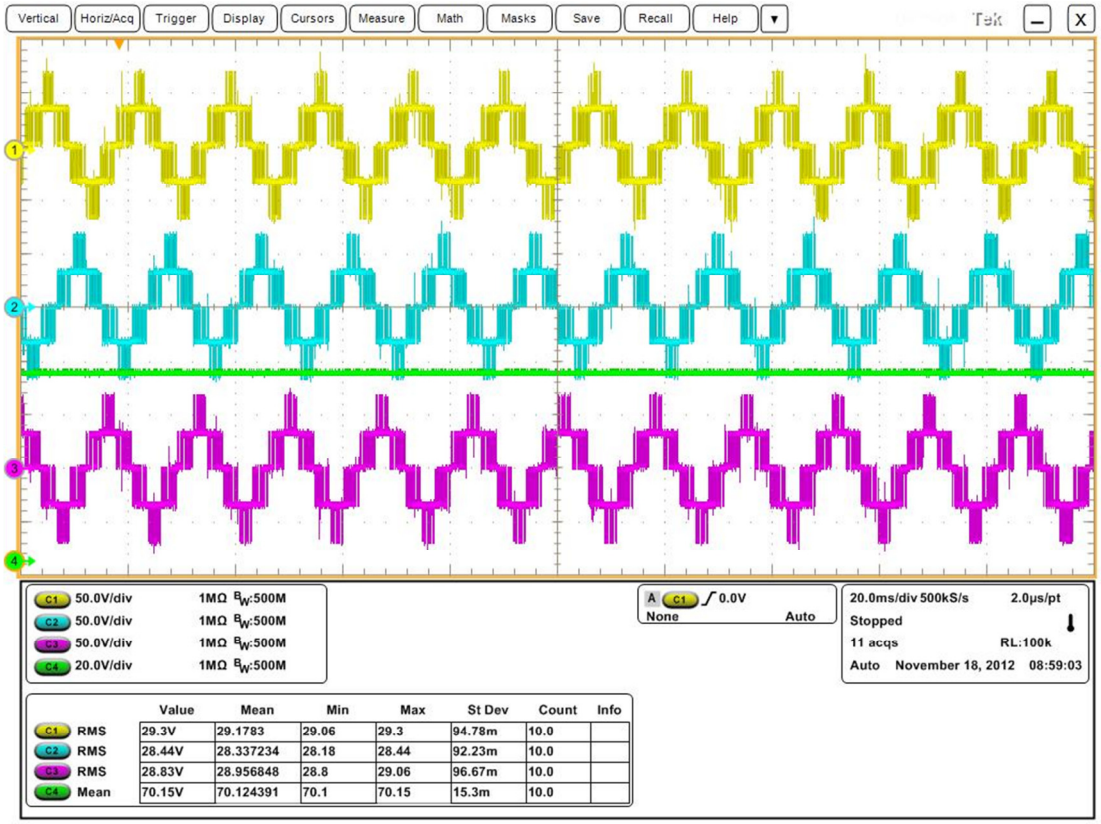

Figure 4.51 3L NPC line voltage measurement at converter side

Figure 4.52 shows the measurement of the line voltage (channel 1, blue), line current (channel 2, pink) and DC bus voltage (channel 4, blue). In the motor mode, unit is running at 60 Hz frequency with open loop control. DC bus is kept to maximum 100Vdc because the gate drivers had no negative bias. The results show that the 3L NPC is working but just require gate boards with negative bias which allows to perform experiment in close loop mode with higher DC bus voltage.

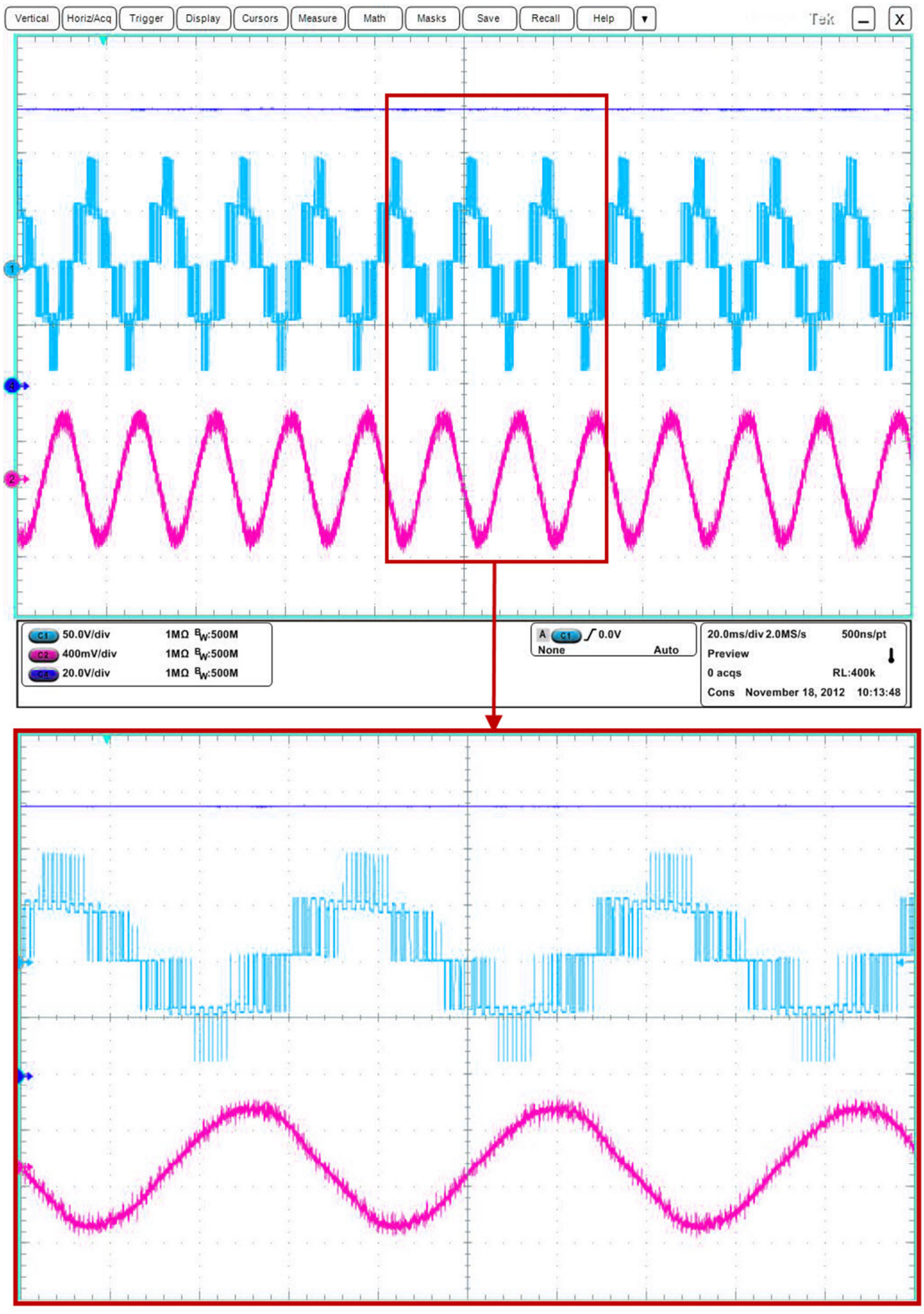

Figure 4.52 3L NPC in motor mode: Voltage and current measurement

4.7. Conclusion

In this chapter, the 2L / 3L VSI and their control techniques are discussed in detail. Both the 2L and the 3L NPC VSI controls are identical except their PI regulators gain parameters are different. The 3L NPC topology allows for medium voltage system. The main advantages of the medium voltage are reduction in distribution cost and higher power density of VSI module. The constant DC bus voltage control and active/reactive power control are discussed in detail. The control loop analysis is performed using Matlab Simulink control design toolbox. The system simulation model is developed in Matlab Simulink to verify control techniques. The experimental setup is discussed in detail including implementation of embedded coding for DSP TMS320F2812 fixed point processor. The experimental results match with the simulation results. In the next chapter energy efficient inverters are discussed in detail. The watt loss calculation for LCL filter, VSI, DC link capacitors, Disconnect, fan/blower is presented. The energy saving standby mode of operation is also discussed in detail.

5. Energy efficient inverter for wind power application

In this chapter, efficiency and standby mode of operation of power conversion unit for the wind power application is investigated. Mathematical model to calculate the power losses in three phase voltages source inverters, LCL filters, DC link capacitors and disconnect switches are presented. A comparison of inverter losses with sinusoidal pulse width modulation (SPWM), space vector PWM (SVPWM) and discontinuous PWM (DPWM) are discussed. Selection of the power modules based on switching frequency, effect of modulation and gate resistance are presented. Techniques to improve the efficiency of the power conversion units are provided. The standby mode of operation is proposed to save energy during unavailability of the wind power. The efficiency of power conversion unit is calculated based on mathematical model and compared with actual measurement.

5.1 Introduction

As discussed in previous chapters, voltage source inverter based power conversion units are used for wind power. The power conversion unit is made up of precharge, LCL filter, VSI, DC link capacitor and VSC (voltage source converter) or CSC (current source converter) as shown in figure 5.1. The efficient power conversion unit saves significant energy during life time operation. To calculate the efficiency, it is required to develop mathematic model of power loss calculation for each section of the power conversion unit. In following section, power loss calculations are presented for the

LCL filter, VSI and DC link capacitors. The novel techniques to reduce the losses are presented. In addition, due to uncertainty of the wind energy, it is important to place the power conversion unit in standby mode to reduce the energy consumption. The energy saving mode is discussed in detail in section 5.4.

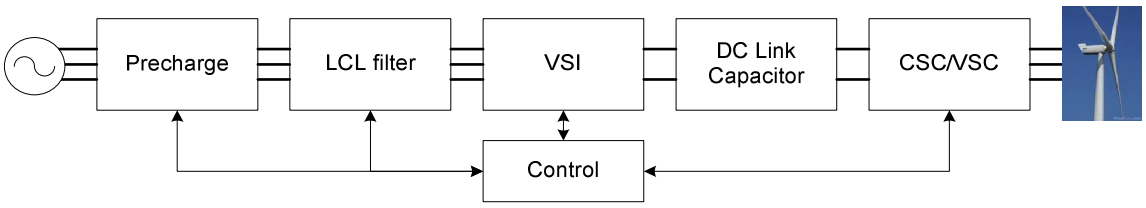

Figure 5.1 Power conversion unit for wind power application

5.2 Power losses in the LCL filter

5.2.1 Core loss

The losses in LCL filter are divided in to core losses and copper losses. The core losses of the LCL filter inductor can be calculated using the Steinmetz equation.

$$P_{Core\_loss} = kf^{\alpha}B^{\beta} \tag{1}$$

Where f is the frequency of the magnetic field, B is flux density, α and β are the coefficient. The total core losses can be divided in to three component: hysteresis losses P_h, eddy current losses P_e and excess losses P_a as shown in equations (2) and (3)[43].

$$P_{Core\_loss} = P_h + P_e + P_a \tag{2}$$

$$P_{Core\_loss} = k_h f B^n + k_e f^2 B^2 + k_a f^{1.5} B^{1.5} \tag{3}$$

Where the k_h ,k_e and n are the coefficients, which depend on the lamination material, thickness, and conductivity of the material. k_a is related to the material thickness, cross sectional area, conductivity and the material microstructure. The equation is only applicable for the sinusoidal flux density of varying magnitude and frequency. Modified steinmezt equation (MSE) is used to predict the losses of with non-sinusoidal waveforms [44][45].

$$P_{MSE\_Core\_loss} = k f_{eq}^{\alpha^{\alpha}} B^{\beta} \tag{4}$$

Where f_{eq} is an equivalent frequency, $f_{eq} = f$ for sine wave and for waveform other than sine wave can be calculated using equation (5).

$$f_{eq} = \frac{2}{\left(2\pi \frac{B_{pp}}{2}\right)^2} \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{5}$$

The use of grain oriented silicon steel and reduce lamination thickness can lower the core losses. In addition, reduce the length of each air gap and increase the number of air gaps with keeping the total air gap length constant can reduces the fringing effect and core losses.

5.2.2 Copper loss

It is easy to calculate copper losses for low frequency sine wave. The current in the LCL filter is not pure sine wave. Current is sum of fundamental (I_f) and harmonic

current (I_h). It means winding loss in the LCL filter inductor has skin and proximity losses. The total copper losses in LCL filter inductor is given by equation (8)

$$I = I_f + \sum I_h \tag{6}$$

$$P_{Cu\_loss} = P_{cu\_f} + P_{cu\_h} = R_f I_f^2 + \frac{1}{2} R_h \sum_n I_h^2 \tag{7}$$

$$P_{Cu\_loss} = P_{cu\_f} \left[1 + \tfrac{1}{2} \frac{R_h}{R_f} \sum_n \left(\frac{I_h}{I_f} \right)^2 \right] \tag{8}$$

Here, P_{cu_f} and P_{cu_h} are winding losses because of fundamental component and harmonic components respectively. The R_f is resistance for fundamental component and R_h is the equivalent resistance for the harmonic component. R_h includes the skin effect and proximity effect. The ratio of R_h to R_f can be calculated using equation below [46][47].

$$\frac{R_h}{R_f} = \sqrt{n} A \left[F_{rs} + \frac{2\left(N^2 - 1\right)}{3} F_{rp} \right] \tag{9}$$

$$F_{rs} = \frac{\sinh\left(2A\sqrt{n}\right) + \sin\left(2A\sqrt{n}\right)}{\cosh\left(2A\sqrt{n}\right) - \cos\left(2A\sqrt{n}\right)} \tag{10}$$

$$F_{rp} = \frac{\sinh\left(A\sqrt{n}\right) - \sin\left(A\sqrt{n}\right)}{\cosh\left(A\sqrt{n}\right) + \cos\left(A\sqrt{n}\right)} \tag{11}$$

$$A = \left(\frac{\pi}{4} \right)^{\frac{3}{4}} \frac{d}{\delta} \sqrt{\frac{d}{p}} \tag{12}$$

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f_{sw}}} \tag{13}$$

In the equations (10) & (11), n is the order of the harmonics, N is the number of turns, F_{rs} and F_{rp} are skin effect and proximity effect factors. In equation (12) & (13) d is the diameter of the winding, p is the winding pitch (i.e. the distance between the centers of the adjacent conductors in same layer) ρ is the resistivity of the winding, μo is the permeability of free space, f_{sw} is the switching frequency of the VSI and δ is the skin depth of the winding. Total power loss in the LCL filter can be given by equation (14)

$$P_{LCL\_loss} = P_{MSE\_Core\_loss} + P_{Cu\_loss} \tag{14}$$

5.3 Power losses in VSI/VSC/CSC

Conduction losses in IGBT can be express by equation as below:

$$P_{IGBT\_cond} = \frac{1}{T}\int_0^T V_{(t)} I_{(t)} dt \tag{15}$$

T is the fundament period. $V_{(t)}$ and $I_{(t)}$ are on state voltage drop across the IGBT and load current through the IGBT respectively. The on state voltage drop can be characterized by dynamic resistance of the IGBT r_o, collector to emitter voltage Vo, and the B is curve fitting constant as shown in equation (16) [48].

$$P_{IGBT\_cond} = \frac{1}{T}\int_0^T \left(V_o r_o i^B{}_{(t)}\right) \cdot i_{(t)} dt \tag{16}$$

For VSI application, the PWM signals are generated by comparison of the sinusoidal control signals to the either saw tooth or triangular carrier signals. The PWMs are used to drive the gate drivers of the IGBTs. Conduction losses in this case can be provided by equation (17) [47].

$$P_{IGBT\_cond} = \frac{1}{2}\left(V_0 \frac{I_{pk}}{\pi} + r_o \frac{I_{pk}^2}{4}\right) + m \cdot \cos\phi \cdot \left(V_0 \frac{I_{pk}}{8} + r_o \frac{I_{pk}^2}{3\pi}\right) \tag{17}$$

The modulation index m is less than 1 for linear mode of the PWM. During the over modulation $1<m<4/\pi$. Conduction losses of the IGBT increase with the higher load current, collector to emitter voltage and modulation index.

$$P_{IGBT\_SW} = f_{SW} \frac{1}{T} \int_0^{\frac{T}{2}} (E_{IGBT\_on} + E_{IGBT\_off})(i_{pk}, t)dt \tag{18}$$

The IGBT switching losses are given by equation (18). The E_{IGBT_on} and E_{IGBT_off} are the turn on and turn off switching losses of the IGBT and f_{sw} is the switching frequency of the IGBT. Switching losses are directly proportional to the switching frequency, load current and collector to emitter voltage. E_{IGBT_on} and E_{IGBT_off} are depend on the gate resistance of the gate drive board. Higher gate resistance leads to increase in switching losses but it will help reduces the dv/dt and di/dt and EMI of the VSI. In addition, it helps increase short circuit capability of power module. Similarly diode conduction losses for the VSI application can be given by equation (19). V_{toff} is the voltage across the diode and r_t is the dynamic resistance of the diode. Diode turn on losses is negligible compare to the reverse recovery losses. Diode switching losses are given by the equation (20).

$$P_{Diode\_cond} = \frac{1}{2}\left(V_{toff} \frac{I_{pk}}{\pi} + r_t \frac{I_{pk}^2}{4}\right) - m \cdot \cos\phi \cdot \left(V_{toff} \frac{I_{pk}}{8} + r_t \frac{I_{pk}^2}{3\pi}\right) \tag{19}$$

$$P_{Diode\_SW} = f_{SW} \frac{1}{T} \int_0^{\frac{T}{2}} E_{Diode\_off}(i_{pk}, t)dt \tag{20}$$

IGBT and diode switching loss calculation depends on actual measurement of the E_{IGBT_on}, E_{IGBT_off} and E_{Didoe_off}. The measurement can be made using double pulse test. The two gate pulses are applied to the IGBT. The first pulse is to close the IGBT and ramp up the current. Since the load is an inductor, the current should ramp linearly. The pulse is terminated when the current has reached the desired value. The current will switch to the freewheeling diode. This gives IGBT turn off losses and diode turn on losses. The second pulse is applied to turn on the IGBT at the present current level, which gives IGBT turn on losses and diode turn off losses. The flow of currents is shown in figure 5.2.The switching losses are calculated by multiplying the voltage and current waveforms. The energy can then be calculated as the area under the resulting waveform.

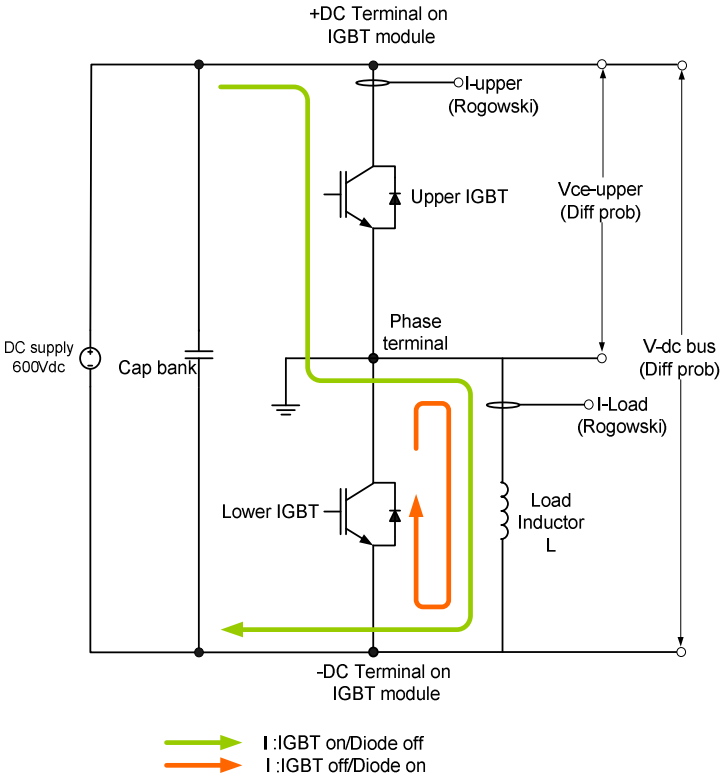

Figure 5.2 Double pulse test circuit

5.3.1 Double pulse test setup

The double pulse test setup is shown in figure 5.3. The IGBT, which is not under test, should be held open via reverse bias. This is necessary for the large module to ensure that this IGBT's does not closed during the test. The DC bus connection for the module under test should be place as close as possible to the DC capacitor bank to minimize parasitic inductance. Likewise, the gate drive board should also be placed close to the module to minimize the parasitic inductance.

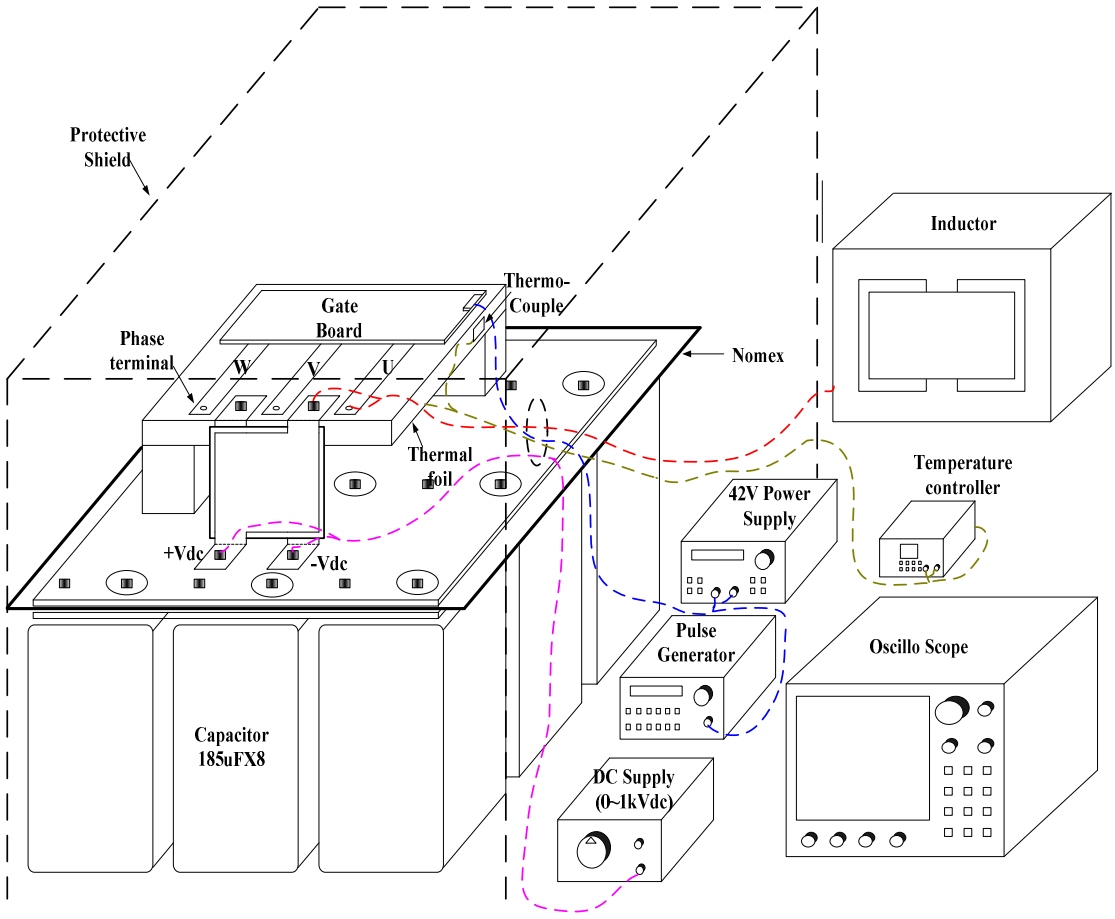

Figure 5.3 Setup for double Pulse Test

The especially design dc bus bars which connect capacitor bank to the IGBT module dc terminal introduce very low inductance (16nH or less). Also this setup incorporates thermo-foil at bottom of the module, thermo-couple at one side of the module, and temperature controller to perform the double pulse testing at 125C. There are two thermo-foil (Minco Inc) connected in parallel, each having resistance 267ohm and supply by 110Vac from SSR of the temperature controller (Omega Inc. Part # CN8200-T1-T2). The J type thermo-couple is used for measurement. It is easy to verify the base plate temperature and IGBT temperature are same or not by setting the temperature controller to 125C and turn it on and when the base plate temperature reach 125C, measure the NTC resistance which must be between 270-300Ω (NTC 125C ~ 275-300Ω). With this test, it can be confirmed that the thermo-foil works very well, without creating hot-spots. In this setup the load inductance used is 96uH. But it is more desirable to select load inductance such that current ramp up to desire value in (30-40us). The first pulse width will be defined by equation (21).

$$\Delta t = L \frac{\Delta I}{V_{Inductor}} \tag{21}$$

The space width should be chosen such that ringing from initial turn off has subsided. This is typically in range of 15-20uS. And the second pulse width should be long enough to capture turn on behavior, typically in range of 5-7uS. With 96uH load inductance, 72uS pulse required to reach 450A. Space intentionally keep wide (96uS), which helps IGBT cool down before turn on again. But this might heat the diodes. HP pulse generator is used to program precise pulse width for this setup. The second pulse width is in range of 10-12uS. Figure 5.4 shows the pulse diagram for the double pulse test setup.

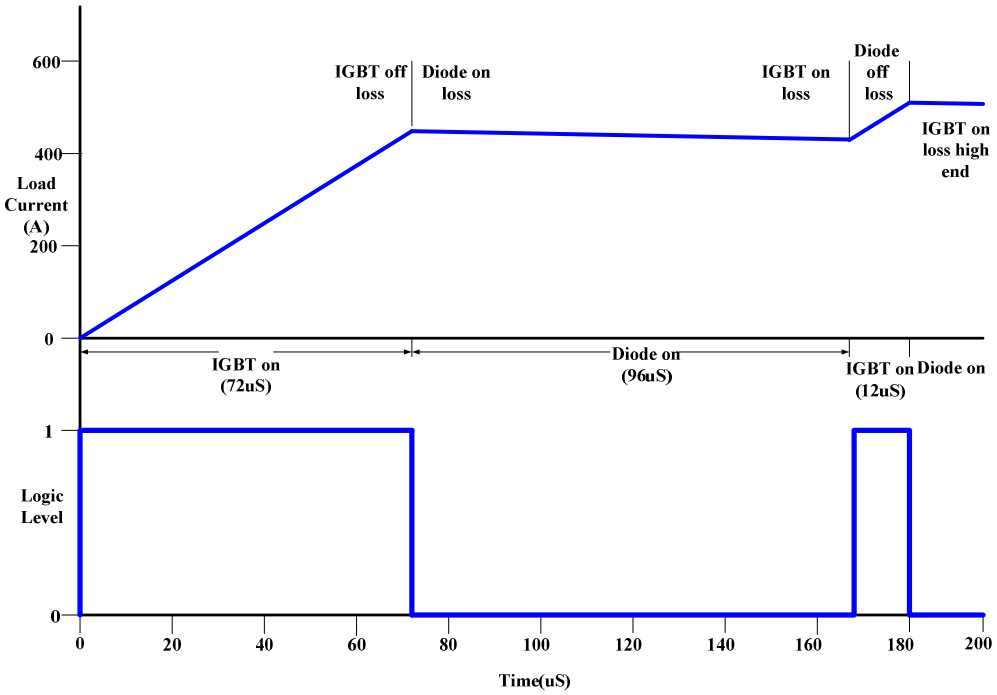

Figure 5.4 Double pulse diagram

The VSI power losses can be reduced by use of the appropriate power modules. For low frequency high power application Si power modules provide lower power losses. For higher frequency application SiC power modules deliver lower power losses compare to Si power modules [51]. The watt loss analysis is performed for two different Infenion power modules 1. FF600R12IS4F with SiC diode for high frequency application and 2.FF600R12IE4 for low frequency application. Figure 5.5 shows the conduction and switching losses for the IGBT. The SiC module conduction losses are higher than Si module. At 4 kHz switching frequency the switching losses in SiC unit is relatively lower compare to Si module. SiC switching losses at 8 kHz are significantly lower than Si module. Figure 5.6 shows the comparison between SiC and Si modules diode conduction and switching losses. Diode reverse recovery losses is highest in Si module at 8 kHz.

Figure 5.7 shows total power loss in Si and SiC module at 4 kHz and 8 kHz switching frequency. For low frequency application (<4 kHz) Si power module is better Vs SiC module and vice versa for high frequency (>8 kHz) application. It is very important to select appropriate power modules, low inductance bus structure and placement of the modules on heat sink to reduce the losses in power structure. The total loss in the VSI is given by equation (22). n_1 and n_2 are number of IGBT and Diode in VSI Power Structure.

$$P_{VSI\_loss} = n_1\left(P_{IGBT\_cond} + P_{IGBT\_SW}\right) + n_2\left(P_{Diode\_cond} + P_{Diode\_SW}\right) \quad (22)$$

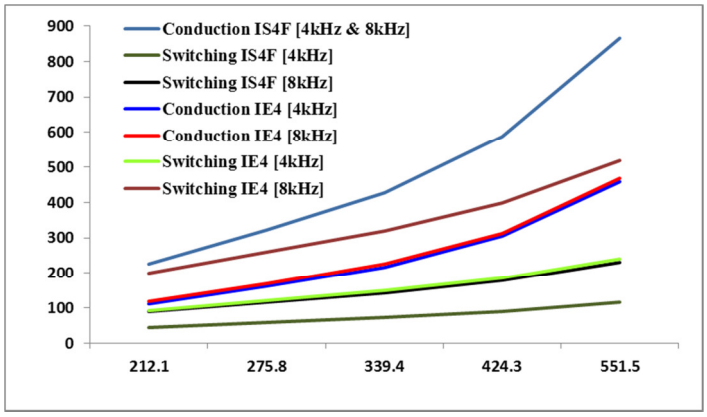

Figure 5.5 IGBT conduction and switching losses for Si and SiC unit

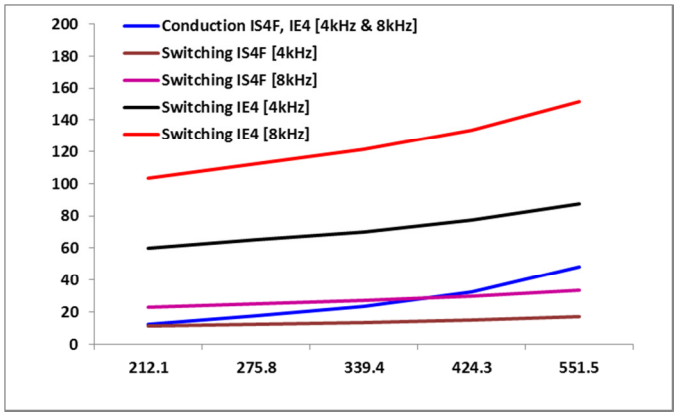

Figure 5.6 Diode conduction and switching losses for Si and SiC unit

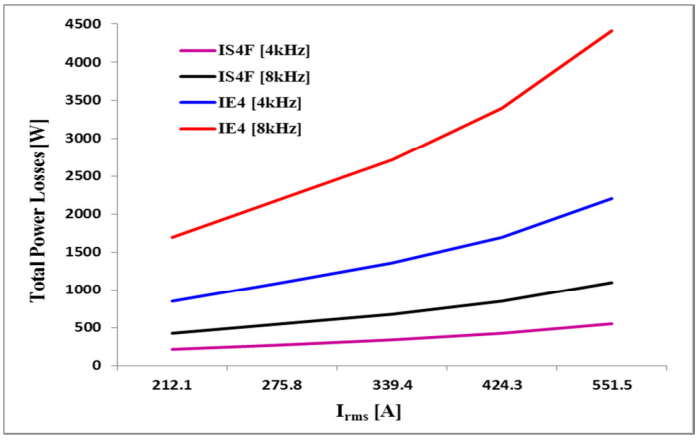

Figure 5.7 Total power losses for Si and SiC unit

The losses in the VSI is also depends on the pulse width modulation (PWM) used to control inverter switching to achieve a variable voltage, variable frequency output [50]. There are mainly two types of PWM techniques used for the VSI. 1. Continuous PWM (CPWM), 2. Discontinuous PWM (DPWM). In CPWM, the modulating signal is a continuous time varying signal, examples of which include conventional sinusoidal PWM (SPWM), space vector PWM (SVPWM), and third-harmonic injection PWM (THIPWM) as shown in figure 5.8. SVPWM was developed to increase the dc-link utilization from m_a=1 in the case of SPWM to m_a=1.15 where m_a is the modulation index. In case of the DPWM modulation technique, the modulating signal is clamped to the dc-link voltage for one third of the period and there is no switching instant during this time. The starting phase angle ψ determines the zero-sequence signal and, hence, the type of DPWM scheme. In DPWM0 $\psi = 0$; DPWM1 $\psi = \pi/6$; and DPWM2 $\psi = \pi/3$. DPWM also provides a linear range of modulation index of m_a=1.15, but by utilizing a discontinuous modulating signal, it reduces switching losses to one third of the SVPWM or THIPWM as given by equation (23). The conduction losses in case of the DPWM increase but the

overall losses in power module is lower compare to SVPWM. DPWM with $\psi = 0$ is shown in figure 5.9.

$$P_{DPWM\ \_SW} = \frac{1}{3} P_{SVPWM\ (THIPWM\ )\_SW} \tag{23}$$

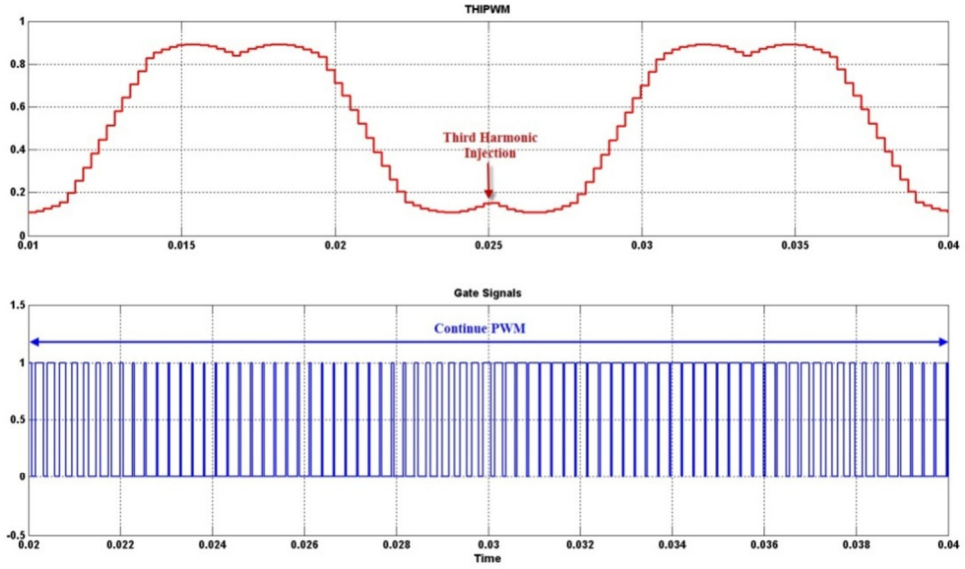

Figure 5.8 THIPWM control signal and PWM gate pulse

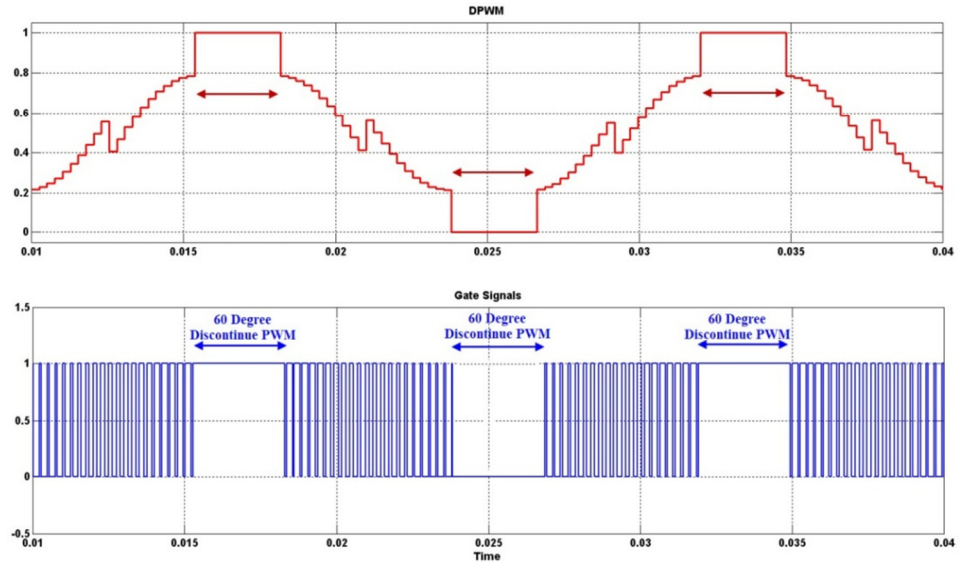

Figure 5.9 DPWM control signal and PWM gate pulse

5.4 Power losses in DC link capacitor and miscellaneous losses

DC capacitor bank is made up of combination of the series parallel connected capacitors to meet the voltage withstand capacity and to achieve the capacitance requirement for the system. Every capacitor has different leakage current. To keep the balance voltage across each capacitor in series connected capacitors required balancing resistor. Balancing resistor requirement is based on type of capacitor and leakage current. In addition each capacitor has equivalent series resistor (ESR). The total losses in DC link capacitors are given by equation (24). R_b is the balancing resistor and R_{ESR} is the capacitor bank equivalent series resistor. Low ESR and lower leakage current capacitor leads to lower overall DC link power loss.

$$P_{DClink\_loss} = \frac{V_{dc}^2}{R_b} + I_{dc} R_{ESR} \tag{24}$$

There are some miscellaneous losses such as losses in switch disconnect, fuses, bus bar or wires, control transformers and fans/blowers. Even though these losses are lower compare to the power modules and LCL filter losses, it is important to consider for efficiency calculation. Some losses like control transformer and fan/blower losses are continues losses even though unit is not running. All this losses can be lump together as miscellaneous losses P_{misc_loss}. Higher efficiency fan/blower with speed control, copper bus bars with tin plating, and lower contact resistance switch disconnect provide lower the miscellaneous losses.

5.5 Efficiency and standby mode of operation

The losses in the power conversion system are dominated by the LCL filter and VSI/VSC/CSC power structures. For higher switching frequency application (>=8kHz), SiC power modules will reduce the losses in VSI/VSC/CSC. The higher switching frequency reduces the size of LCL to attenuate the switching frequency component but it increase the core loss in LCL. The core losses can be improved by using better core material and thinner laminations. For low switching frequency application, the Si power modules are better option compare to the SiC power modules. The size of the LCL gets bigger to attenuate the low switching frequency (<= 4 kHz) components but the core losses are lower. With use of the DPWM technique, VSI switching losses can be further reduces. It is important to note that the DPWM increase losses in the LCL. The selection of SVPWM Vs DPWM method requires balance power loss between the LCL and VSI.

In wind power application, 40% of the time power conversion devices (LCL, VSI/VSC/CSC) are idle (not generating active power) because of unavailability of the wind. In idle mode, VSI and VSC/CSC are modulating at no load. The circulating current through LCL filter generates the core losses in inductors. To keep the filter and VSI/VSC unit cool, fan/blower need to run all the time. It means when unit is not generating any power it is actually consumes significant energy. In order to reduce power loss in LCL filter and VSI/VSC unit and reduce energy consumption by fan/blower, placed the power conversion devices in standby mode. In standby mode, just requires

control power [65]. Disconnect and/or shut down devices which generate power losses or consume energy. The flow chart of the standby mode operation is given below.

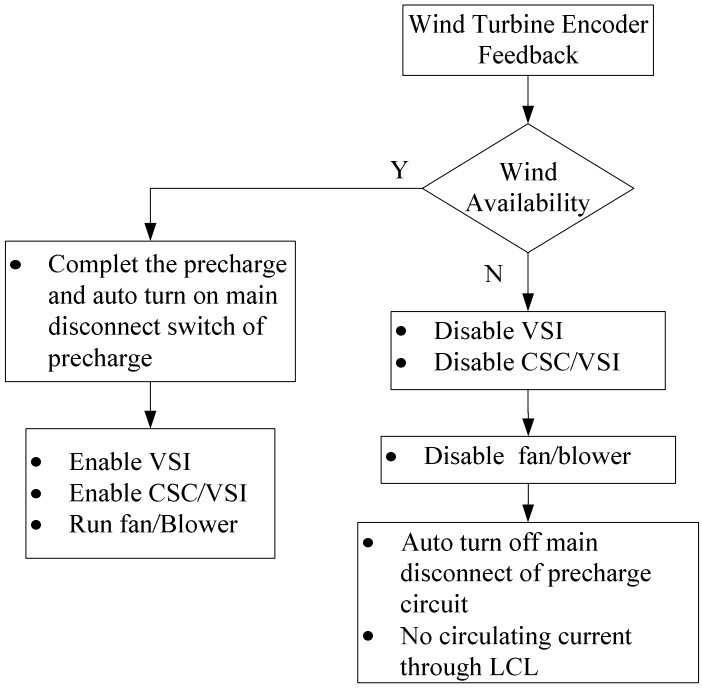

Figure 5.10 Flow chart for standby mode of operation

5.6 Experimental result

Efficiency of the 300HP VSI-VSC unit is calculated and compared with actual measurement. Infineon 450A IGBT power module is used in VSI/VSC. The same power module is used for double pulse test setup is shown in figure 5.11. Using double pulse set up, the E_{IGBT_on}, E_{IGBT_off} and E_{Didoe_off} measurements are performed. It is used for the calculation of the switching losses of the IGBT and Diode. Figure 5.12 and 5.13 shows the IGBT on and off losses waveform at 450A. IGBT on loss is 59mJ and IGBT off loss is 89mJ. Diode turn off loss measurement waveform is shown in figure 5.14. Diode

reverse recovery loss is 10.46mJ. Using this measurement value as well as IGBT and Diode conduction and switching loss equations, power losses are calculated for 2-level VSI and VSC in regenerative mode of operation. Conditions for VSI and VSC power loss calculations are shown in Table 5.1. The losses are calculated at 4 kHz switching frequency with max junction temperature at 125C. Assumption for the grid and the wind generator side power factors are .98 and 0.88 respectively. The VSI and VSC combine watt loss is 6.918kW. Table 5.3 shows the breakdown of the losses in the VSI in inverter and rectifier mode. The losses are calculated for regenerative application, where the energy is feedback to grid. The IGBT conduction and switching losses higher compare to the diode loss in case of rectifier mode. Diode conduction losses are higher compare to IGBT conduction loss in inverter mode.

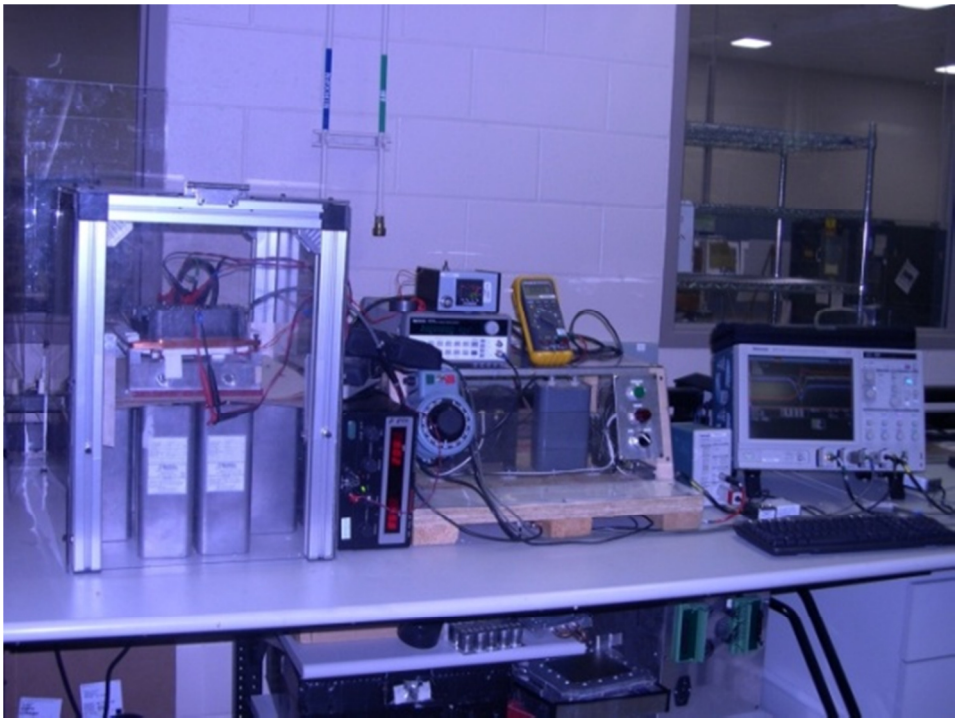

Figure 5.11 Actual double pulse test setup

Switching Frequency	4000Hz
Modulation Index	1
Fundamental Frequency	60Hz
Junction Temperature	125C
Case Temperature	80C
Inverter Power Factor	0.98
Rectifier Power Factor	0.88

Table 5.1. Conditions for VSI watt loss measurement

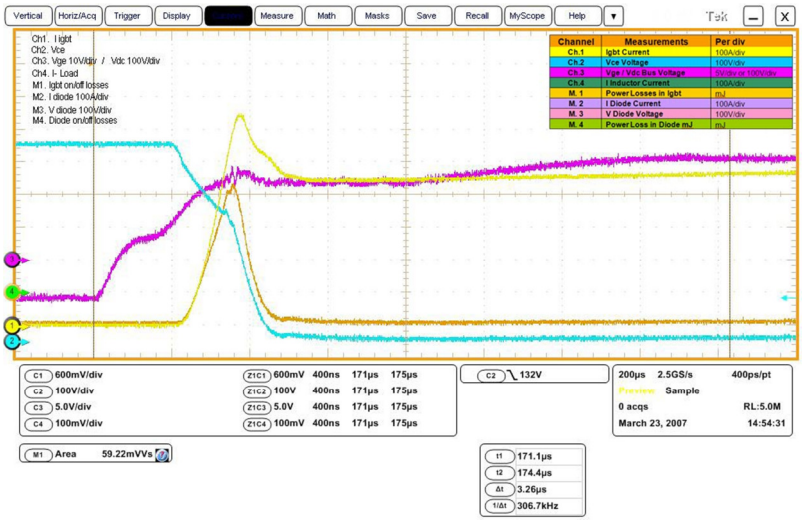

Figure 5.12 IGBT ON loss at 450A

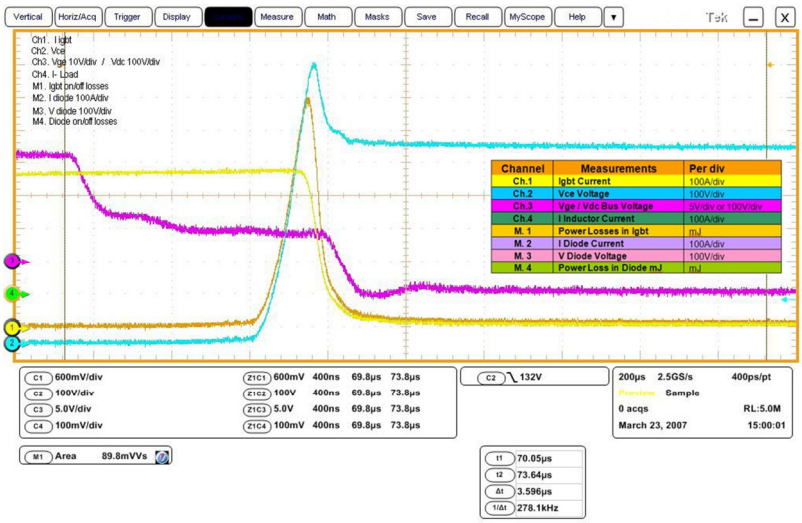

Figure 5.13 IGBT OFF loss at 450A

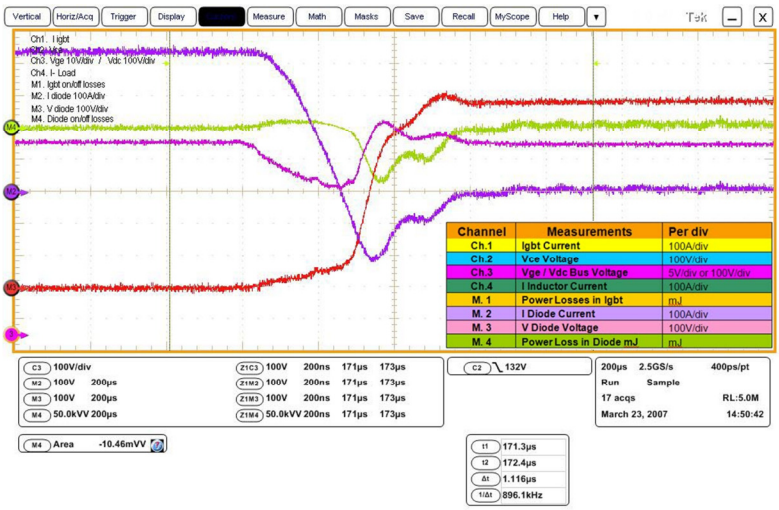

Figure 5.14 Diode OFF loss at 450A

L_g Cu loss [W]	L_g Core loss [W]	L_c Cu loss [W]	L_c Core loss [W]	P_{LCL_loss} [w]
520	186	1213	440	2359

Table 5.2. Power loss breakdown in LCL filter

	Mode of Operation	I_{RMS} [A]	P_{IGBT_Cond} [W]	P_{IGBT_SW} [W]	P_{Diode_Cond} [W]	P_{Diode_SW} [W]	P_{VSI_loss} [W]
Rectifier	**Regen**	360	109	330	48	55	3252
Inverter	**Regen**	360	70	353	129	59	3666

Table 5.3. Power loss breakdown in VSI unit in Regen mode

For the 300Hp unit the grid side inductor Lg is 60uH and line side inductor is 180uH. Using the inductor core loss and copper loss equations, inductor losses are calculated as shown in Table 5.2. The control transformer rated for 750VA, and the blower input rating is 240VAc, 2A (480VA). Balancing resistor for the DC capacitor bank is 8 kΩ which translates in to 61W loss. ESR of the DC capacitor bank is 2mΩ

leads to 256W power loss. The total loss in system is equal to 10.34kW which does not include Bus bars, fuse and switch disconnect losses. The calculated efficiency of the power conversion system is 95.9%. The actual measurement of the unit efficiency was performed using yokogawa power meter. The measurement is shown in Table 5.4. The input voltage and current waveform are shown in figure 5.15. The efficiency is in range of 96%, which is very close to the calculated efficiency.

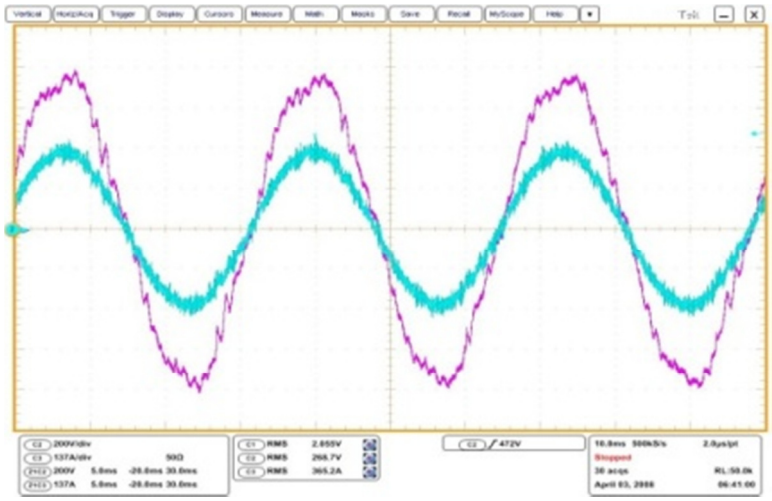

Figure 5.15 Input voltage and current waveform for 300Hp unit

Unit Loading	Power Out (Watts)	Power In (Watts)	Drive Efficiency	Voltage In	Current In	Voltage Out	Current Out	Power Factor
180A (50%)	117570	121850	96.49	464.75	158.63	445.47	177.95	0.95
270A (75%)	170020	176390	96.39	452.84	228.55	416.17	263.02	0.98
360A (100%)	246210	255630	96.31	466.82	317.54	447.9	351.53	1.00

Table 5.4. Measured efficiency for 300Hp unit at different load condition

If the power conversion unit is running at no load condition during unavailability of the wind, the circulating current though the LCL unit for 300HP is around 35Arms. The total

core loss in LCL is around 626W. The loss in capacitor bank is 61W across balancing resistor. Assume negligible losses in VSI, VSC, bus bars and fuses at no load condition. Blower is still required to keep the LCL and other component cool. Total watt loss is around 1.067kW when power conversion unit running at no load condition. By placing the unit in to standby mode, 1kW watt loss can be avoided for 300Hp unit. In wind farm, multiple MW units are installed. Placing these units in standby mode during unavailability of wind, a significant amount of energy can be saved.

5.7 Conclusion

In this chapter, efficiency calculation for the power conversion devices is provided in detail. LCL filter, VSI and DC link capacitors power losses are calculated. Calculation of the VSI switching losses requires IGBT and Diode turn on and turn off losses. Double pulse test method to measure the IGBT and Diode turn on and turn off loss are discussed in detail and verified with experimental setup. The calculated efficiency is compared with the measured efficiency of the power conversion devices. Measured efficiency is very close the calculated efficiency. Power conversion unit standby mode of operation is provided using flow chart. The total energy saving by standby mode of operation for 300Hp unit is provided in experimental results. In following section, standards for the frequency and voltage regulation are reviewed for different grid codes. Proposed medium voltage based DC distribution system are discussed in detail with its advantage and novel control for frequency and voltage droop support are provided with simulation and experimental results.

6. MVDC distribution system: frequency and voltage droop support

In this chapter the novel medium voltage DC distribution system is presented in detail. The MVDC distribution system has many advantages includes grid support, cost efficiency and power density etc. In order to offer grid support, overview of the grid standards is provided for different grid systems. The main focus is on the frequency and voltage droop support. The novel control for the frequency and voltage droop support is provided in this chapter. The control loop analysis is performed using single phase equivalent frequency and voltage droop model in Matlab control design toolbox. The relationship between the grid frequency and grid inertia is established in terms of mathematical model. The simulation model of the system with frequency and voltage droop support is generated in Matlab Simulink. The experimental setup for the system is discussed in detail. The simulation and experimental results are compared, which shows that the system is able to support the grid to increase its stability and reliability.

6.1. Overview of the grid standard

As renewable energy penetration level increase in power grid system, power system operator are challenged by the penetration impacts to maintain reliability and stability of the power system. Therefore, grid codes are being published and updated by transmission and distribution system operator of the different country. In this section the recent grid codes used in conjunction with the large wind farm integrated to electric grid are analyzed and compared.

6.1.1. Active power requirement and frequency regulation

The grid codes impose the operational frequency ranges for wind power generators as given in Table below [49] [52]. Based on requirements, the wind powers are required to operate continuously between 47.5Hz and 52Hz for the most of the grids. For the frequency ranges between 47 and 47.5Hz as well as between 52 and 53Hz, the wind power generators need to operate for limited time duration. This is very wide range in relation to realistic events. This is due to the wide swing of active power demand and supply at any instant of the time. Nevertheless a model of a wind turbine should be able to operate within this range. Outside this range wind power generators need to isolate itself from the grid.

Frequency range requirement					
Frequency (Hz)	Minimum Time Delay				
	Denmark[2]	Germany[3]	Ireland[4]	Scotland[5]	UK [6]
52 Hz t to 53 Hz	3 min	%	%	%	%
51.5 Hz to 52 Hz	30 min	%	60 min	Continuous Operation	Continuous Operation
51.0 Hz to 51.5 Hz	30 min	Continuous Operation	60 min	Continuous Operation	Continuous Operation
50.5 Hz to 51.0 Hz	30 min	Continuous Operation	60 min	Continuous Operation	Continuous Operation
49.5 Hz to 50.5 Hz	Continuous Operation	Continuous Operation	Continuous Operation	Continuous Operation	Continuous Operation
49.5 Hz to 47.5 Hz	30 min	Continuous Operation	60 min	Continuous Operation	Continuous Operation
47.5 Hz to 47.0 Hz	3 min	%	20 sec	20 sec	20 sec
>47.0 Hz	%	%	20 sec	20 sec	20 sec

Table 6.1 Operational frequency range requirement for different grid

According to the National Grid code, during the frequency support operating mode which will result in active power output changing, in response to a change in system frequency, in a direction which assists in the recovery to target frequency (50/60Hz), by operating so as to provide primary (Pri) response and/or secondary(Sec) response and/or high frequency response [50][51]. Primary response is defined as the automatic increase in active power output of a generator set or, as the case may be, the decrease in active power demand in response to a system frequency falls. This increase in active power output or, as the case may be, the decrease in active power demand must be in accordance with the provisions of the relevant ancillary services agreement which will provide that it will be released increasingly with time over the period 0 to 10 seconds from the time of the start of the frequency fall on the basis set out in the ancillary services agreement and fully available by the latter, and sustainable for at least a further 20 seconds.

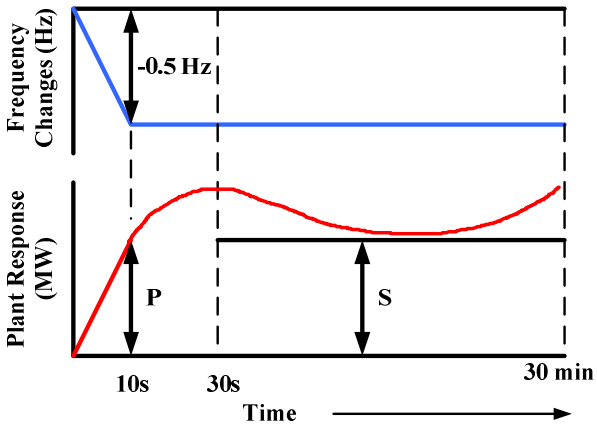

Figure 6.1 Pri and Sec response requirement for frequency support

The interpretation of the primary response to a – 0.5 Hz frequency change is shown diagrammatically in figure 6.1. Secondary Response is defined as the automatic increase in active power output of a generator set or, as the case may be, the decrease in active

power demand in response to a system frequency falls. This increase in active power output or, as the case may be, the decrease in active power demand must be in accordance with the provisions of the relevant ancillary services agreement which will provide that it will be fully available by 30 seconds from the time of the start of the frequency fall and be sustainable for at least a further 30 minutes. Figure 6.1 also shows the interpretation of the Secondary Response to a -0.5 Hz frequency change from reference frequency.

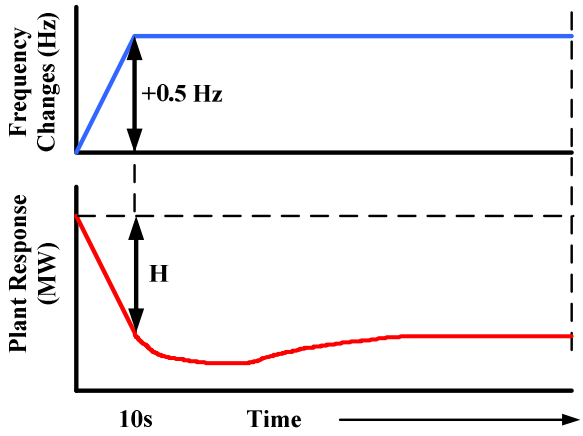

Figure 6.2 High frequency response requirements for grid

High frequency response is defined as an automatic reduction in active power output in response to an increase in system frequency above the target frequency. This reduction in active power output must be in accordance with the provisions of the relevant ancillary services agreement which will provide that it will be released increasingly with time over the period 0 to 10 seconds from the time of the frequency increase on the basis set out in the ancillary services agreement and fully achieved within 10 seconds of the time of the start of the frequency increase and it must be sustained at no lesser reduction thereafter.

The interpretation of the high frequency response to a + 0.5 Hz frequency change is shown diagrammatically in figure 6.2.

The wind power falls under the intermittent power source and can be part of the primary responder in case of the sudden change of the frequency. This can be accomplished if wind power is available with battery backup or other means of energy storage system [58]-[62]. It enables the wind power to push enough active power to the grid for 10sec to keep frequency within limit. Similarly, the wind energy also falls under the high frequency responder. It will store additional active power to the battery during high frequency condition.

6.1.2. Reactive power requirement and the voltage regulation

Reactive power refers to the circulating power in the grid that does no useful work. It is results from energy storage elements in the power grid (mainly inductors and capacitors). It has a strong effect on system voltages. Reactive power levels have an effect on voltage collapse.

Past event related to reactive power as summarized below.

- Voltage drops related to reactive power contributed to blackouts in the West (1996) and in the France (1978)
- PJM itself came close to a blackout due to reactive power problems in 1999

• Significant voltage swings due to the reactive power in the Midwest and Northeast in 2003

Reactive power is used to regulate the grid voltage to a desired nominal value. Often, the reactive power injections regulate the voltage at the location of the injection. The control effects tend to be localized. Few reactive power supply mechanisms identify by different grid are as below;

- Shunt capacitors (fixed and switchable)
- Synchronous condensers
- Synchronous generators
- Static VAR compensators

The grid imposes some indirect requirement of reactive power consumption by the wind power in terms of power factor [49][51]. Simple induction generator, with no additional capacitors attached, will during normal operation consume reactive power. This reactive power has to be produced somewhere in the grid. It is preferred that the wind power consume minimum reactive power, since the distribution of reactive power is relatively cost intensive. The requirements of the reactive power and the power factor are relatively similar in the different Grid Codes as shown in table 6.2. Generally it is in range of the 0.95 lagging to 0.95 leading power factor but sometimes it is depends up the unit rating.

Power factor requirement for selected grid code						
	Canada	**Denmark**	**Germany**	**Ireland**	**Scotland**	**UK**
Static, continues power factor	0.9 lagging to 0.95 leading	Q/Prated=0 to Q/Prated =.1 at full production and through a straight line to Q/Prated =-0.1 to Q/Prated =0 at zero production	0.95 lagging to 0.95 leading for a rated active power capacity <100MW. For a rated active power capacity > 100MW the power factor is voltage dependent.	0.95 lagging to 0.95 leading at full production. 32.6MVAr per 100MW installed, active capacity from 100% production to 50% production. 0.95 lagging to 0.95 leading from 50% production to idle.	0.95 lagging for production between 100% - 20%. 0.95 leading for production between 100% to 50%.	0.95 lagging to 0.95 leading

Table 6.2.Power factor requirements for different grid

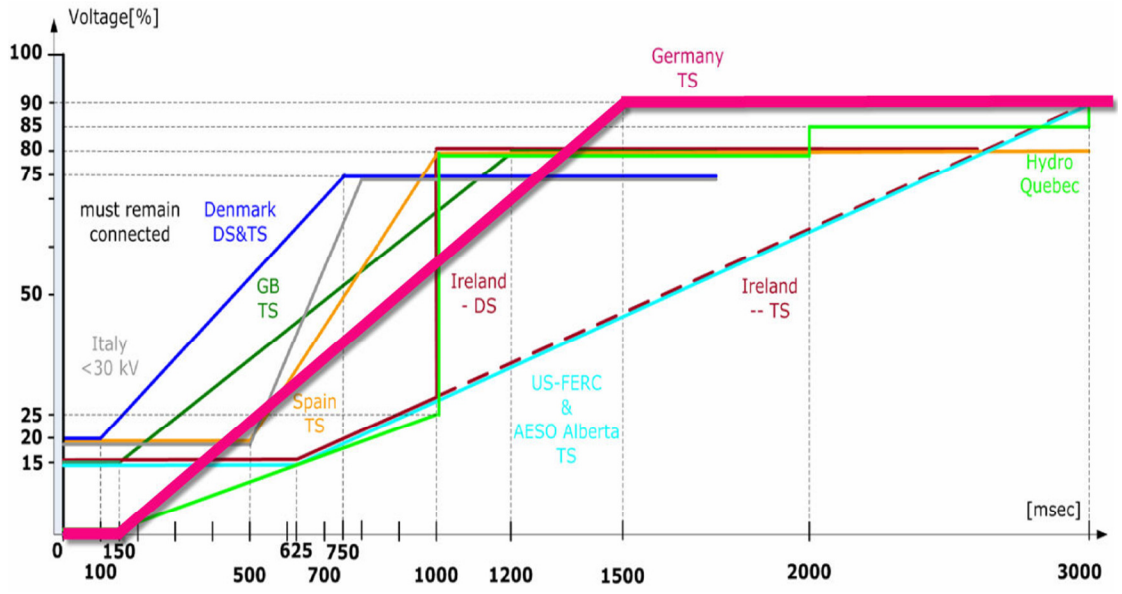

Figure 6.3 Low voltage ride though chart, source NREL

In addition to power factor requirements, grid codes require some level of fault ride-through capabilities for the wind power. A summary of these requirements are given in table 6.3. Voltage profiles are given in figure 6.3 specifying the depth of the voltage dip and the clearance time as well. However, in some of the grid codes the calculation of the voltage during all types of unsymmetrical faults is very well defined e.g Ireland, while other country does not define clearly this procedure.

Country	Voltage Level	Fault ride-through capability				
		Fault duration	Voltage drop level	Recovery time	Voltage profile	Reactive current injection
Denmark	DS	100 msec	25%Ur	1 sec	2, 3-ph	no
	TS	100 msec	25%Ur	1 sec	1, 2, 3-ph	no
Ireland	DS/TS	625 msec	15%Ur	3 sec	1, 2, 3-ph	no
Germany	DS/TS	150 msec	0%Ur	1.5 sec	generic	Up to 100%
UK	DS/TS	140 msec	15%Ur	1.2 sec	generic	no
Spain	TS	500 msec	20%Ur	1 sec	generic	Up to 100%
Italy	> 35 kV	500 msec	20%Ur	0.3 sec	generic	no
USA	TS	625 msec	15%Ur	2.3 sec	generic	no
Ontario	TS	625 msec	15%Ur	-	-	no
Quebec	TS	150 msec	0%Ur	0.18 sec	Positive-sequence	no

Table 6.3. Low voltage ride through requirement for different grid

The voltage profile for ride-through capability can be summarized as shown in figure 6.3. The German grid code requires wind power installations to remain connected during voltage sags down to 0% from the rated voltage at the PCC for duration of 150 msec. Moreover, during the fault a reactive current injection up to 100% is required. Same requirement regarding reactive current injection is present in the Spanish grid code. This

demand is relative difficult to meet by some of the wind turbine concepts due to lack of energy storage system.

6.2 Medium Voltage DC distribution system for wind power applications

The proposed MVDC distribution for the wind farm is shown in figure 6.4. The power generated by the generators is converted to the DC form. The DC to DC converters are used so that the DC bus voltage can be higher than the generator voltage. The power is collected from all the turbines and transferred to the grid side converters. Multiple large size inverters transfer the power to the utility grid. The generator side converters adjust the power from the turbines and can place them on Maximum Power Point Tracking (MPPT). The grid side inverters can either keep DC bus voltage of system constant or inject active reactive power to the grid or support the frequency and voltage droop. The energy storage components (ultra- capacitor and batteries) are either directly connected to the DC system or connect via DC/DC converter. They exchange power with the DC system to perform power rate control, power smoothing, power shifting, and transient stability control. The rating of the generator side converter can be half of the conventional double conversion converters. The DC distribution system is also more efficient, cost effective, and easier to control. Figure 6.5 shows the actual output power profile of a 72MW wind farm in Wisconsin for 1AM (high wind) and 1PM (low wind). The actual capacity factor at 1AM is 43.7% and at 1PM is 26%. The typical capacity factor of the wind turbines and farms are around 30%. For individual wind turbines the grid side inverter is rated at the maximum power of the turbine. In the proposed system,

since fewer high power inverters are utilized, a power averaging is applied. Grid side inverters maybe rated at lower power ratings. In addition, if power smoothing by generator side converters and energy storage elements are performed, the total rating of the inverters can be lowered. Furthermore, if medium voltage grid side inverters are used, conventional grid side transformers could be avoided [32][33]. This will provide a large cost saving for the system. The goal is to achieve higher overall efficiency and reliability at lower cost compared to the existing AC distribution systems. Another added advantage of the DC distribution system is significant cost saving in terms of installation of distribution network as mention in chapter 1.

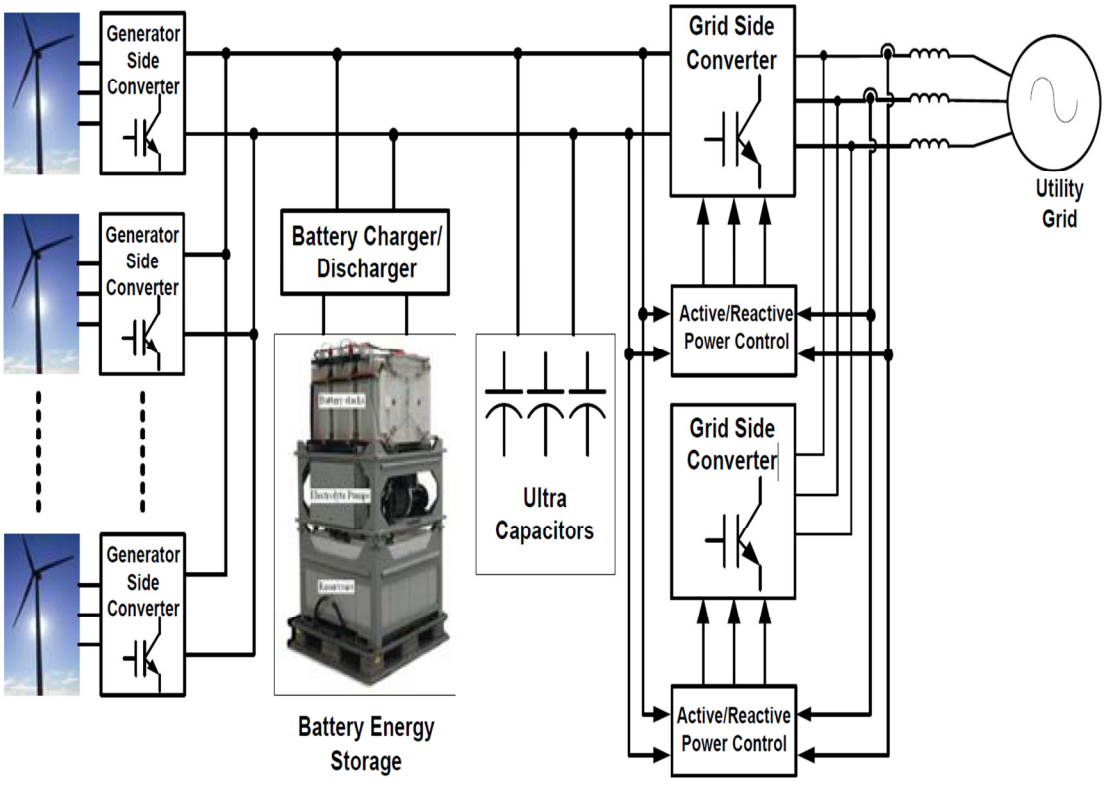

Figure 6.4 Proposed MVDC distribution system

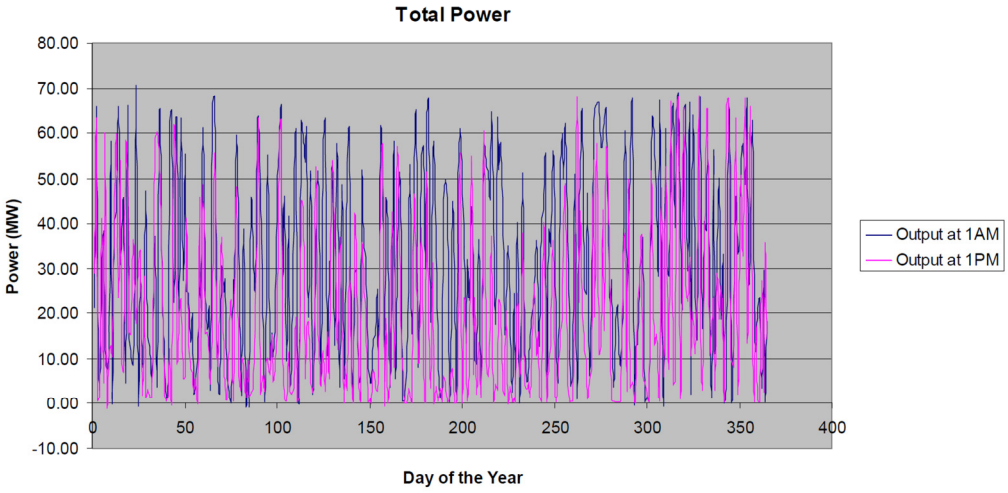

Figure 6.5 Power profile of 72MW wind farm at 1AM & 1PM during a year

The most important application of the MVDC system is to provide the frequency and voltage droop control. Grid tried to control the frequency within the limit specified by the electric supply regulation. Limit on the frequency are in range of +/-1% of the rated frequency. Grid must need to ensure that sufficient generation and / or demand are held in automatic readiness to manage all credible circumstances that might result in frequency variations [54]. As renewable installed capacity is significant part of the total grid capacity, the renewable energy system must support the frequency variation control even for short duration before the conventional frequency control mechanism as shown in figure6.6 kicks in. Governor control takes 6-60sec to respond to the frequency variation whereas the automatic generation control takes up to 5 minutes to respond. Last alternative is the load shedding. The proposed MVDC system with ultra-capacitors and battery backup with DC/DC converter can allow the VSI to support frequency droop for short duration before the automatic generation control take appropriate action. Similar requirements for the reactive power supply to keep the AC voltage within the range.

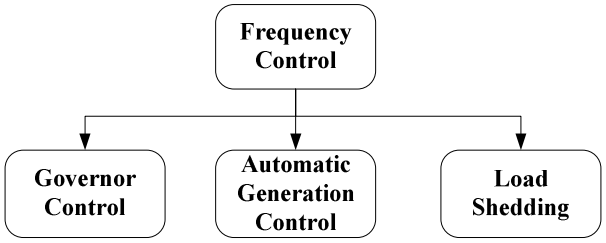

Figure 6.6 Conventional frequency control techniques for grid

Figure 6.7 shows the overview of the control used for the MVDC distribution system for the wind power application. The generator side converter (VSC) is use the MPPT algorithm to converter AC to DC. The DC/DC converter is used to charge the battery as well as to keep the DC bus the system constant. The grid tie inverter is used for frequency and voltage droop control to support the grid. The detail of the frequency and voltage droop control is provided in next section.

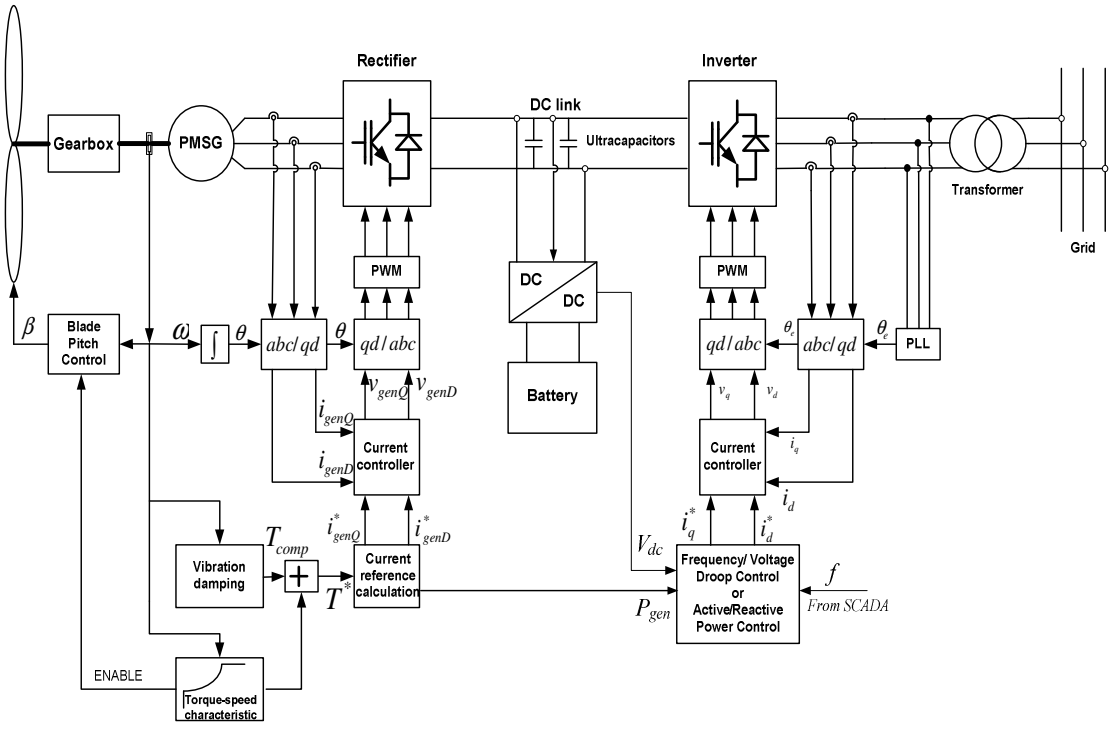

Figure 6.7 Over view of MVDC system with frequency and voltage droop control

6.3. Frequency droop and voltage droop control

Consider the AC system with two nodes as shown in figure 6.8 with generator and load is connected to node 2, whereas the wind power is connected to node1. This simple system is used to develop the frequency droop control and voltage droop control which can also be applied to the complex grid. Transmission line impedance is given by equation (2). Node 1 is considering the reference node with voltage $V_1\angle 0$, whereas node 2 is at voltage $V_2\angle\delta$. The vector diagram of the simplified system is shown in figure 6.9.

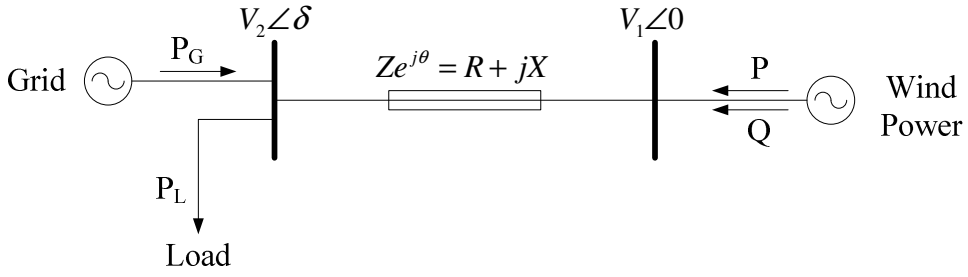

Figure 6.8 Simplified model of MVDC interface system with two nodes

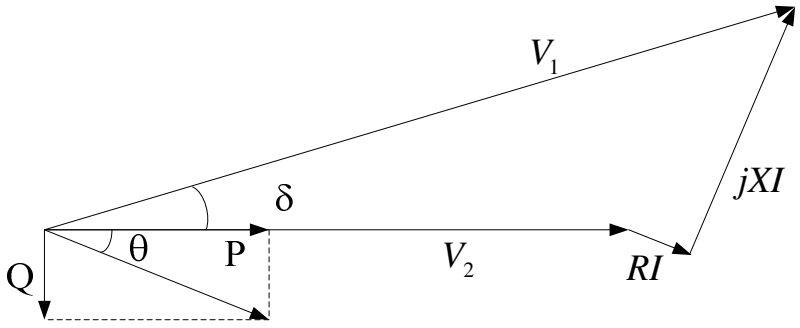

Figure 6.9 Vector diagram of two node system

The power flow equation of the system is given by equation (1), which can be simplified in form of equation (3) and (4) as below.

$$S = P + jQ = VI^{*} \tag{1}$$

$$Ze^{j\theta} = R + jX \tag{2}$$

$$P = \frac{V_1}{R^2 + X^2}\left(RV_1 - RV_2\cos\delta + XV_2\sin\delta\right) \tag{3}$$

$$Q = \frac{V_1}{R^2 + X^2}\left(XV_1 - XV_2\cos\delta - RV_2\sin\delta\right) \tag{4}$$

For Transmission line, inductance is much greater than resistance, neglect resistance R and take θ=90 Thus,

$$P = \frac{V_1V_2\sin\delta}{X} \tag{5}$$

$$Q = \frac{V_1^2}{X} - \frac{V_1V_2\cos\delta}{X} \tag{6}$$

If power angle δ is small, in this case cosδ=0 and sinδ=δ

$$\delta = \frac{PX}{V_1V_2} \tag{7}$$

$$Q = \frac{V_1(V_1 - V_2)}{X} \tag{8}$$

Variation in real power lead to change in frequency and variation in reactive power leads to variation in the voltage magnitude of the nodes.

$$\delta_1 - \delta_2 = (\omega_1 - \omega_2)t = \frac{(P_1 - P_2)X}{V_1V_2} \tag{9}$$

$$(V_1 - V_2) = Q\frac{X}{V_1} \tag{10}$$

$$(f_1 - f_2)t = \frac{(P_1 - P_2)X}{2\pi V_1 V_2} \tag{11}$$

Frequency susceptibility factor K_{pf} and voltage susceptibility factors K_{qv} can be defined based on equations (12) and (13) as below [63].

$$K_{pf} = \frac{\Delta P}{\Delta f} \tag{12}$$

$$K_{qv} = \frac{\Delta Q}{\Delta V} \tag{13}$$

The grid supply is mostly dominated by the synchronous generator. The synchronous generator inertial constant is given by equation (14)

$$H = \frac{\frac{1}{2}J\omega^2}{MVA} \tag{14}$$

Where H = Inertia constant in MWs / MVA, J is moment of inertia in kgm^2, ω is nominal speed of rotation in rad/s and MVA is the rating of the machine. The inertial response of a synchronous generator is the initial power injection to the transmission system following a change in system frequency caused by a disturbance such as a loss of generation or sudden increase in demand. The inertia constant is defined as the stored energy in the rotating mass at the rated speed in MWs/MVA. The majority of generators connected to the grid transmission system have an inertia constant H of between 3MWs/MVA and 9MWs/MVA. After a system disturbance which results in an imbalance between supply and demand, the inertia prevents an instantaneous change in speed. The rate of change of the speed will be governed by the following equation:

$$\Delta f = \frac{\Delta P}{2H} \tag{15}$$

Frequency susceptibility factor K_{Pf} can be define in term of inertia constant as below:

$$K_{pf} = 2H \tag{16}$$

Figure 6.10 and 6.11 show the frequency verses active power and voltage verses reactive power characteristics. Slope of the characteristic will be defined based on the grid regulation requirements and limitations, which is nothing but inverse of the frequency susceptibility factor and voltage susceptibility factor.

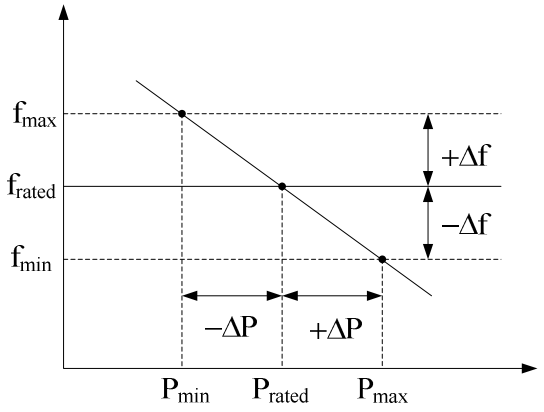

Figure 6.10 Frequency Vs active power characteristics

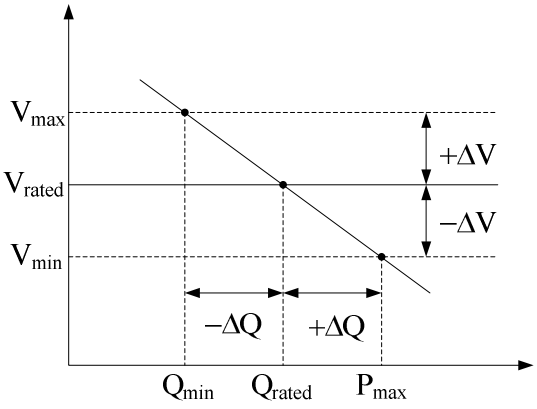

Figure 6.11 Voltage Vs reactive power characteristics

The single phase frequency droop control block diagram is shown in figure 6.12. The block diagram is very similar to the current control block diagram discussed in chapter 4. The difference between f_{ref} and $f_{(s)}$, which is Δf convert to the P_{ref} using the PI regulator. The gain of the PI regulator is defined by the frequency susceptibility factor $K_{pf.}$. The P_{ref} is reference power, which is compared with the $P_{(s),}$ actual power measurement. The differential input is convert to $i_{(s)ref}$ using gain/attenuation block. The sample and hold circuit, PI regulator, PWM modulator and LCL filter transfer function are same as current control regulator. Figure 6.13 shows the single phase equivalent voltage droop control loop.

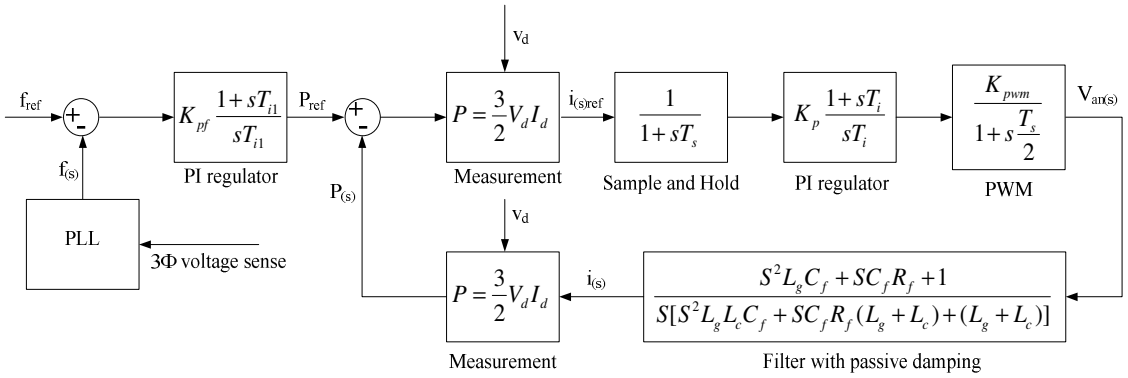

Figure 6.12 Single phase equivalent block diagram of frequency droop control

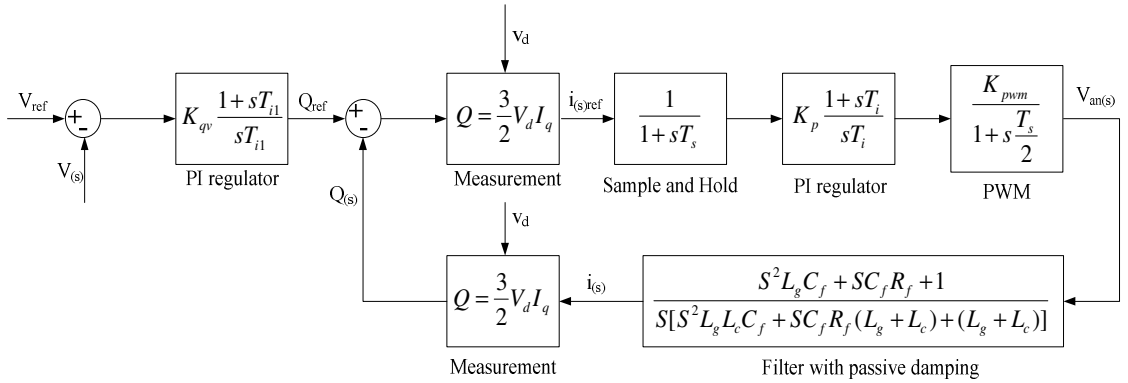

Figure 6.13 Single phase equivalent block diagram of the voltage droop control

Based on above equations the frequency droop control and voltage droop control is implemented as shown in figure 6.14. Error in frequency will be amplified by the K_{pf} and using PI regulator provides additional reference power required to meet the grid reference frequency. Similarly the error in voltage will provide in term of the reactive power required to meet the grid voltage conditions. Simulation of the frequency and voltage droop control required variable frequency – voltage source. Simulation results of the frequency and voltage droop support control are provided in following section.

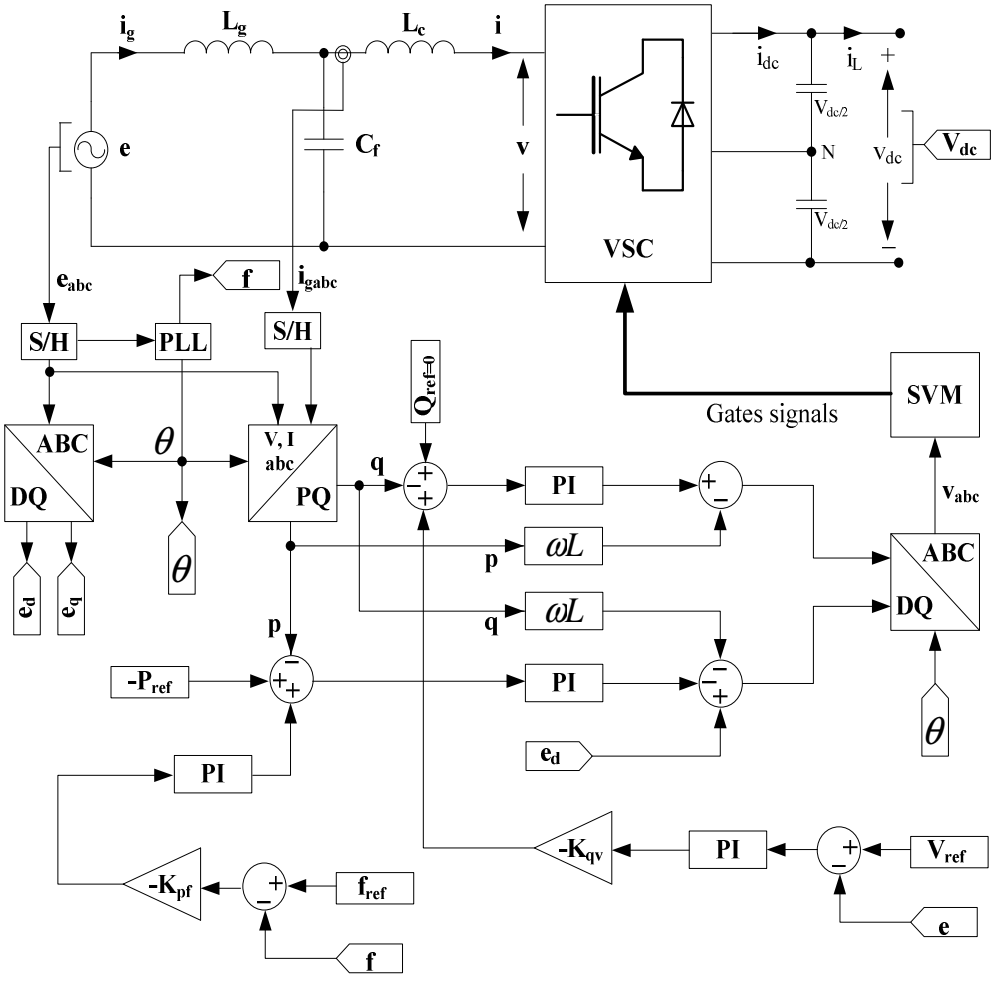

Figure 6.14 Control diagram of VSI with Frequency and Voltage droop support

6.4. Simulation result

The VSI with LCL filter and its control techniques are implemented using Matlab Simulink. The rated power of the inverter is 600kW and the results are displayed in per unit. Simulating the frequency droop control requires variable frequency source, which is dependent on demand and supply of the active power. Similarly, for voltage droop control requires variable voltage source, which is dependent on demand and supply of the reactive power. The variable frequency and voltage source was developed in Matlab Simulink to simulate the system. The block diagram of the simulated system is shown in figure 6.15.

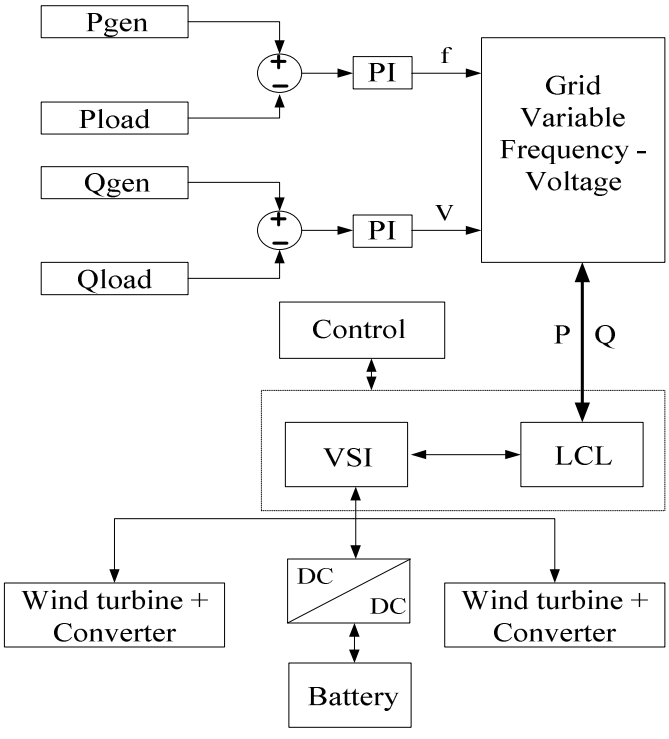

Figure 6.15 Block diagram of the simulated system in Matlab Simulink

Difference between Pgen and Pload translates in to equivalent frequency variation and difference between Qgen and Qload results in to voltage amplitude variation. The variable frequency and voltage source connected to VSI using LCL. VSI is fed by the DC/DC converter which is supply by the battery backup system. DC/DC converter keeps the DC bus voltage constant. For simulation purpose, the wind turbine and converter system are ignored. VSI control includes frequency and voltage droop control. If the frequency or voltage of the variable source varies based on the active- reactive power demand and supply variation, the control will inject or extract active and/or reactive power from source to keep the frequency and voltage to reference value. For simulation purpose it is assumed that the DC source is infinite but in actual application it will be limited and supports the frequency and voltage droop for short duration until the automation generation control will respond.

The simulation results for frequency droop control are shown in figure 6.16. The waveforms from top are phase voltage, line current, reference frequency, actual frequency with / without control, and converter side line to line voltage. One can observe that when the active power demand P_L increase, the frequency droop control generate active power from DC storage system and inject to the source to meet the demand, which allow frequency closely match with the reference frequency. In second last waveform of the frequency control simulation result shows that with frequency droop control the actual frequency (59.9Hz) is very closely follow the reference frequency (60Hz). In absence of the frequency droop control, as demand increase and no additional active power available, the frequency drops down (59.5Hz). Voltage droop control simulation

results are shown in figure 6.17. The first and second waveforms are the phase voltages with and without voltage support control. The voltage sag with voltage support control is less than 10% whereas without is about 50%. The third waveform shows the line current of the VSI. It can be easily observed that when the reactive power demand increases, the reference for the reactive power control goes high and generate more reactive power to keep the phase voltage constant. In absence of the control the phase voltage sag is higher.

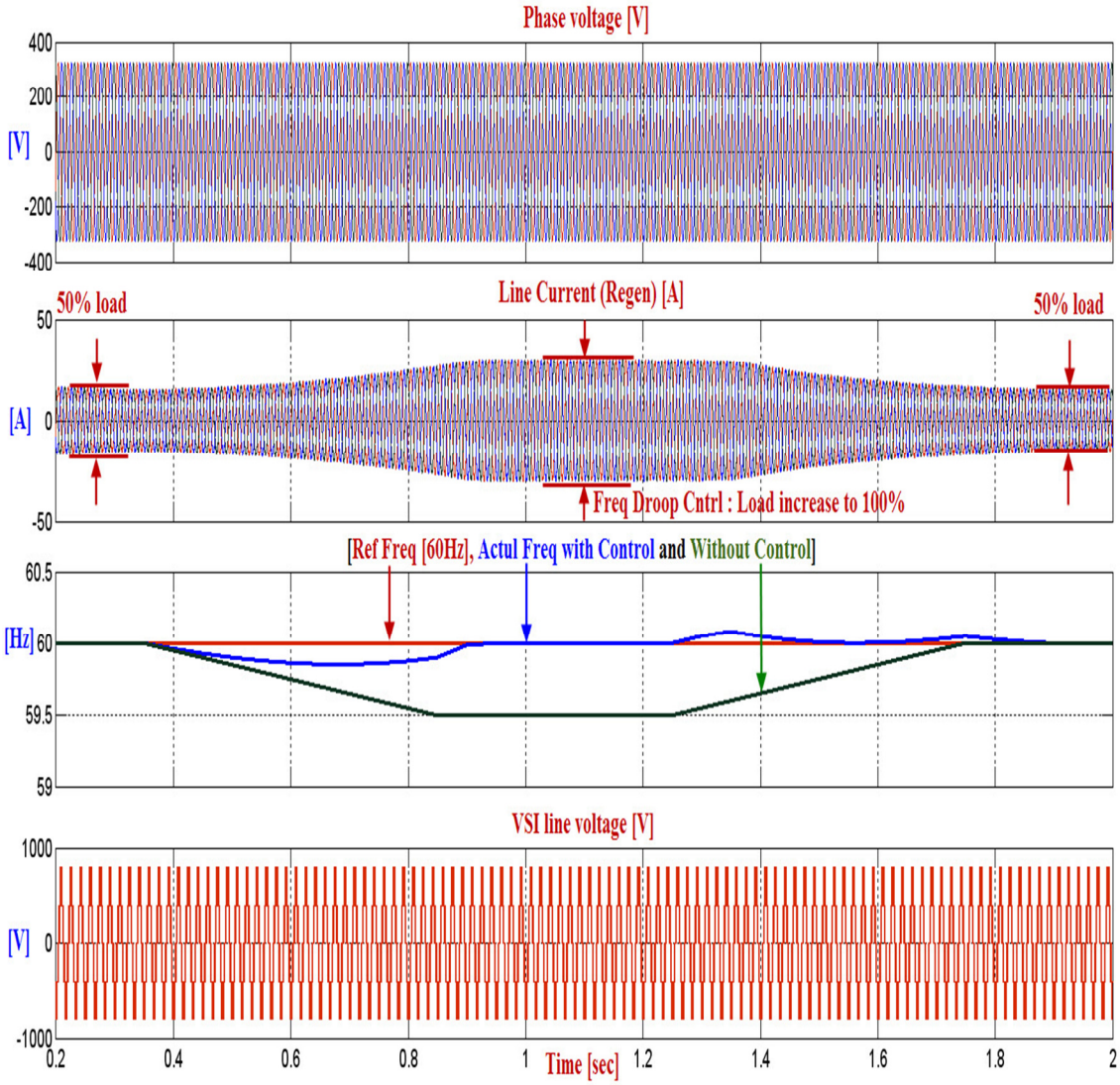

Figure 6.16 Simulation results for frequency droop control

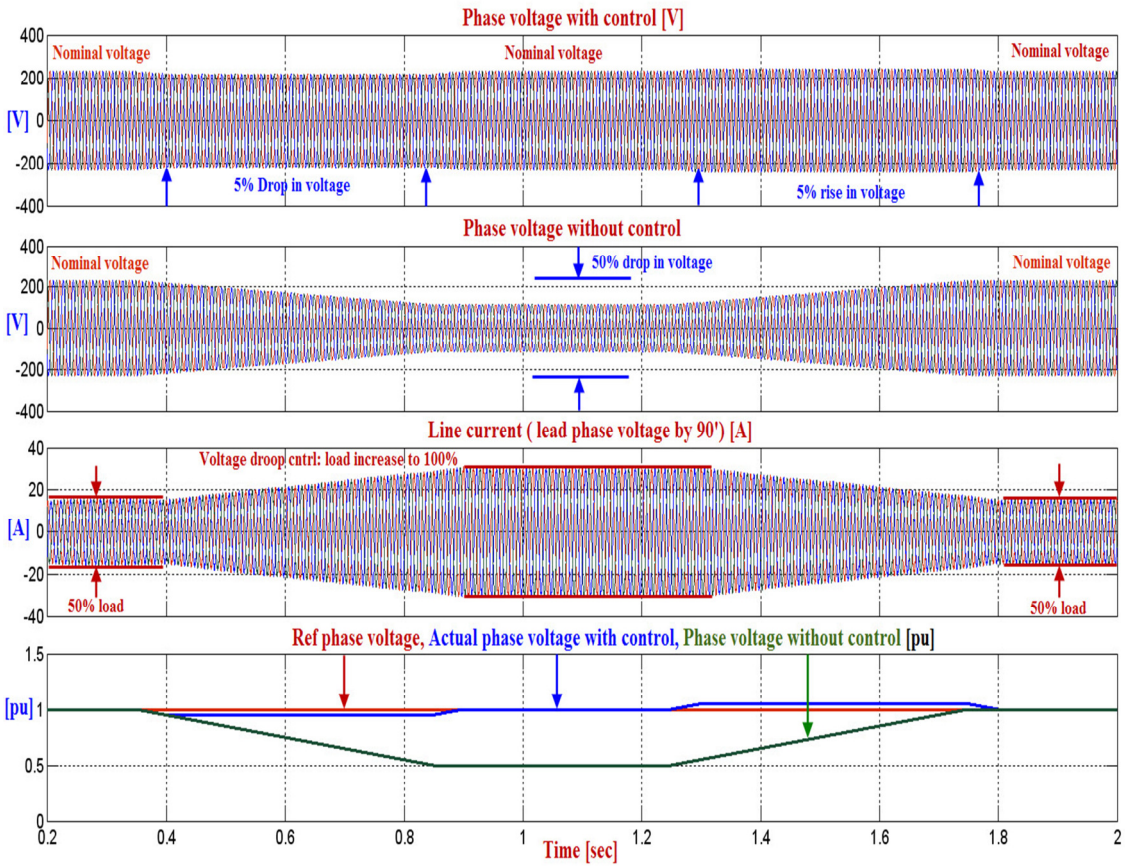

Figure 6.17 Simulation results for voltage droop control

6.5. Experimental result

The experimental setup for frequency and voltage droop control is shown in figure 6.18. The experimental setup is same as in chapter 4. The frequency and voltage droop control is implemented in the GPDSP. The AFE regulated DC bus supply is nothing but combine system of the energy storage system with DC/DC converter and the wind generator. For the frequency droop support the frequency feedback should be provided by the upper level SCADA system of the grid. This is recommended because it provides same feedback to all over the grid. This result in all the wind farms provides appropriate active

power injection to grid. The cumulative effect by all wind farms help to support the frequency droop. If the individual VSI measure its grid frequency, the measurement error results in inappropriate injection of active power which may not effective to support the frequency. For the voltage droop support line voltage should be measured by individual VSI because voltage may varies at different level of the transmission system. The experiment ran in motor mode and regenerative mode. Generally in motor mode it takes active power from grid and feed to the energy storage devices. In regenerative mode it takes active power from the energy storage unit and feed back to the grid.

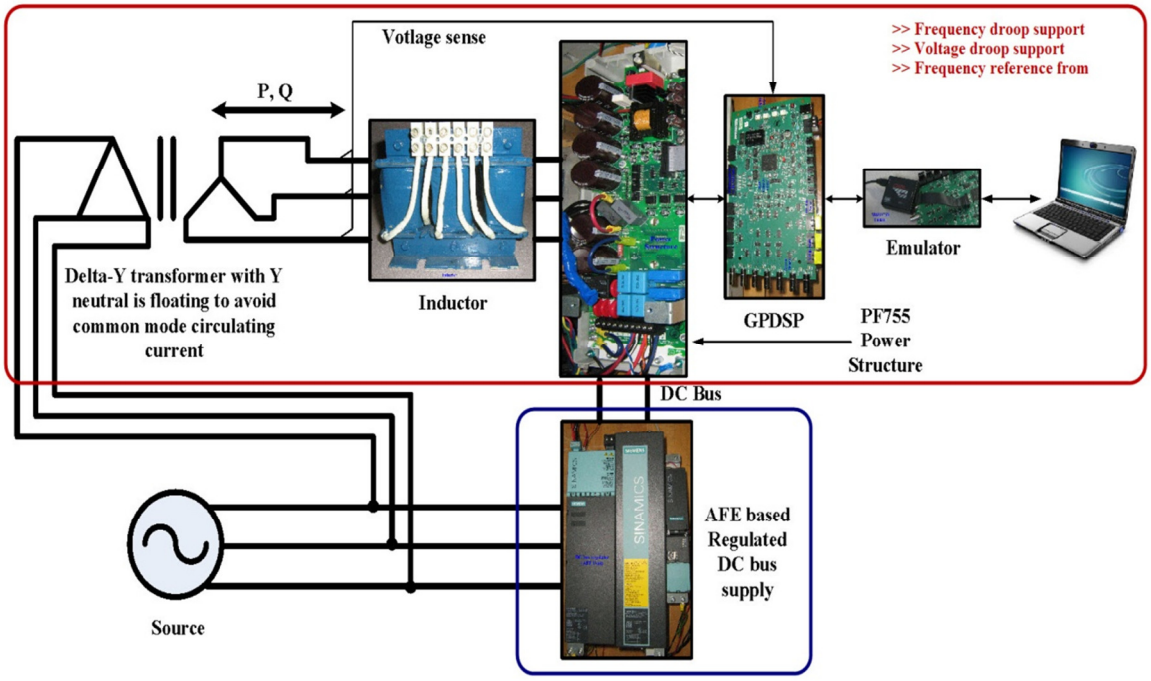

Figure 6.18 Experimental setup for frequency and voltage droop control

The no load operation of the PF755 unit is shown in figure 6.19. The channel 1 is the line voltage measurement of phase L1 (Yellow). Channel 3 is the converter side current (blue) measurement of phase L1 and Channel 4 shows the DC bus voltage measurement

(green). At no load the converter side current is dominated by switching frequency component. The DC bus voltage is set by the regulated AFE bus supply which is in this case is 761Vdc. The source voltage is 400Vac.

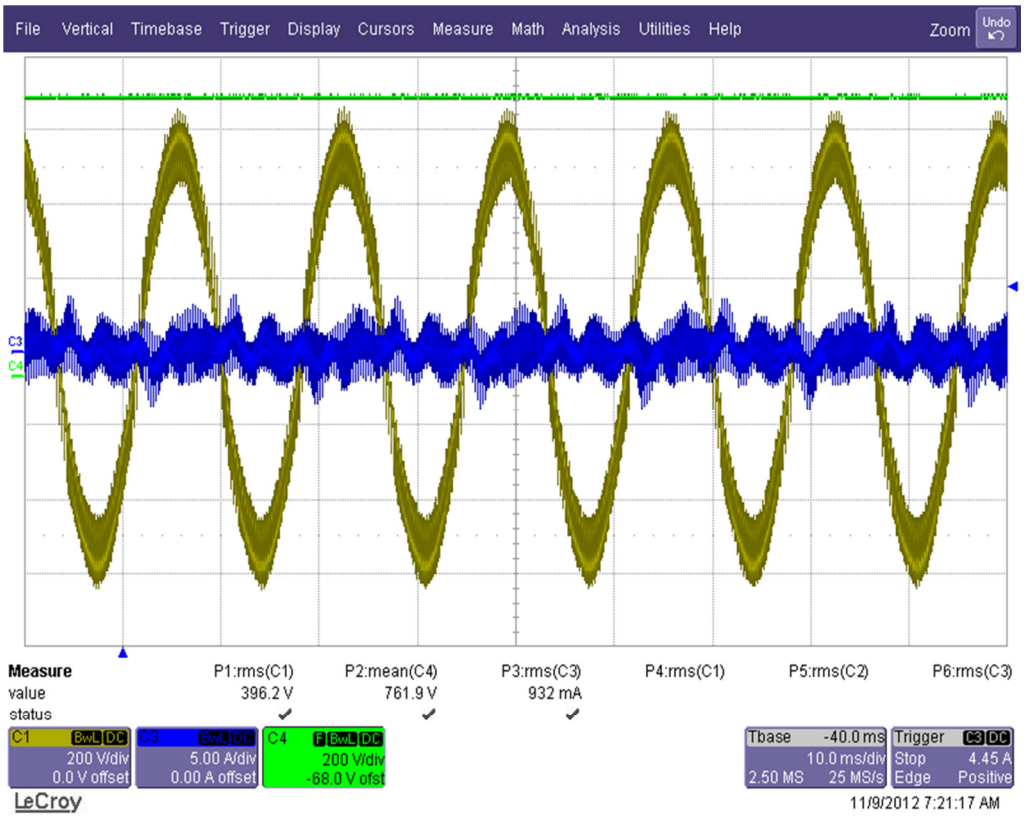

Figure 6.19 Experimental result of VSI in Regen mode at no load

Figure 6.20 shows the experimental result in regenerative mode at 25%, 50%, 75% and 100% loading. For the regenerative mode the line current is 30 degree lagging the line voltage. The DC bus voltage remains stable with different loading conditions. The reactive power reference set to zero so the power factor remains unity for all the loading conditions. The 100% loading related to 10kW which is the rating of the PF755 unit. The current waveform becomes more sinusoidal as load increases.

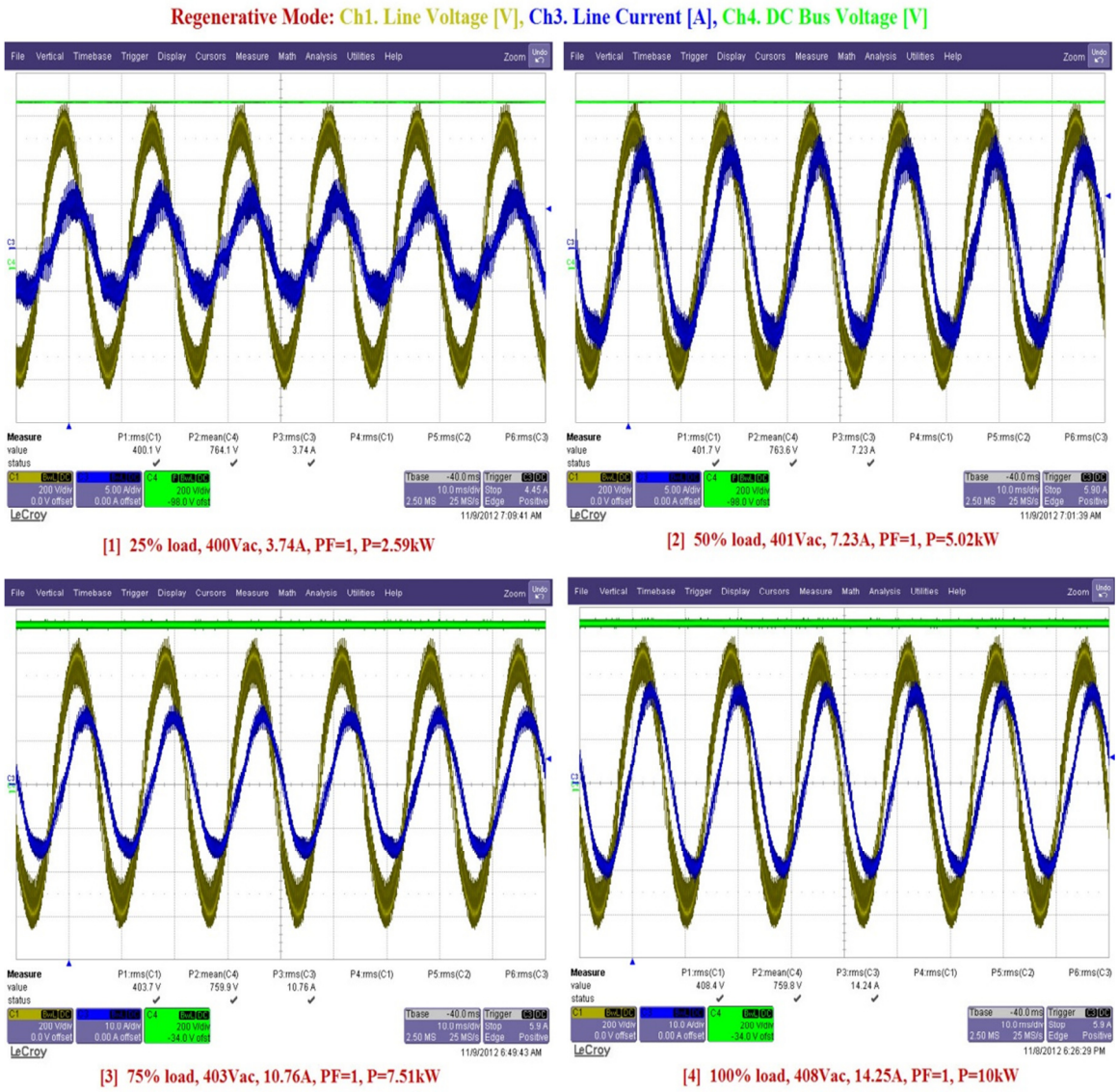

Figure 6.20 Experimental result of VSI in Regen mode at 25% to 100% load

Figure 6.21 shows the three phase current waveforms at different load conditions in regenerative mode. At 25% loading relates to 3.73A, 50% loading relates to 7.22A, 75% loading relates to 10.7A and 100% loading relates to 14.21A. The current waveforms are symmetric with minimum DC off set. Just inductor is used to interface with grid instead of LCL filter; the line current has the switching frequency harmonics in it.

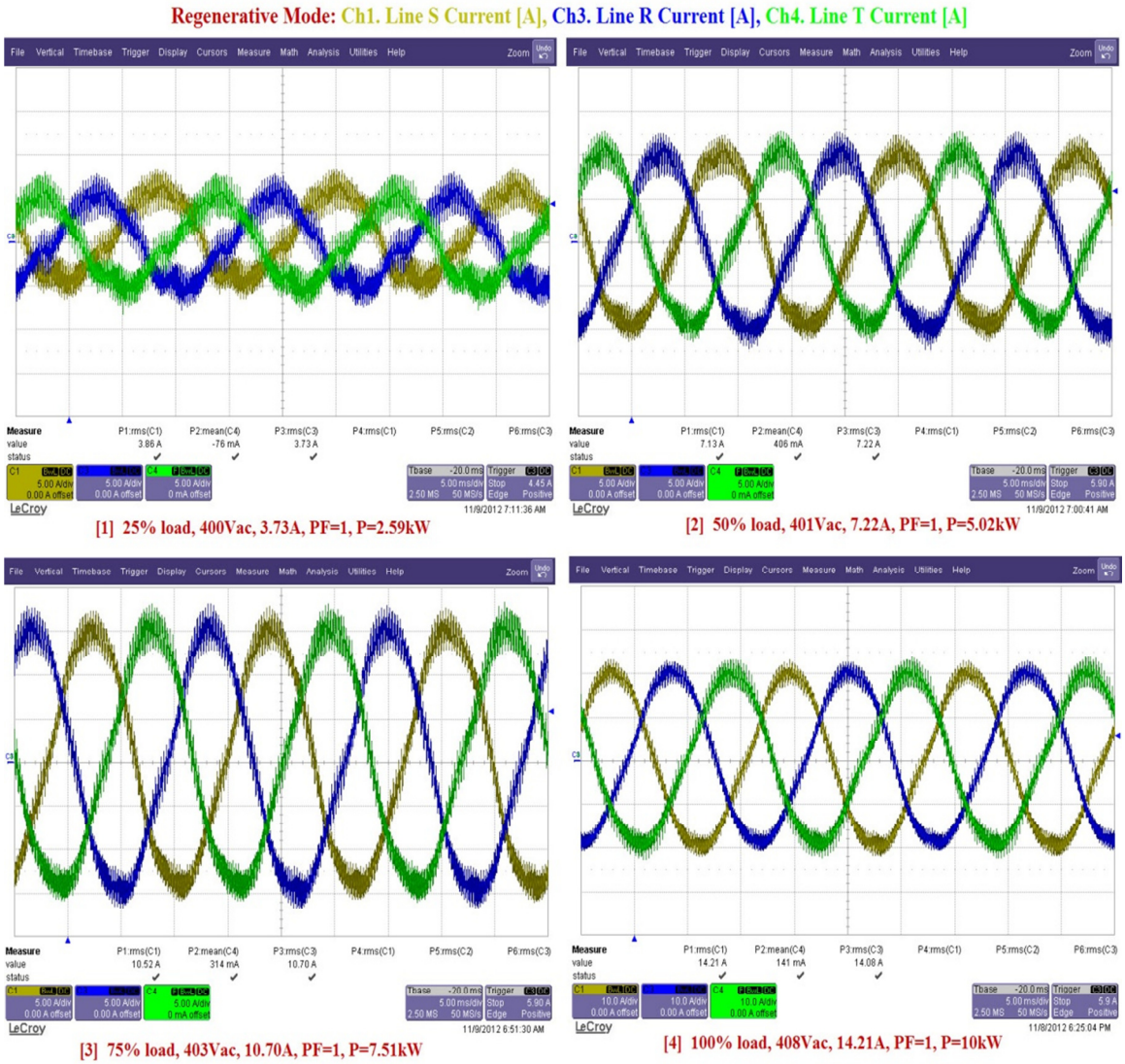

Figure 6.21 3Ph current in Regen mode at 25% to 100% load

Figure 6.22 show the experimental result in motor mode at 25%, 50%, 75% and 100% loading. For the motor mode the line current is 210 degree lagging the line voltage. The DC bus voltage remains stable with different loading conditions. The reactive power reference set to zero. The experimental results show that VSI can run in to regenerative mode or motor mode with just reference signal sign change. The unit can be loaded from no load to full load, which allow supporting the frequency control.

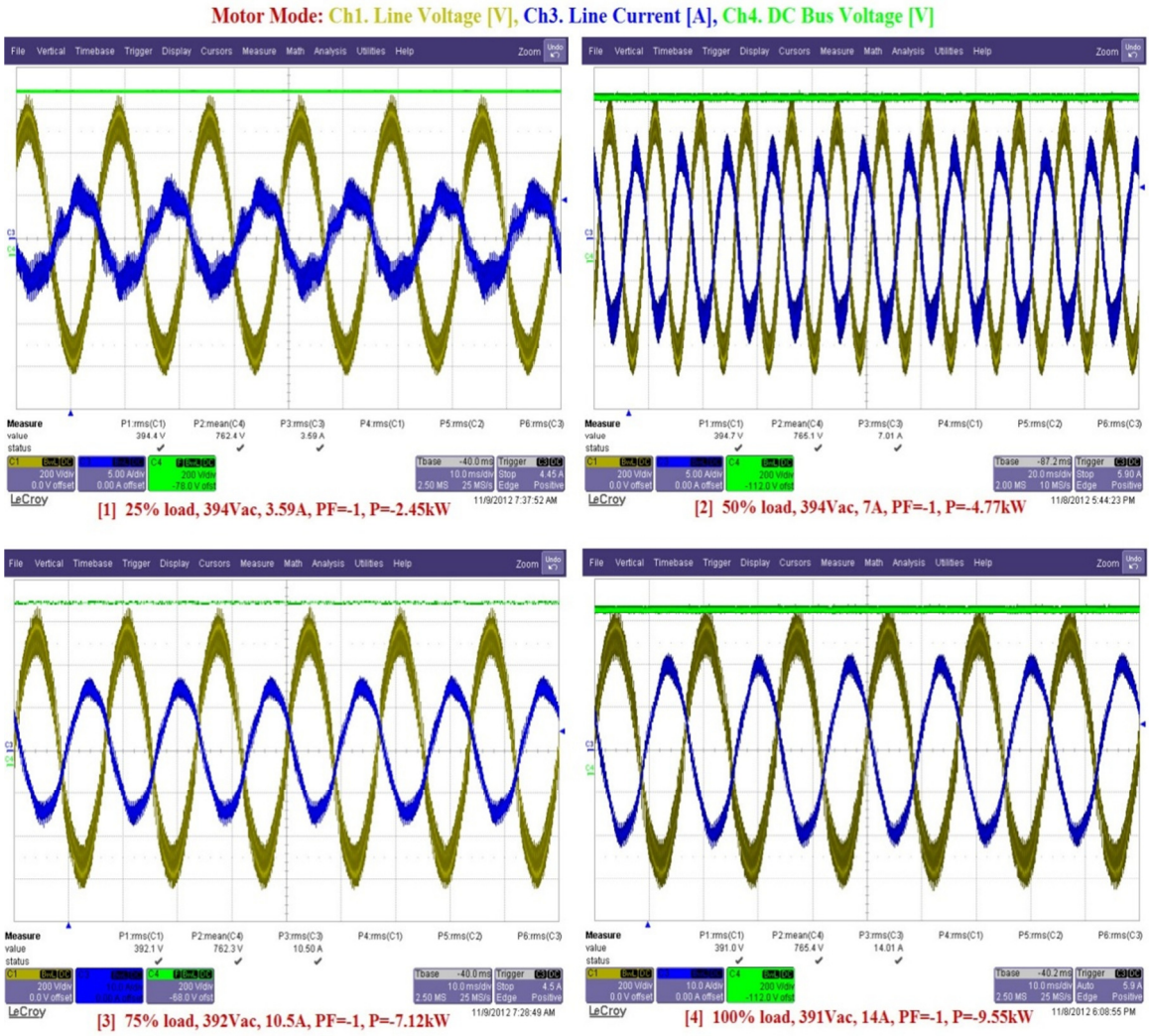

Figure 6.22 Experimental result of VSI in Motor mode at 25% to 100% load

Figure 6.23 shows the experimental result of the capacitive reactive power loading of the PF755 Fr2 unit. The active power reference set to 75% in the regenerative mode. The reactive power reference changes from 0% to 75% in 25% increment. The power factor changes from unity to 0.96, 0.866 and 0.689 respectively. The active power, reactive power and total KVA measurement is also shown in figure 6.23. Most of the time grid requires the capacitive reactive power to support the voltage droop. Just by changing the reference in the control loop the voltage droop support can be achieved without any issue.

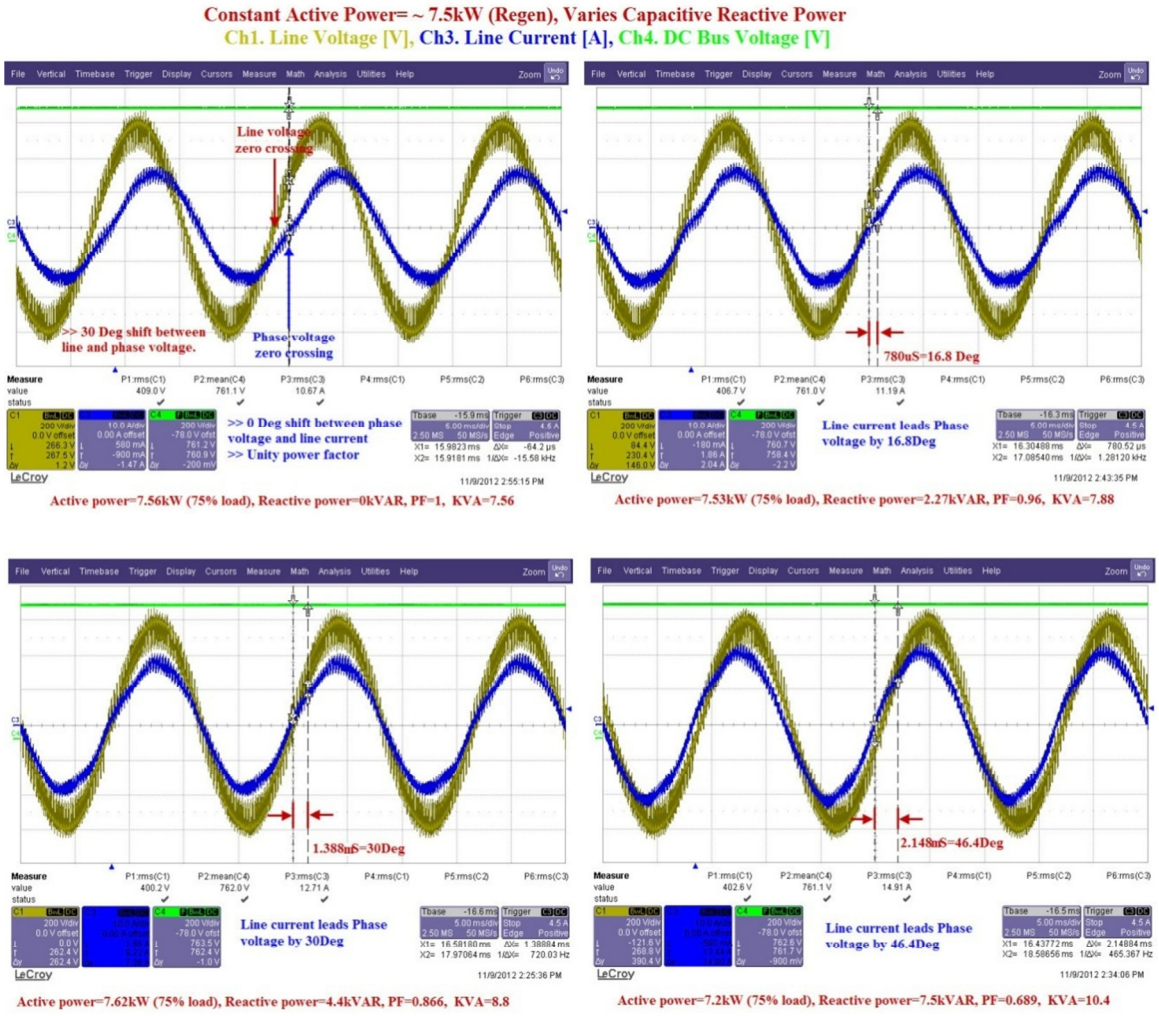

Figure 6.23 Active power = 75% and variable reactive power (capacitive)

Figure 6.24 shows the experimental result of the inductive reactive power loading of the PF755 Fr2 unit. The active power reference set to 75% in regenerative mode except in 4th waveform where the active power set to zero. The reactive power reference changes from 0% to 75% in 25% increment. The power factor changes from unity to 0.92(inductive), 0.8 (inductive) and 0(inductive) respectively. The active power, reactive power and total KVA measurement is also shown in figure 6.24. Rarely the grid requires the inductive reactive power to support the voltage droop but the control allows accomplishing it.

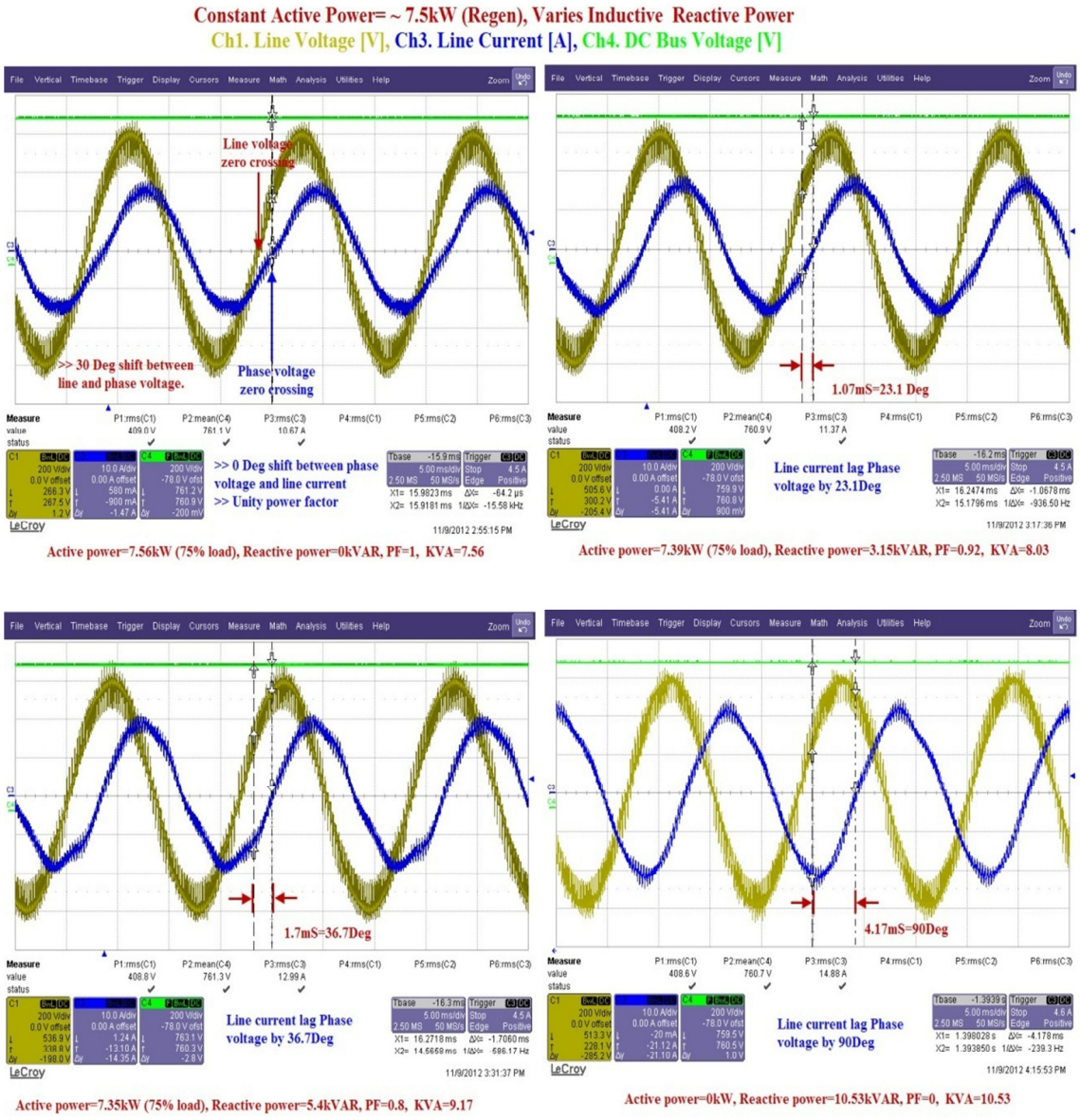

Figure 6.24 Active power set to 75% and variable reactive power (inductive)

Figure 6.25 shows the experimental result of the injection of active power to the grid. The channel 1 (Yellow) is the line voltage, channel 3 (Blue) is converter side current and channel 4 (Green) is the DC bus voltage. There is ramp in the active power injection from 0 to 50% loading. Once it reaches 50% load, there is step change in active power

reference to 100%. The unit successfully responds to step change within 250mS. The zooms in waveforms provide detail about start up, step change, steady state conditions.

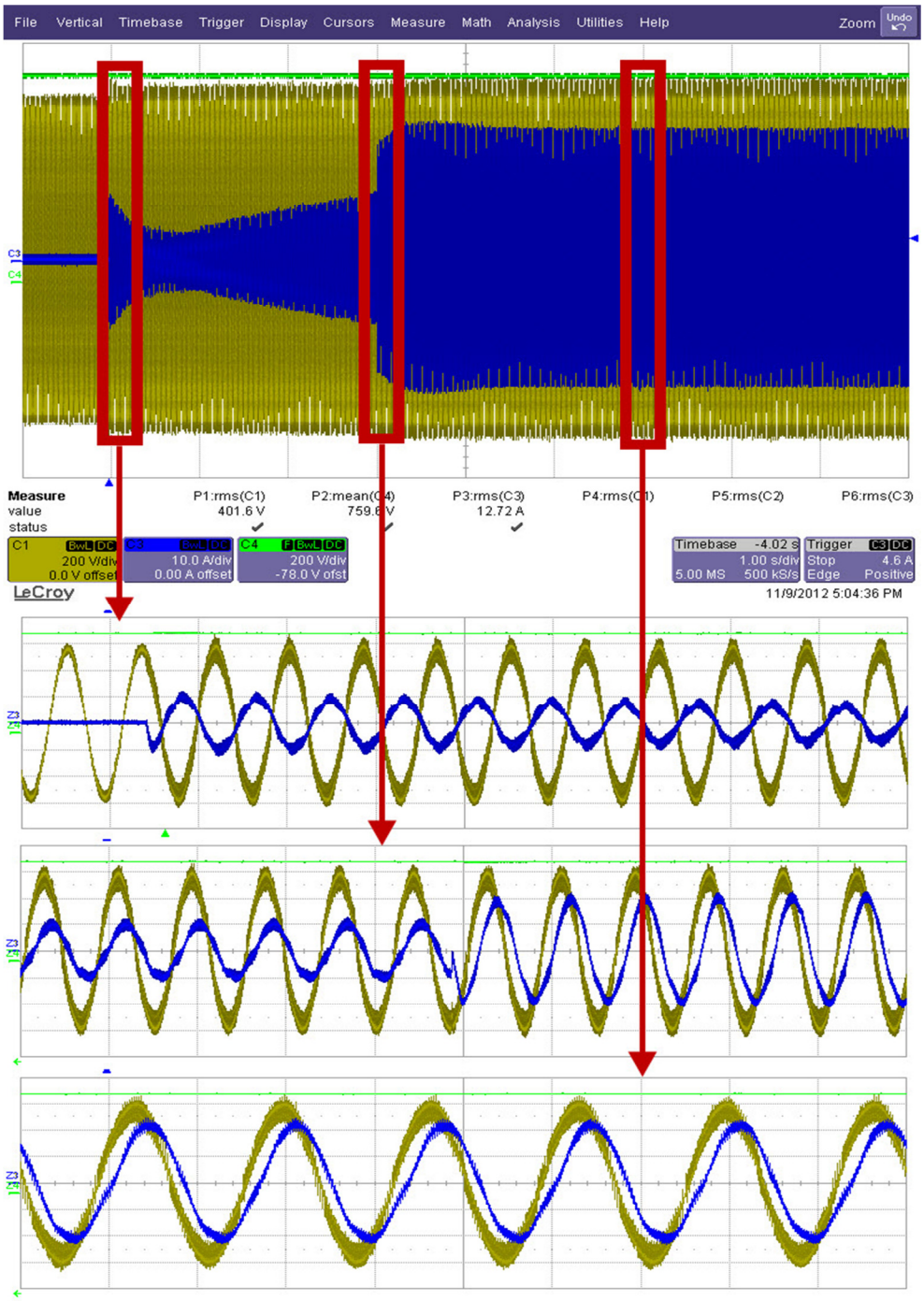

Figure 6.25 Ramp and step change of active power reference

The active power and reactive power reference can be changed simultaneously to provide both frequency and voltage droop support. To demonstrate the capability of the control, the unit ran with constant active power 75% load in regenerative mode and capacitive reactive power reference changes from 0% to 75% and go back to 0%. The experimental result is shown in figure 6.26. During the ramp up of the capacitive reactive power the line current gradually start leading the line voltages. Zoom in version of startup sequence is captured in waveforms 1-6 as shown in figure 6.26. The results show that the control is robust enough to support the active and reactive power injection to the grid.

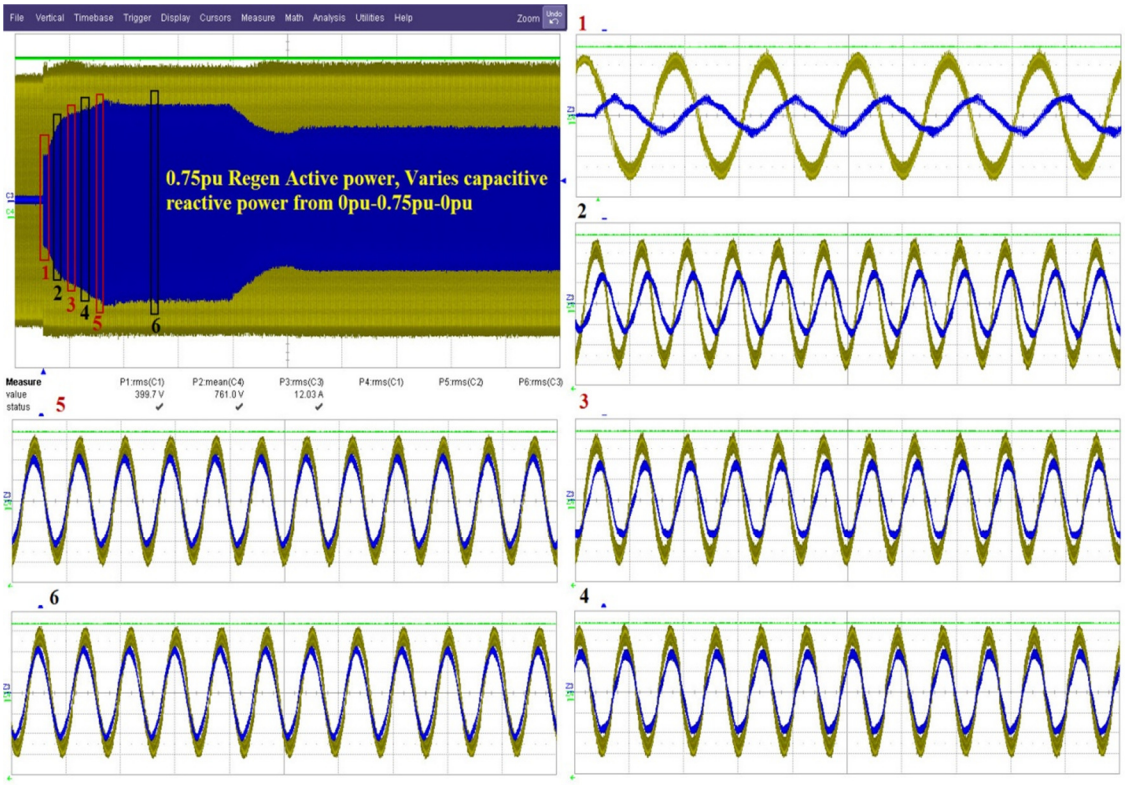

Figure 6.26 Active power 75%, reactive power ramp changes

The unit used for experimental setup is just 10kW rated and grid is stiff enough that there won't be any effect on frequency or voltage by injecting active and or reactive power to

the grid. In order to see how the active power reference signal is generated based on variation in grid frequency, we created the frequency change profile as shown in figure 6.27 where the reference frequency is 60Hz and actual grid frequency drop down to the 59.5Hz. Using Matlab Simulink model, the equivalent active power requirement reference signal is calculated. This active power reference signal is feed to the control. As shown in figure 6.27 the active power generation ramp up from 50% (5kW) to 100% (10kW) in response to 0.5Hz drop in grid frequency. When the grid frequency goes back to normal the active power generation goes back to original value of 50% (5kW). The zoom in waveform of the ramp profile shows that phase voltage and line current are in phase means unit is in regenerative mode.

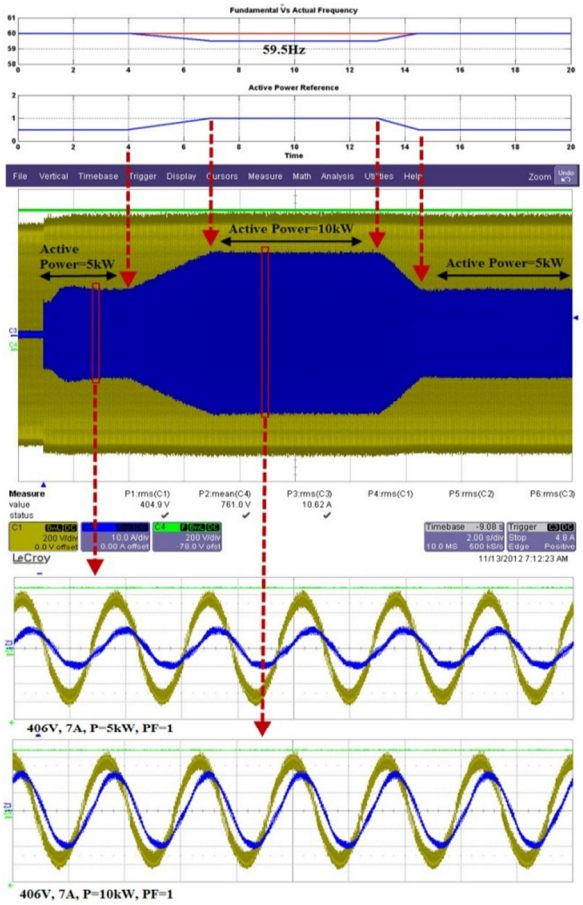

Figure 6.27 Frequency droop support with 100% max load profile

The above experimental results show that the VSI can quickly deliver active power to support the frequency. The VSI can run in overload mode for short duration to support big drop in frequency. This is illustrated by the experimental result. As shown in figure 6.28 the frequency drop from 60Hz to 59.25Hz. The equivalent active power reference signal is generated using Matlab Simulink. At nominal frequency (60Hz) , the VSI is injecting the 50% (5kW) of active power to the grid. When the frequency drop to 59.25Hz, the active power reference command generated is 1.5pu. The VSI unit is injecting 150% (~15kW) active power to the grid to keep the frequency stable. The VSI response is strictly following the active power reference common. The zoom in waveform during 150% loading and 50% loading is shown in figure 6.29. The experimental results validate that VSI can run in overload mode to support frequency.

Sometime the VSI is just turn on and the grid may face frequency droop condition. In order to validate this worst case scenario, the frequency profile 2 is created. The active power reference signal is generated by Matlab Simulink. As shown in figure 6.29, when the VSI about to turn on, the grid frequency drop to 59.25Hz. The VSI start injecting the active power 150% (15kW) to the grid. Suddenly the frequency starts recovering and come back to normal (60Hz) and VSI is generating nominal active power 50% (5kW). After some duration the frequency start dropping again, in response, the VSI start ramp up the generation of the active power up to 150% of the rating of unit. It can be observed in figure 6.29 that active power generation follow the active power reference signal and providing frequency support to the grid. The zoom in waveforms conforms that unit is running in regenerative mode.

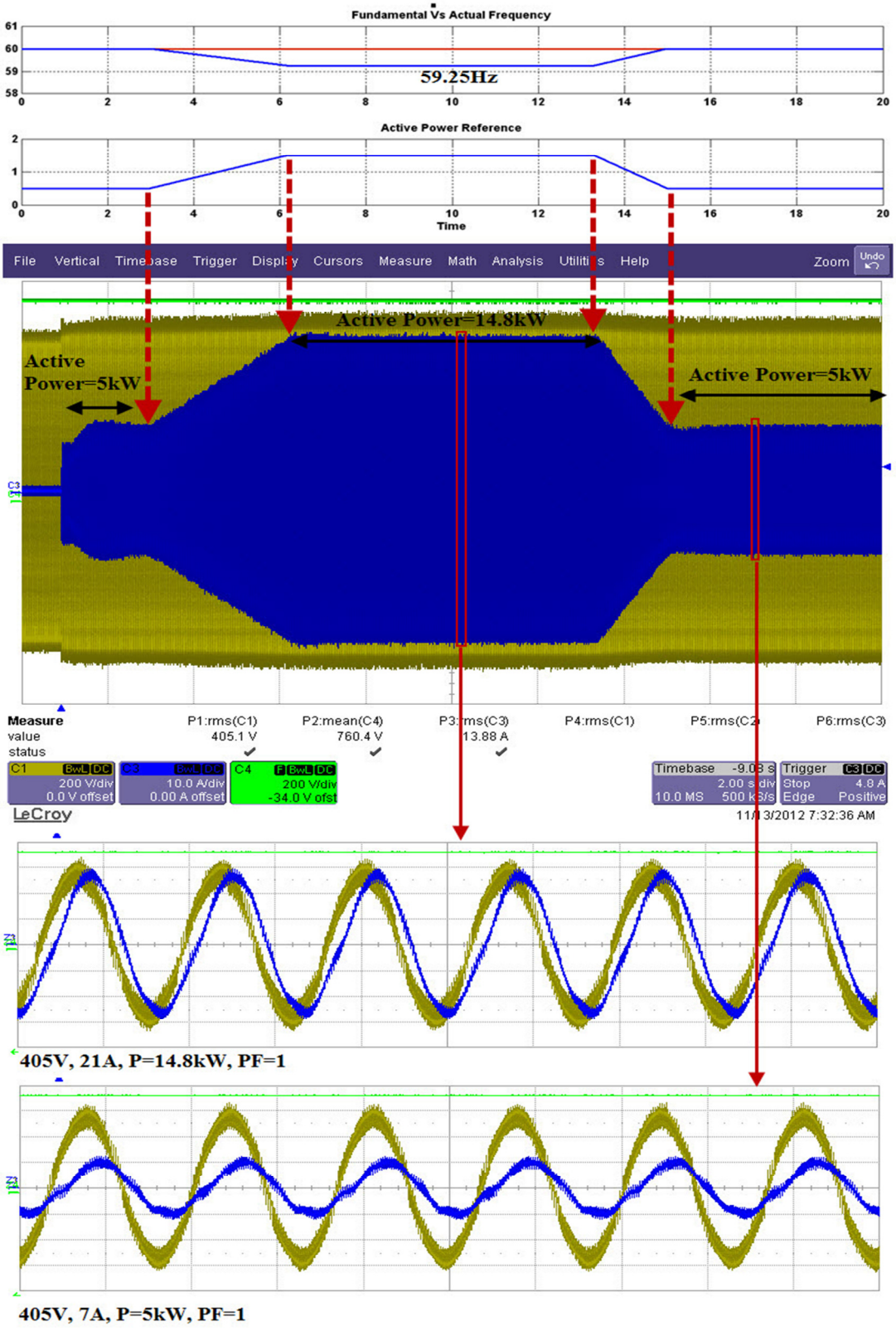

Figure 6.28 Frequency droop support with 150% load profile 1

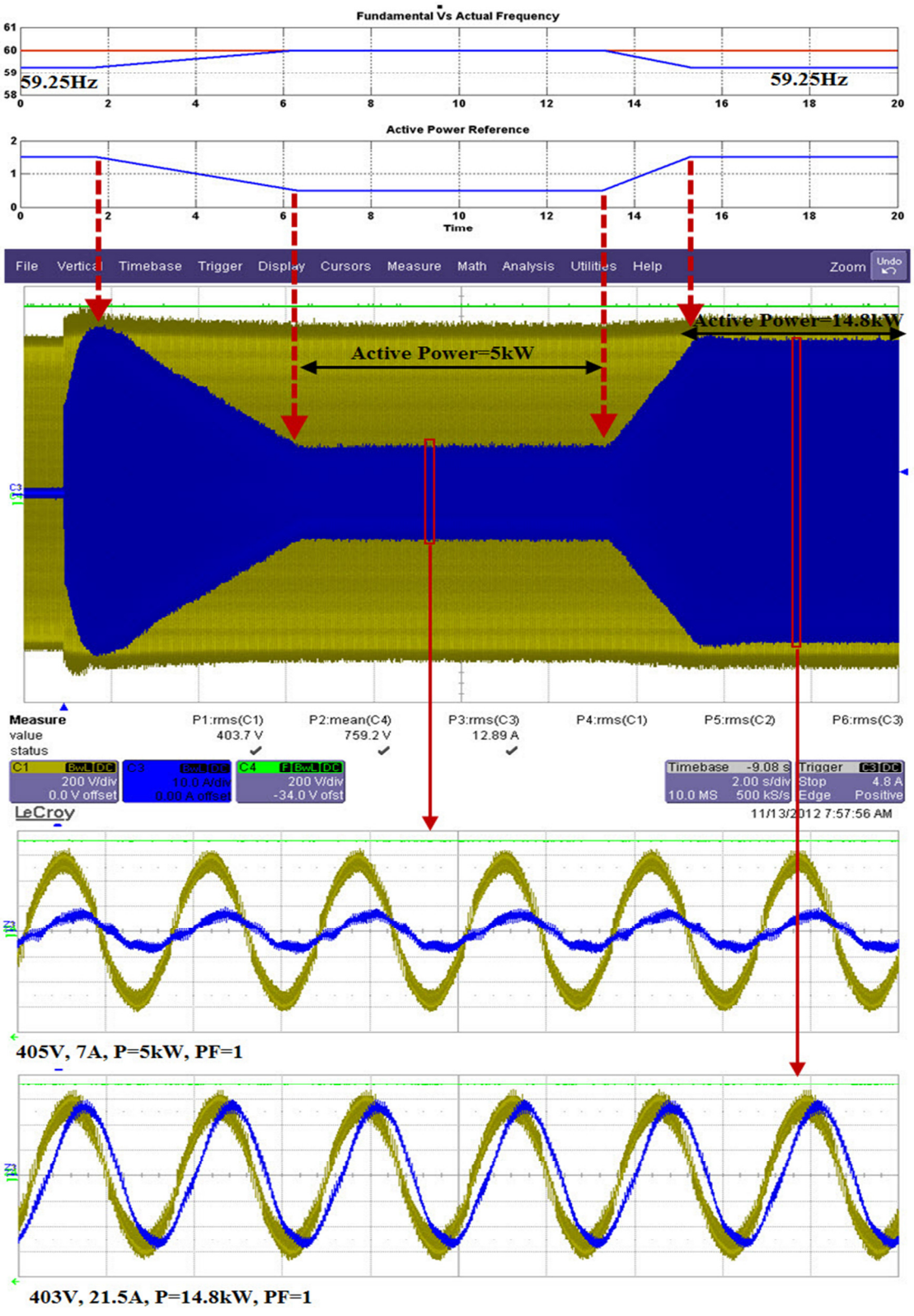

Figure 6.29 Frequency droop support with 150% load profile 2

The voltage droop support can be validated the same way as the frequency droop support. The voltage droop profile is created and reactive power reference signal is generated using the Matlab Simulink. The voltage droop profile 1 is shown in figure 6.30, where the voltage is drop to 60% of the nominal value. The reactive power reference signal is generated and feed to the VSI control. In this case the it required 150% reactive power (capacitive) to keep the voltage within limit. The expreimental result shows that the VSI control generates the around 120% (12kVAR) reactive power and as the voltage come back to nominal vaule it reduces the generation of reactive power gradually up to 50% (4.7kVAR). The zoom in waveforms shows that the line current is leading the phase voltage by 90', which proves that it is running in capacitive reactive power generation mode.

Sometime the VSI is just turn on and the grid may face voltage droop condition. In order to validate this worst case scenario, the voltage profile is created. The reactive power reference signal is generated by Matlab Simulink. As shown in figure 6.31, when the VSI about to turn on, the grid voltage drop to 60% of nominal voltage. The VSI start injecting the reactive power ~150% (12kVAR) to the grid. Suddenly the voltage starts recovering and come back to nominal value and VSI is generating nominal reactive power ~50% (3.8kVAR). After some duration the frequency start dropping again, in response, the VSI start ramp up the generation of the reactive power up to 150% rating of the unit. It can be observed in figure 6.31 that reactive power generation follow the reactive power reference signal and providing voltage support to the grid. The zoom in waveforms conforms that unit is running in capacitive reactive power mode.

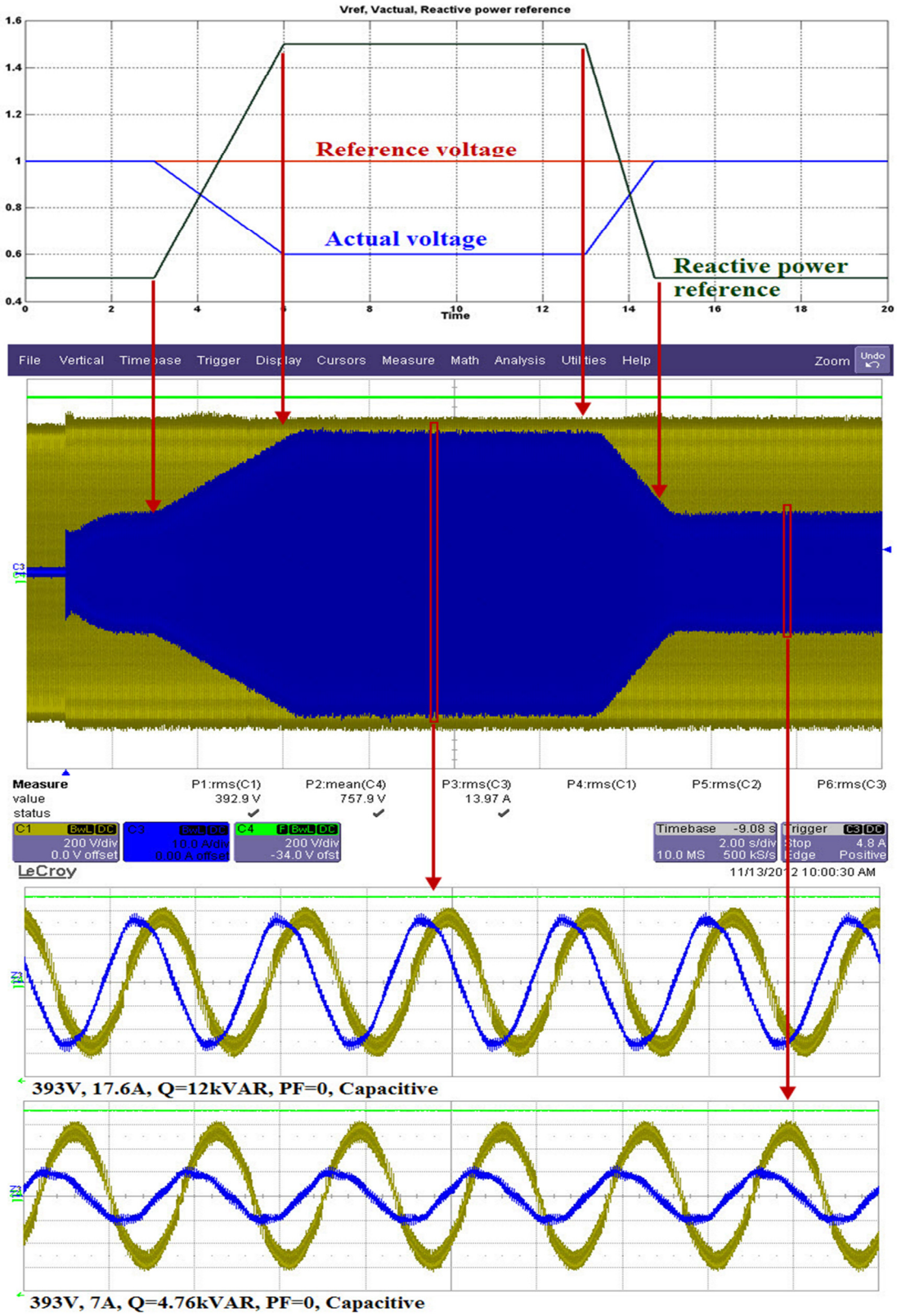

Figure 6.30 Voltage droop support with 150% load profile 1

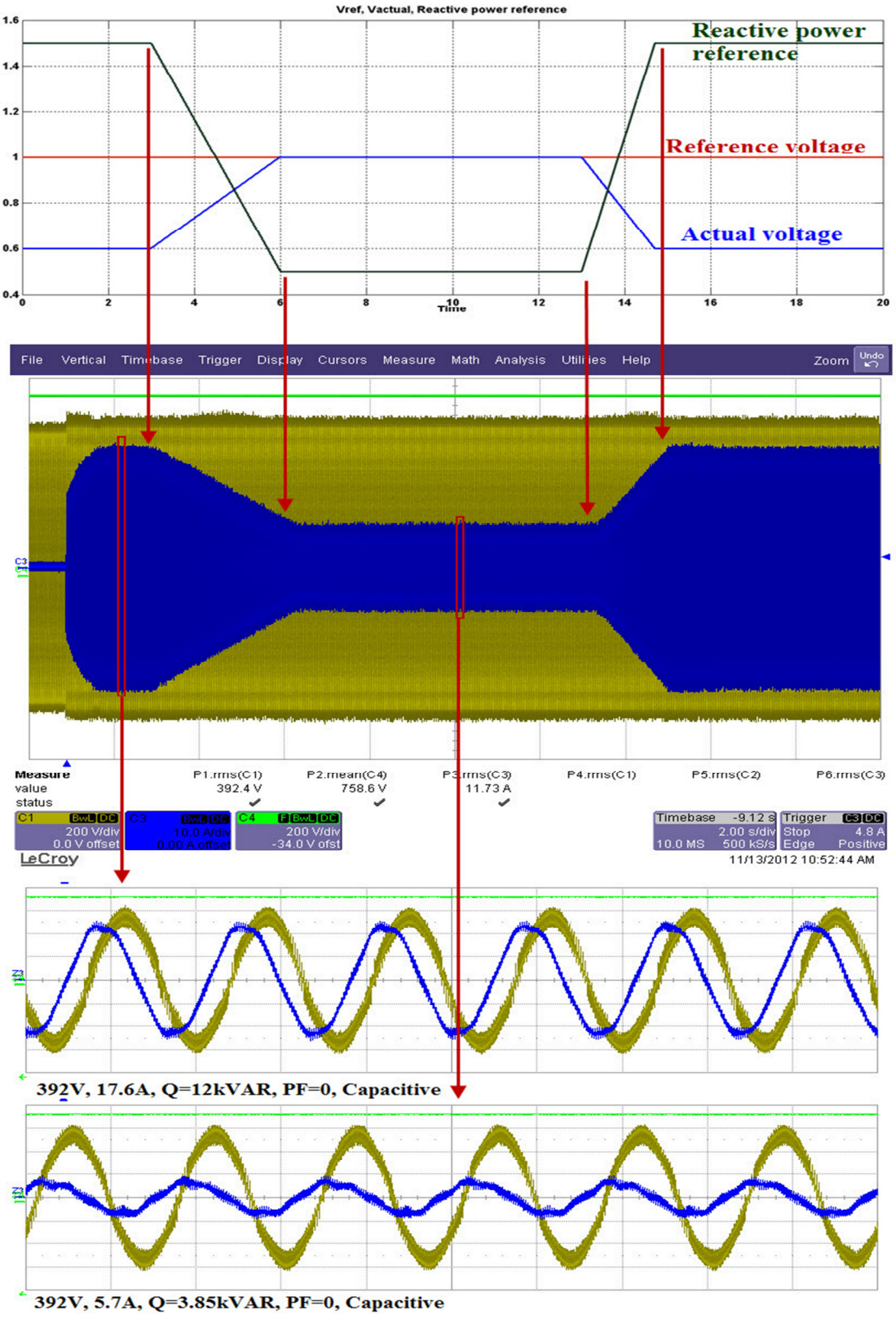

Figure 6.31 Frequency droop support with 150% load profile 2

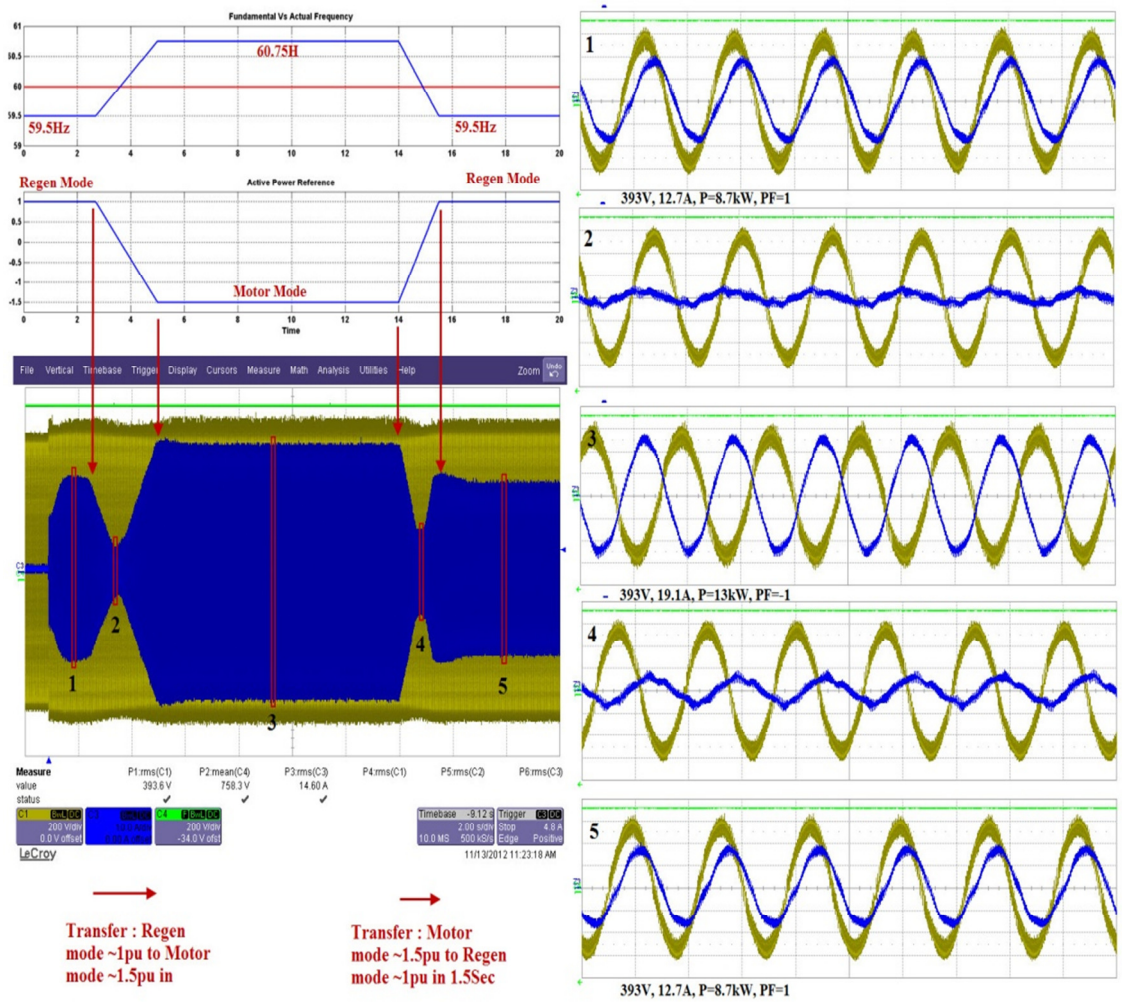

Figure 6.32 Frequency droop support with Regen and Motor mode operation

Sometime the frequency swing between low to high and come back to low frequency. This scenario is validate by the frequency profile as shown in figure 6.32, where at start of the VSI unit the frequency is 0.5Hz below the nominal frequency. Suddenly the system frequency goes above the nominal frequency (60.75Hz) and then come back to low frequency again. The active power reference signal is swing between positive and negative value. The positive value refers to active power injection in to the grid (Regenerative mode) to boost the frequency. Generally this power is delivering from energy storage unit. The negative value refers to active power take from the grid and

sends to energy storage unit (Motor mode) to reduce the frequency of grid. The experimental result shows that initially unit injecting active power at 100% rating then it goes in to motor mode with 150% rating and come back to the Regen mode again. During this operation the DC bus remains constant. The waveform 1 shows that unit is running in regenerative mode. Waveform 2 shows the transition between regenerative modes to motor mode. Waveform 3 shows the unit is in motor mode. Waveform 4 shows the unit is in transition from motor to regenerative mode again. The response of the VSI unit is very quick. It changes from 100% regenerative mode to 150% motor mode less than 1.7 Sec.
It shows that wind power with energy storage unit can provide fast response to support the frequency and voltage droop. The experimental result shows that the DC bus remains constant during the ramp and step changes. In addition it proves that MVDC system can effectively provide frequency and voltage support and provide primary response during frequency/voltage droop conditions.

6.6. Conclusion

In this chapter, a proposed MVDC system is discussed in detail. The main advantages of the proposed MVDC system are active and reactive power rate control, frequency droop control and the voltage droop control. The novel control for the frequency and voltage droop support is provided in this chapter. The control loop analysis is performed using single phase equivalent model in Matlab control design toolbox. The relationship between the grid frequency and grid inertia is established in terms of mathematical model. The simulation model for the system is generated in Matlab

Simulink. The system simulation result is closely matched with the analysis. The experimental result shows that active and reactive power can be adjusted based on frequency feedback as well as voltage feedback to support the frequency and voltage droop condition in grid and increase the reliability and quality of the gird.

7. Conclusion

In this thesis the novel medium voltage inverter based DC distribution system is discussed in detail. This includes the precharge circuit, the TRAP and LCL filter, the voltage source inverter and the frequency and voltage droop control. The novel AC and DC precharge topologies are presented in chapter 1. The proposed AC precharge topology provides precharge to both DC link capacitor as well as LCL filter. Both AC and DC precharge have size and cost advantages. It reduces the maintenance and increases life of the switch gear. Automated AC and DC precharge topology enable standby mode of operation when wind is not available. The TRAP and LCL filters mathematical models are discussed in detail in chapter 2. The optimum design algorithms for the TRAP and LCL filters are presented. The effects of the grid impedance / isolation transformer are discussed in detail and used this information to design the TRAP and LCL filters. The algorithms are implemented in MATLAB. The resonance issues with LCL filter are discussed in depth and different topologies for the passive resonance damping for the LCL filter are presented. Each passive damping topologies pros and cons are compared. The TRAP and LCL filters for 125kW converter were designed using this algorithm. The designed has been tested in simulation and with an experimental setup. Both simulation result and experimental result shows that it meets the IEEE 519 voltage THD and current TDD limits. The 2L and 3L VSI, its control techniques are discussed in chapter 4. Both 2L and 3L NPC VSI control is identical except their PI regulators gain parameters are different. The 3L NPC topology allows for medium voltage system. The main advantages of the medium voltage are reduction in

distribution cost and higher power density of VSI module. The constant DC bus voltage control and Active/Reactive power control are discussed in detail. The control loop analysis is performed using Matlab Simulink control design toolbox. The system simulation model is developed in Matlab Simulink to verify the control techniques. The experimental setup is discussed in detail including implementation of embedded coding for DSP TMS320F2812 fixed point processor. The experimental results match with the simulation results. Calculation of efficiency for power conversion devices is provided in chapter 5. The LCL filter, VSI and DC link capacitors power losses are calculated. Calculation of the VSI switching losses requires IGBT and Diode turn on and turn off losses. Double pulse test method to measure the IGBT and Diode turn on and turn off losses are discussed in detail and verify with experimental setup. The calculated efficiency is compared with the measured efficiency of power conversion device. Measured efficiency is very close the calculated efficiency. Power conversion unit standby mode of operation is provided using flow chart. The total energy saving by standby mode of operation for 300Hp unit is provided in experimental results. Finally, a proposed MVDC system is discussed in detail. The main advantages of the proposed MVDC system are active and reactive power rate control, frequency droop control and voltage droop control. The novel control for the frequency and voltage droop support is provided in chapter 6. The control loop analysis is performed using single phase equivalent model in Matlab control design toolbox. The relationship between the grid frequency and grid inertia is established in terms of mathematical model. The simulation model for the system is generated in Matlab Simulink. The system simulation result is closely matched with the analysis. The experimental result shows that active and reactive

power can be adjusted based on frequency feedback as well as voltage feedback to support the frequency and voltage droop condition in grid and increase the reliability, stability and quality of the gird.

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APPENDIX A: LCL filter design algorithm

```
%% LCL filter design based for 2kHz switching frequency.(4kHz requires step change and initial value changes)

% Trap circuit as below:
%        Line-------Lg=(Ls+L1)---------|----------Lc------Converter
%                                      |
%                                CR series (R is optional)
%                                      |
%                                   Ground
% Lg=source(iso-Xfmr impedance Ls+L1)uH, Lc=L2 uH, Value of C uH


%% Consider drive connected to any source (1. Iso-Xfmr Rating = Drive or 2) Iso-Xfmr Rating >>>>> Drive)
%% Assume Iso-Xfmr impedance is 6% of base impedance
%% case 1.Iso-Xfmr impedance = Lsmin=0
%% case 2.Iso-Xfmr impedance =0.06*Lbase=Lsmax
%% Keep resoance frequency of LgCLc in range such that  13*F < Lg-LC-Lc <0.5*Fsw,
%% where F= fundamental frequency and Fsw is switching frequency.
%% Find attnuation at switching frequency. Higher attenuation better filtering
%% Program gives list of differnt L1CL2 combination.
%% Cost will be driving factor to select one of LCL combination
%% Yogesh patel updated on Apr 17, 2009.


function []=LCLdesign(V,I,Fo,Fsw)

Wsw=2*pi*Fsw;

%base impedance and inductance of drive
Zbase=(V^2)/(sqrt(3)*V*I);
Lbase=Zbase/(2*pi*Fo);
Cbase=1/(2*pi*Fo*Zbase);

% min-max iso-Xfmrimpedance  (10*Unit rating to 1*unit rating)
Lsmin=0.1*0.06*Lbase;
Lsmax=0.06*Lbase;

% Consider reference L2=x*Lbase where (6<=x<=9)
% Consider reference C=m*Cbase where (5<=m<=7)

x=5;
```

```
for p=1:1:4
   x=x+1;
L2(p,1)=x*0.01*Lbase;
L1(p,1)=(1/3)*L2(p,1);  %consider L1/L2 ratio=3
   m=6;
for j=1:1:2
      m=m+1;
C(j,p)=m*0.01*Cbase;
      Frmax(j,p)=((L1(p,1)+L2(p,1))/(L1(p,1)*L2(p,1)*C(j,p)))^0.5*(1/(2*pi));

Frmin(j,p)=((L1(p,1)+Lsmax+L2(p,1))/((L1(p,1)+Lsmax)*L2(p,1)*C(j,p)))^0.5*(1/(2*pi
));
end
end

k=0;
for i1=1:1:4
for j1=1:1:2
if (Frmax(j1,i1)>6*Fo&&Frmax(j1,i1)<0.7*Fsw)
if (Frmin(j1,i1)>6*Fo&&Frmin(j1,i1)<0.7*Fsw)
         k=k+1;
L2p(i1,1)=L2(i1,1);
L1p(i1,1)=L1(i1,1);
Cp(j1,i1)=C(j1,i1);

Attmax(j1,i1)=20*log10(abs(1/((i*Wsw)^3*(L2p(i1,1)*L1p(i1,1)*Cp(j1,i1))+i*Wsw*(L
2p(i1,1)+L1p(i1,1)))));

Attmin(j1,i1)=20*log10(abs(1/((i*Wsw)^3*(L2p(i1,1)*(L1p(i1,1)+Lsmax)*Cp(j1,i1))+i*
Wsw*(L2p(i1,1)+(L1p(i1,1)+Lsmax)))));
         A(k,:)=[(L2p(i1,1)/Lbase)*100,  (L2p(i1,1)*10^6),  (L1p(i1,1)/Lbase)*100,
(L1p(i1,1)*10^6),  (Cp(j1,i1)/Cbase)*100,  (Cp(j1,i1)*10^6),  Frmax(j1,i1),  Frmin(j1,i1),
Attmax(j1,i1) Attmin(j1,i1)];
end
end
end
end

M=A(:,:);
disp('Available Options Based on 13*Fo<Fr< 0.5*Fsw')
disp('  %L2      L2uH      %L1      L1uH      %C      CuFFrmax Hz      FrMin Hz
Attenmax dB    Attenmin dB')

%write result in excel spread sheet name "LCLdesigndd-mmm-yyyy"

warning off MATLAB:xlswrite:AddSheet
```

```
filename=['LCLdesign ' date];
msg={'Available Options Based on 13*Fo<Fr< 0.5*Fsw'};
lable={'%L2','L2 uH','%L1','L1 uH','%C','CuF','Frmax Hz','FrMin Hz','Attenmax dB','Attenmin dB'};
xlswrite(filename,msg,'LCLdesign at 2kHz', 'A2');
xlswrite(filename,lable,'LCLdesign at 2kHz', 'A4');
xlswrite(filename,M,'LCLdesign at 2kHz', 'A5');
```

APPENDIX B: Trap filter design algorithm

```
%% Trap filter design based on standard 3% line side and 9% converter side reactor

% Trap circuit as below:
%       Line-------Lg=(Ls+L1)---------|----------Lc------Converter
%                                     |
%                                LfCfR series (R is optional)
%                                     |
%                                   Ground
% Lg=source(iso-Xfmr impedance Ls+L1=3%)uH, Lc=L2=9% uH, Value of Lf uH
% and Cf uF need to determied

%% Consider drive connected to any source (1. Iso-Xfmr Rating = Drive or 2) Iso-Xfmr
Rating >>>>> Drive)
%% Assume Iso-Xfmr impedance is 6% of base impedance
%% case 1.Iso-Xfmr impedance = 2*L1
%% case 2.Iso-Xfmr impedance is negligible compare to L1
%% Keep resoance frequency of Lg-LC-Lc in range such that  13*F << Lg-LC-Lc
<0.5*Fsw,
%% where F= fundamental frequency and Fsw is switching frequency.
%% For this design we keep 13*F < Lg-LC-Lc < 0.5*Fsw.
%% V is L-L voltage, I phase current, Fo fundamental frequency, Fsw switching
frequency
%% Yogesh patel updated on Mar 31, 2009.


function [L11,Lf1,Cf1,L21]=trapdesign(V,I,Fo,Fsw)

%base impedance and inductance of drive
Zbase=(V^2)/(sqrt(3)*V*I)
Lbase=Zbase/(2*pi*Fo);
Cbase=1/(2*pi*Fo*Zbase);

% 3% and 9% drive reactors
L1=0.03*Lbase;
L2=0.09*Lbase;

%switching frequency and min-max resonance frequency
Wo=2*pi*Fsw;
Wmin=0.2*Wo;              %max allowable Lg-LC-Lc resonant frequency
Wmax=0.5*Wo;              %min allowable Lg-LC-Lc resoanat frequency
```

```
% min-max iso-Xfmr impedance
Lsmin=0.0*L1;
Lsmax=2*L1;
step=10;
Lsstep=(Lsmax-Lsmin)/step;

% consider L is function of L2=9%impedance (min value of L is 10% of L2)
% Increase L in step and find corresponding C
% Lg=Ls+L1 varies 3% to 9% as source impedance increases (Ls increase)
% Increase Lg in steps
% Find W correspond to L,C and differnt values of Lsmin<=Ls<=Lsmax
% if Wmin<W(different Ls)<Wmax satisfy, correspond L,C are the design parameter

minper=10;
perstep=5;
maxval=(100-minper)/perstep;
Lmin=0.1*L2-((perstep/100)*L2);


for k=1:1:maxval
L(k,1)=Lmin+(perstep/100)*k*L2;              %increase L in 10% step of L2
C(k,1)=1/(Wo^2*L(k,1));                  %correspond to L
   Lg=0;
P(k,1)=0;
   Lg=(L1+Lsmin)-Lsstep;


   % Increase Ls in step and find corrospending resonance frequency
for m=1:1:step+1
   Lg=Lg+Lsstep;
Lg1(m)=Lg*10^6;

F(k,m)=(1/(2*pi))*sqrt((Lg+L2)/(Lg*L2*C(k,1)+Lg*L(k,1)*C(k,1)+L2*L(k,1)*C(k,1)));
% Resonant frequency for Lg-L-C-L2 confirguration

   % Condition check Wmin<W(different Ls)<Wmax
if(F(k,m)*2*pi>Wmin)
if( F(k,m)*2*pi<Wmax)
Pass(k,m)=1;              % pass the condition
P(k,1)=P(k,1)+1;
else
Pass(k,m)=0;              % fail the conidtion
end
end
end
end
```

```
%if above conditions failed less then 80% of the Ls steps for specific value of L anc C
%then there will be no optimum value of L and C for this design

if max(P)<(0.8*(step+1))
sprintf('%s','%%%%%%%% Did not find optimum value of L and C of LC tuned Ckt
%%%%%%%%')
   Lf1=0;
   Cf1=0;
   L11=L1*10^6;       %L1 in uH
   L21=L2*10^6;       %L2 in uH
else
z=0;
for i=1:1:maxval
if P(i,1)<max(P)
else
z=i;
end
end

Lf=L(z,1)          %optimum value of L
sprintf('%s','L is equl to (Percentage of L2)')
Lfper=(Lf/L2)*100  %percentage of L2
Cf=C(z,1);         %optimum value of C

%max,min resonance frequency,transfer function and bode plot for Lg(min-max)-Lf-Cf-
L2 configuration
Frmax=(1/(2*pi))*sqrt(((L1+Lsmin)+L2)/((L1+Lsmin)*L2*Cf+(L1+Lsmin)*Lf*Cf+L2*
Lf*Cf))
Frmin=(1/(2*pi))*sqrt(((L1+Lsmax)+L2)/((L1+Lsmax)*L2*Cf+(L1+Lsmax)*Lf*Cf+L2
*Lf*Cf))

Lfperbase=(Lf/Lbase)*100
Cfperbase=(Cf/Cbase)*100

Lf1=Lf*10^6;           %Lf in uH
Cf1=Cf*10^6;           %Cf in uF
L11=L1*10^6;           %L1 in uH
L21=L2*10^6;           %L2 in uH
Lsmax1=Lsmax*10^6;     %Lsmax1 in uH
Lsmin1=Lsmin*10^6;     %Lsmin1 in uH

%[Tmax,Zinmax,Zomax]=trap((L11+Lsmin1),Lf1,Cf1,L21);
%[Tmin,Zinmin,Zomin]=trap((L11+Lsmax1),Lf1,Cf1,L21);

%subplot(2,2,1);
```

```
   %bode(Zinmin,Zinmax,Zomin,Zomax)
%subplot(2,2,2);
   % bode(Tmin, Tmax)

   R=0;
BaseR=(R/Zbase)*100

 %% Trap filter with R in series of LC tuned ckt with min Ls

num1rmax=[((L1+Lsmin)*L2*Cf+(L1+Lsmin)*Lf*Cf+L2*Lf*Cf),(Cf*R*((L1+Lsmin)+
L2)),((L1+Lsmin)+L2),0];
  den1rmax=[(Lf*Cf+(L1+Lsmin)*Cf),Cf*R,1];
Zormax=tf(num1rmax,den1rmax);                %output impedance
  den2rmax=[(Lf*Cf+L2*Cf),Cf*R,1];
Zinrmax=tf(num1rmax,den2rmax);               %input impedance
  num2rmax=[Lf*Cf,Cf*R,1];
Trmax=tf(num2rmax,num1rmax)*Zbase;                %transfer function

  %% Trap filter with R in series of LC tuned ckt with max Ls

num1rmin=[((L1+Lsmax)*L2*Cf+(L1+Lsmax)*Lf*Cf+L2*Lf*Cf),(Cf*R*((L1+Lsmax)
+L2)),((L1+Lsmax)+L2),0];
  den1rmin=[(Lf*Cf+(L1+Lsmax)*Cf),Cf*R,1];
Zormin=tf(num1rmin,den1rmin);                %output impedance
  den2rmin=[(Lf*Cf+L2*Cf),Cf*R,1];
Zinrmin=tf(num1rmin,den2rmin);               %input impedance
  num2rmin=[Lf*Cf,Cf*R,1];
Trmin=tf(num2rmin,num1rmin);                 %transfer function

%subplot(2,2,4);
bode(Trmax)                          %**bode plot optional
%subplot(2,2,3);
 % bode(Zormin,Zinrmin,Zormax,Zinrmax)          %**bode plot

end
```

APPENDIX C: LCL filter damping calculation

```
%% Calculate Resonance Frequency and plot the Impedance of LCL filter Vs Frequency
for several damping circuits

functionZo = LCLdamping(V,I,Fo,R)

%base impedance and inductance of drive
Zbase=(V^2)/(sqrt(3)*V*I)
Lbase=Zbase/(2*pi*Fo);
Cbase=1/(2*pi*Fo*Zbase);

BaseR=(R/Zbase)*100

L1=0.03*Lbase
L2=0.09*Lbase
C=0.05*Cbase
C1=0.04*Cbase;
C2=0.01*Cbase;
R2=8;
R3=500;
R4=2000;
Rd=0.5;
Ld=0.02*Lbase;


%% Configuration L1--- C ---L2
%Impedance see from converter side
num1=[L1*L2*C, 0, (L1+L2), 0];
den1=[L1*C, 0, 1];
Zc1=tf(num1,den1);

%Impedance seen from grid side
den11=[L2*C,0,1];
Zg1=tf(num1,den11);

%Transfer function ig/Vc or ic/Vg
den12=[1];
Tr1=tf(den12,num1)*Zbase;

% Resonance frequency
Fr=(1/(2*pi))*(sqrt((L1+L2)/(L1*L2*C)))

%bode(Tr1)
```

```
%% Configuration L1---C&R serie ---L2
%Impedance see from converter side
num2=[L1*L2*C, C*R*(L1+L2), (L1+L2), 0];
den2=[L1*C,C*R,1];
Zc2=tf(num2,den2)/Zbase;

%Impedance seen from grid side
den21=[L2*C,C*R,1];
Zg2=tf(num2,den21)/Zbase;

%Transfer function ig/Vc or ic/Vg
den22=[C*R,1];
Tr2=tf(den22,num2)*Zbase;

%bode(Tr2)


%% Configuration L1---C1 & (C2&R2 series) parallel ---L2
%Impedance see from converter side
num3=[L1*L2*C1*C2*R2, L1*L2*(C2*R2+C1), (L1+L2)*C2*R2, (L1+L2), 0];
den3=[L1*C1*C2*R2, L1*(C2*R2+C1),C2*R2, 1];
Zc3=tf(num3,den3)/Zbase;

%Impedance seen from grid side
den31=[L2*C1*C2*R2, L2*(C2*R2+C1),C2*R2, 1];
Zg3=tf(num3,den31)/Zbase;

%Transfer function ig/Vc or ic/Vg
den32=[C1*C2*R2, (C2*R2+C1), 0];
Tr3=tf(den32,num3)*Zbase;

BaseR2=(R2/Zbase)*100

%% Configuration L1---C & R3 parallel ---L2
%Impedance see from converter side
num4=[L1*L2*C*R3, L1*L2, (L1+L2)*R3, 0];
den4=[L1*C*R3, L1, R3];
Zc4=tf(num4,den4)/Zbase;

%Impedance seen from grid side
den41=[L2*C*R3, L2, R3];
Zg4=tf(num4,den41)/Zbase;

%Transfer function ig/Vc or ic/Vg
```

```
den42=[R3];
Tr4=tf(den42,num4)*Zbase;

BaseR3=(R3/Zbase)*100

%% Configuration L1 & R4 parallel ---C & R4 parallel ---L2 & R4 parallel
%Impedance see from converter side
num5=[L1*L2*C*(R4^3), 3*L1*L2*(R4^2), (R4^3)*(L1+L2), 0];
den5=[L1*C*(R4^2), 2*L1*R4, (R4^2)];
Zc5=tf(num5,den5);

%Impedance seen from grid side
den51=[L2*C*(R4^2), 2*L2*R4, (R4^2)];
Zg5=tf(num5,den51);

%Transfer function ig/Vc or ic/Vg
den52=[L1*L2*R4, (R4^2)*(L1+L2), (R4^3)];
Tr5=tf(den52,num5);


%% Configuration L1 --- (Ld& Rd parallel) & C series ---L2  parallel
%Impedance see from converter side
num6=[L1*L2*Ld*C, (C*Rd)*(L1*L2+L1*Ld+L2*Ld), Ld*(L1+L2), Rd*(L1+L2), 0];
den6=[L1*Ld*C, C*Rd*(L1+Ld), Ld, Rd];
Zc6=tf(num6,den6)/Zbase;

%Impedance seen from grid side
den61=[L2*Ld*C, C*Rd*(L2+Ld), Ld, Rd];
Zg6=tf(num6,den61)/Zbase;

%Transfer function ig/Vc or ic/Vg
den62=[Ld*C*Rd, Ld, Rd];
Tr6=tf(den62,num6)*Zbase;

BaseRd=(Rd/Zbase)*100
```

Curriculum Vitae

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- Power engineer for Multidrive Project
  - Design of AC/DC precharge, control bay and harness
  - Selection of components for Inverter, LCL and precharge
  - Updates one-line diagram, FRS and design documents
  - Competitive cost analysis, design review and drive build
  - Testing of Fr8 Inverter, Frame10 common bus inverter and LCL filter
- Designed and analyzed LCL and Trap filters for active converters
- Competitive design analysis of active filters and watt loss calculation
- AFE control implementation using TI DSP TMS320F2812
- Completed open IGBT module test of PF755 FR7 drive and set the thermal regulator for liquid cool version
- Managed PF700L FR2, 700S control 300HP, 480Vac, 360A Direct Liquid Cooled Drive project
- IGBT Module characterization
- Designed and layout of gate drive board for PF700L Fr2 Drive
- Qualification testing of Drives
- Completed EMC tests, UL, CE and TUV certification of PF700L FR2 and PF753 FR2-7 drives.

Electrical Engineer, Spellman High Voltage Electronics Corp. Hauppauge, NY (Oct 2005- Aug 2006)

- Designed 52kW, 800Vdc quasi resonant power supply
- Performed thermal evaluation of the power supply
- Completed UL certification tests and EMC tests
- Prepared the test data sheets and test reports

Electrical Engineer, APL Engineered Materials Inc. Urbana, IL (Oct 2003- Sep 2005)

- Analyzed and tested the IM-5 power supply for hollow cathode and filament ion gun
- Designed and developed a new dispenser controller
- Designed power supply controller for cluster beam application
- Automation of Sc Annealing process: control the high vacuum system, cryogenic pump, furnace, high pressure argon supply

Research Assistant, Grainger Power Electronics and Motor Drives Laboratory, Chicago, IL (Aug 2001- Sep 2003)

- Developed new power electronics converter topologies for switched reluctance generator and performed simulations using PSIM software and Matlab-Simulink
- Actively involved in simulations and testing of buck, boost and fly back converter topologies using PSIM.

Publication and others:

- Y. P. Patel, and B. Fahimi, "Thyristor-based resonant current controlled switched reluctance generator for distributed generation," *Journal of Electrical Engineering and Technology*, March 2007
- Y. Patel, D. Pixler, and A, Nasiri, "Analysis and design of TRAP and LCL filter for active switching converters," *IEEE International Symposium on Industrial Electronics*, Bari, Italy, July. 2010.
- Y. Patel, A. Nasiri, "DC distribution system architecture and control for wind power application", IEEE Energy conversion congress and exposition (ECCE), pp. 3493-3499, Sep 2012.
- Contributed in a chapter titled "Switched reluctance motor drives," in the book titled "Vehicular Electric Power Systems: Land, Sea, Air, and Space Vehicles," by A. Emadi, Marcel Dekkar, Inc., 2003
- 6 pending patents

Computer Skills:

- **Languages:** C/C++, Assembly language, VHDL
- **Simulation Software:** Matlab-Simulink, PSIM, Simplorer
- **PLC software & Others:** PLC programming for SIMATIC S7 Micro/WIN V 3.2 from Siemens, RSLogix 5000 from Allen Bradley, AutoCAD Electrical, Microsoft Visio, DX Designer and PCB layout software Expedition from Mentor Graphics, SAP and Lotus Notes.