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1968 (5th) The Challenge of the 1970's

Apr 1st, 8:00 AM

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DIGITAL FILTERING IN SPACE COMMUNICATION
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Introduction

In ground receivers for space applications, a bank of filters is frequently used to demultiplex the received subcarriers. Such filter banks are also frequently used for measurements of the doppler shift of the received signals. These filters are generally characterized by having a narrow bandwidth. This means that they are rather costly and often difficult to construct to the desired specifications. Since the baseband structure varies from mission to mission, the useful life of these baseband filters is short.

An alternate approach to the filtering problem that can cut cost and increase flexibility while at the same time improve system performance is therefore welcome. Such an approach exists in digital filtering.

A digital filter is a computer program that allows digital computer to be used as a linear filter. Such programs can now be written for a general purpose computer that allows the computer to be used as a filter bank in real time.

The block diagram of a typical digital filter bank is shown in fig. 1. The signals to be filtered are passed through an A-D converter into the computer. The computer output is passed through a D-A converter thus completing the filtering operation.

Since the program can easily be modified, such parameters as center frequency, bandwidth, and rate of cut-off can be altered virtually without cost as the mission requirements demand. If desired, other operations such as demodulation and decoding can also be done by the computer at the same time.

This paper discusses the techniques of digital filtering and their application to the baseband filtering problem. The techniques are discussed with reference to the digital resonator, the digital equivalent of the parallel RLC network. Practical considerations such as performance limitations due to computer size and speed for real time operation are considered. In conclusion, two examples of typical digital filters and their performance is discussed.

Synthesis of Digital Resonators

The baseband filtering problem can frequently be solved by use of a suitable combination of single tuned circuits with proper center frequencies and bandwidths. Because of this central role played by the single tuned circuitry or resonator, the synthesis of digital resonators will be discussed in detail.

An analog single tuned circuit, or resonator, consisting of a parallel combination of a resistor, coil and capacitor is shown in fig. 2. Its response

to an input can be described by the differential equation:

$$C \frac{d^2 v}{dt^2} + G \frac{dv}{dt} + \frac{1}{L} v = \frac{di}{dt} \qquad (1)$$

or by the transfer function

$$H(s) = \frac{1}{C} \cdot \frac{s}{s^2 + \frac{G}{C} s + \frac{1}{LC}} \qquad (2)$$

For this circuit to exhibit oscillatory behaviour the condition

$$\left(\frac{G}{C}\right)^2 - \frac{4}{LC} < 0 \qquad (3)$$

must be satisfied. When this condition is satisfied, the circuit has a pair of complex poles located at:

$$P_{1,2} = \frac{-G}{2C} \pm j \sqrt{\frac{1}{LC} - \left(\frac{G}{2C}\right)^2} \qquad (4)$$

and zeros at $s = o$ and $s = \infty$

Fig. 3 shows the s-plane picture for the circuit in fig. 2.

When the output from the single tuned circuit is sampled every T sec. as indicated in fig. 4, we have a situation that corresponds functionally to the digital filtering situation. The transfer function of the combination of the tuned circuit and the sampling switch results in the s-plane picture shown in fig. 5.

When we are working with sampled data systems, as we are in this case, it is more convenient to work in the Z-plane rather than the s-plane, since the s-plane contains so much redundant information. The relationship between the two planes is given by the transformation:

$$Z = e^{sT} \qquad (5)$$

where T is the sampling interval.

By use of the transformation, 5, we can map the s-plane point by point into the Z-plane. We see that the origin in the s-plane maps into the point $Z = 1$ and ∞ in the s-plane maps into the origin in the Z-plane. In this manner the s-plane pole zero pattern for the single tuned circuit, fig. 5, can be mapped into the corresponding Z-plane picture, fig. 6. The zero at the origin in the Z-plane corresponds to the zero at ∞ in the s-plane. We also see that the jω-axis in the s-plane maps into the unit circle in the Z-plane.

We have obtained the Z-plane picture, fig. 6, by periodically sampling the output of the single

tuned circuit. From this Z-plane picture we can form the transfer function, $H_D(Z)$, between the input and the sampled output:

$$H_D(Z) = \frac{Y(Z)}{X(Z)} = \frac{Z(Z-1)}{(Z-\gamma_1)(Z-\gamma_2)} = \frac{Z(Z-1)}{Z^2 - KZ - L} \quad (6)$$

This transfer function can be interpreted as the response $y(nT)$ of a circuit to an excitation $x(nT)$, where $X(Z)$ is the Z-transform of $x(nT)$ defined by 7.

$$X(Z) = \sum_{n=0}^{\infty} x(nT) \, z^{-n} \quad (7)$$

By clearing fractions in 6 we obtain the equation:

$$\left[1 - \frac{K}{Z} - \frac{L}{Z^2} \right] Y(Z) = \left[1 - \frac{1}{Z} \right] X(Z) \quad (8)$$

or:

$$Y(Z) = \frac{K}{Z} Y(Z) + \frac{L}{Z^2} Y(Z) + X(Z) - \frac{1}{Z} X(Z) \quad (9)$$

By use of 7 we can easily show that this equation in Z corresponds to the following difference equation in nT:

$$y(nT) = K \, y[(n-1)T] + L \, y[(n-2)T] + x(nT) - x[(n-1)T] \quad (10)$$

This is a second order difference equation. This equation can easily be implemented by use of a digital computer. The flow chart for this implementation is shown in fig. 7. Each time delay, T, corresponds to a register (or other storage unit) in the computer. We note that zeros in the transfer function are caused by feed forward delays, while poles are caused by feedback delays.

To this flow chart will be referred to as a digital network. This digital network will have a pair of complex poles located at:

$$\gamma_{1,2} = \frac{K}{2} \pm j \sqrt{-\left[L + \left(\frac{K}{2} \right)^2 \right]} \quad (11)$$

when:

$$L + \left(\frac{K}{2} \right)^2 < 0 \quad (12)$$

The network also has zeros at $Z = 0$ and $Z = 1$. Since $Z = e^{sT}$, where T is the sampling interval, we can obtain the complete frequency response of the digital network by letting $s = j\omega$, i.e., $Z = e^{j\omega T}$.

When we make this substitution we obtain (after some simplification) the amplitude response of this digital network.

$$\left| H_D(\omega) \right| = \frac{2 \left| \sin \frac{\omega T}{2} \right|}{\sqrt{1 + K^2 + L^2 - 2K(1-L)\cos \omega T - 2L \cos 2\omega T}} \quad (13)$$

This amplitude response is plotted in fig. 8, for:

$K = .9$

and

$L = -.81$

We notice that the frequency response is periodic with period $\frac{1}{T}$. This is due to the effect of sampling and is only a reflection on the fact that the bandwidth of the signal, W, must satisfy the sampling theorem

$$W < \frac{1}{2T} \quad (14)$$

in order to avoid aliasing. Since we are only using the central portion $\left(-\frac{1}{2T}, \frac{1}{2T} \right)$ of the spectrum, the periodic nature of the frequency response is unimportant.

We now have a digital network that, for our purposes, has the same response as a single tuned circuit. We therefore call this network a digital resonator.

The digital resonator can be specified in terms of the coefficients in the computer program, K and L, in terms of its pole locations or more usually in terms of its center frequency and bandwidth.

When we apply the usual high Q approximations for resonant circuits we obtain the following simplified formulas for the digital resonator.

Resonant Frequency:

$$f_o = \frac{1}{2\pi T} \cos^{-1} \left(\frac{K}{2 \sqrt{-L}} \right) \quad \text{Hz} \quad (15)$$

Filter bandwidth between 3 db points:

$$f_\beta = \frac{1 - \sqrt{-L}}{\pi T} \quad \text{Hz} \quad (16)$$

For the filter designer it is usually more informative to know the filter design in terms of the desired filter parameters. When we solve for K and L in terms of the resonant frequency and bandwidth we obtain the expressions:

$$L = - (1 - \pi T f_\beta)^2 \quad (17)$$

and:

$$K = 2(1 - \pi T f_\beta) \cos 2\pi f_o T \quad (18)$$

In concluding this section, we point out that the same technique that was used to obtain the digital resonator from the corresponding analog filter can also be used for any other filter for which an s-plane pole zero pattern can be obtained.

Furthermore, we note that the response of the network is unaffected by whether the zero in the transfer function occurs at the input or output. By use of this fact we can implement the digital resonator as shown in fig. 9. This saves one storage operation without altering the response of the network. This form of the resonator can therefore be implemented with one register less. Since this form uses the minimum number of delay elements it is frequently referred to as the canonical form.

An Improved Digital Resonator

The digital resonator modeled after the parallel RLC circuit has a non-zero response at $f = \frac{1}{2T}$. As a result the increase in attenuation is not as rapid toward the high frequency end of the band as toward the low. If this effect is troublesome, it can very easily be remedied. The cure is to take the zero at the origin in the Z-plane and move it to $Z = -1$. When this is done we obtain the transfer function:

$$H_D(Z) = \frac{(Z+1)(Z-1)}{Z^2 - KZ - L} \qquad (19)$$

The amplitude response of this improved digital resonator is:

$$\left| H_D(\omega) \right| = \frac{4 \left| \cos \frac{\omega T}{2} \right| \left| \sin \frac{\omega T}{2} \right|}{\sqrt{1 + K^2 + L^2 - 2K(1-L)\cos\omega T - 2L \cos 2\omega T}} \qquad (20)$$

The frequency response of the improved resonator for the case $K = .9$, $L = -.81$ is shown in fig. 10.

As we see the two digital resonators differ only in their frequency response near the sampling frequency. In the high Q case the same formulas for bandwidth and resonant frequency can therefore be used for both resonators.

The only remaining task in this section is to realize this resonator as a flow chart for computer programming. This we will do in the same manner as before. from the transfer function, 19, we form the difference equation, 21:

$$y(nT) = K\, y[(n-1)T] + L\, y[(n-2)T] + x(nT) \\ -x[(n-2)T] \qquad (21)$$

This difference equation gives us the flow chart, fig. 11. This flow chart is converted into the canonical form shown in fig. 12 in the same manner as previously. Both implementations have the same response but the one shown in fig. 12 is more conservative with respect to high speed memory.

Effects of Computer Speed and Size

That the size and speed of the computer used to synthesize the filter limits the complexity of a filter if it is to be used in real time is probably not so surprising. It is therefore well worth to look closely at the proposed filter structure to see if it will yield the best possible performance for a given computer size.

In our discussion of current real time capability we will use the IBM 360/50 as an example of a modern high-speed general purpose computer. This computer has approximately the following execution times:

ADD FIXED POINT	4 μsec
ADD LOGICAL	4 μsec
ADD FLOATING POINT	7 μsec
OR EXCLUSIVE	6 μsec
MULTIPLY FIXED POINT	21 μsec
MULTIPLY FLOATING POINT	25 μsec
LOAD REGISTER	3 μsec

The digital resonator described in this paper requires two multiplications and three additions. If it is implemented in floating point arithmetic it will therefore require approximately 71 μsec per processed data point (when we neglect possible small delays caused in loading and unloading). With a sampling rate of 2.10^3 samples/sec. we see that a bank of 6 to 7 different filters can be implemented by the same registers in real time by the IBM 360/50 computer if the operations are done serially. The speed of operation can be increased in two ways. One is by use of a higher speed computer, the second is by use of a computer that can perform many operations in parallel.

Computers that perform additions in a fraction of a μsec and have multiplication times of about one μsec are currently representative of the most advanced machines available. With such a computer, it is possible to bring the execution time of the filter down to about 5 μsec. This will allow the real time use of approximately 10 filters in a 10 KHz or 100 filters in a 1 KHz bandwidth.

Of operations that should be avoided whenever possible are those requiring a power series expansion for a solution. Of these are square rooting, log and the trigonometric functions. All these operations require repeated multiplications and since multiplication is a relatively slow operation they all require considerable time.

When sin and cos functions are needed, they can usually be more easily generated by periodically pulsing a very high Q digital resonator.

Gain, Sampling Rate and Noise

When we are working with digital networks we encounter many phenomena that are not present in the analog world. One of these is pleasant and is the lack of interaction or loading when several circuits are cascaded. Since we are working with numbers and not voltages and currents, we can cascade any number of digital resonators until we obtain the desired frequency response. The response of one resonator is not affected by the circuits it is connected to.

Another phenomena is filter gain. A digital filter of conventional design will usually have a gain of between two and ten in the passband. The narrower the bandwidth is, the greater the gain will be. If we perform several filtering operations on a signal its amplitude may be so large as to cause an overflow. We must therefore be on the lookout for this contingency and if necessary, multiply the signal by an appropriate fraction to prevent an overflow from occurring. If we work in floating point arithmetic the danger of overflow is greatly reduced as compared to fixed point arithmetic. The price of this advantage is more complex hardware and somewhat slower operation.

Since a digital filter works with numbers, not with voltages and currents, it is subject to the effects of roundoff errors. The effect of roundoff errors is similar to quantizing noise.

The noise caused by roundoff errors is reduced by using a longer word length.

The sampling rate places a limitation on the high frequency content of the input signal. The sampling theorem, 14, says that at least two samples must be taken per sec. for each Hz of bandwidth of the signal. When an ideal filter is used to limit the bandwidth of the input signals this definition poses new difficulties. When a real filter is used there is a big question as to how the bandwidth should be defined. The higher the sampling rate is, the smaller the aliasing error will be. In order to keep the aliasing and reconstruction errors to about 1 to 2%, it is necessary that the bandwidth, W, is defined as the point at which the response of the filter is down 20 db.

A Typical Digital Resonator

In order to demonstrate the techniques of designing a digital resonator, a computer program was written for a resonator with a center frequency $f_o = \frac{1}{6T}$ Hz and a 3 db bandwidth of $f_\beta = \frac{1}{10\pi T}$ Hz. The digital resonator satisfying these requirements has $K = .9$ and $L = -.81$. The frequency response for this resonator is shown in fig. 8. Fig. 13 shows an input signal consisting of a step with a finite rise time followed by a rised sinewave with a frequency approximately equal to f_o. The resulting output from the digital resonator is shown below the input. The actual signals consist of sample points but the curves have been drawn continuous for convenience in observation.

Conclusions

In this paper we have outlined a system capable of implementing a large number of different filter structures on a digital computer. The filtering problem can in most cases be conveniently and easily solved by use of a combination of digital resonators. The parameters of the digital resonator K, and L, have been directly related to the center frequency and bandwidth of the digital resonator.

Examples of digital resonators and plots of frequency response and input and output waveforms have been presented. It is seen that the digital resonator acts like a parallel RLC circuit driven by a current source. The validity of the approximate formulas developed for center frequency and bandwidth can easily be established by measuring these parameters on the given curves.

Some of the problems associated with computer speed and word length have been pointed out. In conclusion it should also be pointed out that contrary to the situation in the analog world, it is no more difficult to build a very low frequency digital filter than one operating at moderate frequencies. This is due to the fact that the response of the digital filter is determined by numerical constants and not by enormous coils and capacitors. The digital filter is therefore very well suited for use when the specifications call for narrow bandwidths at low frequencies.

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J. F. Kaiser, F. Kuo, Eds. 1966, System Analysis by Digital Computer, Wiley, pp. 218-277.

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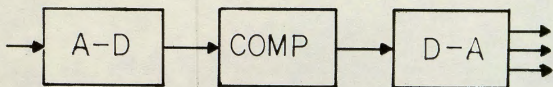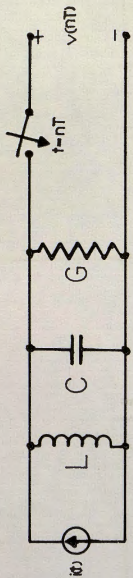
1. Block diagram of a digital filter.
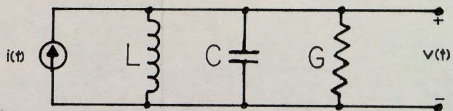
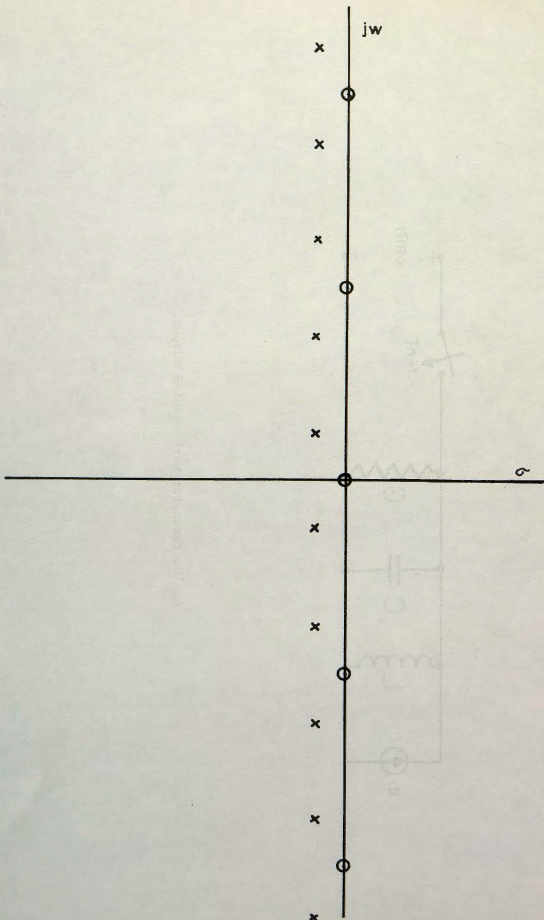2. Analog resonator (parallel RLC network).
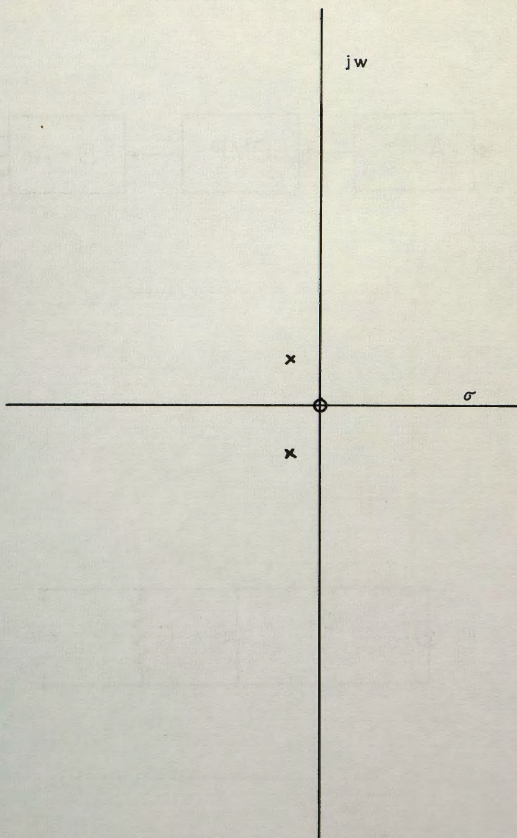
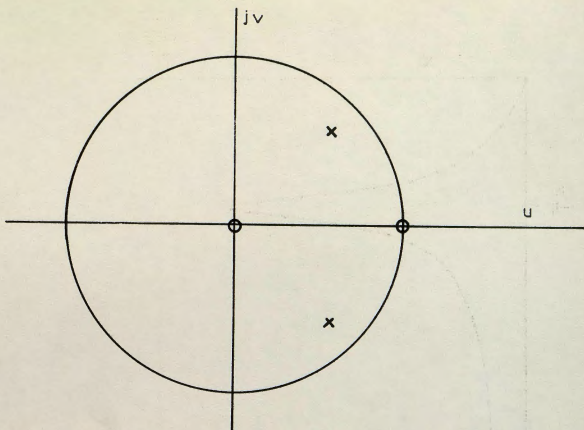3. S-plane pole-zero pattern for the analog resonator.
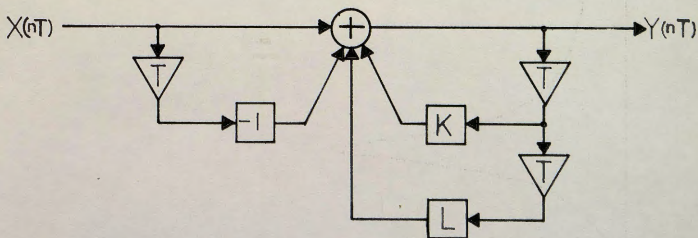
4. Analog resonator with sampled output.

5. S-plane pole-zero pattern for the analog resonator with sampled output.

6. Z-plane pole-zero pattern for the analog resonator with sampled output. This is also the pole-zero pattern for the digital resonator shown in fig. 7.


7. Flow diagram for a digital resonator. T is a delay of one sampling interval. This digital resonator has the same pulse response (at the sampling times) as the RLC network in fig. 2.
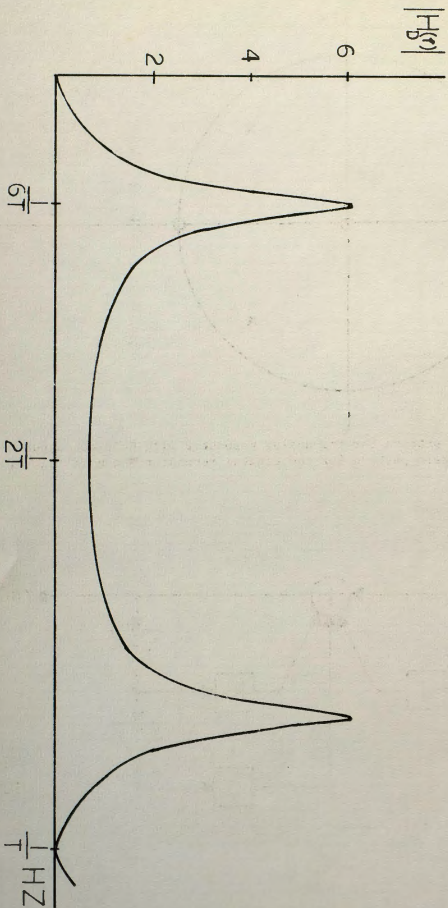
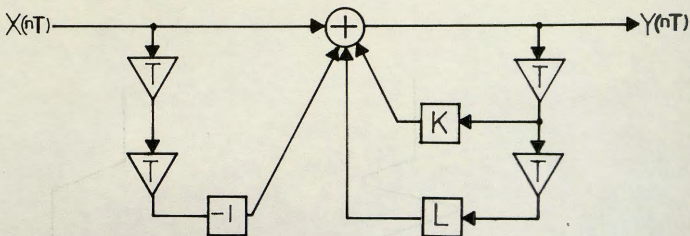8. Amplitude response for the digital resonator.
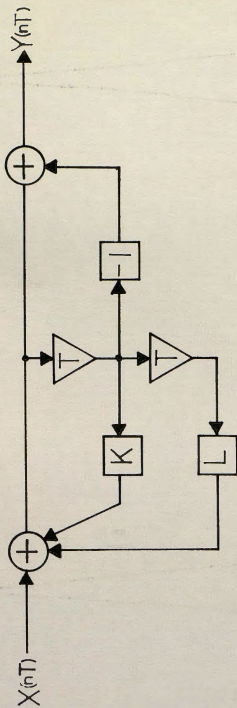
9. A more economical implementation of the digital resonator shown in fig. 7. This form has the same response but uses the minimum number of delay elements. It is therefore often referred to as the canonical form.
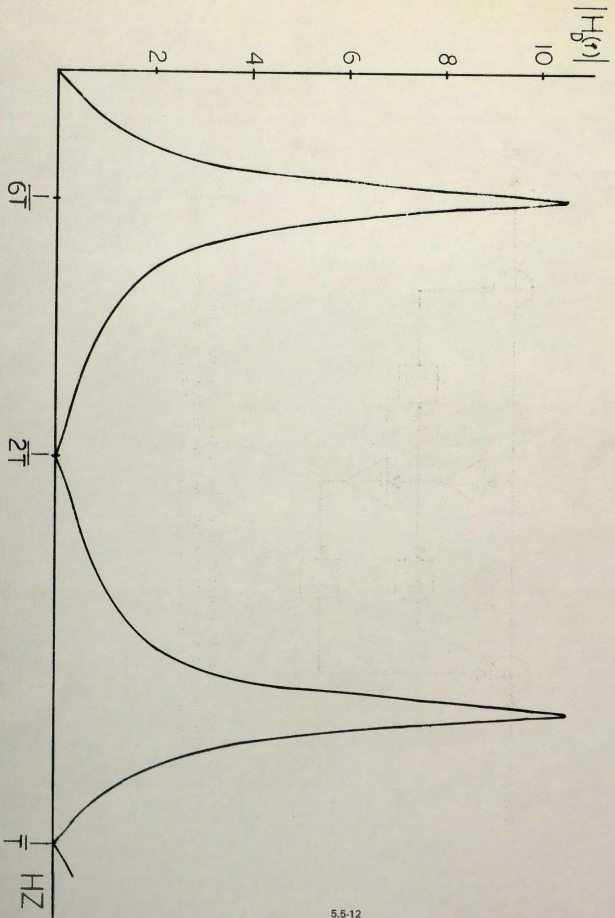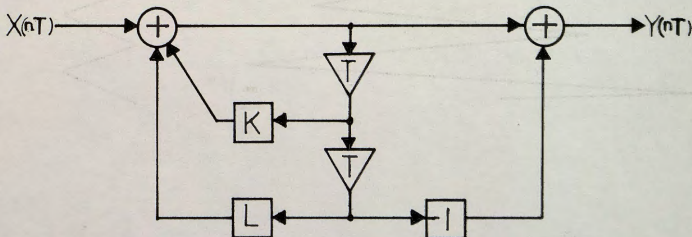
10. Frequency response of the improved digital resonator.

11. An improved digital resonator. This resonator has zero response both for $f = o$ and for $f = \frac{1}{2T}$.

12. Canonical form of the improved digital resonator.

13. Input-Output Waveforms for the digital resonator in fig. 9.

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