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## AIRBORNE COMPUTER TECHNOLOGY

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### ABSTRACT

The development of airborne digital computer has been greatly influenced by rapid technological advances. This paper provides an overview of the present status and the direction of further evolution. It discusses the changes that are taking place in the areas of hardware, software and computer organization; and suggests a number of approaches towards a broadened usage of airborne computer to take advantage of its increasing capability and decreasing cost.

### INTRODUCTION

The airborne digital computer has been in existence for less than twenty years. In this short time, however, much has been accomplished. It has been used in the guidance of our space flight to the moon. It is at the control of our land based and submarine based intercontinental ballistic missiles. It performs the navigation, fire control, weapon delivery and electronic warfare computations in our military aircraft. It is also appearing now in our commercial airliners.

During this time, the computing speed of a typical airborne computer has increased by two orders of magnitude, and the storage by more than one order of magnitude. This is accompanied by a reduction in its weight, size, power consumption and cost, and, at the same time, an improvement in its reliability and flexibility. This trend of dynamic progress is continuing.

This paper will provide an overview of the present status of airborne computer technology and the direction of its further development. Discussion will address the advances that are being made in the areas of hardware, software and computer organization. A number of approaches towards the broadened usage of airborne computers, to take advantage of its increasing capability and decreasing cost will be suggested.

### TREND OF DEVELOPMENT

The trend in development of the airborne computer is exemplified by the three charts appearing with the figures at the end of this paper.

Figure 1 shows the growth of the computer operating speed through the years. This growth is an indication of the persistent increase in the computing capacity of the airborne computer. It is made possible by a combination of the following efforts:

- 1) Use of faster memories
- 2) Use of faster logic circuits
- 3) Use of parallel arithmetic operations
- 4) Use of overlap and indexing techniques.

This increased speed allows the airborne computer to perform broader types of functions, to be shared by larger number of tasks, and to be used in a more flexible manner. A contemporary computer can perform 200,000 to 800,000 operations per second. With this capability, a single computer or a single system of computers, can perform all the processing functions required on an aircraft, including that for flight control.

Figures 2 and 3 show, respectively, the trends of weight and power consumption of an airborne computer. Together, weight and power represent the "burden" sustained for the use of a computer. Both have been reduced through the use of circuits with higher level of integration, memories with higher efficiency, and better packaging and interconnection techniques. A typical contemporary computer, with 8000 words of internal memory, weighs between 15 and 50 pounds and requires between 50 and 250 watts of power, although these numbers can be considerably lower or higher for designs to meet specific requirements.

### A TYPICAL GENERAL PURPOSE AIRBORNE COMPUTER

AP-101 developed by the Federal Systems Division of International Business Machines Corporation is a typical contemporary general purpose airborne computer. As shown in Figure 4, it measures 7.62 inches x 10.12 inches x 19.56 inches and fits a standard aircraft transport rack (ATR) case. It can be used to perform the computational tasks for navigation, guidance, weapon delivery and data management onboard an airplane, or similar tasks on a large space vehicle.

The functional characteristics of AP-101 can be summarized as in Figure 5, its physical characteristics as in Figure 6.

#### A TYPICAL SUBSYSTEM PROCESSOR

SP-1, a smaller computer belonging to the same family as AP-101, is designed to serve the subsystem applications. It can perform the processing functions required for the midcourse guidance of a missile, the stabilization and control of a drone, the navigation of an aircraft, or the attitude control and stabilization of a spacecraft. As shown in Figure 7, it measures 4.1 inches  $\times$  10.1 inches  $\times$  13.6 inches.

The functional and physical characteristics of SP-1 are summarized in Figures 8 and 9. SP-1 can also be supplied without structure and power supply, to be integrated into the subsystem it serves. The physical parameters of the basic assemblies are also shown in Figure 9.

#### EVOLUTION OF CIRCUIT TECHNOLOGY

Subminiature vacuum tubes, discrete semiconductor components and hybrid circuits were used in the early airborne digital computers. The preference quickly shifted to integrated circuits when these were developed and then improved. Throughout the mid-1960's, as the yield of integrated circuits increased, the use of bipolar silicon integrated circuits became almost universal. This, together with memory improvements, brought about a general increase in computing speed and a reduction in weight and power consumption. With reduced hardware penalty and improved reliability, parallel arithmetic operations became generally used in computers designed during this period. Word length became more standardized. Floating point number representation began to appear. The number of instructions in a basic instruction set started to grow faster. At the same time, the cost of airborne computers became lower.

The march towards higher density circuits regained momentum in the late 1960's when medium scale integration (MSI) and large scale integration (LSI) circuits became available.\* A typical contemporary computer, such as AP-101, uses MSI circuits with up to thirty gates per chip. As the yield of LSI circuits increase, the interconnecting and packaging technology improve and the designers learn to use LSI circuits more effectively, the level of circuit integration used in an airborne computer is expected to continue to grow. There are already computers built with LSI circuits containing several hundred gates per chip. If the present rate of progress continues,

thousands of LSI circuits containing several/gates per chip will be used in airborne computers of the late 1970's. This trend is illustrated in Figure 10.

The impact on the design and application of airborne computer due to the wide use of LSI circuits can be expected to be even greater than that caused by the introduction of IC. The potential benefits to the computer due to the use of LSI are:

- 1) Smaller size and weight
  - Expectation: 10 mil<sup>2</sup> per gate, in late 1970's
- 2) Higher speed
  - Shorter distances, less capacitance
- 3) Lower power
  - Less capacitance to drive
- 4) Greater reliability
  - Simpler processing (less manual and more automated)
  - Fewer external connections
- 5) Lower cost
  - More automated fabrication and assembly
  - Expectation: 1¢ per gate, in late 1970's

Summarized below are some of the special efforts that are being undertaken so that LSI's of increasing level of complexity can be fully utilized:

- 1) Computer aided design (CAD) for chip layout, placement and simulation.
- 2) Chip layout to minimize external wiring and maximize chip standardization.
- 3) Discretionary wiring technique to increase chip utilization — to use a standardized chip for different functions, and to tolerate the existence of chip imperfections.
- 4) Incorporation of built-in test circuits.
- 5) Packaging techniques to provide sufficient cooling to the chips.
- 6) Approaches to increase the yield of acceptable chips.

In conjunction with the evolution towards higher levels of circuit integration, there is also a trend towards the increased usage of metal oxide semiconductor (MOS) devices, which utilize field effect to enhance the flow of current in a semiconductor. In comparison with bipolar

\*The dividing lines between IC, MSI and LSI are not uniformly defined. Generally, a single chip containing up to ten gate circuits is referred to as an IC, one containing ten to hundred gate circuits as MSI, and one containing more than one hundred gate circuits as LSI.

devices, a MOS device has the following general characteristics:

- 1) Smaller size. The chip area required for a MOS gate is one-fifth to one-tenth that of a bipolar gate.
- 2) Higher input impedance. While a bipolar device is current controlled, a MOS device is voltage controlled. It has no fanout limitation, and permits the use of simpler circuits.
- 3) Lower power consumption.
- 4) Simpler process. Fewer diffusion steps. Fewer photomask steps. Expectation of higher yield and lower cost.
- 5) Slower speed. Due to stray circuit capacitance and the necessary charging and discharging of this capacitance. This disadvantage is being overcome by device design to reduce the capacitance and circuit design to take advantage of the smaller geometry.

In the development of MOS technology, the early efforts were mostly directed towards P-channel MOS (P-MOS) devices because they were easier to produce. N-channel MOS (N-MOS) devices are capable of higher switching speed and smaller size since they depend on the mobility of electrons rather than holes. However, N-MOS is relatively less utilized because more stringent manufacturing controls are needed for its production. The current emphasis is on complementary MOS (CMOS) which combines P-channel and N-channel devices on the same substrate. Although somewhat larger in size and requiring more processing than P-MOS, CMOS devices are capable of higher speed, have higher noise immunity and consume much less power. It is expected that the several different approaches to MOS as well as the variations to each of these approaches will all be further explored and utilized. However, CMOS or one of its refinements will likely become the dominant circuit technology in the late 1970's.

#### EVOLUTION OF MEMORY TECHNOLOGY

Most of the early airborne computers used electromechanical memories: drums or discs. This gave way to devices which contain no moving parts, do not require maintenance and are not restricted to serial access. Many types of these devices have been used, including thin film, wired array and multiaperture memories. However, until recently, the preference gravitated towards ferrite coincident - current cores and plated wires. The cores provide fast, high density, random access, large size memories at a few cents per bit. The plated wires provide nondestructive readout (NDRO) capability. A typical contemporary computer offers either, or an optional choice, of these two memories. Figure 11 shows a section of the core memory used in AP-101. The core size

is 8 mils ID, 14 mils OD. 147,456 cores are contained in each memory module, organized into 8,192 half words.

AP-101 can be provided with up to 65,536 half words of internal memory with an addressing capability of 524,288 halfwords. The design characteristics of the core memory are as follows:

- 1) Storage Capacity: 32,768, 36-bit words (including 2 parity bits and 2 storage protect bits per word)
- 2) Module Size: 8,192, 18-bit half words (including 1 parity bit and 1 storage protect bit per half word)
- 3) Access Time: 450 nanoseconds
- 4) Cycle Time: 900 nanoseconds
- 5) Power: 110 watts operating, 35 watts standby
- 6) Weight: 18.65 pounds
- 7) Size: 508 cubic inches

AP-101 design also provides for an interchangeable procured NDRO plated wire memory, with the following characteristics.

- 1) Storage Capacity: 32,768, 36-bit words (including 2 parity bits and 2 storage protect bits per word)
- 2) Module Size: 8,192, 18-bit half words (including 1 parity bit and 1 storage protect bit per half word)
- 3) Access Time: 400 nanoseconds
- 4) Cycle Time: 1.0 microsecond write, 0.5 microsecond read
- 5) Power: 43 watts operating, 25 watts standby
- 6) Weight: 18.5 pounds
- 7) Size: 405 cu. in.

With the advent of LSI, semiconductor memory has appeared in airborne computers. This usage is expected to increase due to the many attractive characteristics of the semiconductor memory. The principal ones are listed below:

- 1) High speed
- 2) High density
- 3) Low power consumption
- 4) Technology common to that for processor logic circuits
- 5) Possibility of combining logic and storage functions on the same chip
- 6) Continuous output capability, resulting in good signal-to-noise ratio.



Development work in semiconductor memory is currently being undertaken in several different technological approaches. The salient features of the main approaches are summarized in the following:

- 1) Technology based on bipolar junction transistor
  - a) Flip flop commonly used as the storage element
  - b) High switching speed
  - c) Larger size, higher power consumption
- 2) Technology based on MOS field effect transistor
  - a) Fewer devices needed to form a storage element
  - b) Smaller size, lower power consumption
  - c) Simpler processing, lower cost
  - d) Slower switching speed (for devices now available)
- 3) Charge coupled devices
  - a) Derived from MOS technology. Very simple storage element structure
  - b) Operates as a dynamic shift register
  - c) Capable of high bit rates, 10 megabits per second or more
  - d) Data must be circulated and regenerated
- 4) MNOS (Metal Nitride Oxide Silicon) transistor
  - a) Storage element can be formed with only one device, by utilizing its hysteresis operating characteristics
  - b) High density. Potential of one million bits per square inch or more
  - c) Non-volatile. Potential of long retention time of one year or more
  - d) Long write time (for devices now available)
  - e) Similar to MOS, can utilize processes developed for MOS

Work is also being carried out in a number of other variations.

Considerable further effort is still required: to improve and assure the yield of the chips; to perfect the mounting, bonding and interconnection of the chips; to effectively and efficiently package the memory elements and supporting circuitry; and to quantize and characterize their reliability and environmental capabilities. At the same time, a non-volatile semiconductor memory with fast read-write capability, which can survive a power down condition is still much desired and not yet available. The pace at which semiconductor memory will be used in airborne computers will depend to a large extent on its success and growth in commercial applications which

represent a larger market force. However, its wide usage can be expected by the late 1970's. CMOS with its good combination of high density, high speed and very low power consumption can emerge as the dominant high speed read-write memory. MNOS or a variation: MAOS (Metal Alumina Oxide Silicon), with an even higher density, an even lower power dissipation but a substantially lower writing speed, may become the choice for read mostly memory or electrically alterable read only memory.

Semiconductor memory is not the only technology currently under development. A number of other technologies are being worked on. These include the following mass memory approaches:

- 1) Magnetic bubble domain memory
  - a) Utilization of cylindrical domain formed in an orthoferrite or garnet plate under the influence of a transversely applied magnetic field as storage element.
  - b) High storage density — greater than  $10^6$  bits per square inch.
  - c) Large capacity capability — with low volume, weight and power consumption. One conceptual design of a  $10^8$ -bit mass storage system yields a volume of 520 cu. in., weight of 27.4 pounds and power consumption of 22.2 watts. These numbers can further decrease.
  - d) NDRO, non-volatile.
  - e) Capability to perform logical functions — on-chip decoding, signal processing.
  - f) Basically serial in operation.
  - g) Potential solid state replacement for tapes, discs, drums.
- 2) Optical beam accessed memory
  - a) Use of optical material as storage medium, and laser beam as means for reading or writing
  - b) Potential of very high density —  $10^7$  bits per square inch or more
  - c) Potential utilization of holographic techniques to improve signal to noise ratio and reduce the penalty of imperfect alignment
- 3) Ferroacoustic memory
  - a) Use of magneto-restrictive magnetic film on glass or wire substrate as storage medium. Writing accomplished by coincident application of acoustic wave along the substrate and current pulse through a write-sense conductor. Reading by sensing the voltage pulse induced by the acoustic wave.

- b) Synchronous high data rate serial operation.
- c) NDRO, non-volatile.

## EVOLUTION IN COMPUTER DESIGN

In addition to the evolution in hardware, there are also a number of evolving trends in airborne computer design. These developments are stimulated by user requirements, availability of newer technology and the accumulated experience of the designers. These developments are not necessarily without controversy. The direction and rates of evolution are not always uniformly persistent. However, the general trends are clearly discernible.

- 1) Trend towards increased processing capability
  - a) General use of parallel rather than serial operation
  - b) Use of overlap operations
  - c) Use of sophisticated indexing and addressing techniques
  - d) Increasing memory size to accommodate increasing utilization of computer. A current airborne computer typically offers a basic capacity of at least 4,000 words. 32,000 words or more are not uncommon.
  - e) Richer instruction repertoire to increase the performance of a computer. A current computer has a basic instruction set of from 30 to over 100.
  - f) Microprogramming increasingly provided to accommodate functional improvements, design changes and different operational modes.
- 2) Trend towards general purpose capability
  - a) Development of "family" of airborne computers, providing wide spectrum of capability and using common basic design. This approach facilitates accommodation of individual requirement without sacrificing process learning which benefits reliability, cost and efficient use of computer.
  - b) Use of computer modules such as CPU modules, memory modules, power supply modules, from which new members of the "family" can be constructed.
  - c) Affiliation of airborne computers with commercial computers to take advantage of commonality in components and software. In such a case, the instruction set of the airborne computer is generally a subset of the commercial computer's.
  - d) Standardization of word lengths. 16- and 32-bit lengths are increasingly being

adopted, with the former used for simpler applications and the latter for more elaborate applications.

- 3) Trend towards easier use
  - a) All current airborne computers are provided with assemblers and diagnostic programs. Increasingly, they are also being provided with compilers and simulators — operable on commercial computers.
  - b) Sharing of software by computers in a family.
  - c) Use of higher order language (HOL) to reduce software effort and provide better control.
  - d) Floating point provision increasingly available to ease programming and program validation.
- 4) Trend towards greater flexibility in computer organization to take advantage of new hardware and software concepts
  - a) Judicious use of Read Only Memory, Read Mostly Memory, Block Oriented Random Access Memory and Mass Memory to optimize computer design.
  - b) Use of multiprocessor and multicomputer configurations to satisfy a system requirement.
  - c) Use of parallel processor for the processing of radar and acoustic signals, the correlation of multisensors, and pattern recognition.
  - d) Greater emphasis on the design of optimized input/output subsystem, power supply and interconnections.
  - e) Integration of logic and memory functions where advantageous.
- 5) The trend towards greater application of fault tolerant computer design is stimulated by the desire to:
  - a) Increase the computer reliability
  - b) Increase its operating life
  - c) Assure proper operation during a critical time period
  - d) Avoid maintenance during a given time span
  - e) Provide graceful degradation
  - f) Avoid single point failures.

The penalty for incorporating this feature is decreasing as the computer state-of-art advances.

The early fault tolerant computers made use of masking approaches such as component redundancy, modular redundancy and computer redundancy. More recent designs also make use of error detecting — error correcting codes and self-repairing approaches. In the latter, a computer is partitioned into a number of functional modules, each provided with one or more unpowered spares. A control unit is used to detect the presence of a fault and carry out the recovery operation. A transient fault is corrected by repetition of the computation. A permanent fault is corrected by the replacement of the faulty module with a spare. The control unit, being the hard core of the system, is protected by redundancy, majority voting and spares.

The optimum fault tolerant configuration for a specific application can be determined only through a pertinent tradeoff, and can be a combination of several approaches. However, with pre-planning, standard modules and circuits can be designed and then utilized to make up different configurations to satisfy different applications. This concept is illustrated in Figure 12. By varying the numbers of the functional units and the fault detecting, code translating and power switching circuits in the control unit, different fault tolerant configurations can be realized.

#### BROADENED USAGE OF AIRBORNE COMPUTER

With the increasing capability and decreasing size, power consumption and cost of the future airborne computer, its broadened utilization can be anticipated. Listed below are several illustrations. The degree to which any such approach can be beneficial to a given application, of course, should be determined by specific tradeoffs.

- 1) Increased usage of computing approaches that will result in better system performance and/or more effective programming.
  - a) Use of rigorous rather than expansion equations for greater flexibility to accommodate changes and refinements.
  - b) Use of individually optimized equations for each type of weapon or sensor in vehicles equipped with multiple weapons or sensors.
  - c) Use of more powerful estimation methods.
  - d) Use of table lookups, or table lookups in combination with interpolations.
- 2) Increased usage of computer to aid or enhance the sensors
  - a) Digital processing of sensor data
  - b) Digital control of sensors
  - c) Computer compensation for individual sensors and/or installations
  - d) Use of simple sensors with computer performing the transformation of sensor data

into coordinates, scales and formats required for computation.

- e) Use of nonlinear and non-explicit sensors
  - f) Use of multisensors with multispectral coverage, and use of computer to process and correlate their outputs.
- 3) Increased usage of an independent I/O processor, to simplify programming of main computations, to provide better performance or to improve dynamic response.
  - 4) Increased usage of computer to aid and enhance system control and stabilization
    - a) Use of simple control mechanisms with computer providing the necessary transfer functions and coordinate transformations.
    - b) Minimization of the use of electromechanical mechanisms.
    - c) Freedom to use dynamically unstable configurations, with versatile digital filtering in the computer providing the stabilizing transfer functions.
  - 5) Increased usage of computer to monitor the overall system performance
    - a) Use of computer to monitor the performance of other equipment on the vehicle.
    - b) Use of computer to assess the probability of mission success.
    - c) Storage of data for post flight analysis.
    - d) Use of computer to suggest attractive alternate targets/missions, based on current inputs and its estimation of the probability of success of the original mission.
    - e) Storage of data for maintenance analysis.
  - 6) Increased usage of computer to enhance the overall system performance
    - a) Computer controlled flight for RPV and manned aircraft.
    - b) Computer derived information base regarding own position, weather, target, environment, etc., generated from preset data, sensor input, and real-time data link communication with ground stations, satellites, other aircraft.
    - c) Computer organized situation displays.
    - d) Computer controlled weapon delivery and electronic warfare.
    - e) Computer controlled evasive and emergency maneuvers.
    - f) Automated reporting and record keeping.
    - g) Computer integrated avionics system.

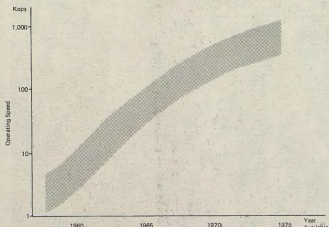


Figure 1. Trend of Airborne Computer Operating Speed

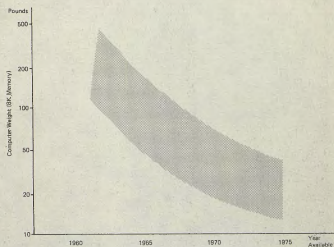


Figure 2. Trend of Airborne Computer Weight (Normalized to 8K Memory)

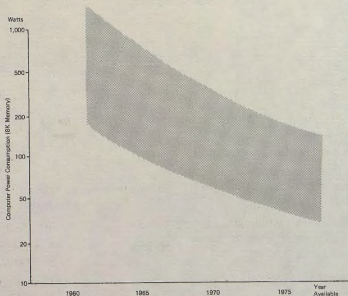


Figure 3. Trend of Airborne Computer Power Consumption (Normalized to 8K Memory)



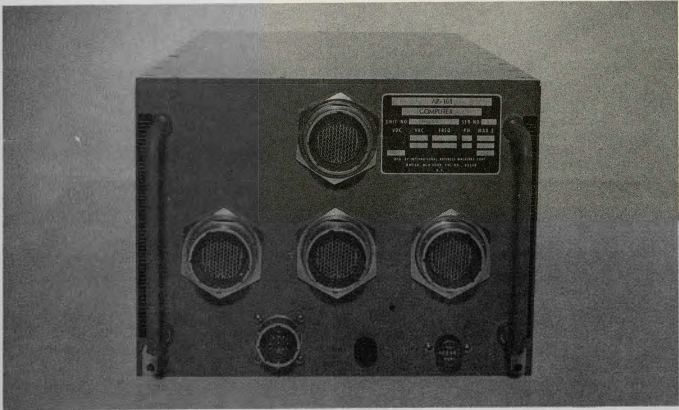


Figure 4. AP-101 General Purpose Airborne Computer

Type:	General-purpose, parallel, micro-programmed		
Organization:	Binary, fractional. Fixed and floating point		
Word Length:	32 bits, full word; 16 bits, half word.		
Storage Type:	900 nanosec. core with storage protection. Can be provided with plated wire memory	Dimensions:	7.62 inches x 10.12 inches x 19.56 inches (Standard ATR)
Storage Size:	Up to 65,536 half words internal, addressing to 524,288 half words	Volume:	1508 cu. in.
Throughput:	550 KOPS	Weight:	48 pounds (with 65,536 half words storage)
Average Execution Times:	1.65 $\mu$ s add, 5.45 $\mu$ s multiply, 8.65 $\mu$ s divide	Power:	340 watts (with 65,536 half words storage)
Instruction Set:	117	Built-In Test:	Greater than 95% detection of failures

Figure 5. Functional Design Characteristics of AP-101

Figure 6. Physical Characteristics of AP-101

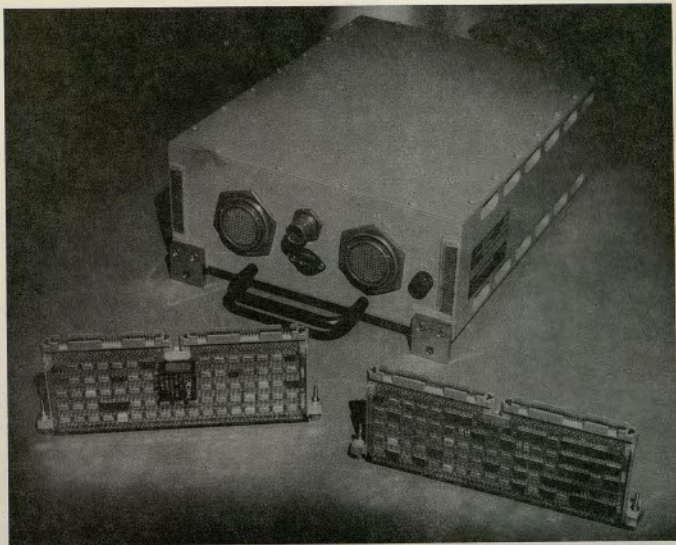


Figure 7. SP-1 Airborne Subsystem Processor

Type:	General-purpose, stored program, parallel
Organization:	Binary, fractional, fixed point
Word Length:	16 bits, instructions; 16 and 32 bits, data
Storage Type:	1.33 $\mu$ s core
Storage Size:	4,000 to 16,000 16-bit words
Throughput:	350 KOPS
Average Execution Times:	2.7 $\mu$ s add, 5.7 $\mu$ s multiply, 8.0 $\mu$ s divide
Instruction Set:	41

Figure 8. Functional Design Characteristics of SP-1

	Including Power Supply and Structure, With 4000 Words Memory	Without Power Supply and Structure, With 4000 Words Memory
Dimensions:	4.1 inches $\times$ 10.1 inches $\times$ 13.6 inches	3.6 inches $\times$ 8.8 inches $\times$ 3.1 inches
Volume:	560 cubic inches	100 cubic inches
Weight:	18.1 pounds	3.6 pounds
Power:	72 watts	52 watts

Figure 9. Physical Characteristics of SP-1

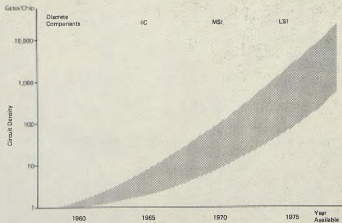


Figure 10. Trend of Circuit Density Used in Airborne Computer

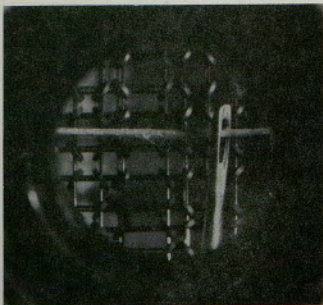


Figure 11. Core Memory Array

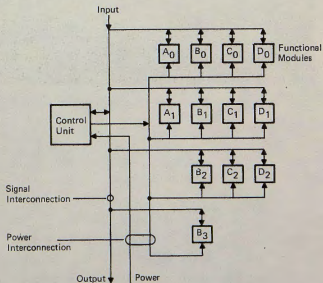


Figure 12. Fault Tolerant Computer