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1.0 Introduction

Advances in microelectronics technologies over the past several decades have truly revolutionized modern society in almost every aspect of human endeavor. The continuous scaling of the commercial semiconductor technology to smaller and smaller device and interconnect feature sizes (referred to as Mooreís Law due to Gordon Moore of Intel) has lead to more and more functionality being developed onto a single silicon ëchipí. Moreover, the manufacturing cost of an on-chip function is getting cheaper and cheaper. These two factors: ëmore for lessí represents the fuel that has propelled the microelectronics technology revolution of the 20th century. How long will this technology revolution last into the new millennium is a key question that the semiconductor industry is continuously evaluating. An excellent roadmap of the commercial semiconductor technology needs for the next 15 years (from 1997 to 2012) is described in The National Technology Roadmap for Semiconductors, published by the Semiconductor Industry Association (SIA) in December 1997 [1].

However, due to the extreme radiation and environmental conditions in space, the commercial semiconductor technology is not readily applicable to spaceborne applications. The challenge then remains how to infuse into spaceborne applications the commercially driven semiconductor revolution that has been so pervasive on ground. Since space microelectronics, and especially radiation-hard microelectronics represents a very small (read insignificant) fraction of the total world semiconductor output, it is essential for space microelectronics technology to heavily leverage and incrementally build upon the commercial technology. Two questions are relevant to the proposed transfer of commercial semiconductor technology to space:

- Can research and development of advanced space microelectronics technologies benefit the commercial semiconductor industry?
- Is there a space microelectronics technology roadmap that can address spaceborne systems with minimum change to the commercial semiconductor roadmap?

In this paper we make an initial attempt to address these two questions. In Section 2, we propose a vision for highly intelligent autonomous micro-spacecraft systems as a grand challenge for future deep-space micro-robotic scientific exploration. These systems require:

- On-board sensing, processing and storage capabilities;
- Autonomous control, navigation, planning;
- Low-power consumption microelectronics devices and architectures;
- Highly miniaturized for light-weight and extremely small volumes;
- Reliable over large temperature ranges and radiation conditions;
- Tolerate (operate through) failures and survive 10 or more years in operation;
- Adapt and reconfigure in the presence of unexpected conditions as well as scientific opportunities;
- Self asses its state of health, and request assistance only when necessary, etc.

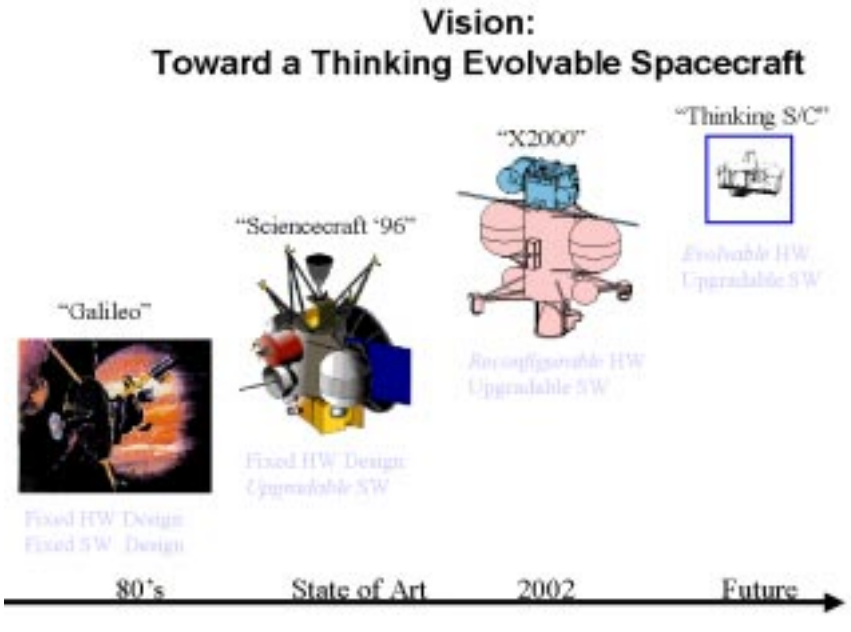
In essence, most of the above described characteristics of future deep-space Microsystems are consistent with the technology needs of current and future highly portable computation and communication devices. Examples include portable electronics, mobile cellular devices, hand-held personal digital assistants, etc.

In Section 3, we focus on integrated micro-avionics systems that subsume all the space-craft electronics as well as opto-electronics devices into a single architecture. An instance of this architecture using distributed computing is described in Section 4, followed by a discussion of commercial off-the-shelf technology microprocessor selection for space in Section 5. In Section 6 we propose a technology-scaling concept leading towards complete Systems On A Chip (SOAC). In Section 7 we offer our concluding remarks. The concepts described in this paper are currently being applied as part of the newly formed NASA Advanced Deep Space Systems Development Program (also known as X2000), and implemented by the Center for Integrated Space Microsystems (CISM) at the Jet Propulsion Laboratory.

2.0 A Vision of Future Spacecraft Microsystems

A vision of future highly miniaturized, autonomous, and intelligent space micro-systems is illustrated in Figure 1 below, in four steps. The first concept illustrates the highly successful Galileo spacecraft that was launched in 1989 to explore Jupiter and its surrounding moons. Soon after it was launched, Galileo experienced a major failure in the high-gain antenna crip-pling the spacecraft and jeopardizing the whole mission. However, after extensive and very costly software reprogramming of the complete computer system that enabled more on-board data analysis, data compression, and data processing, Galileo made a series of spectacular discoveries including liquid ocean beneath the icy crust of Europa (one of Jupiterís moon). In this case, the software reprogramming was very costly as well as time consuming.

The next concept labeled Sciencecraft shows a miniaturized spacecraft designed around a specific science instrument, with a modular software architecture that allows continuous software upgrading as part of the mission design and not only in response to failures or anoma-lies. A ten-year mission to Pluto would plan a continuous and seamless upgrade of software modules during the long cruise to the outer solar system.

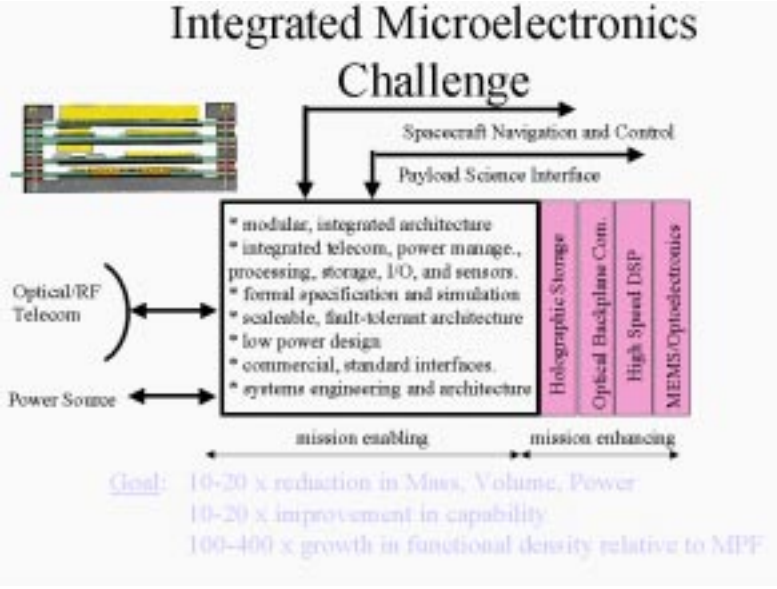


To take this the next logical step, consider the concept behind the X2000 Sciencecraft, which contains both reprogrammable hardware as well as upgradable software. In this concept, hardware reconfigurable elements such as Field Programmable Gate Arrays (FPGAs) and Reprogrammable Switches, enable the spacecraft electronics to assume different configurations during different mission phases, as well as due to failures or unforeseen targets of opportunities. Consider the electronics to consist of a ëvolumeí of highly integrated reconfigurable and reprogrammable devices. New hardware configurations can be sent to the sciencecraft, in support of specific functions that the system needs to perform efficiently.

Finally, the concept of highly intelligent ëthinkingí sciencecraft implies that the system can autonomously self-evaluate its state of health or performance, determine the desirable state of health or performance, and then either reconfigure to a known target state, or evolve over time towards the target state. This evolution could be a long-term effort on behalf of the sciencecraft to achieve its programmed goal in the presence of changing on-board resources (due to failures or resource conflicts), and due to changes in environmental conditions (temperature, radiation). Examples of highly intelligent and autonomous Microsystems include planetary micro-explorers; micro-rovers cooperating on the surface of a planet searching for scientific discoveries; penetrators or submarines in search of biological evidence, etc.

3.0 Integrated Spacecraft Micro-Avionics System

The concept of an integrated microspacecraft avionics system implies that all of the system electronics is designed as part of the same integrated architecture, in contrast to separately designed sub-systems that are then connected together. This approach is characteristic of highly integrated and miniaturized commercial systems such as hand-held devices or portable systems. The same model applies to miniaturized space computer systems. In the concept depicted in the figure below, all of the spacecraft electronics for command and data handling, attitude control and navigation, power management and distribution, science data storage and processing, telecommunication, as well as interfaces to payload, are designed as a single system. Typically, these are all separate sub-systems. Conceptually, one only needs external connections to a power source, a communication physical device (radio antenna or optical device), and any special devices that can not be integrated into the microelectronics system.



Also shown in the figure is an approach for integrating all of the electronics into a single 3D stack of modules (or slices), much like a loaf of bread. To further facility technology transfer to space applications, the spacecraft consists of a mission enabling part, and a mission enhancing part. The mission enhancing elements are high-risk high-payoff technologies that are not critical to the mission, but which could enhance the mission if successful. We have listed only some of the technologies currently under consideration: Holographic Storage, Optical Backplanes, High-Speed Digital Signal Processors and Neural Networks, MEMS and Optoelectronic Devices, etc.

4.0 Distributed Fault Tolerant Computing Architecture

In more traditional spacecraft systems of the 80s and 90s, long-term system reliability was achieved using a ëdual-stringí approach to redundancy. That is, each sub-system typically consisted of a primary unit and a backup. The backup was used in case the primary failed. For highly miniaturized sub-system-less architectures the redundancy approach needs to be revisited as a means of achieving the desired system level reliability. In Figure 3, we show a distributed computer architecture with multiple computer nodes interconnected via a reliable and redundant computer network. The number of nodes or the interconnect architecture are both scaleable depending on the level of system reliability required, and depending on the mass, volume, and power constraints. Figure 3 depicts the current architecture of the X2000 Program First Delivery spacecraft system that will be delivered in October 2000. The following features are of interest:

- Each computer node in this architecture can be a ëmasterí and control all of the space craft devices.
- The system can operate in one of the following modes:

(a) single computer mode for low-power and low-performance with two cold spares in case of failures;

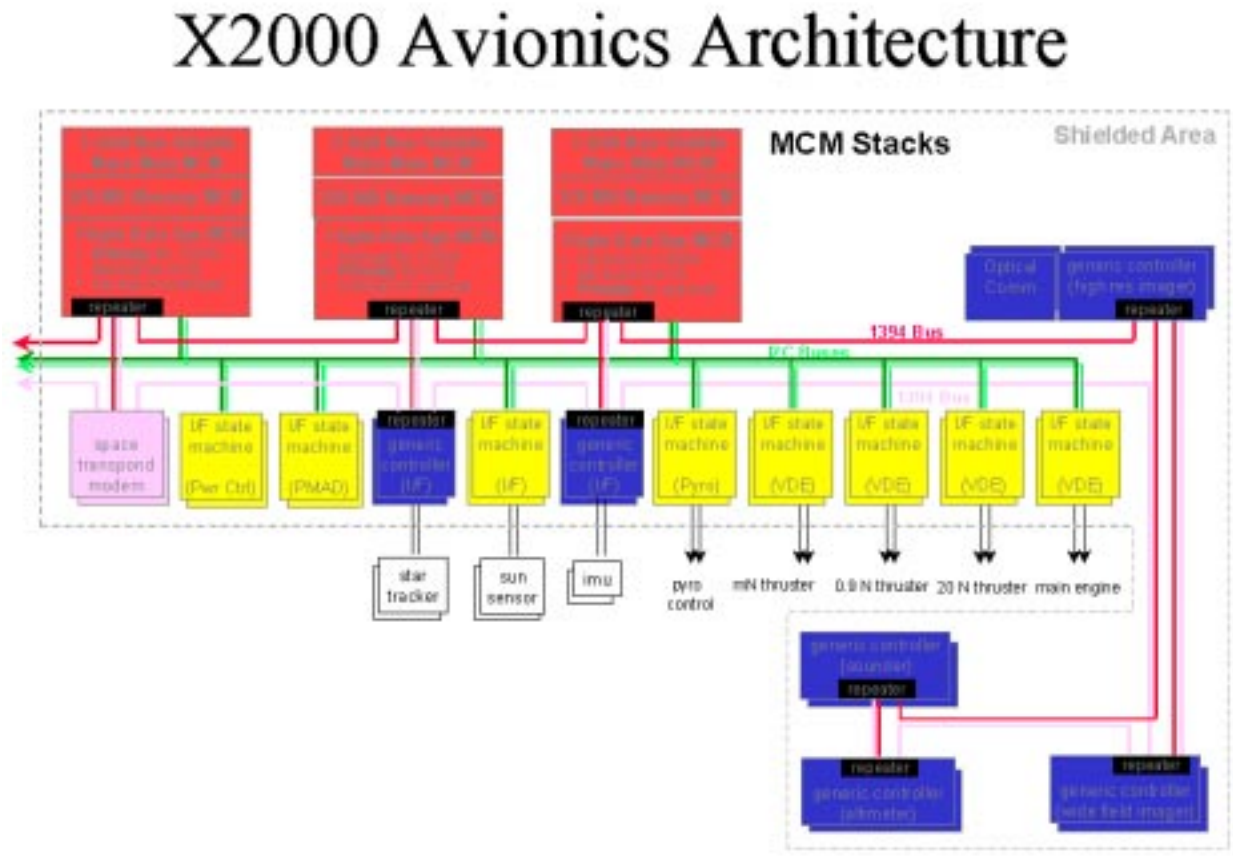
(b) dual-module redundancy for real-time error detection; third node can either be a cold spare, or act as a functional enhancement for higher performance (if the power constraints allow it);

(c) triple modular redundancy for highly reliable computation; if the power constraints are severe and if performance is not a big driver, the clock rate of each node can be reduced to remain within a constant power consumption constraint.

- Each device in the system is an intelligent device with local low-power micro-controller capabilities, local diagnostics, fault isolation and recovery capabilities, and local redundancy.
- The software architecture is based on a message-passing object-oriented distributed architecture where a software module can reside and execute on any of the nodes. Object replication and voting, distributed checkpoint and rollback, and other software implemented fault-tolerance features enable a distributed fault-tolerant system.
- The avionics architecture is based exclusively on standard commercial interfaces such as:

(a) 1394 Firewire local interconnect network operating at a rate of 100 MBPS;
(b) IIC Inter-IC bus for low-rate low-power telemetry;
(c) PCI local bus for connecting high-speed devices to the computer nodes;
(d) 1149.1 IEEE standard JTAG test bus.

- The software architecture is built on top of a commercial operating system such as the VxWorks real-time kernel, as used on the Mars Pathfinder computer, and the programming language is either C, or C++. Recently, support for the programming language Java is being considered due to its wide use by the commercial industry.



5.0 Leveraging Commercial Off-The-Shelf Technology

The most obvious example for the space microelectronics industry to leverage on-going developments in the commercial industry is in the area of microprocessors. Developing a new instruction set architecture (ISA) is extremely complex, requires years of development and fine-tuning, as well as large resources in software development and support tools (compilers, debuggers, operating systems, etc.) Building upon existing commercial microprocessors is thus essential for the space microelectronics community. Which microprocessor, then, should the space-community consider for their applications? Let us first consider some data from the commercial embedded computing as well as workstation-based microprocessor market.

Recent data published by the Microprocessor Report [4] shows the total volume of sales in both the embedded and workstation-based microprocessor systems markets. The following observations are of interest. First the volume of embedded processors is significantly larger than the workstation market (180 million versus 80 million for all of the year 1997). Second, the workstation market is dominated by PCs, due to the sluggish sales of the Macintosh computers. In the embedded market the big players include: Motorola 68000 series, MIPS, SuperH, and the ARM micro-controllers followed by i960 and x86 micro-controllers. To use one of these micro-processors or micro-controllers in space, one has to purchase the Intellectual Property (IP) or license, and transfer the core design to a radiation hard foundry. This process may take 2-3 years, by which time the selected processor is no longer current. In the worst case it may not even be supported with commercial software tools and support equipment hardware.

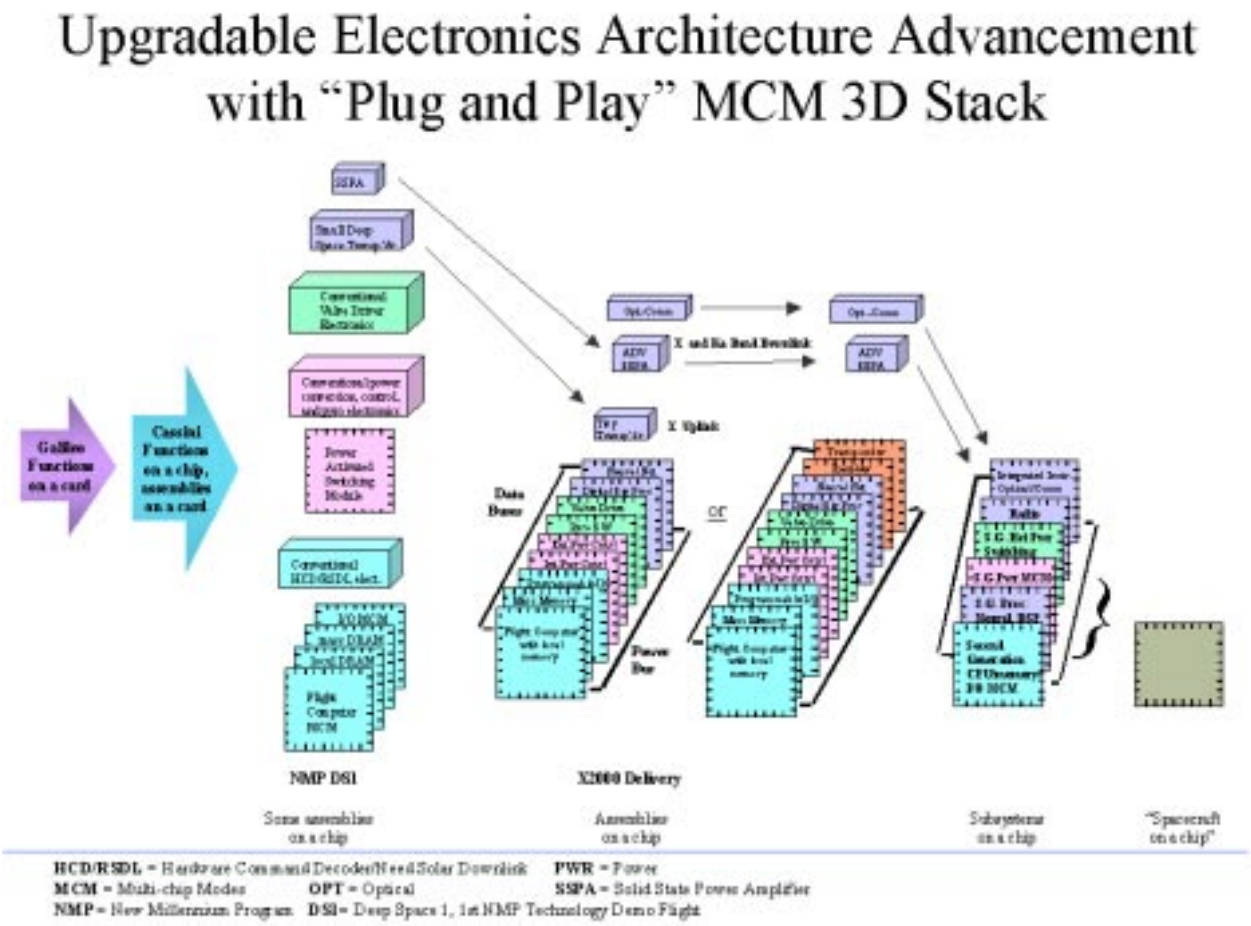
Therefore, there is a built-in risk factor that has to be considered with any commercial processor selection. Picking a long-term partnership with a commercial vendor is essential; however, it is very difficult to achieve due to the low volume of production. Since developing a custom microprocessor for space is out of the question, the space community will have to learn to work with the commercial sector and manage the risk accordingly.

6.0 Towards Avionics Systems on a Chip

The commercial semiconductor technology roadmap as described by the Semiconductor Industry Association [1] envisions the continuous technology scaling of silicon based Complementary Metal Oxide Semiconductor (CMOS) devices unimpeded by physical limitations for the following 15 years. With a new generation of lithography technology introduced every 3 years and the number of devices on a single chip increasing exponentially, future chips will integrate todayís single-board systems or even larger complete systems, onto a single chip. Moreover, higher levels of integration will introduce new directions for technology scaling. That is, more of the system will be integrated onto a single chip as a means of improving performance, rather than improving the performance of any single functional unit. Consider the capability of placing onto a single chip not only logic, but, lots of local memory, power management components, mixed signal technology, high-frequency telecommunications elements, sensor technology, and so on. The challenge now becomes system integration and test, as well as design synthesis and system verification. Future spacecraft Microsystems technologies are particularly enabled by the use of Systems On A Chip (SOAC). This technology promises dramatic reductions in systems mass, volume, and power, while still increasing system functionality, and improving system reliability. In the figure below, we depict a system technology scaling roadmap that leads towards systems on a chip. Originating from current state of the art where subsystems are typically packaged in boxes that are connected with heavy cables, X2000 is planning to package all microelectronics modules into stackable ëslicesí. These slices can either be arranged into a 3D structure resembling a loaf of bread, or they could be tiled onto a secondary structure (or a combination of the two approaches). With technology scaling, we anticipate fewer slices to be used for the same function, and we anticipate smaller formats for each slice. Driven only by practical limits, we anticipate each sub-system of today to be designed as individual chips, within the next 10-15 years. These chips will be used either individually or embedded in the structure as part of a spacecraft ëelectronic skiní, or perhaps embedded within an inflatable structure for high-aperture antennas, etc.

Some of the systems on a chip solutions currently under design include:

- Processor In Memory (PIM) which combines logic and DRAM and SRAM devices on a single chip;
- Inertial Reference Systems (IRS) for an integrated micro-gyro and micro-accelerom eter;
- Active Pixel Sensor (APS) and integrated logic, includes sensor technology, logic and mixed signal devices for A/D conversion;
- RF front-end, which combines 3D Micro Electro Mechanical Systems (MEMS) with logic, power electronics and wave-guide technology;
- Opto-Electronics such as Vertical Cavity Surface Emitting Lasers (VCSELs), and logic.
- Neural Network analog circuits with sensor technology for distributed smart sensing.



All of the above listed systems on a chip technologies, when integrated together, will result in a very powerful microspacecraft system that will be highly miniaturized, highly capable, and ultra reliable.

7.0 Conclusions

In this paper we described at the conceptual level, a space microelectronics and microsystems technology vision and roadmap into the new millennium. Starting with a vision of highly integrated, autonomous, and intelligent microsystems, we introduced the concept of a sub-system-less and seamless integrated electronics system, a distributed reliable architecture for highly reliable and long-term survivable missions, a strategy for leveraging the commercial semiconductor revolution, and a technology scaling roadmap leading towards systems on a chip within the next 10-15 years. This vision and roadmap is currently being used by the X2000 Advanced Deep-Space Systems Development Program, and implemented at the Center for Integrated Space Microsystems (CISM), a NASA Center of Excellence at the Jet Propulsion Laboratory [5].

References

[1] The National Technology Roadmap for Semiconductors, SIA, December 1997
[2] NASA Strategic Plan, 1998 NASA Policy Directive, NPD 1000.1
[3] The Space Science Enterprise Strategic Plan Origins, Evolution, and Destiny of the Cosmos and Life, National Aeronautics and Space Administration, November 1997
[4] Microprocessor Report, Volume 12, No. 1, January 26, 1998
[5] See URL: cism.jpl.nasa.gov