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Electrical Characterization and Testing of Microelectronic Materials, Devices, and Circuits

David Kotecki

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Principal Investigator: Kotecki, David E.
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Title:
Electrical Characterization and Testing of Microelectronic Materials, Devices, and Circuits

Project Participants

Senior Personnel

Name: Kotecki, David
Worked for more than 160 Hours: Yes
Contribution to Project:

Post-doc

Graduate Student

Name: Turner, Steven
Worked for more than 160 Hours: Yes
Contribution to Project:
Steven Turner was supported by this grant during the spring semester of 2002. Steve was involved in the design of high speed digital logic using SiGe technology. Inherent in the design process was integrated test sites to determine the performance of the logic. This work formed the seed for a current project supported by DOD on high speed digital design using InP technology. Steve is currently a PhD candidate in the electrical engineering program at UMaine.

Name: Yang, Fan
Worked for more than 160 Hours: Yes
Contribution to Project:
Fan Yang was a graduate research assistant supported by this grant for two years. His research involved the investigation of electrical transport in microelectronic capacitors fabricated using HfO2 dielectrics. His research on electrical characterization of HfO2 dielectrics formed the basis of his MS thesis in electrical engineering, resulted in two publications, and accounted for most of the research conducted under this grant. Fan is current a PhD candidate in electrical engineering at University of Buffalo.

Name: Tonti, Janelle
Worked for more than 160 Hours: Yes
Contribution to Project:
Janelle Tonti was a graduate research assistant supported by this grant for one semester. Her resarch involved the design and characterization of high-speed serializers and deserializers. The results of her work during the Fall semester of 2003 resulted in a follow-on grant through the Maine Technology Institute and formed the foundation of her research resulting in a M.S. degree in electrical engineering expected in December 2004.

Undergraduate Student

Name: Cote, Crystal
Worked for more than 160 Hours: Yes
Contribution to Project:
Crystal Cote was employed as an undergraduate researcher. Her primary responsibility was in the development of LabView software for controlling instrumentation for performing temperature dependent I-V and C-V measurements.

Name: Reblin, Jason
Worked for more than 160 Hours: Yes
Contribution to Project:
Jason Reblin was employed as an undergraduate researcher. His primary responsibility was in the development of LabView software for controlling instrumentation for performing precise DC mosfet characterization.

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Name: Carr, Crystal

Worked for more than 160 Hours: Yes

Contribution to Project:

Crystal was involved with the design and testing of high-speed digital logic circuits. Here work was supported in part by this grant and in part by the NSF-REU program at the University of Maine and was performed during the Summer of 2002. Crystal is currently a NSF GK-12 Fellow pursuing a M.S. degree in Electrical Engineering

Years of schooling completed: Junior

Home Institution: Same as Research Site

Home Institution if Other:

Home Institution Highest Degree Granted(in fields supported by NSF): Doctoral Degree

Fiscal year(s) REU Participant supported: 2002

REU Funding: REU site award

Name: Traxlier, Alexander

Worked for more than 160 Hours: Yes

Contribution to Project:

Ms. Traxlier spent the Summer of 2002 working on the DC characterization of CMOS devices using equipment supported from this grant. She was supported in part by this grant and in part by the NSF-REU at UMaine.

Years of schooling completed: Freshman

Home Institution: Same as Research Site

Home Institution if Other:

Home Institution Highest Degree Granted(in fields supported by NSF): Doctoral Degree

Fiscal year(s) REU Participant supported: 2002

REU Funding: REU site award

Name: Yu, Piu

Worked for more than 160 Hours: Yes

Contribution to Project:

Piu Lam Yu was employed during the summer of 2001 and supported in part by this grant and in part by a NSF-REU program at UMaine. He was involved with the testing of a custom-designed integrated circuit which contained digital control logic.

Years of schooling completed: Freshman

Home Institution: Other than Research Site

Home Institution if Other: New Jersey Institute of Technology

Home Institution Highest Degree Granted(in fields supported by NSF): Doctoral Degree

Fiscal year(s) REU Participant supported: 2001

REU Funding: REU site award

Name: Pierce, Kyle

Worked for more than 160 Hours: Yes

Contribution to Project:

Kyle Pierce was employed during th summer of 2001 as supported in part by this grant and in part by a NSF-REU program at UMaine. He was involved with the testing of a custom-designed phase locked loop freuency synthesizer.

Years of schooling completed: Sophomore

Home Institution: Other than Research Site

Home Institution if Other: Rose-Hulman

Home Institution Highest Degree Granted(in fields supported by NSF): Bachelor's Degree
Fiscal year(s) REU Participant supported: 2001
REU Funding: REU site award

Organizational Partners

Other Collaborators or Contacts

Equipment provided by this grant has been used by other researchers at the University of Maine to support their research efforts. These collaborations have included work conduced by Prof. Rosemary Smith on capacitor sensors and Prof. Mauricio Pereira da Cunha on dielectric characterization of new materials.

Activities and Findings

Research and Education Activities:

The goals of this project were to provide 1) infrastructure needed to establish the foundation of a microelectronics test laboratory for wafer level testing and materials characterization 2) investigate the electrical transport properties of HfO2 dielectrics as a function of temperature.

Findings:

The funding provided by this grant allowed the establishment of the Microelectronics Test and Characterization Laboratory within the electrical engineering department at the University of Maine. Equipment in this laboratory include a temeprature controlled Cascade Microtech microprobe station capable of probing 30x30 micron test sites on a substrate over the temperature range of -60 to 200C; two Keithly Instruments Source Measurement Units capable of performing precise DC characterization of materials and devices; a 500MHz bandwidth digital oscilloscope and 200MHz digital logic analyzer; varous DC power supplies; digital voltage meters; a precision nanovolt meter; and a picoamp meter. This equipment has been used for materials characterizaiton; integrated circuit testing; and device characterization.

The primary finding from our research on HfO2 dielectrics include the characterization of electron transport in sputtered HfO2 dielectrics using Pt electrodes as a function of temperature resulting in a model of electron transport in HfO2 dielectrics. These finding are provided later on in the form of a MS thesis from Mr. Fan Yang, a graduate research assistant supported by this project.

Training and Development:

This project supported six undergraduate students. Four were employed to assist in the testing of materials and integrated circuits and became familiar with the procedures involved in electrical testing. Two of the students were primary involved with the development of LabView software used to control instrumentation and developed software modules used to perform CV, IV, It, and Cf measurements as a function of temperature.

Outreach Activities:

Journal Publications

Fan Yang, D.E. Kotecki, G. Berhnardt, M.Call, "Electrical and Structural Characterization of HfO2 MIM Capacitors", Proc. of the Mater. Res. Soc.,, p. 203, vol. 745, (2003). Published

Fan Yang and D.E. Kotecki, "Leakage Behavior of HfO2 Thin Films in MIM Structures", J. Vac. Sci. and Technology A, p. , vol. , (2004). Submitted

Books or Other One-time Publications

Fan Yang , "Characterization of HfO2 Capacitors ", (2004). Thesis, Published
Bibliography: M.S. Thesis; Department of Electrical and Computer Engineering, University of Maine, 2004

Web/Internet Site

Other Specific Products

Contributions

Contributions within Discipline:

The major conclusion from the research on electron transport in HfO2 was a model which describes electron transport as a function of temperature. The model indicates that electron transport at temperatures below 50C can be described by a hopping mechanism where carriers are transported through the dielectric due to crystalline defects and electronic states produced by impurities; at high temperatures (100-200C), the transport is dominated by thermal emission over the Schottky barrier at the electrode/dielectric interface.

Contributions to Other Disciplines:

Contributions to Human Resource Development:

This project supported nine students over the past three years. This resulted in one student (Fan Yang) receiving his MS degree in electrical engineering based on the research conducted as part of this project. Two other students (Steven Turner and Janelle Tonti) were able to start new resarch efforts which have led to additional funding through other sources.

Contributions to Resources for Research and Education:

This grant established the 'Microelectronics Testing and Characterization Laboratory' in the Department of Electrical and Computer Engineering at the University of Maine. This laboratory continues to function and has susported activities in the testing of high speed circuits; testing of analog amplifiers; and materials characterization.

Contributions Beyond Science and Engineering:

Categories for which nothing is reported:

Organizational Partners

Activities and Findings: Any Outreach Activities

Any Web/Internet Site

Any Product

Contributions: To Any Other Disciplines

Contributions: To Any Beyond Science and Engineering

CHARACTERIZATION OF HFO_2 CAPACITORS

By

Fan Yang

B.S. Northern Jiaotong University, 1999

A THESIS

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

(in Electrical Engineering)

The Graduate School

The University of Maine

December, 2003

Advisory Committee:

David E. Kotecki, Associate Professor of Electrical and Computer Engineering, Advisor

John F. Vetelino, Professor of Electrical and Computer Engineering

Robert Lad, Professor of Physics

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CHARACTERIZATION OF HFO_2 CAPACITORS

By Fan Yang

Thesis Advisor: Dr. David E. Kotecki

An Abstract of the Thesis Presented
in Partial Fulfillment of the Requirements for the
Degree of Master of Science
(in Electrical Engineering)
December, 2003

Hafnium oxide (HfO_2) is a promising dielectric for future microelectronic applications. HfO_2 thin films (10-75nm) were deposited on Pt/SiO_2/Si substrates by pulsed DC magnetron reactive sputtering. Top electrodes of Pt were formed by e-beam evaporation through an aperture mask on the samples to create MIM (Metal-Insulator-Metal) capacitors. Various processing conditions (Ar/O_2 ratio, DC power and deposition rate) and post-deposition annealing conditions (time and temperature) were investigated. The structure of the HfO_2 films was characterized by X-ray diffraction (XRD) and the roughness was measured by a profilometer. The electrical properties were characterized in terms of their relative permittivity (ϵ_r(T) and ϵ_r(f)) and leakage behavior (I-V, I-T and I-time). The electrical measurements were performed over a temperature range from -5 to 200^{o}C. For the samples with best experimental results, the relative permittivity of HfO_2 was found to be ~ 27 after anneal and increased by $0.027\%/^o$C with increasing temperature over the measured temperature range. At 25^oC, leakage current density was below 10^{-8} A/cm^2 at 1 volt. The leakage current increased with temperature above a specific threshold temperature below which the leakage current didn't change much. The leakage current increased with voltage. At voltages below 1volt, it's ohmic; at higher voltages, it follows Schottky model. The breakdown field is $\sim 1.82\times10^6$ V/cm. The optical bandgap was measured with samples deposited on quartz substrates to be 5.4eV after anneal.

ACKNOWLEDGMENTS

This work has partially been supported by National Science Foundation under contract NSF-EPS-0082973.

I am deeply grateful to Professor David E. Kotecki, my academic advisor, for his valuable direction, support and advice. I also want to thank Professor Robert Lad and Professor John Vetelino for their advice for my thesis.

I would like to thank R. Laibowitz of IBM for providing the $Pt/SiO_2/Si$ samples. I would also like to express my gratitude to Dr. George Bernhardt and Dr. Michael Call from the Laboratory for Surface Science and Technology, who helped me with the deposition work and taught me the operation of many devices.

Finally, I would like to thank my wife for her love and support.

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CHAPTER 1

INTRODUCTION

1.1 Background

Silicon dioxide has been used as the primary gate dielectric material in Si MOS (Metal-Oxide-Semiconductior) transistors since 1957, when the usefulness of the Si/SiO_2 material system was first demonstrated. Since the first MOS device, the fundamental device structure and materials have not changed much even though the size of the transistors has been reduced. In the area of Very Large Scale Integration (VLSI), the size of the MOS transistor has been continually reduced and the density of CMOS (Complementary MOS) circuits has increased by a factor of 2 every 3 years [1].

Figure 1.1 shows the device minimum feature size generated from the 1994, 1997, 1998/99 and 2001 International Technology Roadmap for Semiconductors (ITRS) [2]. The minimum feature size is expected to continue to be reduced for the next 10 years and an acceleration in the feature size is evident. Figure 1.2 depicts the Intel's Lithography Roadmap, which shows the trend in the minimum feature size over the past 30 years and the predicted future.

The ever-increasing trend towards smaller device sizes and higher integration density requires the scaling of many device parameters. In particular, in Si MOS devices, the thickness of the gate insulator must decrease as the lateral dimensions are reduced. This is true for both constant field scaling originally proposed by Dennard [3] and generalized scaling proposed by Baccarani [4]. It is very difficult to obtain oxides thinner than $\sim$0.8-1.0nm corresponding to the thickness of a native oxide. At such thicknesses, neither the controllability nor the reliability can be guaranteed. Another fundamental limit to the scaling of the gate dielectric thicknesses is the exponential increase in tunnelling current with decreasing oxide thickness. For the $polySi/SiO_2/Si$ system with

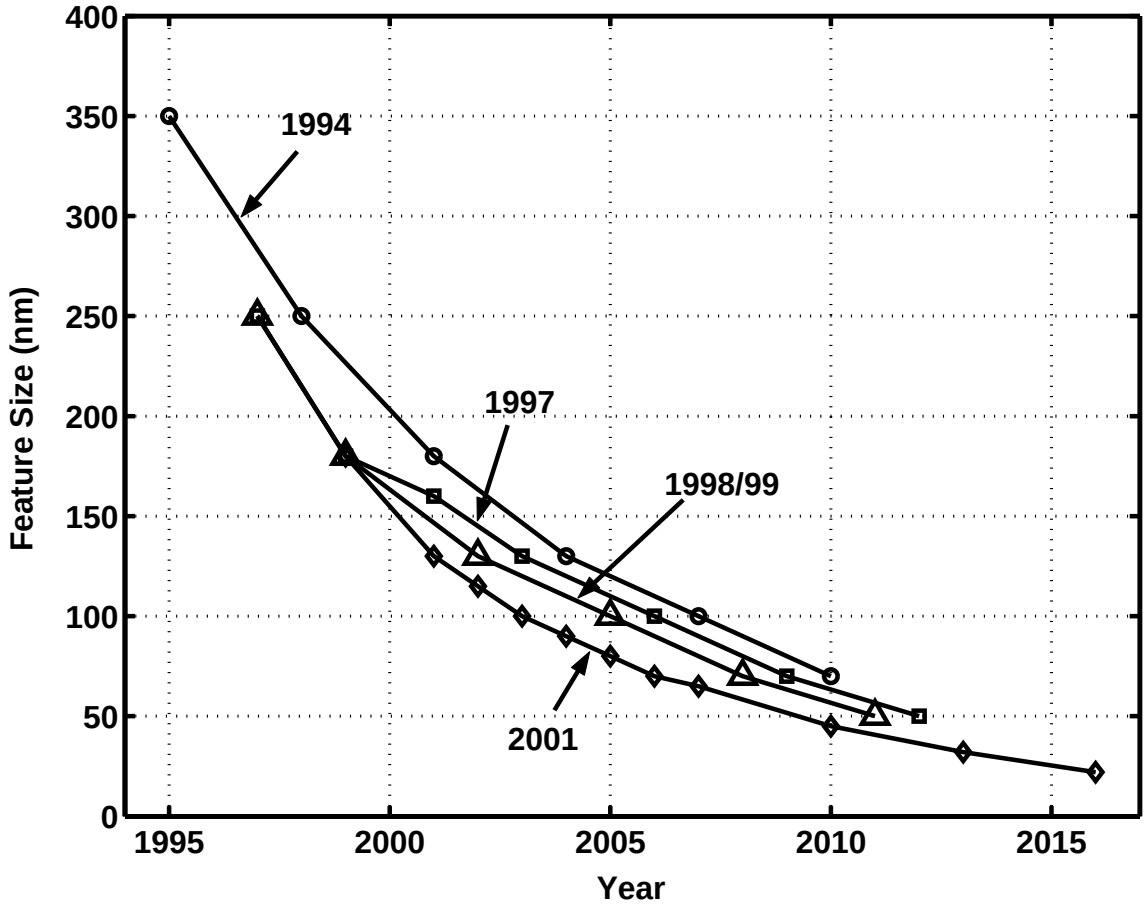


Figure 1.1: Technology node trends for ITRS Roadmap

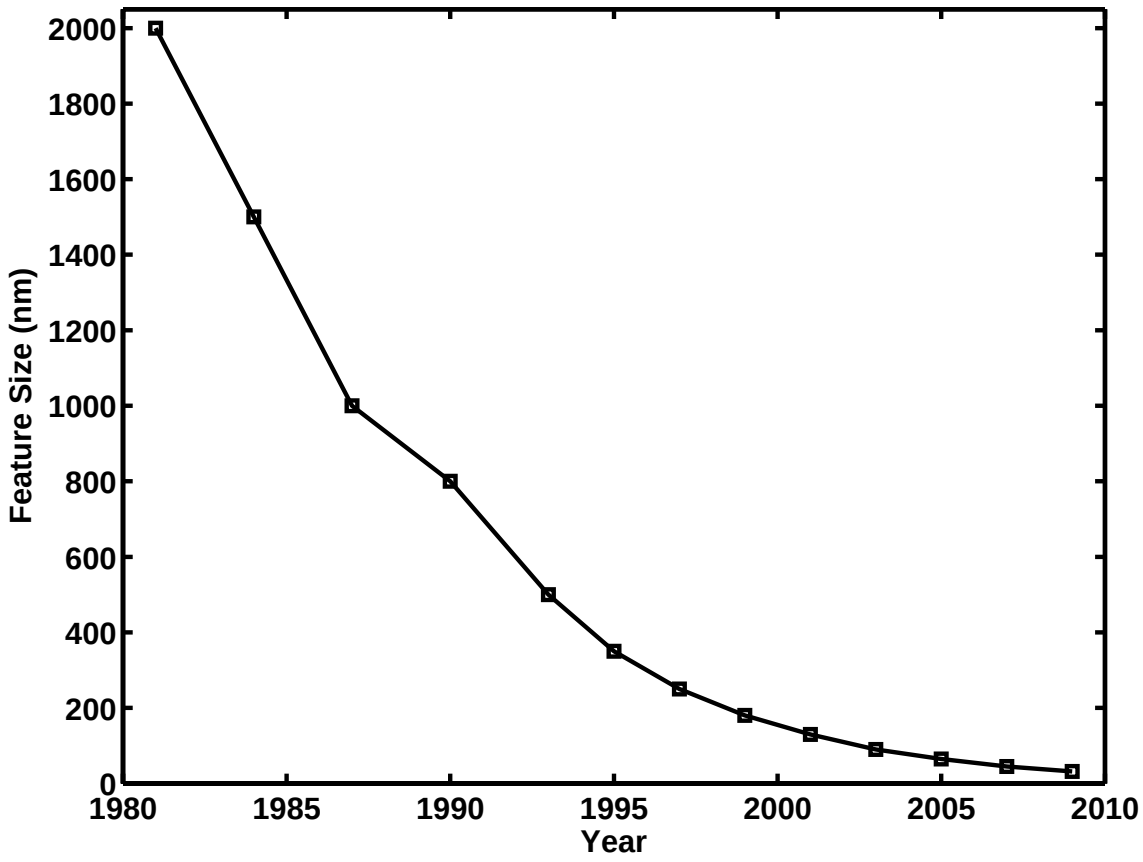


Figure 1.2: Technology node trends for Intel Lithography Roadmap

a gate bias of $\sim$ 1V, the leakage current increases from $\sim 10^{-6}$A/cm^2 for a 3nm thick SiO_2 layer to ~ 10A/cm^2 for a 1.5nm thick SiO_2 layer: seven orders of magnitude in increased current for a thickness change of only a factor of 2. A high gate leakage current can alter the device performance and increase the standby power consumption.

Reducing the gate leakage current is an important reason for searching for alternatives for SiO_2-based gate dielectrics. Another limitation for thin oxides might stem from their reduced lifetime. The lifetime estimations for thin SiO_2 gate oxides lead to the conclusion that a 1.5nm thick oxide cannot meet the 10-year requirement lifetime at any bias. Oxide reliability thus remains one of the major issues in CMOS scaling. It's another driving force towards replacing SiO_2 by high-K dielectrics. Because of these limitations, the semiconductor industry has been investigating alternatives to the Si/SiO_2 system. Table 1.1 shows the timeline for the recent and anticipated future requirements for the equivalent SiO_2 gate oxide thickness, the electrical requirements of the oxide and the experimental results of leakage current density at the gate bias in the appropriate technology generations. Preliminary analysis indicates that, balancing the gate leakage control requirements against performance requirements, high-K materials may be required for the gate dielectric by around the year 2005 [6].

The gate capacitance of a CMOS device is given by

$$C = \frac{\epsilon_0 \epsilon_r A}{d}, \tag{1.1}$$

where ϵ_0 is the permittivity in vacuum ($\epsilon_0 = 8.85418 \times 10^{-14}$F/cm), ϵ_r is the relative permittivity of the dielectric material, A is the area of the capacitor (gate length$\times$gate width) and d is the thickness of the dielectric film. The gate capacitance is proportional to the dielectric constant, the length and width of the gate, and inversely proportional to the thickness of the gate dielectric material.

To reduce the leakage current while maintaining the same gate capacitance, a thicker dielectric film with a higher dielectric constant is required. But not all materials

Production Year	Technology Node(nm)	Gate dielectric(SiO_2 equivalent)thickness for high performance(Å)	Gate bias V_{dd}(V)	Leakage current(A/cm^2)
2001	130	13-16	1.1	> 0.1
2002	115	12-16	1.0	> 0.1
2003	100	11-16	1.0	> 0.1
2004	90	9-14	1.0	> 1
2005	80	8-13	0.9	> 2
2006	70	7-12	0.9	> 5
2007	65	6-11	0.7	> 10
2010	45	5-8	0.6	> 100
2013	32	4-6	0.5	
2016	22	4-5	0.4	

Table 1.1: Gate dielectric requirements for future technologies (according to the ITRS Roadmap 2001)

with higher dielectric constant than SiO_2 are acceptable as a gate dielectric material in Si based MOS devices.

The gate leakage current is exponentially dependent on the dielectric layer thickness, while the capacitance is only linearly dependent on the thickness. Short-channel performance degradation, which is caused by the fringing field from the gate to the Source/Drain (S/D) region, depends on the gate dielectric thickness-to-length aspect ratio. Therefore, materials with a too high dielectric constant create additional problems. A desirable alternative gate dielectric material should have a dielectric constant 4-10 times higher than SiO_2, which is 3.9. That is, the alternative material should have a dielectric constant between 15 and 40. The use of such high-K dielectric materials would provide the equivalent oxide thicknesses (EOT) required to maintain current drive, while maintaining acceptably low tunneling current. EOT refers to the thickness of any dielectric scaled by the ratio of its dielectric constant to that of SiO_2 (K_{SiO_2}) such that:

$$EOT = d \cdot (\frac{K_{SiO_2}}{K_x}) = d \cdot (\frac{3.9}{K_x}), \tag{1.2}$$

where d is the physical thickness of the dielectric, and K_x is the dielectric constant of the alternative dielectric.

At first glance, this would seem to be a winning proposal, since a substantial reduction in the current should be possible with only small increase in dielectric thickness. For a large number of dielectrics, however, the gate current is also exponentially dependent upon the barrier height between the electrode and the conduction band of the insulator and between the conduction band of the insulator and the substrate. Therefore, not only is a material with higher dielectric constant is required, but this material must also have a suitable barrier height on both sides to keep the leakage current within reasonable limits.

However, physical thickness and interfacial band alignment are only two factors that affect device performance. Other limitations on the material choice come from stability issues. Alternative gate dielectrics have to be compatible with a CMOS process flow. That poses severe restrictions on the material due to post-growth processing steps (thermal stability and manufacturability). The high-K dielectric would be most likely deposited on a Si channel. Therefore, it should not show any tendency to form a silicide, silicon dioxide, or the mixtures of those by any of the following reactions:

$$\begin{aligned} Si + MO_x &\longrightarrow M + SiO_2 \\ &\longrightarrow MSi_2 + SiO_2 \\ &\longrightarrow M + MSi_xO_y, \end{aligned} \tag{1.3}$$

where M represents a metallic element.

Thermodynamic stability considerations (to avoid the reactions in Eq.(1.3)) reduce the number of possible candidates significantly. In addition, all radioactive oxides and oxides not solid at 1000K are not suitable. Figure 1.3 shows an overview of all existing binary oxides [7, 8]. Only the oxides of the elements in the shaded squares are capable

for use for gate insulators; other elements can be eliminated from further consideration due to the reasons given above.

In recent years, many high-K dielectric materials have been suggested as replacement candidates for silicon dioxide and silicon nitride gate dielectrics, such as Ta_2O_5, TiO_2, Y_2O_3, CeO_2, Al_2O_3, Pr_2O_3, $SrTiO_3$, $BaSrTiO_3$(BSTO), ZrO_2 and HfO_2. Unfortunately, many of them have drawbacks. Ta_2O_5 requires TiN electrode [9] and has very high leakage current on Si [10]; TiO_2 has poor band alignment with silicon. Ta_2O_5, TiO_2, $SrTiO_3$ and $BaSrTiO_3$ are thermally unstable when directly contacted with silicon [11]. The formation of SiO_2 and/or metal silicide often occurs when these materials are deposited on silicon. Further growth of silicon dioxide or a silicide takes place during subsequent annealing, which is usually found to be necessary to reduce leakage currents. An underlying SiO_2 layer reduces the effectiveness of any high-K material, since SiO_2 has a lower dielectric constant and thus reduces the effective capacitance of the dielectric film. For example, to obtain an EOT of 1.5nm one could use a 11.54nm thick film with a K=30. The presence of an 1nm interfacial SiO_2 layer would reduce this thickness down to 3.85nm. For the same required EOT, the physical thickness of the high-K material decreases due to interfacial layers, thus the leakage current through the film increases substantially. Although an additional barrier layer can be added to solve this problem, it will add process complexity and impose thickness scaling limitations. Some ferroelectric materials such as BSTO ($K>200$) have too high dielectric constant, which may cause fringing field induced barrier lowering effect as mentioned above. Materials having relatively low dielectric constant such as Al_2O_3 (K=12) and Y_2O_3 (K=14) do not provide sufficient advantages over SiO_2 or Si_3N_4.

Among the materials with medium dielectric constant and good compatibility with silicon, ZrO_2 and HfO_2 are attracting much attention. Hf forms the most stable oxide with the highest heat of formation (ΔHf=271Kcal/mol) among the elements in group IVA of the periodic table (Ti,Zr,Hf). Hf can also reduce the native SiO_2 layer

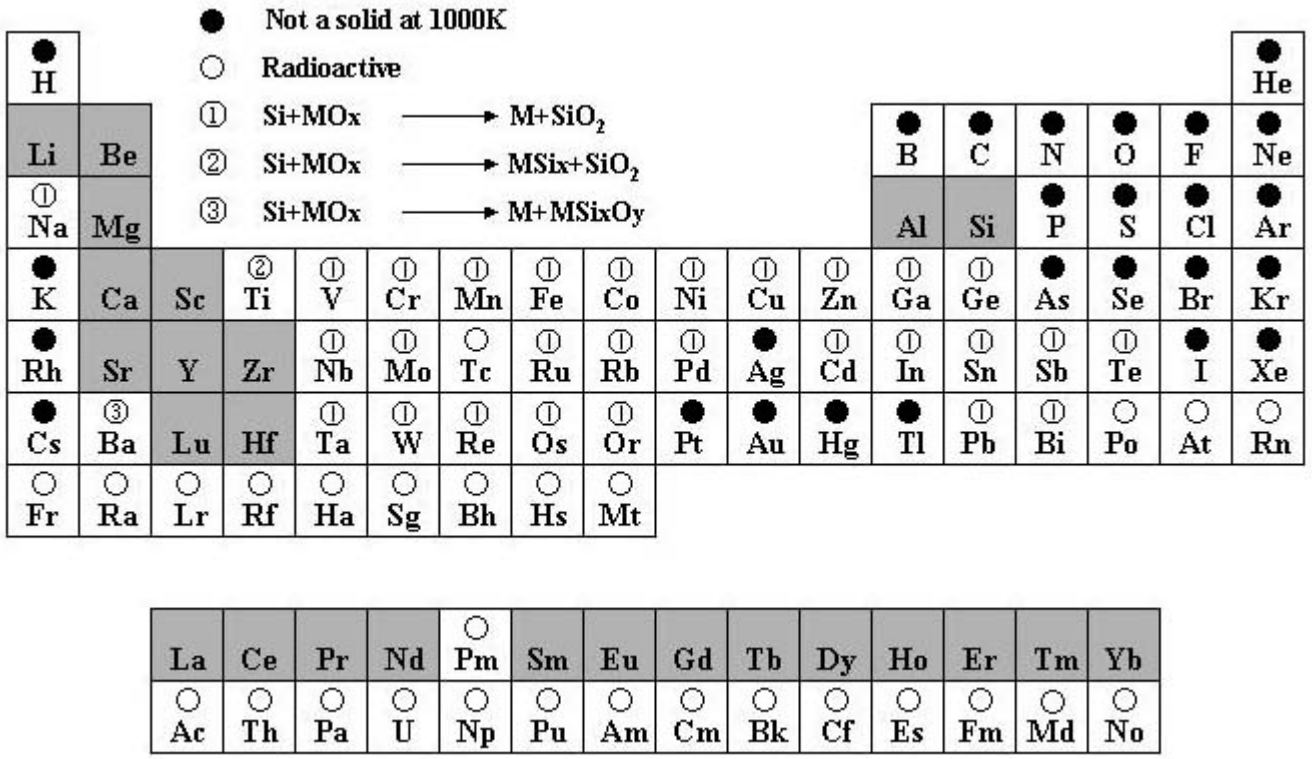


Figure 1.3: Overview of all existing binary oxides

to form HfO_2. Unlike other silicides, the silicide of Hf can be easily oxidized to form HfO_2. The oxidization of $ZrSi_2$ forms SiO_2, but the oxidization of $HfSi_2$ forms HfO_2. HfO_2 is very resistive to impurity diffusion and intermixing at the interface because of its high density (9.68g/cm^3). In addition, HfO_2 is compatible with n^+ polysilicon gate without any barrier materials. These properties make HfO_2 one of the most promising candidates for alternative gate dielectric application [12, 13, 14, 15].

HfO_2 can also be used in optical coatings and optoelectronic devices. It's a very commonly used material for optical coatings because of its hardness and good transparency in the visible and ultraviolet ranges of the spectrum. Its large transparent range is from the UV to the IR (0.22-12μm) [16]. The ease of evaporation adds to its popularity [17].

1.2 Purpose of the Research

The goal of the thesis is to investigate the physical and dielectric properties of HfO_2 thin films deposited by pulsed DC magnetron reactive sputtering in the MIM (Metal-Insulator-Metal) structure. Different deposition conditions were investigated and the relationship between the deposition condition and electrical properties were investigated.

1.3 Thesis Organization

This thesis investigated the effects of deposition conditions and measurement environments on the physical and dielectric properties of HfO_2 thin films in MIM (deposited on Pt/SiO_2/Si substrates) and MIS (deposited on SiO_2/Si substrates) structures, and built models for the capacitance and leakage current.

Chapter 2 describes the experiment methods including the deposition protocols, deposition condition matrix, measurement environments and devices used in the experiments.

Chapter 3 discusses in detail the measurement results of HfO_2 in MIM structure and analyzes the data to acquire the properties of HfO_2 films.

Chapter 4 describes the models for the capacitance and the leakage currents of HfO_2 capacitors based on the experiment data.

Finally, Chapter 5 draws the conclusions from the experiment data and indicates the tasks for future work.

CHAPTER 2

EXPERIMENT PROCEDURE

This chapter provides an overview of the experiment procedure, including the deposition method and the electrical and physical characterization techniques.

2.1 Deposition Method

The HfO_2 thin films were deposited by pulsed DC magnetron reactive sputtering using a Hf target. The deposition system is at the Laboratory for Surface Science and Technology (LASST) [18]. The target was 99.9% pure Hf excluding Zr which was present at 2.24%. Other contaminants such as H, Mg, Al, Si, Ti, V, Cr, Mn, Co, Ni, Cu, Nb, Mo, Sn, Ta, W, and Pb were less than 100ppm, except for Fe, which was present at 245ppm [19]. The magnetron was pulsed at a rate of 20KHz with a 50% duty cycle. The deposition rate of HfO_2 was measured at different O_2/Ar ratios with a DC power of 100 and 300 Watts (keeping the total flow rate and pressure the same) using an in-situ quartz crystal microbalance (QCM) placed at the same location as the substrate.

The deposition rates varied from 0.6 to 8.4nm/min at a power of 100W and from 1.8 to 27nm/min at a power of 300W as the $\%O_2$ was changed. Hysteresis was observed when increasing and then decreasing the $\%O_2$ in the chamber as shown in Figure 2.1. As the O_2/Ar ratio was increased, the deposition rate remained at a high level until the ratio reached a specific value, and then the rate decreased sharply to a low level and remained there. Then if the O_2/Ar ratio was decreased, the rate remained at the low level until the ratio reached a much lower value, and then the rate went back to the high level. The hysteresis is probably due to a poisoning of the Hf target with O_2 causing the formation of a thin layer of HfO_2 on the surface of the target at high O_2 partial pressure.

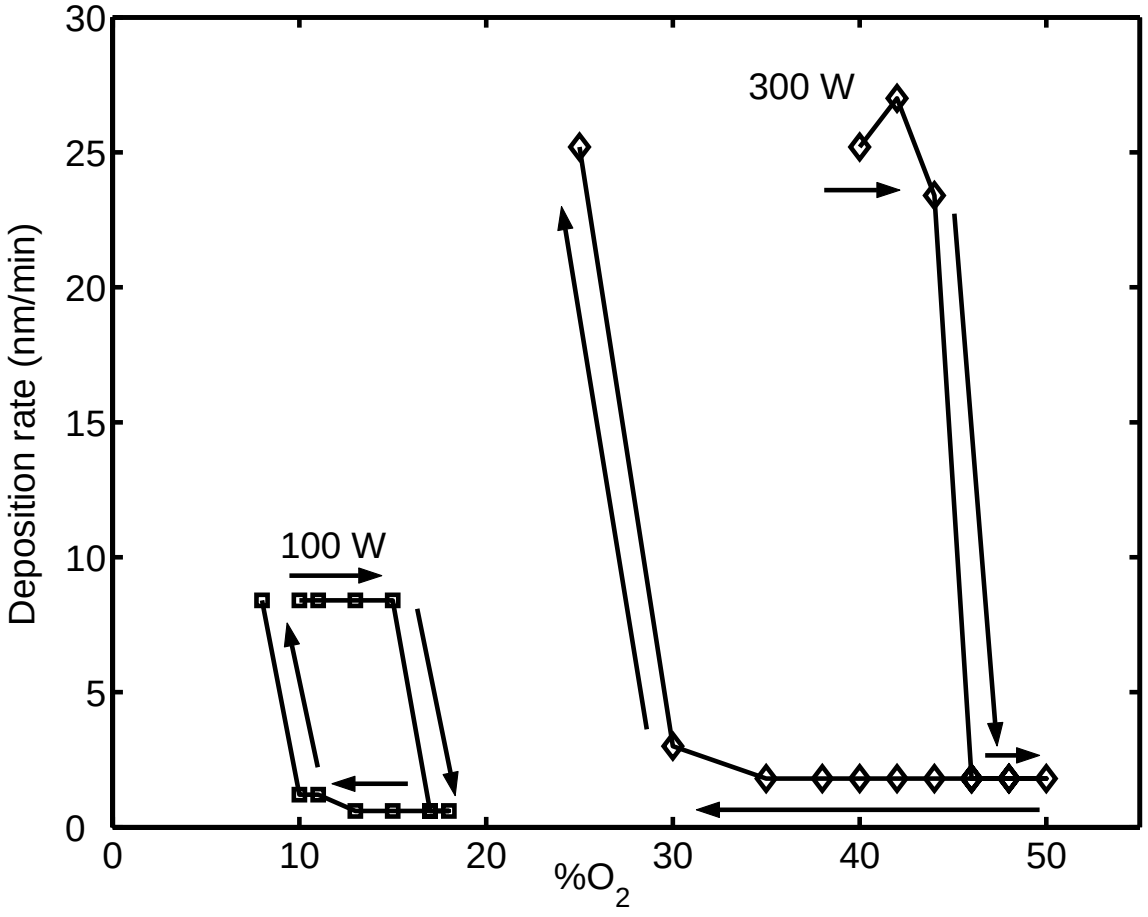


Figure 2.1: Deposition rate as a function of the percent of O_2 in the flow

2.2 Deposition Protocol for MIM Capacitors

The MIM capacitors were investigated first, using Pt coated SiO_2/Si substrates and Pt top electrodes. One advantage of the MIM structure is that there are no interfacial oxide effects at the dielectric electrode interface allowing an understanding of transport properties of the HfO_2 dielectrics.

A deposition protocol was determined after the deposition rates for the HfO_2 were measured and the Pt/SiO_2/Si substrates were investigated by X-ray diffraction(XRD) as a function of annealing temperature.

The deposition protocol used for the MIM capacitor formation is shown in Figure 2.2. The Pt/SiO_2/Si substrates were first annealed for one hour at a temperature of 700^{o}C in air to stabilize the substrate. Figure 2.3 shows the XRD spectra of the substrate as a function of anneal temperature. After the 700^{o}C anneal, the Pt changes from a mixed (110) and (111) orientation to a predominantly (111) orientation. The properties of the substrates should not change much during the HfO_2 deposition and post-deposition annealing. Thus any changes in permittivity and leakage current which are observed after the anneal are attributed to the result of the changes in the properties of HfO_2 thin films.

2.3 Experiment Procedure

Four deposition conditions were chosen for the deposition of HfO_2 used in the formation of the MIM capacitors; they are listed in Table 2.1. We chose the O_2/Ar ratio so that a high deposition rate and a low deposition rate would occur with the same ratio. Two thickness series were deposited by changing the deposition time, at the same O_2/Ar ratio and the same DC power level, one at high rate and one at low rate. In each series, five samples with the thickness 10, 20, 30, 50 and 75nm were deposited on Pt/SiO_2/Si substrates and one 50nm sample was deposited on a quartz substrate. The

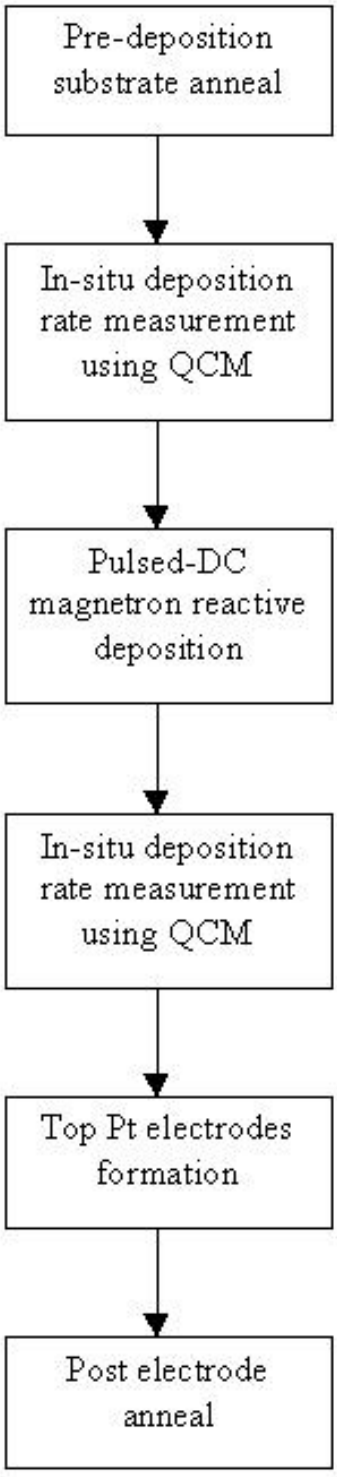


Figure 2.2: HfO_2 Deposition Protocol

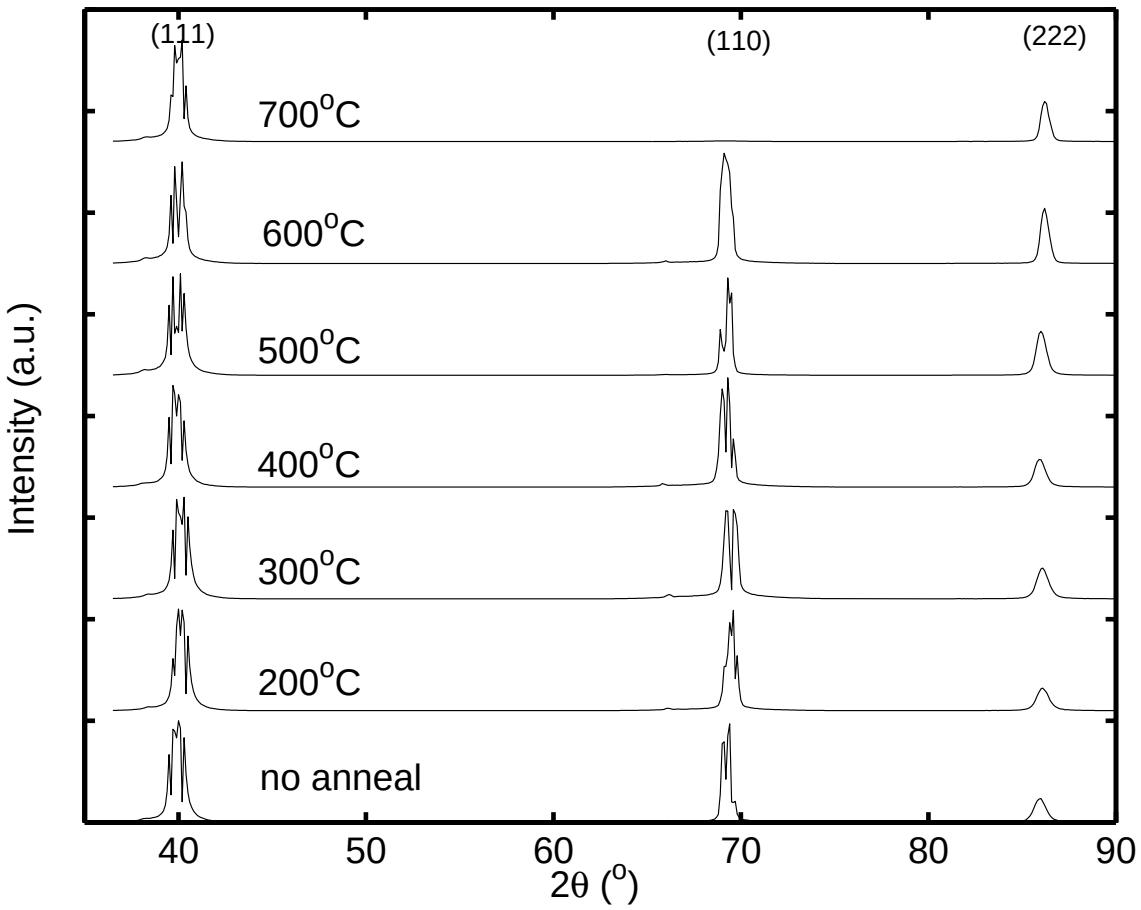


Figure 2.3: XRD data of Pt substrates as a function of annealing temperature

Series	DC Power	Thickness	$\%O_2$	Deposition Rate(nm/min)
A	100W	10,20,30,50,75nm	13	8.4
B	100W	10,20,30,50,75nm	13	0.6
C	300W	10,20,30,50,75nm	40	25.2
D	300W	10,20,30,50,75nm	40	1.8

Table 2.1: Experimental Matrix for MIM structure

deposition rate was measured before and after each deposition by QCM to ensure the deposition rate remained constant during the deposition. The deposition temperature is room temperature.

After deposition, the top Pt electrodes were formed by e-beam evaporation through an aperture mask to create the top electrodes for the MIM capacitors. The aperture mask has many apertures with different sizes. The diameters of the mostly used circular electrodes are $\sim$300, $\sim$115 and $\sim$90 μm. Finally, post-electrode anneal was performed at 600^{o}C for 60 minutes in air. All the measurements were performed before and after post top electrode anneal.

2.4 Measurement Procedure

2.4.1 Physical Measurement Procedure

The roughness of the HfO_2 films and the substrates was measured by a Alpha-Step 500 Tencor profiometer.

The structure of the HfO_2 films and substrates was characterized by X-ray diffraction (XRD) using a Scintag X2 system.

The optical bandgap of the HfO_2 was determined from optical absorption measurements on the 50nm HfO_2 films deposited on the quartz substrates by means of Beckman Diode Array UV-VIS Spectrometer 7400.

2.4.2 Electrical Measurement Procedure

The electrical properties were characterized in terms of their relative permittivity (ϵ_r) as a function of frequency, bias voltage and temperature, and leakage behavior as a function of voltage(I-V), time(I-t) and temperature(I-T).

The electrical measurements were performed over a temperature range from -5 to 200^{o}C and a frequency range from 100 to 1M Hz. The samples were measured on a temperature controllable platform on a Cascade Microtech probe station. The probe station has tiny probes that can contact the small electrodes of the capacitors. The temperature was controlled by a Temptronic thermal controller.

The relative permittivity was also measured under different humidity environment to determine the effect of humidity uptake on electrical measurements.

The capacitance and leakage current were measured using an Agilent 4284A Precision LCR Meter and Keithley Model 236/237 Source-Measure Unit, respectively. The relative permittivity was calculated from the measured capacitance using the relation:

$$\epsilon_r = \frac{C \cdot d}{\epsilon_0 A}, \tag{2.1}$$

which can be derived simply from Eq.1.1.

All the measurements were performed at 25^{o}C unless otherwise specified. The electric measurements for all samples were performed before and after the post electrode anneal.

CHAPTER 3

CHARACTERIZATION OF HFO_2 CAPACITORS

This chapter investigates the physical and electrical characterization of HfO_2 thin films in a MIM structure with Pt electrodes. One advantage of the MIM structure is that there are no interfacial oxide effects at the dielectric interface allowing an understanding of transport properties of the HfO_2 dielectrics.

3.1 Physical Characterization

The roughness was measured for both the HfO_2 films and the Pt/SiO_2/Si substrates. The deposited films have similar roughness to the substrates. Roughness effects are thus not considered when analyzing the electrical data. The mean roughness was in the range of 0.3 to 1nm for the 50nm thick films.

Figure 3.1 shows the the highest peak of the XRD spectrum at 28.3 degrees for the 50nm thick low deposition rate HfO_2 films deposited at a power of 300W as a function of annealing temperature. The XRD results indicate the films are deposited with some crystallinity and have a $(\bar{1}11)$ orientation. The intensity of the $(\bar{1}11)$ peak increase by approximately 25% after a 600^{o}C anneal. No other peaks are observed in the XRD spectrum. The phase of the peak shift to the left after the 500^{o}C and 600^{o}C anneal, which means the film becomes denser. It may be because that the film became more stoichiometric after being annealed in the air. The HfO_2 films deposited at a power of 100W show the similar spectrum.

The optical bandgap was determined for the 50nm HfO_2 films deposited on the quartz substrates. The optical bandgap, E_{opt}, can be derived from the transmission of visible light by the Tauc method [20, 21]. The absorption as a function of frequency $\alpha(\omega)$ is given by

$$\alpha(\omega) = B(\hbar\omega - E_{opt})^2/\hbar\omega \tag{3.1}$$

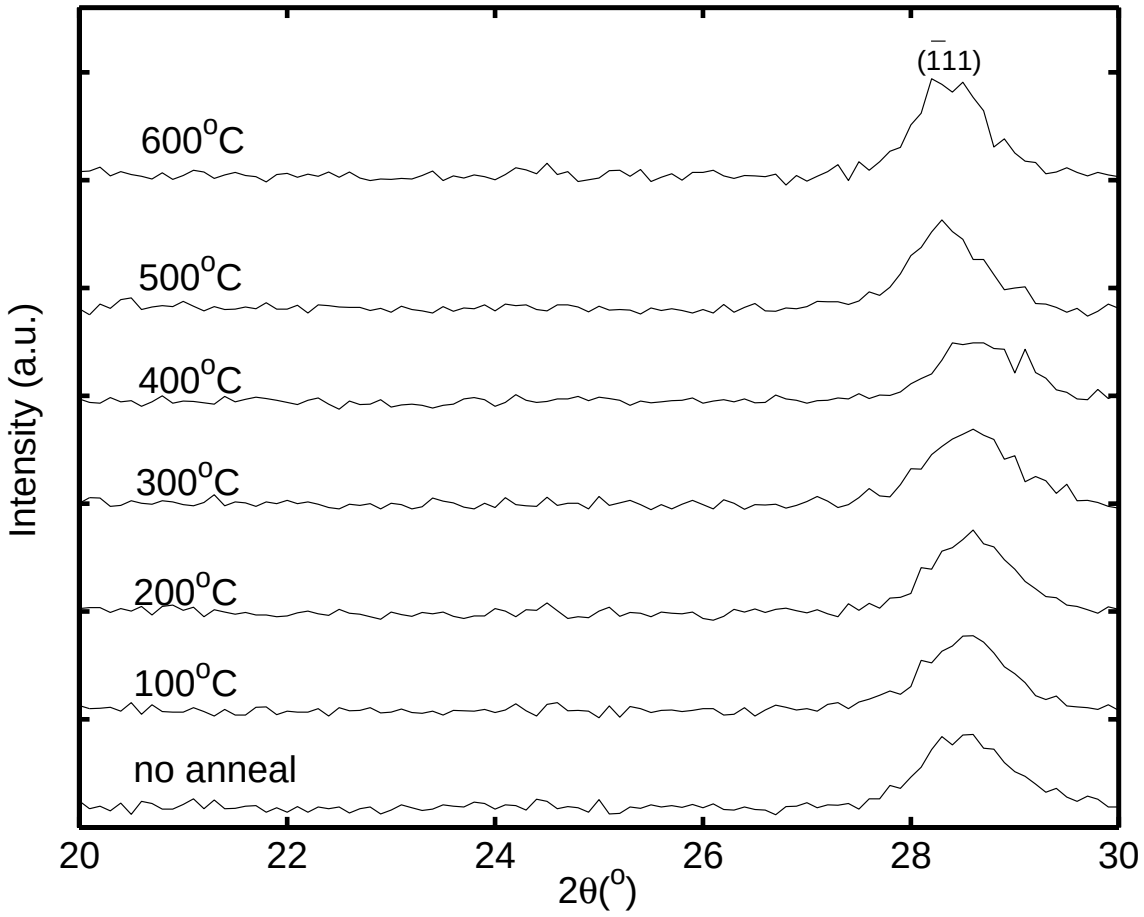


Figure 3.1: XRD data of HfO_2 thin film as a function of annealing temperature

where B is a constant, and $\hbar$, ω and E_{opt} are the reduced Plank constant, angular frequency and optical bandgap respectively. The optical bandgap E_{opt} and B of the film can be determined graphically by extrapolating the linear region of the curves of $(\hbar * \alpha * \omega)^{1/2}$ as a function of $\hbar * \omega$ [20, 21].

Figure 3.2 shows the curves of $(\hbar * \alpha * \omega)^{1/2}$ as a function of $\hbar * \omega$ for the high rate samples and the low rate samples. The circles show the data of the high deposition rate samples (series A and C) and the triangles show the data of the low deposition rate samples (series B and D). The bandgap was calculated to be between 3.8-4.2eV for deposition series A and C and between 5.1-5.5eV for deposition series B and D before the post-deposition anneal. For the samples deposited at low rate, the slope of the linear region is sharper and the bandgap is larger. The reason may be that the Hafnium was not fully oxidized at high rate and thus HfO_x (with $x < 2$) was formed instead of HfO_2. This is consistent with the results of electrical measurements, where the higher relative permittivity and higher leakage currents of series A and C indicate that the Hafnium on these samples was not fully oxidized.

The bandgap is 5.4eV for all samples after the 600^{o}C post-deposition anneal as shown in Figure 3.3. Similar electrical properties were also observed on series A and C samples to series B and D samples after the post-deposition anneal. This indicates that the samples were fully oxidized during the post-deposition anneal in air.

3.2 Electrical Characterization

The electrical properties were characterized in terms of their relative permittivity (ϵ_r), dissipation factor (δ) and leakage (I) behavior. The electrical measurements were performed over a temperature range of -5 to 200^{o}C and a frequency range of 100 to 1M Hz.

The relative permittivity (ϵ_r) and dissipation factor (δ) of every sample were measured before and after anneal. In terms of dissipation, the samples deposited at a

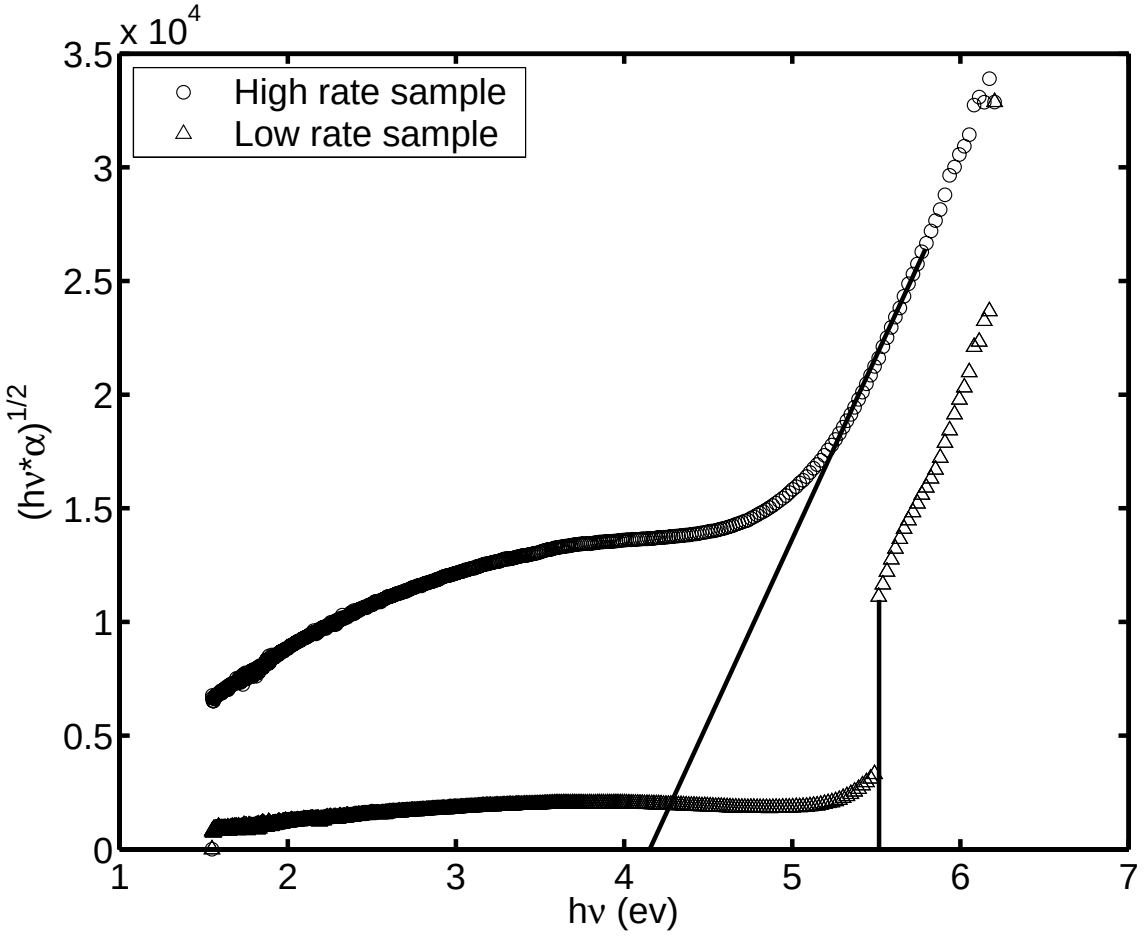


Figure 3.2: $(\hbar * \alpha * \omega)^{1/2}$ as a function of $\hbar * \omega$ for HfO_2 deposited at high deposition rate and low deposition rate before anneal

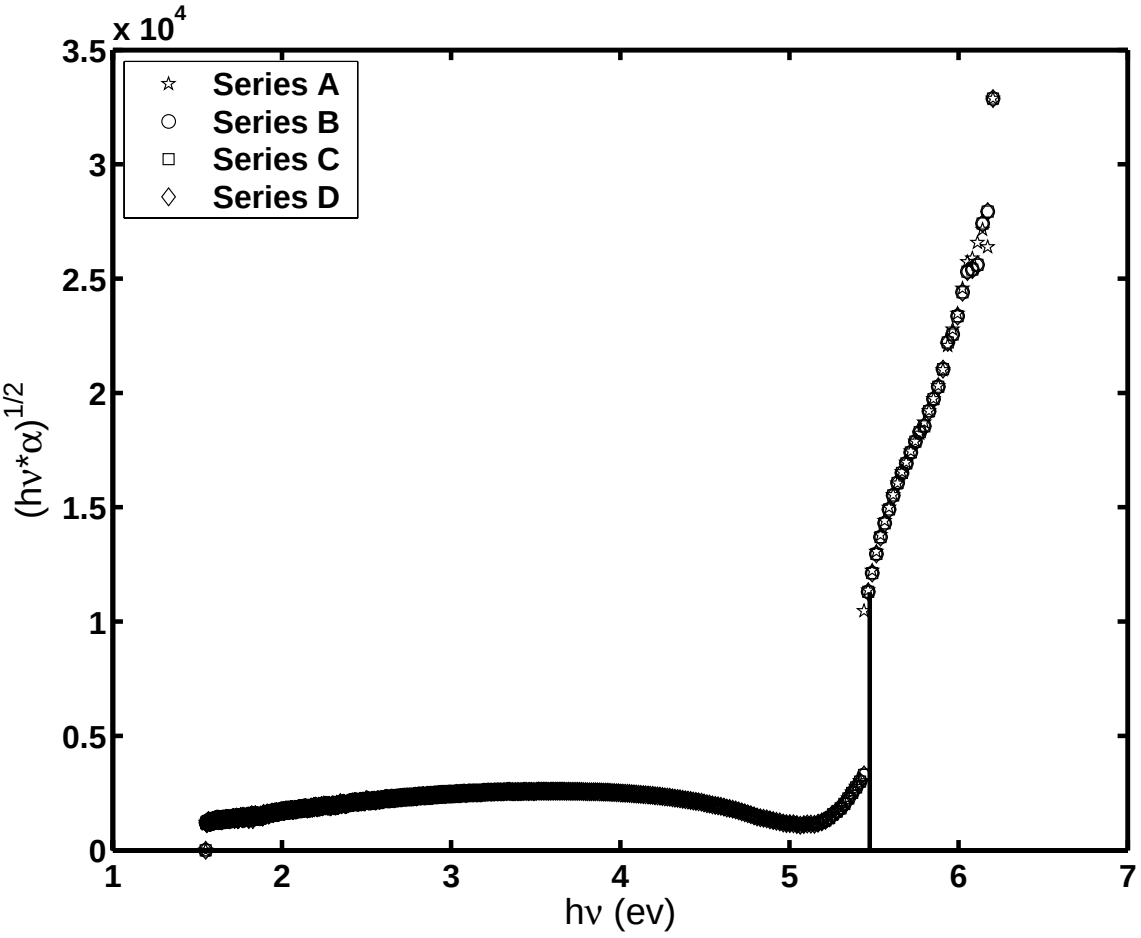


Figure 3.3: $(\hbar * \alpha * \omega)^{1/2}$ as a function of $\hbar * \omega$ for HfO_2 after anneal

power of 300W are lower than those deposited at 100W, and the samples deposited at the higher rate are lower than those at the lower rate before the post-deposition anneal. The dissipation factors of the 300W high rate samples are all less than 0.03 at a frequency of 1KHz. The dissipation factors of the 100W low rate samples are greater than 0.1, and some are up to 0.3-0.4. The high dissipation of these samples makes their permittivity measurement unreliable. After the anneal, the dissipation factor for the samples deposited at high rate decreased by an order of magnitude, but that for the samples deposited at low rate didn't change much.

The relative permittivity of the samples deposited at 300W and 100W showed similar trend versus thickness. For the samples deposited at the high rates, the relative permittivity increases with the thickness continuously. The high rate samples have much higher relative permittivity than low rate ones. After post-deposition annealing, the relative permittivity of both the high rate samples and low rate samples decreased. The relative permittivity of high rate samples is only a little higher than that of low rate samples. Figure 3.4 shows the relative permittivity (solid lines) and dissipation factor (dashed lines) as a function of thickness measured at a frequency of 1KHz for the samples deposited at a power of 300W. As mentioned above, the permittivity measurement of the samples deposited at a power of 100W and low deposition rate because of their high dissipation factor. So it's hard to compare them with the data of the samples deposited at 300W.

Figure 3.5 shows the relative permittivity as a function of frequency for the HfO_2 sample with a thickness of 50nm deposited at a power of 300W and low deposition rate both before and after the post-deposition anneal. Before anneal, the relative permittivity decreased with the increase of frequency. The relative permittivity changed from $\sim$26 at 100Hz to $\sim$16 at 1MHz. After the anneal, the relative permittivity doesn't change much over the measurement frequency range. The relative permittivity is $\sim$28.5 at 100Hz and $\sim$27 at all frequencies above 1KHz.

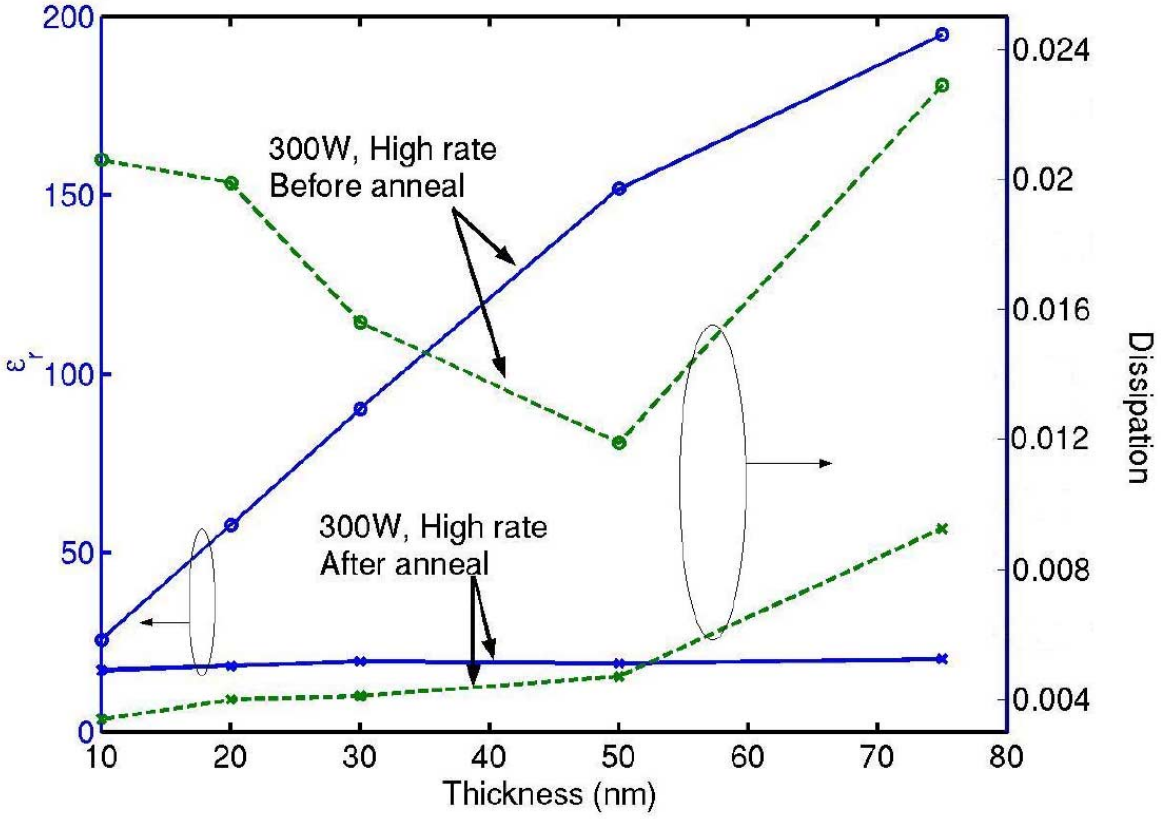


Figure 3.4: The relative permittivity and dissipation factor of HfO_2 as a function of thickness at 1KHz

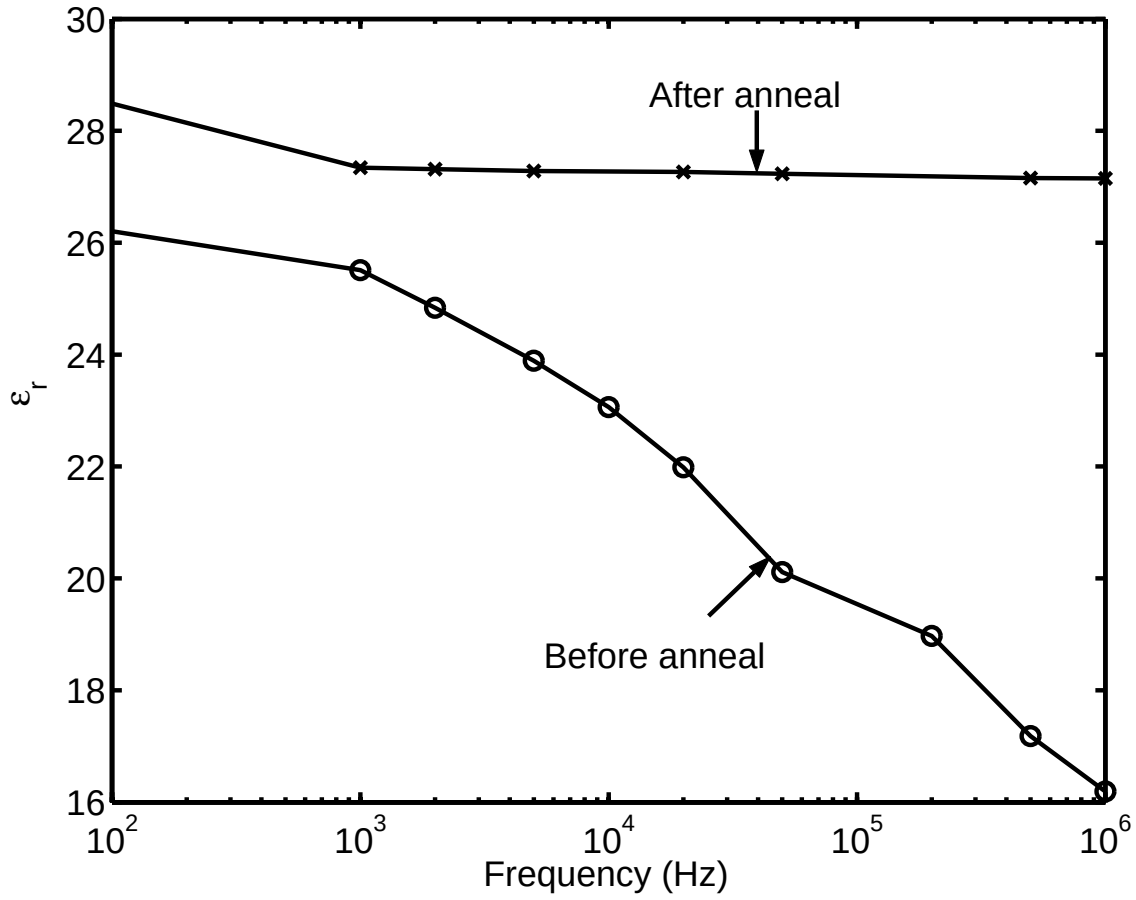


Figure 3.5: The relative permittivity of HfO_2 as a function of frequency for the 50nm sample of deposition series B

The relative permittivity increases over the measured temperature range before and after anneal of the HfO_2 sample with a thickness of 50nm in series A, as shown in Figure 3.6. After being annealed, the samples have much flatter ϵ_r(T) curve. The relative permittivity changes little with the increase of temperature. After anneal, the permittivity increased by a rate of $0.027\%/^oC$.

The relative permittivity is also a function of bias voltage. Before the post-deposition anneal, the relative permittivity increased by 9.3% when the bias voltage increased from 0 to 3volts. After the anneal, the relative permittivity remained constant over the measurement range from 0 to 5volts. The data is depicted in Figure 3.7. The triangles shows the data for the sample with a thickness of 20nm of deposition series B; the circles shows the data for the sample with a thickness of 75nm of deposition series A.

The humidity uptake was found to affect the electrical measurements before the final anneal. The measurement showed great difference (higher relative permittivity) after the sample was exposed overnight in air.

The relative permittivity becomes higher under the same measurement condition when the sample was exposed in high humidity environment. After being heated at 100^oC and cooled down, the relative permittivity decreased. This is because the humidity in the sample was expelled during the anneal. When the sample underwent the same temperature change procedure, the great change in relative permittivity didn't occur. The reason is that the sample didn't contain as much humidity as before and thus the measurement result was consistent. The change of relative permittivity during thermal cycling is shown in Figure 3.8.

The relative permittivity was measured in different humidity environment with all the other conditions the same. In high humidity environment, the capacitance thus the relative permittivity increased more than 8% in 20 minutes. The changes of relative permittivity with time under different humidity are shown in Figure 3.9. So we can

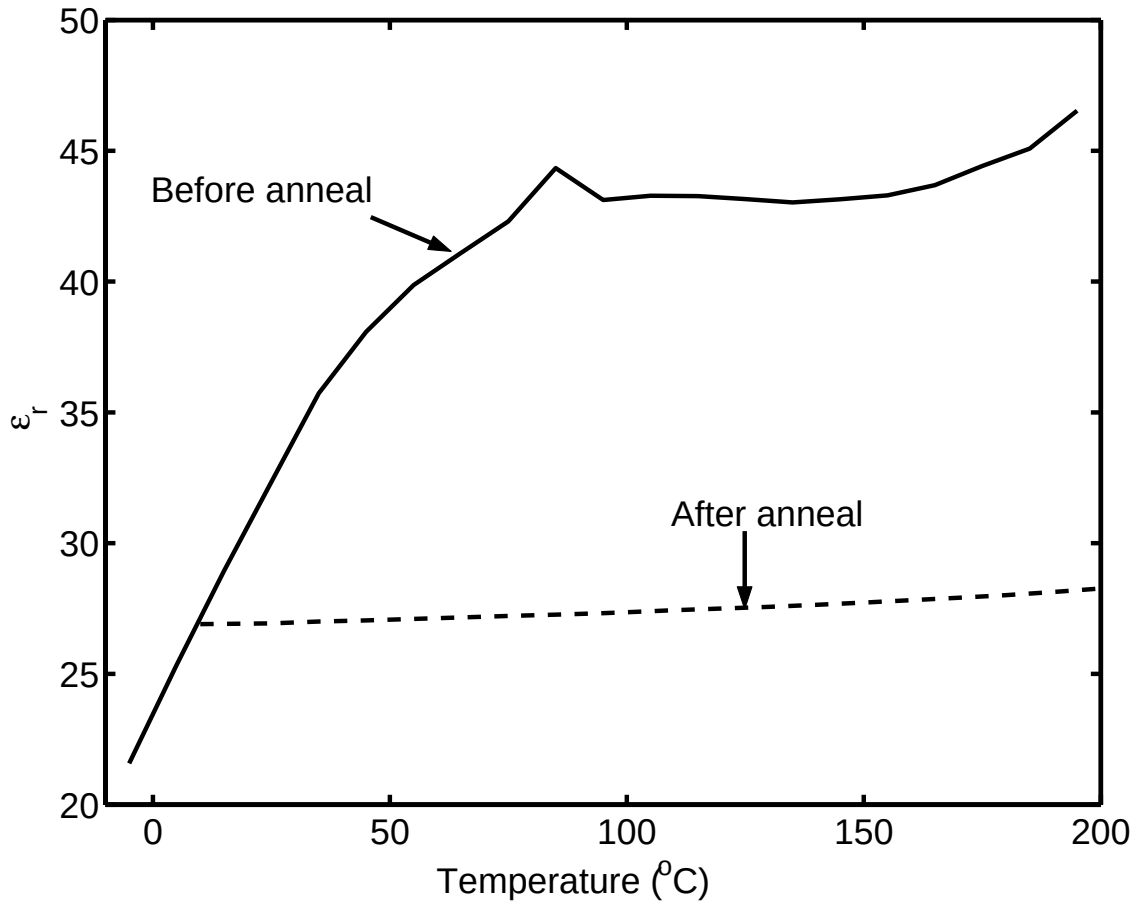


Figure 3.6: The relative permittivity of HfO_2 as a function of temperature for the 50nm sample of deposition series A

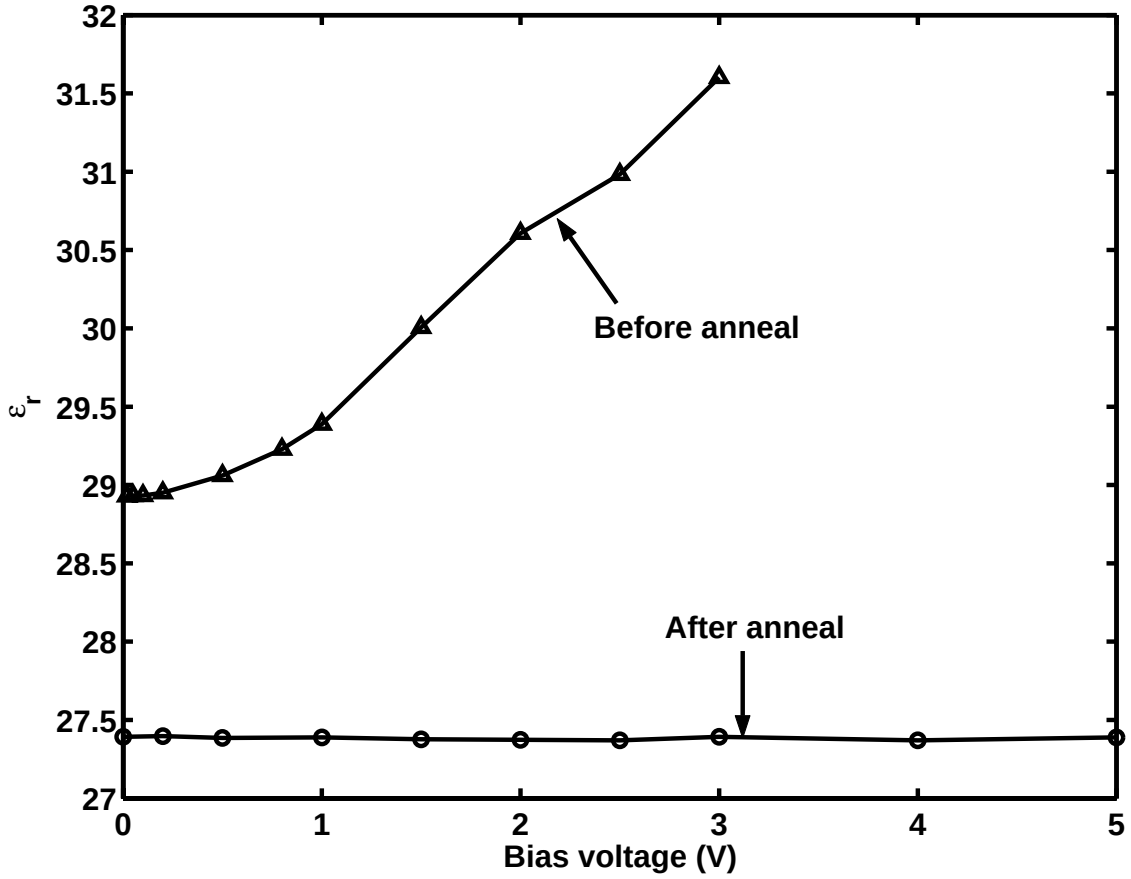


Figure 3.7: The relative permittivity of HfO_2 as a function of the applied bias voltage

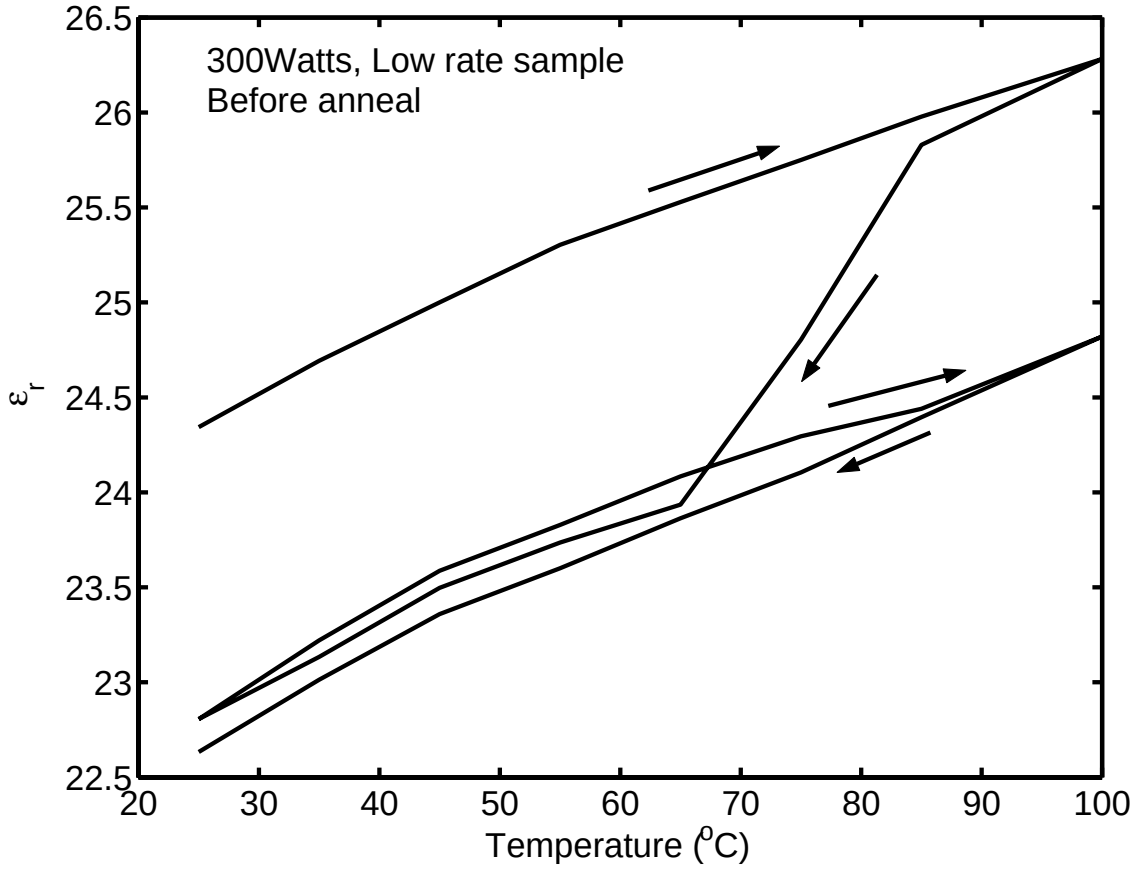


Figure 3.8: The change of relative permittivity of HfO_2 as a function of temperature (before anneal)

conclude that the humidity uptake is the reason for the change. After anneal, the influence of humidity on relative permittivity is greatly reduced most likely due to densification and more complete oxidization of the HfO_2 film.

The leakage current was measured as a function of time, voltage and temperature (I-t, I-V and I-T) for a step-function voltage input. The current density was found to decrease as a function of time following a power law $J(t) = J_0 t^{-n} + J_u$, where J_u was the final, steady-state leakage current density. The leakage current of series B and D decreases faster than that of series A and C, as shown in Figures 3.10 and 3.11. After anneal, all the series behave similarly to the low deposition rate samples but the decrease in current is even faster (n is larger). It takes only 1 to 3 minutes for the leakage currents to decrease to a stable level. The leakage current for the samples after anneal were shown in Figures 3.12 and 3.13. These transient currents may be due to the movement of charge defects in the film, such as oxygen vacancies, but further work is needed to fully investigate the cause of this transient current.

All the following measurements were performed after the leakage current decreased to a stable value to exclude the influence of transient response. Before anneal, the high deposition rate samples have leakage currents about 3-5 orders of magnitude higher than low deposition rate samples. As mentioned in Section 3.1, at high deposition rate, the Hafnium was not fully oxidized and thus HfO_x (with $x < 2$) was formed instead of HfO_2. The high deposition rate samples contain more metal than the low deposition rate samples. So they have much higher leakage currents. Before the post-deposition anneal, the 300W samples have leakage currents one order of magnitude lower than the samples deposited at 100W. The order of the magnitude of the leakage currents density (A/cm^2) at 1volt are -4 (300W high rate), -6 to -9 (300W low rate), -3 (100W high rate) and -8 (100W low rate). After the anneal, the leakage currents of all the series are in the same order of magnitude -9 or -10 at 25^oC, and increase to -6 or -7 at 200^oC.

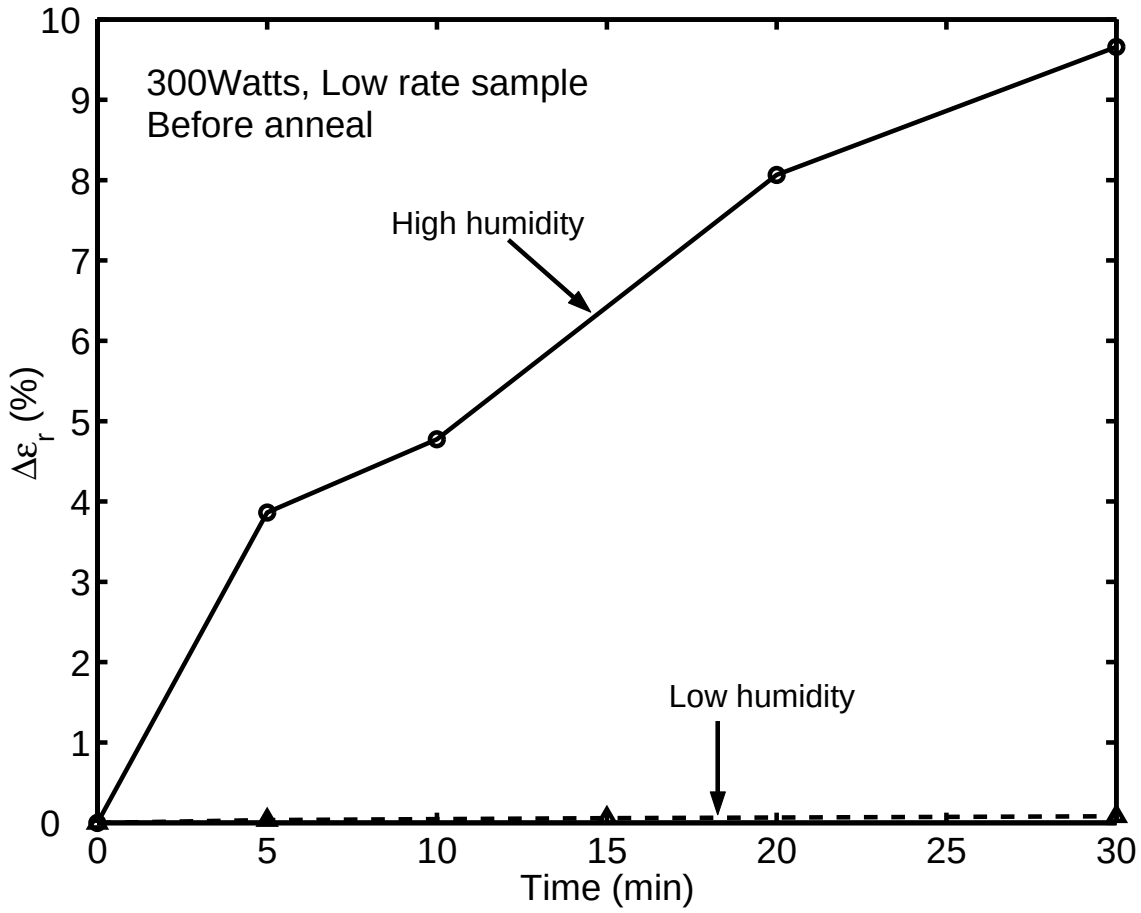


Figure 3.9: The change of relative permittivity of HfO_2 as a function of time under different humidity conditions (before anneal)

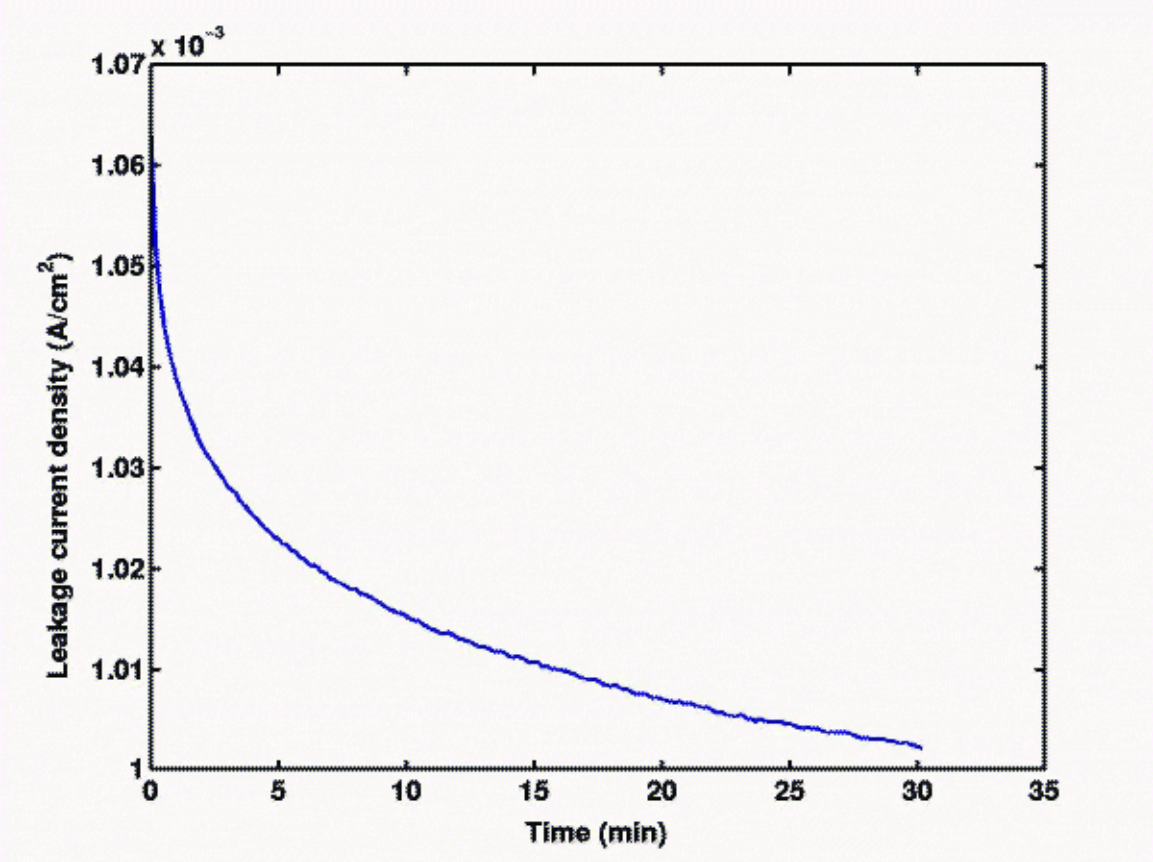


Figure 3.10: The leakage current of HfO_2 as a function of time for the sample with a thickness of 20nm of series A at 1volt before anneal

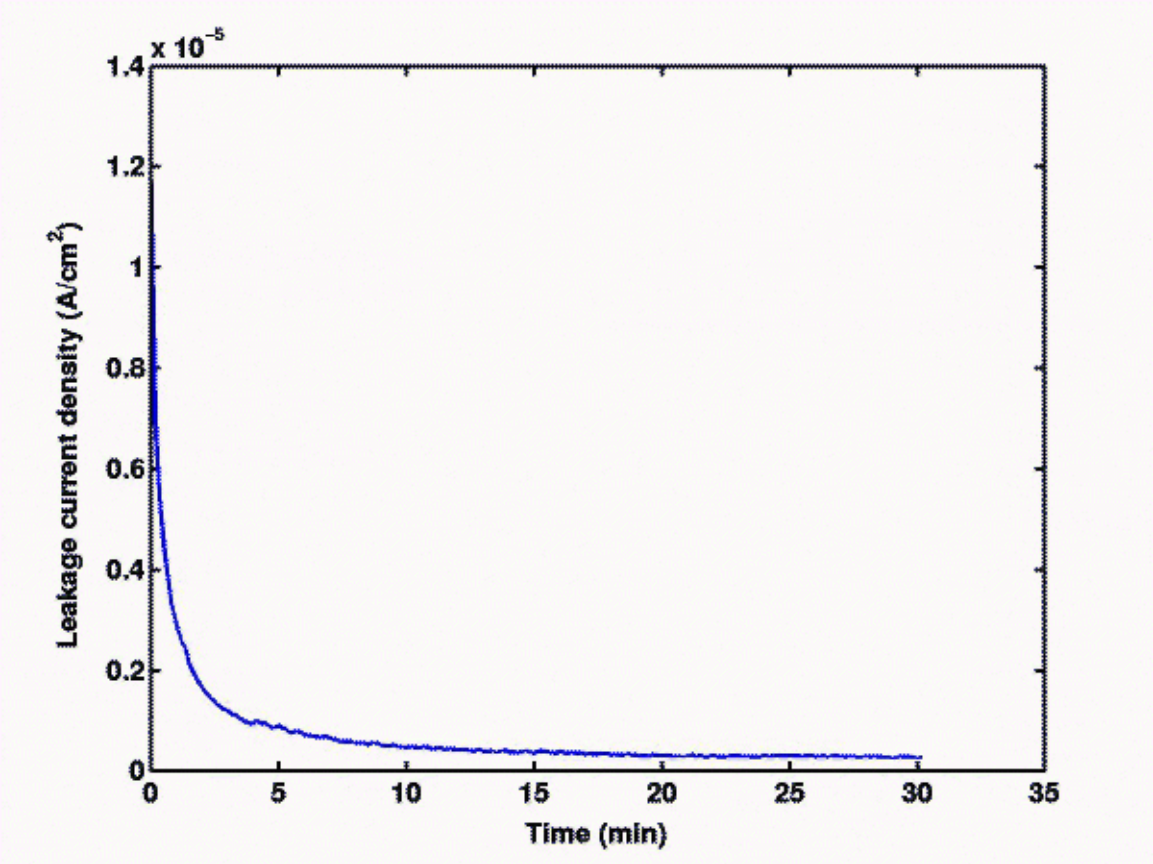


Figure 3.11: The leakage current of HfO_2 as a function of time for the sample with a thickness of 75nm of series B at 1volt before anneal

Figure 3.12: The leakage current of HfO_2 as a function of time for the sample with a thickness of 20nm of series A at 1volt after anneal

Figure 3.13: The leakage current of HfO_2 as a function of time for the sample with a thickness of 75nm of series B at 1volt after anneal

The leakage current density increases with the increase of voltage. When the voltage is between -1 and 1V, the increase of leakage current is linear. With the voltage above 1.5volts, the current has a higher rate of change. The leakage current as a function of voltage for the 50nm film from series B is shown in Figures 3.14 and 3.15. Similar behavior was observed both before and after the post-deposition anneal.

The leakage current density also changes with the temperature. The leakage current density increased with the increase of temperature when the temperature is higher than a specific threshold. When the temperature is below the threshold, the leakage current showed little temperature dependence. The threshold is different for the four series and is discussed further in section 4.2. The leakage current as a function of temperature for the 75nm film of series B is shown in Figure 3.16. The samples of other deposition series have similar leakage behavior.

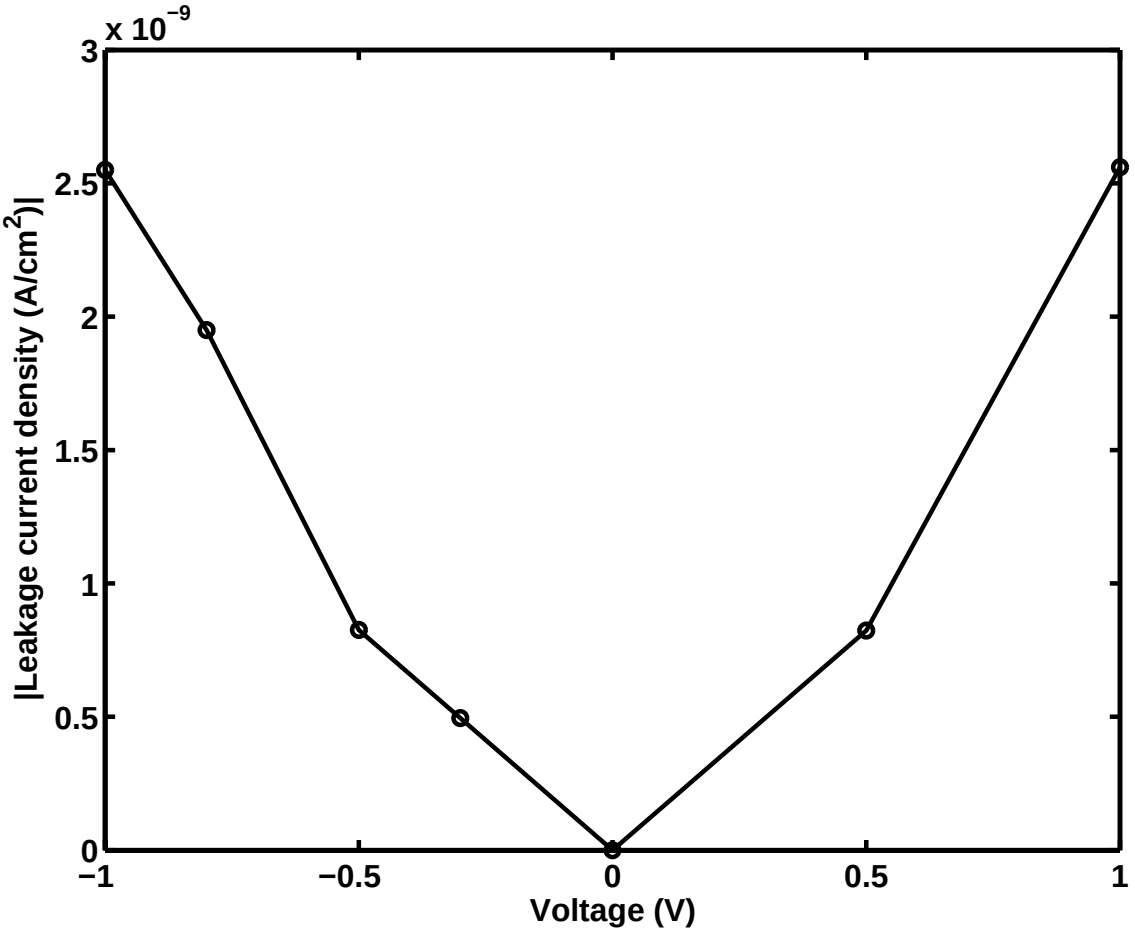


Figure 3.14: The leakage current of HfO_2 as a function of voltage for the 50nm sample of series B

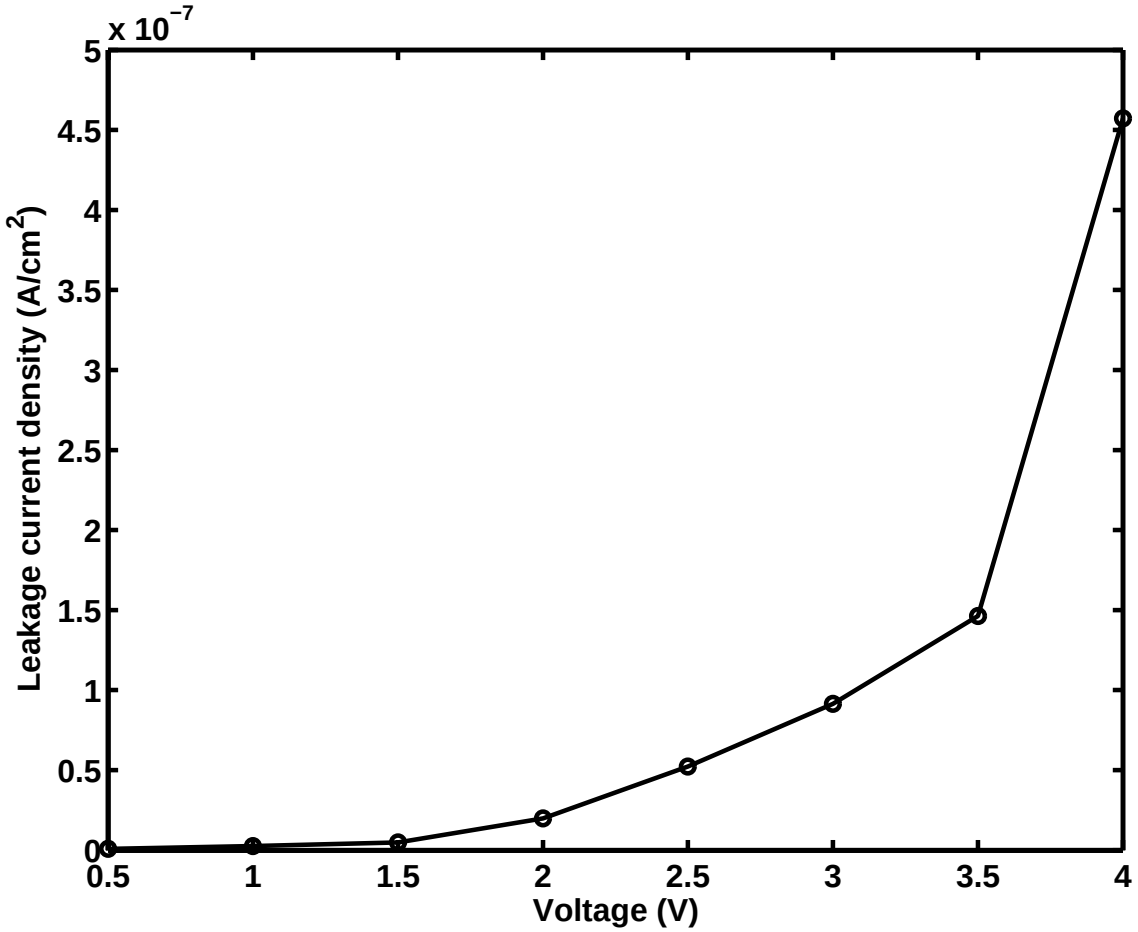


Figure 3.15: The leakage current of HfO_2 as a function of voltage for the 50nm sample of series B

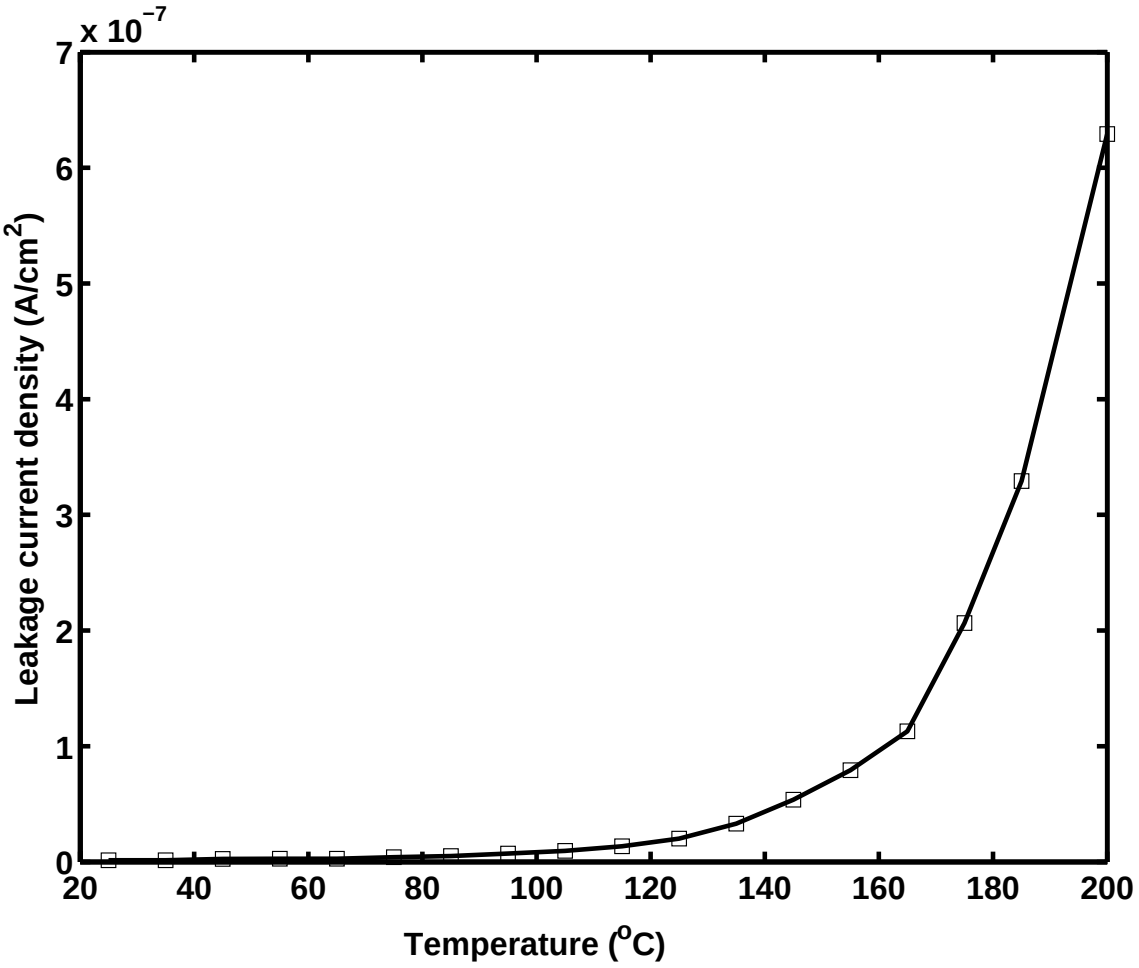


Figure 3.16: The leakage current of HfO_2 as a function of temperature for the 75nm sample of series B

CHAPTER 4

DISCUSSION OF RESULTS

This chapter describes the models for the permittivity and leakage current of the HfO_2 films.

4.1 Permittivity Model

4.1.1 Permittivity Model vs Frequency

The model for permittivity is for the HfO_2 films after the post-deposition anneal.

The permittivity of HfO_2 is nearly constant but decreases slightly between 1KHz to 1MHz. The relative permittivity of the HfO_2 films was found to follow a linear relation to the logarithm of frequency over the frequency range from 1KHz to 1MHz, as shown in Figure 4.1. The solid line shows the relative permittivity of HfO_2, and the dotted line shows the linear relation to log(f). The relation is given by

$$\epsilon_T(f) - \epsilon_0 = a \cdot log(f) \tag{4.1}$$

where ϵ_T is the permittivity of HfO_2 which is a function of frequency, ϵ_0 is low frequency limit of permittivity, a is constant, and f is the frequency. The 50nm film can be modeled with ϵ_0=27.535 and a=-0.0643.

At frequencies below 1KHz, the curve of permittivity vs. frequency deviated from the relation of Eq.4.1. Further investigation is needed to determine if this is a real effect or measurement artifact.

4.1.2 Permittivity Model vs Temperature

The relative permittivity of the HfO_2 films is also a function of temperature as mentioned in Chapter 3. After the final anneal, it increases slightly with temperature

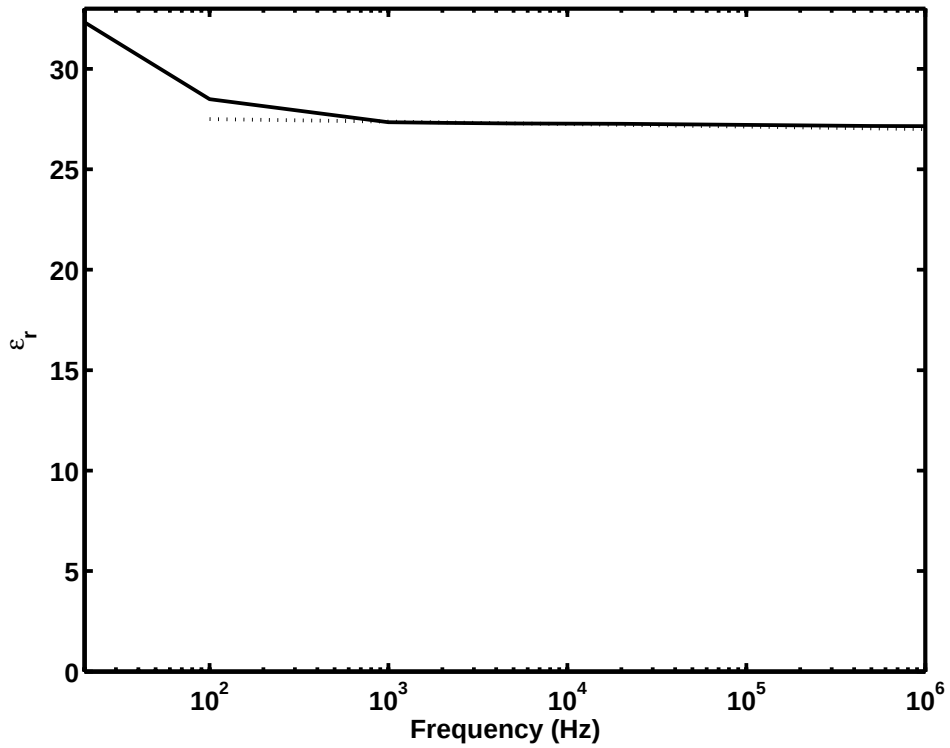


Figure 4.1: The relative permittivity of HfO_2 as a function of frequency for the 50nm sample of deposition series B

over the measurement range from 26.90 to 28.27. The function is approximately linear over the measurement temperature range, as indicated by the dashed line in Figure 3.6. The permittivity as a function of temperature is given by

$$\epsilon_T(T) - \epsilon_0 = c \cdot T \tag{4.2}$$

where ϵ_T is the capacitance as a function of temperature, ϵ_0 is the capacitance at a given temperature (here T=5^{o}C), T is the temperature in ^{o}C, and c is a constant. For all of the measured samples, ϵ_0 ≈26.90 and c=0.0072. The result for the 50nm film of series B is shown in Figure 3.6.

The relative permittivity of the HfO_2 films remains constant at different bias voltage from 0 to 5volts excluding the measurement error.

4.2 Leakage Model

4.2.1 Leakage Model vs Time

As mentioned in Chapter 3, the leakage current of HfO_2 MIM capacitors was found to decreased as a function of time following a power law.

$$J(t) = J_0 t^{-n} + J_u \tag{4.3}$$

where J is the leakage current density which is a function of time, J_0 is the initial current density when the voltage is applied, J_u is the steady-state leakage current density when the time goes to ∞, and n is a constant. The curves of log(J) vs. time for the samples of series A and B before the post-deposition anneal are shown in Figures 4.2 and 4.3 respectively. The leakage current for the samples after the anneal has similar behavior but decreases much faster with time. The curves of log(J) vs. time for the samples of series A and B after the post-deposition anneal are shown in Figures 4.4 and 4.5

respectively. Because of the shorter measurement time and the smaller range of current for the samples after the anneal, fluctuations due to noise are evident.

Series A and B can be modeled with n=0.0094 and n=0.62 before anneal and with n=0.90 and $n \approx$1 after anneal.

4.2.2 Leakage Model vs E and T

The field dependence of the leakage current density of the HfO_2 films after the post-deposition anneal was found to follow the Schottky model. The temperature and field dependence of the leakage current for the standard thermionic emission Schottky model is given by

$$J = A^* T^2 exp(\frac{-W_B}{kT}) exp(\frac{q}{kT}\sqrt{\frac{q}{4\pi\epsilon}E}) \tag{4.4}$$

where A^* is the effective Richardson's constant, which incorporates carrier mobility; q is the electronic charge, ϵ is the permittivity; k is Boltzmann's constant, J is the leakage current density; T is the temperature, E is the electric field across the film; W_B is the barrier height. If the conduction mechanism is thermionic emission, the plots of log(J) vs. $E^{1/2}$ and log(J/T^2) vs. 1000/T yield straight lines. The barrier height, W_B, can be extracted from either the slope or the intercepts of the plots [22, 23].

For fields above 1×10^5 V/cm, the curve of log(J) vs. $E^{1/2}$ for the 50nm series B HfO_2 is shown in Figure 4.6. Other series have similar behavior. It's approximately linear at voltages above 1volt. Below the knee in the Schottky plot (1V, E=2×10^5 V/cm), the field dependence is approximately Ohmic. In the Ohmic region, the resistance of the film is approximate $3.9\times10^8 \Omega\cdot cm^2$. At 27^{o}C, the dielectric breakdown occurred at $\sim$9.1V for the film with a thickness of 50nm, that is under an electric field of 1.82×10^6 V/cm.

The temperature dependence of the leakage current density for the HfO_2 films with a thickness of 75nm of all the deposition series after the post-deposition anneal at

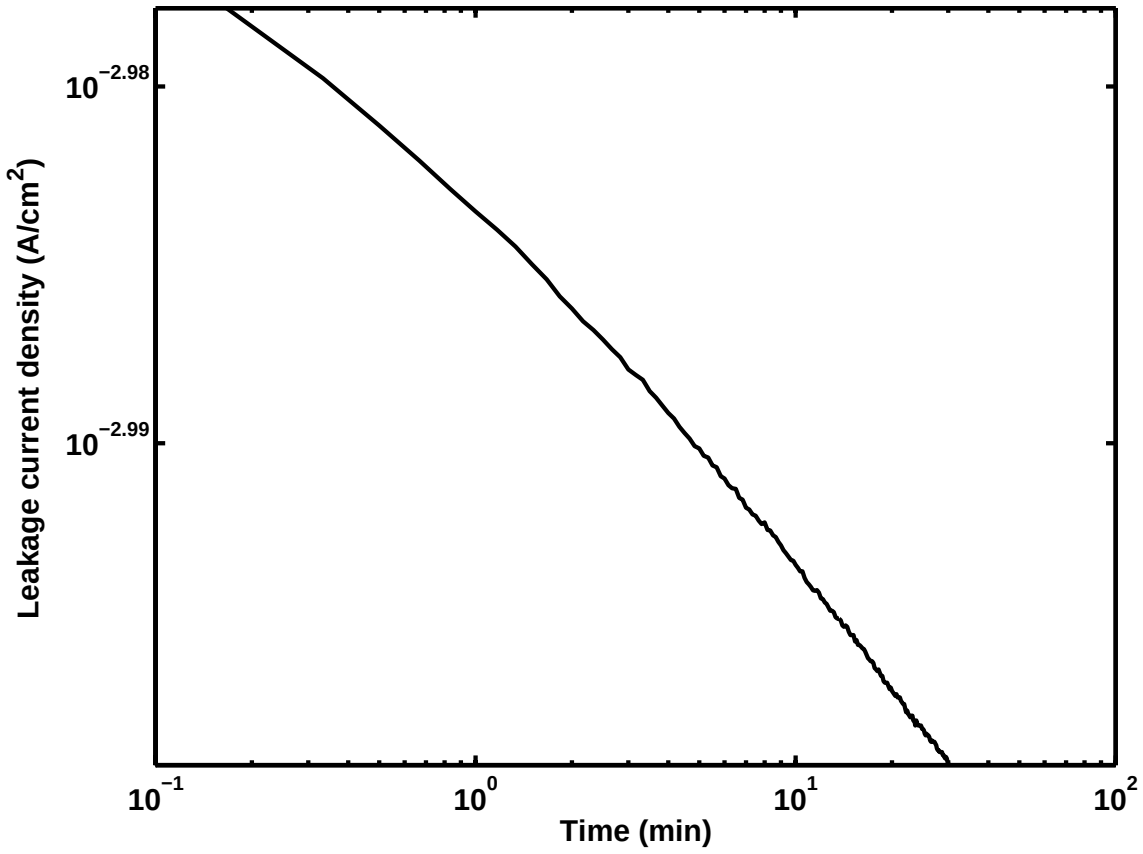


Figure 4.2: The leakage current of HfO_2 as a function of time for the sample with a thickness of 20nm of series A at 1volt before anneal

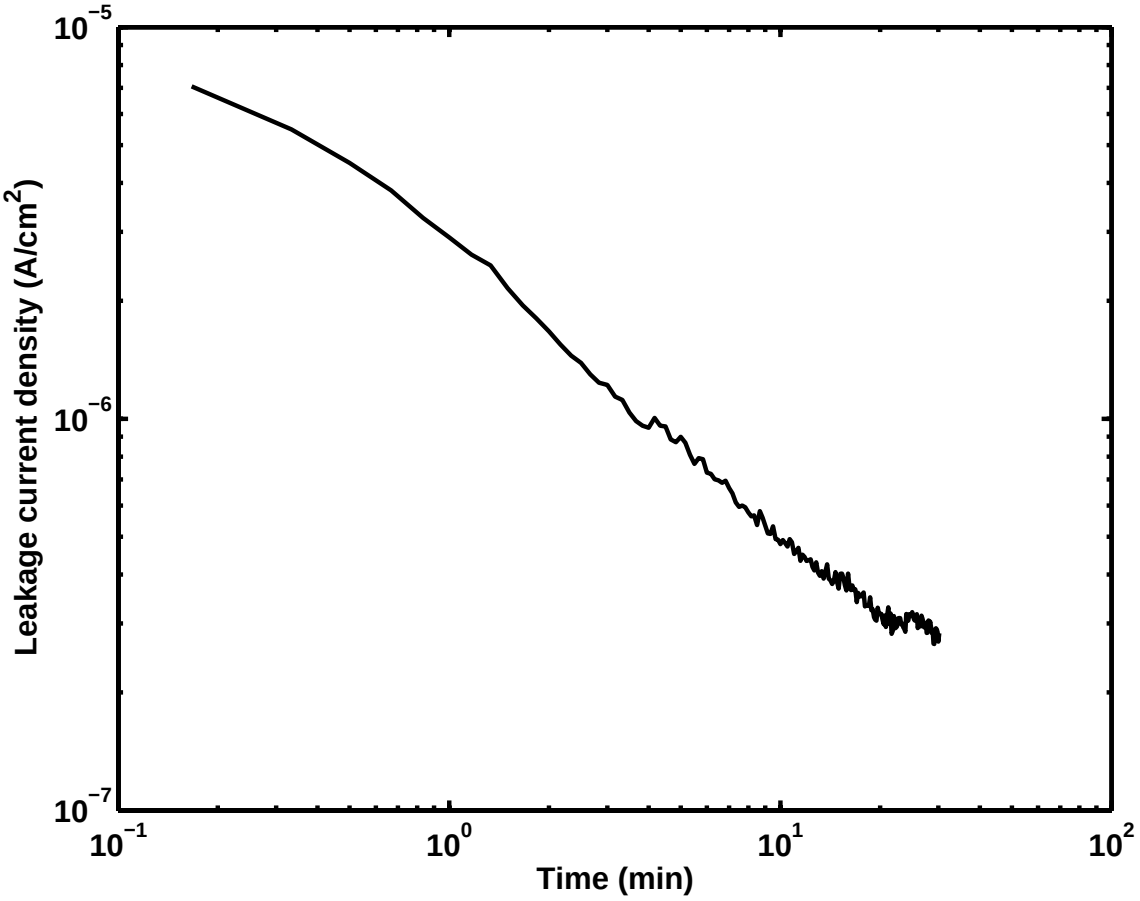


Figure 4.3: The leakage current of HfO_2 as a function of time for the sample with a thickness of 75nm of series B at 1volt before anneal

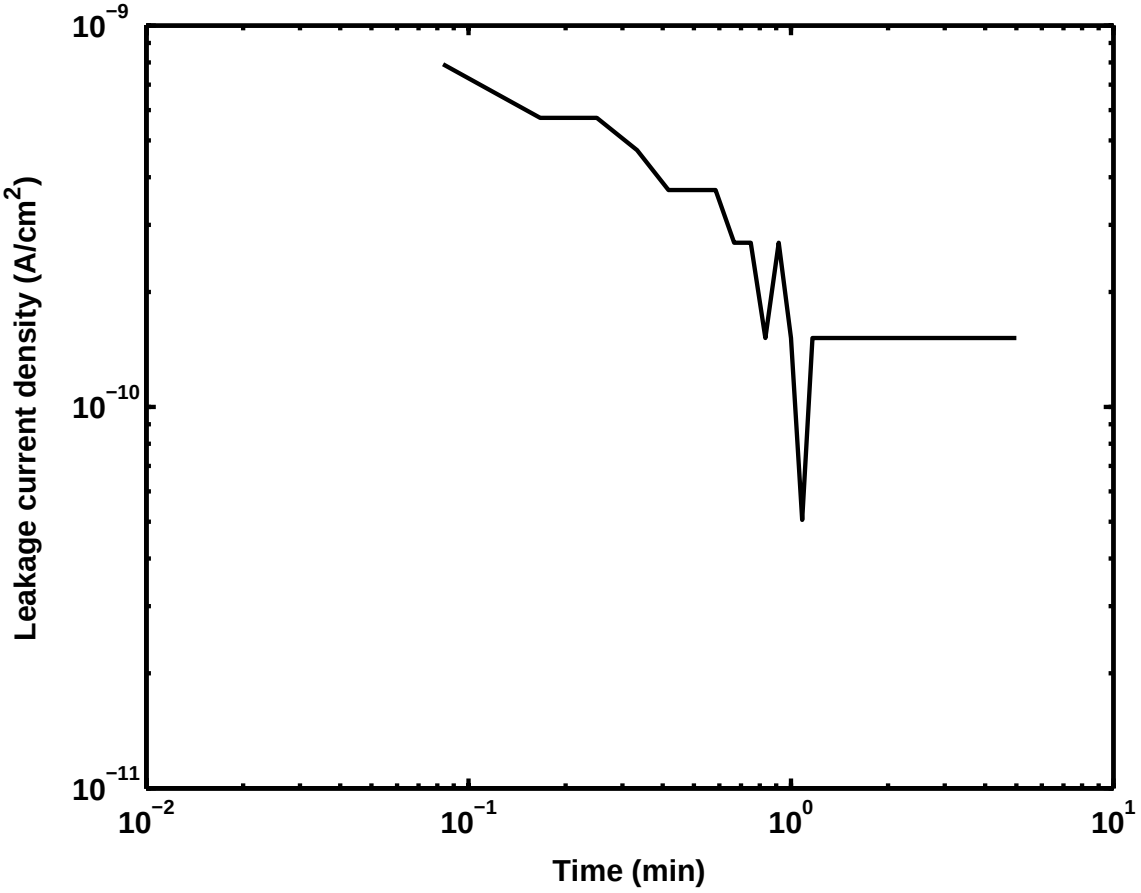


Figure 4.4: The leakage current of HfO_2 as a function of time for the sample with a thickness of 20nm of series A at 1volt after anneal

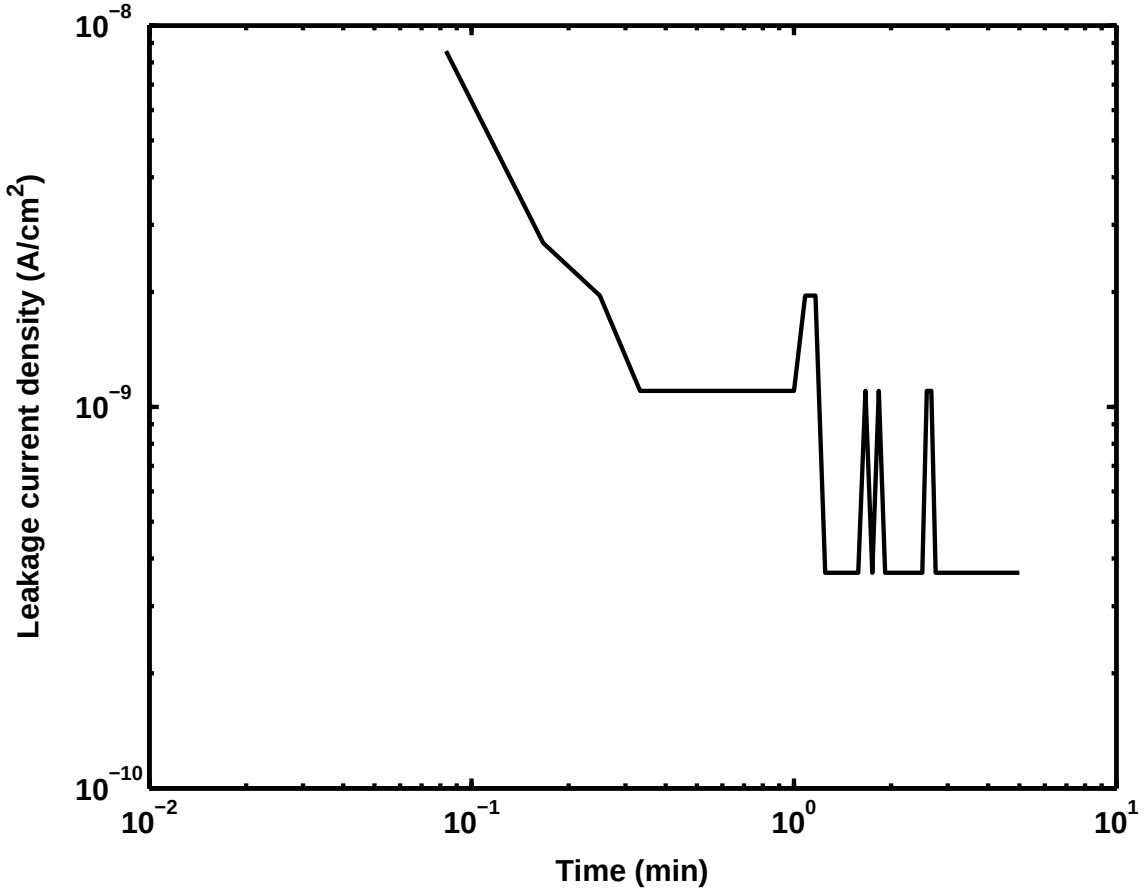


Figure 4.5: The leakage current of HfO_2 as a function of time for the sample with a thickness of 75nm of series B at 1volt after anneal

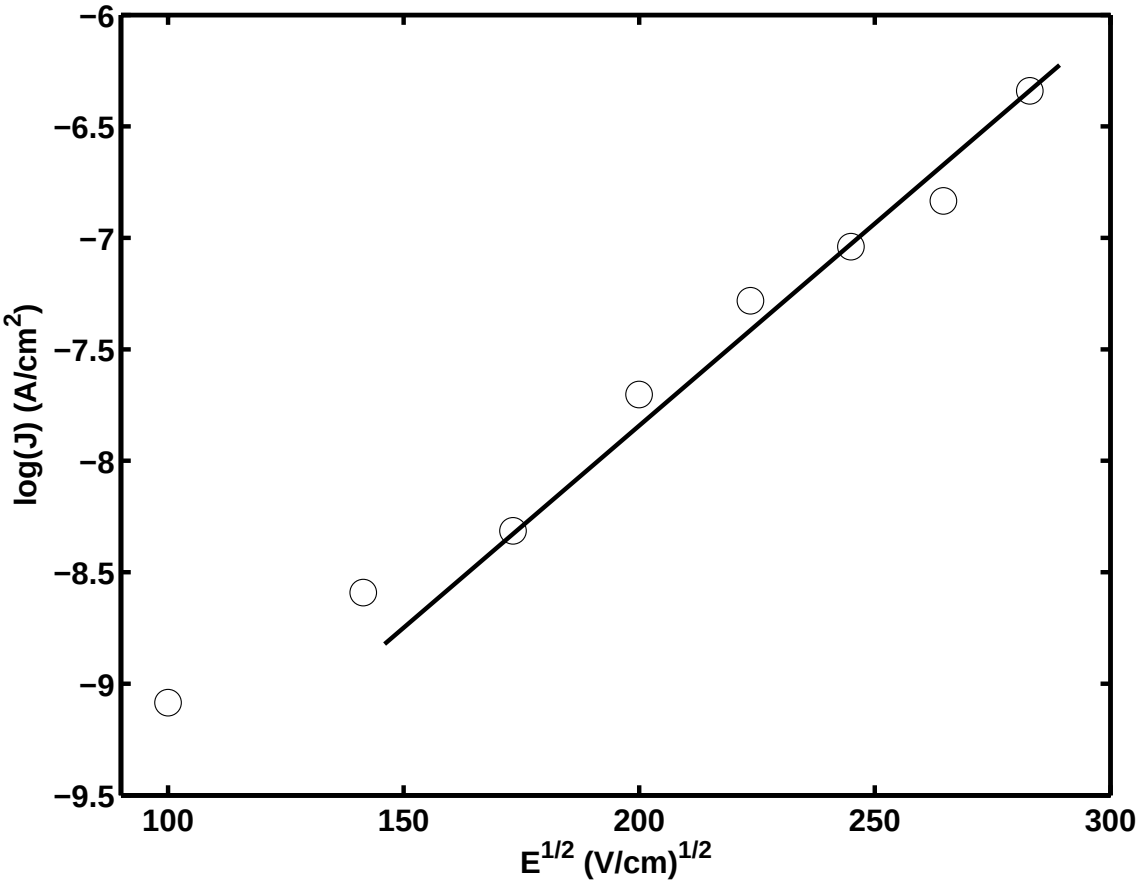


Figure 4.6: Field dependence of the leakage current density for the 50nm series B HfO_2 thin film after anneal at a temperature of 25^{o}C

a field of 1.333×10^5 V/cm is shown in Figure 4.7. At high temperatures, the curves of $\log(J/T^2)$ vs. $1000/T$ for all the series are linear. The temperature thresholds for the linear region are $\sim135^o$C, $\sim125^o$C, $\sim145^o$C and $\sim155^o$C for deposition series A, B, C, and D respectively. Using the data in Figure 4.6 and 4.7, and Eq.4.4, the Shottky barrier height W_B is estimated to be between 0.866eV to 0.885eV using.

From the discussion above, the conclusion can be drawn that the leakage behavior of HfO_2 thin films with top Pt electrode follows the Schottky model at fields higher than 1.333×10^5V/cm and temperatures higher than 125^oC. Below 125^oC, the leakage current density is nearly independent of temperature.

One possibility of such leakage behavior may be due to mobile defects in the HfO_2. The HfO_2 is assumed to be filled with mobile charged defects such as oxygen vacancies. Initially, the defects are uniformly distributed within the HfO_2 film at low temperature and low field. If there are sufficient numbers of defects, an electron may be able to tunnel through the Schottky barrier to one of the defects, then hop, from one defect to the another defect, finally reaching the other electrode. The hopping model would produce a nearly Ohmic response. On the other hand, if the defects are non-uniformly distributed (e.g., more defects near one of the electrodes than the other and thus a reduced defect region near one of the electrodes), the Schottky barrier could be the dominant barrier for electron transport and the current would follow a Schottky model. If the defects are charged, under high fields the defects will drift with the electric field and accumulate at one of the electrodes; similarly, at high temperatures, the defects would be much more mobile and would drift with the electric field (even at low fields) and accumulate at one of the electrodes. Thus, the Schottky barrier would dominate at high fields and high temperatures; a hopping mechanism would dominate at low fields and low temperatures. The models are depicted in Figure 4.8.

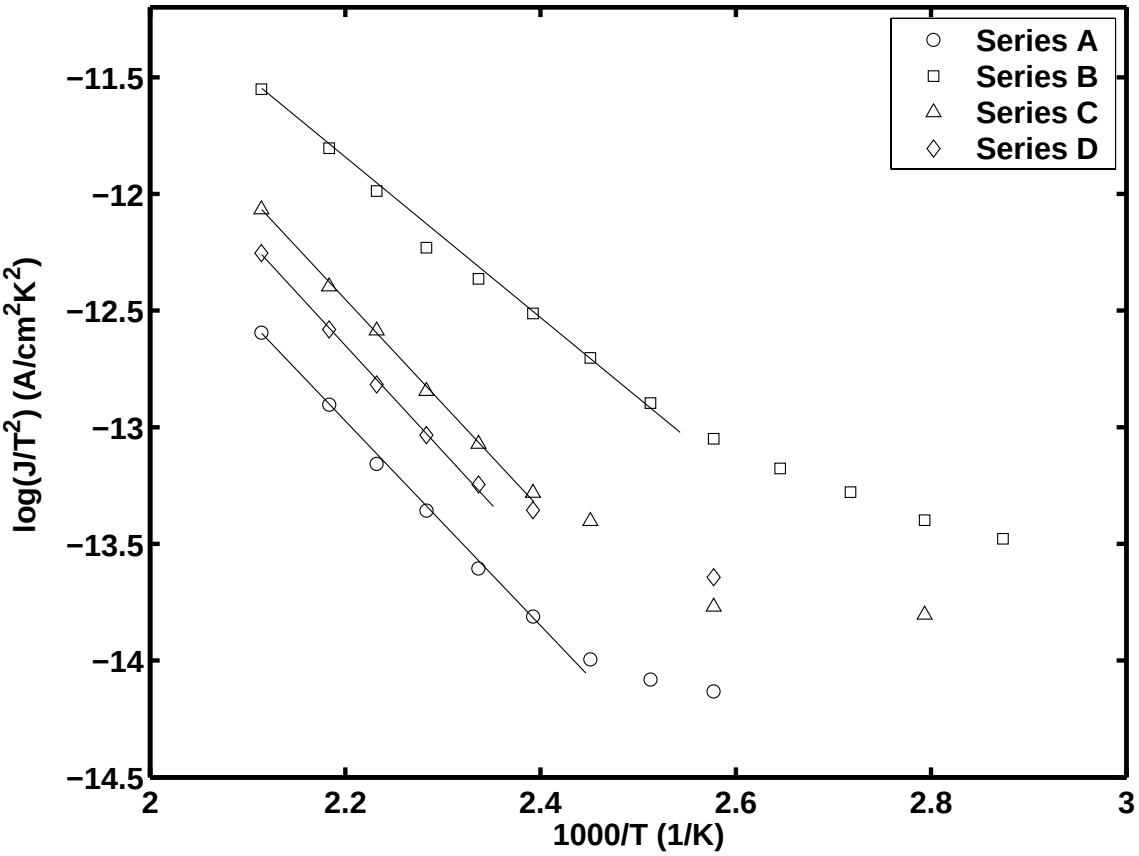
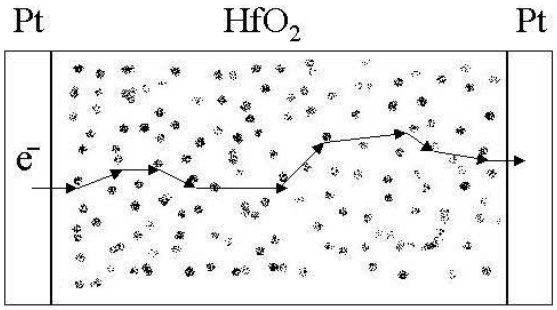
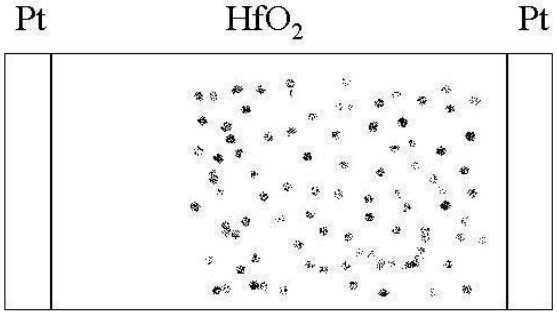


Figure 4.7: Temperature dependence of the leakage current density of HfO_2 for the 75nm thick samples of all deposition series at a field of 1.333×10^5 V/cm



At low temperature and low field, electrons can tunnel through the Schottky barrier to a defect state and hop from defect to defect.



At high temperature and high field, the Schottky barrier at interface dominates the leakage behavior.

Figure 4.8: Possible leakage model to explain carrier transport in thin films of HfO_2

CHAPTER 5

CONCLUSION AND TASKS FOR FUTURE WORK

5.1 Summary

This thesis investigated a promising dielectric for future microelectronic applications– HfO_2 in MIM structures. The HfO_2 thin films were deposited by pulsed DC magnetron reactive sputtering under different conditions. The physical and dielectric properties (relative permittivity and leakage behavior) were studied before and after the post-deposition anneal, and models for the permittivity and leakage current were developed.

5.2 Conclusion

Our experiment demonstrates that high quality thin film of HfO_2 can be deposited by pulsed DC magnetron reactive sputtering. The deposition rate versus Ar/O_2 ratio shows hysteresis. As the O_2/Ar ratio was increased, the deposition rate remained at a high level until the ratio reached a specific value, and then the rate decreased sharply to a low level and remained there. Then as the O_2/Ar ratio was decreased, the rate remained at the low level until the ratio reached a much lower value, and then the rate went back to the high level. The samples deposited at high power have lower dissipation. The best condition is 300Watts high deposition rate followed by a 600^oC, 60 minutes anneal in air. The samples made under this condition have low dissipation factor (<0.01) and lower leakage current ($<10^{-9}$A/cm^2 at a field of 1.333×10^5V/cm).

The relative permittivity is a function of thickness, temperature, frequency and bias voltage. The dependence of relative permittivity on these conditions becomes weaker after the post-deposition anneal of 600^oC for 60 minutes. The ϵ_r(T) curve increases slightly over the temperature range from -5 to 200 ^oC by 5.13% after anneal and the ϵ_r(f) curve decreases slightly over the frequency range from 100 to 1MHz

following a linear relation to the logarithm of frequency. Humidity uptake is found to be able to increase the relative permittivity of the HfO_2 films before anneal. The optical bandgap is the same for all the samples after annealing at 5.4eV.

The leakage current is a function of time, voltage and temperature. The leakage current density decreases with time following a power law. The leakage current decreases much faster after the post-deposition anneal than before the anneal. The leakage current density increases with the increase of voltage. At voltages below 1volt, the relation is approximately Ohmic. At higher voltages, it follows the relation of Schottky model. The leakage current density increases with the increase of temperature. At temperatures above a specific threshold temperature, the leakage current density follows the relation of Schottky model. The barrier height is estimated to be between 0.866eV to 0.885eV, and the dielectric breakdown occurs under an electric field of 1.82×10^6 V/cm.

As a result of my work, HfO_2 thin films shows good properties as a gate dielectric material. It has proper dielectric constant, low dissipation factor and low leakage current density. The working conditions such as temperature, voltage and frequency have little influence on its dielectric constant. So HfO_2 is a promising alternative for SiO_2, and it's worth investigating more deeply.

5.3 Tasks for Future Work

Due to the limit of time and the breakdown of devices, the properties of HfO_2 thin films in MIS structure haven't been investigated. Similar characterization of MIS capacitors will be made. The investigation of the HfO_2 MIS capacitors with different thickness SiO_2 layers would make the properties more clear. The deposition protocol of MIS capacitors is introduced briefly as follows.

The HfO_2 thin films were deposited on SiO_2/Si substrates with 29.73Å SiO_2 layer with standard deviation of 0.22Å to create MIS capacitors. The SiO_2/Si was grown by thermal oxidation by National Semiconductor using a state-of-the-art growth process.

Series	DC Power	Thickness	$\%O_2$	Deposition Rate(nm/min)
E	100W	0,3,7,10,20nm	13	8.4
F	300W	0,3,7,10,20nm	40	25.2

Table 5.1: Experimental Matrix for MIS structure

The small set of deposition conditions, which were listed in Table 5.1, are similar to those of MIM capacitors.

Two series were deposited, one at DC power 100 Watts and the other at 300 Watts. There are five samples in each series. One sample has no HfO_2 layer and the Pt electrodes were formed directly on the substrate to investigate the properties of the SiO_2/Si, four samples with the thickness of 3, 7, 10, 20nm were deposited. The deposition temperature is room temperature.

On all the samples, the thickness of top Pt electrode is 100nm.

It would be helpful to explore the properties for the HfO_2 thin films deposited under more deposition conditions such as different temperatures, pressures, more DC power levels and different duty cycles [24, 25, 26, 27, 28, 29].

The sputtering deposition method may cause damage and thus is not suitable for industrial application. So other deposition methods received attention and high quality HfO_2 thin films have been made with these deposition methods such as ion assisted deposition (IAD) [30, 31], electron-beam deposition [32] and especially the metal-lorganic chemical vapor deposition (MOCVD) [33]. It is valuable to investigate the deposition conditions and properties of HfO_2 thin films for these deposition methods.

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