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# A Frequency Response Based Approach to DC-DC Control Loop Design

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# A FREQUENCY RESPONSE BASED APPROACH TO DC-DC CONTROL LOOP DESIGN

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# A FREQUENCY RESPONSE BASED APPROACH TO DC-DC CONTROL LOOP DESIGN

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## ABSTRACT

This thesis encompasses control theory, mathematical models and practical methods for developing high performance control loops for compact DC-DC power converters. In this research we compare an existing hardware control loop design developed through traditional empirical tuning methods to a control loop established by a proposed systematic design approach. To address the many problems of ad-hoc controller design for DC-DC converters, we develop a procedure utilizing tools from frequency domain analysis and loop shaping techniques. This design approach is used to ensure control loop stability and to verify improved loop performance. This systematic control loop design procedure can be utilized for future development work to create improved DC-DC converter control loops. Our goal is to turn the art of traditional empirical tuning into a science by creating a systematic process utilizing tools that can quantify and define DC-DC converter control loop performance.

Mathematical simulations are used to verify the control loop models before hardware verification. Finally we compare resulting performance of the control loop circuitry designed with the proposed approach to that of the empirical approach.

# TABLE OF CONTENTS

Page

# LIST OF TABLES

**Table** **Page**

# LIST OF FIGURES

**Figure** **Page**

# NOMENCLATURE

FET: Field Effect Transistor

ESR: Equivalent Series Resistance

PWM: Pulse Width Modulation

CCM: Continuous Conduction Mode

DCM: Discontinuous Conduction Mode

OLG: Overall Loop Gain

SSA: State Space Averaging

OTC: One Time Constant

# CHAPTER I

# INTRODUCTION

Historically it has been difficult to determine the required feedback control loop parameters upon the initial design of a power converter. DC-DC converters have many control and power circuitry components which are misunderstood and difficult to characterize. These complex elements make the analysis of the control loop difficult. In most cases, at the start of a design, estimates of the control parameter values are determined. Many times these control parameters are based on years of experiences resulting in empirical tuning of the feedback elements. Once the hardware has been built and system dynamic testing begins, the long hours of painstaking and frustrating empirical tuning become a reality. This controller design problem may consume the majority of the effort in developing a DC-DC converter.

The goal of this research is to provide a systematic method to improve an analog controller for a DC-DC power converter. Currently, there are multiple methods used for

modeling power conversion systems such as DC-DC converters. A simulation package such as PSPICE® or SABER® can be used for this purpose. Additionally, Mathcad® can support this effort and make it easier to deal with the equations required to determine the time response of the DC-DC converter. Good models must be available in order to achieve good results. Many of the components within a DC-DC control loop system model do not exist and must be created by the user. This requires a deep understanding of the power components being evaluated. In order to obtain the results that closely match real world hardware, we must include some or all of the parasitics contained within the individual components that make up the converter. These components consist of diodes, FETS, capacitors, and inductors. Understanding the details of these components will allow us to determine what parasitics can be omitted to simplify the model without having much effect on the simulation results. By utilizing mathematical models we can develop a good understanding of each segment of the power converter as well as the effect that each segment has on the control system.

The motivation for this research comes from many years of utilizing empirical tuning methods for DC-DC converter control loops. The difficulty with this method is revealed by the painstaking non-systematic nature of the resulting lab work. This has resulted in the desire to create a systematic approach for defining and improving these control parameters. It is imperative we establish a mathematical systematic approach (a process) that can be easily utilized for developing control loops and establishing the resistive, inductive and capacitive component values for the DC-DC converter analog

controller. Having a process like this will dramatically reduce development costs as well as design time.

Improving the stability of the control loop and maximizing converter performance will be the key focus for our process. Utilizing new tools such as Mathcad® and Simulink® we can get a good look at how the system will perform in the real-world hardware. Of course our ultimate goal is to establish a means to effectively utilize these tools to accurately predict how DC-DC converter control loop will respond. We will discuss new and old methods that can be used to understand and feedback control system for DC-DC converters. We will also review some of the newer tools created that make it easier to work through some of the difficulties of the mathematical equations. This will be followed by reviewing some of the more traditional mathematical tools used to quantify the feedback loop stability and system transient response.

In order to fully understand the methods described in our process, we will first discuss the operating principles of DC-DC converters. We will review the DC-DC converter power topology first, then move on to the power flow, timing, small-signal analysis and finally the DC-DC output filter characteristics. Following this we then will describe our systematic approach for a voltage mode control loop design used to control a DC-DC buck converter.

After describing the difficulty with empirical tuning of control loops in the introduction of chapter I, the rest of this thesis is organized as follows. In Chapter II, we review the basic DC-DC converter operation as well as frequency domain and time domain characteristics of the DC-DC converters. We also review basic concepts and

tools such as Bode diagrams and the Laplace transform. In Chapter III we go on to develop the improvement process and describe the DC-DC converter hardware system containing the control loop. We then establish how to treat the non-linear dynamics of the converter so traditional mathematical tools for frequency domain analysis can be applied. We further discuss how to compensate the DC-DC converter error amplifier in order to ensure good stability and time response. These chapters will serve as the basis for our process of determining feedback component values that will ensure good DC-DC converter control loop performance. Finally we verify our mathematical approximation by comparing it to the lab data (scope plots) of the existing converter in order to ensure our approach and the mathematical model represent and produce results closely matching the real world hardware.

Finally, in Chapter IV, the proposed design process as applied to the existing DC-DC converter is evaluated by utilizing both the time domain and frequency domain analysis. This proposed process will be implemented utilizing both the mathematical model and the real hardware. The experimental data is used to compare the old design to the new one.

# CHAPTER II

# DC-DC CONVERSION

## 2. 1 DC-DC Conversion Background

DC-DC converters are used to convert voltage up or down. A buck converter the a higher voltage on the input to a lower voltage on the output. A boost converter the voltage is shifted upward from the input. A buck-boost will regulate the output voltage even if the input voltage is below or above the output voltage set point. DC-DC converters are used in a variety of applications, however, systems such as battery systems or systems that contain a constant DC bus will utilize DC-DC converters to interface to downstream components that require a different voltage level.

In 1976, Fred C. Lee of Virginia Polytechnic Institute established a method for obtaining a small signal model for buck, boost and buck-boost converters.[6] By taking the transform of the loop components we can establish an independent transfer function of the individual blocks within the system. Combining these transfer functions we can

obtain the gain and phase plots [2], [3], [4] in the frequency domain. Also, if we apply the step function and take the inverse Laplace transform [2] and plot the resulting time domain function we can obtain the transient response of the system.

In the past, taking the inverse Laplace transform in this way was very difficult due to the complexity of each equation. With the use of Mathcad® taking the Laplace transform becomes a very simple task.

State space averaging, [1],[3],[13],[14] shown in Figure 1, is a technique proposed by Slobodan Cuk and R. D. Middlebrook[15] in 1976, and used very effectively in deriving models for power converters. This technique allows ideal components (FET switches) to be evaluated and weighted with a duty cycle value. This average is established over a single power cycle or a single period. The state space average equations are the equations of valid small signals around a nominal operating point. A key point in state space averaging is that we ignore terms with products of any two small signal perturbations and this makes the dynamic model linear.[10] Once again, time domain expressions can be obtained by taking the inverse Laplace transform of the transfer function equations. State space averaging is a great technique for developing mathematical models. Again, with new software programs such equations can be easily manipulated. For our purposes, we will simply create transfer function equations directly from the components within the system. These transfer function equation can be directly graphed in the frequency domain and the inverse Laplace transforms will be graphed in order to obtain the time response.

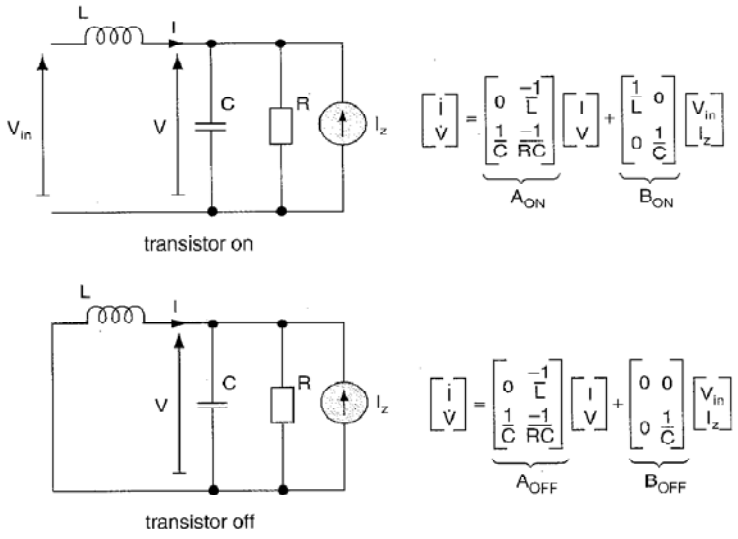


Figure 1: State Space Averaging Model for a DC-DC Converter

## 2. 2 Concepts and Criterion for Loop Stability

The concepts for defining the stability of a system used in this research are not necessarily novel; however, establishing a concise process by which all of these concepts can be utilized to improve a control loop for DC-DC converters is extremely valuable. We will attempt to create this approach to organize these concepts in a way that will be effective in DC-DC converter design. In addition, we will also develop an understanding of instability caused by certain elements within system control loop.

In the following paragraphs we discuss several key concepts relating to control loop system stability that are very important. It is imperative that we understand how the concepts apply to switched mode power conversion technology. This will help support our efforts in determining the best approach to identify a systematic approach to improving DC-DC converter control loop performance.

With voltage mode control the output LC filter shown in Figure 1 adds up to 180° phase lag to the feedback loop. The error amplifier has negative feedback therefore it adds 180° phase lag to the loop as well. The system must be compensated otherwise the feedback loop could be inherently unstable. Also, as the input voltage increases so will the loop gain of the system. This makes it harder to stabilize. Another difficult problem when implementing empirical tuning methods is obtaining lab measurements of the phase and gain margin. It is virtually impossible because the optimal point for AC signal injection is embedded inside the control chip and is not accessible. AC signal injection is a technique used to measure the system phase and gain by implementing a frequency sweep and observing the reduction in amplitude and phase shift at certain points within the system.

Finally, establishing the gain and phase [2], [3], [11] characteristics of each element within the control loop is difficult because the modulator, opto-isolator, and Field Effect Transistors in the power train are nonlinear elements and have bandwidth limiting characteristics.

The design process being developed is based on the concepts of the Nyquist stability criterion [2], [3], [6]. The following are well known Nyquist criterion concepts that apply to our voltage mode control system.

A simplified version of the Nyquist stability criterion can be used because the unity gain crossover occurs only once in the gain versus frequency plot. When evaluating the open loop gain we need to realize that if the open loop gain crosses the 0 dB (or unity) point only once, the system is stable if the crossover frequency point (unity or zero

dB point) is less than the corresponding point where the phase plot crosses the -180° line. If the phase lag at the crossover frequency exceeds 180° phase shift, then the loop will oscillate at the crossover frequency. The phase margin [2], [3], [11] is commonly known as the amount by which the phase lag is less than the critical value of -180° at the crossover frequency $f_c$ on the gain versus frequency plot. In addition, the gain margin [2], [3], [11] is the factor by which the gain is less than unity (0 dB) at the point when the phase plot reaches -180°. If the phase lag at $f_c$ is only a few degrees less than 180° (small phase margin) the system will be stable but will have considerable overshoot and ringing at the crossover frequency $f_c$. If the phase margin of the system is at least 45°, the system will yield good response with little overshoot and no ringing. Finally, we should have at least 20 dB of gain margin when phase approaches -180°. In addition, at frequencies less than $f_c$ the phase lag may be permitted to exceed 180° even though the open loop gain is greater than one. Understanding these items will support our efforts in identifying the best possible process for improving DC-DC converter control loop performance.

### 2. 3 Phase and Gain Plots

A generic feedback control loop used in DC-DC converters is shown in Figure 2.

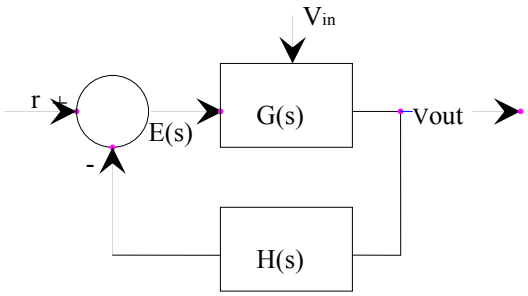


Figure 2: DC-DC Converter Closed Loop Configuration

Let $G(s)H(s)$ be the loop gain transfer function. A random particular example is

$$G(s)H(s) = \frac{1*10^6(s+10)}{(s^2)(s+100)(s+1000)} \tag{2.1}$$

Converting this transfer function to the following form shown in Equation 2.2 and taking 20*log $\left| G(s)H(s) \right|$ we can establish the logarithmic magnitude gain plot in dB.

$$|G(j\omega)H(j\omega)| = 20 * log \left| \left\{ \frac{100 * \left|1 + \frac{j\omega}{10}\right|}{|(j\omega)^2| * \left|1 + \frac{j\omega}{100}\right| + \left|1 + \frac{j\omega}{1000}\right|} \right\} \right| \ dB \tag{2.2}$$

$$|G(j\omega)H(j\omega)| = 20 * log\ |(100)| + 20 * log\ |(1 + \frac{j\omega}{10})| - 40 *$$

$$log\,|(j\omega)| - 20 * |\left(1 + \frac{j\omega}{100}\right)| - 20 * log\ |(1 + \frac{j\omega}{1000})|\ dB \tag{2.3}$$

The following form can be derived from the transfer function and used to establish the phase plot.

$$\emptyset_{G(j\omega)H(j\omega)} = \tan^{-1}(\frac{\omega}{10}) - \tan^{-1}(\omega^2) - \tan^{-1}(\frac{\omega}{100}) - \tan^{-1}(\frac{\omega}{1000})$$

(2.4)

We would like to use Bode plot information for ensuring a stable DC-DC feedback control system. In fact we can monitor the gain margin at the converter switching frequency to ensure that we have reduced the gain at that point to prevent instability. By providing at least 20 dB of gain margin at the converter switching frequency we can eliminate switching noise from being amplified by the control loop. As we explain later, we set the corner frequency of the output LC filter to approximately 1/10 of the converter switching frequency. This LC filter will inherently provide a negative -40 dB per decade of system gain roll-off, ensuring that the switching frequency noise will not be present in the system output.

As stated previously, a phase margin of 45° yields good response with little overshoot and essentially no ringing. The Bode plots in Figure 3 illustrate a system that is nearly unstable. Later we illustrate how to compensate a system so we may improve the system stability, reduce overshoot and ringing.

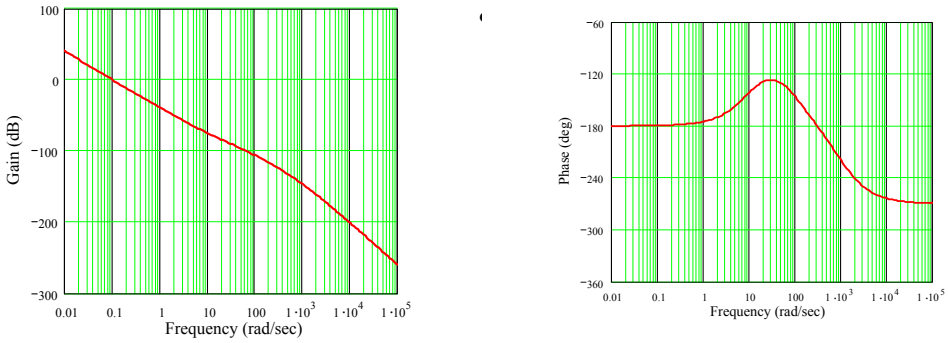


Figure 3: Phase and Gain Plots

## 2. 4 Time Domain Characteristics

For the purpose of analysis, it is important to represent the feedback loop mathematically. The following equation is called the closed loop transfer function and represents the system in Figure 2. Equation (2.5) and Figure 2 can be used to establish the frequency and time domain performance of the system. $G(s)$ is typically considered the plant and $H(s)$ is the compensator.

$$\frac{V_{out}}{r} = \frac{G(s)}{1+G(s)H(s)} \tag{2.5}$$

The right side of this equation is typically a ratio of two polynomials. The roots of the numerator are called the zeros and roots of the denominator are called the poles. The denominator of the closed loop transfer function is called the characteristic function and setting the characteristic function equal to zero yields the characteristic equation. We use the characteristic equation to establish the stability of the overall system transfer function.

$$1 + G(s)H(s) = 0 \tag{2.6}$$

The roots of the characteristic equation are used when determining the stability of the system. These roots can be real or complex. In the s-domain, if the roots are in the left-hand plane (left of the imaginary axis), then the feedback loop will be stable. If one or more of the roots lie in the right-hand plane (to the right of the imaginary axis) then the system will be unstable. If the roots lie on the imaginary axis and none in the right hand plane then the system will be marginally stable.

In order to express the characteristic equation in the frequency domain the Laplace transform [2], [3] or transform tables can be used.

$$F(s) = \mathcal{L}\{f(t)\} = \int_{0^-}^{\infty} e^{-st} f(t)dt \tag{2.7}$$

To express the response of a system in the time domain, we can take the inverse Laplace transform of the following equation.[2], [3]

$$\mathcal{L}^{-1}\{F(s)\} = \frac{1}{2\pi}\int_{c-j\infty}^{c+j\infty} e^{st}F(s)ds = f(t) \tag{2.8}$$

By subjecting the closed loop transfer function to a step input and applying the inverse Laplace transform [3], [10] we can generate a time response of our DC-DC converter system. The following equations can be used to establish the time domain transient response of our second order system to a step response.

Consider the following transfer function

$$G(s) = \frac{(\omega_a^2)}{s^2 + 2z\omega_a s + (\omega_a^2)} \qquad G(s) = \frac{100}{s^2 + 2z\omega_a s + (\omega_a^2)} \tag{2.9}$$

where $z$ is the damping ratio [2], [5] and $\omega_a$ is the natural frequency.

Applying a step input to the above system [10], the output becomes

$$y(s) = \frac{100}{s(s^2+2z\omega_a s+{\omega_a}^2)} \tag{2.10}$$

its inverse Laplace transform is obtained as

$$y(t) = 1 - \frac{e^{-z(\omega_a t)}}{\sqrt{(1-z^2)}}\sin[\,\omega_a(\sqrt{(1-z^2)})t + \theta] \tag{2.11}$$

Clearly, when the damping ratio $z$ decreases, the closed loop roots approach the imaginary axis and the response will become increasingly oscillatory.

The following quantities in Table I are used to characterize the time response plot of a second order system. It should be noted, as the damping ratio increases the system will oscillate less but may require more time to settle out. Let the following illustrate characteristics of the time response of a second order control system for a DC-DC converter.

TABLE I: TIME RESPONSE EQUATIONS

| | | |
|---|---|---|
| $OTC = 1/(z\,\omega_a)$ | Time required for the output to reach 63% of the final value | (2.12) |
| $T_p = \frac{p}{\omega_a\sqrt{(1-z^2)}}$ | Peak Time | (2.13) |
| $T_s = \frac{4}{z\omega_a}$ | Settling Time is the point after four time constants and defines the time where the response remains within 2% of the final output. | (2.14) |
| $M_{pt} = 1 + e^{-\frac{zp}{\sqrt{(1-z^2)}}}$ | Peak value of the time response overshoot | (2.15) |
| $PO\% = (M_{pt} - 1)100$ | The percent overshoot is the maximum amount of overshoot of the time response. | (2.16) |

The quantities in Table I will help us to evaluate and define the swiftness and other characteristics of the system time response. Another important note is that a third order system can be approximated by the dominant roots of the second order system as long as the real part of the dominant roots is less than 1/10 of the real part of the third root.

## 2. 5 Time Response Simulation Example

Below we plot the time response of a second-order plant to a step input. Changing the damping ratio will modify the system's response. The damping ratio [2], [5], [10] will affect the amount of overshoot and the quickness of the settling time. In this example we randomly pick the damping ratio $z$ in order to illustrate the effect it has on the time response of the system. Let the damping ratio $z = 0.215$ and $\omega_a$ =4.631.

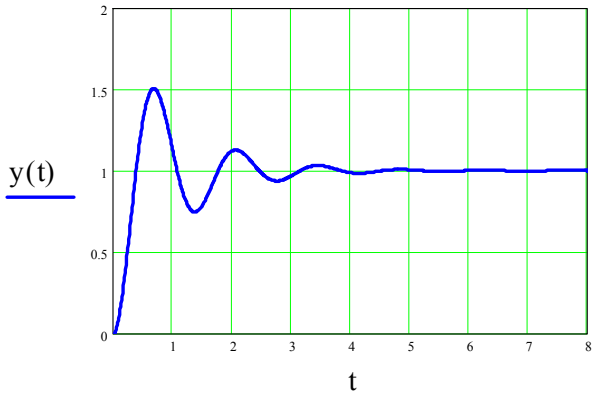


Figure 4: Transient Response ($z = 0.215$)

In Figure 4 it can be seen that the percent overshoot is PO = 50.083% and the amount of time required to get to that peak is $T_p$= 0.695 seconds. This plot also has a settling time of $T_s$=*4.018* to come within +/- 2% of its final value. The damping ratio chosen can be adjusted based on the requirements of the system. In Figure 5, the damping ratio (z = 0.10) will cause more overshoot (P.O. = 72.929%) however will have a quicker peak time ($T_p$= 0.682 seconds) and a much longer time to settle out ($T_s$ = 8.639) than in

the previous case. In Figure 6, with a damping ratio of ($z$=0.50) you can see that the overshoot is much less (P.O. = 16.309%) and requires less time to settle ($T_s$ = 1.6 seconds) however the peak time is much larger *($T_p$*= 0.725).

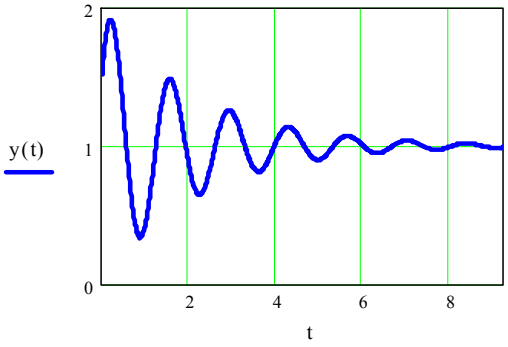


Figure 5: Transient Response (*z=0.10*)

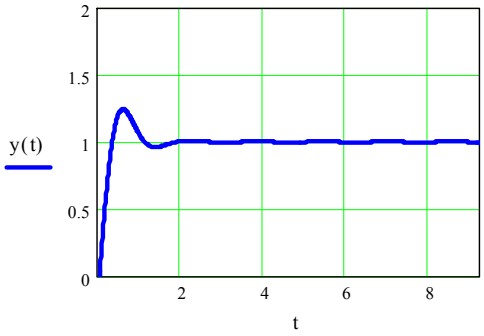


Figure 6: Transient Response (*z =0.5)*

The most important concept to take from this is that the damping ratio and the natural resonant frequency of the system will play a key role in determining the system performance. Understanding how these items can affect the system performance will help us develop a good control loop design approach.

# CHAPTER III

# IMPROVING THE CONTROL PERFORMANCE

## 3. 1 Improving the Feedback Loop

In this chapter we will begin to develop the main portion of the design process to improve the selection of feedback control parameters for DC-DC converters. We will utilize figures, flow charts, schematics, equations and graphs to support the development of this design process.

The simulation model established will be tested by utilizing the component values from an existing Core Technology, Inc. compact DC-DC converter. Since this DC-DC converter control loop has been developed using empirical methods, it will also be used as a subject to be improved with the newly created design process. In the following chapters, we compare this empirical controller design with the new controller design based upon the proposed systematic design process. Comparisons will be made in both the time domain and the frequency domain and simulation results will be compared to lab results.

To improve the empirically design controller we use the proposed design process to select feedback components then feed the values into our simulation model. Once we have improved the design using simulation, we implement the changes on the real hardware and then compare the simulations with the lab results.

### 3. 2 DC-DC Converter Technology

The targeted 200 watt DC-DC converter for control loop performance improvement was empirically developed and was based on previous knowledge and experience. The topology under consideration is a half bridge forward converter. See Figure 7, the DC-DC converter block diagram.

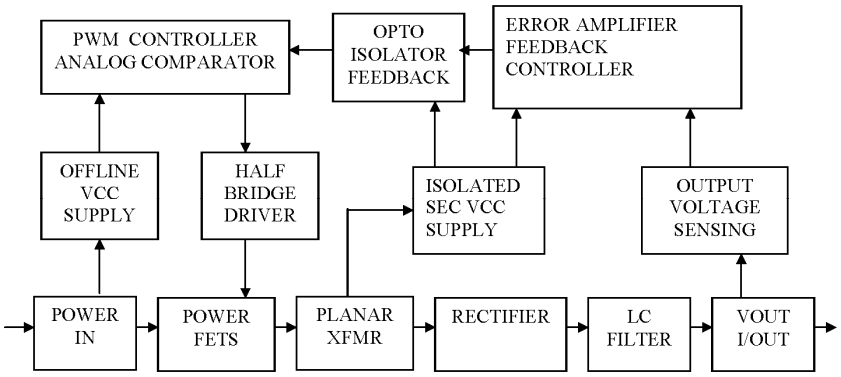


Figure 7: DC-DC Converter Block Diagram

Our task is to utilize our simulation model to compare the old and newly proposed design. We do this by inserting the component values from the empirically designed converter into our simulation tools to obtain baseline frequency and time domain responses. We can then utilize our proposed design process to obtain a new error

amplifier configuration and component values. The new error amplifier configuration and component values derived from our proposed process will be inserted into the simulation tools to determine if the design will meet our performance requirements. If so, we can build new hardware. Comparing results from the new and old designs, we can quantify our improvement.

### 3. 3 Converter Topology and Basic Operation

By evaluating the voltage control loop in the existing Core DC-DC converter we establish the motivation for developing the new design method. Obtaining lab results from this converter and comparing these results to our simulations will help us verify our model. The schematic diagram in Figure 8 and 9 can be used to describe basic converter operation. The primary power transfer occurs with the two active switches. These switches (FETs) transfer current back and forth through the main power transformer charging and discharging opposing capacitors C20 and C26. The control chip (U8) receives the $V_C$ control signal via the opto-isolator (U3) from the secondary. The primary side control chip generates a ramp signal that intersects with the $V_C$ control signal to terminate the pulse that drives the active switches. This signal that drives the active switches in an alternative fashion is called the PWM signal. This is the signal that is ultimately affected by the secondary compensation (the error amplifier) and the output voltage.

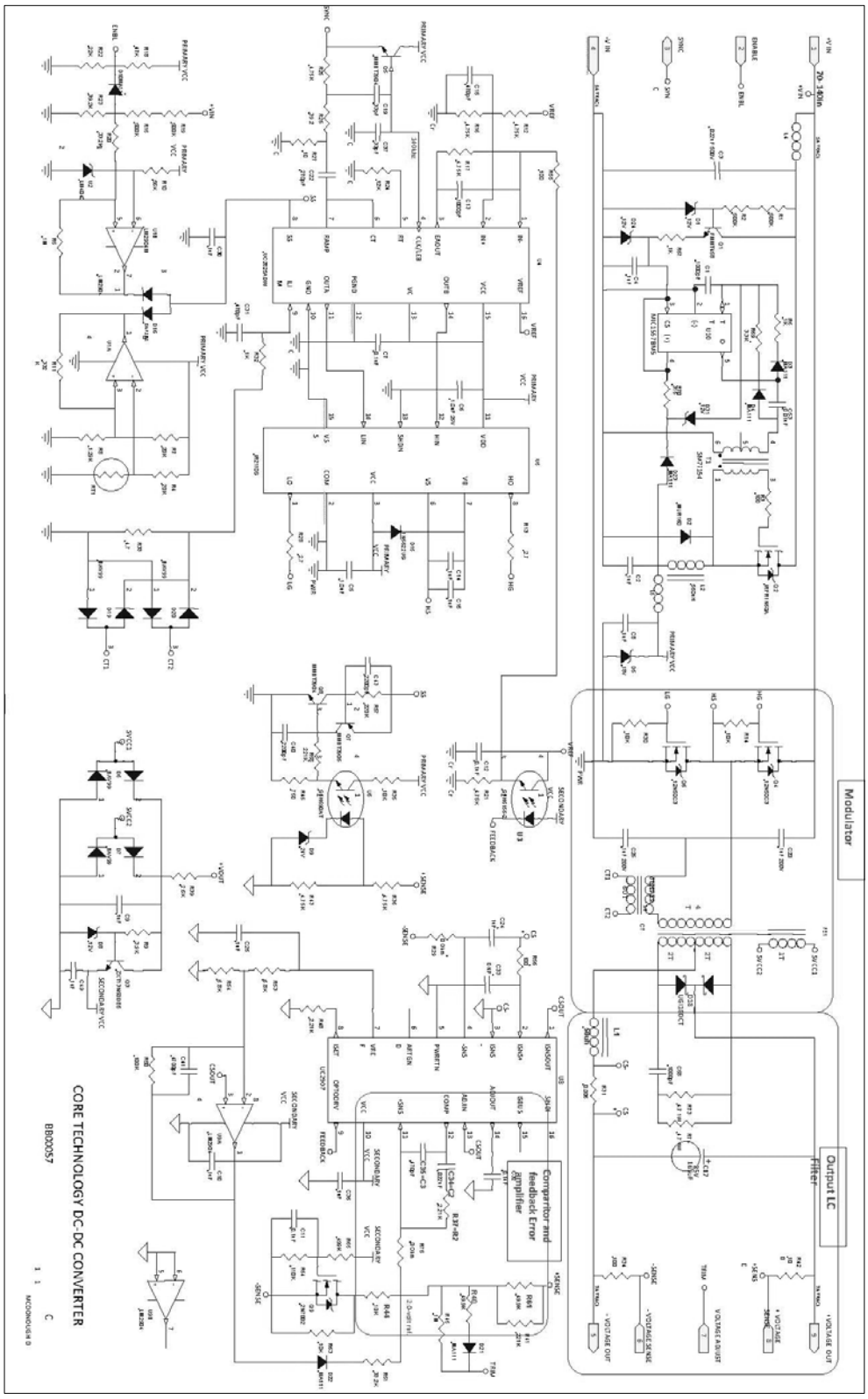


Figure 8*:* Core Technology, Inc. Unimproved DC-DC Converter Schematic

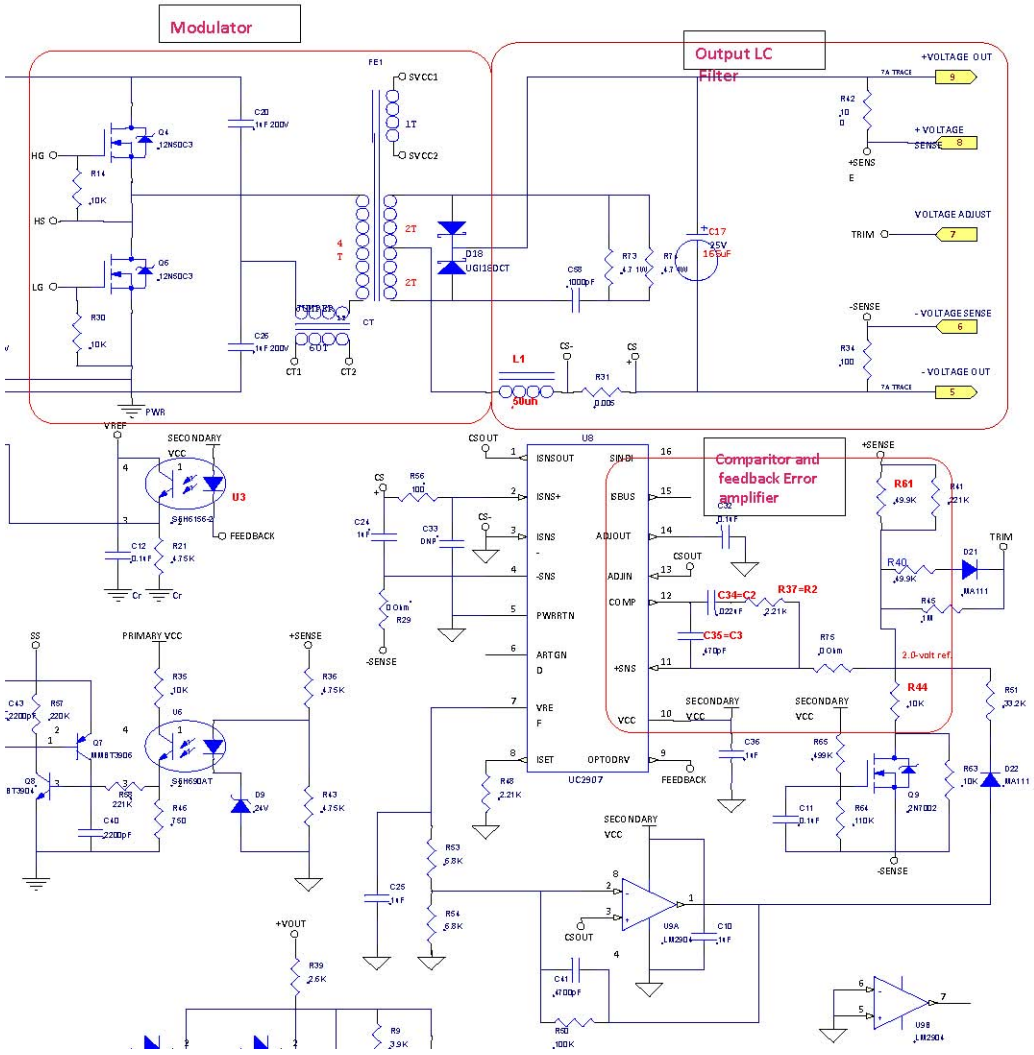


Figure 9: Unimproved LC Filter and Error Amplifier

On the secondary side, the power is transferred from the primary via the power transformer (T1) and down converted by a factor of 4 due to the center tapped secondary winding and a transformer turns ratio of 2/4 or 1/2. Once this square wave is generated on the secondary of the power transformer, it is rectified via the secondary ultra-fast

rectifiers (D18). This rectified square wave is then filtered and smoothed via the output LC (L1 and C17) filter. The remaining output ripple is highly dependent on the LC filter corner frequency and the equivalent series resistance (ESR) of the output capacitance (C17). The output voltage is divided down to establish a voltage equal to the reference into the compensating error amplifier. This will set the output voltage regulation point. This converter has an input voltage range of 70-Vdc to 140-Vdc and has an output regulation set point of 12 Vdc. The maximum output current is 16 amps.

### 3. 4 DC-DC Converter Control System

The equations to determine gain and phase margins are intended to ensure small-signal stability. In addition, these calculations are only intended to be applied to linear systems. In switch mode DC-DC converters, elements such as PWM circuitry and the effects from variations in output capacitor resistance (equivalent series resistance, ESR) are non-linear elements. We handle this problem by utilizing what we call small-signal analysis: the analysis of small perturbations around a large-signal operating point. The basic premise of our control system is that a bounded but uncontrolled source voltage is applied to the input of the system. Our system must accept this input voltage and then act to maintain a well controlled output voltage on the basis of a reference.

The difference between the output voltage measurement point and the reference produces an error voltage to be utilized by the controller to adjust the PWM signal in

order to maintain a well-regulated output voltage. The goal of the controller design is to reduce this error voltage as close to zero as possible. In addition, it is important to reduce this error quickly. With negative feedback there is an inherent trade-off between system response time and system stability. The quicker we attempt to reduce the error voltage the greater the potential for instability. Our system feedback control can be summarized in the following flow diagram of Figure 10.

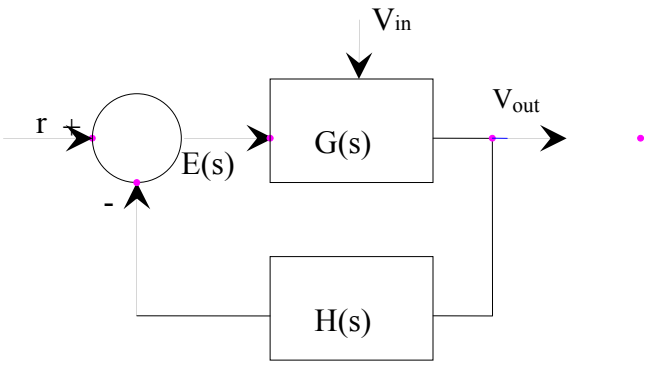


Figure 10: Basic System Feedback Control Diagram

The reference to output transfer function becomes

$$\frac{V_{out}}{r} = \frac{G(s)}{1+G(s)H(s)} \tag{3.1}$$

In the frequency range where $|G(s)H(s)| >> 1$, the transfer function is simplified as

$$\frac{V_{out}}{r} = \frac{1}{H(s)} \tag{3.2}$$

and is independent of *G(s)*. This means that the closed loop gain is independent of input supply voltage, temperature effects and component variations. It is only dependent on

*H(s)* and the accuracy of the *H(s)* parameters. In general the system should be designed so that *G(s)*>>*H*(s) and *G(s)H(s)*>>1 while still maintaining stability.

### 3. 5 Buck Converter Duty Cycle Versus Vout

Figure 11 is a standard switched mode DC-DC Buck converter [3]. The input voltage is switched via a FET (field effect transistor) at some fixed frequency and duty cycle. The switch will apply a square wave voltage to the output LC filter. The LC output filter then smoothes the output voltage which is a portion of the input voltage. The transfer function for this buck converter stage is

$$V_{out} = \frac{t_{on}}{T}(V_{in}) = V_{in}d \tag{3.3}$$

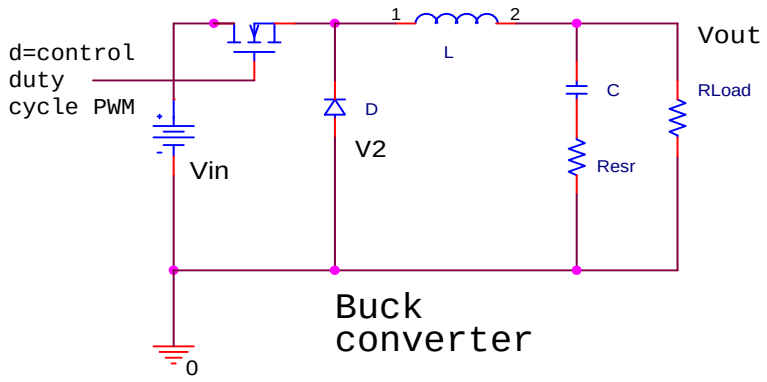


Figure 11: Buck Converter Modeling Schematic

$d = \frac{t_{on}}{T}$ is the small signal duty ratio.

The signals $V_2$ and $V_{out}$ are shown in Figure 12 and we assume the system is in the continuous conduction mode (CCM)[3] meaning that the current continuously flows through the inductor L, and does not drop to zero or less than zero. The current will flow through the inductor when the switch is closed and through the diode when the switch is open. Our analysis will be based on CCM operation because in CCM it is more difficult to achieve small-signal stability. Discontinuous mode [3] or DCM is another mode where the FET switch, the diode and the output power inductor all have zero current flowing. In this mode the control chips are designed to begin a power pulse at the beginning of each clock cycle even if the output filter inductor has zero current flowing. With inductor current at zero in discontinuous mode the system order is reduced to one, this makes the small-signal stability easier to obtain. Also, with the exception of hysteric controlled converters all other PWM type converters essentially have similar small-signal behavior.

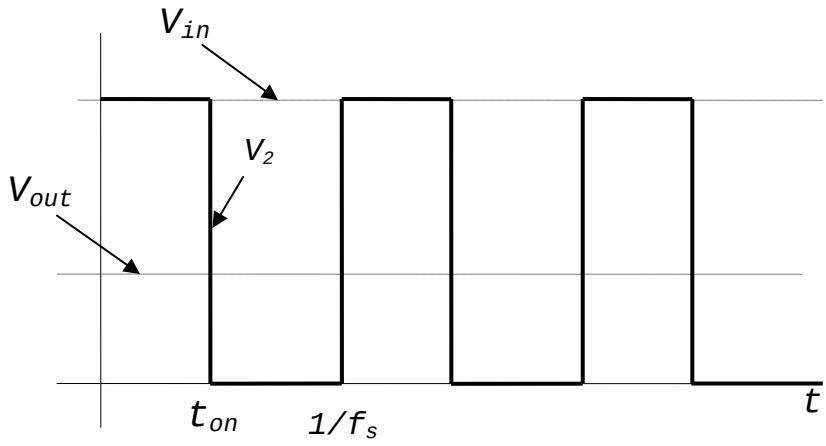


Figure 12: Timing Diagram For ON/OFF Time for Power Flow

### 3. 6 Error Amplifier and PWM Signal

With voltage mode control the PWM signal is generated as shown in Figure 13 and Figure 14. It can be seen that the width of the PWM signal is generated at the point in time where the control chip generated saw-tooth (or ramp) signal crosses the output voltage from the error amplifier. In addition, it illustrates that the ramp signal starts at zero and extends linearly to a maximum voltage $V_p$. A minimum duty cycle will result as the error signal gets very close to zero and will approach 100% width as the error signal increases to $V_p$. The duty cycle of the modulator can be determined as $\frac{V_{err}}{V_p}$. For an isolated buck converter, we reference the duty cycle to the secondary of the power transformer. The gain of the modulator is then computed as $K_{mod} = \frac{V_{out}}{V_{err}} = \frac{V_{in}}{V_p}$ and the duty cycle can be shown to be

$$d = t_{on} f_s = \frac{V_{err}}{V_p} \tag{3.4}$$

Ideally our system is completely linear and the output of the error amplifier $V_{err}$ is a DC voltage and is not affected by the ESR variation in the output capacitor. In real life there is always a slightly triangular oscillation riding on *Verr*, due to the *Resr* (in the output filter capacitor) at the converter switching frequency [12], [13]. The *Resr* can cause large signal switching instability. This is what makes the phase margin at the converter switching frequency a main issue in the controller design.

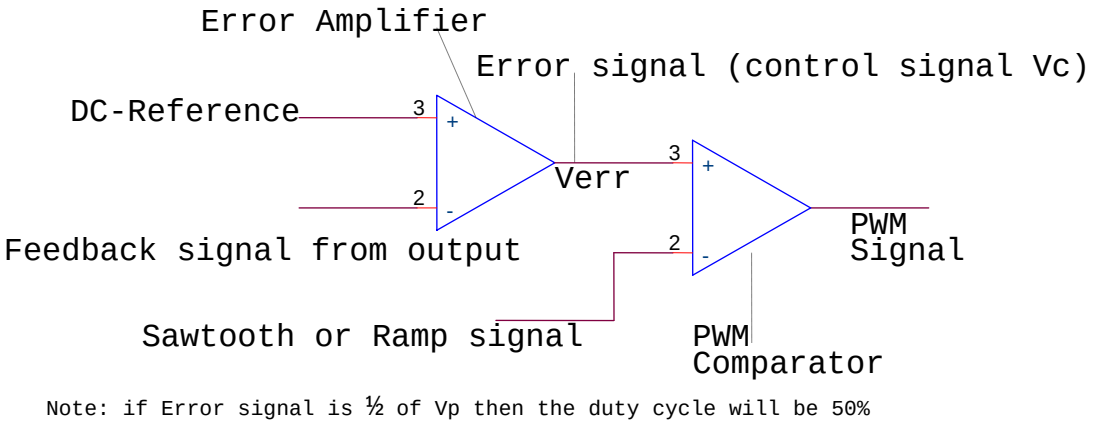


Figure 13: Error Amplifier and Comparator to Generated PWM for the FET Drive

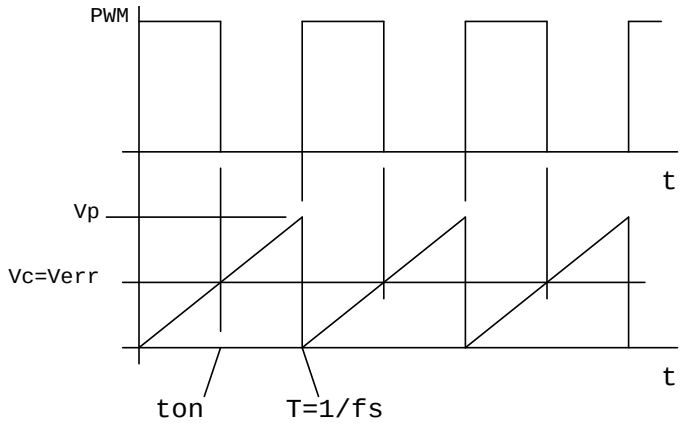


Figure 14: Ramp, Verr and Generated PWM Signals for the FET Drive

This type of oscillation caused by the output filter capacitor *Resr* is called sub-harmonic oscillations. Although the converter may regulate at the correct output voltage, these oscillations will show up riding on the output voltage. The amplitude of these oscillations will depend on the output LC filter components.

### 3. 7 Output LC Filter Characteristics and Bode Plots

Figure 15 shows an output LC filter for a buck converter. The process of deriving the transfer function and ultimately establishing frequency and time domain characteristic plots requires the use of the Laplace transform. First, the components are converted into impedances in the frequency domain. The transfer function $V_{out}/V_{in}$ will be used for the frequency response of the loaded LC filter.

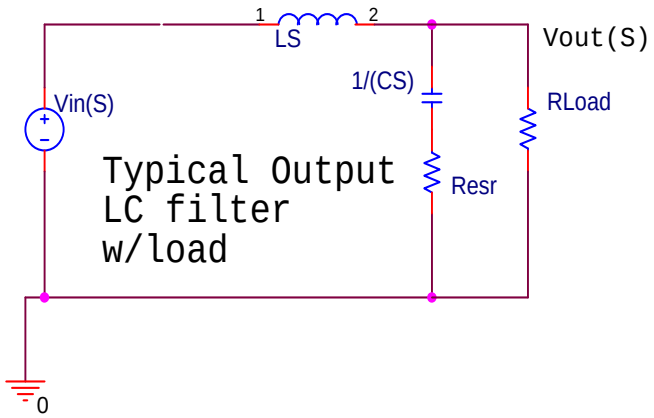


Figure 15: Output LC Filter

The following LC filter transfer function representing the open loop characteristics of our system plant can be evaluated by our model. Next we establish phase and gain plots of this portion or our control system. This equation will be needed to define the overall system loop response.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1/LC}{(s^2+\frac{s}{R_L C}+\frac{1}{LC})} \tag{3.5}$$

where $R_L = R_{LOAD.}$

The two poles of the transfer function are

$p_1 = -\alpha + j\omega,\ and\ p_2 = -\alpha - j\omega$ where

$\alpha = \frac{1}{2R_L C}$ , $j = \sqrt{-1}$ (3.6)

For these types of filters (lightly damped), $\omega_d = \sqrt{(\frac{1}{LC})} - \alpha^2$. However, for the natural resonant (peak) frequency we can use the approximation of

$$\omega_d = \sqrt{(\frac{1}{LC})} \quad (3.7)$$

If $s = j\omega$ , we see that the transfer function contains complex numbers and will have a real part and an imaginary part. The amplitude of the complex number is the square root of the sum of the squares of the real and imaginary parts. In addition, the phase is the inverse tangent of the ratio of the imaginary part to the real part. This transfer function can be described in terms of magnitude and phase as a function of frequency. We do this by plotting the gain in dB and the phase in degrees versus the log of frequency. These are, of course, the Bode plots and allow easy visualization of the system characteristics as they relate to system stability.

From the derived transfer function the following can be determined: the gain is equal to one and the phase is zero for $\omega$ much less than $\sqrt{1/(LC)}$ and the gain will be equal to $R_L\sqrt{C/L}$ while the phase is equal to 90° for $\omega = \sqrt{1/(LC)}$ (the resonant peak

frequency). The gain slope is equal to $-1/(\omega^2 LC)$ and the phase is -180° for ω much greater than $\sqrt{1/(LC)}$.

### 3. 8 The Bode Plots

The Bode plots in Figure 16 are of the output LC shown in Figure 15 and described by Equation 3.5. They contain values $R_L$=0.75 ohms, $C$=165 μf, $L$=50 μh.

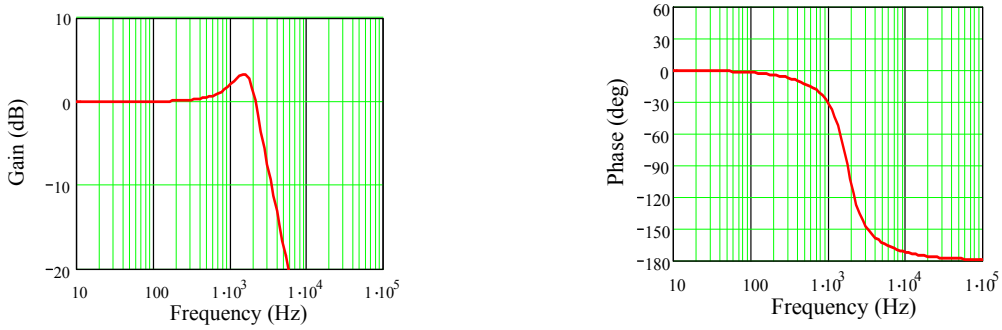


Figure 16: Phase and Gain Plots (Open Loop Plant)

The gain of the LC filter is unity at low frequencies and contains a resonant peak at $f = f_{peak}$ =1.75 KHz. The slope becomes -40 dB per decade (called a -2 slope because it is proportional to $\frac{1}{\omega^2}$ ). The phase changes from zero to -180° in two decades starting at approximately one decade prior to the resonant peak change to -180° at approximately one decade after the resonant peak.

### 3. 9 The Linear Time Invariant Representation

Shown in Figure 17 and 18 is the PWM (pulse width modulation) switch model similar to the model of a BJT (bipolar junction transistor). Note that the active devices (FETs) of the DC-DC converter are discontinuous in their operation. In order to use frequency domain techniques to investigate stability, transient response, settling time and external load disturbances, the averaging method is used. [3] [7],[13],[12] By analyzing the system in this way, we can evaluate DC-DC converter control loop performance based on its Bode plots. We can use the averaging technique for switching power converters because the switching rate is very fast with respect to the rate of change of other system variables. This method gives excellent accuracy providing the system bandwidth is 1/10 of the converter switching frequency and it works fairly well up to 1/3 of the switching frequency. Of course it can be used up to the 1/2 the switching frequency and this would be the theoretical limit due to the Nyquist sampling criterion. [1], [2], [6] [9]

The linear time invariant PWM model allows us to ignore the nonlinear dynamics in describing the relationship between the average terminal voltage and currents. The schematic of Figure 17 shows the two modes of operation: Mode-1 when the switch (FET) is closed (for time DT) and Mode-2 when the switch is open (for time (1-D)T. Later we combine these two modes and replace the active devices with a DC-transformer containing a turns-ratio representing the duty cycle or duty ratio D. For our purposes this theoretical transformer can pass both DC and AC voltage.

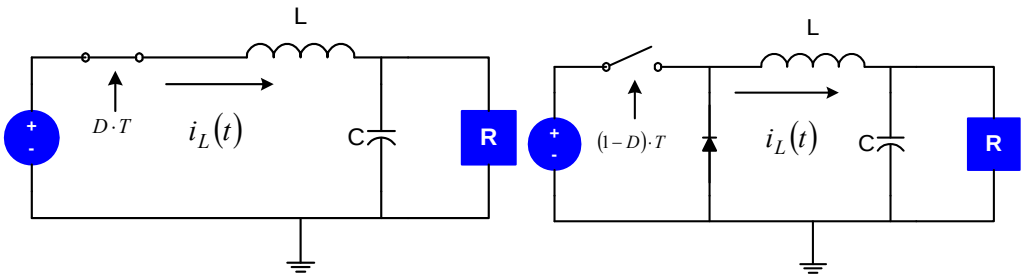


Figure 17: Switched model Illustrating Mode 1 and 2

Figure 18 illustrates the buck topology under consideration and defines the terminals of the PWM switch model, a (active), p (passive) and c (common).

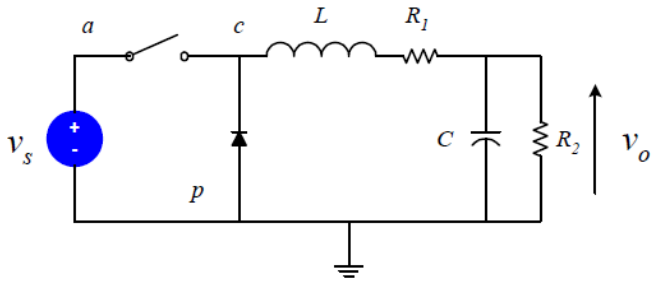


Figure 18: Buck Topology Illustrating PWM Switched Model for Averaging Waveforms

With a simple equivalent circuit model of the PWM switch as shown in Figure 19, we can now represent the relationship between the average terminal values (considered as DC) and the small-signal perturbations (considered ac) affecting the system. We are able to do this because in our model they are extremely small with respect to the averaged or DC values due to the system's inability to change much during one or even several duty cycles. Because the changes are so small, we can remove the non-linear small signal perturbations by ignoring the products of any two small signal variables. The PWM switch model can be used with any topology because the following terminal currents and

voltages largely remain invariant. The instantaneous currents $i_a(t)$ and $i_c(t)$ and the instantaneous terminal voltages $v_{ap}(t)$ and $v_{cp}(t)$, are shown in Figure 19. Also, the averaged current in the active terminal $i_a$ is related to the averaged current in the common terminal $i_c$ by a simple relationship where *d(t)(same as d)* is the instantaneous change in the duty cycle represented in Equation 3.8. We can drop the time function notation for simplicity, however the time dependent nature of these expressions is understood. In addition, $\hat{d}$ is the ac or small signal perturbation or the small change in the average duty ratio $D$ and requires $\left(\widehat{d}/D\right) \ll 1$. Therefore $d$ can be used to determine the average current $i_a$ shown in Equation 3.9 and the average terminal voltages show in Equation 3.10.

$$d(t) = D + \hat{d} \tag{3.8}$$

$$i_a = d i_c \tag{3.9}$$

$$v_{cp} = d v_{ap} \tag{3.10}$$

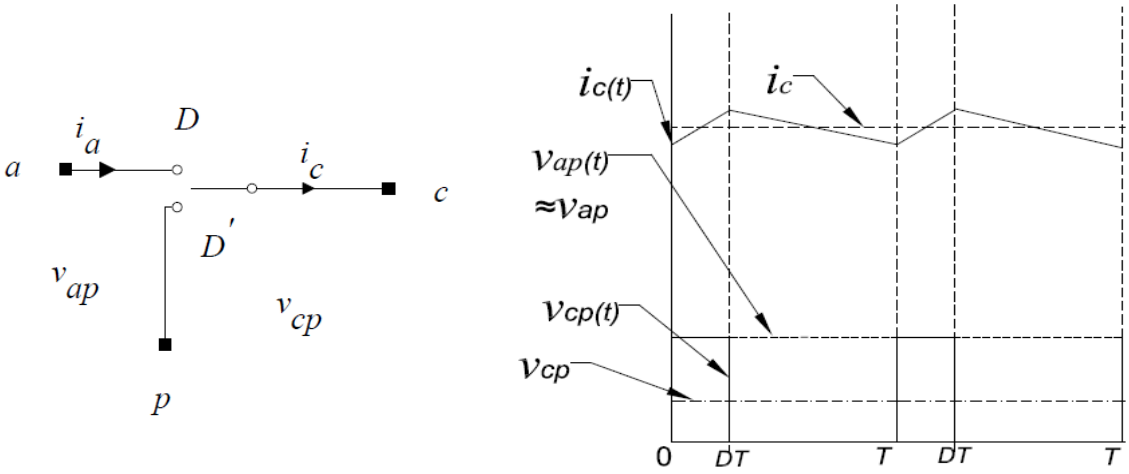


Figure 19: PWM Switch Model and Corresponding Averaged Waveforms

In the signal diagram of Figure 19 the average current is represented by $i_c$ while the actual instantaneous current is shown as $i_c(t)$. The same notation is used for $v_{ap}$ and $v_{cp}$. The instantaneous terminal voltages always have the same shape.

All terminal voltages are also perturbed in this manner.

$$v_{ap} = V_{ap} + \hat{v}_{ap} \tag{3.11}$$

$$v_{cp} = V_{cp} + \hat{v}_{cp} \tag{3.12}$$

Using the perturbations representation as described above it follows that

$(V_{ap} + \hat{v}_{ap}) = (\hat{v}_{cp} + V_{ap} D)/(D + \hat{d})$ (Note: $V_{cp} = V_{ap} D$)

$$(V_{ap} + \hat{v}_{ap})(D + \hat{d}) = V_{ap} D + \hat{v}_{cp}$$

$$\hat{v}_{ap} D + \hat{v}_{ap}\hat{d} + V_{ap}\hat{d} + V_{ap} D = V_{ap} D + \hat{v}_{cp}$$

Since $V_{cp} = DV_{ap}$ and ignoring the product of any two small signal perturbations (or the second order effects) such as $\hat{v}_{ap}\hat{d}$ it follows that

$$\hat{v}_{ap} D = \hat{v}_{cp} - V_{ap}\hat{d}$$

$$\hat{v}_{ap} = \hat{v}_{cp}/D - V_{ap}\hat{d}/D \tag{3.13}$$

By performing the same process on the current we obtain

$$\hat{\imath}_a = I_c \hat{d} + D\,\hat{\imath}_c \tag{3.14}$$

### 3.9.1 Averaged Model

Figure 20 shows the averaged switched circuit model [7],[3] and illustrates the DC-transformer schematically after combining the two switched conditions. The duty cycle variable *d* represents the turn ratio of the hypothetical DC transformer. With this model the primary current becomes $I_L d$ and the secondary voltage is $V_i d$. This DC transformer will allow us to create the averaged continuous model.

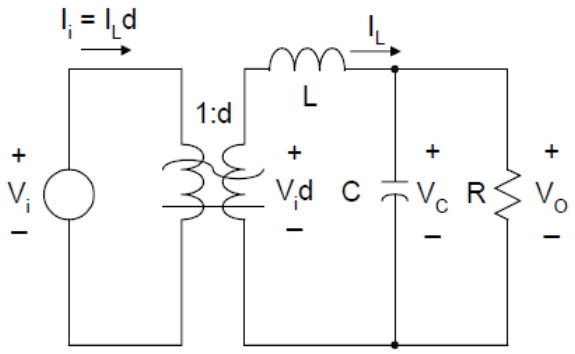


Figure 20: Resulting Averaged Model

Neglect the hat or second order terms due to their insignificance

$v_i = V_i + \hat{v}_i, \quad i_L = I_L + \hat{\imath}_L, \quad d = D + \hat{d}$ then

$$v_i d \approx (V_i + \hat{v}_i)(D + \hat{d}) = V_i D + V_i \hat{d} + \hat{v}_i D + \hat{v}_i \hat{d} \approx V_i D + V_i \hat{d} + \hat{v}_i D \qquad (3.15)$$

because $\hat{v}_i \hat{d}$ is negligible. From Figure 21 and Equation 3.15, it can be shown that the product of $v_i d$ is linearized about the operating point, $V_i D$

### 3.9.2 The Linear Model

As previously described, to obtain a linear model we need to define the small signal parameters based on a large signal operating point [3], [7]. Mathematically this linearization involves separating each variable into its DC and AC components. In the linearized model of Figure 21 we can see the averaged duty cycle being used along with the addition of the primary incremental change in current in $I_L\hat{d}$ and the incremental change in voltage on the secondary $V_i\hat{d}$. Because our equations will contain the product of two small signal variables, the system will still have some non-linearity. However, as previously mentioned we can ignore the products of any two small signal variables because they are extremely small with respect to our averaged operating points. In general, the linear approximations work well as long as the small signal amplitudes are small enough not to "rail" the duty cycle full-on or full-off for multiple cycles.

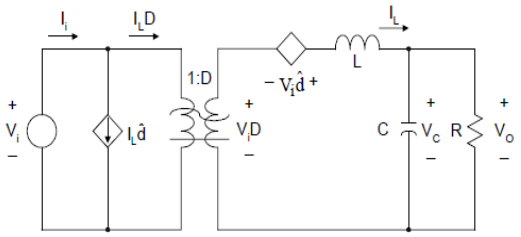


Figure 21: The Linearized Model of a Buck Converter

If we apply the generalized control law to the linearized power [3], [7], [12] circuit in Figure 22 a flow diagram can be derived. This flow diagram will help illustrate how $\hat{d}(s)$, the transformed control variable, varies as a function of converter elements affecting the control loop.

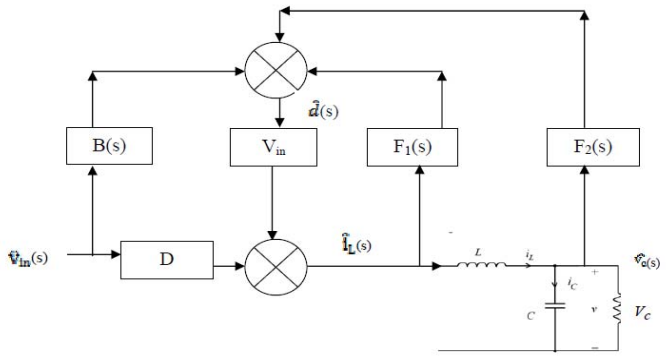


Figure 22: Generalized System Configuration for the Time Invariant Model

From the flow diagram in Figure 22 it can be seen that the inductor current, output voltage, and the input voltage variables can each affect the system control variable $\hat{d}(s)$.

$$\hat{d}(s)=-F_1(s)\,\hat{i}_L(s)-F_2(s)\,\hat{v}_c(s)+B(s)\,\hat{v}_{in}(s) \qquad (3.16)$$

For purposes of completeness, feed forward control is also shown. However, it will not be used in our analysis of the voltage mode control. In Figure 23 we show the complete buck converter flow diagram and eliminate the items which do not contribute to the voltage mode control.

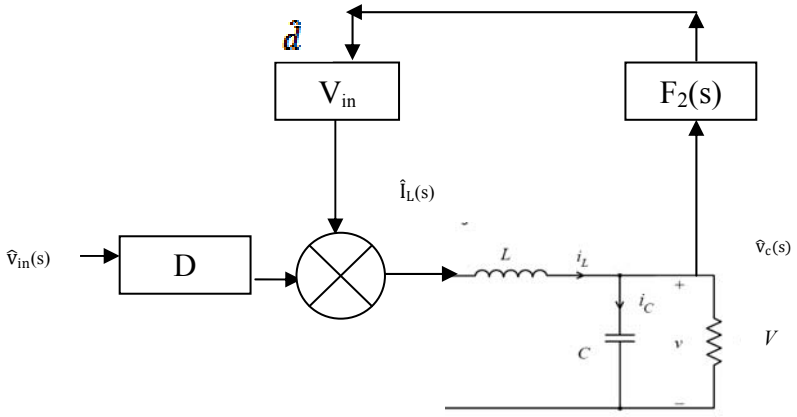


Figure 23: Voltage Mode Control Flow Diagram

For voltage mode control $F_1(s)\ \hat{i}_L(s) = 0$, $B(s)\ \hat{v}_{in}(s) = 0$, and $F_2(s) = \frac{K(s)}{V_p}$. Therefore the system open loop transfer function can be defined as

$$\hat{d}(s) = -F_2(s)\,\hat{v}_c(s) \tag{3.17}$$

A more detailed flow diagram which can illustrate the individual components within the control loop can be seen in Figure 24. Included are the values within the functional blocks in order to help describe how each part of the system affects the control signal.

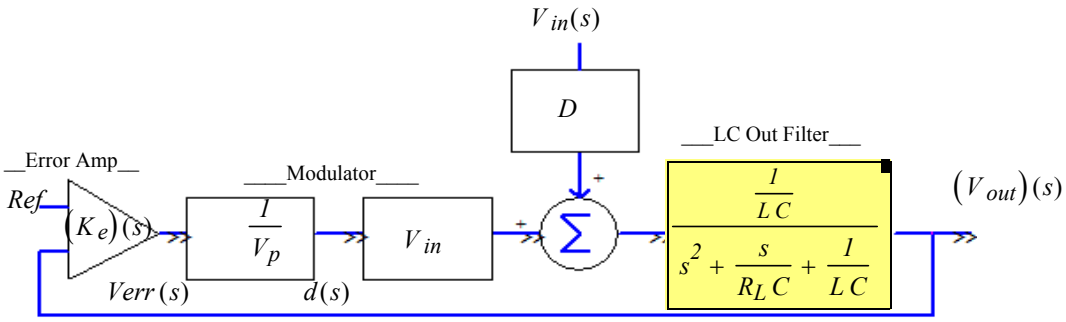


Figure 24: Generalized Control Law from Time Invariant Model

The overall open-loop gain is the product of the individual gains around the control loop of the system (the error amplifier, the modulator, etc.). That is

$$G(s)H(s) = \frac{\frac{V_{in}K(s)}{V_p LC}}{s^2 + \frac{s}{R_L C} + \frac{1}{LC}} \tag{3.18}$$

Equation 3.18 illustrates the basic DC-DC buck converter system's transfer function. It is important to note that this transfer function is independent of the duty cycle $D$ and is dependent on the DC input voltage $V_{in}$. Thus the open loop gain function is dependent on the DC operating point. Another interesting point is that the output load resistance shows up in the second term of the denominator. It would seem that if the load resistance goes to infinity, the system would become unstable, but as previously discussed; the DC converter will go into DCM discontinuous mode. When this occurs, the system will become a first order system and becomes easier to stabilize. Additionally, the error amplifier negative feedback causes an inherent -180° phase shift and can cause our system to go unstable at 180° rather than 360°. It is for this reason that we review the gain margin at the -180° point on the Bode plots.

### 3. 10 Open Loop Phase and Gain Margin of the Buck Converter

In the following example we will use real world values chosen from a generic design similar to the design under consideration. These values are shown in Table II below and we use them to obtain the gain and phase plots. We can insert them into the open loop transfer function and use this function to derive the Bode plots so we may obtain the gain and phase margin.

TABLE II: GENERIC DESIGN COMPONENT PARAMETERS

| ***Variable = Value*** | ***Variable = Value*** |
|---|---|
| $V_P = 2\ Volts$ | $C = 540\ uf$ |
| $R_L = 0.5\ Ohms$ | $L = 16\ uf$ |
| $f_s = 100\ KHz$ | $V_{in} = 12\ Volts$ |
| $K_{err} = 5.6$ | $s = j2\pi f$ |
| $K(s) = R_2/R_1$ | $G(s)H(s) = \dfrac{\frac{V_{in}K(s)}{V_p LC}}{s^2 + \frac{s}{R_L C} + \frac{1}{LC}}$ |

Figure 25 shows the phase and gain plots from our generic DC-DC converter.

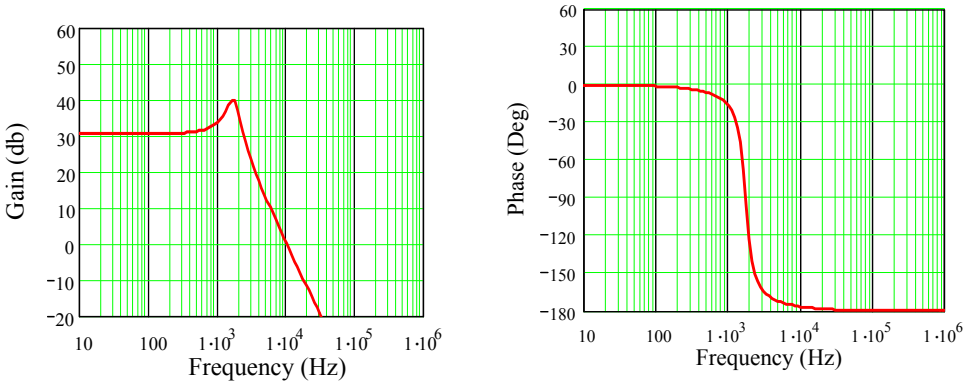


Figure 25: Phase and Gain Plots

Our example shown in Figure 25 is close to being unstable with at best 5° of phase margin which is not acceptable. We will use these tools (Bode plots) to define the robustness of the control loop.

### 3. 11 Frequency Compensation and Circuit Implementation

The system we have just analyzed in the previous plots would be viewed as nearly unstable due to the lack of phase margin at the crossover frequency. In this case, the system would experience a lot of ringing under any external disturbance.

Obviously we need to provide some frequency compensation. We will now shape the open loop transfer function to provide adequate gain and phase margins to ensure a stable system with good transient response. This is accomplished by applying a lead, a lag, or a Lead-lag network to the error amplifier. Determining the proper network and components within that network is our challenge. In the next section, we describe each compensation network in order to help us determine how to apply them.

#### 3.11.1 Lag Compensation

Based on the initial run of the phase and gain plots we need to reduce the gain at lower frequencies so when the system loop reaches the unity gain point there will be a phase margin of at least 45°. This is achieved by rolling off the gain of the error amplifier with local feedback around the error amp as shown in Figure 26. With the addition of $C_2$ we now have the amplifier gain of

$$K(s) = \frac{-V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1(1+R_2C_2s)} \tag{3.19}$$

This allows the same DC gain; however, we add a pole at frequency

$$\omega_p = 1/(R_2C_2) \tag{3.20}$$

As previously discussed this single pole compensation method is called lag compensation [2],[3],[11],[12],[15]. This causes the phase shift to change from zero degrees at 1/10 of the corner frequency to -90° at 10 times the corner frequency. Shown in Figure 27 is the lag compensated error amplifier.

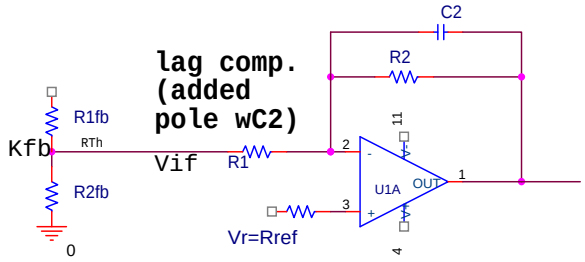


Figure 26: Lag Compensated Error Amp

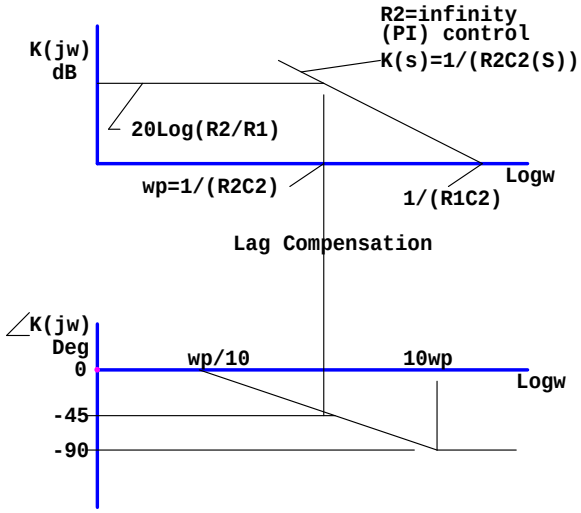


Figure 27: Error Amp Lag Compensated Phase and Gain

The amplitude of the compensated error amplifier gain in dB will add to the amplitude of the control loop. The error amplifier phase adds to the overall phase lag. The phase lag compensation becomes a proportional integral control with $R_2=\infty$.

We now use straight line approximations [3],[12],[15] of the transfer function to gain insight and to pick the filter components. The lag compensating straight line transfer function (Equation 3.21) dictates the value of the gain below the resonant frequency and produces a negative slope of 20 dB per decade.

$$\frac{V_{in}}{\left(2\pi \cdot f \cdot V_p \cdot R_1 \cdot C_2\right)} \tag{3.21}$$

Beyond the resonant peak Equation 3.22 defines the shape of the gain plot and produces a negative slope of 40 dB per decade.

$$\frac{V_{in}}{\left(2\pi \cdot f\right)^3 \cdot V_p \cdot R_1 \cdot C_2 \cdot L \cdot C} \tag{3.22}$$

The resonant frequency where the gain will peak is

$$G_{fpk} = \frac{V_{in}}{2\pi f V_p R_1 C_2}\ R_L\sqrt{C/L)} \tag{3.23}$$

At a particular frequency (the resonant frequency) the output filter capacitor and inductor reactances are equal in magnitude but opposite in sign and exhibit minimum impedance. This is common for series LC circuits. When this occurs we call this the resonant frequency.

To achieve a 6 dB gain margin at $f_{pk}$=*1.71 KHz* we can set the gain at the peak point ($G_{fpk}$) equal to ½ yielding a $R_1C_2$ product of (.00324). We then pick $R_1 = 167$K ohms and $C_2 = 0.02\ uf$ to make $R_1C_2$ product close to (.00324),

$$R_1C_2 = \frac{V_{in}}{2\pi f V_p(G_{fpk})} R_L\sqrt{C/L)} \tag{3.24}$$

resulting in $R_1C_2 = 3.24x10^{-3}$.

The unity gain crossover frequency has been reduced and will now be less than 300 Hz which is about an order of magnitude below the resonant frequency. It is important to note that the gain margin of 6 dB was based on the resonant peak. The resonant peak is dependent on the output load value. So, if we were to decrease the load, this would also decrease the gain margin. We could use the smallest load before the converter would go into the discontinuous mode. While the phase margin would be -90°, the dominant pole has reduced the system bandwidth to a point where the transient response would be very poor. In addition, the low frequency gain has been reduced. The lag compensator contributed -90° phase shift. The output LC filter contributes another

-180° of phase shift. Equation 3.25 can be used to establish the phase and gain plot illustrating the characteristics of the lag network. This transfer function appears to be like the previous *OLG* transfer function. However, it contains the addition of $C_2$ in the $K_e(s)$ term.

$$OLG(s) = \frac{\frac{V_{in}\cdot K_e(s)}{V_p\cdot L\cdot C}}{(s)^2 + \frac{s}{R_L\cdot C} + \frac{1}{L\cdot C}} \tag{3.25}$$

Table III shows the values utilized for the Lag compensation error amplifier. Figure 28 and Figure 29 illustrate the resulting phase and gain margin. For a 6 dB gain in margin at the resonant peak we can set the $G_{fpk}$=0.5. As mentioned before we do this to obtain an $R_1C_2$ product.

TABLE III: LAG DESIGN COMPONENT PARAMETERS

| ***Variable = Value*** | ***Variable = Value*** |
|---|---|
| $V_P = 2\ Volts$ | $C = 540\ uf$ |
| $R_L = 0.5\ Ohms$ | $L = 16\ uf$ |
| $f_s = 100\ KHz$ | $V_{in} = 12\ Volts$ |
| $K_{err} = 5.6$ | $C_2 = 0.021\ uf$ |
| $G_{Rpeak} = 1.713\ KHz$ | |
| $R_{ampOL} = 1E9\ Ohms$ | $R_1 = 167K\ Ohms$ |
| $s = j2\pi f$ | $V_{out} = 5\ Volts$ |
| $K(s) = \frac{R_2}{\left[R_1 \cdot \left(1 + R_2 \cdot C_2 \cdot s\right)\right]}$ | $OLG(s) = \frac{\frac{V_{in} \cdot K_e(s)}{V_p \cdot L \cdot C}}{(s)^2 + \frac{s}{R_L \cdot C} + \frac{1}{L \cdot C}}$ |

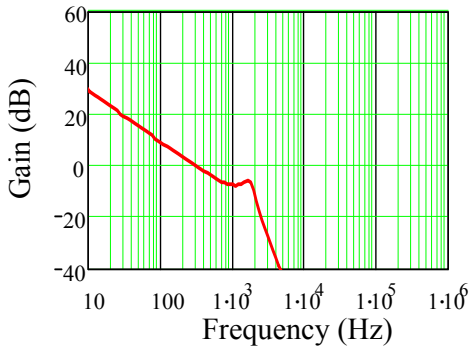


Figure 28: Lag Compensated Gain Plot

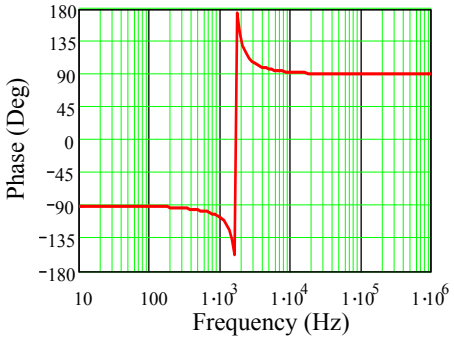


Figure 29: Lag Compensated Phase Plot

In Figures 28 and 29 it can be seen that the lag compensation has moved the unity gain point to a lower frequency allowing a phase margin of approximately 90°. However, the DC gain could be higher as well as the gain margin (approximately 5 dB) where the phase approaches 180° is not acceptable based on our criteria for our stable system. We can now explore the lead compensation network.

### 3.11.2 Lead Compensation

Using a lead network [2],[3],[11],[12],[15] is another method of compensation. We can increase the phase by adding a lead capacitor $C_1$ in parallel with the input resistor (on the negative terminal) of the error amp (see Figure 30). This will introduce a zero into the system transfer function. The addition of the lead capacitor will increase the gain; however, if we set the break frequency $f_{brk}=1/(R_1C_1)$ of the zero to be the same as the crossover frequency, we can increase the phase margin by 45°. It is important to note that pure lead compensation is physically unrealizable since the gain cannot continue to rise indefinitely due to the limitations in the open loop amplifier gain bandwidth. Obviously the gain-bandwidth of the operational amplifier used with lead compensation must be much higher than that required for lag compensation. The following is the transfer function for the lead compensated error amplifier.

$$K_e(s) = \frac{R_2 \cdot (1 + R_1 \cdot C_1 \cdot s)}{R_1} \tag{3.26}$$

$C_1$ is determined from $C_1 = \frac{1}{(\omega_z \cdot R_1)}$ where $\omega_z$ is the break frequency.

Figure 30 and 31 illustrate how the addition of $C_1$ increases the system gain at higher frequencies.

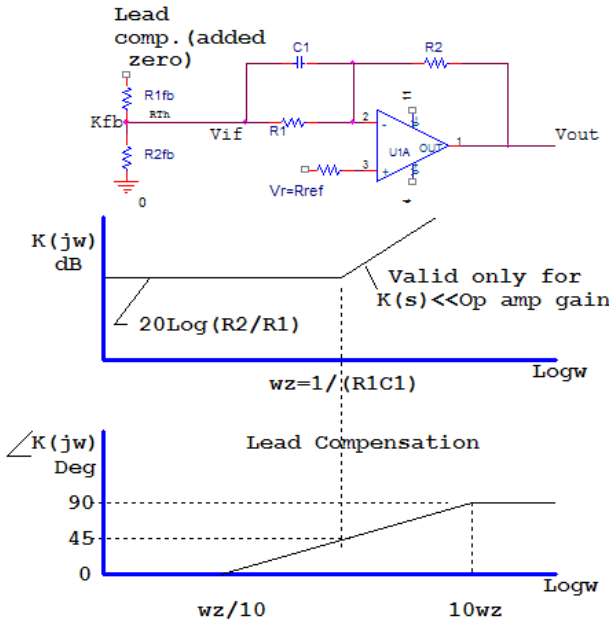


Figure 30: Lead Compensated Error Amp with Phase and Gain Diagram

Table IV shows the values derived in the lead compensator and the corresponding effects on the Bode plots.

TABLE IV: LEAD DESIGN COMPONENT PARAMETERS

| Component | Value |
|---|---|
| $V_P = 2\ Volts$ | $C = 540\ uf$ |
| $R_L = 0.5\ Ohms$ | $L = 16\ uf$ |
| $f_s = 100\ KHz$ | $V_{in} = 12\ Volts$ |
| $K_{err} = 5.6$ | $C_2 = 0.021\ uf$ |
| $G_{Rpeak} = 1.713\ KHz$ | $C_1 = 58.8\ nf$ |
| $R_{ampOL} = 1E9\ Ohms$ | $R_1 = 167\ KOhms$ |
| $s = j2\pi f$ | $V_{out} = 5\ Volts$ |
| $K_e(s) = \frac{R_2 \cdot (1 + R_1 \cdot C_1 \cdot s)}{R_1}$ | $OLG(s) = \frac{\frac{V_{in} \cdot K_e(s)}{V_p \cdot L \cdot C}}{(s)^2 + \frac{s}{R_L \cdot C} + \frac{1}{L \cdot C}}$ |

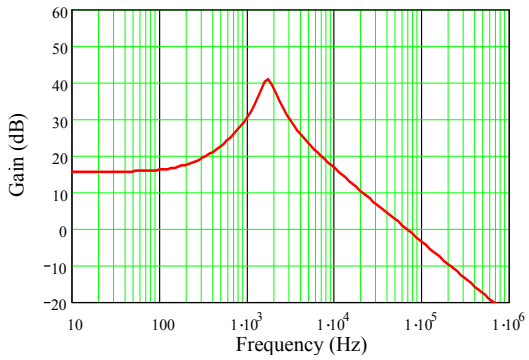


Figure 31: Lead Compensated Gain

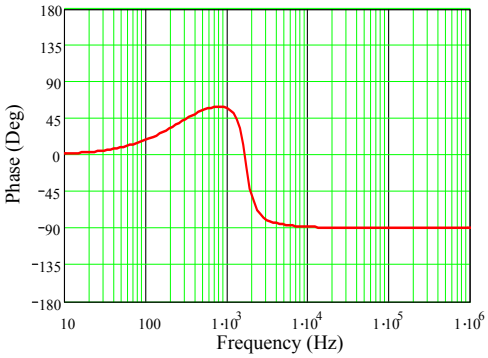


Figure 32: Lead Compensated Phase

It can be seen from Figure 31 that the lead compensation has increased the gain at the higher frequencies. However, the problem here is that the DC gain dropped dramatically. We get the benefit of higher gain at the higher frequency but there is a consequence of low DC gain, which can cause DC error. Combining the lead and the lag compensation, we can obtain the benefits of both as shown in the following section.

### 3.11.3 Lead-lag Compensation

It is possible to combine both lead and lag networks to achieve better performance. The goal with the this type of compensation [2],[3],[11],[12],[15] is to achieve low DC error and high bandwidth for a quick responding system. The new error amplifier configuration is shown in Figure 33. This configuration shows the insertion of one capacitor $C_1$ in parallel with the input resistor while inserting another capacitor $C_2$ in series with the feedback resistor $R_2$. By shaping the frequency characteristics of the error

amplifier in this manner we can achieve high gain at low frequencies and provide acceptable phase margin at the crossover point.

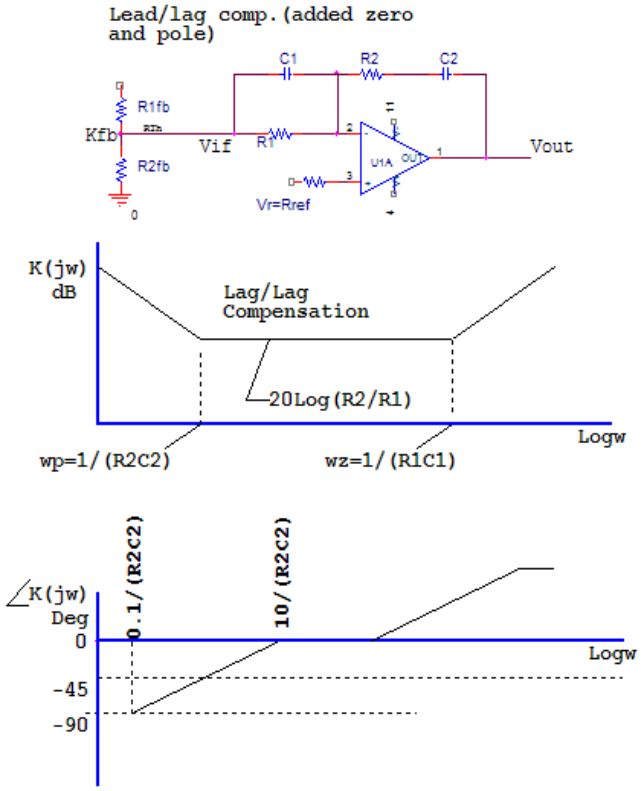


Figure 33: Lead-lag Compensated Error Amp with Phase and Gain Diagram

The Lead-lag error amplifier gain is:

$$K_e(s) = \frac{\left(\frac{1}{C_2 \cdot s} + R_2\right)}{\left(\frac{\frac{1}{C_1 \cdot s} R_1}{\frac{1}{C_1 \cdot s} + R_1}\right)} \tag{3.27}$$

Table V shows the values used in order to derive the Bode plots.

TABLE V: LEAD-LAG DESIGN COMPONENT PARAMETERS

| Component | Value |
|---|---|
| $V_P = 2\ Volts$ | $C = 540\ uf$ |
| $R_L = 0.5\ Ohms$ | $L = 16\ uf$ |
| $f_s = 100\ KHz$ | $V_{in} = 12\ Volts$ |
| $K_{err} = 5.6$ | $C_2 = 0.021\ uf$ |
| $G_{Rpeak} = 1.713\ KHz$ | $C_1 = 15\ pf$ |
| $R_{ampOL} = 1E9\ Ohms$ | $R_1 = 10.5K\ Ohms$ |
| $s = j2\pi f$ | $R_2 = 59K\ Ohms$ |
| $K_e(s) = \dfrac{\left(\dfrac{1}{C_2 \cdot s} + R_2\right)}{\left(\dfrac{\dfrac{1}{C_1 \cdot s} R_1}{\dfrac{1}{C_1 \cdot s} + R_1}\right)}$ | $OLG(s) = \dfrac{\dfrac{V_{in} \cdot K_e(s)}{V_p \cdot L \cdot C}}{(s)^2 + \dfrac{s}{R_L \cdot C} + \dfrac{1}{L \cdot C}}$ |

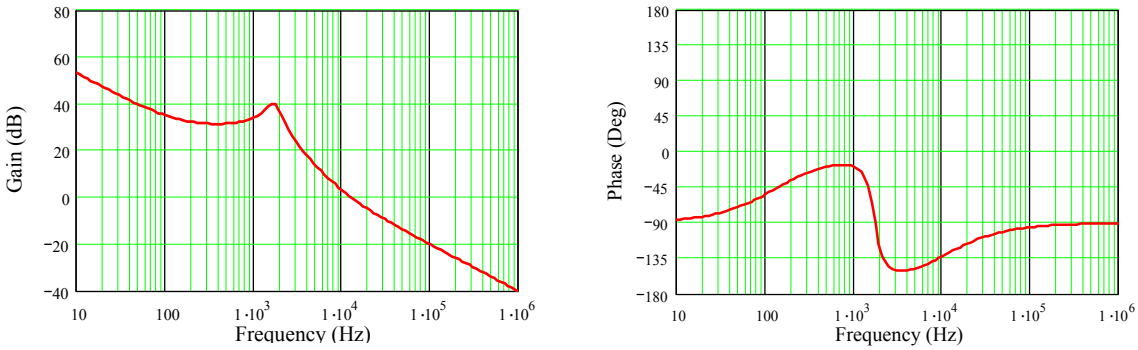


Figure 34: Error Amp Lead-lag Compensated Phase and Gain Plots

It is shown in Figure 34 that we can obtain a substantial improvement with this type of Lead-lag compensation network. As shown, at the crossover frequency we have obtained 45° of phase margin. This meets our criteria for a very stable control loop. In

addition we have obtained excellent gain (approximately 55 dB) at low frequency reducing the possibility of DC error that may have occurred with a non-compensated (approximately 30 dB gain at DC) or a lead only compensated (approximately 20 dB gain at DC) system. This is extremely important because this analysis has shown that by combining the networks we can improve system performance with the addition of only two capacitors to the error amplifier.

### 3. 12 Straight Line Approximation with Lead-lag Compensation

Figure 35 shows a straight-line approximation of the open loop gain plot illustrating a few critical points of the DC-DC converter. The Lead-lag components contained within the system feedback loop are included in the plot.

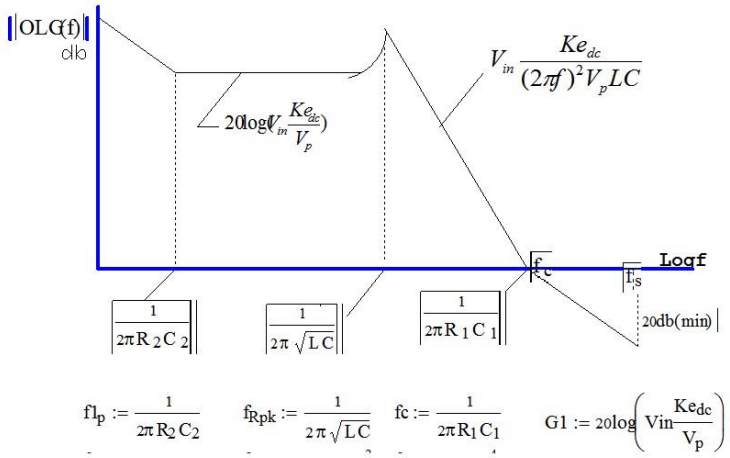


Figure 35: Straight Line Approximations of Open Loop Gain Equations

It can be seen from the above diagram at the lower frequency that $V_{in}(K_e/V_{p)}$ dictates the shape of the gain plot. At the higher frequencies $V_{in}/((2\pi f)^2 V_p LC)$ dictates the shape of the gain plot by producing a negative slope of -40 dB/decade. At the resonant frequency the gain will peak and is defined by

$$G_{fpk} = V_{in} \frac{K_{err}}{V_{in}} (R_L \sqrt{C/L}) \tag{3.28}$$

A commonly used rule of thumb is, the slope of the gain response as it crosses the unity-gain (0 dB) axis is not more the 20 dB per decade (-6 dB per octave), and the phase margin should be greater than or equal to 45°. Also, the recommended gain margin should be (-6 dB to 12 dB) as the phase reaches 180°. Finally a recommended phase margin of 45 to 60° will ensure good stability properties and transient response. We should also be aware that phase shift causing instability can be attributed to other system details such as time delays in the FET drive system, or hold time in a sampling system. There is also a potential for op-amp and other component parasitics that can cause phase lags. All of these factors indicate the importance of having a generous phase margin.

### 3. 13 From Transfer Function Verification to Hardware Test

In this section we derive the transfer function for the existing DC-DC converter and the error amplifier employing a Lead-lag compensator. This transfer function is then

used to simulate our new design. After successful testing with our simulation method, we can test the actual hardware and compare the simulation results to the actual lab results. This will provide verification for our simulation model as well as our design method.

Our existing DC-DC converter topology is a half bridge forward converter with an input voltage ranging from 70 Vdc to 140 Vdc. The output is 12 Vdc and there is a transformer isolating the primary from the secondary. The feedback loop contains an analog opto-isolator and is used to provide the analog feedback signal from the secondary across the isolation barrier back to the primary. This signal that is produced on the primary side (input side of the converter transformer) is the signal that is used as the control signal to intersect the ramp for termination of the PWM pulse that drives the primary side switches. For simplicity, the opto-isolator is not shown in our control loop and is assumed not to cause any non-linearity or bandwidth limitations. Our goal is to proceed and use a systematic method to determine if it is possible to improve the existing control loop bandwidth transient response and stability. This will be accomplished in the following manner:

a) Derive the existing phase, gain and transient response plots from the schematic of our existing converter.

b) Obtain frequency and transient plots of the actual hardware and compare the theoretical results to the real hardware results.

c) Derive the transfer functions of the improved design; determine the corresponding error amp components; obtain the gain, phase and transient plots of the new transfer function and compare this to the previous design.

d) Insert the newly obtained components into the existing converter and obtain the real hardware results. Compare these to the result from the original design.

e) Finally, quantify the improvements of the new design to the performance of the old converter. Then ask the question, can the design process be improved? How?

By implementing these steps, we should be able to establish a design process to improve DC-DC converter control loops in real world applications.

Additionally, we will need a simple block diagram description when performing the tasks previously explained. One such diagram shown in Figure 36 can be used to evaluate, explain and improve DC-DC converter control loop performance. The feedback elements in schematic form will help the designer understand how the DC-DC converter feedback works. The following schematic diagram also illustrates the individual blocks we must model, including the modulator, the power transformer, the LC filter, voltage measurement point, the Lead-lag compensation, the error amplifier and other miscellaneous portions of the system.

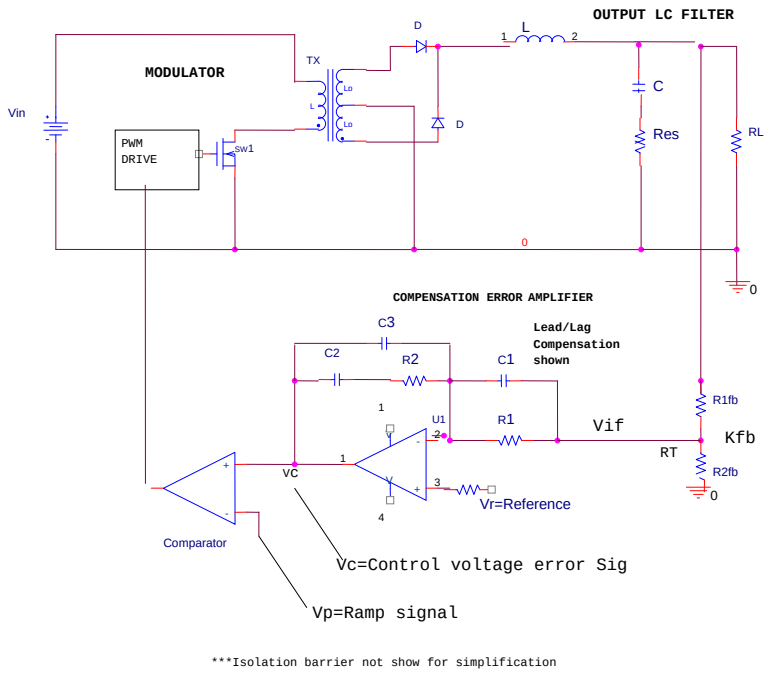


Figure 36: Feedback Elements in Schematic Form

### 3. 14 Developing the Transfer Function

Figure 37 shows an output LC filter for our buck converter. The process of deriving the transfer function requires us to converter all components into impedances within the frequency domain. Creating the transfer function $V_{out}/V_2$ will allow us to obtain the frequency response of the loaded LC filter. The following equation is the filter transfer function. For simplicity we neglect R(esr) and inductor resistance.

$$V_{out} = \frac{V_2\left(\frac{1}{LC}\right)}{\left(s^2+\frac{s}{R_L C}+1/LC\right)} \tag{3.29}$$

Let $N_s$ be the secondary and $N_p$ as the primary turns of the power transformer. Then $V_2$ is obtained as $V_2 = (V_{in})(N_s/N_p)$ and

$$\frac{V_{out}}{V_{in}} = \frac{\frac{N_S}{N_p}\left(\frac{1}{LC}\right)}{\left(s^2+\frac{s}{R_L C}+1/LC\right)} \tag{3.30}$$

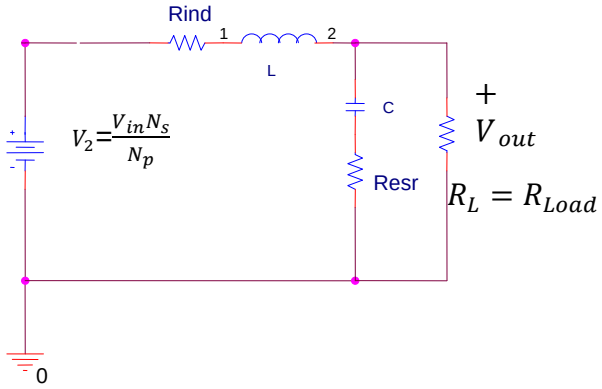


Figure 37: Buck Converter Output LC Filter

We can set the numerator and denominator each equal to zero. This will allow the determination of the roots of the numerator (zero's of the system LC filter) and the roots of the denominator (the poles of the system LC filter)[1]. The derived second order transfer function contains two poles; $p_1=-\alpha + j\omega_d$ and $p_2=-\alpha - j\omega_d$ where j = √(-1), and $\alpha = 1/(2R_LC)$. This type of filter is considered lightly damped; so we can use the approximation of

$$\omega_d = \sqrt{\left(\frac{1}{L \cdot C}\right)} \tag{3.31}$$

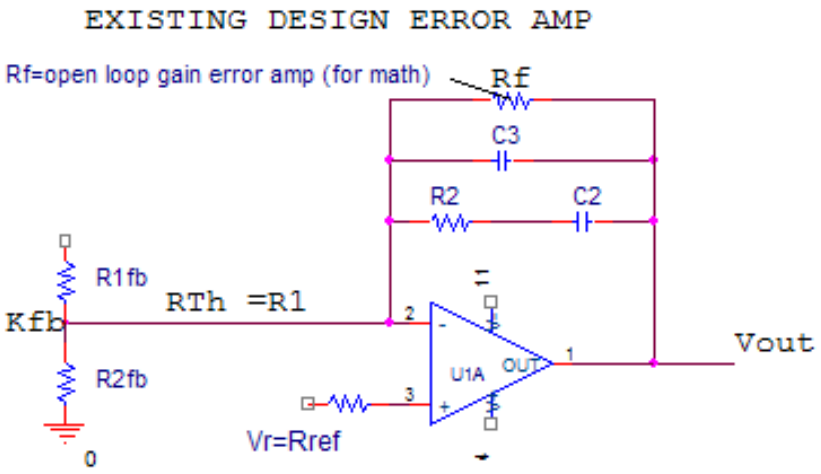


Figure 38: The Existing Error Amplifier Design

Figure 38 shows the existing DC-DC converter error amplifier with its transfer function shown in Equations 3.32 through 3.38, where $R_1$ is the Thevenin equivalent of $R_1fb$ and $R_2fb$.

$$K_e = \frac{1}{\left[\frac{1}{R_{fe}} + \frac{1}{\frac{1}{s \cdot C_3}} + \frac{1}{\left(R_2 + \frac{1}{s \cdot C_2}\right)}\right]} \Bigg/ R_1 \tag{3.32}$$

$$K_e(s) = R_{fe} \frac{\left(R_2 \cdot s \cdot C_2 + 1\right)}{\left(R_2 \cdot s \cdot C_2 + 1 + s^2 \cdot C_3 \cdot R_{fe} \cdot R_2 \cdot C_2 + s \cdot C_3 \cdot R_{fe} + s \cdot C_2 \cdot R_{fe}\right) \cdot R_1} \tag{3.33}$$

As previously illustrated the modulator portion of our converter has a gain of

$$K_{\text{mod}} = \frac{1}{V_P} \cdot V_{in} \frac{N_S}{N_P} \tag{3.34}$$

Because the overall loop gain *(OLG)* is the product of the individual gains around the control loop (error amplifier, modulator and LC filter, etc.) we can now derive the complete system transfer function. Figure 39 describes the DC-DC converter feedback loop which is used to derive the gain, phase and time response of our control system.

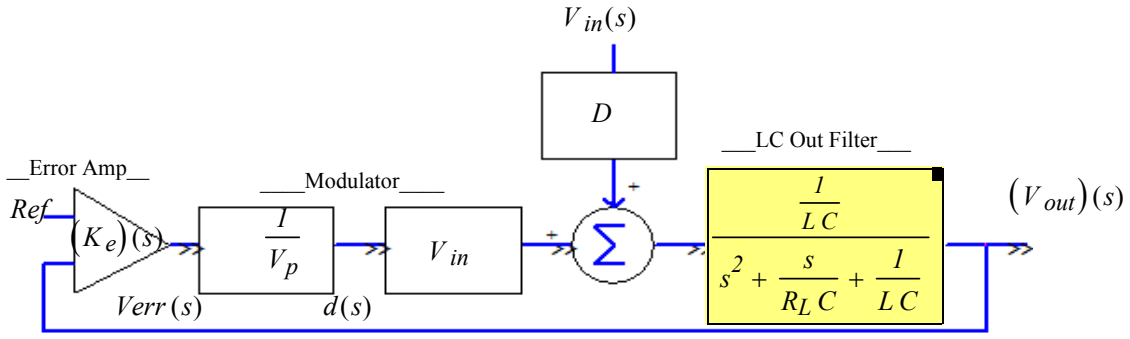


Figure 39: Feedback Loop Flow Diagram

From Equations 3.35 to 3.38, the open loop transfer function is derived.

$$V_2 = V_{in} * N_s / N_p \tag{3.35}$$

$$K_e(s) = R_{ef} \frac{\left(R_2 \cdot s \cdot C_2 + 1\right)}{\left(R_2 \cdot s \cdot C_2 + 1 + s^2 \cdot C_3 \cdot R_{fe} \cdot R_2 \cdot C_2 + s \cdot C_3 \cdot R_{fe} + s \cdot C_2 \cdot R_{fe}\right) \cdot R_1} \tag{3.36}$$

$$K_{\text{mod}} = \frac{1}{V_P} \cdot V_2, \qquad FLT(s) = \frac{\frac{1}{L \cdot C}}{(s)^2 + \frac{s}{R_L \cdot C} + \frac{1}{L \cdot C}} \tag{3.37}$$

$$ModLC(s) = \frac{\frac{K_{\text{mod}}}{L \cdot C}}{(s)^2 + \frac{s}{R_L \cdot C} + \frac{1}{L \cdot C}} \qquad OLG(s) = \frac{\frac{K_{\text{mod}} \cdot K_e(s)}{L \cdot C}}{(s)^2 + \frac{s}{R_L \cdot C} + \frac{1}{L \cdot C}} \tag{3.38}$$

Table VI shows the existing feedback components and the corresponding phase and gain plots which are shown in Figure 40. It can be concluded from Figure 40 there is very little phase margin and very little gain margin. The system will have difficulty maintaining stability under all operating conditions.

We prefer to have a 20 dB gain margin. In addition, the low frequency gain could be higher. The phase plot is also a problem. This design is marginally stable because we have approximately 10° of phase margin. This is the area we hope to improve. If we are able to increase the phase margin we should be able to improve the design by reducing the overshoot and ringing.

TABLE VI: UNIMPROVED CONVERTER COMPONENT VALUES

| | | |
|---|---|---|
| $V_P = 2$ Volts | $C = 165$ uf | $V_{in} = 116$ V |
| $R_L = 0.75$ Ohms | $L = 50$ uf | $N_p = 4$ |
| $f_s = 140$ KHz | $V_{out} = 12$ Volts | $N_s = 2$ |
| $R_2 = 2.2$K Ohms | $C_2 = 0.022$ uf | $C_1$ = n/a |
| $G_{Rpeak} = 1.713$ KHz | C3 = 470 pf | |
| $R_{ampOL} = 1E9$ Ohms | $R_1 = 8.3$K Ohms | |

From the above values we obtain the Bode plots of the existing converter.

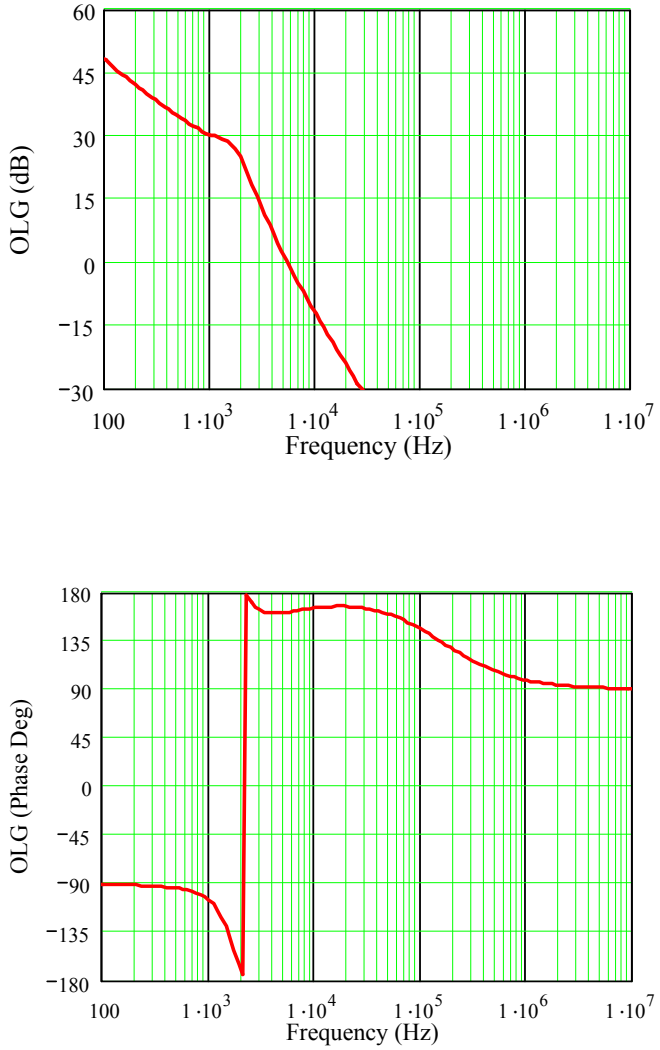


Figure 40: Bode Plots for Existing Hardware Model

To verify the accuracy of our model, we will compare the time response from the simulations to the actual hardware time response. As previously mentioned we get the

time response by taking the inverse Laplace transform $\{x(t) = \mathcal{L}^{-1}[X(s)]\}$ of the *OLG* (overall closed loop transfer function) shown in Equation 3.38. In addition we can apply a step input as shown in Equation 3.39 and obtain the transient response of the existing DC-DC converter shown in Figure 41.

$$y(t) = \mathcal{L}^{-1}[(1/s)OLG(s)] \tag{3.39}$$

Using simulation software and Equation 3.39, we produce the existing DC-DC system transient response shown in Figure 41.

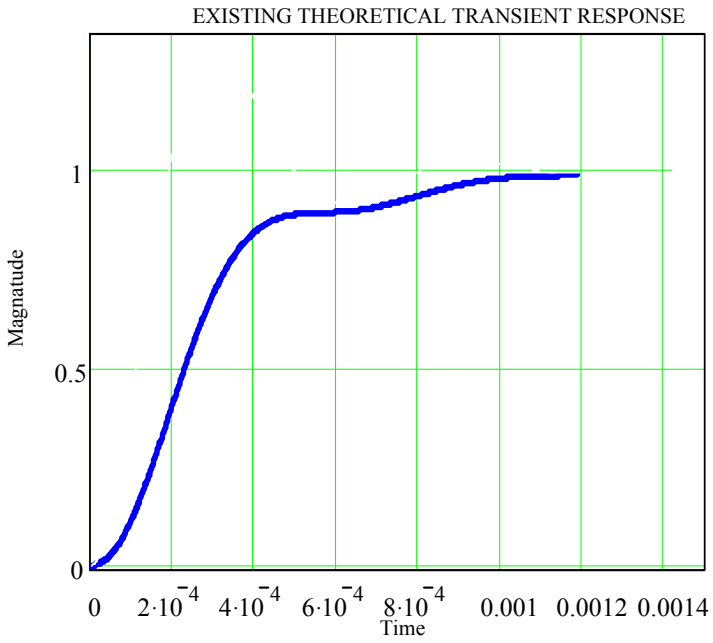


Figure 41: Simulated Time Response of Existing Design

For comparison purposes we have taken the actual hardware and applied a step input to evaluate the real world control loop transient response. The scope plots were lab generated and are shown in Figure 42. You can see from these lab results, the actual hardware closely matches the simulated response. Based on these results it appears that

model accurately approximates the real world hardware response and our model is validated.

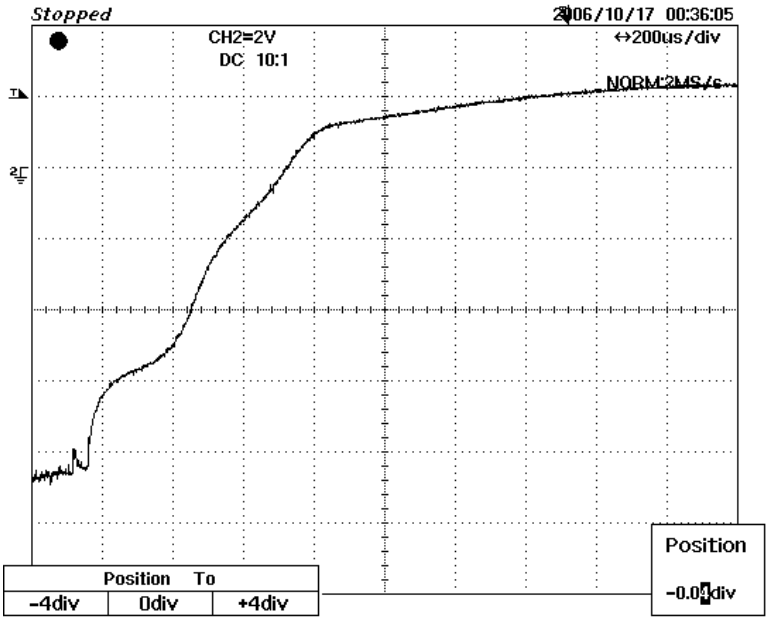


Figure 42: Lab Results Transient Response from Existing Hardware

The initial startup is a slightly different than our mathematical simulation and is related to the secondary side current limit circuitry of the DC-DC converter. By comparing the two time plots one can conclude that the mathematical model represents the existing converter hardware fairly accurately.

### 3. 15 The Systematic Design Process

The goal of the design process is to achieve the best possible transient response while maintaining excellent stability of our system. Utilizing this approach we gain the benefit of following a systematic approach supported by powerful simulation software allowing the observation of both the frequency domain and time domain characteristics. Creating and importing the system transfer functions into Mathcad provides valuable insight into the characteristics, performance and ultimately the improvement of DC-DC converter control loops.

Common characteristics of the output LC filter are unity gain at lower frequencies and a resonant peaking at the second order pole frequency. The resonant peak is determined largely by the output load resistance. The filter has a classic shape and just after the resonant peak the gain will fall at a rate of -40 dB per decade. Also just after the resonant peak (at higher frequencies) the phase shift goes from zero to –180° lagging. Knowing this we must shape the loop in a way to ensure stability.

A Lead-lag network is utilized as we have previously determined and it provides us with high DC gain (zero steady state error) while maintaining at least 45° of phase margin at the crossover frequency. In addition, we must provide a minimum of 20 dB of gain margin (at the switching frequency) as the phase approaches -180°. The above mentioned criteria will be used as a basis for our design process.

An explanation of each stage will allow us to understand our approach for improving and shaping the gain and phase characteristics of the control loop. We choose

our switching frequency based on several key items such as system form factor, efficiency and output ripple voltage. These parameters all fight each other and the typical trade-off analysis must be performed to determine the switching frequency. In most converter topologies, higher switching frequencies will result in smaller filter components, reduced output ripple and reduced efficiency due to switching losses. Once we have established the optimal switching frequency we then pick the crossover frequency at least 10 times lower so we can achieve at least 20 dB of gain margin at the switching frequency. By ensuring 20 dB of gain margin at the switching frequency we will reduce the effects of the output ripple (caused by the output filter capacitor ESR). If the gain was high at this point it could cause large signal instability. In addition, we would like to ensure a phase margin of at least 45° at the unity gain cross-over frequency and to do this we must utilize a lag network. The lag network results in a low gain at lower frequencies, leading to a tracking error at DC. This lag network or lag compensation can be accomplished by inserting a series R-C network as local feedback around the compensation error amplifier. We want this lag network to add a pole at the crossover frequency. In this step we can determine $R_2$ by selecting the point at which the $R_2/R_1$ will be equal to unity gain right at the cross-over frequency. We can use the straight line approximation to find the slope of the output LC filter and set the feedback $R_2/R_1$ equal to the slope, then $R_2$ can be determined based on the given crossover frequency. We can fix the low DC gain at the lower frequencies by combining a lead network with the existing lag compensator. By doing this we establish Lead-lag compensation. By adding a lead capacitor in parallel with the input R of the error amplifier we increase the gain

and phase margin of the open loop gain function. By inserting the lead capacitor (introducing a zero) into the compensation amplifier and forcing the break frequency of this zero to be the same as the unity gain frequency $f_c$ of the output LC filter we can ensure a phase margin of 45° at the cross-over frequency. In addition, we can also obtain high DC gain at low frequencies in order to achieve a small tracking error at DC. By using Lead-lag compensation we can achieve the improved response time and still maintain system stability.

The output filter capacitor ESR (Equivalent Series Resistance) is an inherent parasitic in all capacitors. The ESR in this component will introduce a zero into the system. This will add some phase lead. However, it should not be relied upon for any beneficial use due to its variations in value over time, temperature and operating frequency.

Lastly, by setting $C_3$ equal to the output capacitance (of the LC filter) times the output capacitor ESR divided by our established $R_2$, the error amplifier gain will be reduced at the system switching frequency enough to attenuate the effects of the ESR of the output filter capacitor. We essentially add $C_3$ for a high frequency roll-off. This occurs because the pole at $1/\left(R_2 \cdot C_3\right)$ cancels the zero at $1/(Resr \cdot C)$.

Below we discuss a design procedure to improve DC-DC converter control loops by increasing stability and improving the transient response.

**The Design procedure can be summarized as below:**

1) Establish the transfer function for the DC-DC converter under consideration.

2) Create a Mathcad® simulation model based on the transfer function obtained.

3) Utilize Mathcad® to run the phase and gain plots. With these plots establish the proper compensation requirements and establish if the system will meet design requirements.

4) Apply the Detailed Loop Shaping Procedure "DLSP" shown below to ensure 45° of phase margin and at least 20 dB of gain margin at the converter switching frequency.

5) Insert the new component values back into the model and obtain the phase, gain and time response. Use Mathcad® to obtain the complex inverse Laplace transforms in order to obtain the time response of the improved system.

6) Review the new controller frequency and time domain Bode plots to see if they meet the desired requirements with the mathematical model. If so, utilize the new component values in the actual hardware and obtain the time response from the hardware. Compare the lab results to the simulations for verification.

**Detailed Loop Shaping Procedure (DLSP)**

The following is detailed loop shaping procedure to be used in the control system design for DC-DC converters. This process should be modified based on converter topology and control method. This procedure (DLSP) is to be implemented in step 4 of the main process described above.

1) Set the switching frequency of the system to meet the required specifications, output ripple requirements, efficiency and control chip functionality.

2) Choose the proper configuration for the error amplifier compensation. This will depend on system topology and current mode or voltage mode control. For our converter under consideration we have established mathematical models for negative feedback utilizing voltage mode control.

3) Derive the cross-over frequency $f_c$ and pick this point at least 10 times lower than the system switching frequency.

4) Obtain $R_2$ and $C_2$ for the compensating pole portion of the Lead-lag network. Based on the previous discussion for lag network pole placement, the pole needs to be located at least 1/10 of the output LC resonant frequency. The value of $C_2$ is determined from the following equations. $0.1\omega_n = \omega_p = 1/(R_2C_2)$, $C_2 = 1/(R_2(0.1\omega_n))$, $\omega_n = 1/\sqrt{(LC)}$. A value of $R_2$ can be chosen to be much smaller than the input impedance of the error amplifier.

5) After deriving $R_2$ and $C_2$, we can calculate $R_1$ establishing a high DC gain. We do this by setting the error amplifier gain to $K_e = R_2/R_1$ and substituting $K_e$ into equation $(V_{in})(K_e)/(2\pi f_c)^2 VpLC$ from Figure 35 straight line approximation. At unity gain this equation will be equal to one. Substituting $K_e$ we achieve $R_2 = R_1(2\pi f_c)^2 VpLC/(V_{in})$.

6) Now Obtain $C_1$ for the compensating zero. To re-establish the high gain as the frequency increases so we can maintain excellent transient response we now need to introduce the zero for the lead network portion of the error amplifier network. Place the zero at the **crossover frequency** $f_c = 1/(2\pi \cdot R_1 \cdot C_1)$. To calculate $C_1$ adjust the above equation to $C_1 = 1/(2\pi \cdot R_1 \cdot f_c)$. From previous discussions we know this step will provide

45° of phase margin only if we pick the break frequency of the zero equal to the unity gain frequency of the open loop system.

7) Let $R_2 \cdot C_3 = Resr \cdot C$. Inserting an additional capacitor $C_3$ as shown in Figure 38 will add an additional pole in the system and reduces the gain at the operational switching frequency of the DC-DC converter. This will cancel the lead compensation effect of the output capacitor's equivalent series resistance (ESR) and enable us to eliminate the effects of the ripple voltage getting back into our control loop error amplifier.

# CHAPTER IV

# AN EXAMPLE OF THE PROPOSED DESIGN PROCESS

## 4. 1 Applying the Lead-lag Compensation to the Existing Design

In this chapter the proposed method is applied to a commercial DC-DC converter. The equations are derived and the Lead-lag compensator is employed. The equations are fed into simulation software and used to generate frequency domain and time domain plots for analysis, system improvements and comparisons to the original design.

In order to improve the existing design we modify the error amplifier and employ a Lead-lag network, which proved to be effective in our situation. In Figure 43 we have the Lead-lag network circuit configuration previously discussed, along with the corresponding transfer function $K_{elead}\ (s)$ derived from the error amp and the simplified transfer function.

$$K_{elead}(s) = \frac{1}{\left[\frac{1}{R_f} + \frac{1}{\left(\frac{1}{s \cdot C_{3b}}\right)} + \frac{1}{\left[\frac{R_{2b} \cdot C_{2b} \cdot s + 1}{C_{2b} \cdot s}\right]}\right]} \cdot \left[\frac{1}{\left(\frac{1}{C_{1b} \cdot s} + R_{f1}\right)} + \frac{1}{R_{1b}}\right] \tag{3.40}$$

$$K_{elead}(s) := R_f \cdot \left(R_{2b} \cdot C_{2b} \cdot s + 1\right) \cdot \frac{\left(1 + R_{1b} \cdot s \cdot C_{1b}\right)}{\left(R_{2b} \cdot C_{2b} \cdot s + 1 + s^2 \cdot C_{3b} \cdot R_f \cdot R_{2b} \cdot C_{2b} + s \cdot C_{3b} \cdot R_f + C_{2b} \cdot s \cdot R_f\right) \cdot R_{1b}}$$

(3.41)

$$OLG_{lead}(s) = \frac{K_{mod} K_{elead}(s)/LC}{(s^2 + \frac{s}{R_L C} + \frac{1}{LC})} \tag{3.42}$$

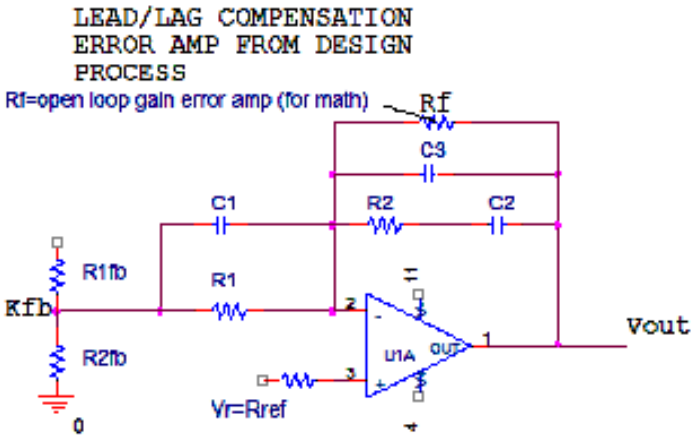


Figure 43: Lead-lag Network Error Amp

## 4. 2 Selecting the Lead-lag Compensation Components

The equations derived in chapter three and four are used to establish the configuration and components for the error amplifier. The best results in our generic examples have been derived using a Lead-lag network. Below we follow our process establishing the component in our new compensation network. In the following procedure we skip steps 1 and 2 because as previously discussed (pg 62, 65, 66) they are based on topology, efficiency, and output voltage ripple of the existing DC-DC converter. We focus on the process for optimizing only the feedback loop in the existing converter. The switching frequency of the existing converter is 140 Khz.

STEP #3: The switching frequency $f_s = 140\ KHz$ was based on required specifications. From this we can choose the crossover frequency $f_c$ equal to or less than 1/10 the switching frequency. If we pick 1/14 the crossover frequency $fc=f_s/14$ then

$f_c = 10\ kHz$.

STEP #4: In this step we determine the capacitor $C_{2b}$ for the pole placement at 1/10 the resonant frequency. Pick $R_{1b}$ = 4.7 K Ohms, then $C_{2b} = 1/( R_{2b}(0.1\omega_n)) = 1.933 \times 10^{-7}$ which is 193 *nf*. The closest standard value would be 0.22 μf.

STEP #5: Calculate $R_{2b}$ utilizing the following equation so we can have unity gain at the crossover frequency. $Ke_{dc} =( R_{2b} / R_{1b})=(2\pi f_c)^2 VpLC/(V_{in})$. This will make $R_{2b}$= 5.22 K Ohms and the closest standard value will be 5.2 K Ohms.

STEP #6: Using equation $C_{1b} = 1/(2\pi R_1 f_c)$ we can determine the value $C_{1b}=3.377\ nf$. The closest standard value of 3300 *pf* can be used.

STEP #7: Set $C_{3b}=R_{esr}.(C/R_{2b})= 1.564 \times 10^{-10}$ or 15.6 nf. The closest standard value will be *15 nf.*

We have inserted all of the components derived in Table VII. It is important to realize that in real life we will need to use the closest standard values to those from our design process.

TABLE VII: IMPROVED CONVERTER COMPONENT VALUES

| | | |
|---|---|---|
| $V_P = 2\ Volts$ | $C = 165\ uf$ | $V_{in} = 116\ V$ |
| $R_L=0.75\ Ohms$ | $L = 50\ uf$ | $N_p = 4$ |
| $f_s= 140\ KHz$ | $V_{out} = 12\ Volts$ | $N_s = 2$ |
| $R_{2b} = 5.23K\ Ohms$ | $C_{2b} = 193\ nf$ | $C_{1b}= 3.3\ nf$ |
| $G_{Rpeak} =1.713\ KHz$ | $C_{3b} = 15\ nf$ | |
| $R_{ampOL} = 1E9$ | $R_{1b} = 4.7K$ | |

The above components will now be inserted into our mathematical model as a means to review our design prior to building the actual hardware. By running our model we can verify that we meet our phase and gain requirements. The following schematic illustrates the improved configuration (Lead-lag network) for the new feedback control system. See the circled areas of Figure 44 and 45.

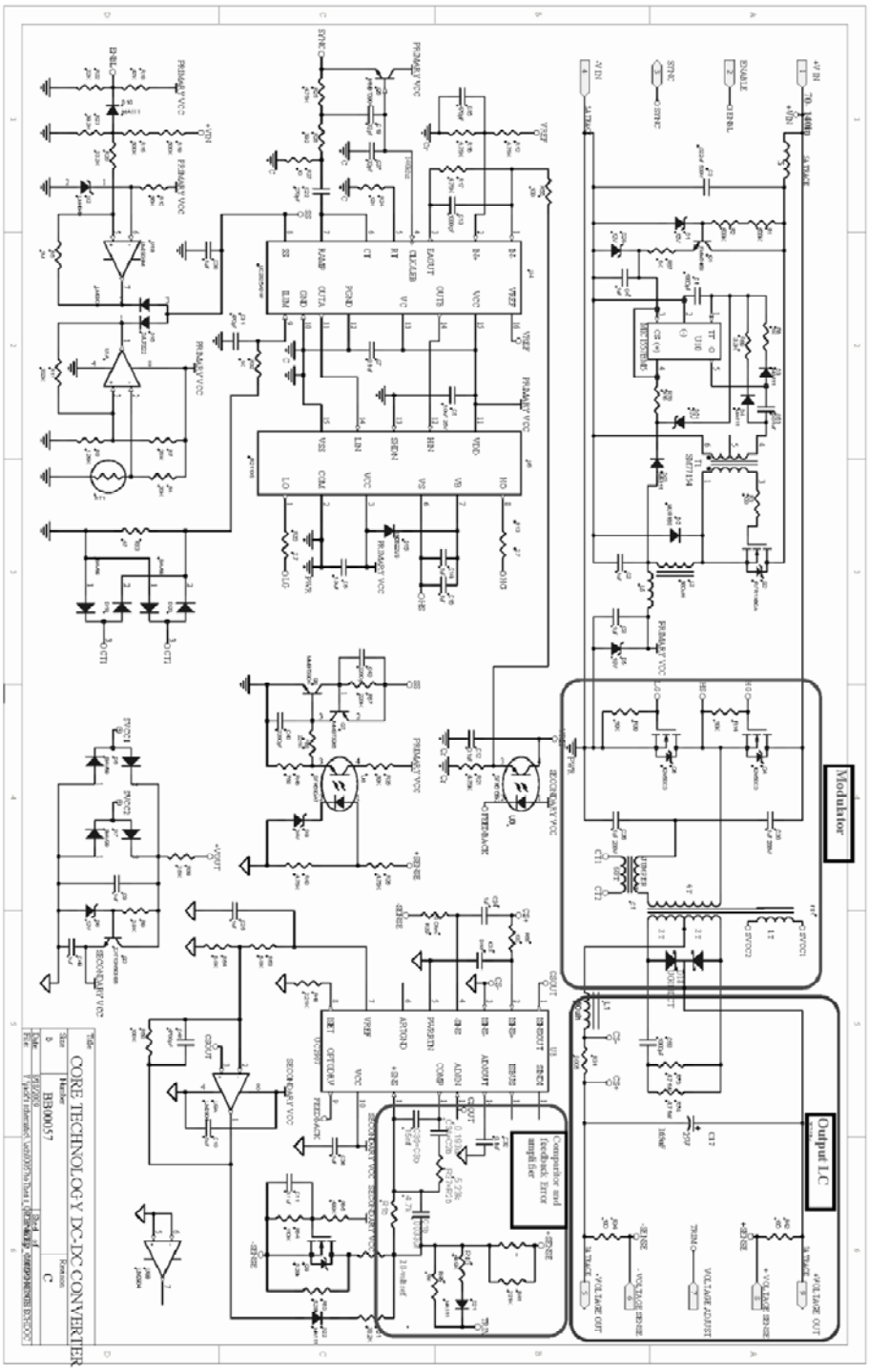


Figure 44: Improved Feedback Configuration Schematic

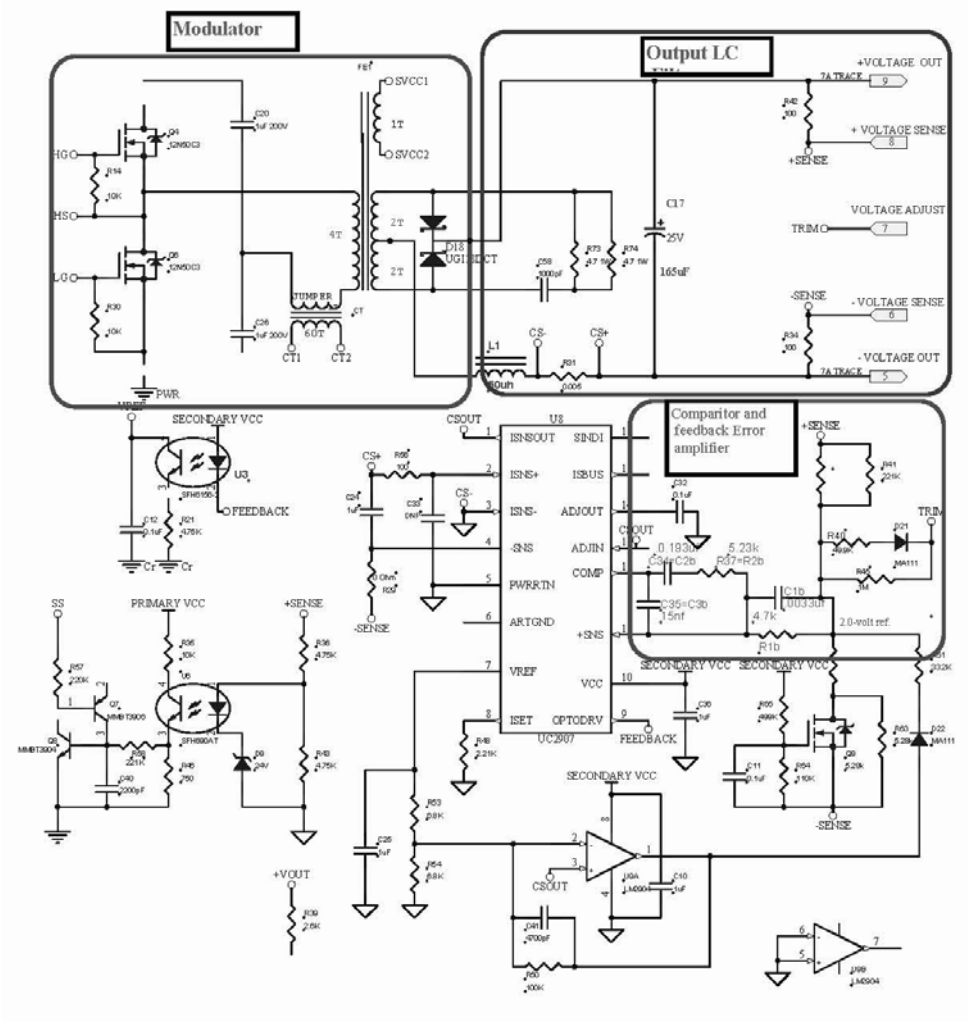


Figure 45: Improved Feedback Configuration Close-up

It can be seen that the new gain plot in Figure 46 resembles the desired generic plot of the Lead-lag network in Figure 35. The original design yielded almost no phase margin (5-10°), and contains positive gain of 15 dB as the phase reaches 180°. Figure 46 and 47 show a dramatic improvement in the dynamic performance of the feedback loop. The improved design has an excellent 60° phase margin, and a very desirable 20

dB gain at the converter switching frequency to squelch the effects of the ESR ripple getting back into the control loop. We also have a very desirable -30 to -40 dB as the phase approaches -180° resulting in a very stable control loop.

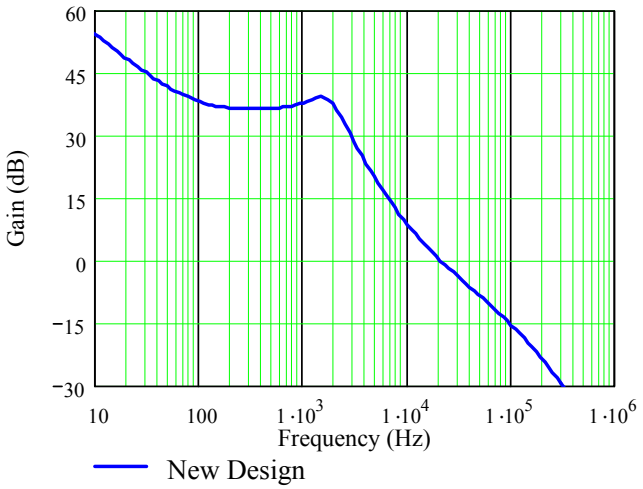


Figure 46: Gain Plot of the Improved System

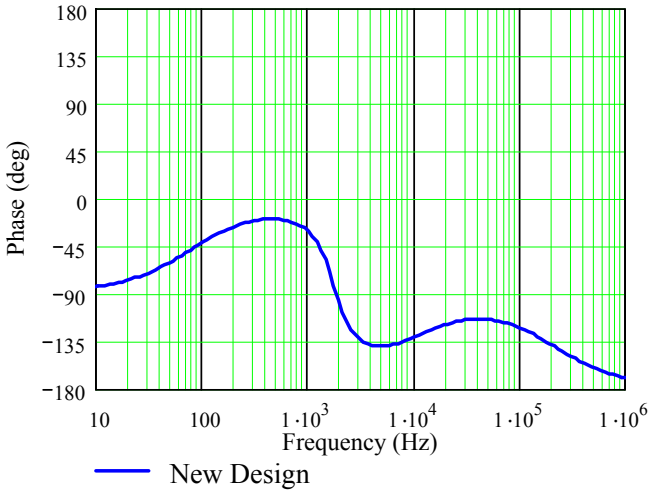


Figure 47: Phase Plot of the Improved System

### 4. 3 Comparison of the Existing versus the Improved System

In Figure 48 we compare the theoretical results from both the existing converter and the newly designed converter.

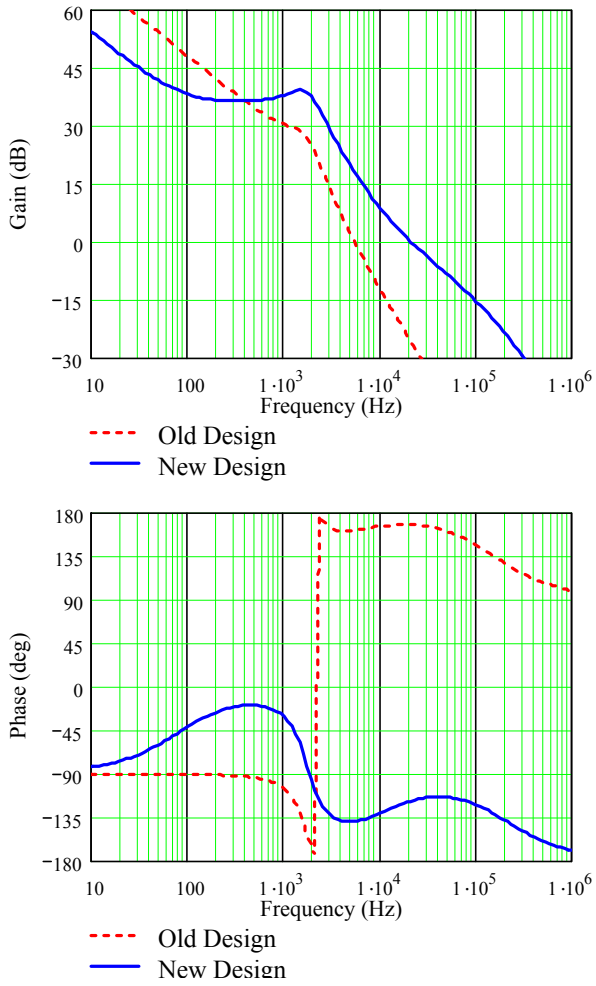


Figure 48: Comparison of Existing Versus Improved System

As observed from the gain plot in Figure 48, we have approximately 20 dB of gain margin at the switching frequency with the improved version as compared to

approximate 15 dB of positive gain margin as the phase approaches 180° with the old design.

The improved design phase plot however is more impressive with a phase margin of about 60° and much improved over the old design. The old design has approximately 15° of phase margin. With approximately 60° of phase margin the new design will have very little overshoot and almost no ringing.

### 4. 4 Simulation Results Versus Lab Results

In the following plots we will compare the simulated time domain results with the actual hardware results. This will allow us to quantify and validate the accuracy of our model. Figure 49 shows the improved time domain transient response from the simulation tools we have used. Also, observing Figure 50 and comparing it to Figure 42 it can be concluded that the improvement is significant over the old design. The rise time and system stability both have been significantly improved.

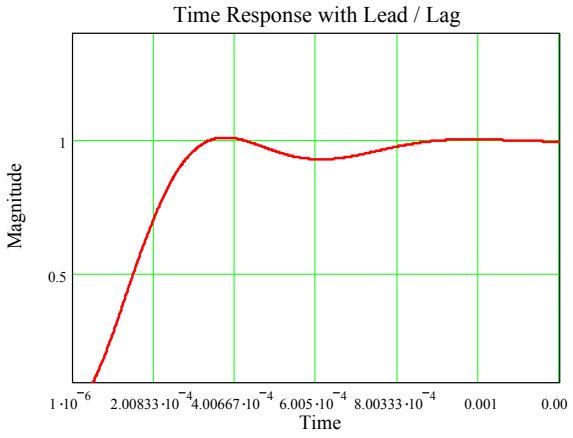


Figure 49: Simulated Transient Response of Improved System

The existing DC-DC converter hardware was modified with the components calculated from our improvement process. Oscilloscope plots of the time response were taken from the improved DC-DC converter so we may quantify the benefit over the old design. It is obvious from Figure 50 that the newly modified design has dramatically improved results and closely matches our simulation results.

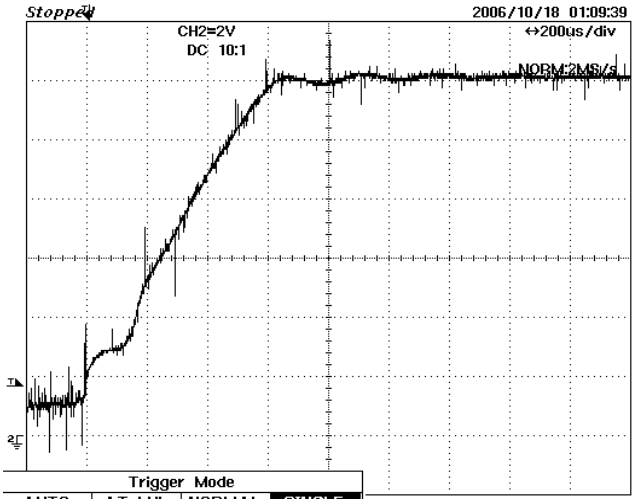


Figure 50: Lab Transient Response of the Improved System

# CHAPTER V

# SUMMARY AND FUTURE RESEARCH

For a power electronic design engineer, having the capability to systematically establishing the proper feedback component values for a DC-DC converter control system is extremely important. In the past, empirical methods have been used to determine the feedback approach. These methods have proven to be time consuming, difficult and ineffective. In this thesis we establish an approach that utilizes modern techniques such as models and mathematical equations to accomplish this task. A good understanding of Bode analyses, Lead-lag networks, and frequency domain analyses will allow us to quantify components that make up our control system. Having these tools to design the feedback system will ensure the DC-DC converter is stable while reducing the development cycle.

The equations established for our system will vary based on the topology under consideration. We should keep in mind that out DC-DC converter system contains discontinuous and non-linear dynamics caused by the PWM circuitry. The active devices of the DC-DC converter are nonlinear due to the instantaneous currents and voltages during the power switching cycle. In addition, although the output filter capacitor's ESR (equivalent series resistance) is a linear element it can be an adverse contributor to the loop dynamics if not treated property.

Using tools such as the Laplace transform and Bode plots require systems that respond in a linear and continuous manner. The averaged switch model and small signal analysis can be employed so we may treat the feedback system as continuous and linear. The small signal schematic will allow us to utilize the generalized flow diagram and will provide a comprehensive method of establishing the open loop system transfer function. Once we have the transfer function we will now have the ability to modify component values to improve the system gain and phase characteristics. We have learned that we can shape and position certain aspects of the system gain characteristics to ensure stability while maintaining good bandwidth and little or no DC error.

Nearly all power converters contain an output LC filter. This LC filter along with the error amp inversion will always create nearly 360° of phase lag producing an inherently unstable system. Knowing this we have learned that we will most likely require a lead, lag or Lead-lag compensation network. This network is implemented in the error amplifier gain stage and will shape the closed loop system characteristic to ensure we have at least 45° of phase margin at the crossover frequency. In addition, we have established that by providing an additional pole into the Lead-lag network we can eliminate or dramatically reduce the effects of the output capacitance equivalent series resistance (ESR) in the LC output filter.

Our time response analysis process is proving to be a valuable tool for evaluating system performance once we have utilized our frequency domain mathematical tools to determine the controller approach. We can use our time response analysis to manipulate the overshoot and settling time of the output LC and ensure we can meet system

performance requirements with various LC filter components. By evaluating the response of the output LC filter (with a pulse input) we can establish the required damping ratio and the natural frequency of the filter. We do this in an iterative manner to minimize the physical size of the output LC filter while maintaining system transient response requirements.

The information contained in this thesis has unveiled a deeper understanding of how our control system will respond when there is not enough phase or gain margin. For example if the system has close to 180° of phase lag at the crossover frequency it will oscillate at the crossover frequency. Knowing this, we could monitor the output oscillations and determine if they are caused by system noise or lack of phase margin in the control loop.

We currently have accumulated a collection of control system knowledge as it relates to DC-DC converters. This information provides an in-depth look at methods and procedures to analyze various aspects of DC-DC converter wave-forms in both the frequency and time domain.

Time response simulation of DC-DC converter transfer functions created with the concepts previously discussed could not be easily viewed without the use of Mathcad® software. This software suite has proven to be a valuable tool in establishing time domain plots from the inverse Laplace transform by simplifying complex DC-DC control loop transfer function equations.

Future research will include establishing similar design tools from various DC-DC converter topologies as well as other current mode conversion techniques.

Adjustments to the software model will be required and a good understanding of each of the new topologies under consideration will be required. Other advanced control techniques such as ADRC (Active Disturbance Rejection Control) can be considered for a process similar to the one discussed in this thesis. By establishing systematic approaches to control loop design we can minimize development design cycles and better understand how to handle difficult design problems.

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