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A Generalized Control Method for Constant Switching Frequency Three Phase PWM Boost Rectifier Under Extreme Unbalanced Operation Condition

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A GENERALIZED CONTROL METHOD FOR CONSTANT SWITCHING FREQUENCY THREE PHASE PWM BOOST RECTIFIER UNDER EXTREME UNBALANCED OPERATION CONDITION

ABHISHEK KUMAR UPADHYAY

ABSTRACT

This thesis presents a generalized control method for constant switching frequency PWM Boost Type Rectifier under extremely unbalanced operating conditions in the power system. The proposed analytical method is verified by using MATLAB/ Simulink model developed under severe unbalanced conditions of input source voltages and input impedances. The closed loop control method for controlling the output DC voltage is also presented and verified by using MATLAB/Simulink model. An experimental model is built to prove the feasibility of the proposed constant switching frequency operation of the PWM Boost Type Rectifier under extreme unbalanced operation conditions by using DSPACE RT1104 digital control system.

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NOMENCLATURES

AC: Alternating Current

DC: Direct Current

EMI: Electro-magnetic interference

IGBT: Insulated-gate bipolar transistor

MOSFET: Metal-oxide field effect transistor

p.f. : Power factor

PWM: Pulse width modulation

rms: Root mean square

THD: Total harmonic distortion

Chapter I

INTRODUCTION

1.1. Introduction

AC to DC converters are widely used in industrial fields for implementing DC power supplies. These converters, also called rectifiers, are used to operate DC electric loads and large AC loads where control is very sophisticated. The conversions are generally done in two steps. In the first step the AC power is converted to DC power and in the second step DC power is converted to DC or AC depending on load. The DC to DC conversion is done with or without isolation from main supply [1]. The lighting system loads are generally supplied with non-isolated DC to DC converters, whereas isolated system is used for welding machines, induction heating loads, telecom power supplies etc. The variable frequency drives use non-isolated DC to AC conversion in the second step of converter (inverter) to run large induction motors.

All the rectifiers can be divided into two types with respect to the capability of power flow directions which are unidirectional and bidirectional. As name suggests unidirectional rectifier can have only one directional flow of power whereas bidirectional rectifiers has capability of instantaneous reversal of power flow. Diode bridge is a simple example of unidirectional power flow converter whereas thyristor bridge can be used to control the flow of energy. They are very robust and cost effective. These devices work on line commutation principle and they generate harmonics and reactive power.

Also, due to natural commutation they can only work at low switching frequencies and is also responsible for electromagnetic interference (EMI). Since harmonics are very harmful for operation of electrical system several stringent standards have been introduced to control and restrict its generation. The main parameters defined which are important to analyze behavior of a power converter are the power factor (p.f.), the displacement angle of fundamental current to voltage (∅) and total harmonic distortion (THD) of the input current. The relationship between these parameters can be given as

$$\boldsymbol{p.f.} = \frac{1}{\sqrt{1+\boldsymbol{THD}^2}}\cos(\boldsymbol{\phi}) \tag{1}$$

Keeping the above requirements in mind various studies and researches has been done on active power factor correction (PFC) system. This utilizes IGBT or MOSFET switches for bridge which are fully controllable using gating signals. The most popular PWM switching is employed to control the gating signals for these switches. The main purpose of these gating signals are given as follow.

1. To eliminate low order harmonics
2. To control the power flow direction
3. To maintain a constant switching frequency

Various converter topologies have been presented to achieve the above mentioned objectives [2]. Boost converters are increasing used for high performance industrial applications. Two level boost converter [3] and three level boost converter [4]-[6] (Vienna rectifier) are the most popular topologies used currently. This paper uses two level boost converter (Fig. 1), it has power regeneration capabilities, wide range DC bus control with low ripple, unity power factor operation and near sinusoidal input current. As the above properties is desirable for high system performance hence it has application in DC motor drives [7], power supply for voltage and current source inverters [8], magnetic power supplies[9], renewable systems and control of reactive power and harmonic compensation [10]. Consider Fig. 1 where $\boldsymbol{V_1}$, $\boldsymbol{V_2}$ and $\boldsymbol{V_3}$ are three phase input source voltages, $\boldsymbol{I_1}$, $\boldsymbol{I_2}$ and $\boldsymbol{I_3}$ are input current flowing through input impedances $\boldsymbol{z_1}$, $\boldsymbol{z_2}$ and $\boldsymbol{z_3}$ respectively and $\boldsymbol{V_{s1}}$, $\boldsymbol{V_{s2}}$ and $\boldsymbol{V_{s3}}$ are synthesized voltages, $\boldsymbol{C}$ is output DC link capacitance, and $\boldsymbol{V_{dc}}$ is voltage across load resistance $\boldsymbol{R}$. $\boldsymbol{S_{w1}}$ to $\boldsymbol{S_{w6}}$ represent switching state of the present IGBT/MOSFET switches.

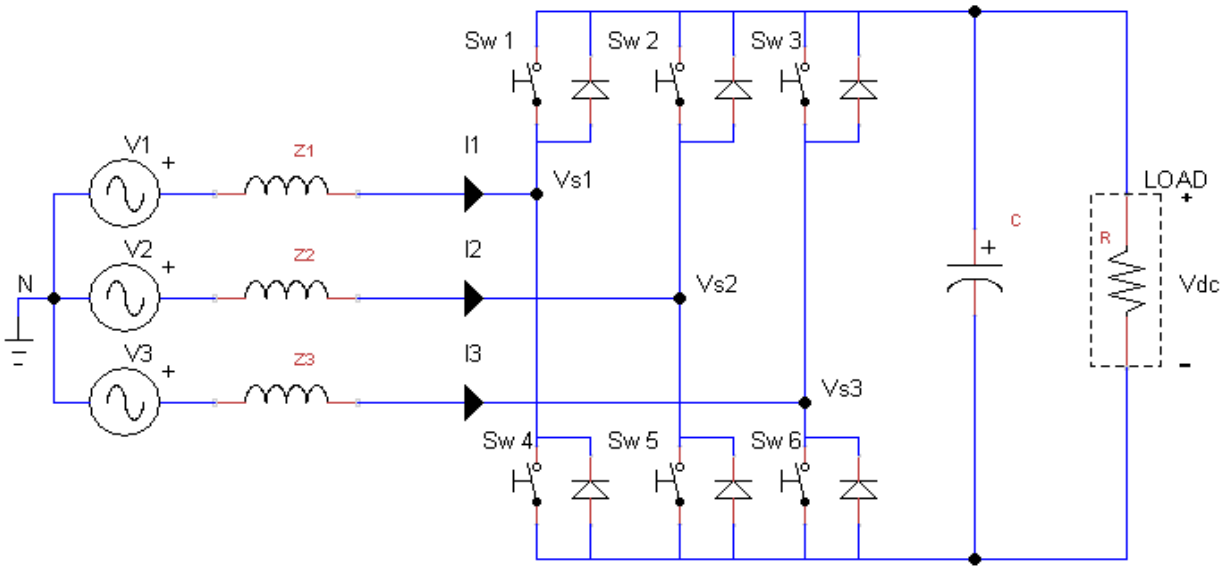


Figure 1: Two level boost type rectifier

The above topology has all the advantages as mentioned when it is working under balanced operation only. In practical world operation of electrical system is not always balanced. The imbalance in input supply can be due to uneven voltage magnitudes or fault at any voltage source. One of the major reason of imbalance is also non uniform distribution of load which results in uneven input impedances. Since, domestic supply is predominantly single phase it makes the electrical system more vulnerable to imbalances [11].

The results published in [12] show the introduction of even order harmonics at the output voltage due to unbalanced input conditions. The even harmonics in the output of the rectifier reflects back odd harmonics in the input current. A new method is proposed in [13] and [14] which eliminates the appearance of second order harmonics in output voltage under extremely unbalanced operating conditions there by elimination harmonics in the input currents. The result is experimentally verified in [15] using seven extreme unbalance cases. One of the case includes single phase operation of three phase boost type rectifier with reduced power capability operating at unity power factor with harmonic elimination. This method uses hysteresis current control (HCC) [16] method to achieve it. This method is very simple to implement as the line current is forced to track the reference current. It has fast current control response and limits peak current. Even though it gives solution for harmonic elimination under various extremely unbalanced cases,

a desirable constant switching frequency has still not been achieved with fixed band HCC under unbalanced operation.

A variable frequency operation results in heavy interaction between the phases when the midpoint of the DC link capacitor is not connected to the ground or the source neutral. This results in acoustic noise, high switching losses and difficulty in designing input filter. [24] presents solution for achieving near constant switching frequency for Vienna rectifier by impressing the interacting voltage appearing at midpoint of DC link capacitor at the input of rectifier of each phase using a bidirectional switch and controlling its duty ratio by sensing inductor current.

A different approach used in [25] where variable hysteresis controller is implemented using fictitious reference voltage which is expressed in terms of reference current. The controller calculates interacting error current present due to interacting voltages at DC link mid-point with respect to ground for various switching positions which is pre-recorded in a table. This interacting current is when subtracted from the error current generated due to comparison of reference current and line current gives the non-interacting error current component which when controlled by the variable hysteresis controller results in near constant hysteresis operation of the Vienna rectifier.

Vienna rectifier has direct connection between the interacting voltage at midpoint of DC link capacitor and the three phase input source. This connection makes control of phase current easy to implement and to predict the voltage at various switching instances. Since, the two level rectifier DC link connected only through the bridge and has no midpoint interaction, prediction of voltage instance at various switching states becomes difficult.

The inverter in [26] and converter in [27] have used the voltage difference between the source neutral and the midpoint of DC link capacitor to calculate the interacting current also called as zero sequence current or neutral current using inductor's current-voltage relationship. This method has been proved experimentally under ±10% unbalanced operation by [26].

Unlike, in [13]-[22] where Dr. Ana V. Stankovic has presented a generalized solution for elimination of harmonics under extremely unbalanced condition but not with constant switching frequency and in [26], [25] and [27] where a method to achieve constant switching frequency under balanced condition only, this thesis presents a simple generalized solution for constant switching frequency under extremely unbalanced condition. All the cases of [15] for extreme

unbalance conditions with imbalance in input voltages and input impedances are taken to verify the results.

A mathematical analysis of the generalized method is developed in Chapter II for constant switching frequency under unbalanced condition for input voltages and input impedances. There are some limitations to this method which is also discussed in details.

Chapter III comprises of general simulation model developed for implementation of analytical solution provided in previous chapter. The simulation model is built using MATLAB/Simulink. It uses Simpowersystems module of Simulink. Simulation for all the cases are provided in open loop and closed loop mode. The results are then summarized to verify and establish the proposed method.

Chapter IV gives details of the experimental set up. The DSPACE bench with DS1104 processor is used for experimental implementation [28]. Hardware set-up are made using Lab-Volt test bench. All the hardware details are provided. It gives various limitations of the device in use to perform experimental verification of the proposed method. The results produced are discussed in details and a simulation analysis is done on the result presented.

Chapter V discusses the future work and method recommended for general operation of the proposed solution using experimental set-up. A conclusion of the whole thesis project is provided to summarize the results.

Chapter II

THEORETICAL ANALYSIS AND LITERATURE REVIEW

2.1. Theoretical Analysis of Unbalanced operation of PWM Boost Type Rectifier

The PWM boost type rectifier is used in industry in various applications of AC to DC converter. It has lot of benefits over conventional converter viz. power factor control, near sinusoidal input currents and the capability of power reversal. But, these all features are only realized with balanced three phase input condition. In unbalanced condition large amount of distortion is seen in the output DC voltage component and input currents [13]. Since the introduction of IEEE 519 and IEC 61000-3-2/61000-3-4 standards, stringent limit is placed on the distortion limit that can be done in input AC line current.

Theoretical analyses of the unbalanced operation of the converter in [14] give insight about the cause of this high distortion presence in input current. Due to unbalanced input condition, second-order harmonic gets introduced in the DC link voltage which in turn reflects back third-order harmonic in the input line current. Hence, any kind of unbalance in input triggers action and reaction causing even harmonics to appear in the DC link voltage and odd harmonics in input current.

The solution developed in [15] provides the method of implementing complete harmonic elimination under unbalanced condition. But, this method has inherent drawback on variable switching frequency. To achieve near constant switching frequency it is important to have a method to eliminate the interaction between phase voltages during unbalanced operation of the converter. The theoretical and mathematical analysis presented in this chapter gives a method of achieving constant frequency under extreme unbalanced condition. The method is discussed in details along with the solution constraints

2.2. Calculation of Reference Current using Harmonic Elimination Method

The reference currents calculated for PWM boost type rectifier as shown in Fig.1 uses harmonic elimination method. The method was proposed by Ana V. Stankovic and Thomas A. Lipo [14]. The method effectively eliminates all the harmonics for unbalanced operation of the converter while operating at unity power factor. The assumptions used for deriving the reference current are

- Input voltages used are in unbalanced condition
- Input impedances used are in unbalanced condition
- There is no loss in converter circuit
- Input complex power is at unity power factor and is constant
- There is no zero sequence component in unbalanced switching function

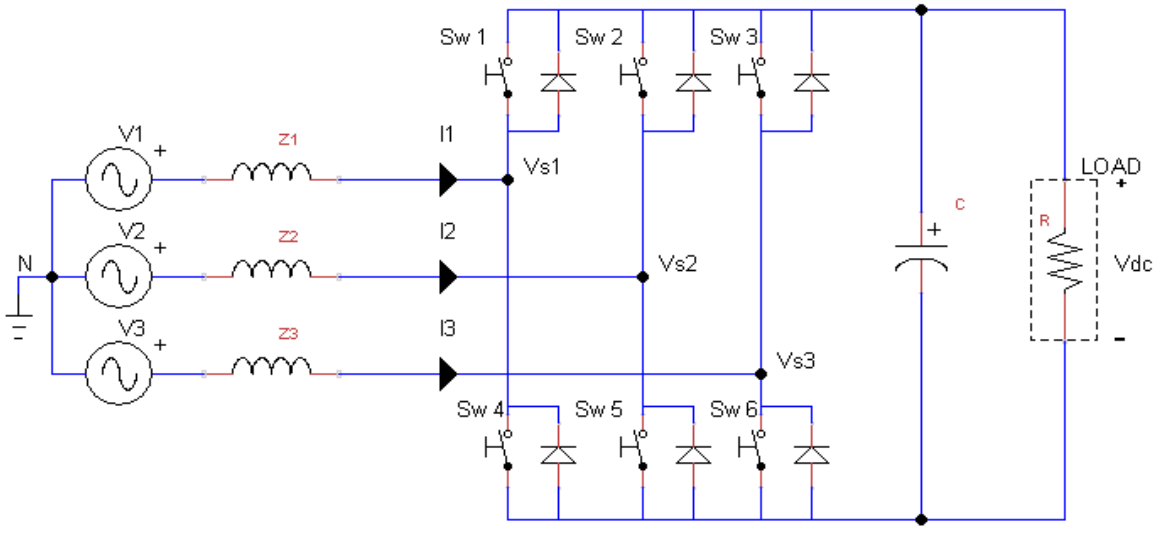


Figure 2: Three Phase PWM boost rectifier for unbalanced operation

These references calculated in this section are applicable to all level of severe fault conditions. One of them includes operation of three phase PWM boost converter using single phase supply. There are no harmonics present in input current and output DC voltage V_{dc} as shown in [15]. The derivation for reference currents is discussed briefly in this section.

$$V_1 = z_1 I_1 + V_{s1} \tag{2}$$

$$V_2 = z_2 I_2 + V_{s2} \tag{3}$$

$$V_3 = z_3 I_3 + V_{s3} \tag{4}$$

$$I_1 + I_2 + I_3 = 0 \tag{5}$$

where V_1, V_2, and $V_3$are rms value of input voltages, I_1, I_2, and I_3 are rms values of input currents, z_1, z_2, and z_3 are input impedances and V_{s1}, V_{s2}, and V_{s3} are rms value of synthesized voltage at input of rectifier. The total input complex power is given by Equation (6).

$$S^* = V_1^* I_1 + V_2^* I_2 + V_3^* I_3 \tag{6}$$

where S is apparent power for which the converter is designed. V_1^*, V_2^*, and V_3^* and S^* are complex conjugate of the three phase input voltages and the apparent power respectively. Equation (7) is derived for second harmonic elimination from the output DC voltage.

$$S_{w1} I_1 + S_{w2} I_2 + S_{w3} I_3 = 0 \tag{7}$$

The rms value of synthesized voltage at the input of the rectifier can also be written in terms of output DC voltage given by equations (8), (9) and (10).

$$V_{s1} = S_{w1} \frac{V_{dc}}{2\sqrt{2}} \tag{8}$$

$$V_{s2} = S_{w2} \frac{V_{dc}}{2\sqrt{2}} \tag{9}$$

$$V_{s3} = S_{w3} \frac{V_{dc}}{2\sqrt{2}} \tag{10}$$

Solving for three phase line currents I_1, I_2 and I_3 with all parameters known such as input complex power S, input voltages V_1, V_2 and V_3, input impedances z_1, z_2 and z_3. We get a quadratic

equation in terms of I_3 as in equation (11). To calculate I_2 with the known value of I_3 equation (12) is used. Equation (5) is used to calculate I_1. There are two solutions for the quadratic equation (11) and correct set of solution is selected by checking phase sequence of the solution. The reactive power of input complex power is set to zero for unity power factor operation.

$$\left[\frac{2z_1\left(V_3^*-V_1^*\right)}{V_2^*-V_1^*}-\frac{\left(z_1+z_2\right)\left(V_3^*-V_1^*\right)^2}{\left(V_2^*-V_1^*\right)^2}-\left(z_1+z_3\right)\right]I_3^2$$
$$+\left[\left(V_3-V_1\right)-\frac{\left(V_3^*-V_1^*\right)\left(z_1+z_2\right)-2z_1S^*}{\left(V_2^*-V_1^*\right)}+\frac{2S^*\left(z_1+z_2\right)\left(V_3^*-V_1^*\right)}{\left(V_2^*-V_1^*\right)^2}\right]I_3 \qquad (11)$$
$$+\frac{S^*\left(V_2-V_1\right)}{\left(V_2^*-V_1^*\right)}-\frac{\left(z_1+z_2\right)S^{*2}}{\left(V_2^*-V_1^*\right)^2}=0$$

$$I_2=\frac{S^*-I_3\left(V_3^*-V_1^*\right)}{\left(V_2^*-V_1^*\right)} \qquad (12)$$

These line currents are used as reference currents for harmonic elimination from Equations (5), (11) and (12). The method of achieving constant switching frequency is discussed in next section.

2.3. Approach for achieving Constant Switching Frequency

The currents calculated in section 2.2 is used as reference line current by the current controller. Fig. 2 has no drawn out mid-point of output DC link, hence it is redrawn by considering a DC-link mid-point ***M*** as shown in Fig. 3 where ***L₁***, ***L₂*** and ***L₃*** are values of input inductances.

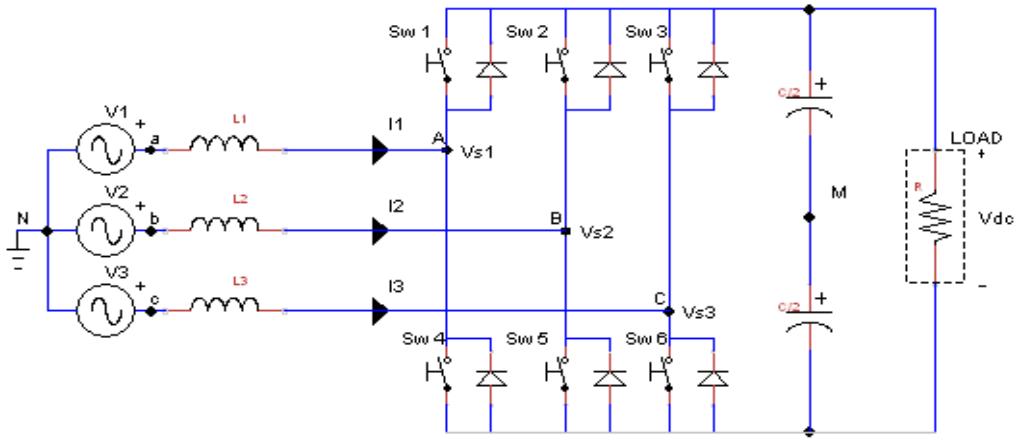


Figure 3: Three phase PWM boost converter model with fictitious midpoint *M* at output DC link

Split output DC link capacitance has value of ***C/2*** each. V_{s1}, V_{s2} and V_{s3} are three level synthesized voltages at points ***A***, ***B*** and ***C*** in Fig.3 respectively with respect to source neutral. A simulation plot of synthesized voltage V_{s1} is shown in Fig. 4 for balanced input condition.

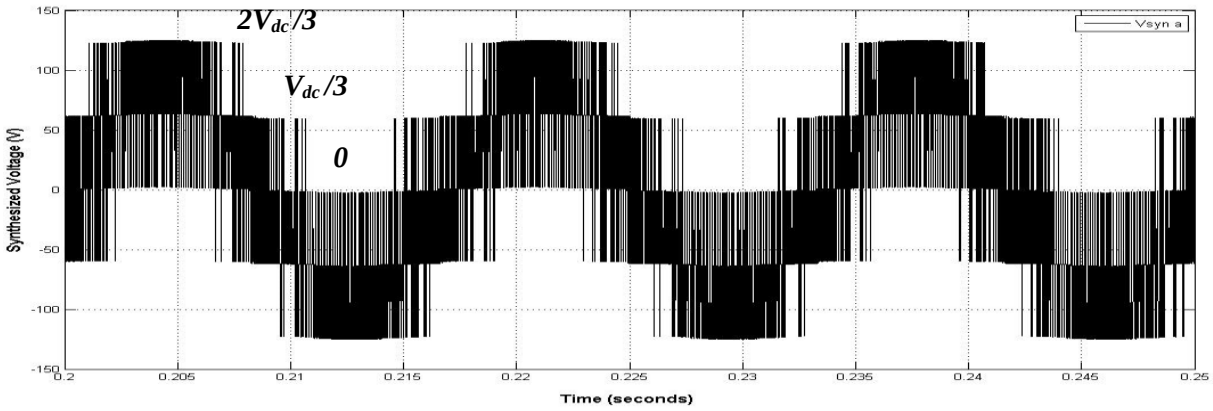


Figure 4: Simulation plot for synthesized voltage V_{s1} at the input of three phase boost converter of phase '**a**'

The voltage takes instantaneous value of ***0***, $\pm V_{dc}/3$ and $\pm 2V_{dc}/3$ depending upon the switching function. The steady state relationship is given by equations (8) - (10) for each phase.

The DC link capacitor of the converter output acts as a DC voltage source in steady state and reflects back at the AC side of the converter (Fig. 3) as three phase two-level ($+V_{dc}$ and ***0***) delta-connected synthesized AC source V_{AB},V_{BC} and V_{CA} as shown in Fig. 5. The current controller uses reference currents calculated in section 2.2 to generate a PWM switching, hence the three phase synthesized voltages V_{AB}, V_{BC} and V_{CA} have a fundamental component with ripple content.

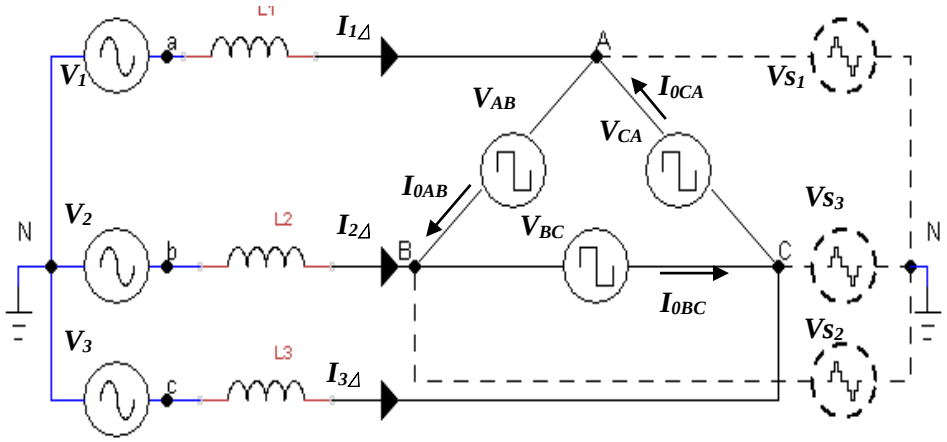


Figure 5: Three phase PWM boost converter average model with DC output voltage reflected to AC side of converter module

The voltage at ***A***, ***B*** and ***C*** with respect to source neutral ***N*** has three level (Fig. 4) due to voltage difference V_{MN} present between points ***M*** and ***N*** (Fig. 3) causing interference between the phases. This interference is removed by connecting ***M*** to source neutral ***N*** or by grounding ***M***. This converts delta-connected synthesized voltage to its star equivalent as shown in Fig. 6.

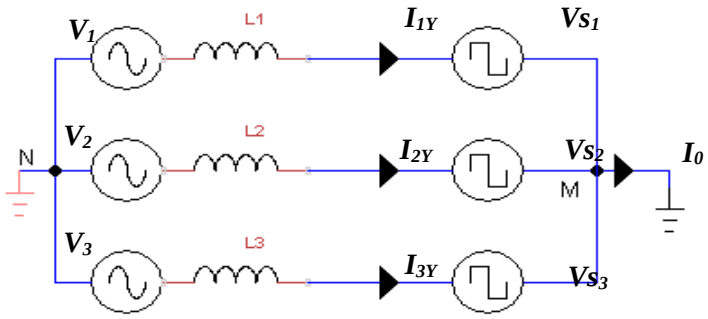


Figure 6: Three phase PWM boost converter model with midpoint *M* grounded at output DC link

The reason for elimination of phase interacting currents, which flow only in the delta-loop between the phases I_{0AB}, I_{0BC}, and I_{0CA} (Fig. 5), is drawn out as neutral current I_0 (Fig. 6) when DC link midpoint ***M*** is grounded. Hence, current equations for Fig. 5 and Fig. 6 are written as

$$I_{1\Delta} + I_{2\Delta} + I_{3\Delta} = 0 \text{ (Floating mid-point } \boldsymbol{M}) \tag{13}$$

$$I_{1Y} + I_{2Y} + I_{3Y} = I_0 \text{ (Grounded mid-point } \boldsymbol{M}) \tag{14}$$

This results in two level ($+V_{dc}/2$ and $-V_{dc}/2$) synthesized voltage (Fig. 6) at ***A***, ***B*** and ***C*** which is essential for constant switching frequency operation as shown in [25]. Fig. 7 shows a typical simulation plot for synthesized voltage V_{s1} (V_{AN}) at AC side of converter for phase '**a**' with DC link midpoint ***M*** grounded for balanced condition.

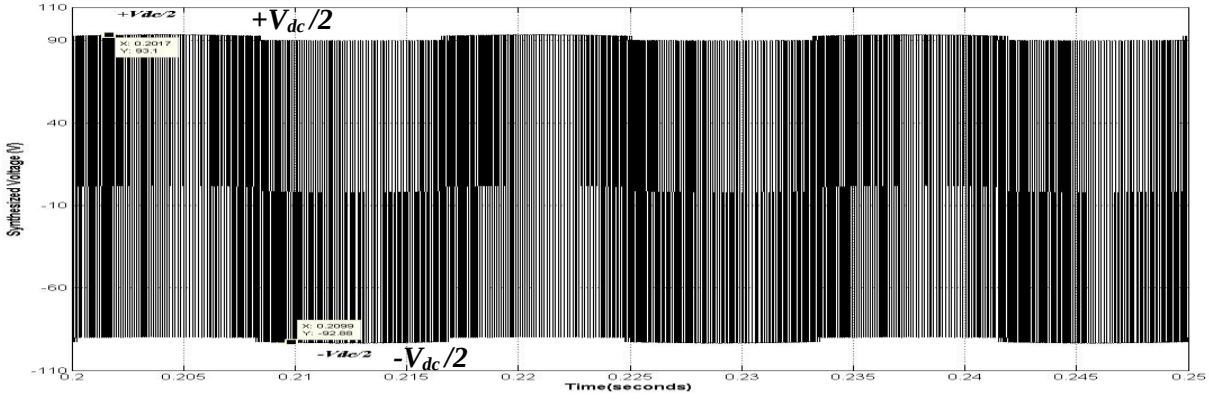


Figure 7: Simulation plot of synthesized voltage V_{s1} at the input of three phase boost converter of phase '**a**' with grounded ***M***

2.4. Calculation of Hysteresis Band for Constant Switching Frequency

With midpoint of the DC link capacitor grounded only two levels of voltages are impressed on the AC side due to output DC link capacitor. Since, the switching frequency is generally much larger than the fundamental frequency of the system, it is assumed that the fundamental component of input voltage source remains constant for one switching period. Consider Fig. 8 a single phase operation of the three phase PWM boost rectifier with midpoint of DC link capacitor grounded. This single phase operation can be extended to all three phases when midpoint ***M*** is grounded, as there is no interaction between the phases.

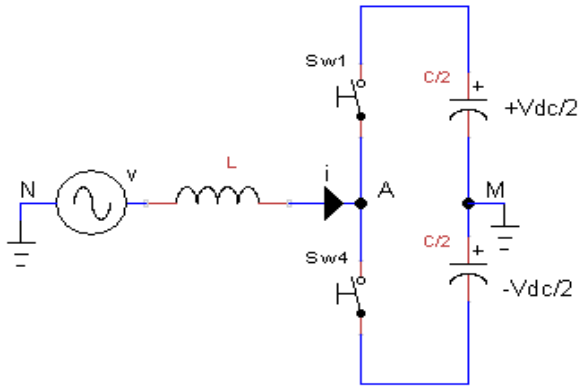


Figure 8: Single phase equivalent circuit with three phase boost rectifier with grounded '*M*'

The relationship for a single phase can be formulated as

$$v = L\frac{di}{dt} + v_A \tag{15}$$

Where $\boldsymbol{v}$ is instantaneous value of input source, $\boldsymbol{i}$ is instantaneous value of current, $\boldsymbol{v_A}$ is instantaneous value of voltage at '*A*' and *L* is value of inductance for input line impedance (neglecting input series resistance). The voltage at point *A* can only take two values ($+V_{dc}/2$) and ($-V_{dc}/2$) in practice. Let $\boldsymbol{i}^*$ be the reference current as calculated in section 2.2 for phase '**a**'. A fictitious reference voltage $\boldsymbol{v_A}^*$ for $\boldsymbol{i}^*$can be calculated using relationship of equation (15) [25].

$$v = L\frac{di^*}{dt} + v_A^* \tag{16}$$

The hysteresis current control uses the difference between reference current and the actual current to generate PWM switching for operation of the converter. Let this difference be error current represented as ***e***. The error current can be defined as

$$e = i^* - i \tag{17}$$

Subtracting (15) from (16) we get

$$L\frac{de}{dt} + (v_A^* - v_A) = 0 \tag{18}$$

The calculation of switching time can be divided into two parts

1. When reference current i^* is in positive half cycle as shown in Fig. 9

2. When reference current i^* is in negative half cycle as shown in Fig. 10

2.4.1. Positive half cycle operation

When the voltage impressed at ***A*** in Fig. 8 is $-V_{dc}/2$ (i.e. $S_{w\,4}$ is ON) the voltage difference between the input source voltage and voltage at ***A*** increases which leads to rise in current. The rising slope of the current depends upon value of inductance ***L*** of input impedance.

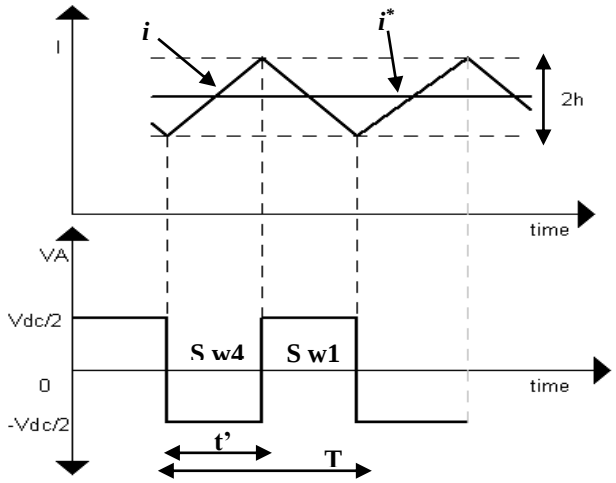


Figure 9: Switching waveform for hysteresis controller for positive cycle of reference current

Equation (18) can be re-written as

$$-(v_A^* - v_A) = L\frac{\Delta e}{\Delta t} \tag{19}$$

Let the time period of the switching cycle be ***T***, hysteresis controller bandwidth be ***2h*** and rising time of the current be ***t'*** as shown in Fig. 9.

So during $0 < t < t'$ equation (19) is expressed as

$$-(v_A^* - v_A) = L \times \left[\frac{e(t') - e(0)}{t' - 0} \right] \tag{20}$$

$$-(v_A^* + \frac{V_{dc}}{2}) = L \times \left[\frac{-h - h}{t' - 0} \right] \tag{21}$$

and during period $t' < t < T$ voltage at ***A*** is $+V_{dc}/2$ ($S_{w\,1}$ is ON) the voltage difference between the input source voltage and voltage at ***A*** decreases hence current decreases. Hence the equation (19) can be written as

$$-(v_A^* - v_A) = L \times \left[\frac{e(T) - e(t')}{T - t'} \right] \tag{22}$$

$$-(v_A^* - \frac{V_{dc}}{2}) = L \times \left[\frac{h + h}{T - t'} \right] \tag{23}$$

Solving for ***T*** we get

$$T = \frac{2 \times h \times L \times V_{dc}}{\left(\frac{V_{dc}}{2} \right)^2 - \left(v_A^* \right)^2} \tag{24}$$

2.4.2. Negative half cycle operation

Fig. 10 shows the negative cycle operation of the hysteresis controller. During this operation Switch $S_{w\,1}$ in Fig. 8 is ON to get negative slope of the line current and $S_{w\,4}$ is ON to get positive slope of the line current. The calculation of time period ***T*** required for switching is calculated below. When slope of current is negative $0 < t < t''$ equation (19) can be written as

$$-(v_A^* - \frac{V_{dc}}{2}) = L \times \left[\frac{h + h}{t'' - 0} \right] \tag{25}$$

When slope of current is positive $t'' < t < T$ equation (19) can be expressed as

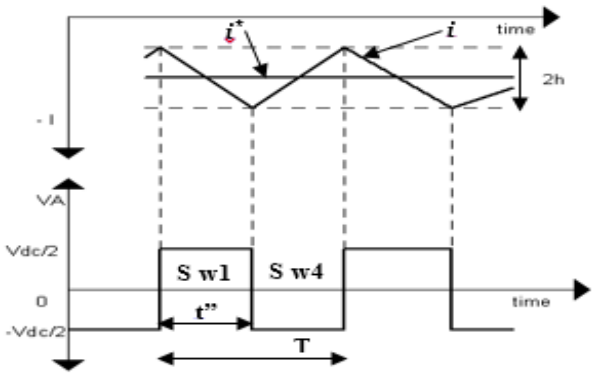


Figure 10: Switching waveform for hysteresis controller for negative cycle of reference current

$$-(v_A^* + \frac{V_{dc}}{2}) = L \times \left[\frac{-h-h}{T-t''}\right] \tag{26}$$

Solving equation (25) and (26) for $\boldsymbol{T}$ we get

$$T = \frac{2 \times h \times L \times V_{dc}}{\left(\frac{V_{dc}}{2}\right)^2 - \left(v_A^*\right)^2} \tag{27}$$

Equation (27) is principally same as that of equation (24) and with one variable $\boldsymbol{v_A^*}$. The difference is due to the operation cycle for both conditions. As (24) represents solution for positive cycle where the value of known quantities $\boldsymbol{v}$ and $\boldsymbol{i^*}$ is positive, solving for $\boldsymbol{v_A^*}$ equation (16) can be written as

$$v_A^* = v - L\frac{di^*}{dt} \tag{28}$$

The value of both $\boldsymbol{v}$ and $\boldsymbol{i^*}$ is negative for equation (26) as it is negative cycle operation and to solve for $\boldsymbol{v_A^*}$.equation (16) can be written as

$$v_A^* = (-v) - L\frac{d(-i^*)}{dt} \tag{29}$$

General equation for (24) and (27) can be expressed as

$$T = \frac{2 \times h \times L \times V_{dc}}{\left(\frac{V_{dc}}{2}\right)^2 - \left(|v| - L\frac{d|i^*|}{dt}\right)^2} \tag{30}$$

The switching frequency f_s for the operation of three phase PWM boost type converter can be given as the reciprocal of equation (30)

$$f_s = \frac{1}{T} = \frac{\left(\frac{V_{dc}}{2}\right)^2 - \left(|v| - L\frac{d|i^*|}{dt}\right)^2}{2 \times h \times L \times V_{dc}} \tag{31}$$

In order to make switching frequency constant only one parameter can be varied and that is bandwidth of the hysteresis controller '***h***' in above equation (31). All other parameters are given. Rewriting the equation (30) for preset value of switching frequency f_s we get

$$h = \frac{\left(\frac{V_{dc}}{2}\right)^2 - \left(|v| - L\frac{d|i^*|}{dt}\right)^2}{2 \times f_s \times L \times V_{dc}} \tag{32}$$

Equation (32) presents instantaneous value of the bandwidth of hysteresis controller ***h*** required to keep the switching frequency constant at a preset value f_s. A variable bandwidth hysteresis controller is required for switching frequency f_s to be constant. A typical simulation plot of the bandwidth ***h*** with respect to its input source voltage for single phase shown in Fig. 11.

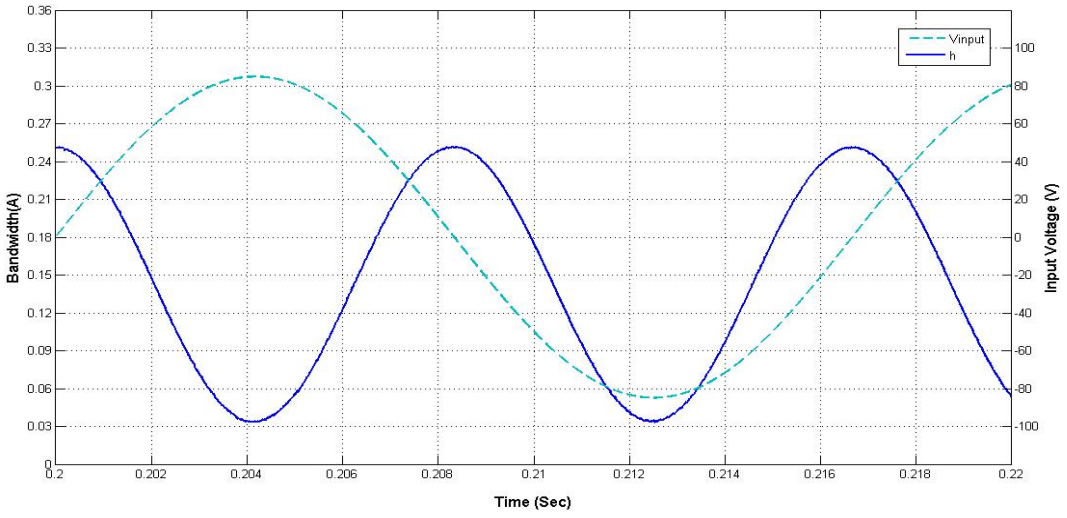


Figure 11: Hysteresis bandwidth '***h***' and input voltage 'V_{input}' for phase '**a**'

The hysteresis bandwidth ***h*** varies in time and is periodic in nature. The plot suggests the frequency of hysteresis bandwidth plot is twice as that of fundamental frequency and is cosine in nature as it is shifted by 90^0 from the fundamental component.

2.5. Constant Switching Condition for Floating Midpoint *M*

The method developed in the previous section is applicable only when the midpoint ***M*** of the DC link is grounded for three phase PWM boost rectifier (Fig. 3). A general method is developed for avoiding interaction of phases due to presence of interacting voltage at point ***M*** with respect to source neutral ***N*** [26] under balanced input condition for inverter. As the method used for calculation of reference currents for harmonic elimination in extreme unbalanced conditions requires the midpoint ***M*** floating as shown in the equation (5), it is desirable to develop a generalized method to decouple the interacting voltage from the delta-connected synthesized voltage with floating ***M***.

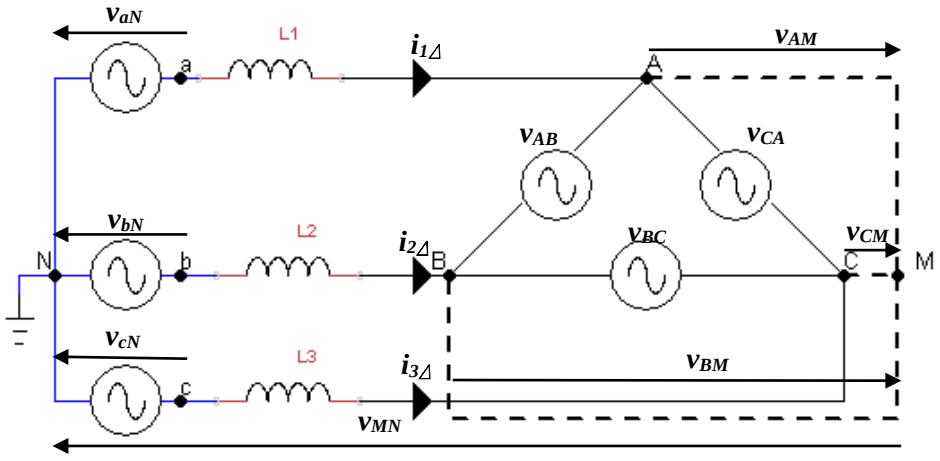


Figure 12: Equivalent circuit of three phase PWM boost rectifier with midpoint floating

Fig. 12 shows the equivalent average model of the converter from Fig. 5 considering floating mid-point ***M*** of the DC link capacitor and fundamental component of delta-connected synthesized voltages. This model is not symmetrical and represents unbalanced operation of the three phase boost converter. The synthesized voltage for each phase at point ***A***, ***B*** and ***C*** referred can be presented as

$$v_{AN} = v_{AM} + v_{MN} \tag{33}$$

$$v_{BN} = v_{BM} + v_{MN} \tag{34}$$

$$v_{CN} = v_{CM} + v_{MN} \tag{35}$$

As the midpoint ***M*** and the source neutral ***N*** is not connected v_{AM}, v_{BM} and v_{CM} are the voltages at point ***A***, ***B*** and ***C*** as referred to ***M*** respectively and v_{MN} is the interacting voltage developed between midpoint ***M*** and source neutral ***N***.

If the connection between DC midpoint ***M*** and source neutral ***N*** is assumed to be grounded in Fig. 12 then a neutral current i_0 flows through the connection ***MN*** as shown in equation (14). The synthesized voltage v_{AM}, v_{BM} and v_{CM} are connected in star and each phase can be evaluated independently as interacting current i_0 is drawn out from the line current with ground ***M***.

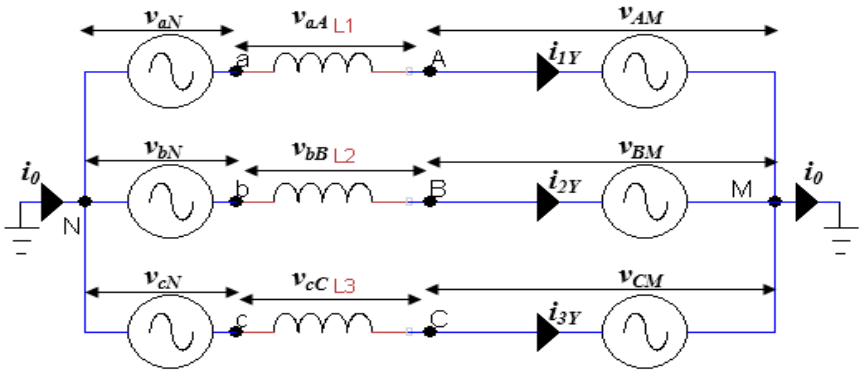


Figure 13: Equivalent Circuit for three phase PWM Converter with DC link mid-point grounded

From Fig. 13 we can express the neutral current flowing as

$$i_0 = i_{1Y} + i_{2Y} + i_{3Y} \tag{36}$$

where i_{1Y}, i_{2Y} and i_{3Y} are current flowing through L_1, L_2 and L_3 respectively and voltage drop across them is v_{aA}, v_{bB} and v_{cC} respectively, the relationship can be expressed as

$$v_{aA} = L_1 \frac{di_{1Y}}{dt}; \text{hence} \quad i_{1Y} = \frac{1}{L_1}\int v_{aA}\,dt \tag{37}$$

$$v_{bB} = L_2 \frac{di_{2Y}}{dt}; \text{hence} \quad i_{2Y} = \frac{1}{L_2}\int v_{bB}\,dt \tag{38}$$

$$v_{cC} = L_3 \frac{di_{3Y}}{dt}; \text{hence} \quad i_{3Y} = \frac{1}{L_3}\int v_{cC}\,dt \tag{39}$$

To calculate the line current flowing in each phase, three single phase equivalent circuit from Figure 13 and they are shown in Figure 14(a), 14(b) and 14(c).

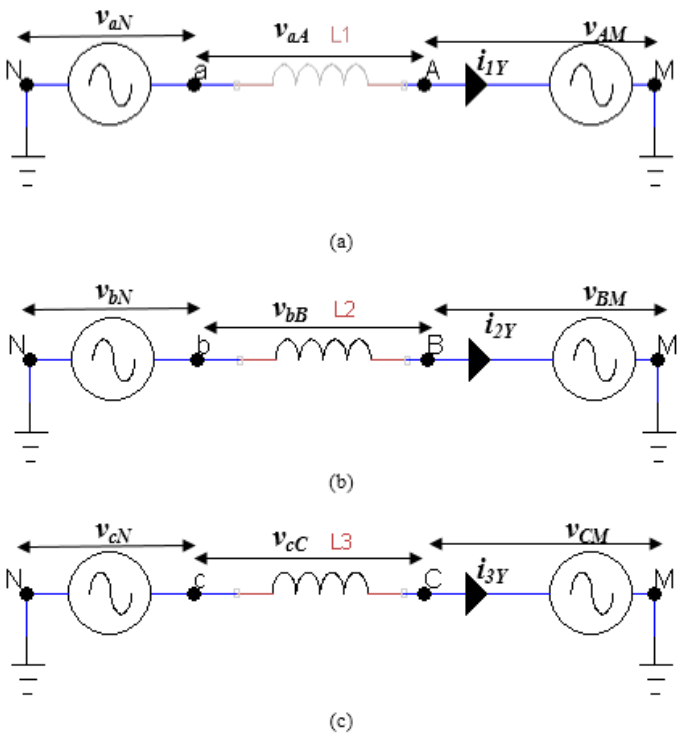


Figure 14: Single phase equivalent circuit for grounded DC mid-point (a) phase 'a', (b) phase 'b' and (c) phase 'c'

As with ***M*** grounded

$$v_{AM} = v_{AN}\ ;\ v_{BM} = v_{BN}\ ;\ v_{CM} = v_{CN} \tag{40}$$

From Fig. 14 with Kirchhoff's voltage law we derived voltage across input inductance as

$$v_{aA} = v_{aN} - v_{AM} \tag{41}$$

$$v_{bB} = v_{bN} - v_{BM} \tag{42}$$

$$v_{cC} = v_{cN} - v_{CM} \tag{43}$$

By using equations (37)-(43) in (36) we can express the neutral current flowing in each phase in terms of voltage difference between the input source voltage and the synthesized voltage which is connected in star due to grounded ***M***. The general expression for neutral current $\boldsymbol{i_0}$ is given by

$$i_0 = \frac{1}{L_1}\int (v_{aN} - v_{AM})dt + \frac{1}{L_2}\int (v_{bN} - v_{BM})dt + \frac{1}{L_3}\int (v_{cN} - v_{CM})dt \tag{44}$$

Where the star connected line currents $i_{1Y,}$ $i_{2Y,}$ and i_{3Y} through input inductors is given by

$$i_{1Y} = \frac{1}{L_1}\int (v_{aN} - v_{AM})dt \tag{45}$$

$$i_{2Y} = \frac{1}{L_1}\int (v_{bN} - v_{BM})dt \tag{46}$$

$$i_{3Y} = \frac{1}{L_3}\int (v_{cN} - v_{CM})dt \tag{47}$$

When the mid-point ***M*** is floating the synthesized voltage referred at point ***A***,***B*** and ***C*** referred to ***N***, v_{AN} , can be resolved into two components as shown in equation (33), (34) and (35). The component which is responsible for generation of star connected line current i_{1Y}, $i_{2Y,}$ and i_{3Y} depends on the voltage across the input inductors as shown in equations (45), (46) and (47).

When the synthesized voltage is connected in delta, the voltage across the inductor with floating mid-point ***M*** is given by substituting equation (33), (34) and (35) in (41), (42) and (43) respectively

$$v_{aA} = v_{aN} - v_{AM} - v_{MN} \tag{48}$$

$$v_{bB} = v_{bN} - v_{BM} - v_{MN} \tag{49}$$

$$v_{cC} = v_{cN} - v_{CM} - v_{MN} \tag{50}$$

The currents $i_{1\triangle}$, $i_{2\triangle}$ and $i_{3\triangle}$ (Fig. 12) flowing through the inductor can be given by

$$i_{1\Delta} = \frac{1}{L_1}\int (v_{aN} - v_{AM} - v_{MN})dt \tag{51}$$

$$i_{2\Delta} = \frac{1}{L_2}\int (v_{bN} - v_{BM} - v_{MN})dt \tag{52}$$

$$i_{3\Delta} = \frac{1}{L_3}\int (v_{cN} - v_{CM} - v_{MN})dt \tag{53}$$

A relationship can be derived between currents flowing through input inductors for star-connected synthesized voltages ($\boldsymbol{i_{iY}}$), current flowing through input inductors for delta-connected synthesized voltages ($\boldsymbol{i_{i\Delta}}$) and voltage difference between mid-point ***M*** and source neutral ***N*** from the above equations (51), (52) and (53). The subscript *i* represent phase 1, 2 and 3.

$$\frac{1}{L_1}\int (v_{aN} - v_{AM})dt = i_{1\Delta} + \frac{1}{L_1}\int v_{MN}\,dt \tag{54}$$

$$\frac{1}{L_2}\int (v_{bN} - v_{BM})dt = i_{2\Delta} + \frac{1}{L_2}\int v_{MN}\,dt \tag{55}$$

$$\underbrace{\frac{1}{L_3}\int (v_{cN} - v_{CM})dt}_{\boldsymbol{i_{iY}}} = \underbrace{i_{3\Delta}}_{} + \underbrace{\frac{1}{L_3}\int v_{MN}\,dt}_{\boldsymbol{i_{0i}}} \tag{56}$$

The equations (54), (55) and (56) shows the relationship between the current flowing through the input inductors for delta-connected synthesized voltages (midpoint ***M*** floating) and for star-connected synthesized voltages (midpoint ***M*** grounded). The constant switching frequency can be only achieved with independent operation of three phases for which star connection of synthesized voltage is essential. But, grounded ***M*** introduces neutral current in the line current which is responsible for undesired third harmonic presence in the input currents.

In order to have benefit of star connection for implementation of constant switching frequency while having floating midpoint, the three phase PWM boost rectifier must appear to have mid-point grounded for the hysteresis current controller (HCC). This concept is implemented in [26] for balanced condition with equal input impedances.

The additional current '$\boldsymbol{i_{0i}}$', which is neutral current flowing in each phase, when added to current flowing through inductor for delta connected synthesized voltages '$\boldsymbol{i_{i\Delta}}$' (midpoint ***M*** floating), respectively, is equal to the current flowing through inductor for star connected synthesized voltage (midpoint ***M*** grounded). The current '$\boldsymbol{i_{0i}}$' can be calculated for each phase by measuring voltage difference between the ***M*** and ***N*** with equation (57)

$$i_{0i} = \frac{1}{L_i}\int v_{MN}\,dt \text{ ; Where } \boldsymbol{i} = 1, 2 \text{ and } 3 \text{ representing three phases} \tag{57}$$

The line currents flowing through input impedances for floating midpoint three phase PWM boost type rectifier '$i_{i\Delta}$ ' is known parameter as it is measured during the operation of the converter. Hence, the current flowing for equivalent star connected synthesized voltages can be calculated from a generalized equation (58)

$$i_{iY} = i_{i\Delta} + i_{0i} \text{ ; Where } \boldsymbol{i} = 1, 2 \text{ and } 3 \text{ representing three phases} \quad (58)$$

The addition of the calculated current 'i_{0i}' equation (57) is done in the current controller using equation (58). This makes the delta connected synthesized voltage (floating ***M***) appear star connected (grounded ***M***) for the current controller. This is shown as fictitious connection between point ***M*** and ***N*** in Fig. 15

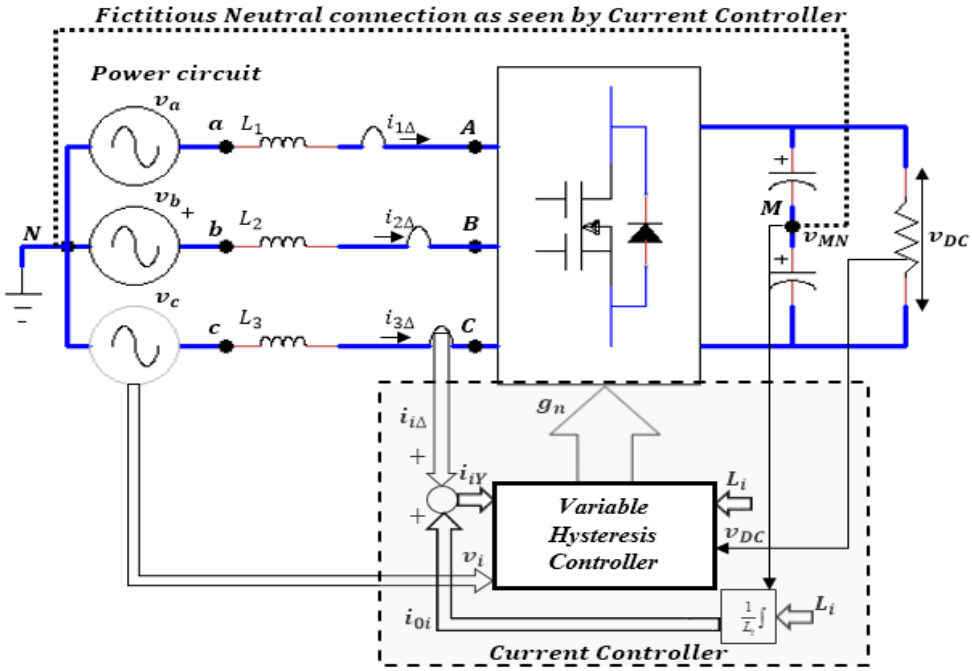


Figure 15: Equivalent circuit of three phase PWM boost rectifier as appeared to the current controller by adding calculated neutral current 'i_{0i}' to measured current '$i_{i\Delta}$' per phase respectively.

All the delta currents $i_{1\Delta}$, $i_{2\Delta}$ and $i_{3\Delta}$ is given as

$$i_{1\Delta} + i_{2\Delta} + i_{3\Delta} = 0 \quad (59)$$

The fictitious connection has the total neutral current flowing from point ***M*** to ***N*** due to the presence of interacting voltage v_{MN} and can be expressed as in (60)

$$i_0 = i_{01} + i_{02} + i_{03} \quad (60)$$

where i_0 is current flowing between M and N through fictitious connection and i_{01}, i_{02} and i_{03} are the current flowing through input line inductors L_1, L_2 and L_3 to make the delta connected synthesized voltage of the converter appear as star connected for the current controller.

$$i_0 = \left(\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}\right) \times \int (v_{MN})dt \tag{61}$$

Equation (61) gives the generalized value of neutral current flowing when point M and N are connected for all level of imbalances in input voltages and input impedances. Next section goes through the implementation of current controller for achieving constant switching frequency under extreme unbalanced condition and the constraints of the solution presented.

2.6. Variable Hysteresis Controller Implementation and Solution Constraints

2.6.1. Variable Hysteresis Controller Implementation

Fig 16 shows the method of implementation in current controller. Line current of each phase ($i_{i\Delta}$) is measured, subscript (i = *1, 2 and 3*) represents each phase. Neutral current is calculated using equations (57) from measured voltage (v_{MN}) between DC link capacitor midpoint (M) and source neutral current (N).

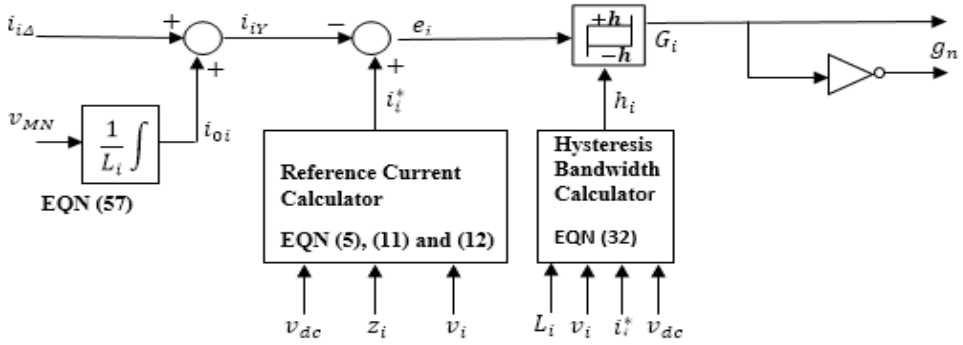


Figure 16: Schematic diagram for implementation of current controller as a variable hysteresis controller for each phase

The output of addition of measured line current and the zero sequence current is then compared with reference current calculated using equations (5), (11) and (12). The error current thus produced is given to a variable bandwidth hysteresis controller. This hysteresis controller is

provided the value of hysteresis bandwidth using equation (32). The output of the hysteresis controller is logic signal (G_i) which is then converted to gating signals (g_n) used for operation of converter's MOSFET/IGBT bridges for near constant frequency operation of the three phase PWM boost converter. Six gating signals are generated for three phase operation subscript *n* gives number of signals generated.

The above current controller is shown for single phase generation of logic signal. It can be easily extended to three phase. All the measured or set input parameters used for calculation of the reference current, the zero sequence current and the bandwidth is given above for closed loop operation of the system.

Fig. 17 shows full schematic of implementation method for achieving near constant switching frequency for extremely unbalanced condition for three phase boost converter. All the signals represented with subscript '*i*' are three phase signals. Six gate pulses g_n implements the logic switching to attain near constant switching frequency at pre-set value of f_s.

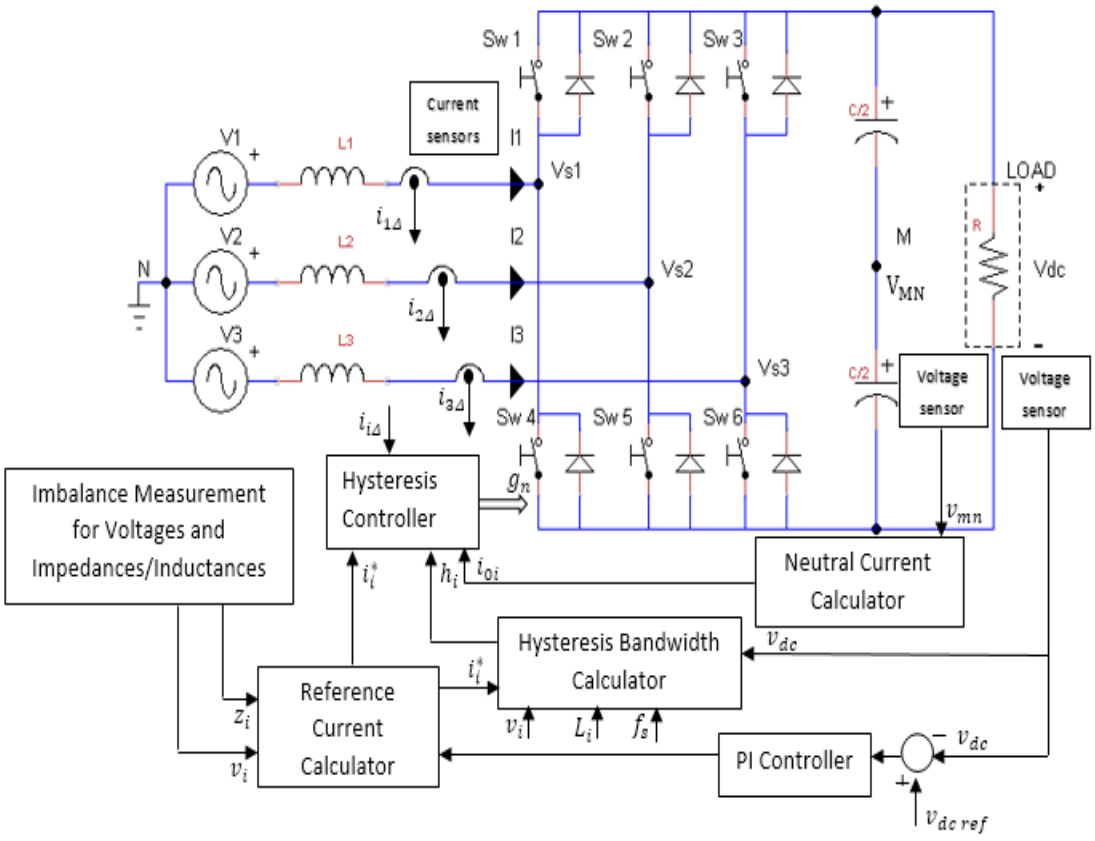


Figure 17: Schematic diagram for implementation of three phase PWM boost converter for unbalanced operation with near constant switching frequency f_{sw} in closed loop operation

2.6.2. Constraints of the Solutions

The solution presented in this chapter has some constraints. These are required for correct calculations of references, effective implementation of switching signals and during calculation of zero sequence current or neutral current and bandwidth for variable hysteresis controller. The constraints required for correct calculation of references and effective implementation of switching signals are explained in details in [15].

As the neutral current calculation is given by relationship as shown in (57)

$$i_{0i} = \frac{1}{L_i}\int (v_{MN})dt$$

This current has inverse relationship with input inductance. For extremely unbalanced conditions of input impedance requires input impedance to zero. This will result in increasing the value of neutral current to infinite. Hence, it cannot be used for zero value of input impedance faults.

The calculation of hysteresis bandwidth is related as given in equation (62) for three phase

$$h_i = \frac{\left(\frac{V_{dc}}{2}\right)^2 - \left(|v_i| - L_i \frac{d|i_i^*|}{dt}\right)^2}{2 \times f_s \times L_i \times V_{dc}} \tag{62}$$

The bandwidth ***h*** depends on the values of output dc voltage, source instantaneous value of voltage, source input inductance, reference current and frequency of operation set. As for extreme imbalance in impedance requires value of inductance to be zero, it makes the value of bandwidth required for near constant switching frequency infinity.

But, input line currents are constrained by equation (63) hence, the value bandwidth does not affect value of line current.

$$i_{1\Delta} + i_{2\Delta} + i_{3\Delta} = 0 \tag{63}$$

Due to inverse relationship of bandwidth and neutral current to the inductance of input impedances the condition of unbalance in impedances is only verified for big imbalance condition. To prove this method for unbalance impedance condition, the impedance of unbalance branch is reduced by ten times.

As to calculate the hysteresis bandwidth accurate measurement of the signal $\boldsymbol{V_{mn}}$ is of very essential. As this signal is very small and close to zero

Using the constraints defined above the method to achieve near constant frequency with unbalanced operation of three phase boost rectifier is developed. The method calculates the reference values of current using harmonic elimination method in extreme unbalanced condition. A method is devised to implement to achieve near switching constant frequency. Then this method is implemented on the topology of boost converter used by eliminating the interaction of phases during unbalanced operation.

Unlike [26] where the calculated neutral current equation flowing through fictitious connection between $\boldsymbol{M}$ and $\boldsymbol{N}$ is valid only for balanced operation of the three phase PWM boost converter, this method presents a generalized solution for calculating the neutral current under various unbalanced condition for input voltages and input impedances. This method is used for achieving constant switching frequency in various extremely unbalanced condition.

The method derived above can be easily implemented using computer programs. A simulation and experimental model can be build using analytic solution provided in this chapter to verify the method developed. Next chapter explains the method of developing such model. The solution is verified by using various plots and comparing it with conventional method as used in [15].

The method is effective for achieving near constant switching frequency under extreme unbalanced condition for three phase PWM boost converter. It provides solution for all levels of unbalances in voltages and constrained level unbalances in impedances.

Chapter III

SIMULATION RESULTS

In the last chapter we have proposed the theoretical and mathematical analysis of the method discussed. To prove this method a simulation model has been built using MATLAB/Simulink's SimPowerSystems module. Three phase input voltages and the line impedances are measured known quantities. Complex power is predetermined by selection of DC link parameter as required for a specific resistive load. The switching frequency of the system is predetermined and the value is assumed at an achievable limit. The DC link mid-point voltage is also measured and is considered as known quantity. A MATLAB m-file is built to calculate magnitude and phase angle of three phase reference current. This m-file is used to calculate the reference current for input-output harmonic elimination based on the equations (5), (11) and (12). Switching frequency of the converter is predetermined and is used for calculation of bandwidth in hysteresis controller using (32). The three phase hysteresis controller used is not fixed, but variable in nature. The value of bandwidth calculated is used to decide the upper limit and lower limit of the hysteresis controllers.

The proposed control method is used in the simulation model for seven different cases of extremely unbalanced input conditions. First open loop configuration analysis is done to establish feasibility of the method and then closed loop operation is also implemented. In all cases we operate at unity power factor with switching frequency held near constant at pre-determined value.

3.1 Simulation Model

The PWM boost type rectifier is operated using the proposed near constant switching frequency method. The input-output harmonic elimination method is used to calculate the magnitude and phase angle of the reference currents. The circuit diagram of the simulation model is shown in Fig. 18. There are three input sinusoidal voltage sources, representing a three phase input supply. Three input inductors connected with the three phases represent the input impedances. There are six IGBTs connected with anti-parallel diode representing the bidirectional switches of the PWM three phase boost rectifier. The rectifier output is given to two identical series-connected DC link capacitors. The voltage at midpoint of the two capacitors, with respect to AC side neutral point, is used to calculate neutral current.

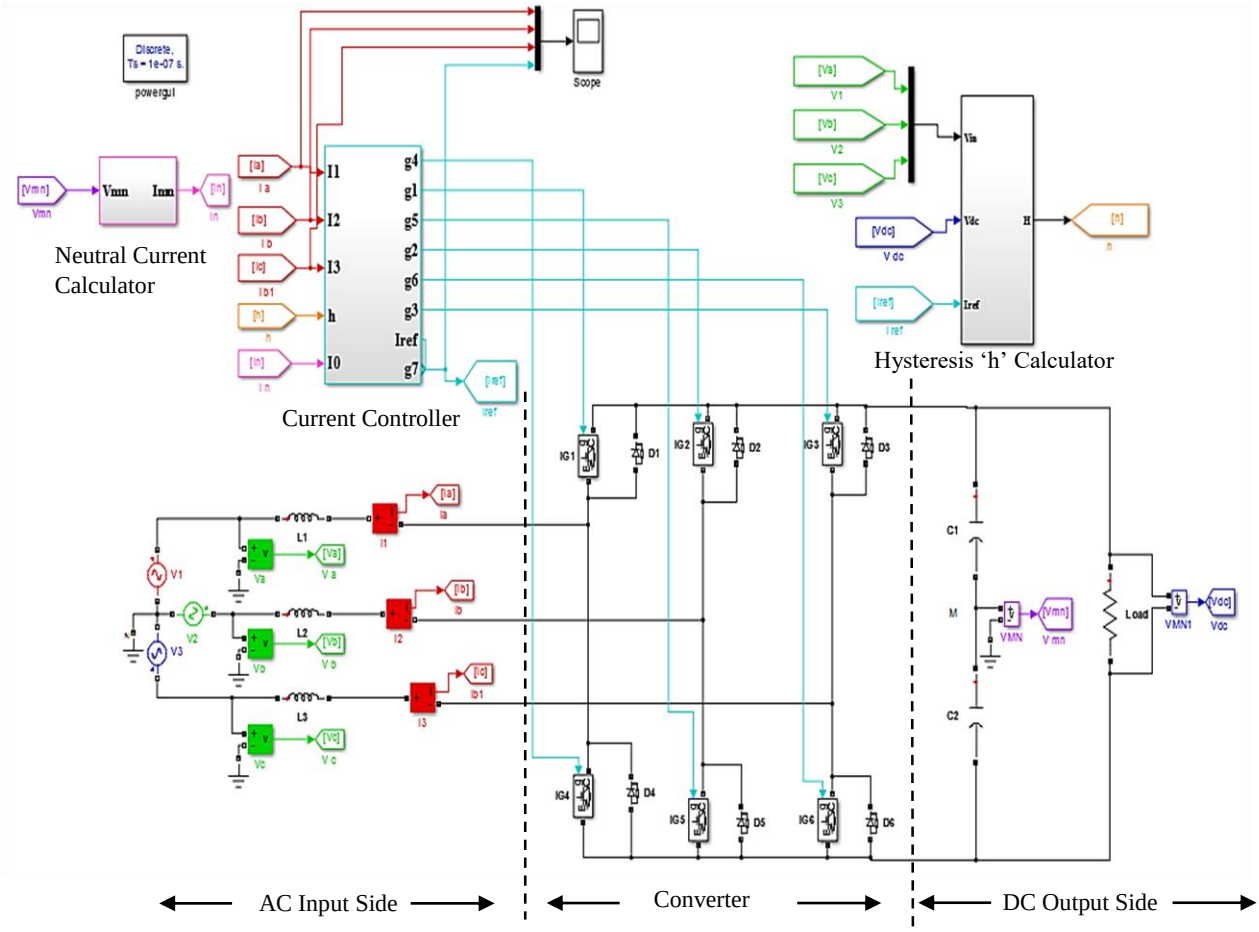


Figure 18: Simulation circuit diagram

The other components of the simulation model are:

1. Current controller
2. Hysteresis bandwidth ‘h’ calculator
3. Neutral current calculator

3.1.1 Current controller

The current controller here is a hysteresis controller with variable bandwidth and is used to track line current of all the three phases independently. Measured value of three phase currents (***I_a, I_b, I_c***), calculated neutral current (***I_0***) from Neutral Current Calculation box, and hysteresis bandwidth (***h***) which is calculated from ***h*** Calculation box, are inputs to the controller as shown in Fig. 19. The output of the controller gives gate signals to all six IGBTs of the converter module. Measured three phase line currents are added to calculated neutral current ‘***I_0***’ in order to implement the fictitious connection between mid-point of DC link voltage and neutral point of AC circuit. In Simulink, the ready built block ‘Relay,’ which is generally used to implement a hysteresis controller and can take only constant value as bandwidth. Hence, a new type of User Defined MATLAB function block ‘myrelay’ is built to implement the variable hysteresis controller; Fig. 20 shows the implementation of variable bandwidth hysteresis current controller relay.

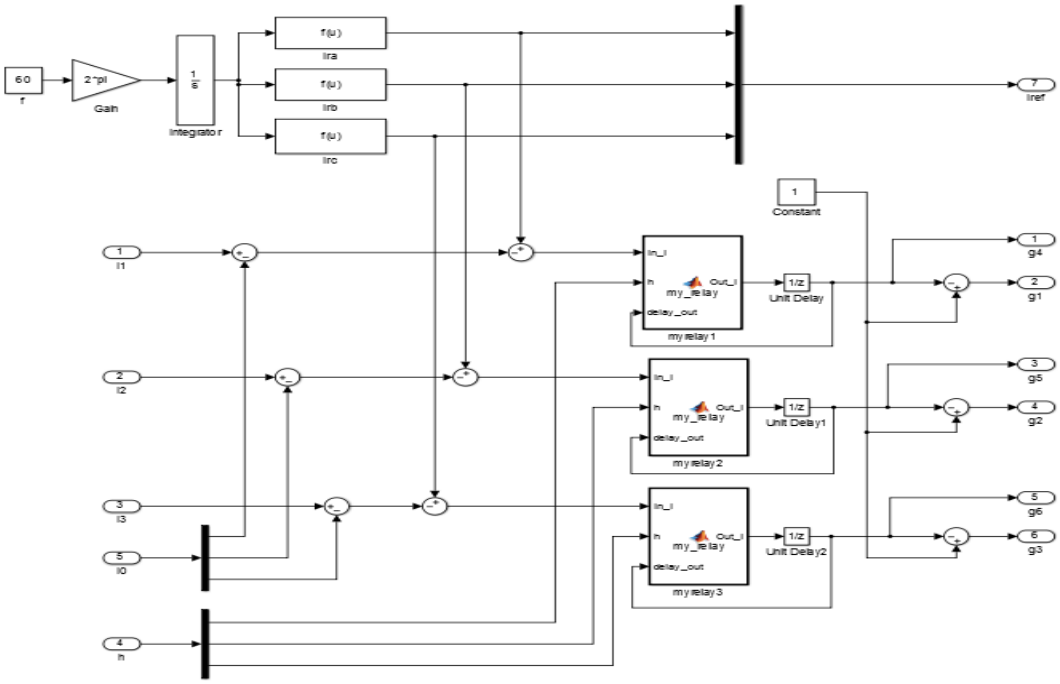


Figure 19: Current controller schematic

The program of the block is attached in the Appendix (A.3.). We have three inputs to the hysteresis block viz. calculated bandwidth (***h***), error current (***In_I***), and previous state input (***delay_out***) implemented by 'unit delay' block or 'memory block' in Simulink. The function block uses a simple logic in implementation. The logic is stated below:

$$In\_I >= +h \text{ , } Out\_I = 1$$

$$In\_I <= -h \text{ , } Out\_I = 0$$

$$+h < In\_I < -h, Out\_I = Previous\ Gate\ State$$

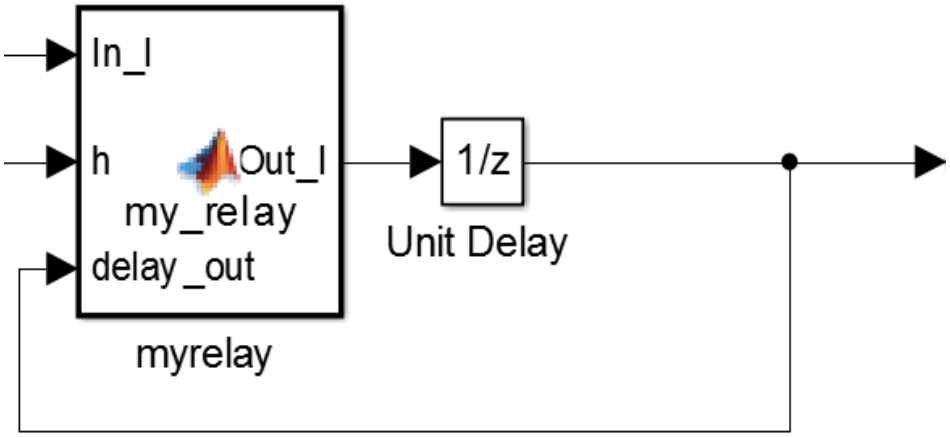


Figure 20: 'myrelay' block

3.1.2 Hysteresis Bandwidth 'h' Calculator

This module is used to calculate the input parameter '***h***' shown in the 'myrelay' block presented in Fig. 20. This is referred to as the bandwidth of the hysteresis controller. It uses calculated three phase reference currents (***I'a***, ***I'b*** and ***I'c*** in Fig. 19), measured three phase input voltages (***Va***, ***Vb***, ***Vc***) input impedances (***La***, ***Lb***, ***Lc***) of each phase and output DC voltage to calculate the value of bandwidth. The switching frequency is predetermined according to operation of the converter. The '***h***' calculator gives a three phase output which is then used by three independent variable bandwidth relays 'myrelay,' to give the gate switching output of the IGBTs. It is

implemented using MATLAB function block. The m-file associated with the algorithm is given in the Appendix (A.2.).

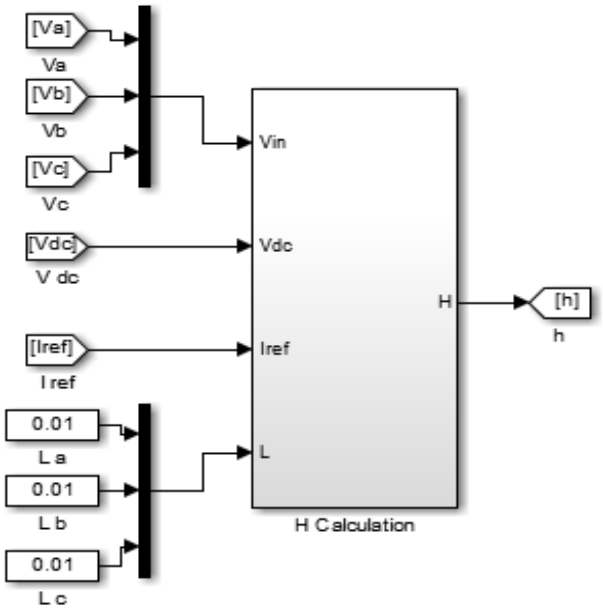


Figure 21: Hysteresis bandwidth 'h' Calculation Module

Fig. 21 shows all the inputs and outputs of bandwidth calculation module. Calculation is based on the equations (32) described in previous chapter.

3.1.3 Neutral Current Calculator

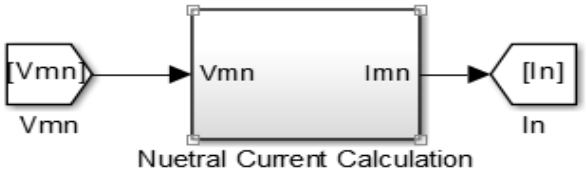


Figure 22: Neutral Current Calculation Module

PWM Boost rectifier does not have neutral current flowing in the circuit as midpoint of the output DC link is not connected with the neutral point of the three phase AC source. Hence, a voltage ($\boldsymbol{V_{mn}}$) exists between the DC link midpoint $\boldsymbol{M}$ and source neutral $\boldsymbol{N}$. In order to make the line current independent from phase interaction, neutral current (I_n) in Fig. 22 is calculated as given

by equation (57) and added to the line current in Hysteresis Controller Module before comparing it with the references. It makes the controller feel that the midpoint of DC link capacitor is connected to the neutral point. Hence it is called a fictitious connection of DC link to the neutral point in the controller. The figure of Neutral Current Calculation module is shown in Fig. 22. The method of implementing Neutral Current Simulink block is given in Appendix (B.2.)

3.2 Open Loop Operation

3.2.1 Method of Implementation

The open loop operation of PWM boost rectifier can be easily modeled in simulation by assuming all the values of the variables in equations for calculation of reference currents and hysteresis bandwidth calculation module beforehand. Hence, for each operation of the module the value of reference currents and hysteresis bandwidth once calculated are set and do not change. It is also called as feed forward approach.

All the values of unbalanced three phase input voltages and input impedances are defined as pre-measured variables. These variables are taken as constant during the time of operation. The formula used to calculate three phase reference currents is made into MATLAB m-file program and is listed in Appendix (A.1.). This program has to be run before executing the Simulink model of the PWM boost rectifier. The m-file required for calculation of value of bandwidth is listed in Appendix (A.2.). This runs in real time to calculate the value of bandwidth during the time of operation. Hence, it can be said that the reference current calculation is done offline and bandwidth calculation is done online during operation of the rectifier.

The flowchart for open loop operation is given in Fig. 23

3.2.2 Flow Chart for Open Loop Operation

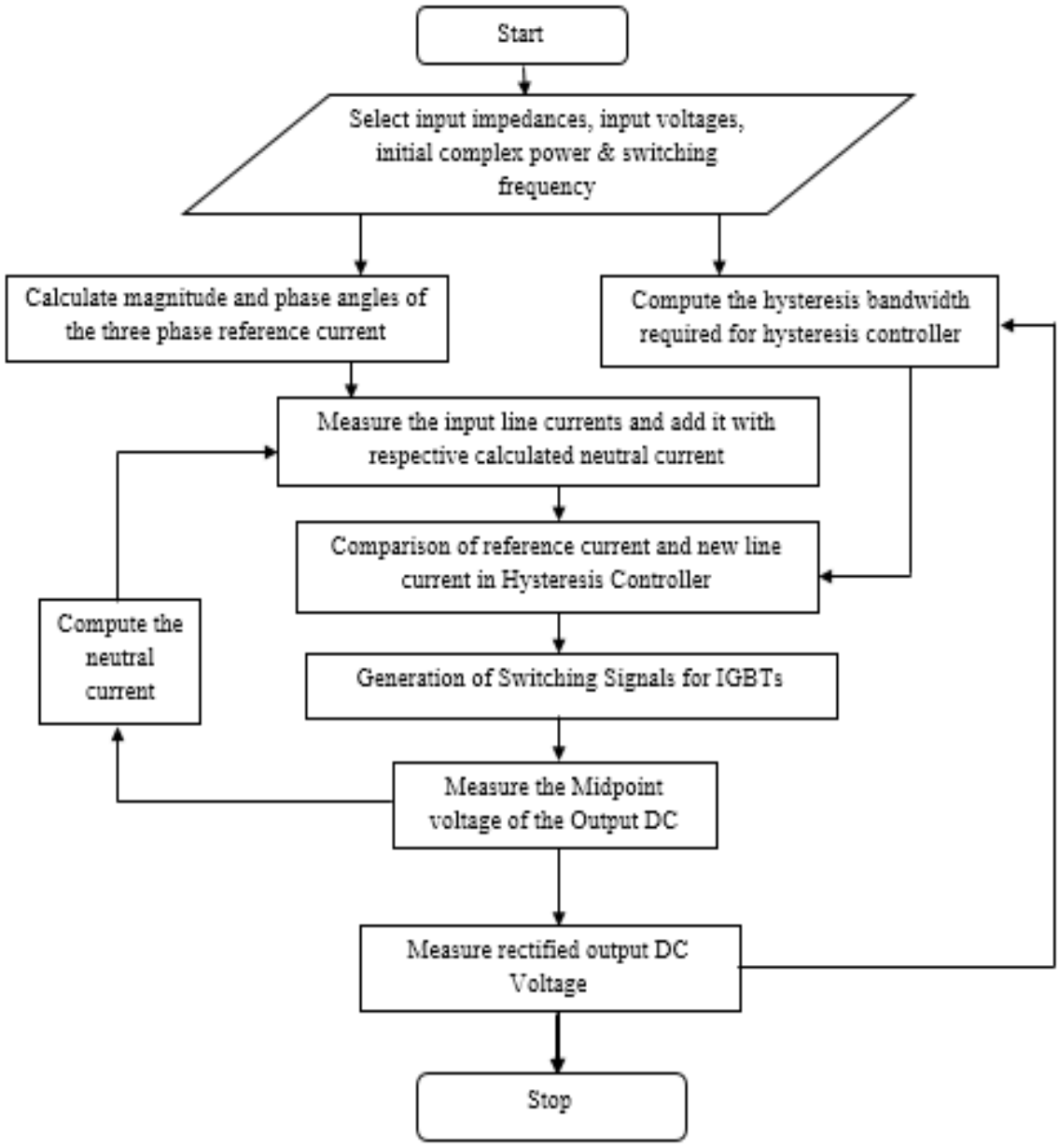


Figure 23: Flowchart of Open Loop Operation

3.3 Closed-Loop Operation

Closed loop operation is performed by controlling the DC output voltage level on line during operation of the PWM boost rectifier. The input impedances and input voltages can be measured and hence are considered as known quantities. As seen in Fig. 24 any change in the output DC voltage value ($V_{dc\ old}$) therefore with respect to set reference output DC voltage ($V_{dc\ ref}$) is measured as error (***DC error***). A voltage controller which is a PI controller (Appendix B.1.) uses error between the reference and the actual output voltage to determine the change in complex power (***S error***). The change in complex power (S_{new}) changes the value of reference current for all the three phases. The Simulink implementation of the voltage controller is shown in the Fig. 24.

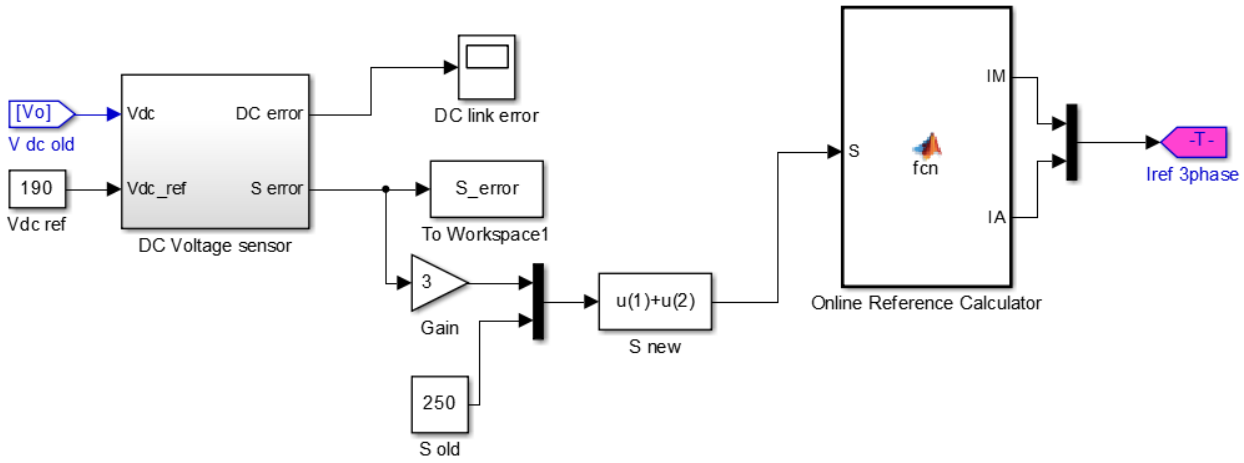


Figure 24: Simulink Model of DC link control for Closed Loop Operation

The reference current calculation uses the equation for input output harmonic elimination method. This online reference calculator (Appendix A.4.) then generates reference current for Hysteresis Controller or Current Controller. The controller tracks the line current and regulates it according to new reference value set at output DC link. The flowchart of the closed loop operation is given in Fig. 25.

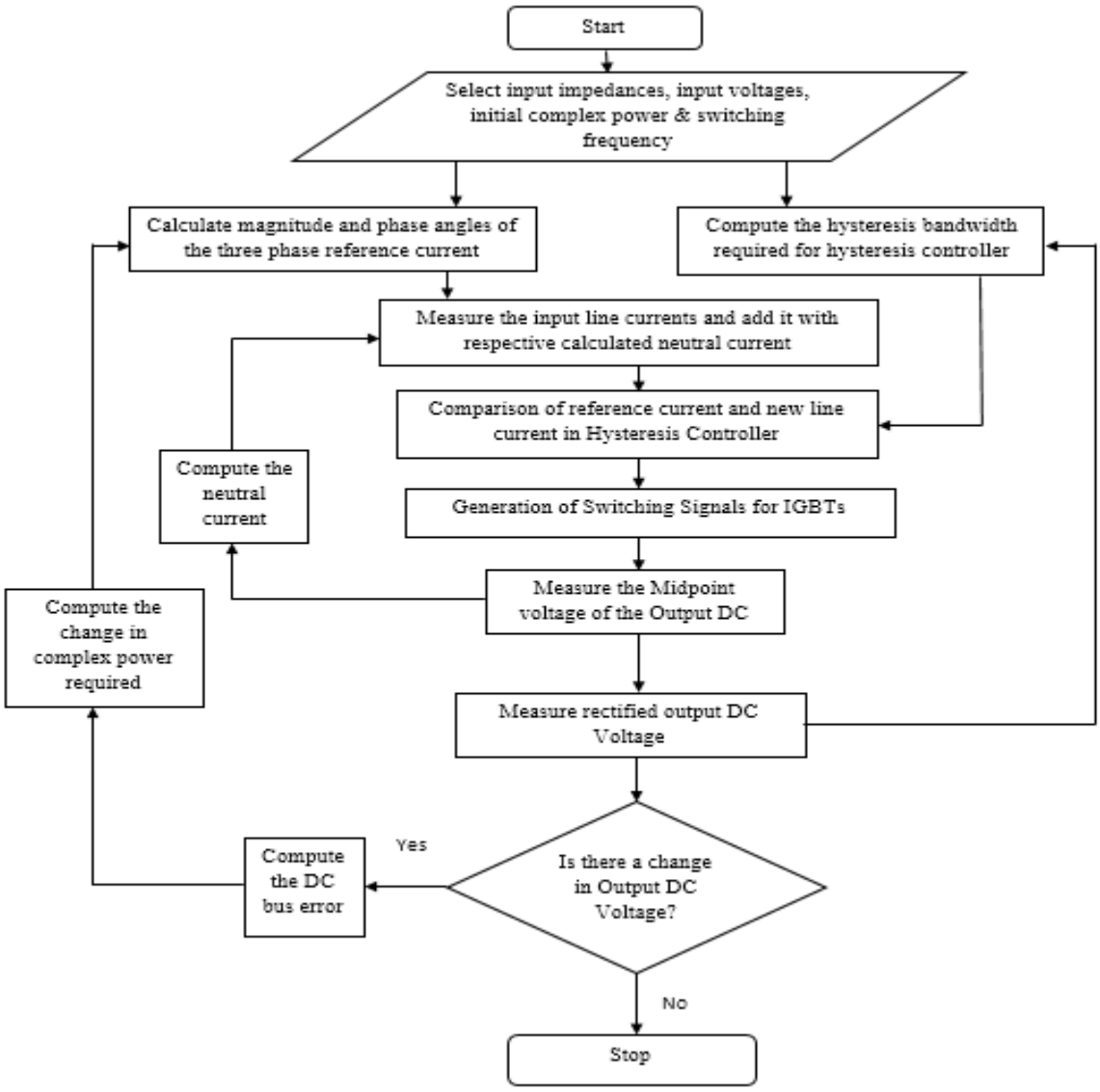


Figure 25: Flow Chart for Closed Loop Operation

There are two types of parameters for the closed loop operation of PWM boost type rectifier.

1. Assumed constant: Input impedances, Input source voltages and Constant switching frequency of the system.
2. Varying online: Output DC voltage, hysteresis bandwidth and reference currents provided to Hysteresis controller.

The MATLAB programs calculates hysteresis bandwidth and reference current are shown in the Appendix A.

3.4 Simulation Results

3.4.1 Open Loop Results

The unbalanced operation of electrical system can be defined in various ways. These unbalances can be in the input impedances of the line, input source voltages or combination of both. Out of all these combinations six extreme unbalanced cases are selected to prove the proposed method. The MATLAB/Simulink model developed for the PWM boost rectifier is simulated for all seven cases for the open loop operation. Simulation for closed loop operation is done for first three cases in order to prove the feasibility of the method. All the cases along with the input conditions and parameters are listed below in Table I.

TABLE I: UNBALANCED CASES

Case #	Input Parameters						Complex Power (VA)	Output Load (Ω)
	Source Voltages (V)			Line Impedances				
	Phase a	Phase b	Phase c	Phase a	Phase b	Phase c		
1	60∠0°	60∠−120°	60∠120°	10mH	10mH	10mH	250	136.9
2	60∠0°	60∠−120°	60∠120°	10mH	1mH	10mH	250	136.9
3	60∠0°	60∠−120°	0	10mH	10mH	10mH	250	136.9
4	60∠0°	60∠−120°	0	10mH	1mH	10mH	250	136.9
5	60∠0°	0	0	10mH	10mH	10mH	100	425.0
6	60∠0°	0	0	1mH	10mH	10mH	100	425.0
7	60∠0°	60∠−180°	0	10mH	10mH	10mH	100	425.0

Simulation parameters, switching devices parameters and component values as taken are provided in Table II and III

TABLE II: SIMULATION PARAMETERS

General Parameters	Values
System fundamental frequency	60 Hz
Switching frequency	9 kHz
Output filter capacitor	100 μF
Switching	Ideal

TABLE III: SWITCH PARAMETERS

Switching Devices	Parameters	Values
IGBT	On Resistance	0.2 Ω
	On Inductance	$7.5*10^{-9}$ H
	Forward Voltage	1 V
Diode	On Resistance	0.4 Ω
	On Inductance	0 H
	Forward Voltage	1.5 V

For all the cases mentioned, one balanced and other six unbalanced, a comparison is provided between the methods of constant hysteresis bandwidth of the hysteresis controller and varying bandwidth to keep switching frequency constant. All the three phase input line currents along with their references generated for input output harmonic elimination are plotted with the output DC link voltage for each case. Fourier plot of all the three line currents for each case is also provided to prove the constant switching result in all the cases.

Case 1 deals with the balanced condition. In this all the input voltages and line impedances are considered balanced. The three phase reference currents are generated with the equation (5), (11) and (12) along with the bandwidth for the current controller using equation (32). The steady state plot of the three phase input line current and output DC link voltage is shown in Fig. 26.a for constant switching frequency. Next plot Fig. 26.b gives the result of case 1 keeping hysteresis bandwidth constant.

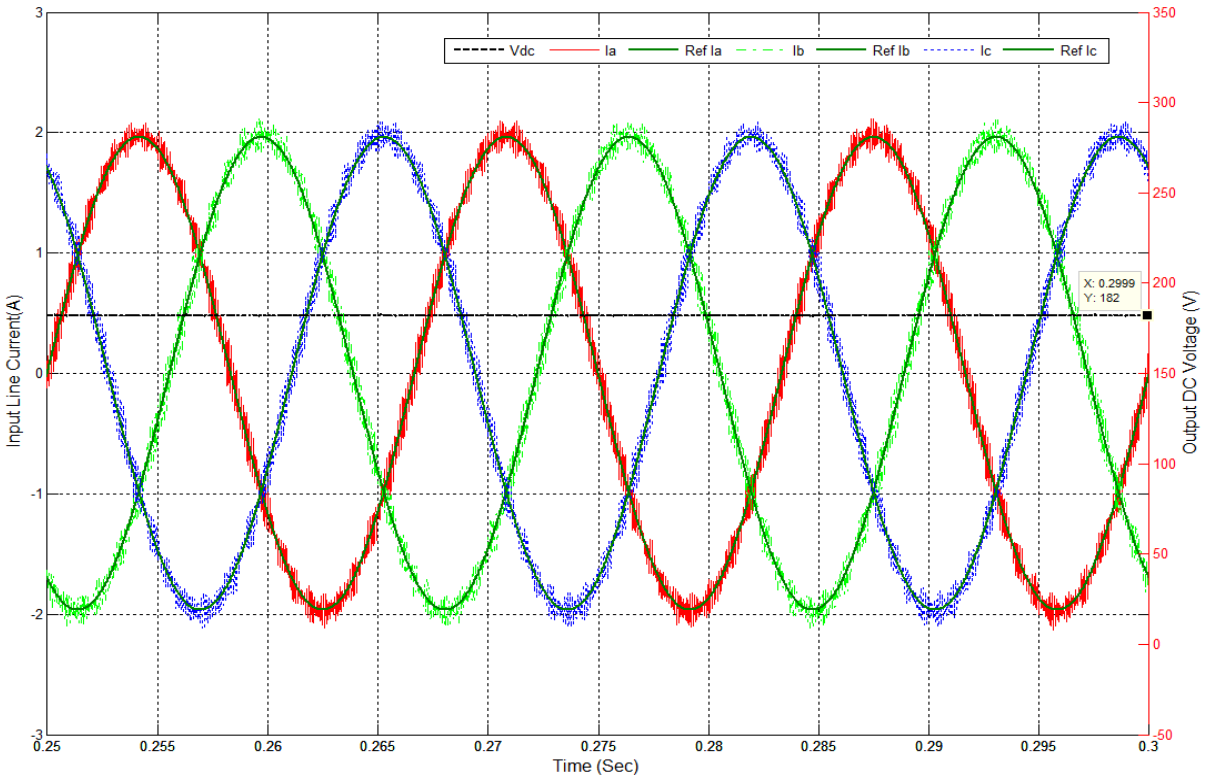


Figure 26.a: Case 1 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

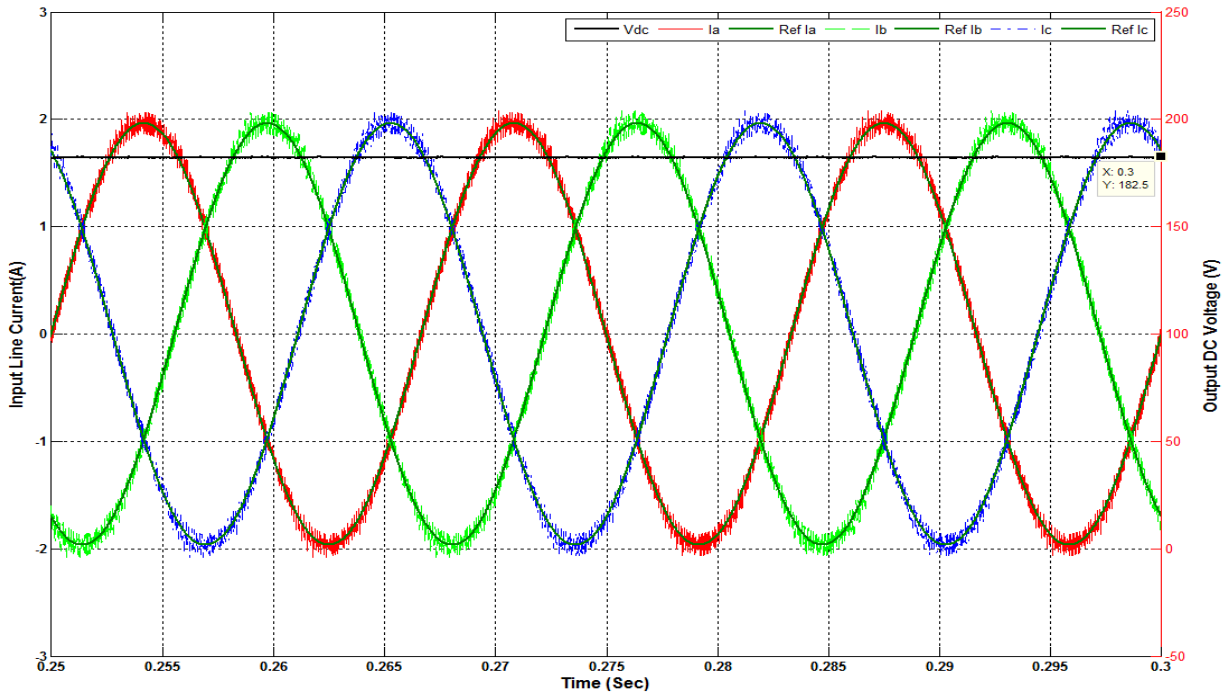


Figure 26.b: Case 1 Line currents and Output DC voltage (Constant Hysteresis Bandwidth, h= 0.1A)

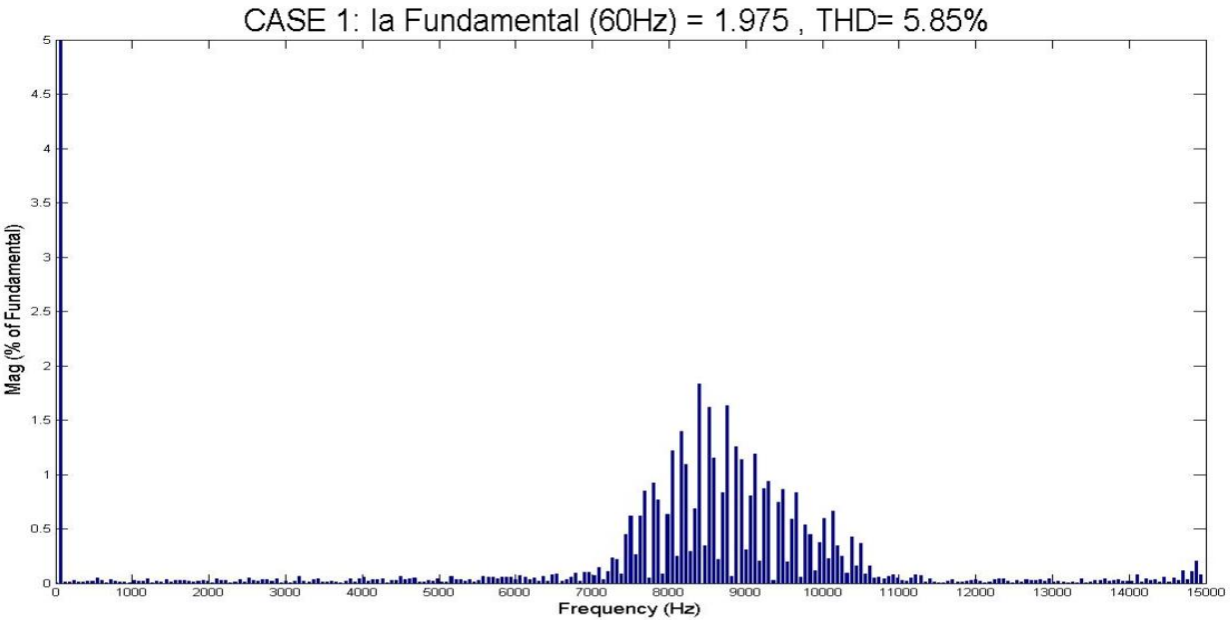


Figure 27.a: Case 1 FFT of phase **a** line current (Constant Switching Frequency fs = 9 kHz)

Fourier spectrum analysis is done for both cases are presented to show the constant switching frequency in which hysteresis bandwidth is variable. As shown in Fig. 27.a and 27.b spectrum of phase **a** line current are analyzed and near constant switching is achieved as preset at 9 kHz with the method developed.

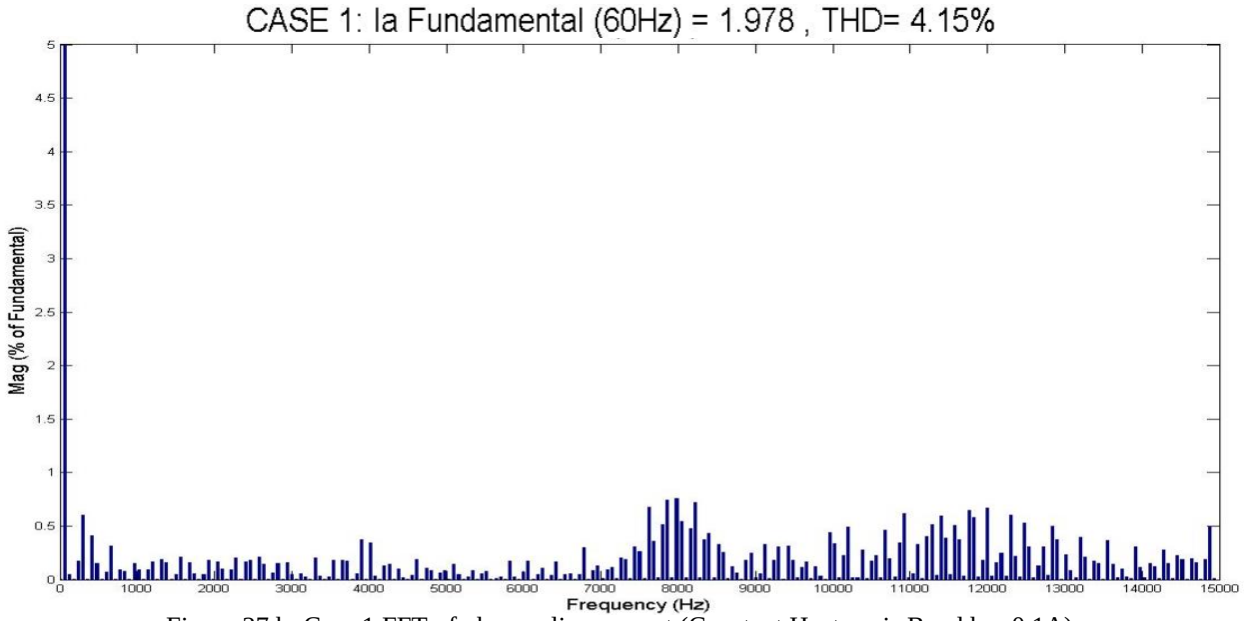


Figure 27.b: Case 1 FFT of phase **a** line current (Constant Hysteresis Band h = 0.1A)

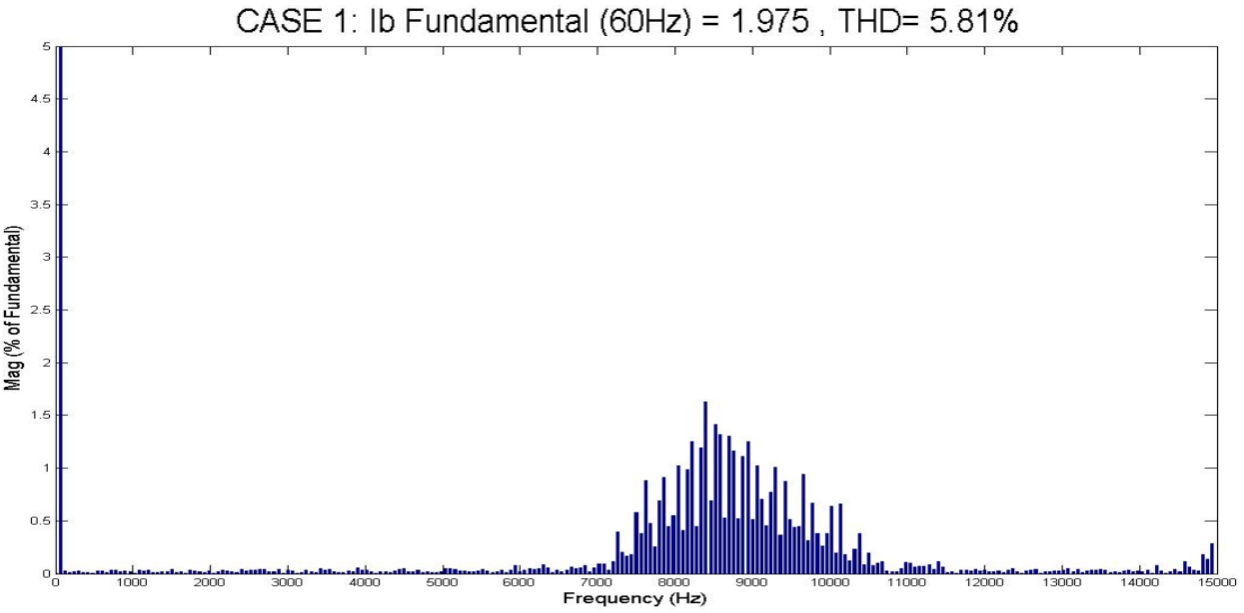


Figure 28.a: Case 1 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

Similar spectrum analysis for phase **b** and phase **c** are presented in Fig. 28 and Fig. 29

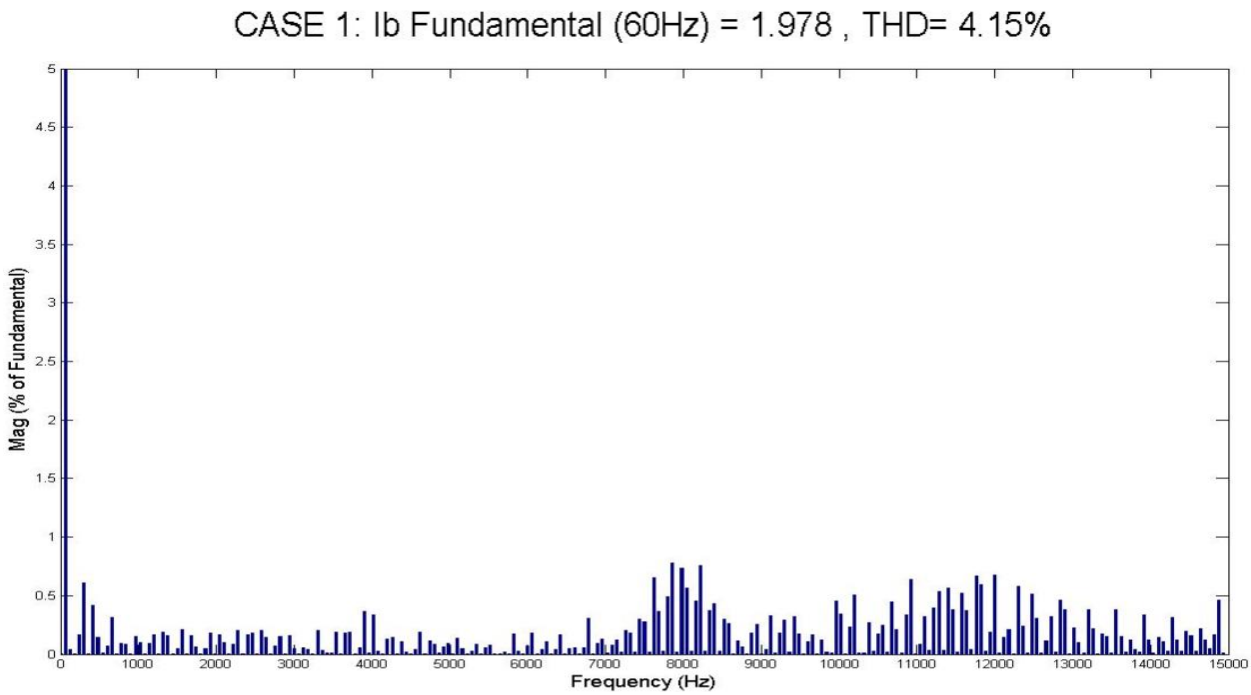


Figure 28.b: Case 1 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

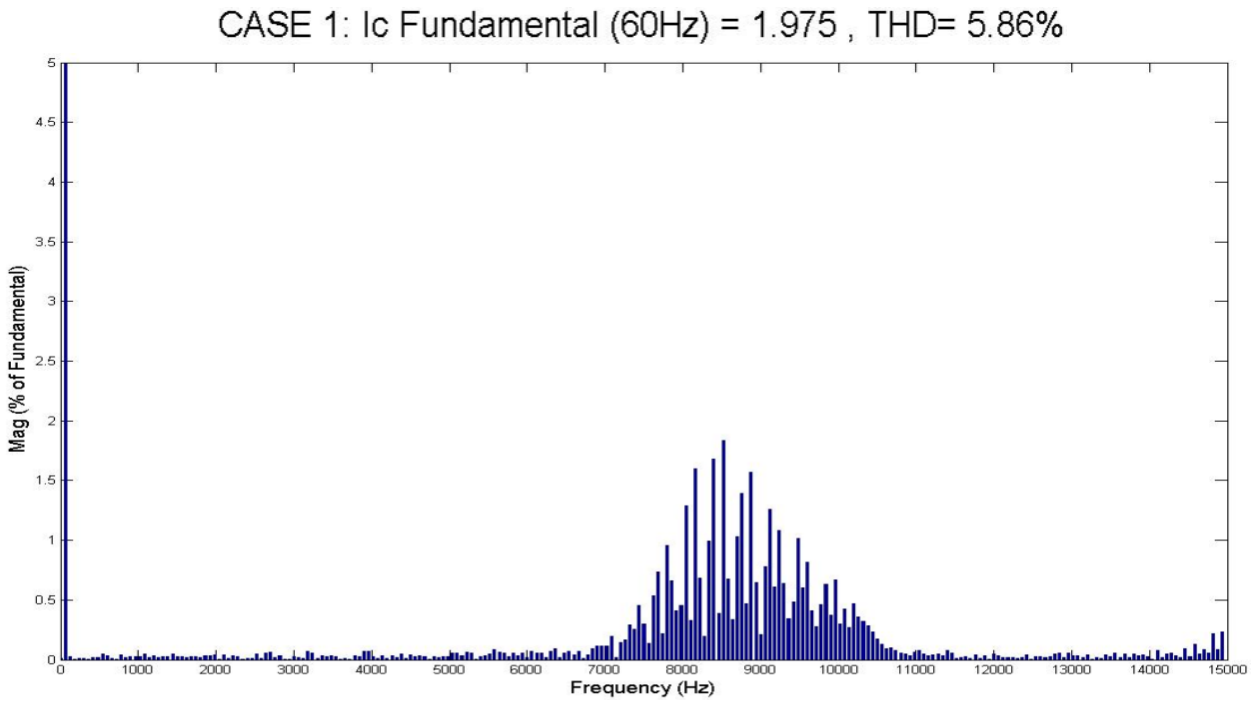


Figure 29.a: Case 1 FFT of phase **c** line current (Constant Switching Frequency fs = 9 kHz)

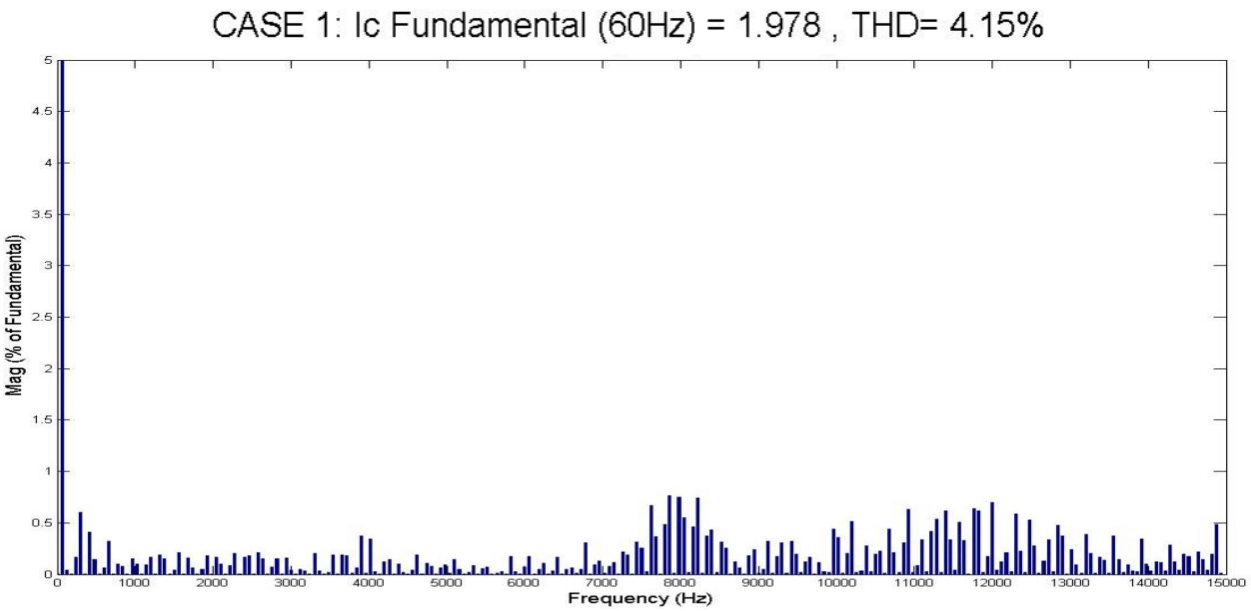


Figure 29.b: Case 1 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

The other six cases presented in the Table I are also analyzed similarly to show the effectiveness of the method in severe unbalanced conditions. Fig. 30 through Fig. 53 show the steady state plots for line current of each phases along with the output DC link voltages and Fourier analysis of all line currents in each phase.

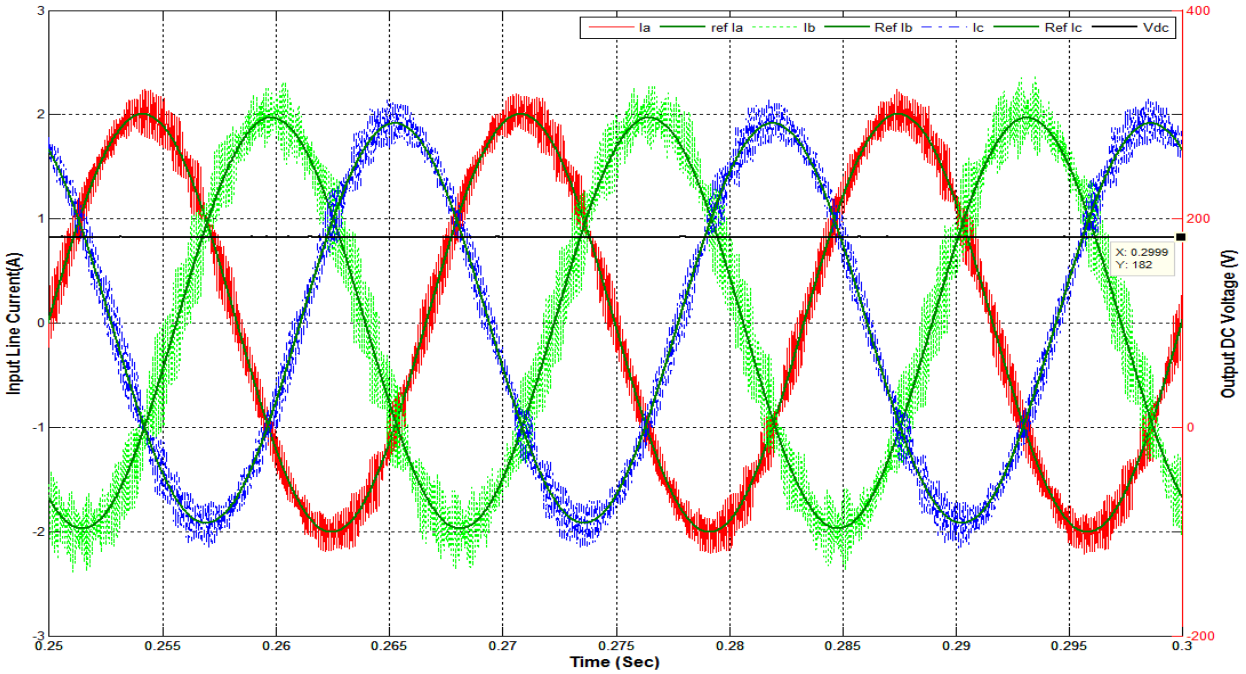


Figure 30.a: Case 2 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

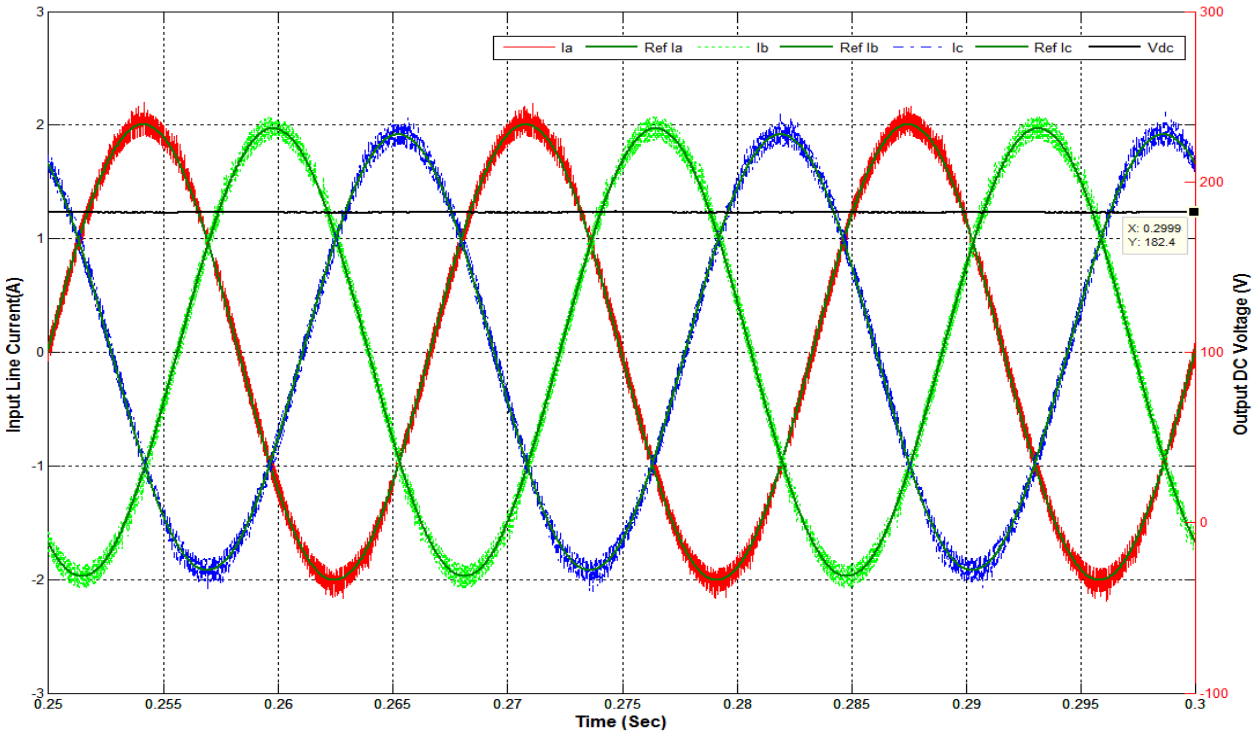


Figure 30.b: Case 2 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

Fig. 31 through Fig. 33 show the Fourier analysis of line current in each phases for case 2.

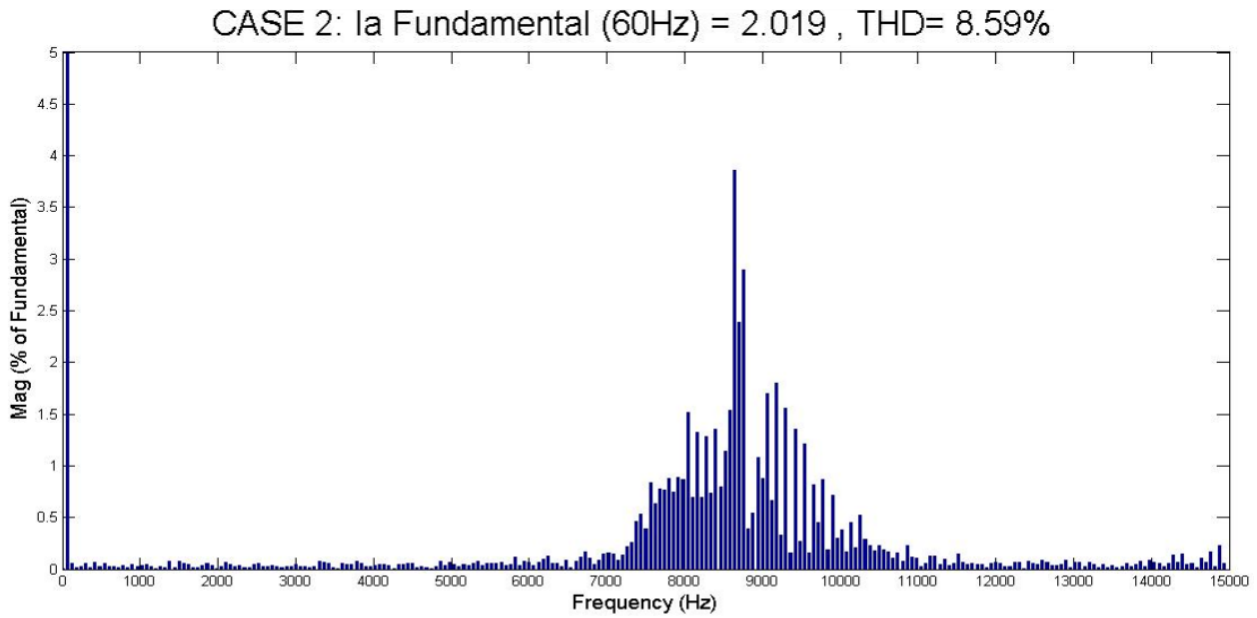


Figure 31.a: Case 2 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

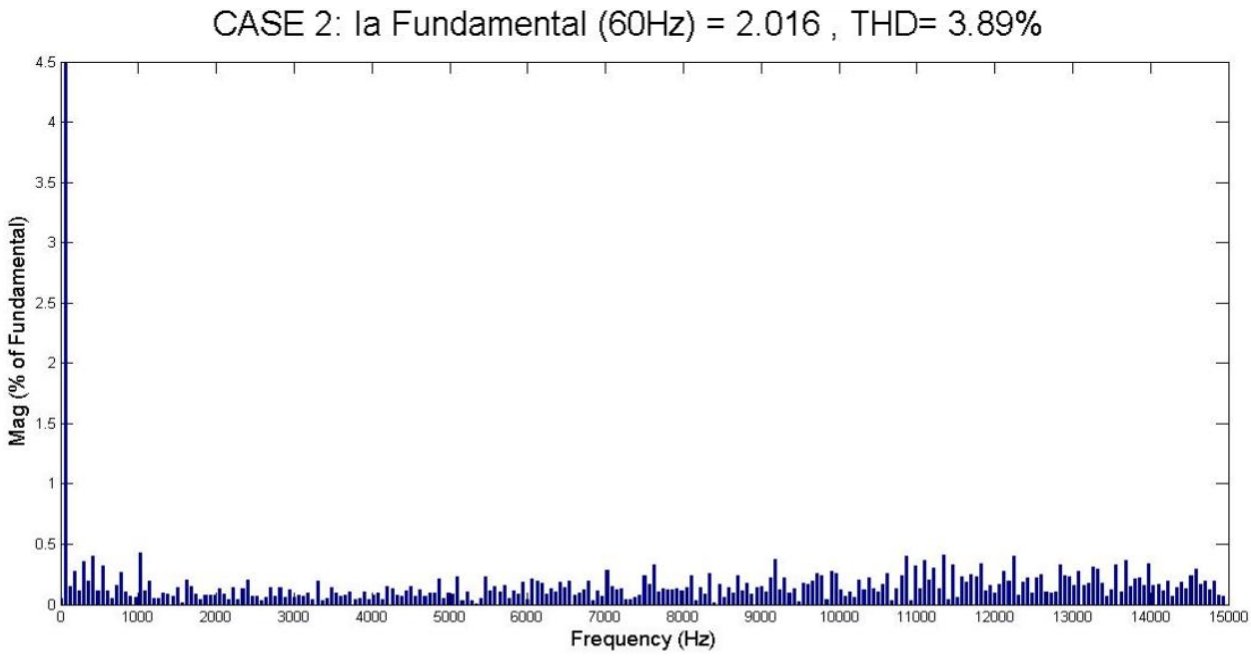


Figure 31.b: Case 2 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

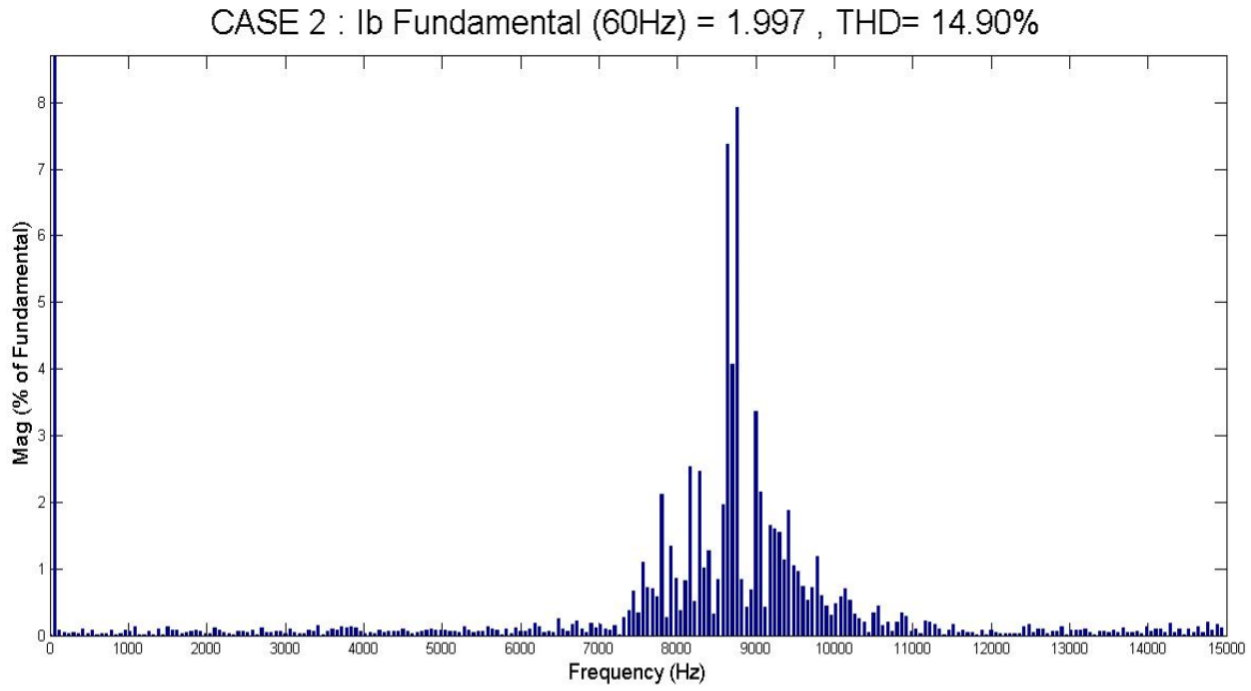


Figure 32.a: Case 2 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

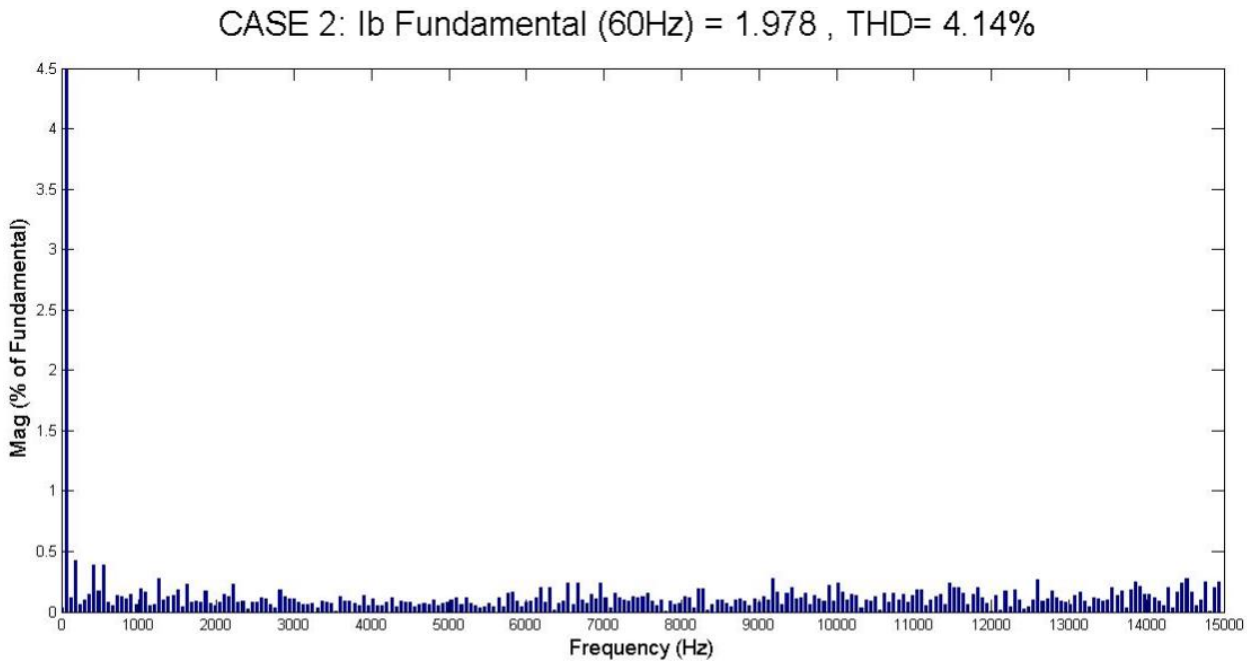


Figure 32.b: Case 2 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

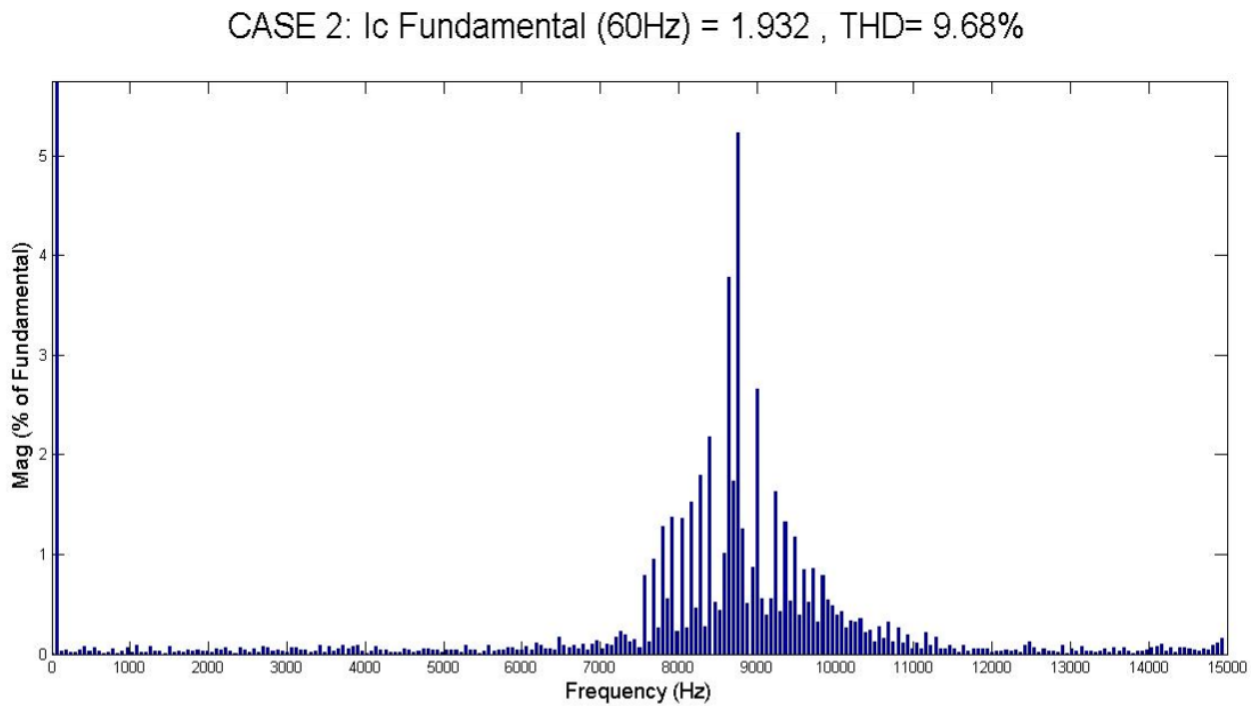


Figure 33.a: Case 2 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

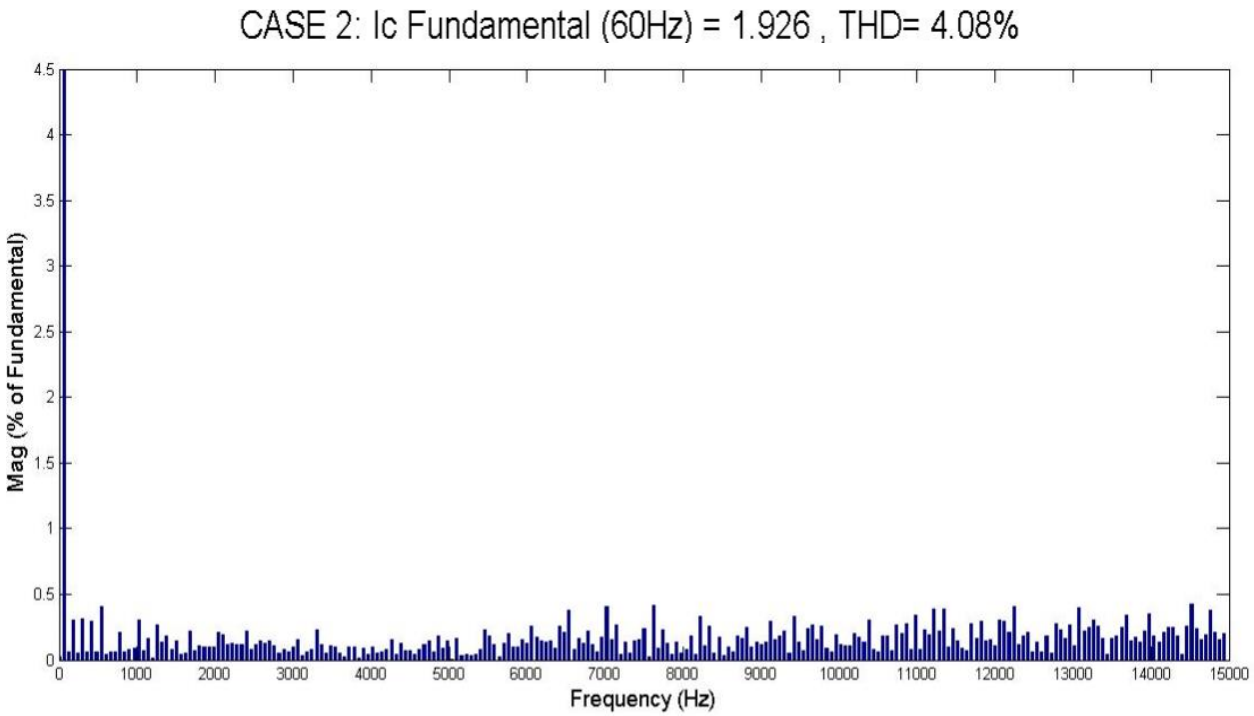


Figure 33.b: Case 2 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

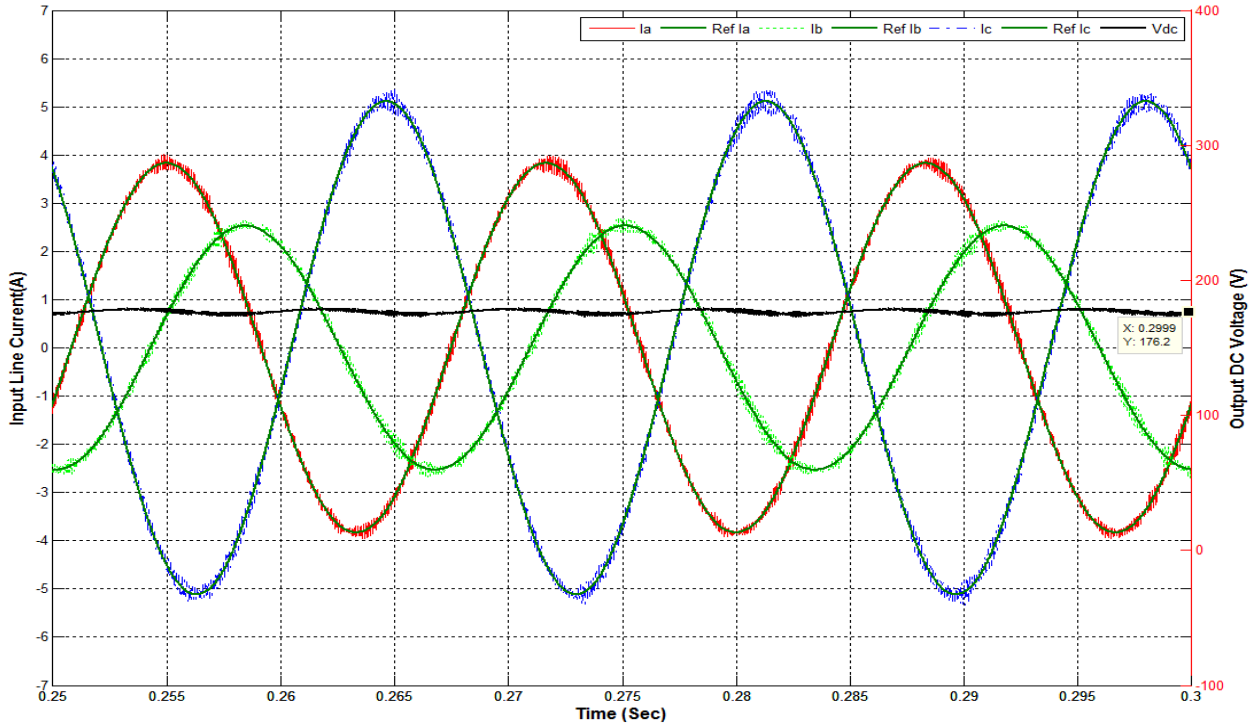


Figure 34.a: Case 3 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

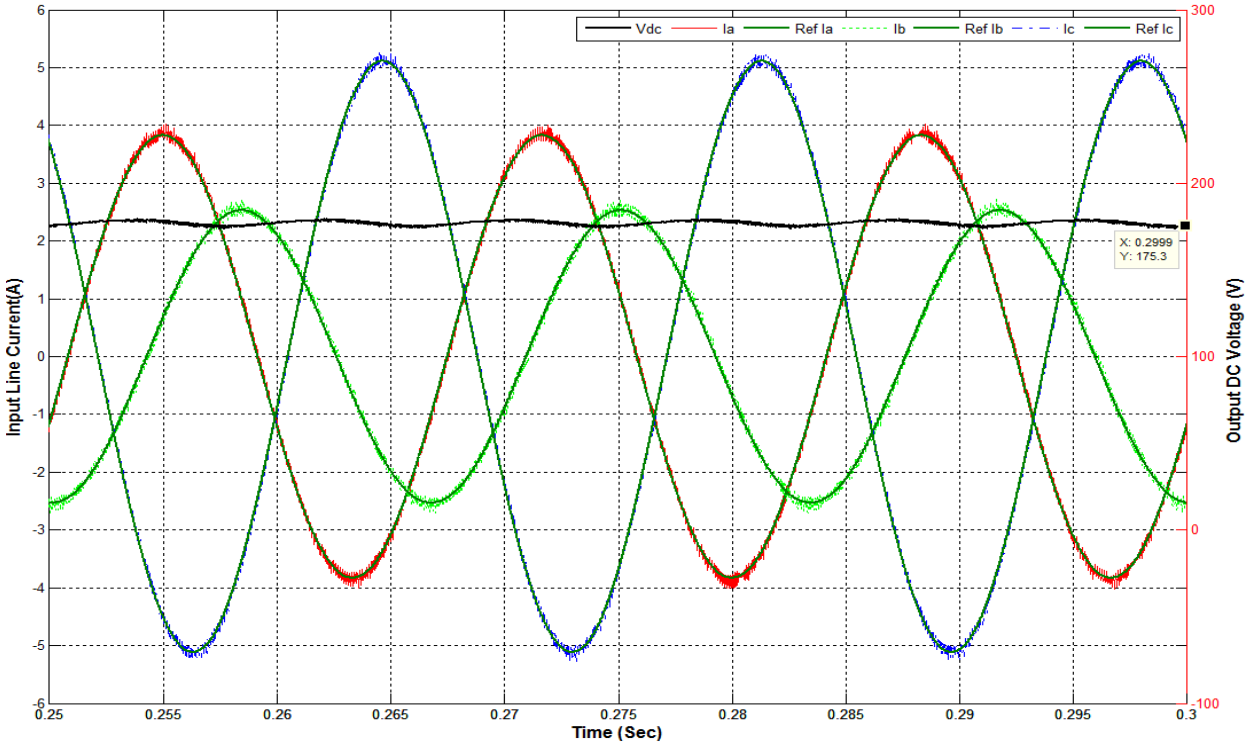


Figure 34.b: Case 3 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

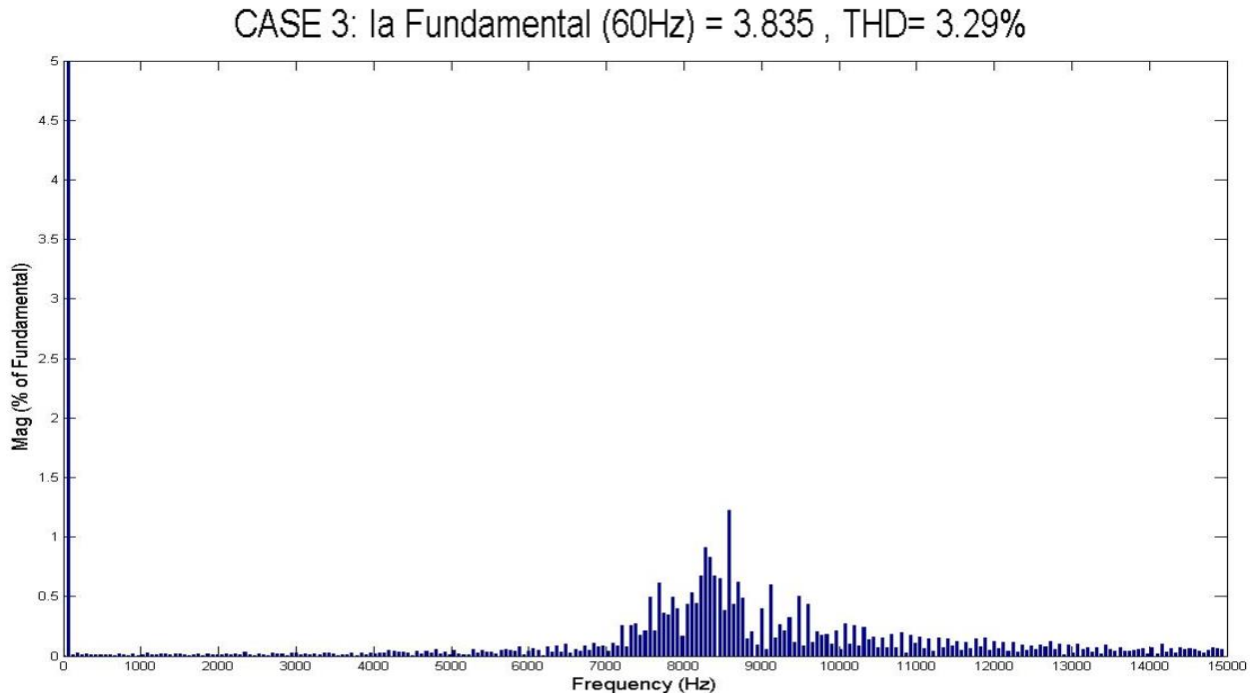


Figure 35.a: Case 3 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

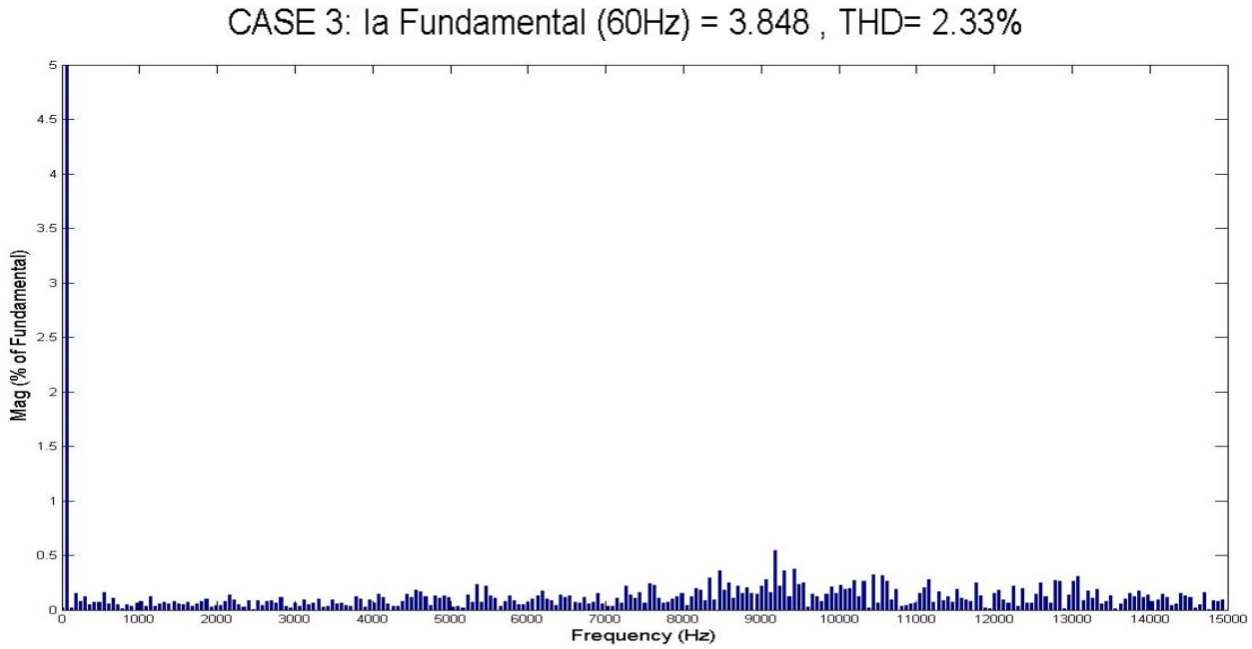


Figure 35.b: Case 3 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

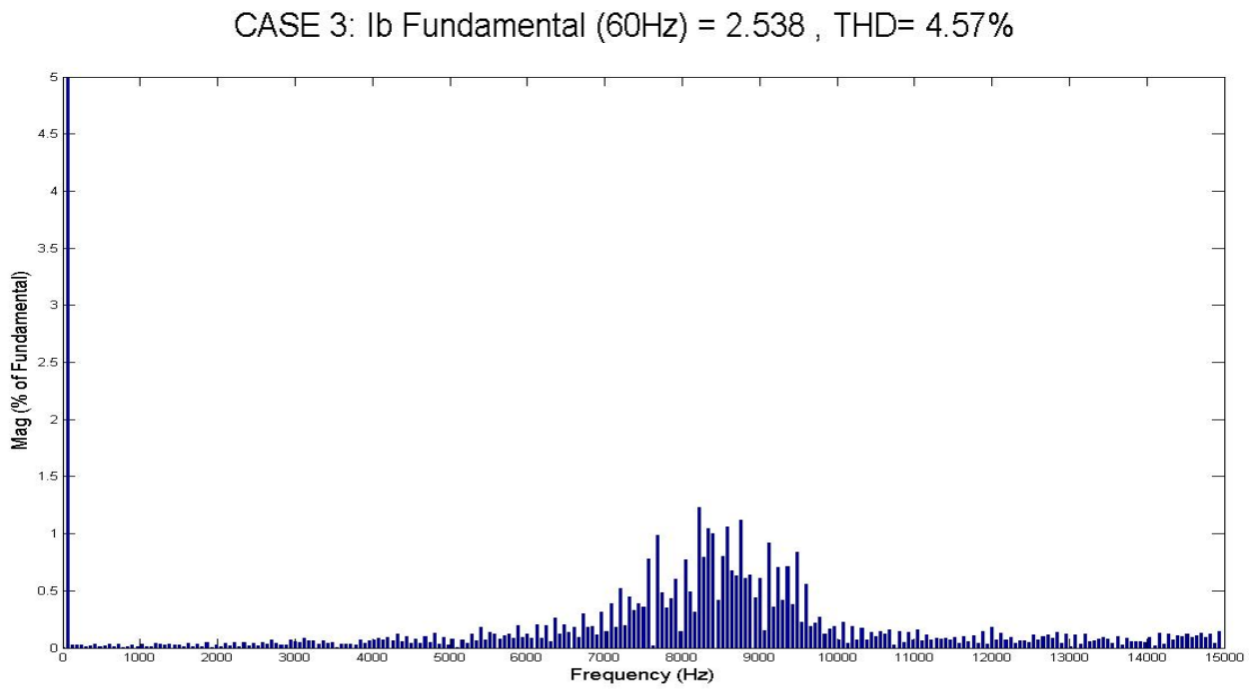


Figure 36.a: Case 3 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

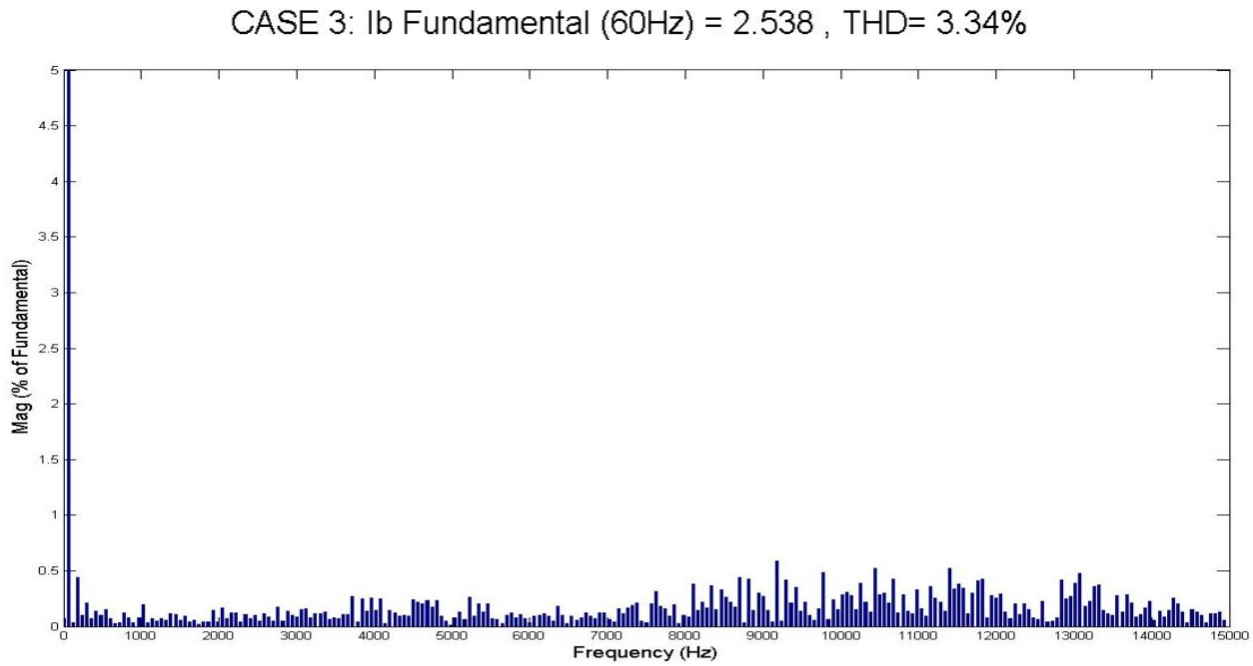


Figure 36.b: Case 3 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

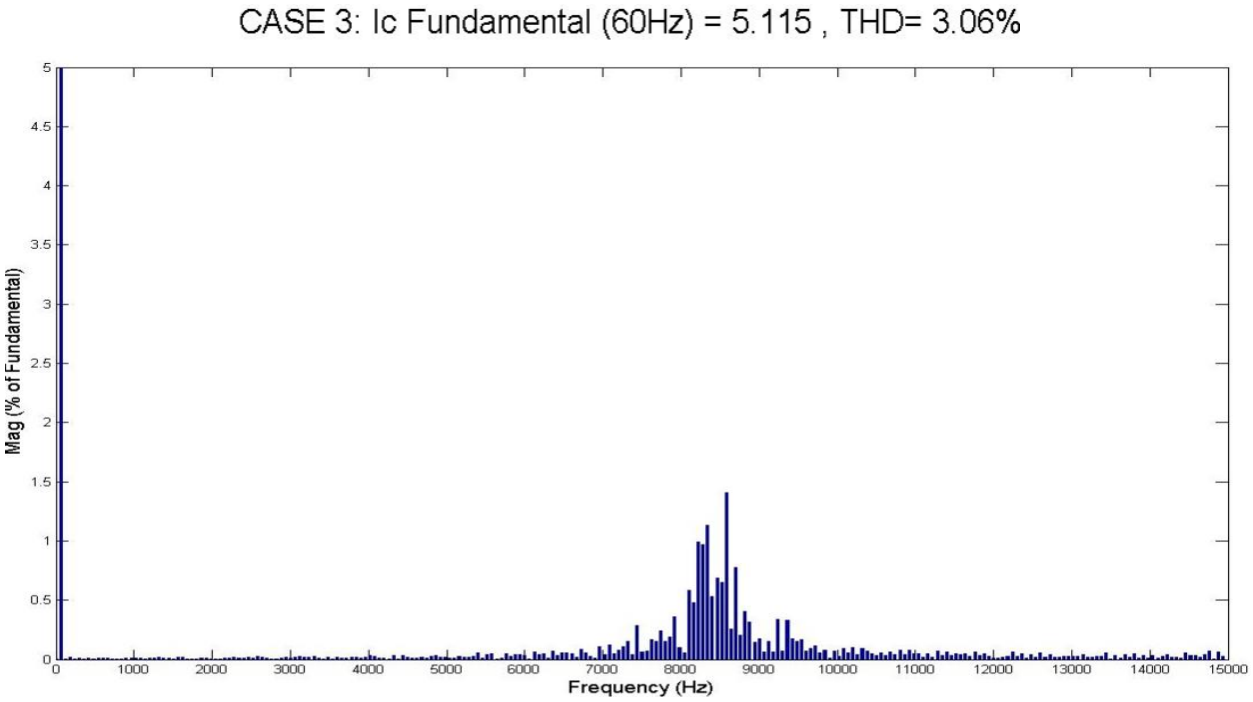


Figure 37.a: Case 3 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

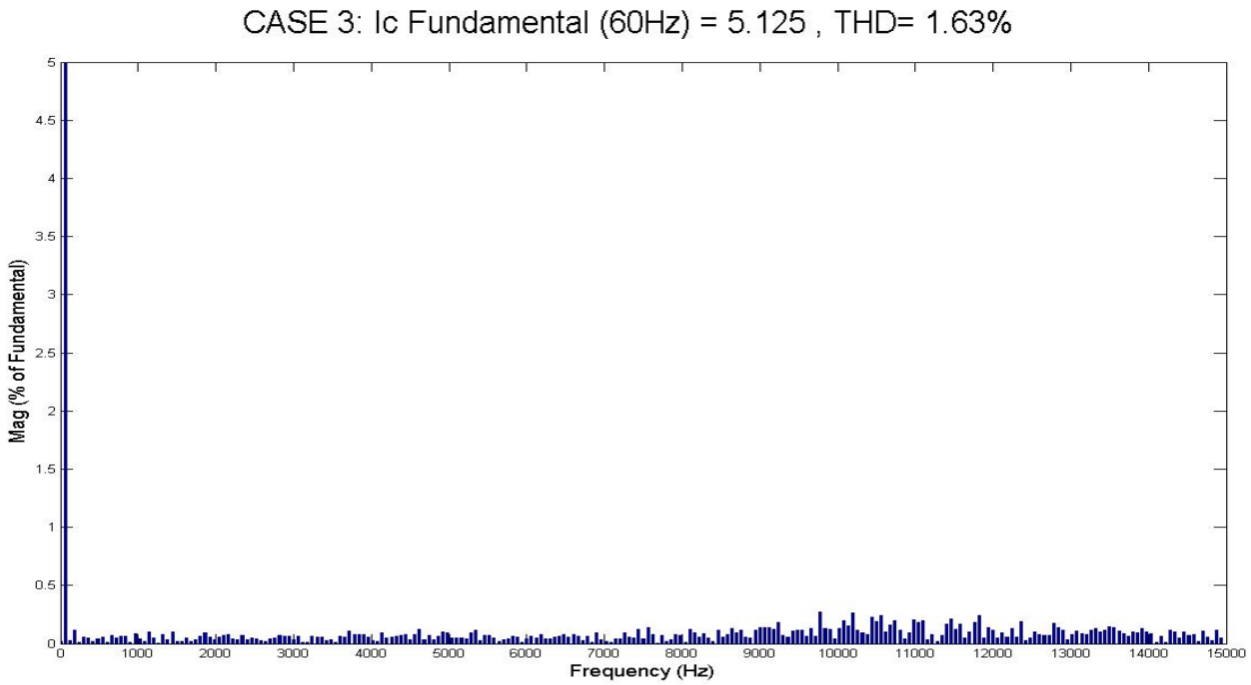


Figure 37.b: Case 3 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

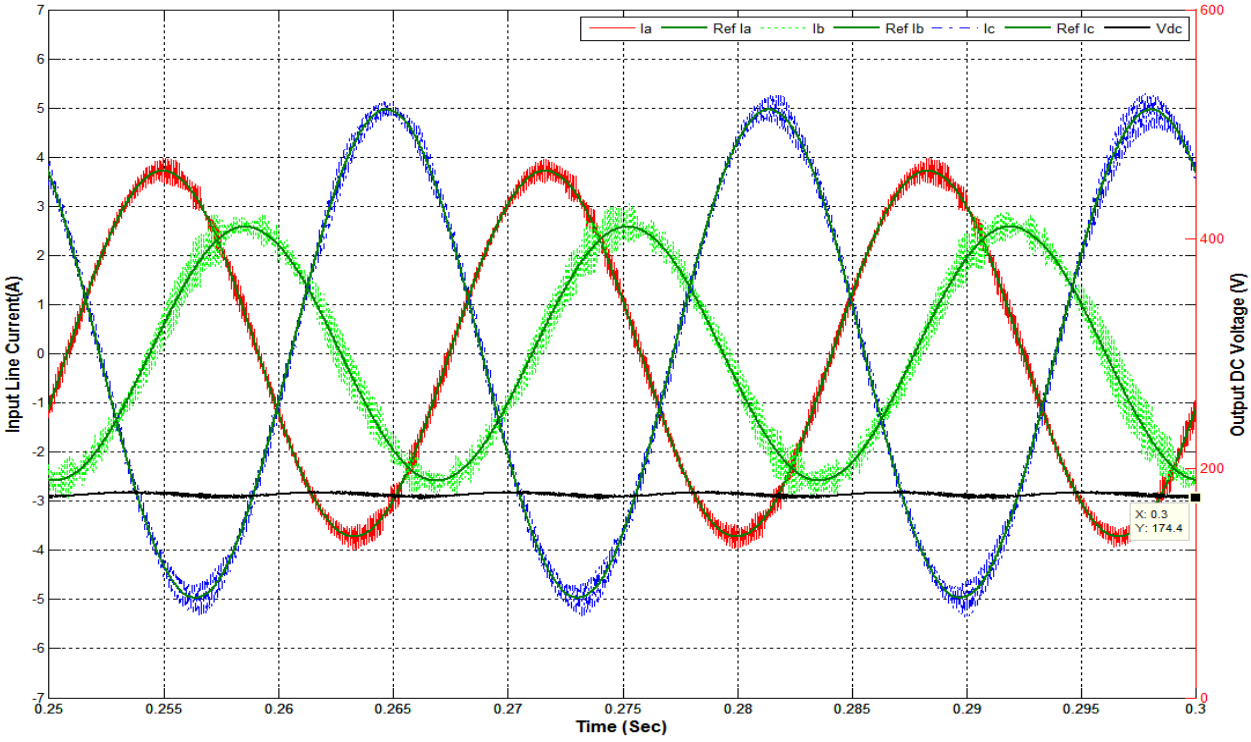


Figure 38.a: Case 4 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

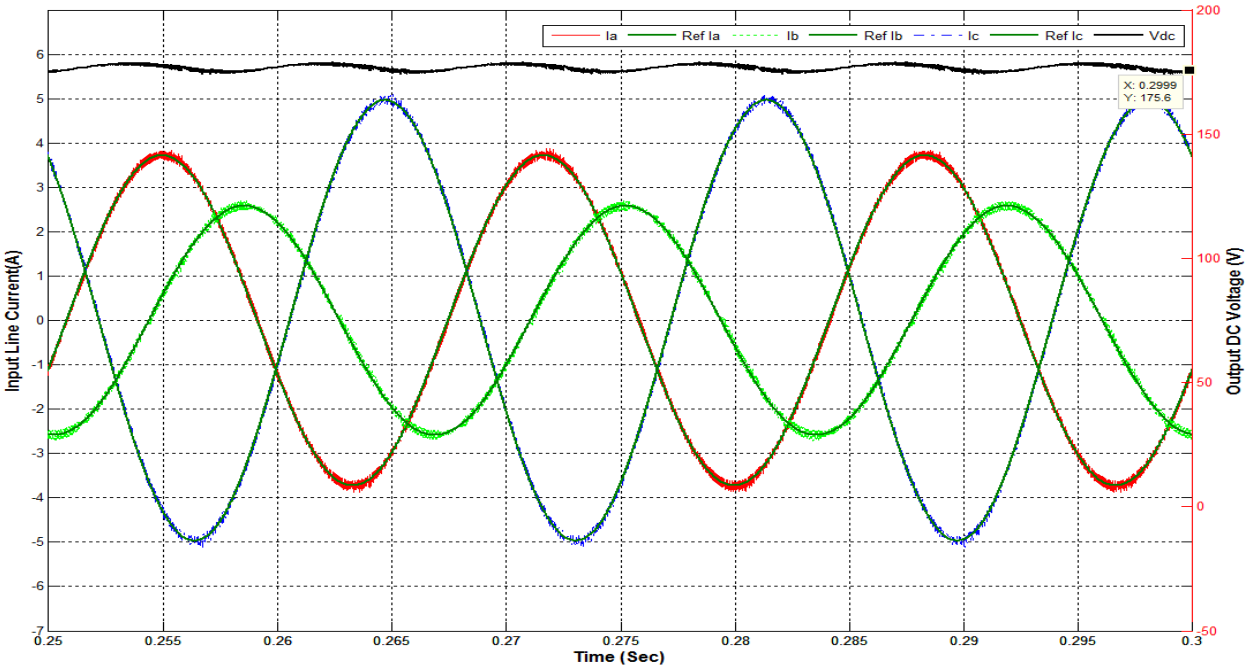


Figure 38.b: Case 4 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

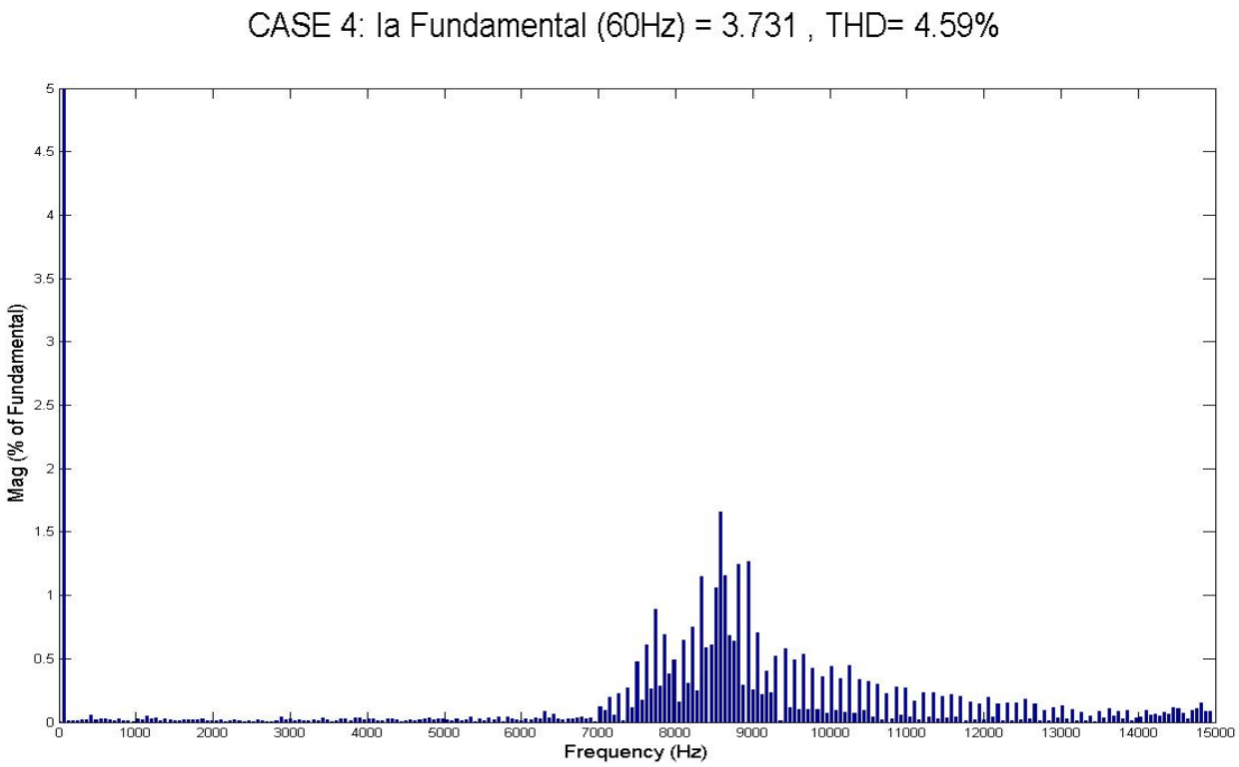


Figure 39.a: Case 4 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

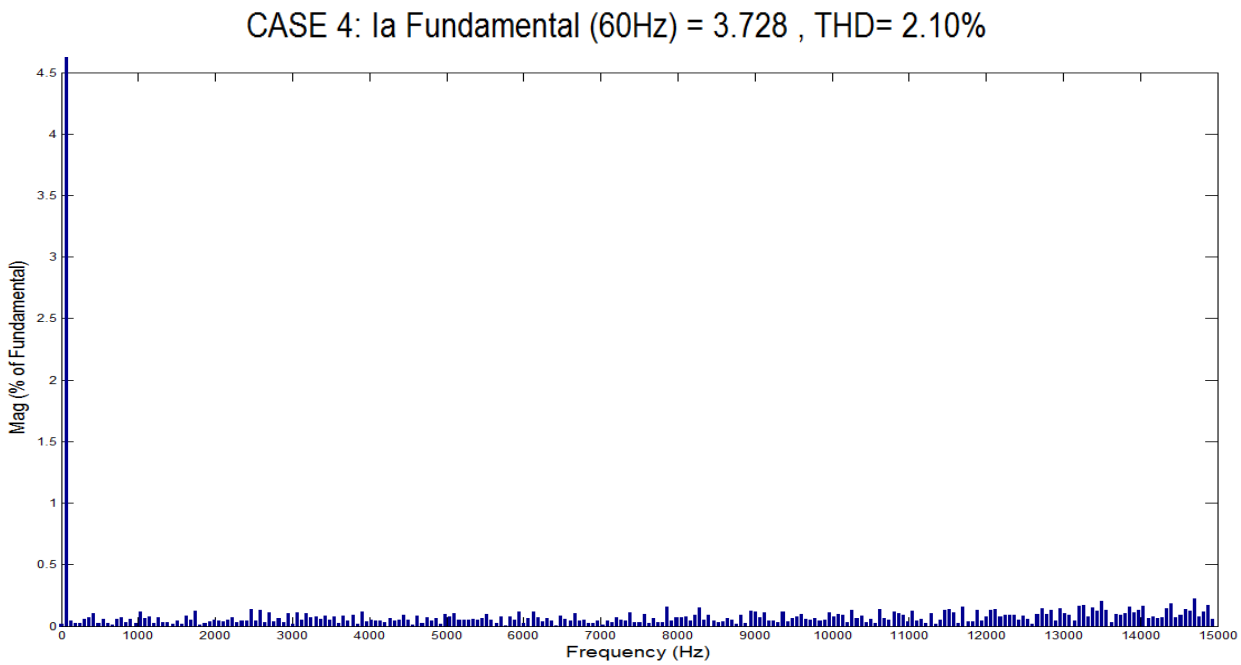


Figure 39.b: Case 4 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

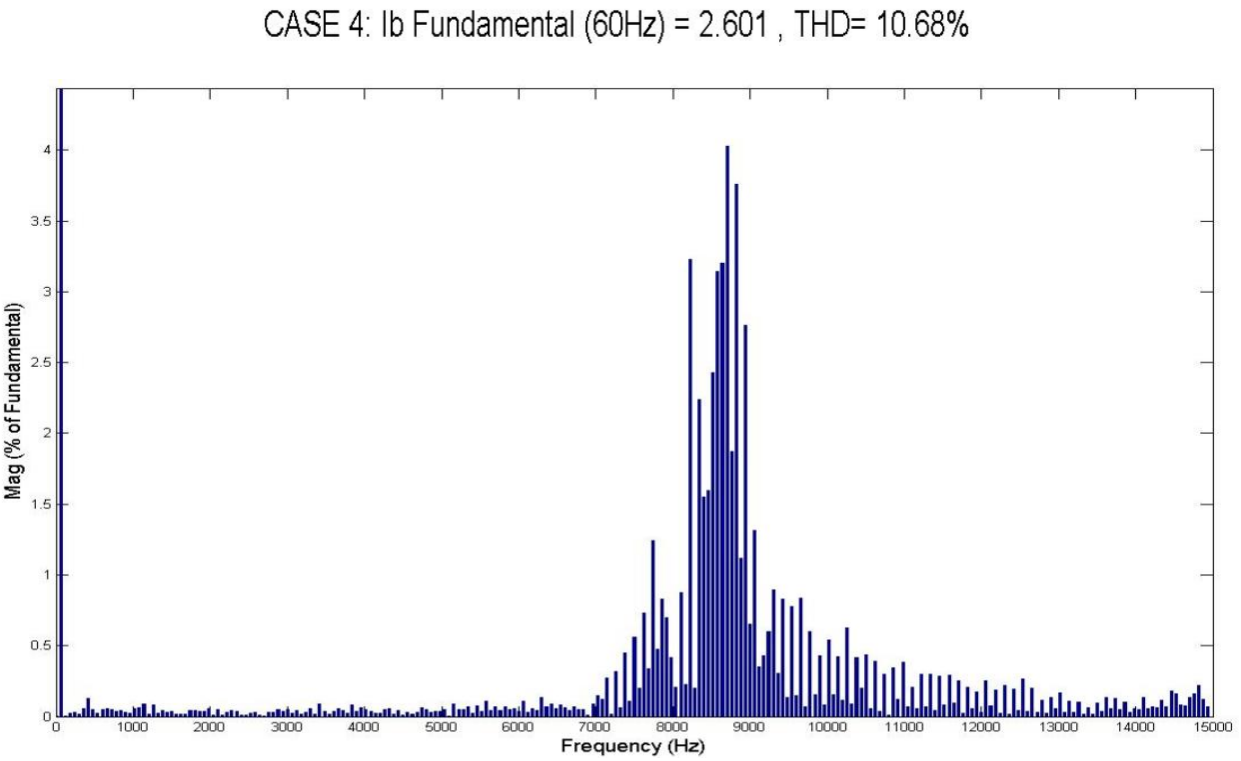


Figure 40.a: Case 4 FFT of phase b line current (Constant Switching frequency fs = 9 kHz)

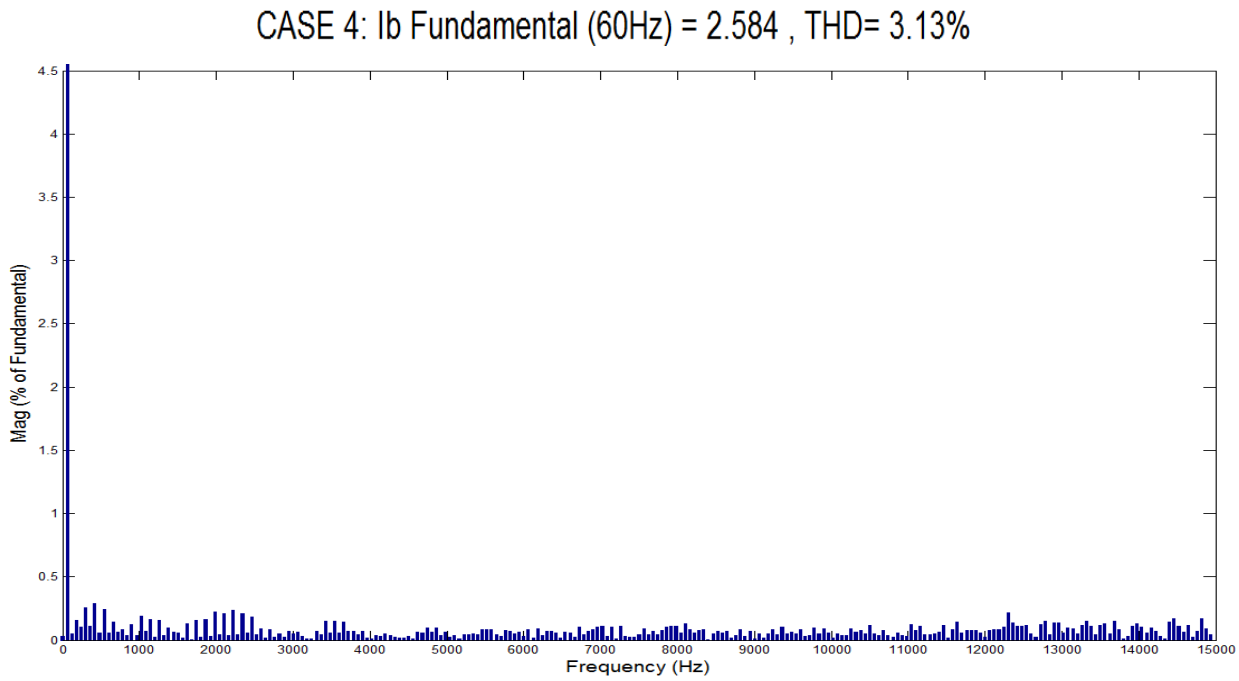


Figure 40.b: Case 4 FFT of phase b line current (Constant Hysteresis band h = 0.1 A)

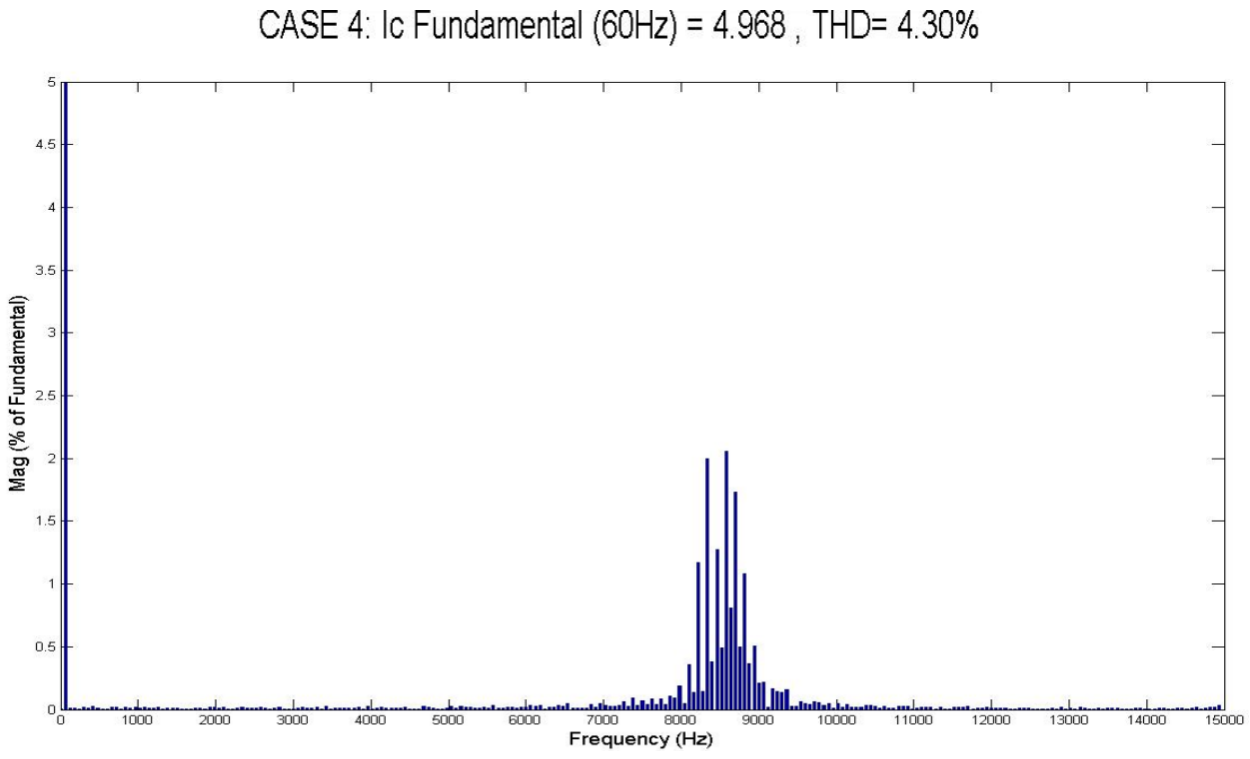


Figure 41.a: Case 4 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

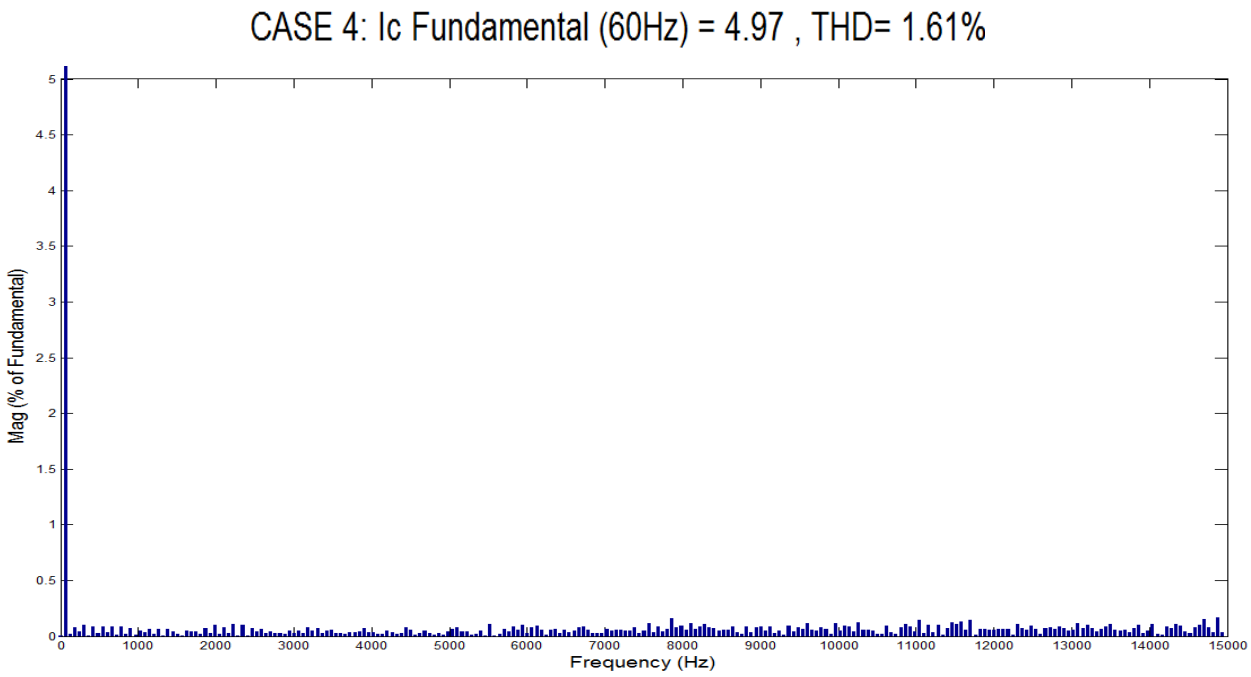


Figure 41.b: Case 4 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

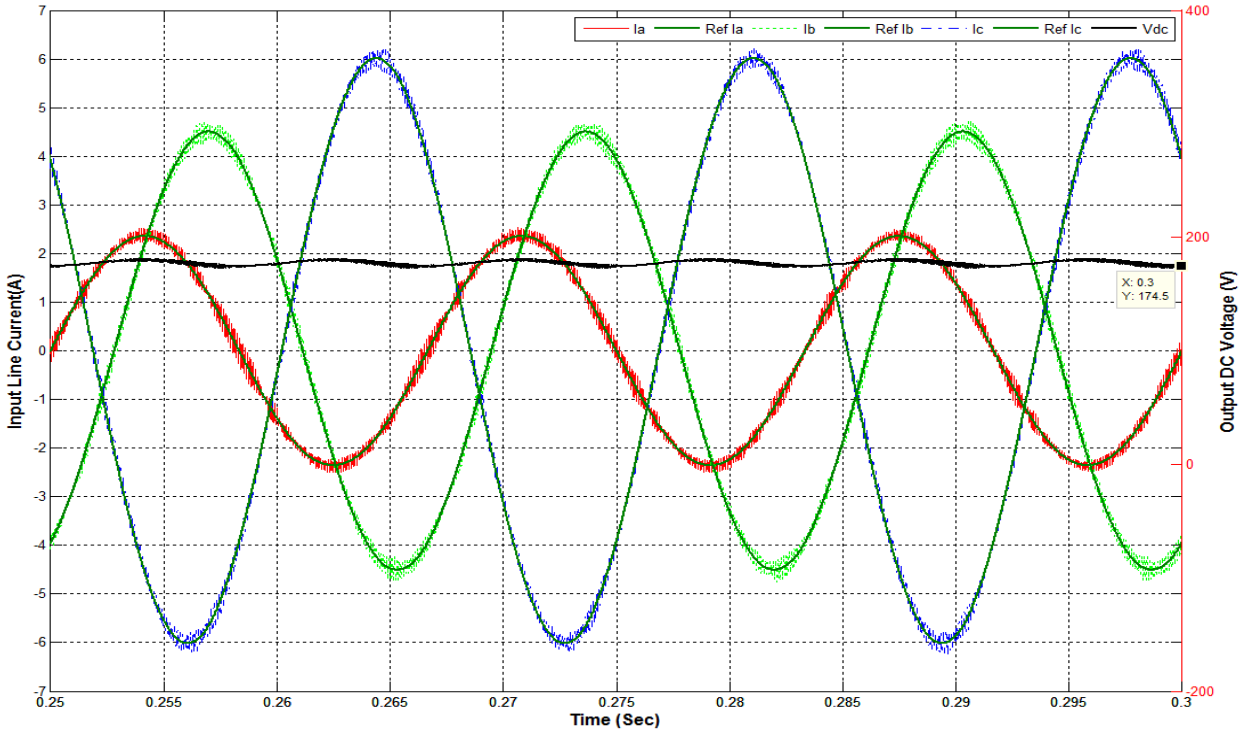


Figure 42.a: Case 5 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

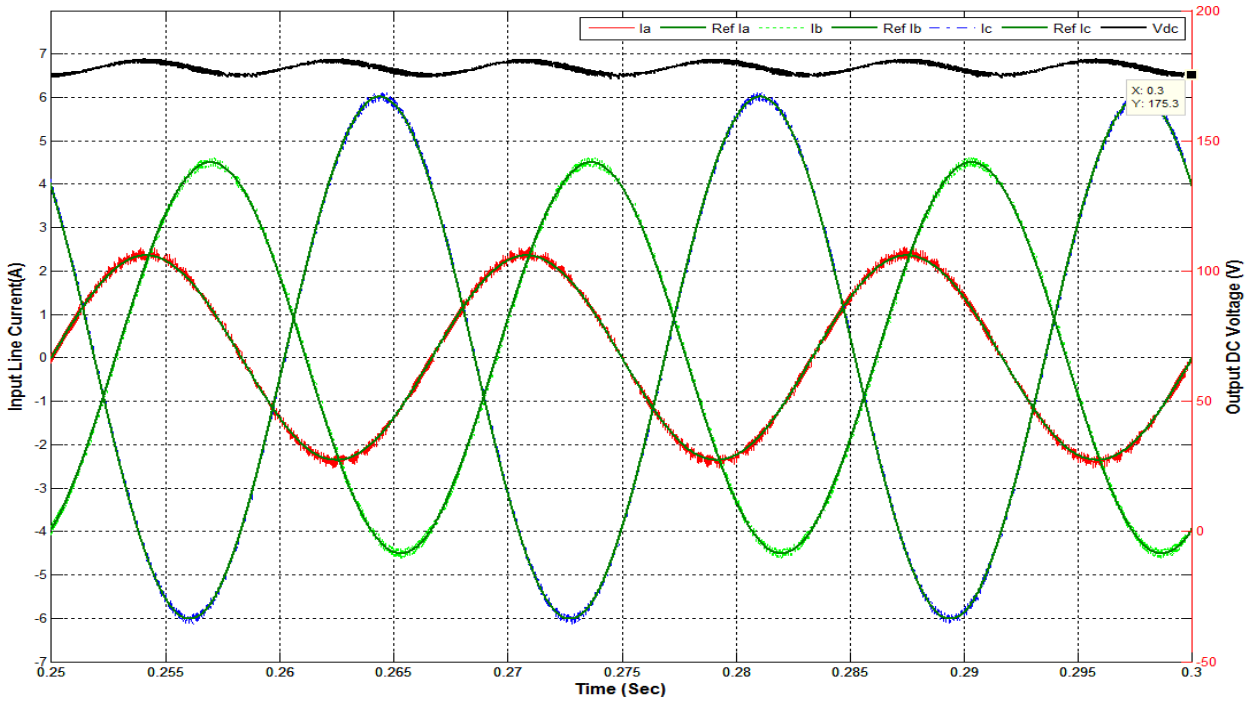


Figure 42.b: Case 5 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

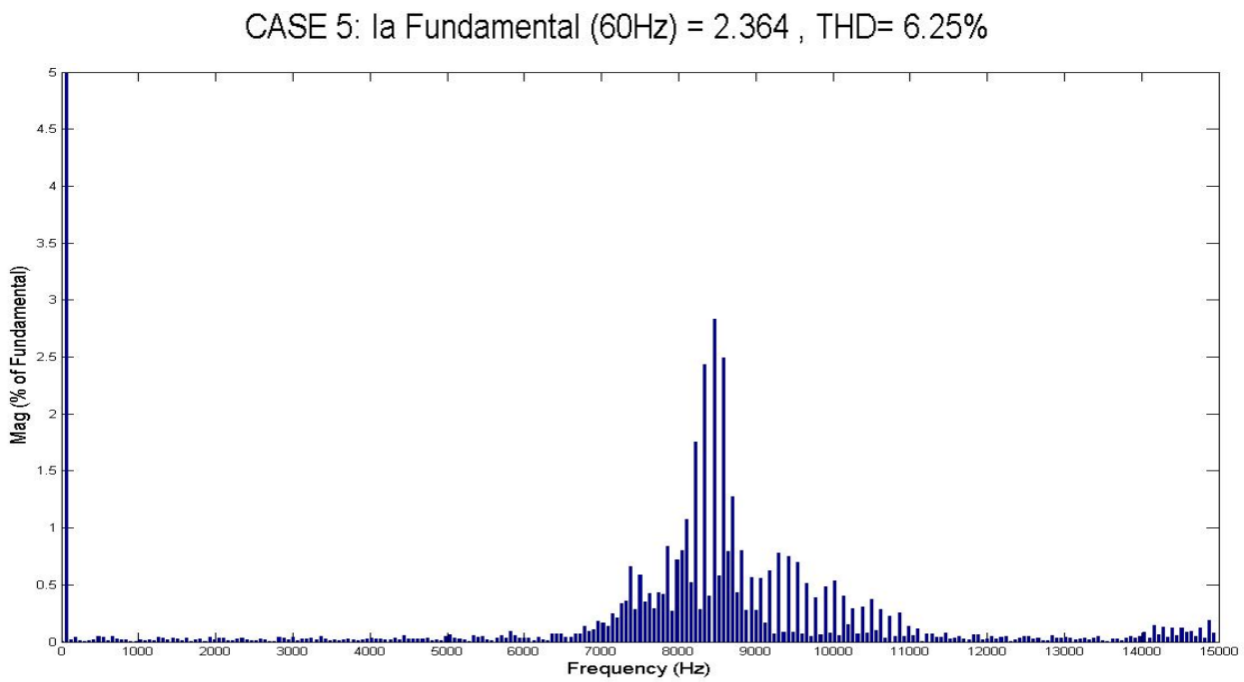


Figure 43.a: Case 5 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

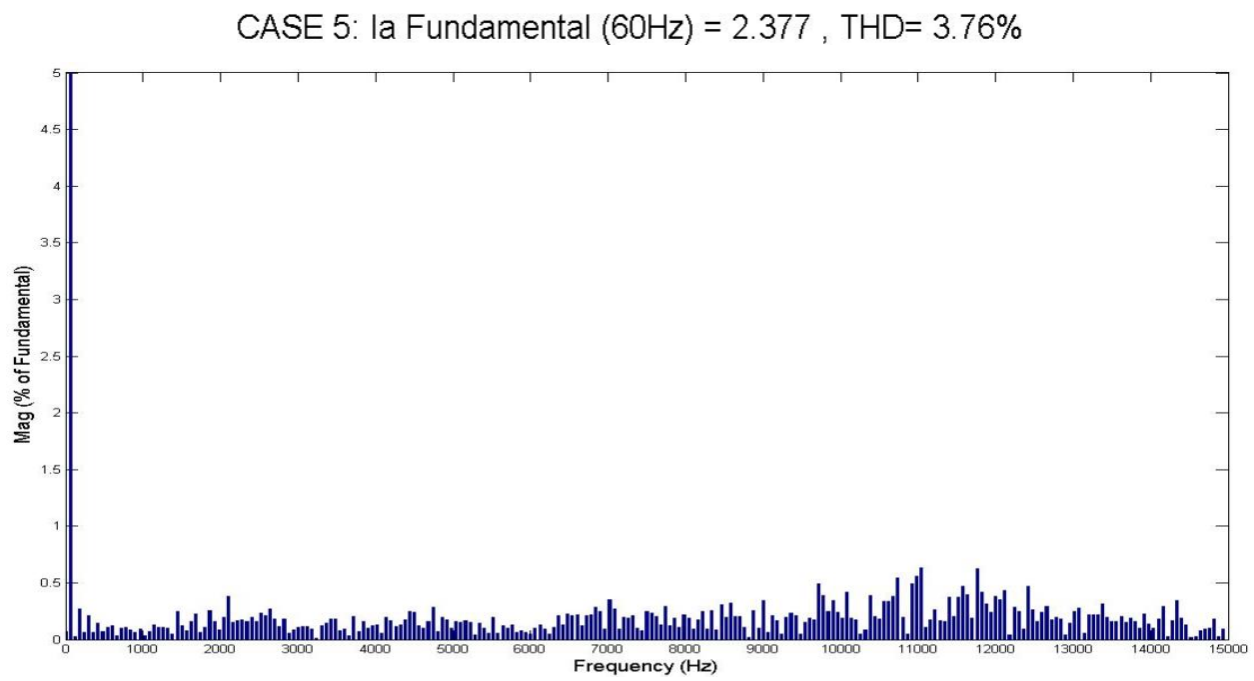


Figure 43.b: Case 5 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

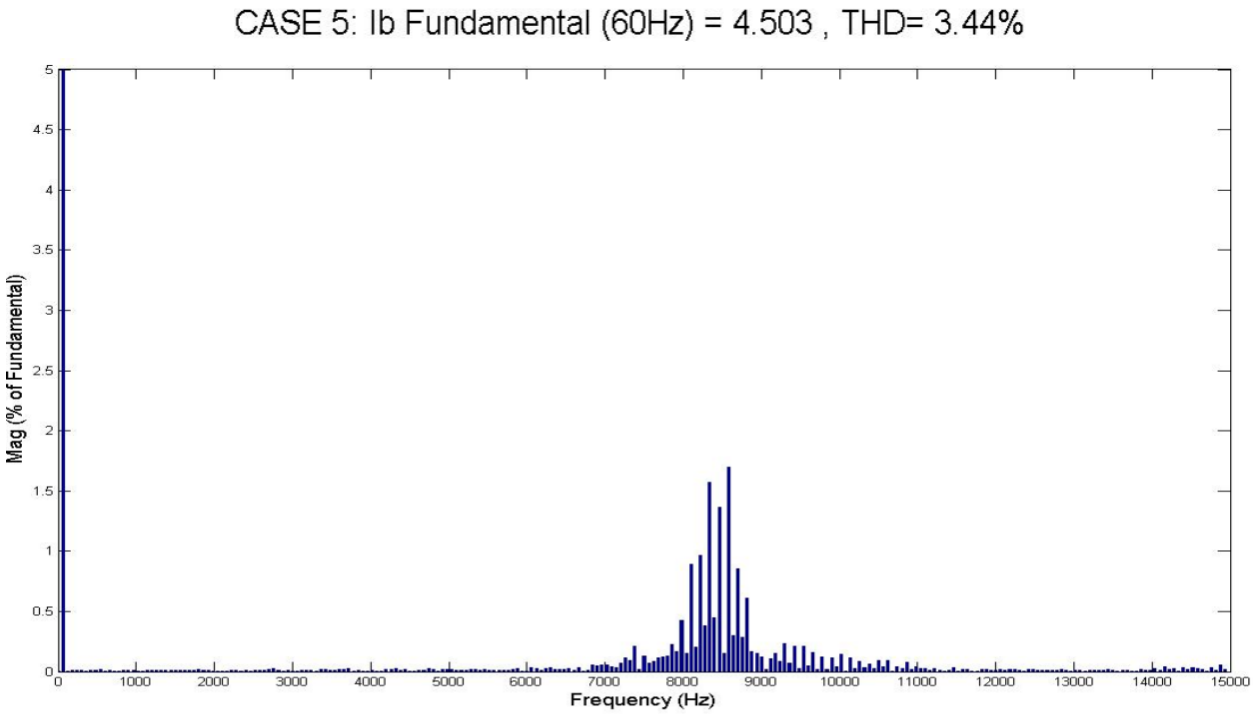


Figure 44.a: Case 5 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

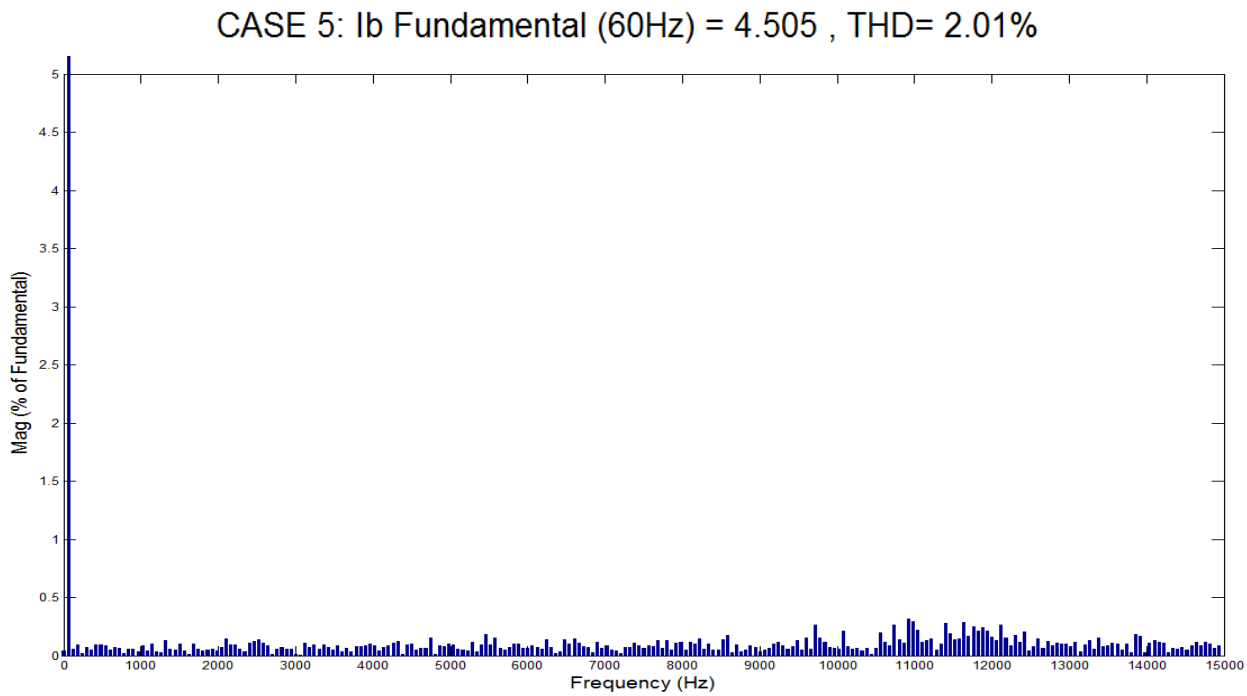


Figure 44.b: Case 5 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

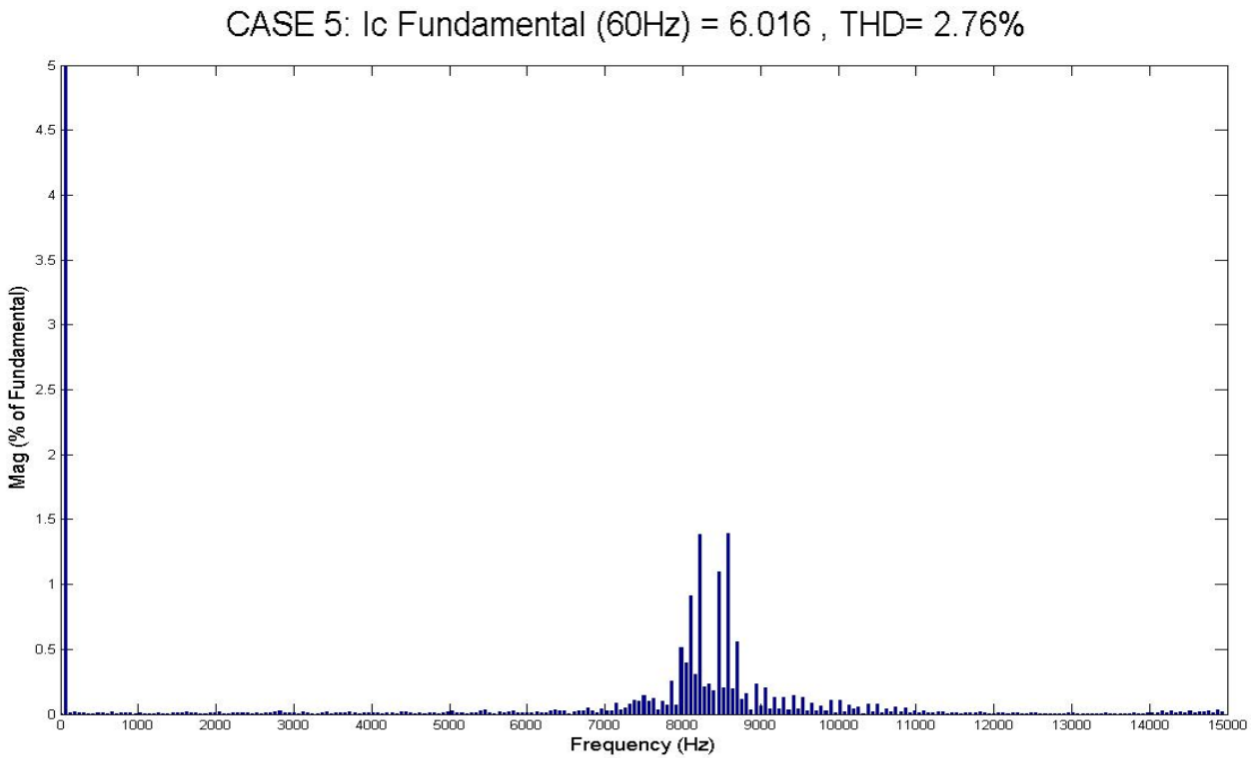


Figure 45.a: Case 5 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

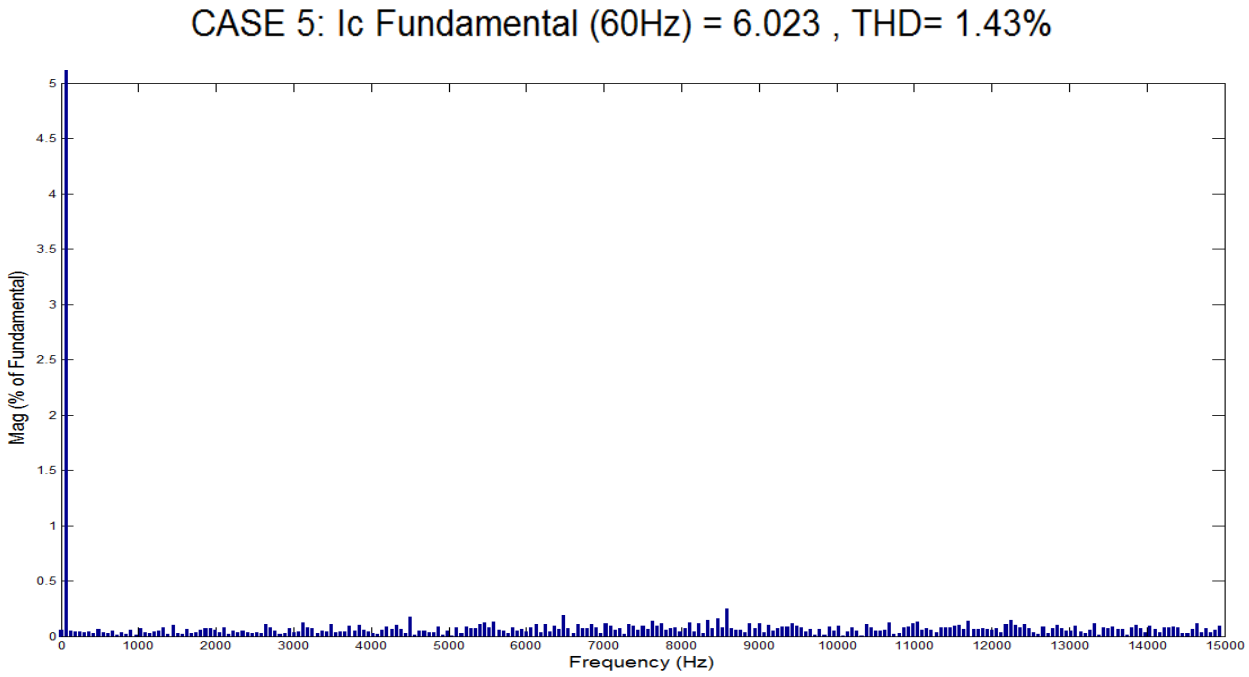


Figure 45.b: Case 5 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

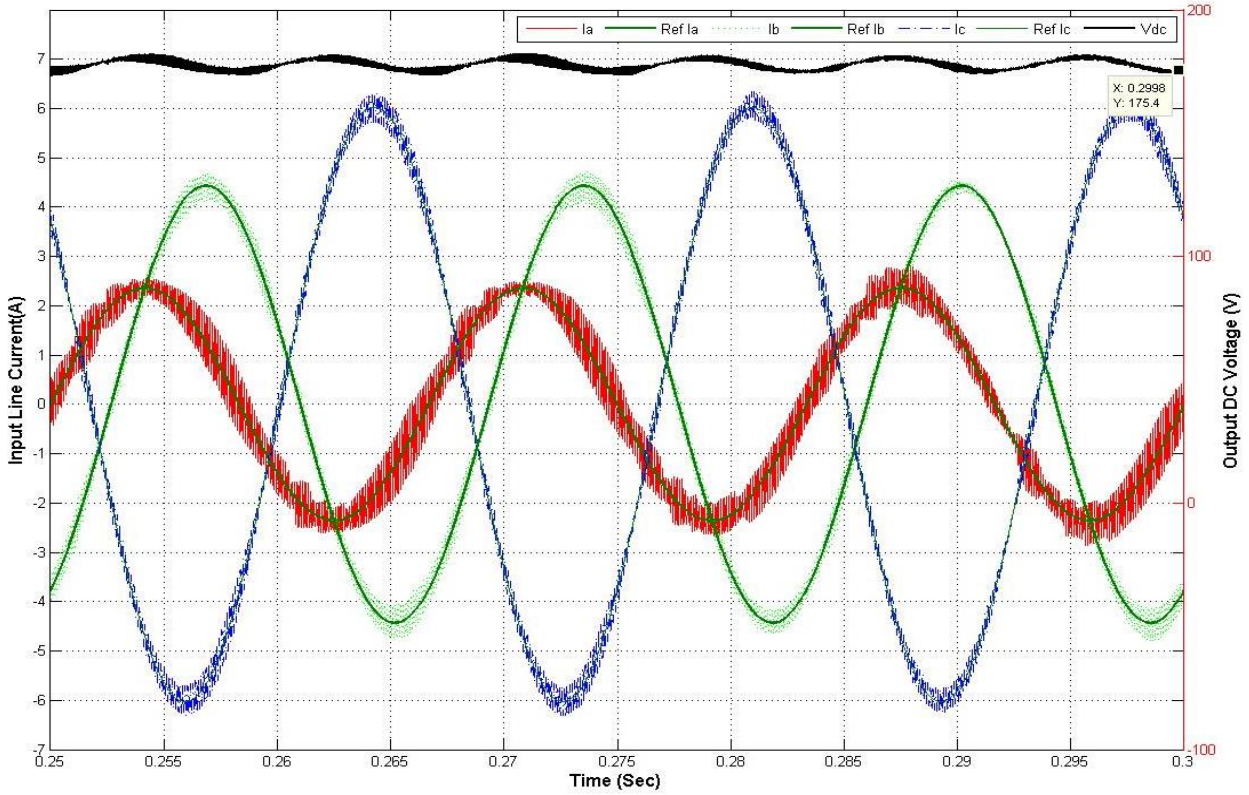


Figure 46.a: Case 6 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

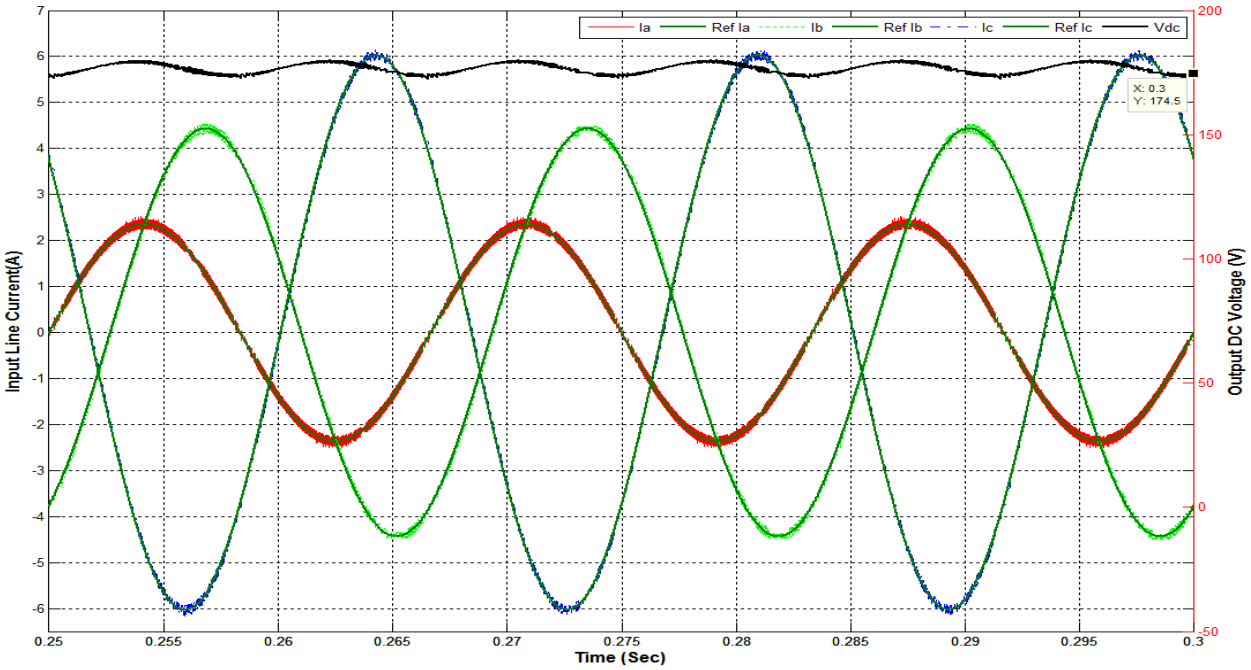


Figure 46.b: Case 6 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

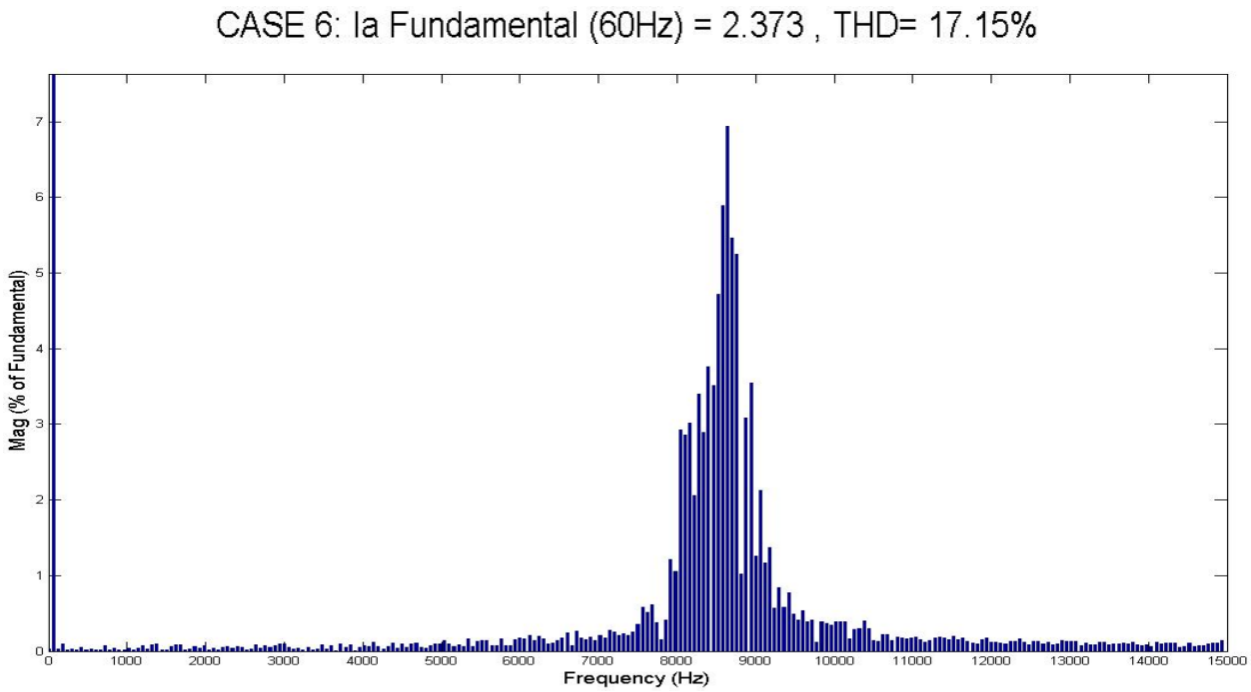


Figure 47.a: Case 6 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

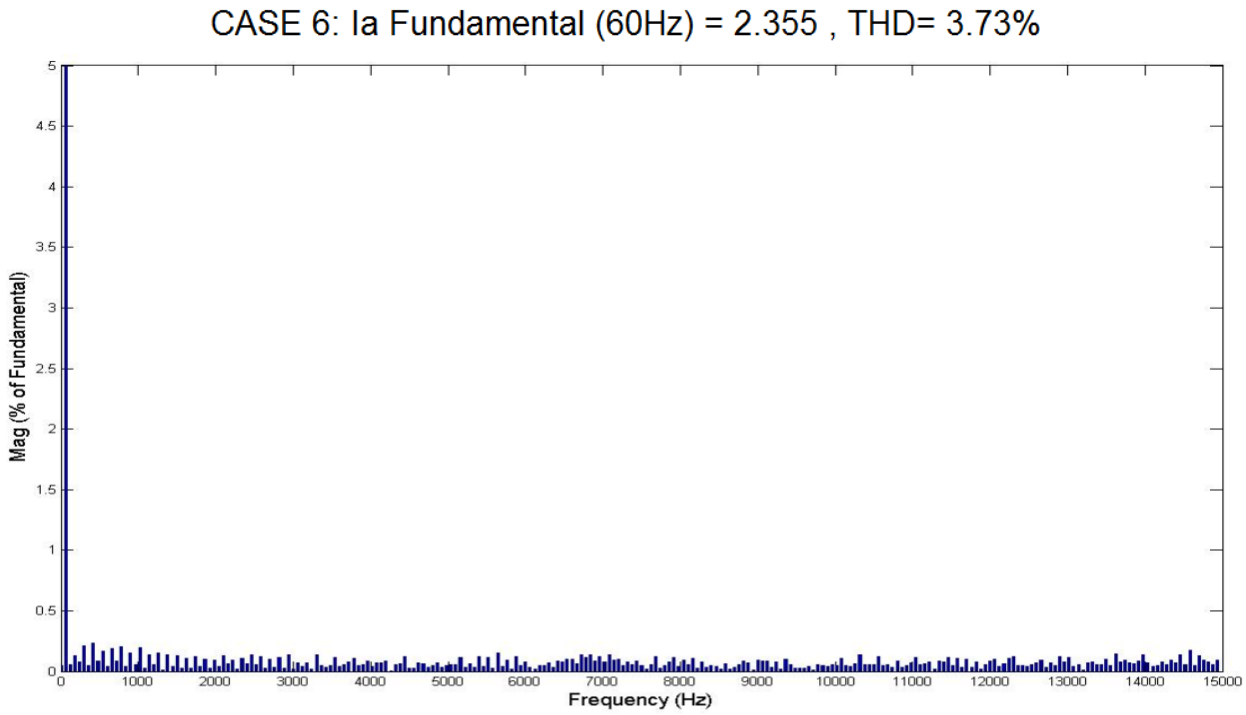


Figure 47.b: Case 6 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

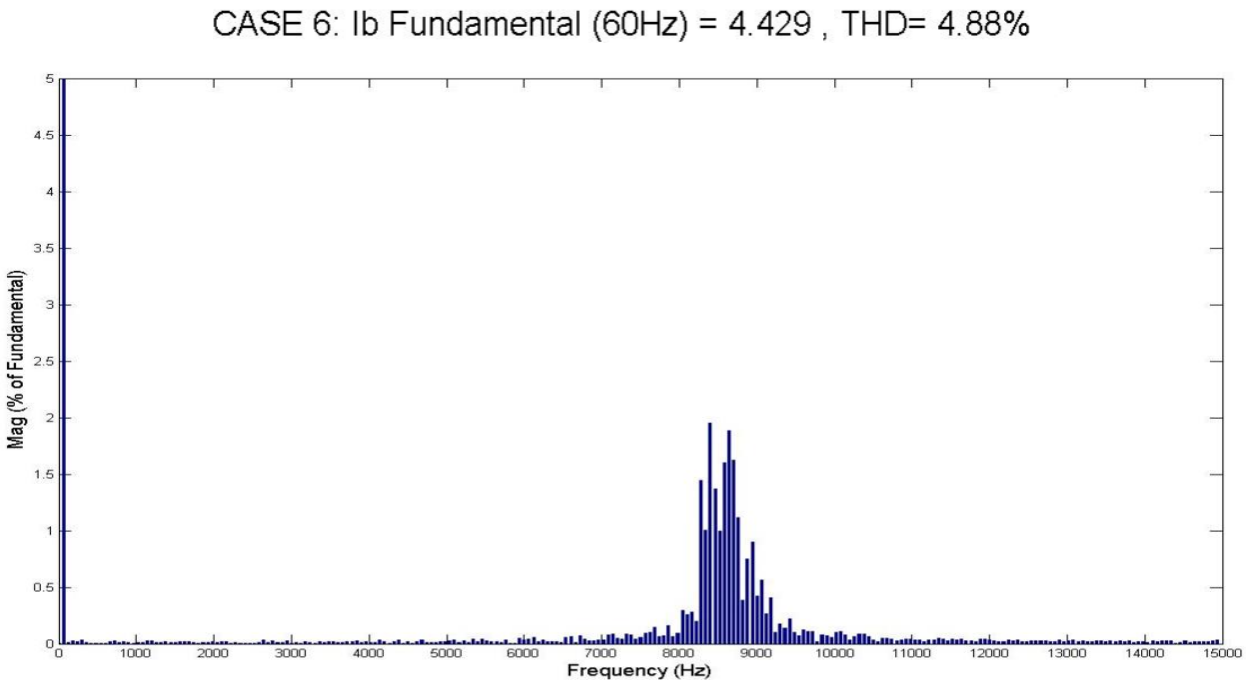


Figure 48.a: Case 6 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

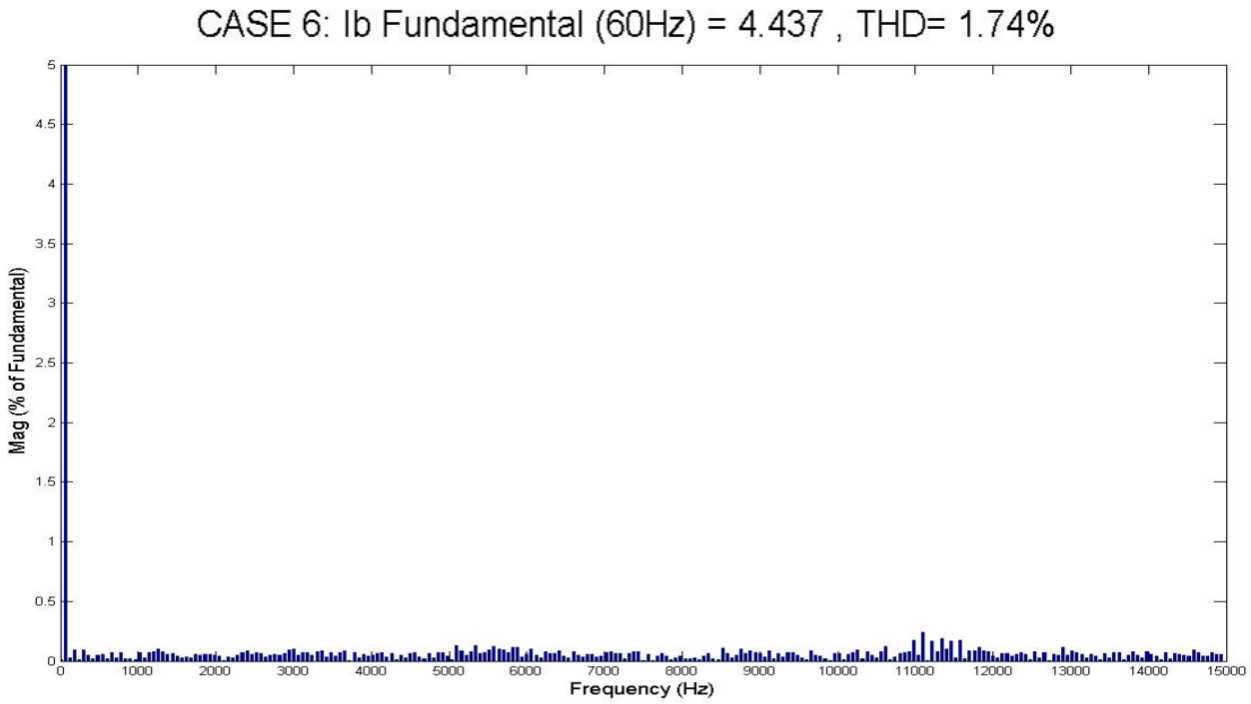


Figure 48.b: Case 6 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

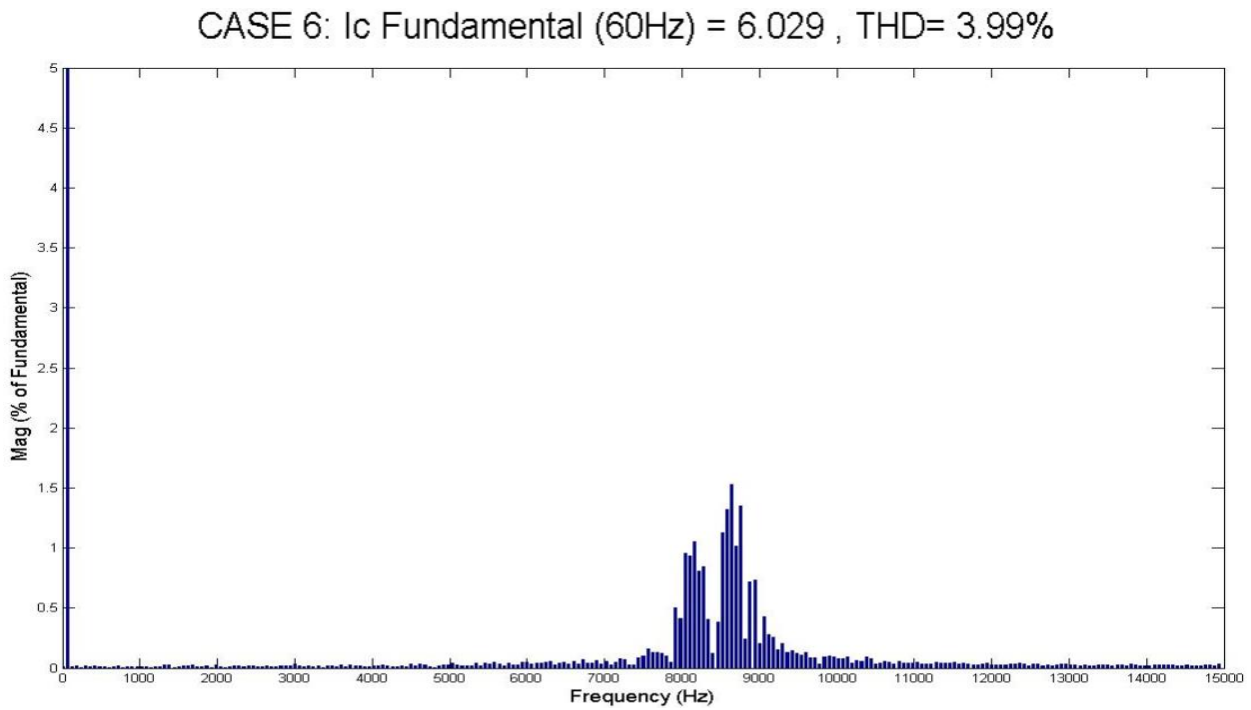


Figure 49.a: Case 6 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

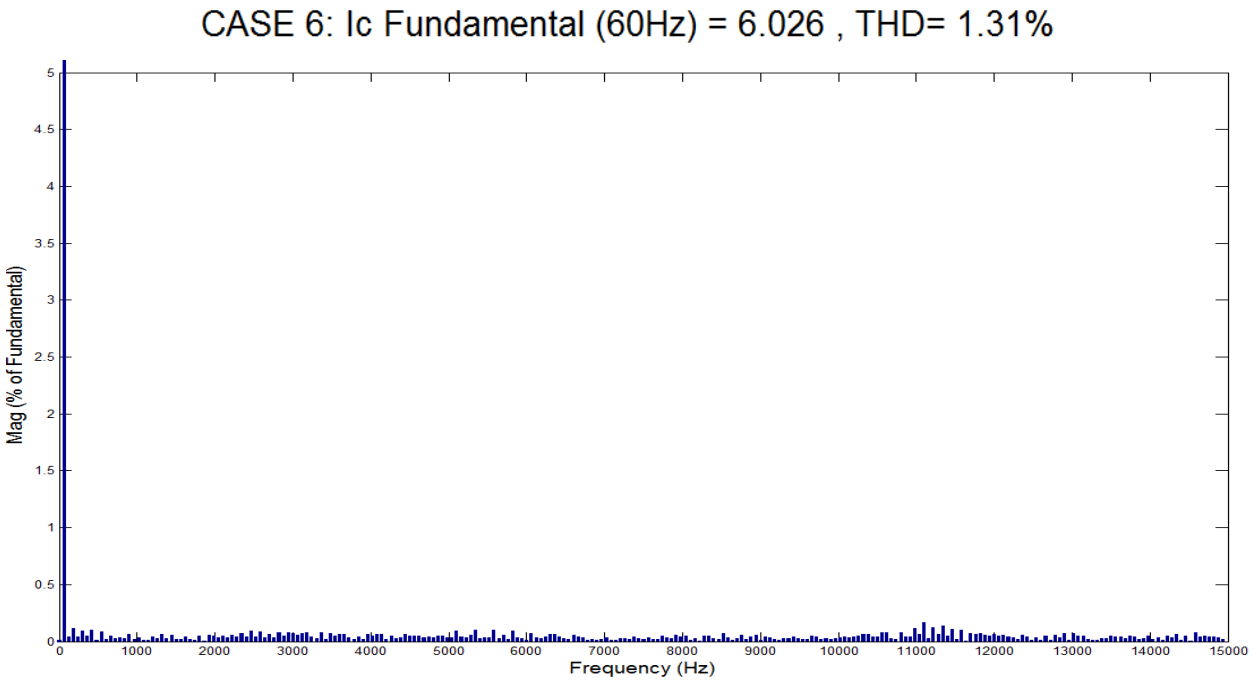


Figure 49.b: Case 6 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

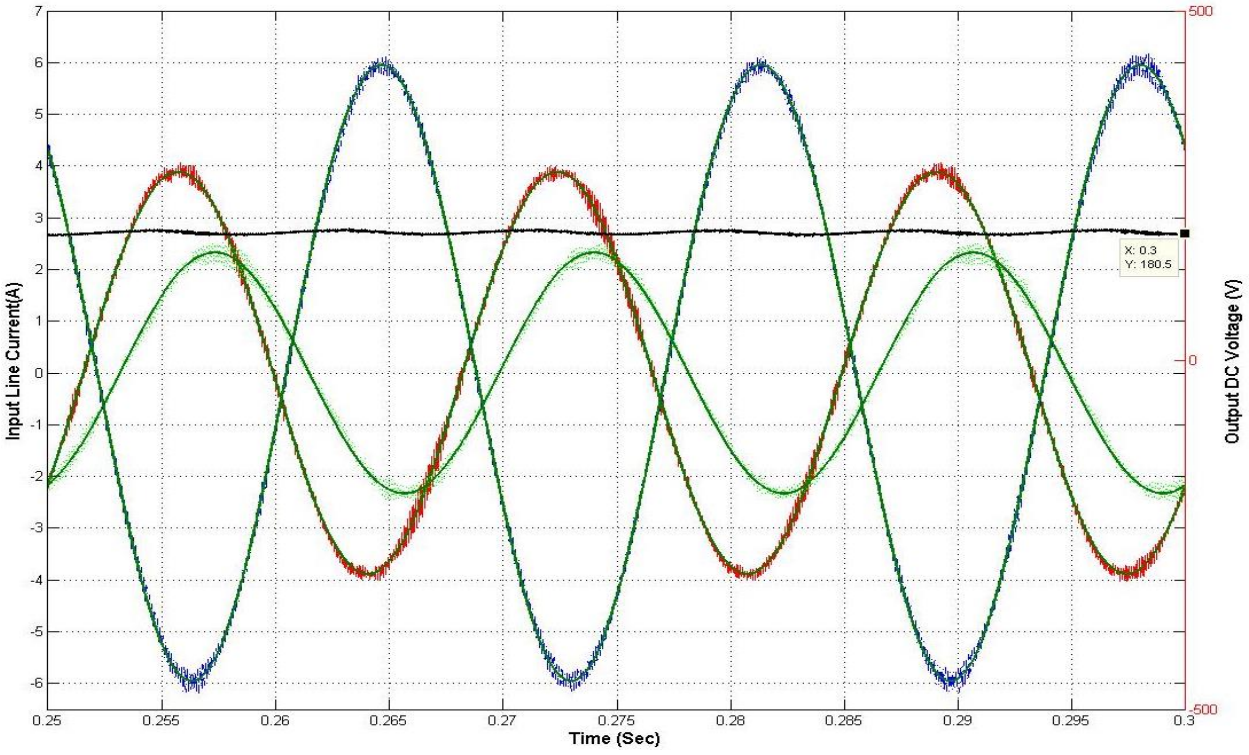


Figure 50.a: Case 7 Line currents and Output DC voltage (Constant Switching Frequency fs = 9 kHz)

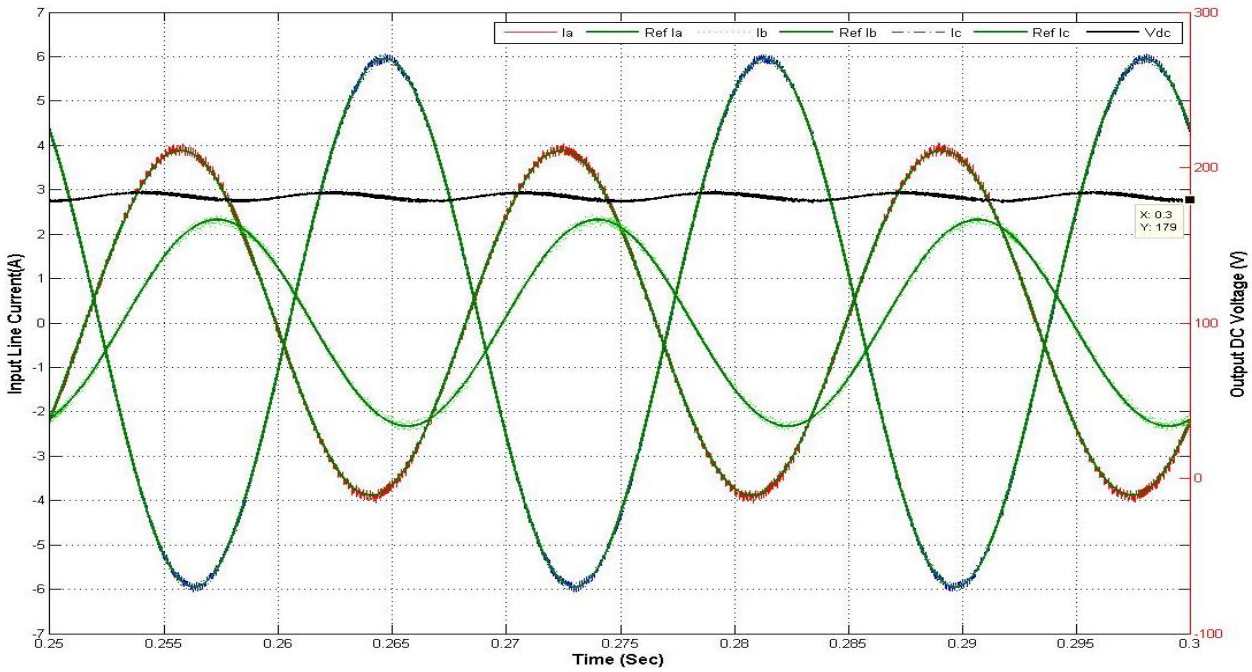


Figure 50.b: Case 7 Line currents and Output DC voltage (Constant Hysteresis band h = 0.1 A)

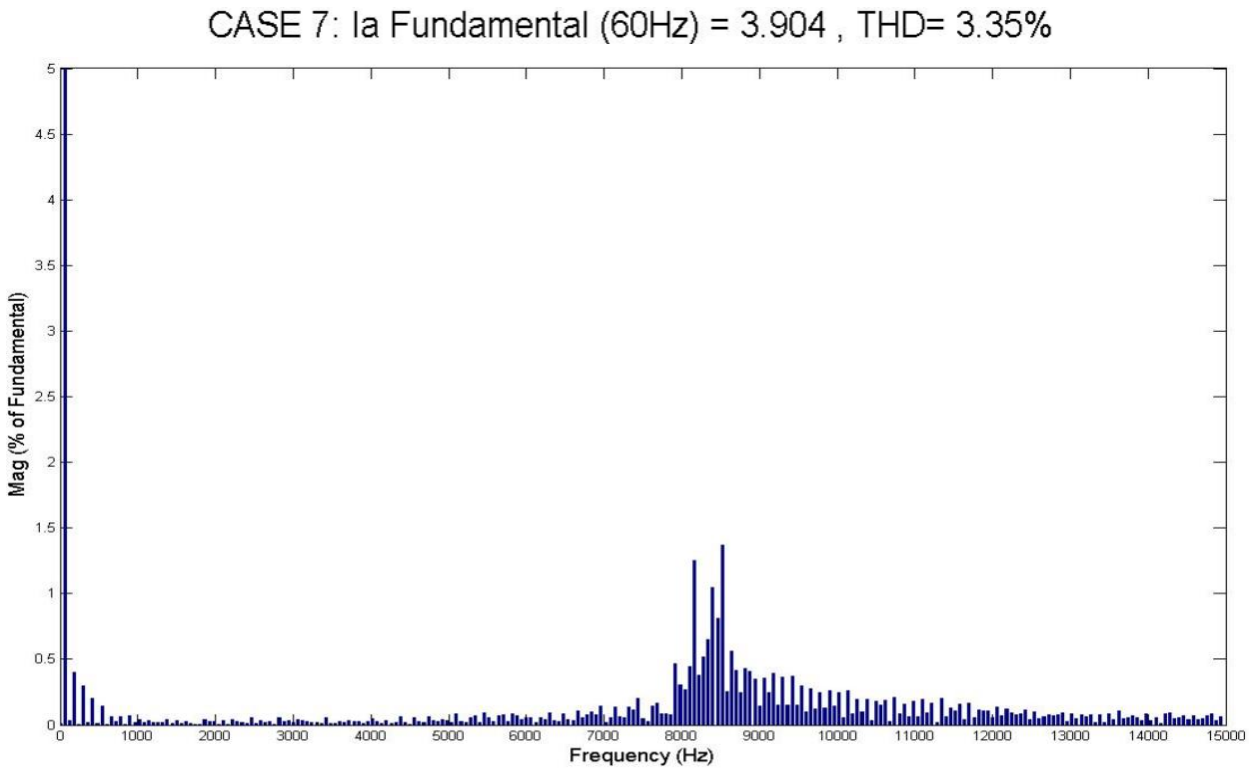


Figure 51 .a: Case 7 FFT of phase **a** line current (Constant Switching frequency fs = 9 kHz)

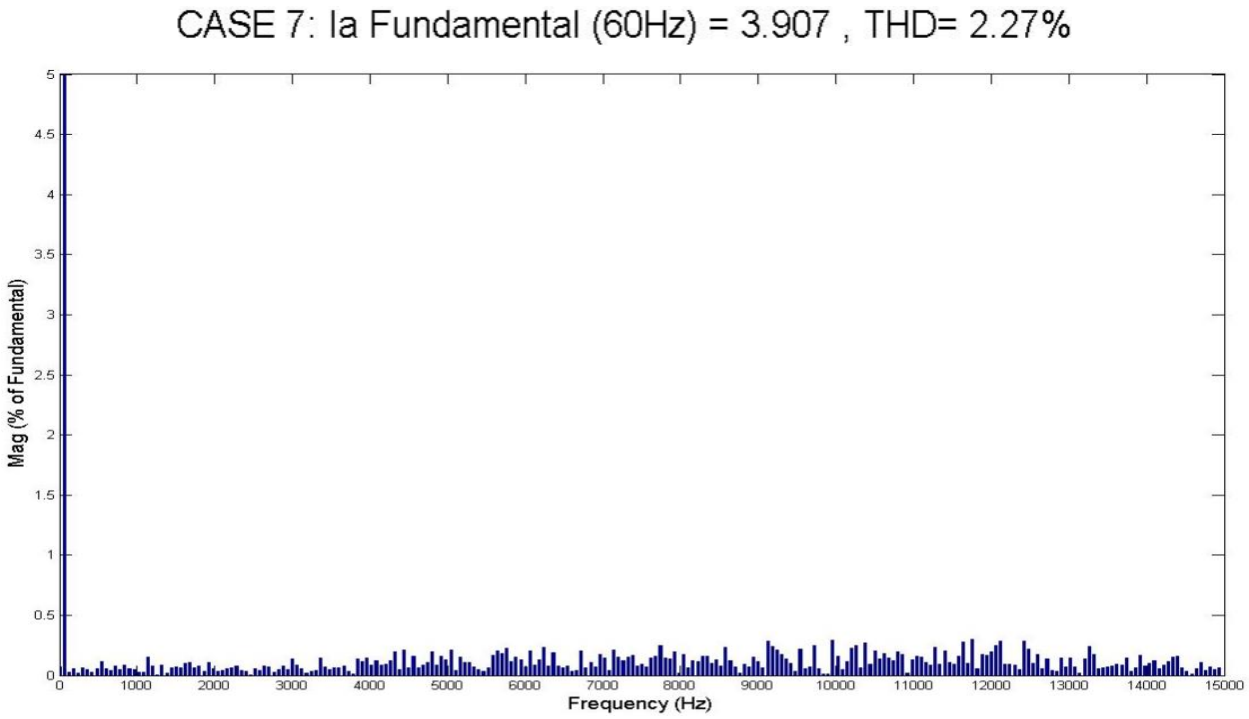


Figure 51.b: Case 7 FFT of phase **a** line current (Constant Hysteresis band h = 0.1 A)

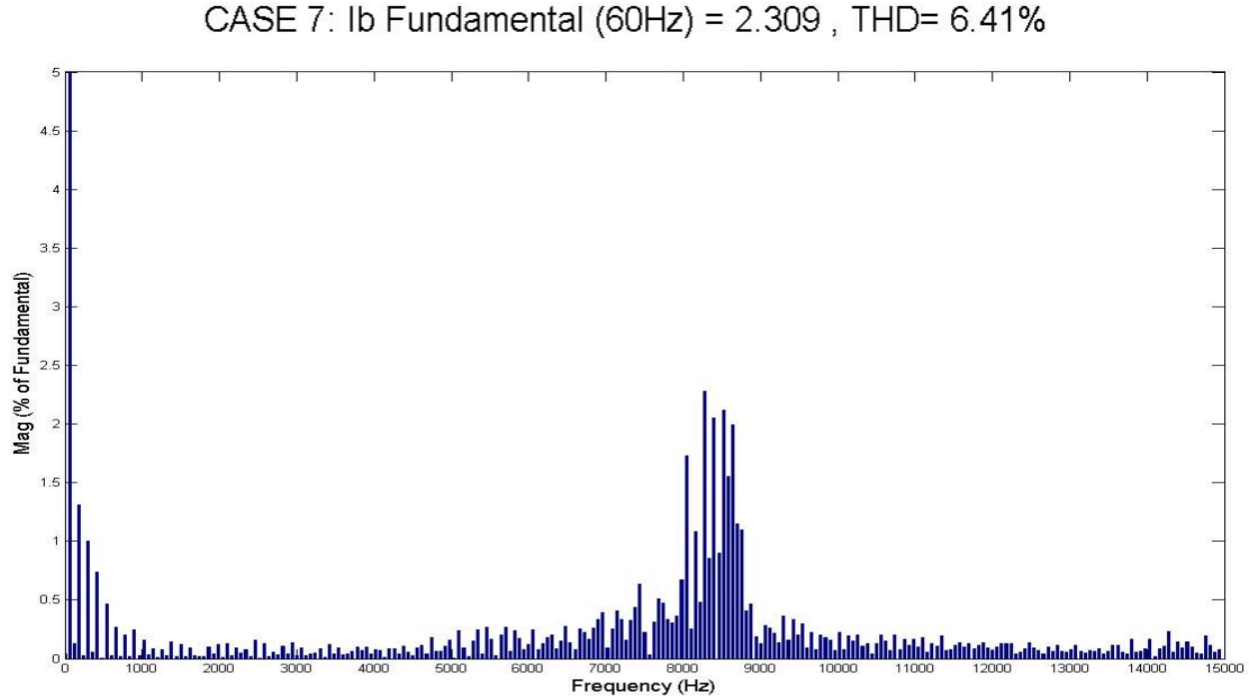


Figure 52.a: Case 7 FFT of phase **b** line current (Constant Switching frequency fs = 9 kHz)

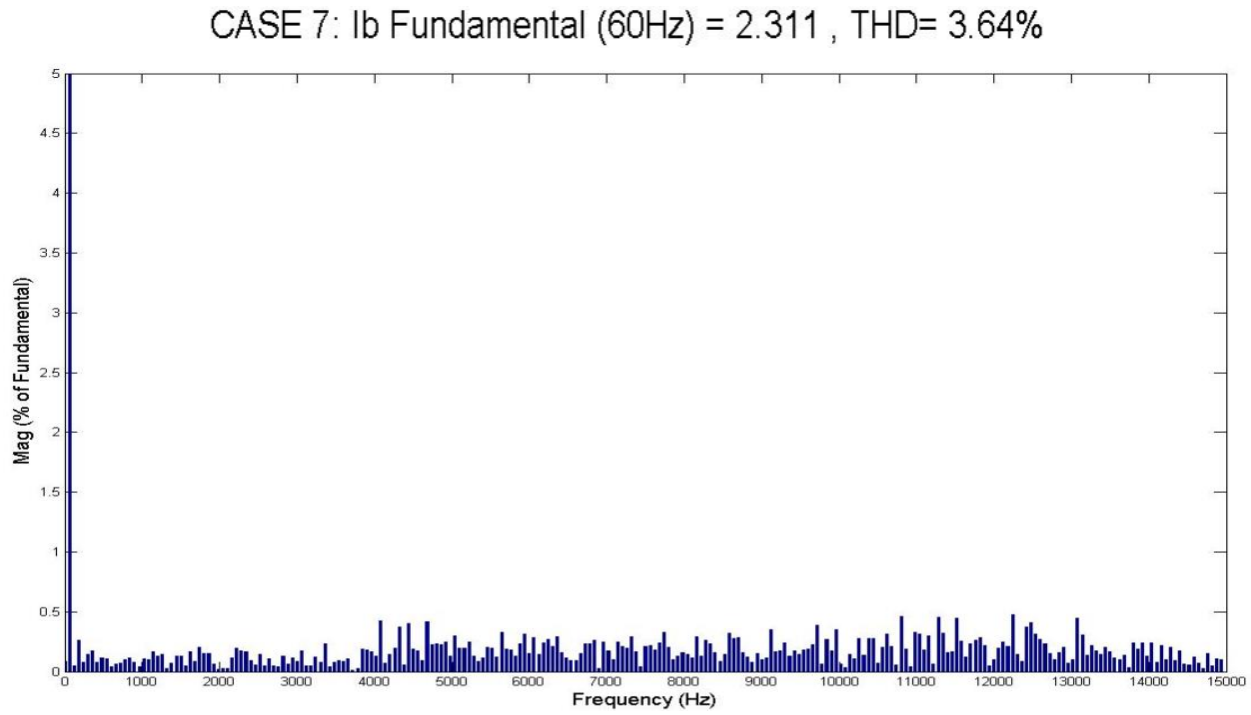


Figure 52.b: Case 7 FFT of phase **b** line current (Constant Hysteresis band h = 0.1 A)

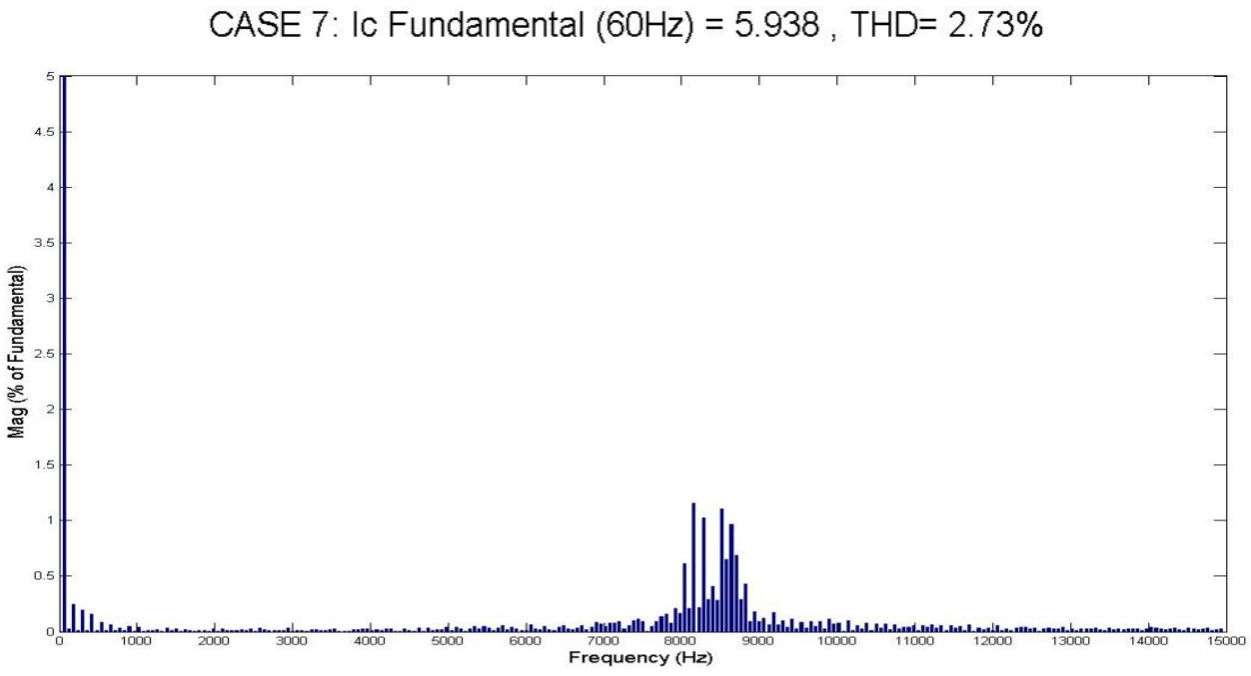


Figure 53.a: Case 7 FFT of phase **c** line current (Constant Switching frequency fs = 9 kHz)

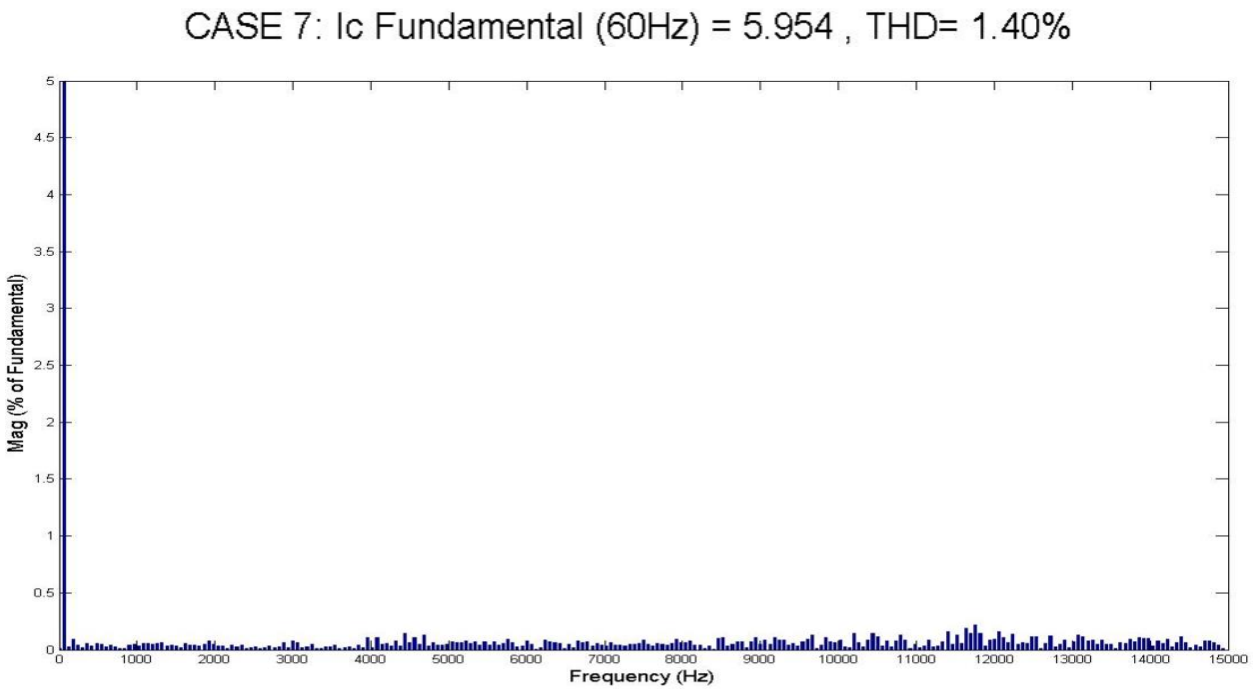


Figure 53.b: Case 7 FFT of phase **c** line current (Constant Hysteresis band h = 0.1 A)

The above results are summarized in Table IV. The steady state values of three phase input rms line currents and DC link output voltage of each case are presented. As the switching devices used in the simulation are not ideal devices, hence there is power loss across them. For extreme unbalanced cases 5, 6 and 7 losses are very high due to increase in line currents and it affects the efficiency. The table also provides input power, output power, efficiency and power factor for each cases. The efficiency of the converter is affected during extreme unbalanced condition case 5, 6 and 7.

Table V provides a summary of all the results for the condition where hysteresis bandwidth is held constant (h = 0.1A) in order to compare the results with the constant switching frequency condition. The results shows that, with the method developed in this paper, while input output harmonic elimination is successfully done under severe unbalanced condition, a constant switching frequency to a preset value is also achieved.

TABLE IV: RESULT SUMMARY (CONSTANT SWITCHING FREQUENCY fs = 9 kHz)

Case #	Input Line Currents (RMS)			Input			Output		Efficiency (%)
	Phase a (A)	Phase b (A)	Phase c (A)	Active Power (W)	Reactive Power (VAR)	Power factor	Power (W)	DC link Voltage (V)	
1	1.397	1.40	1.397	251.30	0.0155	1.00	241.96	182.00	96.28
2	1.428	1.412	1.366	252.30	0.0499	1.00	241.96	182.00	95.90
3	2.638	1.839	3.617	250.70	0.0444	1.00	226.78	176.20	90.46
4	2.712	1.795	3.513	251.50	0.0870	1.00	222.17	174.40	88.34
5	1.672	3.184	4.254	100.3	0.02214	1.00	71.65	174.50	71.43
6	1.678	3.132	4.263	100.60	0.1230	1.00	72.39	175.40	71.96
7	2.761	1.633	4.199	102.70	0.1424	1.00	76.66	180.50	74.64

TABLE V: RESULT SUMMARY (CONSTANT HYSTERESIS BANDWIDTH h = 0.1A)

Case #	Input Line Currents (RMS)			Input Power			Output		Efficiency (%)
	Phase a (A)	Phase b (A)	Phase c (A)	Active (W)	Reactive (VAR)	Power factor	Power (W)	DC link Voltage (V)	
1	1.399	1.40	1.399	251.70	0.3051	1.00	243.29	182.50	96.66
2	1.426	1.399	1.362	250.90	0.0352	1.00	243.02	182.40	96.86
3	2.636	1.795	3.624	251.40	0.6426	1.00	224.47	175.30	89.29
4	2.714	1.827	3.514	250.30	0.2389	1.00	225.24	175.60	89.99
5	1.681	3.186	4.259	101.00	0.0999	1.00	72.31	175.30	71.59
6	1.665	3.137	4.261	99.92	0.1698	1.00	71.65	174.50	71.71
7	2.763	1.634	4.210	102.00	0.8167	1.00	75.39	179.00	73.91

3.4.2 Closed Loop Results

The closed loop operation of the PWM boost type rectifier is performed for three cases from the Table I viz. case 1, 2 and 3. Case 1 is balanced operation and the other two cases are taken to prove the feasibility of method in unbalanced operating condition. The simulation and device parameters used for the closed loop operation are same as that of open loop operation. To show the DC link control of the converter the reference value of output DC link is changed online during

simulation. The converter operates at the changed output DC reference and then returns back to its initial condition during simulation. The average value of output DC link, three phase input line currents, switching frequency and the unity power factor operation of the system is inspected during closed loop operation under steady state condition. The operation parameters used for the closed operation is provided in Table VI.

TABLE VI: CLOSED LOOP OPERATION PARAMETERS

Case #	Output DC link setting		
	Time 0.05s-0.07s	**Time 0.07s-0.23s**	**Time 0.23s-0.3s**
1	182.1 Volt	200 Volt	182.1 Volt
2	182.1 Volt	200 Volt	182.1 Volt
3	176.7 Volt	200 Volt	176.7 Volt

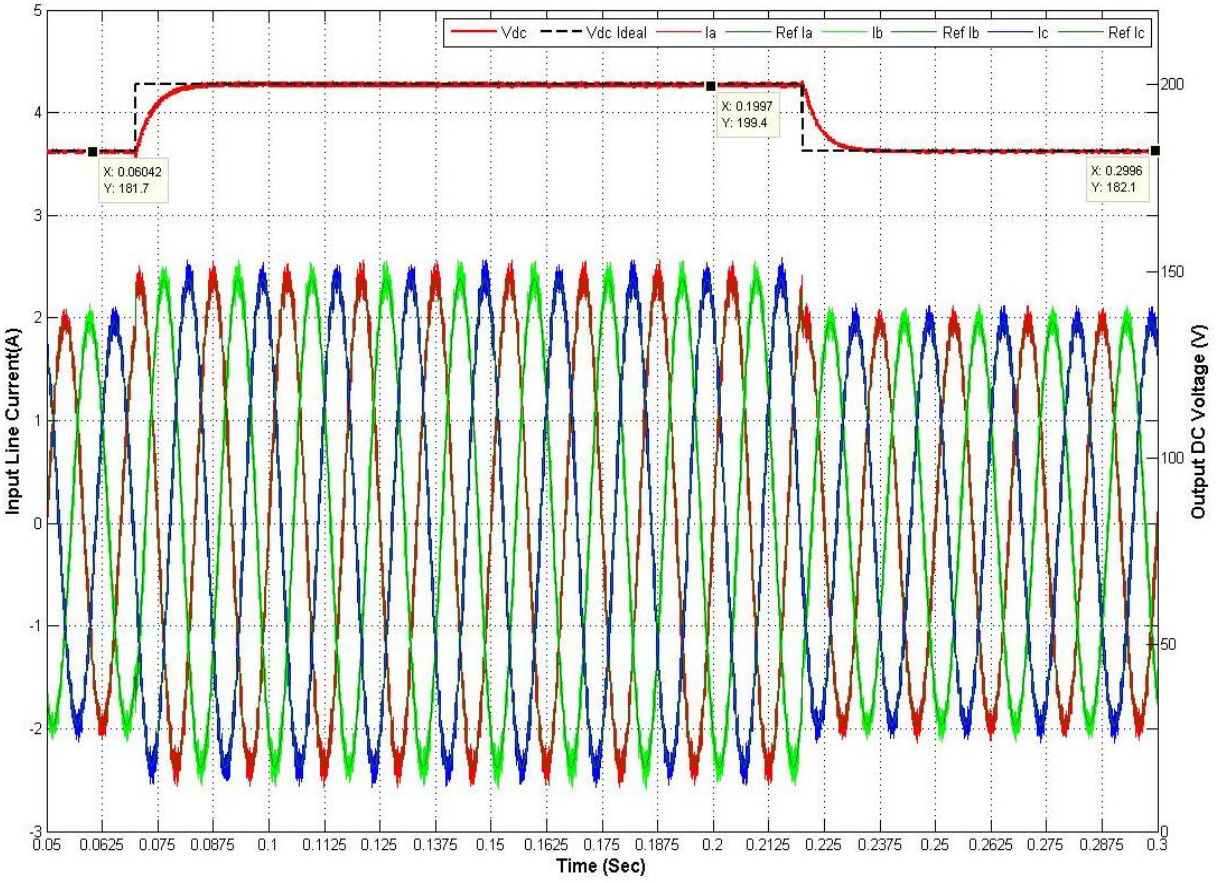


Figure 54: Case 1 Three phase input line currents and output voltage DC link for closed loop operation

Fig. 54 shows that at the pre-set value of time the output DC link voltage changes to 200V and then return backs to initial condition as desired for closed loop operation of the converter. The ideal behavior of closed loop performance is shown in black stripped line and referred as 'Vdc ideal'. To prove the feasibility of method in retaining the ability to have constant switching at a preset value i.e. 9 kHz as desired, Fourier analysis of one cycle of the input line current phase **a** is done at two instances. The first instance is taken when the output DC voltage changes from 182.1 V to 200 V at time, t = 0.18 seconds, and second instance, at time t = 0.27 seconds, is taken when the converter changes the output DC link voltage back from 200 V to 182.1 V. Active power (P) and reactive power (Q) of the system is also plotted to prove the unity power factor operation at all time during simulation. Fig. 55.a and Fig. 55.b give FFT of one cycle of input phase **a** line current. Both the results shows that the system work in near constant switching frequency at the pre-set value of 9 kHz successfully under closed loop operation.

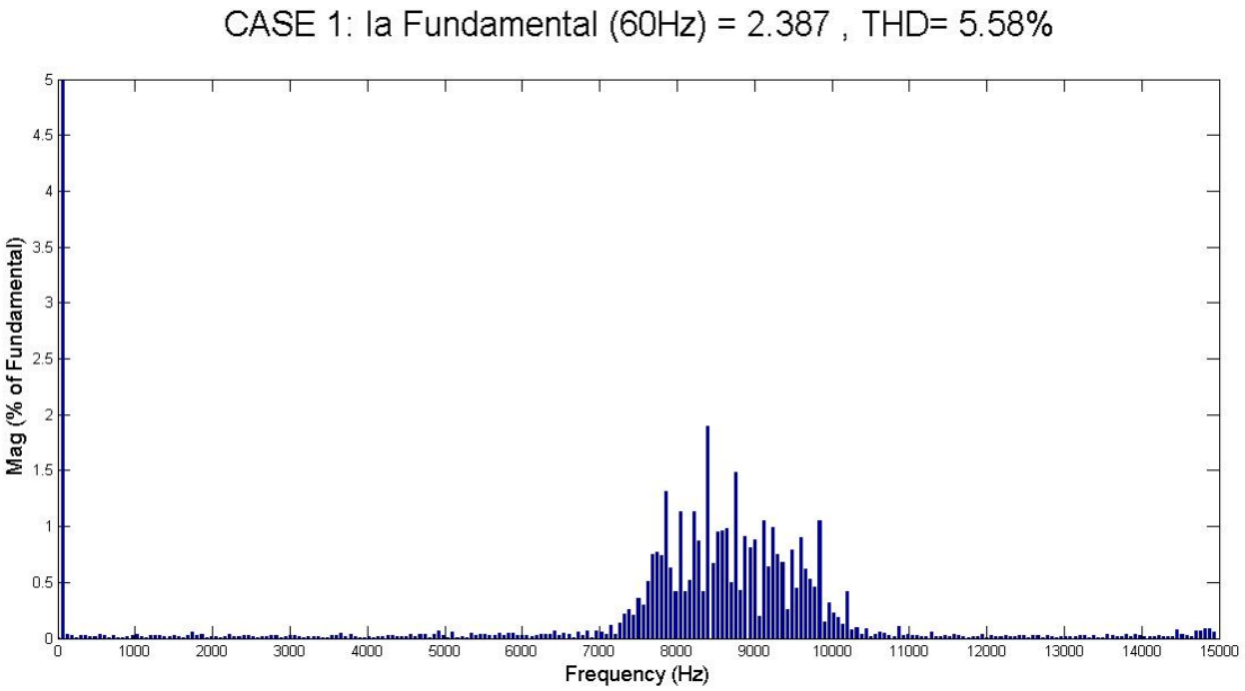


Figure 55.a: Case 1 FFT of phase **a** line current for one cycle at t = 0.18 seconds

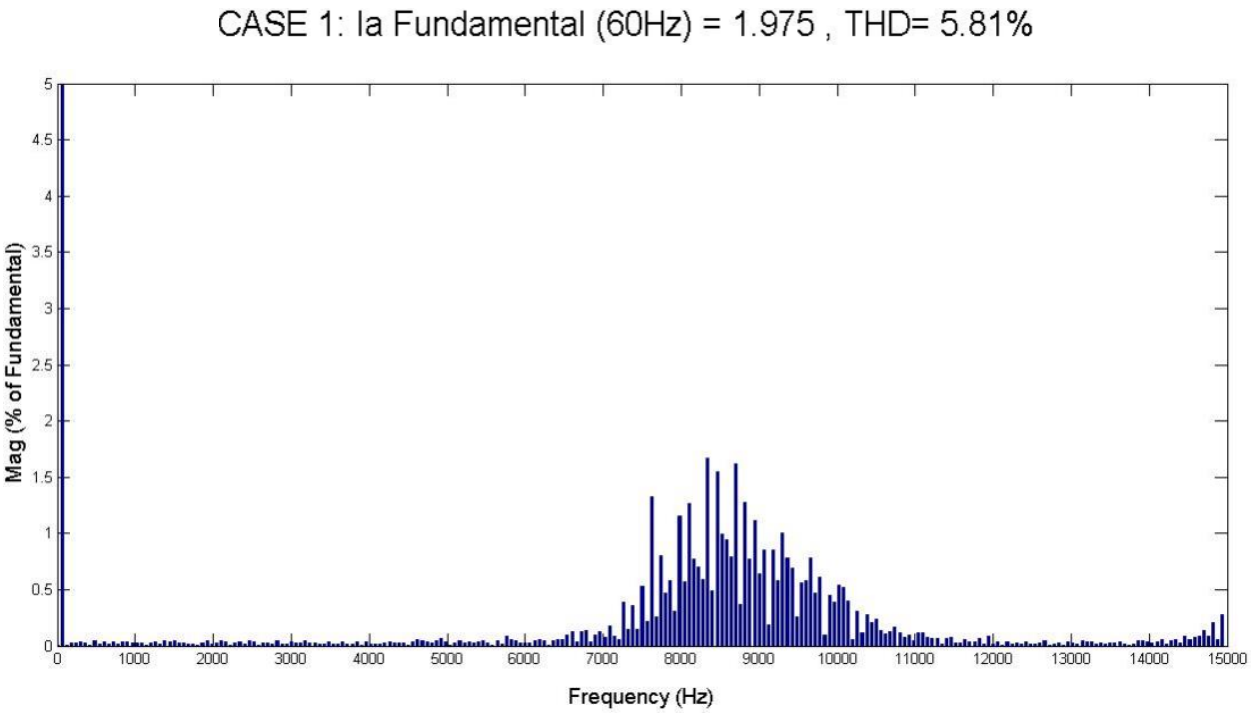


Figure 55.b: Case 1 FFT of phase **a** line current for one cycle at t = 0.27 seconds

Fig. 56 shows that the system operates successfully at unity power factor during change in output DC link control for closed operation successfully. Similarly the results of case 2 and case 3 under unbalanced operations of the PWM boost are shown in Fig. 57 through Fig. 62.

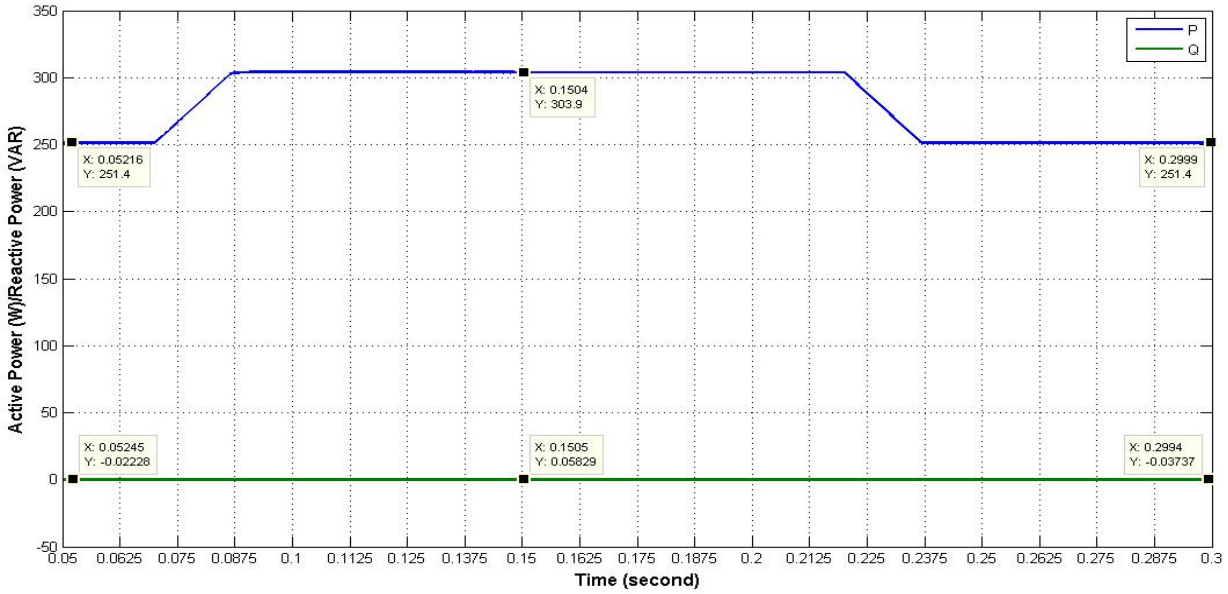


Figure 56: Case 1 Active Power (P) and Reactive Power (Q) for closed loop operation

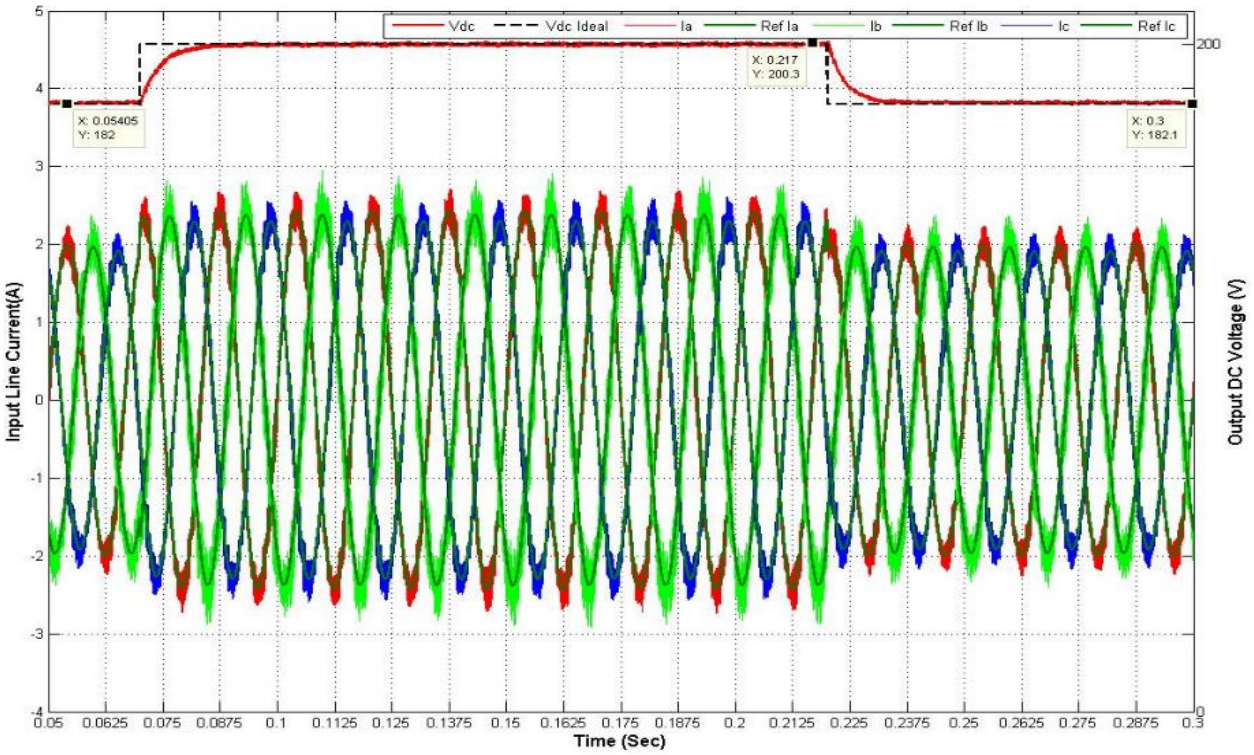


Figure 57: Case 2 Three phase input line currents and output voltage DC link for closed loop operation

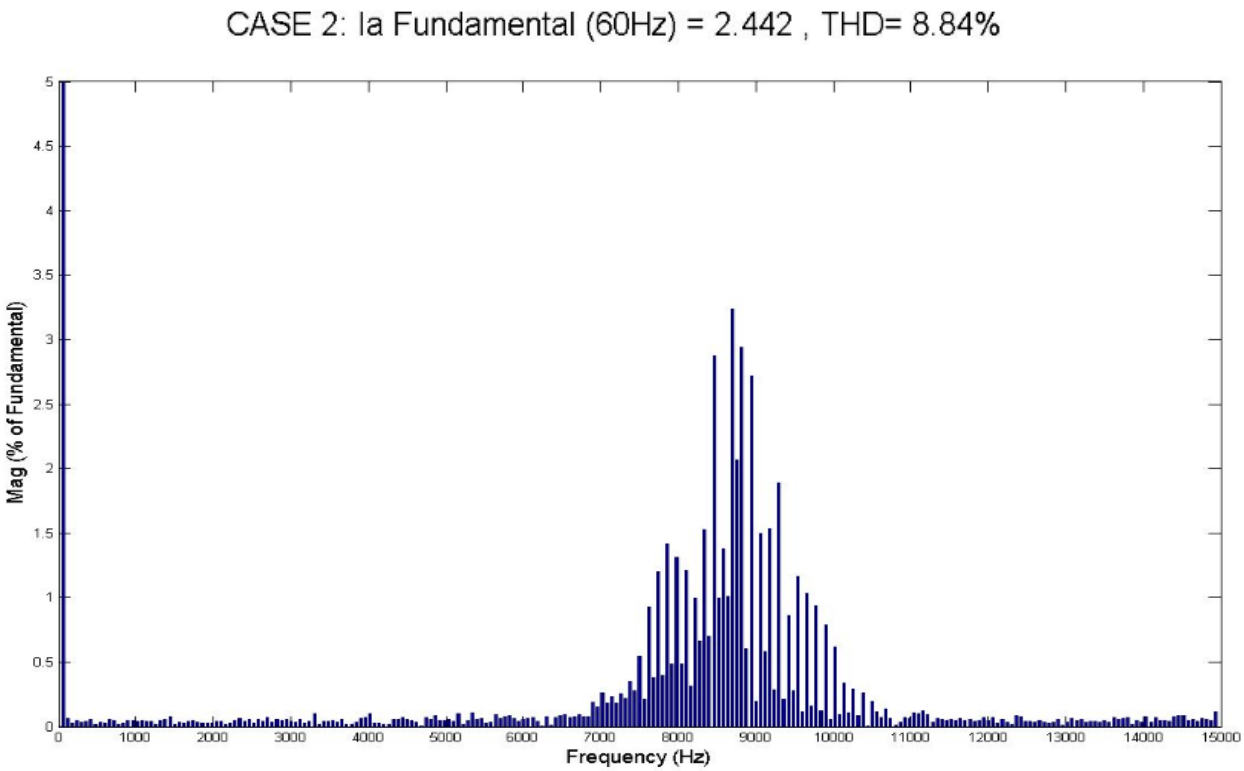


Figure 58.a: Case 2 FFT of phase **a** line current for one cycle at t = 0.18 seconds

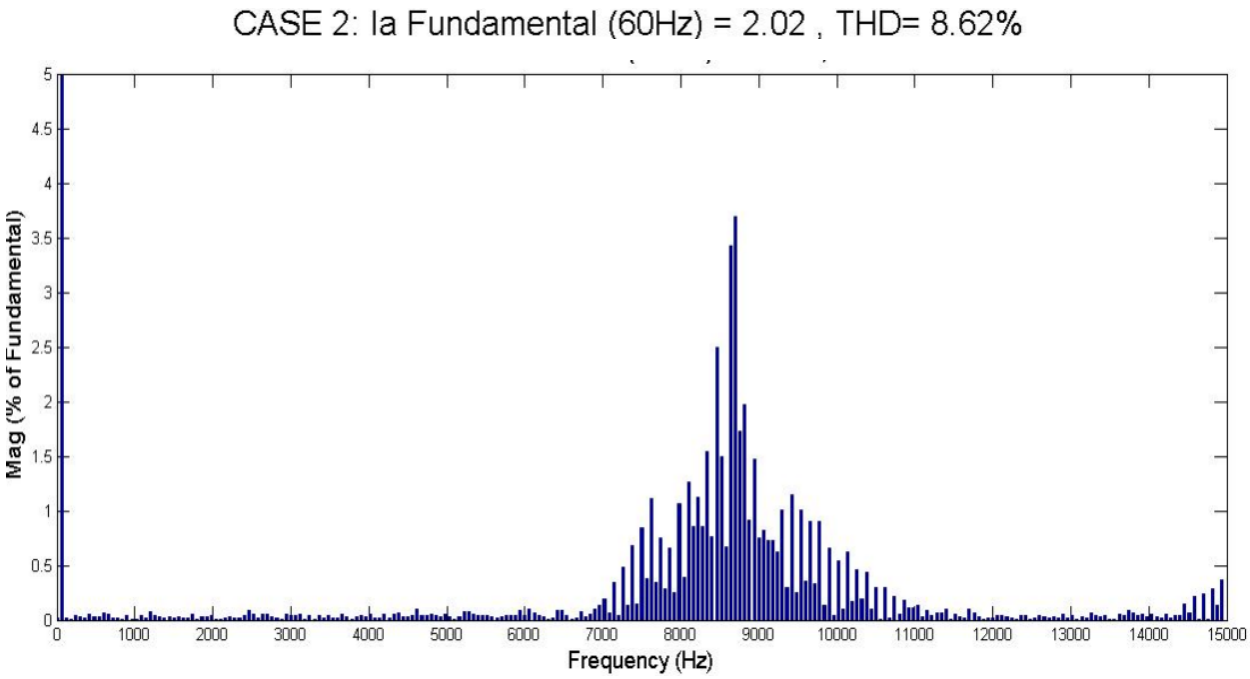


Figure 58.b: Case 2 FFT of phase **a** line current for one cycle at t = 0.27 seconds

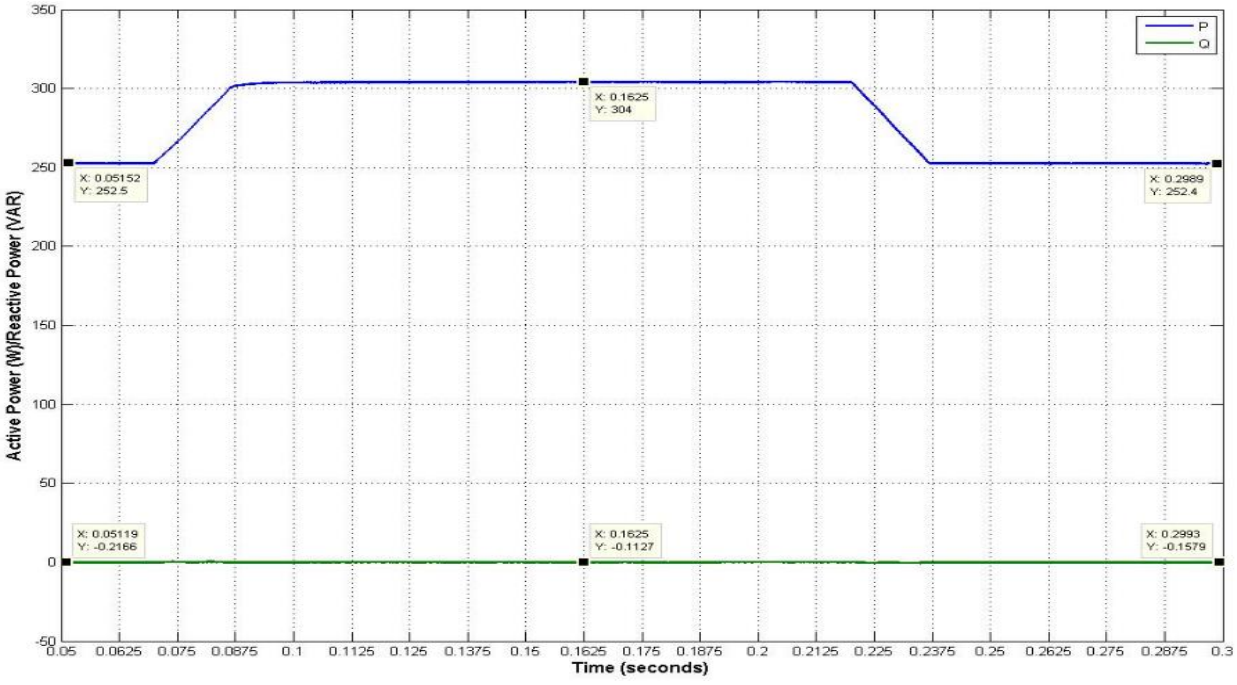


Figure 59: Case 2 Active Power (P) and Reactive Power (Q) for closed loop operation

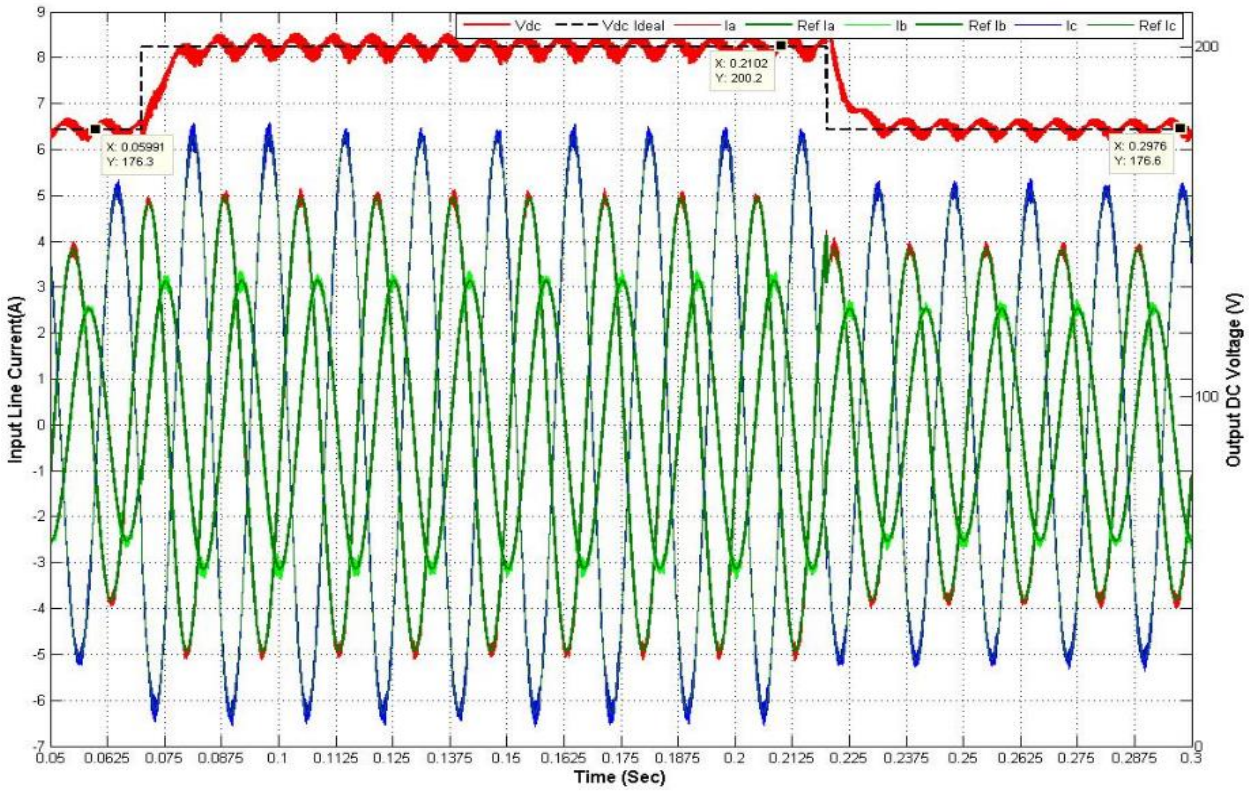


Figure 60: Case 3 Three phase input line currents and output voltage DC link for closed loop operation

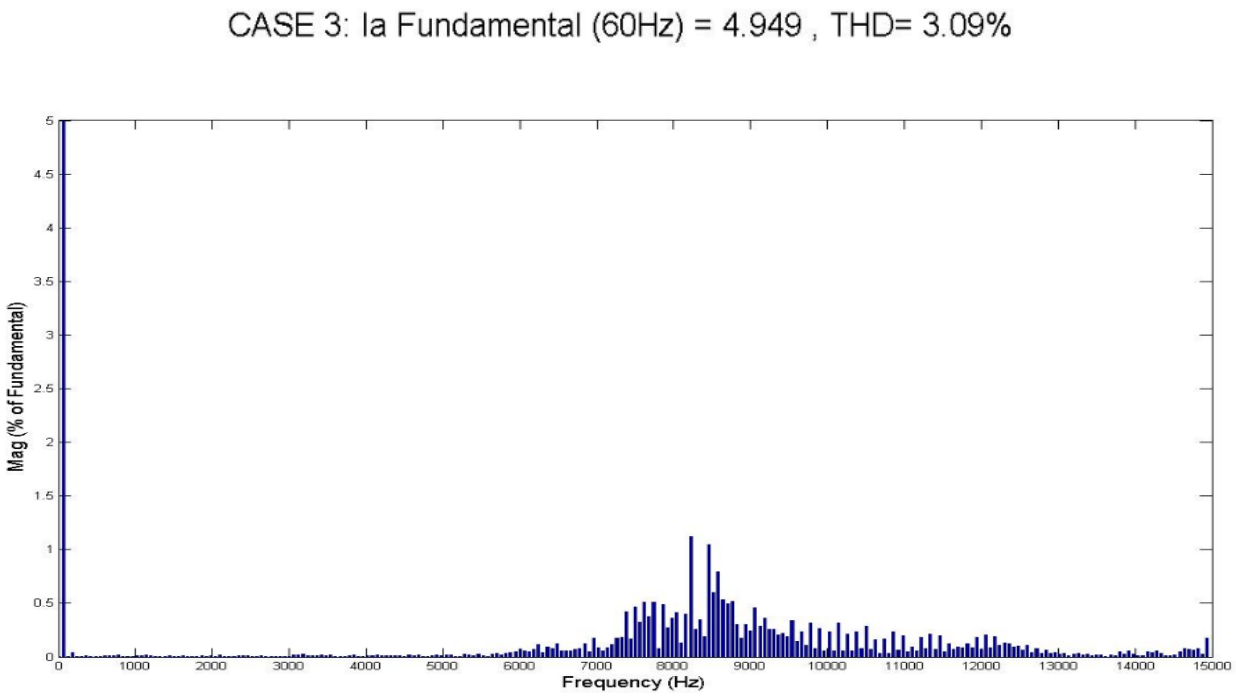


Figure 61.a: Case 3 FFT of phase **a** line current for one cycle at t = 0.18 seconds

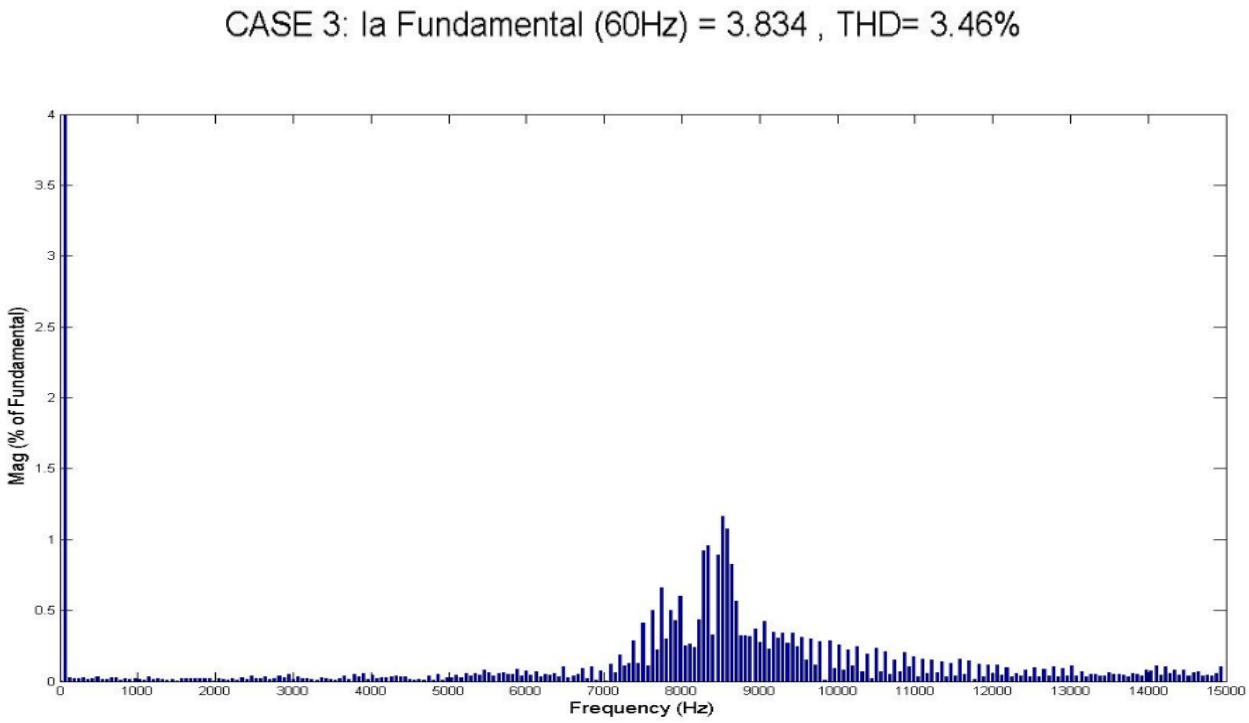


Figure 61.b: Case 3 FFT of phase **a** line current for one cycle at t = 0.27 seconds

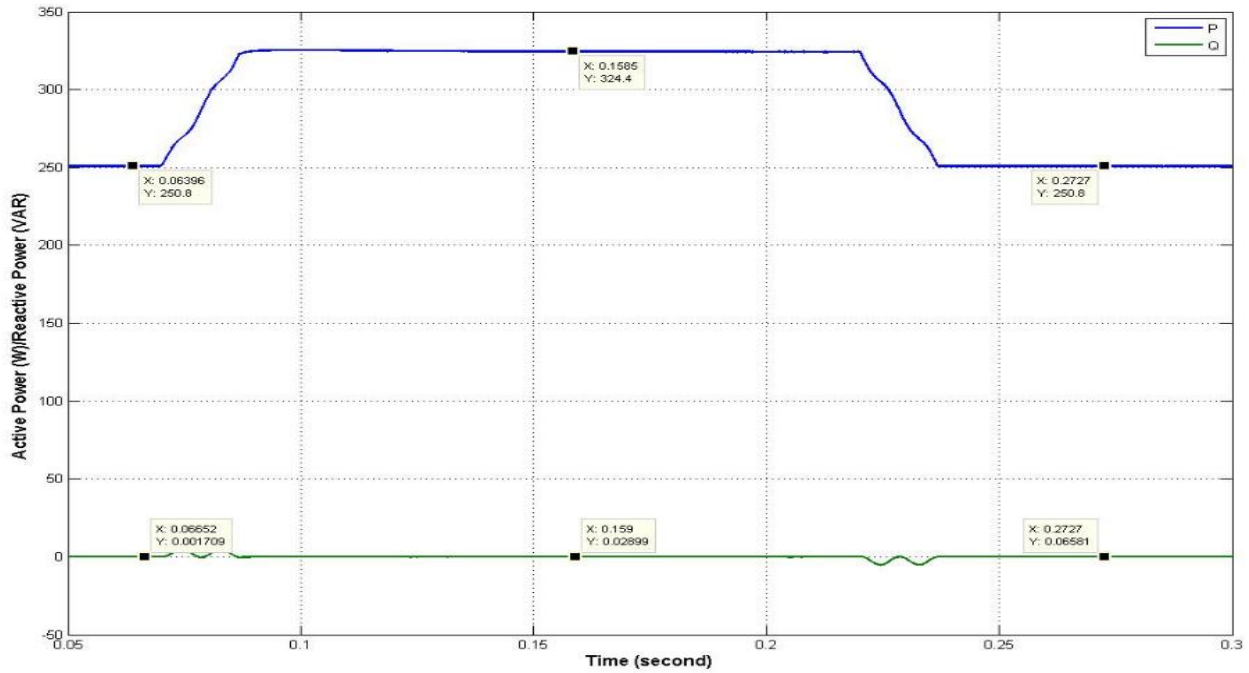


Figure 62: Case 3 Active Power (P) and Reactive Power (Q) for closed loop operation

The above results suggest that the method is effective for extreme unbalanced operating cases and it successfully operates at near constant switching frequency at a predetermined value. It maintains its unity power factor operation as assumed during operation. The method is also operated under closed loop condition as a controllable output DC link and the near constant switching frequency is successfully achieved under steady state condition maintaining input output harmonic elimination.

Chapter IV

EXPERIMENTAL RESULTS

The theoretical analysis and simulation results prove the validity of the method. In this chapter practical analysis of the method using experimental set up is presented. The set up uses Lab-Volt test bench and DSPACE real time implementation module for the experimental verification. MATLAB/Simulink is used as platform to build and implement the control algorithm. All the functional blocks used in implementation is explained in details in the coming sections.

First analysis of all the hardware elements used for building the model is done. Then the Simulink model is explained which is used to implement the control algorithm which is then compiled and uploaded to the Digital Signal Processor board used for real time operation. A Control Desk next generation software is used for result analysis and operation in real time.

Finally, results of the Simulink model of the experimental setup and Experimental model results are presented and compared to analyze the results obtained. The limitations of this experimental set up and various constraints are discussed in details

4.1 Experimental Model

The experimental set up for PWM boost type rectifier is operated using the proposed near constant switching frequency method. The input-output harmonic elimination method is used to calculate the magnitude and phase angle of the reference currents. There are four major parts of experimental prototyping of the converter.

The components of the experimental prototype are

1. Lab-Volt Test Bench Setup
2. Gate Driver Circuit
3. DSPACE Digital Signal Processing Controller
4. MATLAB/Simulink Control Algorithm

4.1.1 Lab-Volt Test Bench Setup

The three PWM boost type rectifier consists of three phase voltage source which is variable in nature and is connected to three input inductors L_1, L_2 and L_3. The three outputs of the input inductors are connected to three phase MOSFET/IGBT bridge rectifier. In this experiment MOSFET bridge is used to achieve constant frequency for balanced and unbalanced cases of Table I. The output of MOSFET bridge is fed to two capacitors C_1 and C_2 which are connected in series. The output of the capacitors is connected to resistive load R. A functional diagram of the experimental setup is shown in Fig. 63.

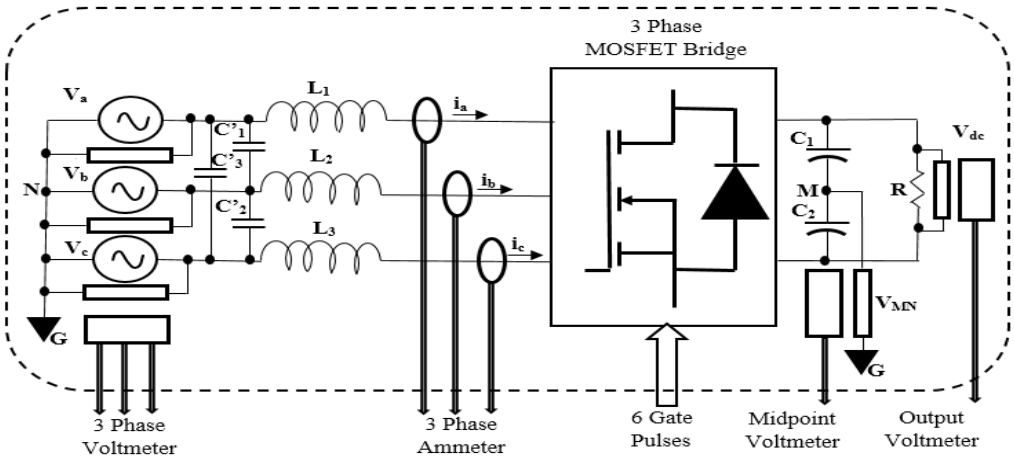


Figure 63: Schematic of Lab-Volt test bench and hardware set up

There are eight parameters which are measured during the operation. Three voltmeters are used to measure each input phase voltage $\boldsymbol{V_a}$, $\boldsymbol{V_b}$ and $\boldsymbol{V_c}$ with respect to neutral which is connected to ground G. There are three ammeters measuring line currents from each phase. Two more voltmeters are used to measure the output voltage across the load and voltage at midpoint M of the capacitors C_1 and C_2 with respect to neutral N. Since, neutral in this set up is connected to ground G, hence the midpoint voltage with respect to ground is same as the neutral. It must be noted that the midpoint of capacitors C_1 and C_2 is not grounded or connected to neutral. There are six external inputs required for the system, which is received as gate signals for the operation of three phase MOSFET bridge converter as desired.

The midpoint voltage measured is very low in amplitude and has lot of switching noises. Hence, we also use an amplifier and low frequency filter to make it useful for further calculations. $\boldsymbol{C'_1}$, $\boldsymbol{C'_2}$ and $\boldsymbol{C'_3}$ are used to smoothen the input three phase voltage from the source.

Table I shows the list of equipment used for experimental set using Lab-Volt test benches and measuring instruments used for result verification. Oscilloscope is used for Fourier transform verification of the line currents. Fluke's Power Quality Analyzer is used for measuring the input voltages, line current, input complex power, power factor and total harmonic distortion (THD) of each phase.

TABLE VII: LIST OF EQUIPMENT AND INSTRUMENTS

Item #	Description	Model	Manufacturer
1	Three phase AC voltage source	EMS 8321	Lab-Volt
2	3 X Series Inductor 10mH	195J20	Hammond Reactor
3	Power MOSFET Bridge	EMS 8837-00	Lab-Volt
4	DC Power Supply	1730 A	BK Precision
5	Resistive Load	EMS 8311-00	Lab-Volt
6	3 X Capacitor	380LX	CDE USA
7	2 X Capacitor	401502-3A	Sangamo
8	PID Controller	EMS 9034	Lab-Volt
9	Voltage Isolator	P 5200	Tektronix
10	Current Probe	80i-110s	Fluke
11	Voltage Isolator/Current Isolator	EMS 9056-10	Lab-Volt
12	Multi-Meter	177	Fluke
13	Oscilloscope	TDS 2014	Tektronix
14	Power Quality Analyzer	43 B	Fluke

4.1.2 Gate Driver Circuit

A driver circuit is needed to trigger six MOSFETs in the three phase MOSFET bridge converter device. The driver circuit generates six gate pulses depending on input logic signal. The drive board is designed using IR21091S driver chip. It converts three gate logic signals coming from DSPACE to six gate signals which is used to switch MOSFET bridge circuit. The driver chip has programmable dead time.

'Dead time' specification is very important for successful operation of a bridge rectifier in practical world. It is important to prevent two switches of same leg from being ON position at same time. As this will result in short circuit of output passive voltage source i.e. two capacitors connected in series at the output end. Hence, for small instance both of the switches on the same leg are in OFF state and this small time is called dead time. Dead time of the driver chip is programmed by introducing a resistor between the DT/SD pin and COM pin. Fig. 64 [29] shows how the gate driver circuit is connected to a single phase one leg of three phase MOSFET bridge rectifier. The logic pulse coming from the DSPACE controller is converter to two gating pulses for switching of upper and lower MOSFETs of each leg the bridge converter circuit.

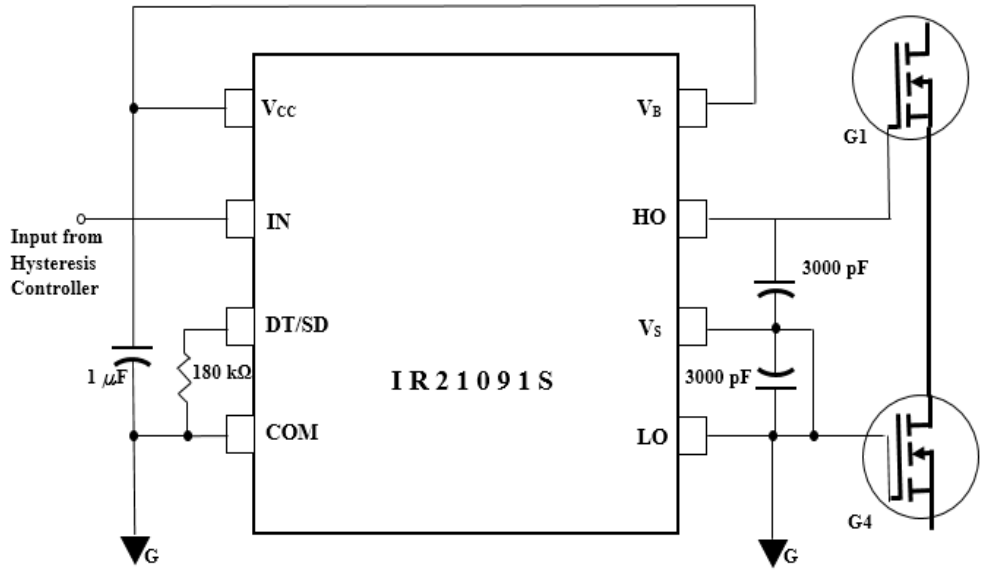


Figure 64: Schematic of gate driver circuit for single phase

4.1.3 DSPACE Digital Signal Processing Controller

DSPACE digital signal processor is used as a current controller for the experiment. This equipment has three parts which is aid to real time implementation of the project.

1. The processor DS1104
2. The connector panel CLP 1104
3. The graphical user interface (GUI) Control desk next generation

The DS1104 is 64 bit floating point processor with clock frequency of 250 MHz. It has on-chip peripherals and is very convenient to connect with computer using 32 bit PCI slot [ ]. It has 8 analog to digital converter (A/D) channels. These A/D Channels are divided into two parts, four of them are multiplex channels and other four parallel channels. It has 8 digital to analog (D/A) converter channels. All the 8 A/D channels are used to acquire signals from external devices. Three phase input voltage signals and midpoint voltage signal of two capacitors with respect to neutral are acquired through four multiplex A/D channels. Phase '**a**' signal is also used for synchronizing. Three phase line current signals and output DC voltage signal is acquired by other four parallel A/D channels. Bandwidth calculation and hysteresis comparison is implemented in DSPACE ds1104 controller. The output logic signals are provided to Gate driver circuit through three D/A channels of the controller. Fig. 65 shows the picture of ds1104 controller board.

Figure 65. Picture of DSPACE DS1104 controller board (courtesy DSPACE)

The connector panel CLP 1104 is used for connecting external devices to the controller board DS1104. It has 16 BNC connectors, 37-pin digital I/O male sub-D connectors, 37-pin slave I/O PWM female sub-D connectors, 15-pin female sub-D incremental encoder interface connector, UART RS 232 connectors and UART RS 422/485 connector. It also has LED indicator panel which indicates the digital signal status. Fig. 66 shows the picture of CLP 1104 connector panel. BNC connectors are used to connect external devices

Figure 66: Picture of CLP 1104 connector board.

from the Lab-Volt test bench to the DSPACE controller board where we perform calculation on the acquired device signals and give the output gate pulses to drive circuit through D/A channel BNC connectors.

Control desk next generation software is used as graphical user interface (GUI) for monitoring and measuring the input and output from the DSPACE controller. A main switch is designed to enable on-line operation of the PWM boost converter. We can monitor all the desired signals on this platform. Fig. 67 shows a typical GUI used for performing this experiment. Plotter_1, Plotter_2, Plotter_3, Plotter_5 and Plotter_6 show three phase reference currents, three phase voltages and synchronizing signal, three phase line current and three phase reference current verses three phase line current respectively. Main switch is enabled to start activation of the gate pulses given to the three phase bridge MOSFETs. The control algorithm used for implementation is developed in MATLAB/Simulink and downloaded on DSPACE controller explained briefly in next section.

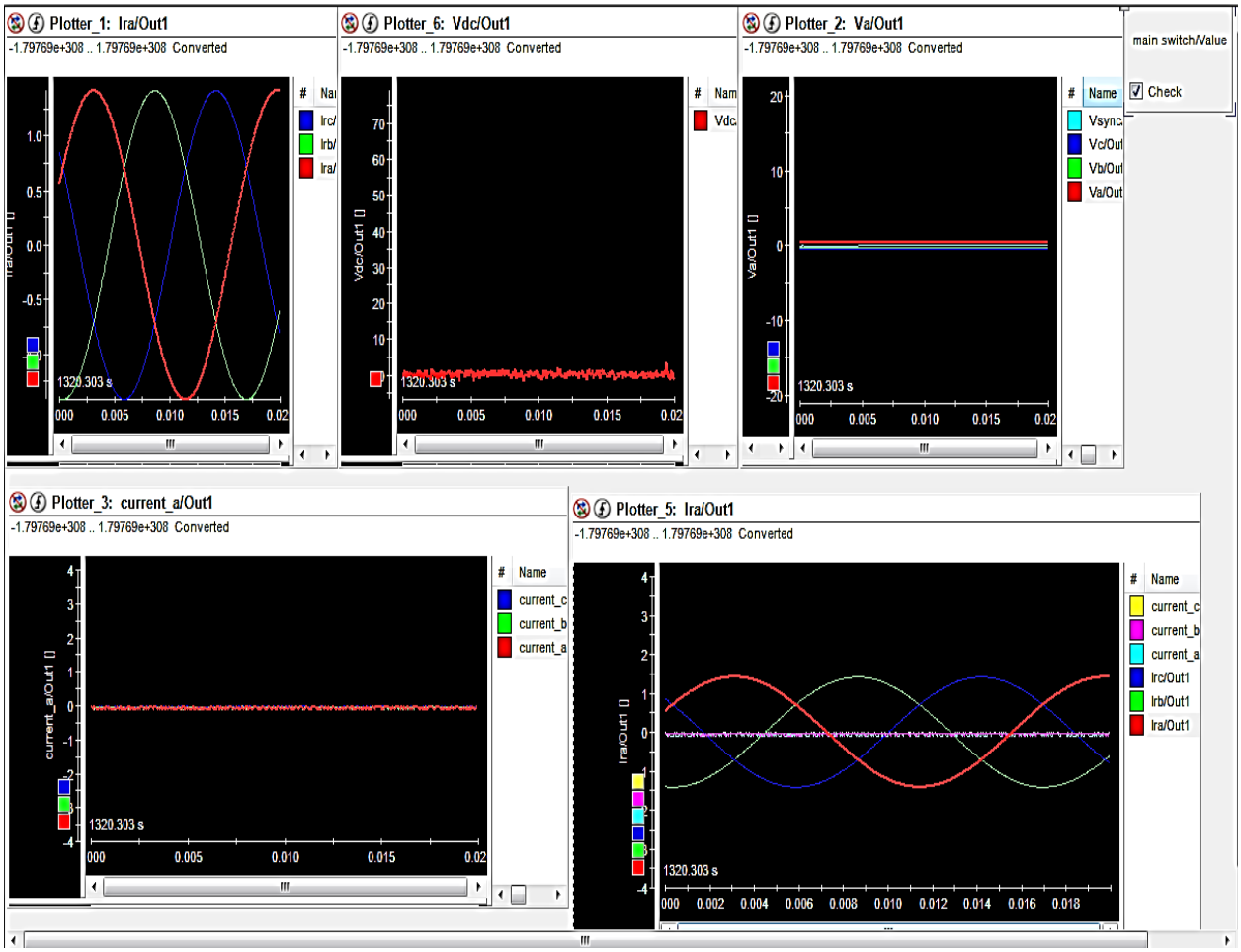
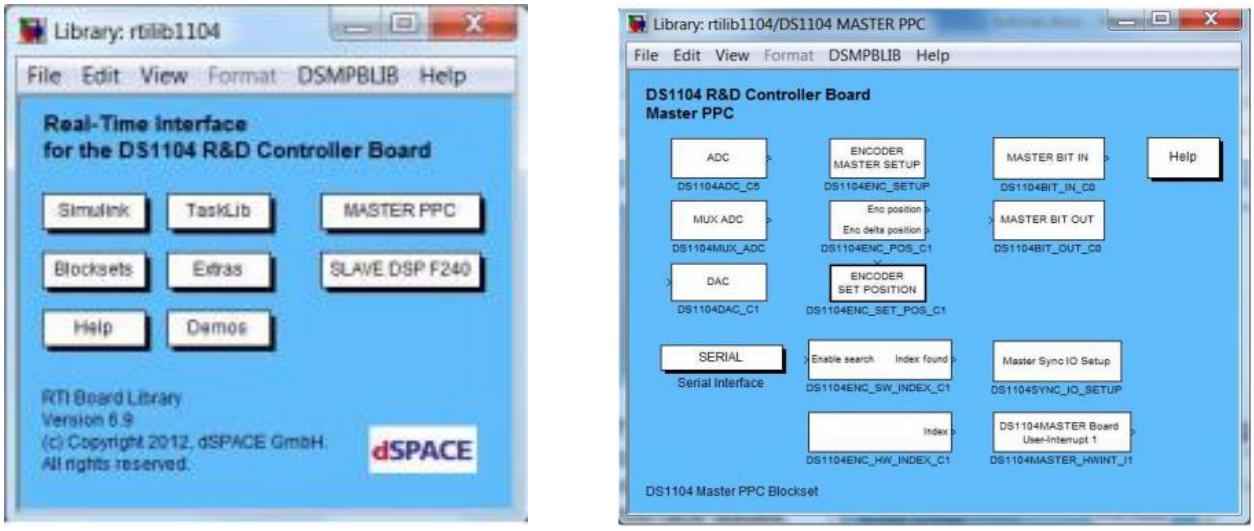


Figure 67: Graphical User Interface screen of the experimental set up on Control desk for Case 1

4.1.4 MATLAB/Simulink Control Algorithm

The DSPACE board DS1104 can be directly programmed from Simulink using the real time interface (RTI) DSPACE block in it. The C code generator Simulink Coder previously known as Real Time Workshop is used for automatic building and implementation of state-flow and control module for real time operation on external devices using DS1104.

All the input and output channels and digital channels can be initialized and programmed through Simulink RTI modules. The Simulink consists of interface modules for DS1104. The modules are shown in Fig. 68. These modules are used to build the whole state-flow algorithm of the experiment in Simulink.



(a) **(b)**

Figure 68: (a) MATLAB/Simulink RTILIBDS1104 blocks for interface between external device and processor DS1104 and (b) MASTER PPC module of the rti1104 blocks used in this experiment

The state-flow diagram is made as a Simulink model. This model is used to generate reference for each case of the experiment, to calculate the hysteresis bandwidth value for the variable bandwidth controller and to generate logic pulses using the controller. Fig. 69 shows the Simulink model used for the experiment. The model uses RTILIBDS1104 library from Simulink. The parallel ADC channels DS1104ADC_C5 to C7 are used for acquiring line current from hardware model. DS1104ADC_C8 is used to acquire output voltage signal across load. The mux ADC channel DS1104ADC_C1 to C4 are used for acquiring three phase source voltage and midpoint voltage of output split capacitors with respect to source neutral. The DAC channels DS1104DAC_C1 to C3 are used to give calculated logic signals to gate driver circuit for switching of MOSFETs. These signals from DSPACE are used to perform switching in order to achieve constant switching frequency. The m-files of Simulink are used to provide initial condition for implementation of the Simulink model and to calculate the bandwidth required for hysteresis controller during operation for constant switching frequency. The m-files used for experimental verification are given in the Appendix (A.5.).

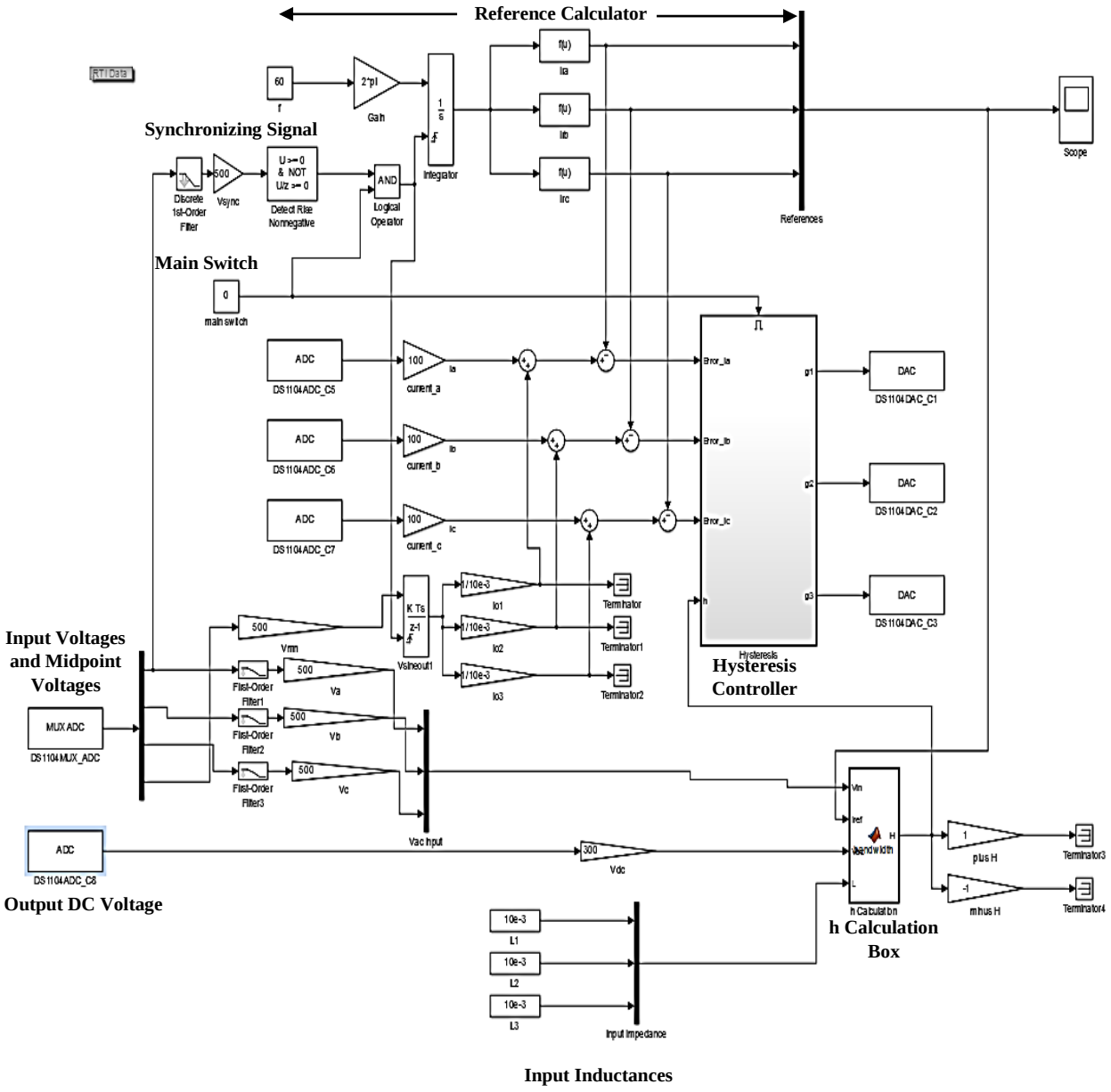


Figure 69: Simulink model for real time implementation for generation of gate pulse

The hysteresis controller used to compare the line current and reference current is same as that of Simulation model. An enable switch is used to activate this controller. The real time implementation of the digital controller is shown in Fig. 70. The enable switch is activated through a main switch. The main switch is also used for synchronization. The signal used for

synchronization is taken from phase '**a**' of the voltage source. The whole experimental set up is shown in function block diagram in Fig. 71.

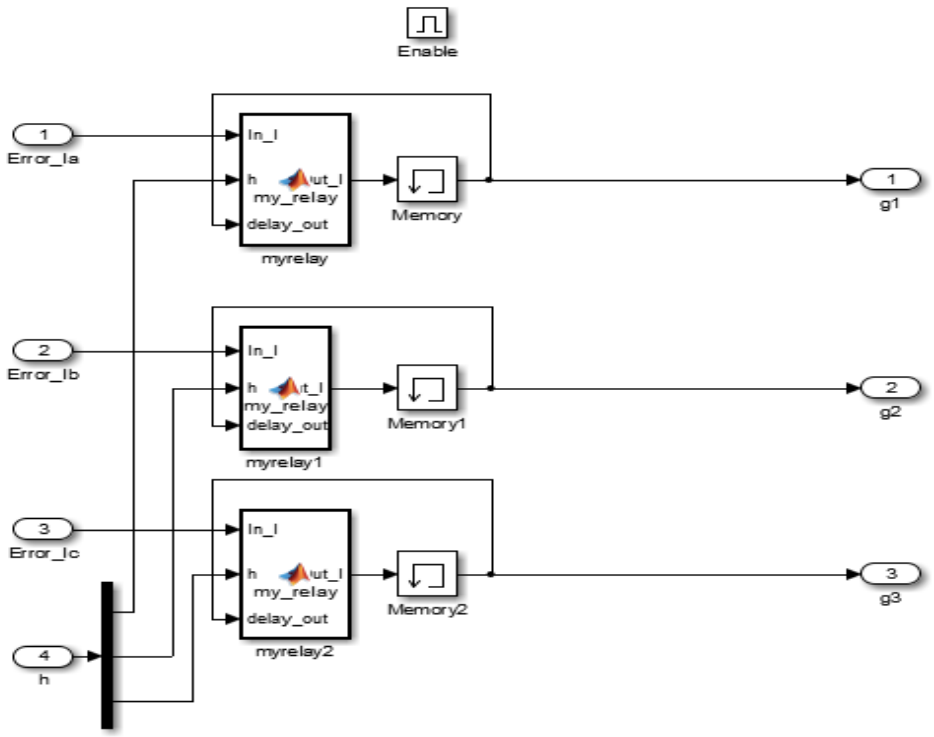


Figure 70: Digital Hysteresis Controller for real time implementation

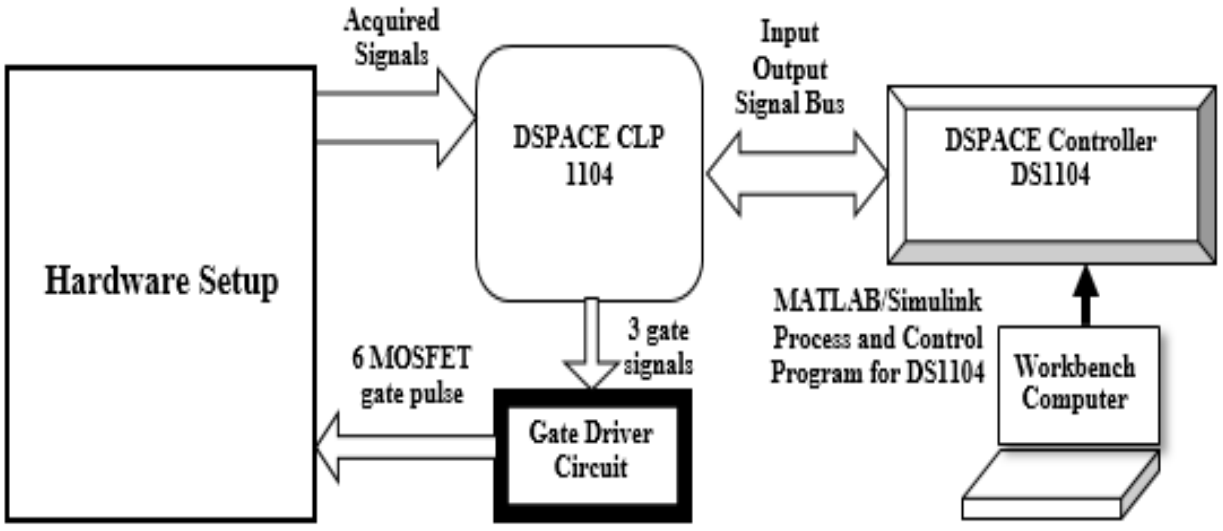


Figure 71: Function block diagram of experimental set-up

The simulation model and the experimental model built for verification have different parameters. This is due to limitation of devices used for the experimental set-up.

It is essential to acquire accurate value of voltage signal between midpoint of DC link capacitors and the source neutral. This signal is used for calculation of neutral current and is responsible for fictitious transformation of delta connected synthesized voltages to star for HCC.

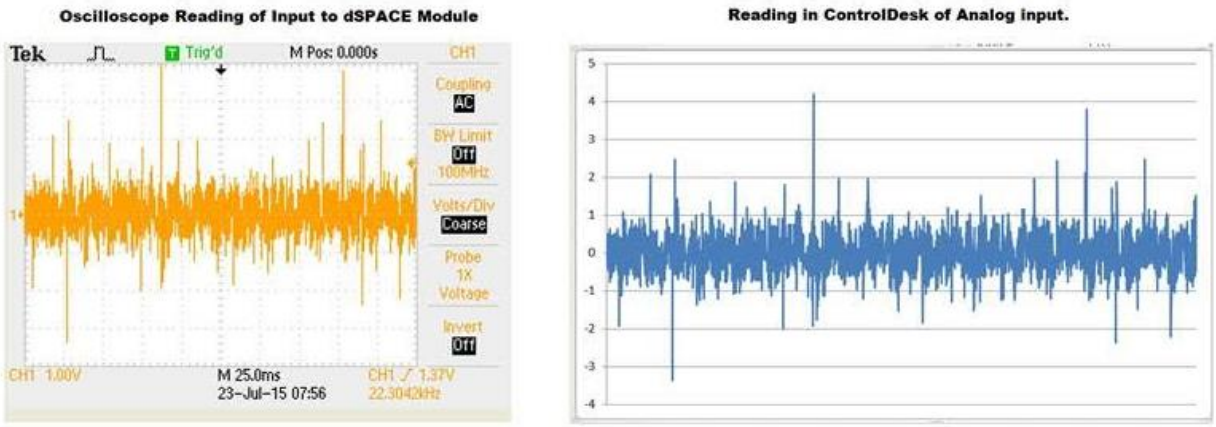


Figure 72: Measured value of voltage difference between the source neutral ***N*** and DC link midpoint ***M***

When, measured this signal is of very small level and has value between 20mV to 40mV and has lot of noise due to switching interaction between phases as shown in Fig. 72. This signal is filtered and amplified to a measured level before it is acquired by DSPASE processor DS1104. This signal is then integrated digitally as shown in Fig. 67. The values of DC link capacitors becomes important, as they must be same in order to measure the correct value of midpoint voltage. Uneven capacitor cannot does not gives correct value at the DC link midpoint of the converter.

4.2 Experimental Results

The Simulation model built for verification of method developed in this thesis has different specification than the experimental model. This is due to current rating of the Lab-volt test bench used and the minimum sampling frequency required for operation in this experiment. The MOSFET Bridge used for experimental set up has maximum current rating of 3 Amperes. The parameters selected for the prototype set up for three phase PWM boost rectifier is given in Table VIII

TABLE VIII: EXPERIMENTAL SETTING

Item #	Parameter Description	Rating
1	Three phase AC voltage	20 V l-n RMS
2	Series Inductor 10mH	10 mH
4	DC Power Supply(Gate Drive Circuit)	15 V
5	Resistive Load	100 Ohms
6	DC link Capacitor (each)	500 uf
7	Operating frequency	60 Hz
8	Sampling Time	40 us

The current and voltage probe setting is provided in Table IX

TABLE IX: PROBE SETTING

Device	Setting
Voltage Isolator	2mV/V
Current Probe	100mV/A
DC Voltage Isolator	33mV/V
Current Probe (Power Quality Analyzer)	1mV/A

The results of this experiment suggest the limitations of the device in use and also explains the condition in which the experimental verification can be carried out successfully. The minimum sampling time that can be used for calculation with DSPACE processor DS1104 is 10 μs. The

maximum ‘turn-around time’ of the program gets compiled from the algorithm built in Simulink as shown in Fig. 67 is 28 μs. Turn-around time of a program includes time required for acquiring of signals and converting it through ADC channels to digital signals, time taken to execute program or algorithm build and time elapsed during conversion of digital signals back to analog through DAC converter. The sample time selected for operation must be greater than the sum of calculation sample time of the processor, the turn-around time of algorithm developed and idle time required by the processor. The idle time of the processor is very small as compared to the sampling time hence can be neglected. When added, the total time required for real time operation is 38 μs. Therefore, the sample time set for operation is 40 μs which is equal to sampling frequency of 25 kHz. This sample frequency is not adequate for achieving constant frequency at pre-set value of 9 kHz. Due to low sampling frequency the precision of digital hysteresis controller reduces. This results in excursion of the line current from the hysteresis bandwidth set for the constant frequency operation.

The results of the experimental set up is verified by the results of operation of similar simulation set up using MATLAB/Simulink model. The sampling frequency used for simulation is same as used in experimental operation. The results includes the plot of input source voltage, plot of line current of each phase with respect to reference set, bandwidth calculated versus error current of phase ‘**a**’, output DC voltage, complex input power, low order Fourier transform (FFT) of phase ‘**a**’ for verifying low order harmonic elimination and high order FFT of phase ‘**a**’ for switching frequency. The experimental results and simulation results are compared under open-loop operation. Since the switching loses of MOSFETs are high hence voltage drop across it and power loss is expected in experimental operation as compared to simulation. Also the FFTs of phase ‘**a**’ for both the models are compared. The error current and bandwidth plot of phase ‘**a**’ is used to show the effect of low sampling frequency on precision of limiting line current in the bandwidth region.

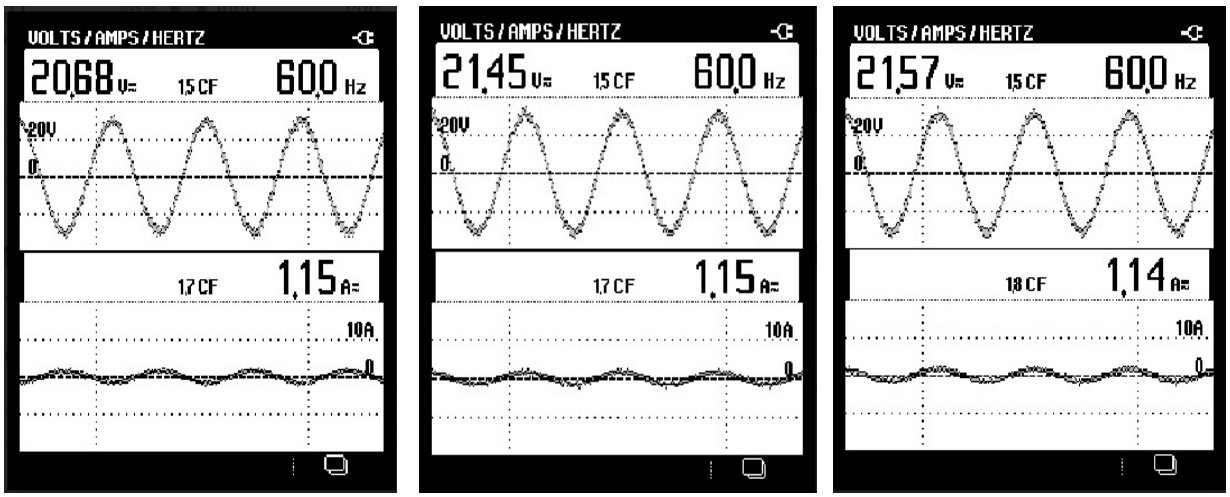
4.2.1 Open-Loop Results

The results of the experiment are verified for only two cases out of the seven cases given in Chapter III. It proves the limitation of the device used for operation in both balanced and unbalanced conditions. The cases for which the results are presented are shown in Table III with the parameters used.

TABLE X: UNBALANCED CASES (EXPERIMENTAL)

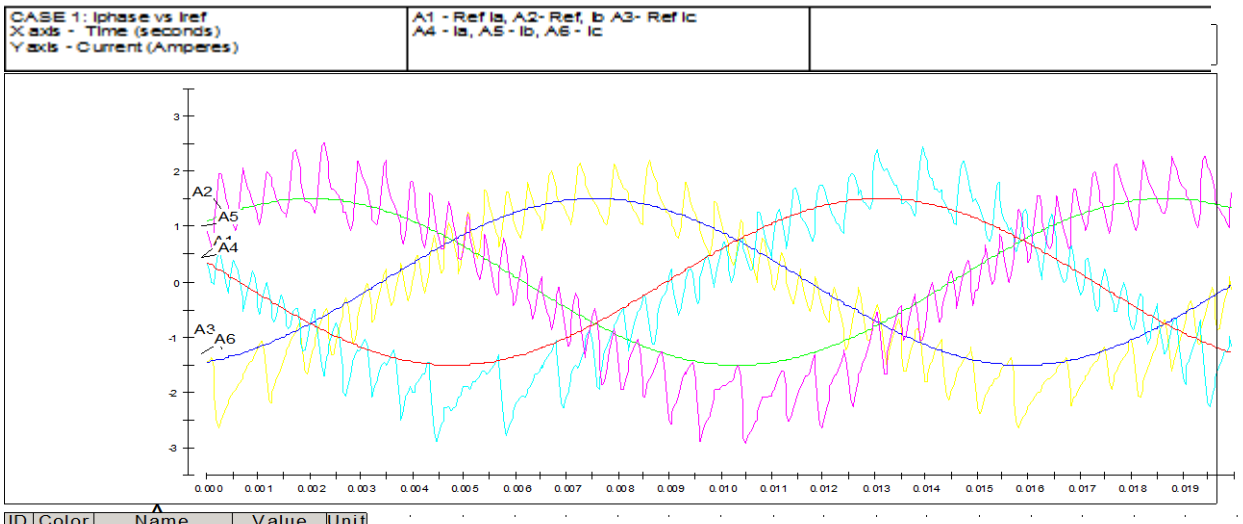
Case #	Input Parameters						Complex Power (VA)	Output Load (Ω)
	Source Voltages (V)			Line Impedances				
	Phase a	Phase b	Phase c	Phase a	Phase b	Phase c		
1	20∠0°	20∠−120°	20∠120°	10mH	10mH	10mH	60	100
3	20∠0°	20∠−120°	0	10mH	10mH	10mH	60	100

The plots for case 1 both experimental and simulation are provided from Fig 73 to Fig 84.



(a) **(b)** **(c)**

Figure 73: Experimental plot of three phase voltage and current plot for experimental set-up (a) Phase '**a**' (b) Phase '**b**' (c) Phase '**c**' for case 1



ID	Color	Name	Value	Unit
A6		current_c/Out1	-1.02539	
A5		current_b/Out1	-1.02539	
A4		current_a/Out1	1.46484	
A3		Irc/Out1	-0.603518	
A2		Irb/Out1	-0.895524	
A1		Ira/Out1	1.49904	

ID	Raster	Platform / Device	Y1	Y2	Y2-Y1	Downsampling	X-Axis Offset
A6	HostService	Platform				[1:1]	0
A5	HostService	Platform				[1:1]	0
A4	HostService	Platform				[1:1]	0
A3	HostService	Platform				[1:1]	0
A2	HostService	Platform				[1:1]	0
A1	HostService	Platform				[1:1]	0

Figure 74.a: Experimental plot for three phase reference current versus line current for case 1

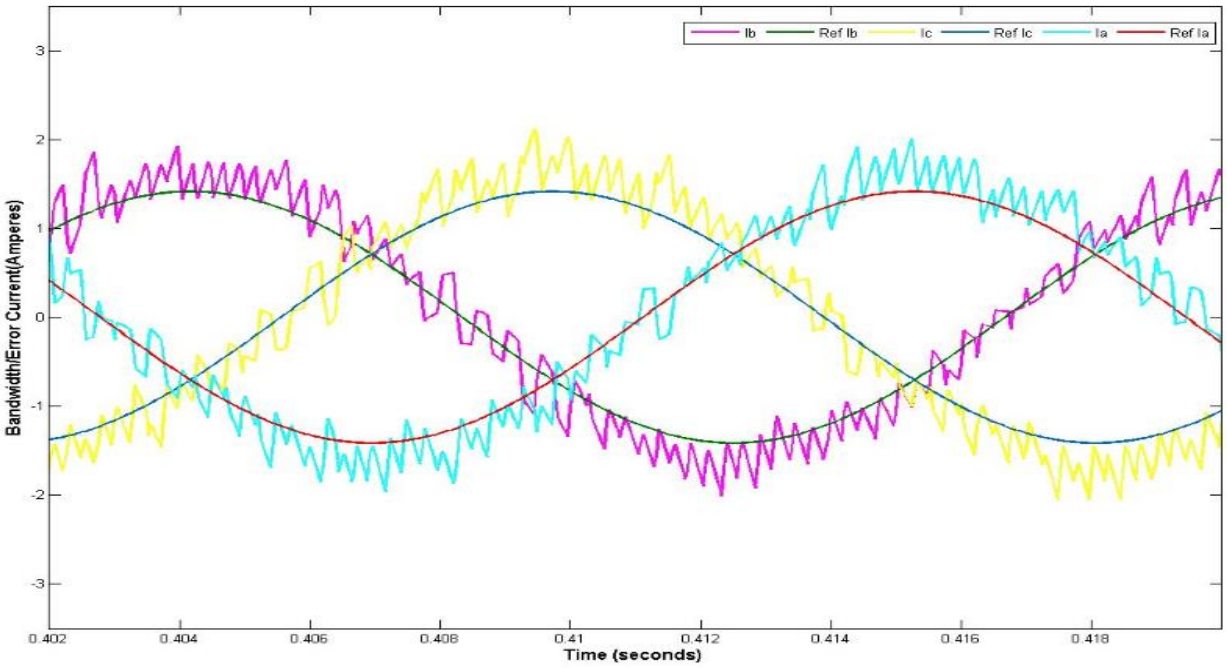
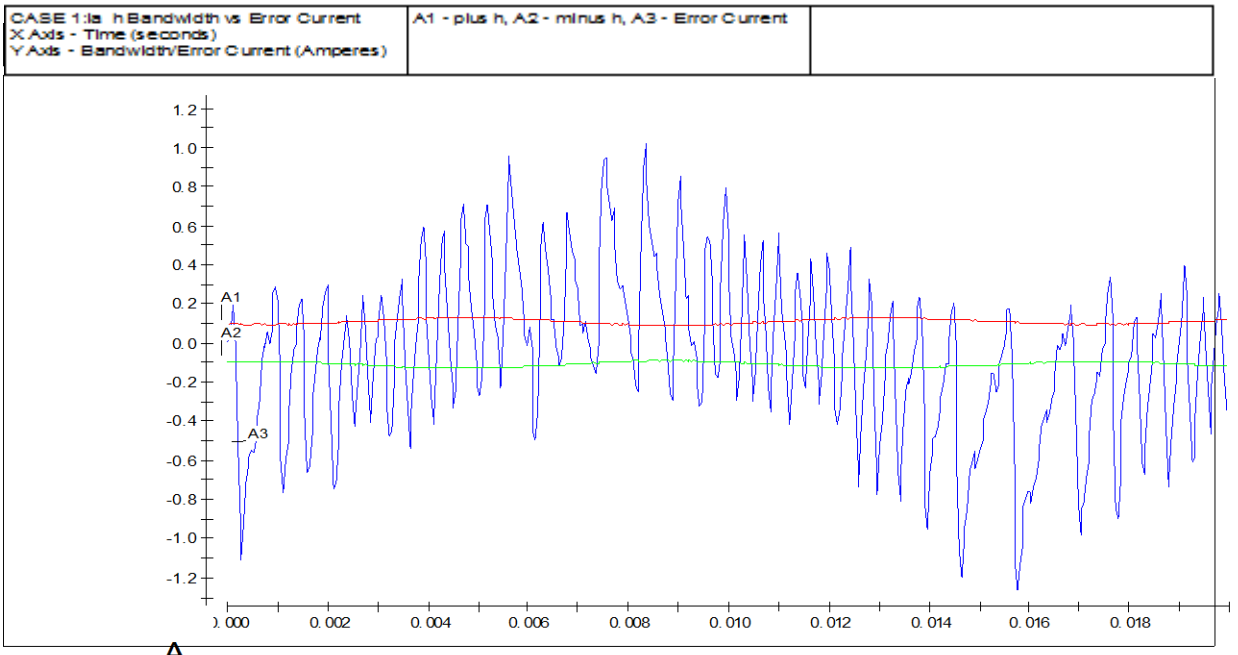


Figure 74.b: Simulation plot for three phase reference current versus line current for case 1



ID	Color	Name	Value	Unit	Raster
A3		Error_Ia/Out1	-0.233031		HostService
A2		Out1[0]	-0.122956		HostService
A1		Out1[0]	0.122956		HostService

ID	Platform / Device	Y1	Y2	Y2-Y1	Downsampling	X-Axis Offset
A3	Platform				[1:1]	0
A2	Platform				[1:1]	0
A1	Platform				[1:1]	0

Figure 75.a: Experimental plot Bandwidth ’h’ and error current for case 1

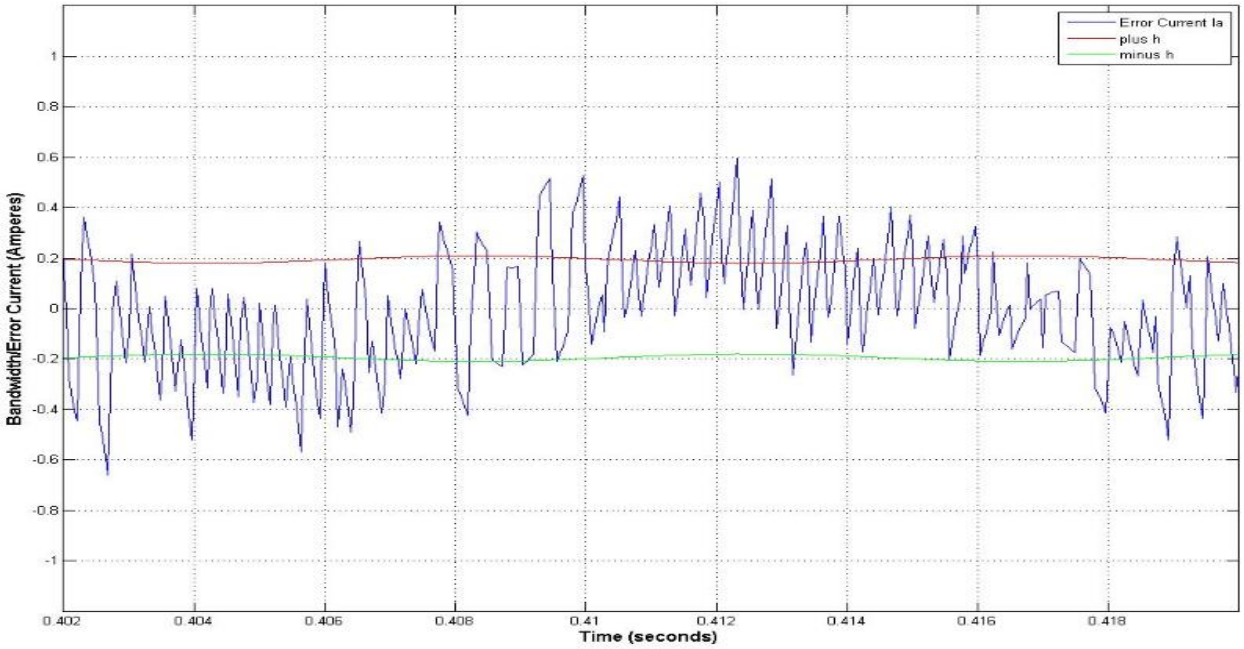


Figure 75.b: Simulation plot Bandwidth ’h’ and error current for case 1

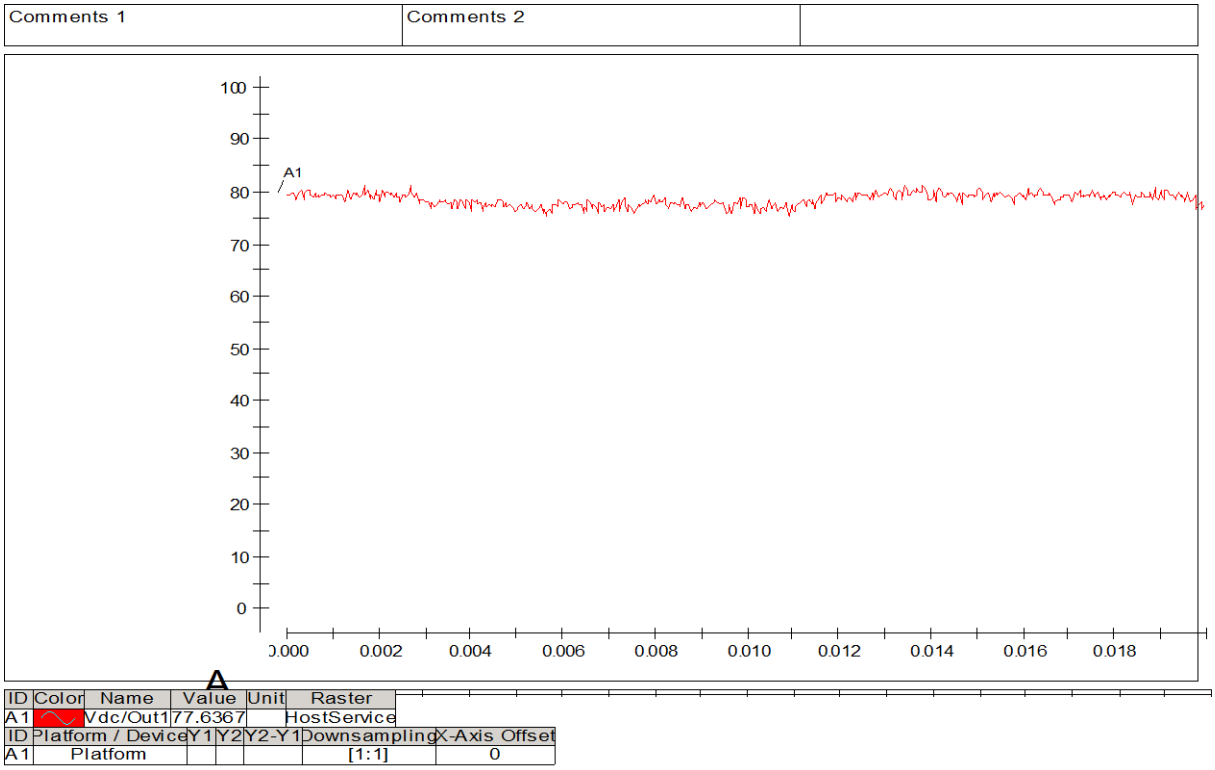


Figure 76.a: Experimental plot output DC voltage for case 1

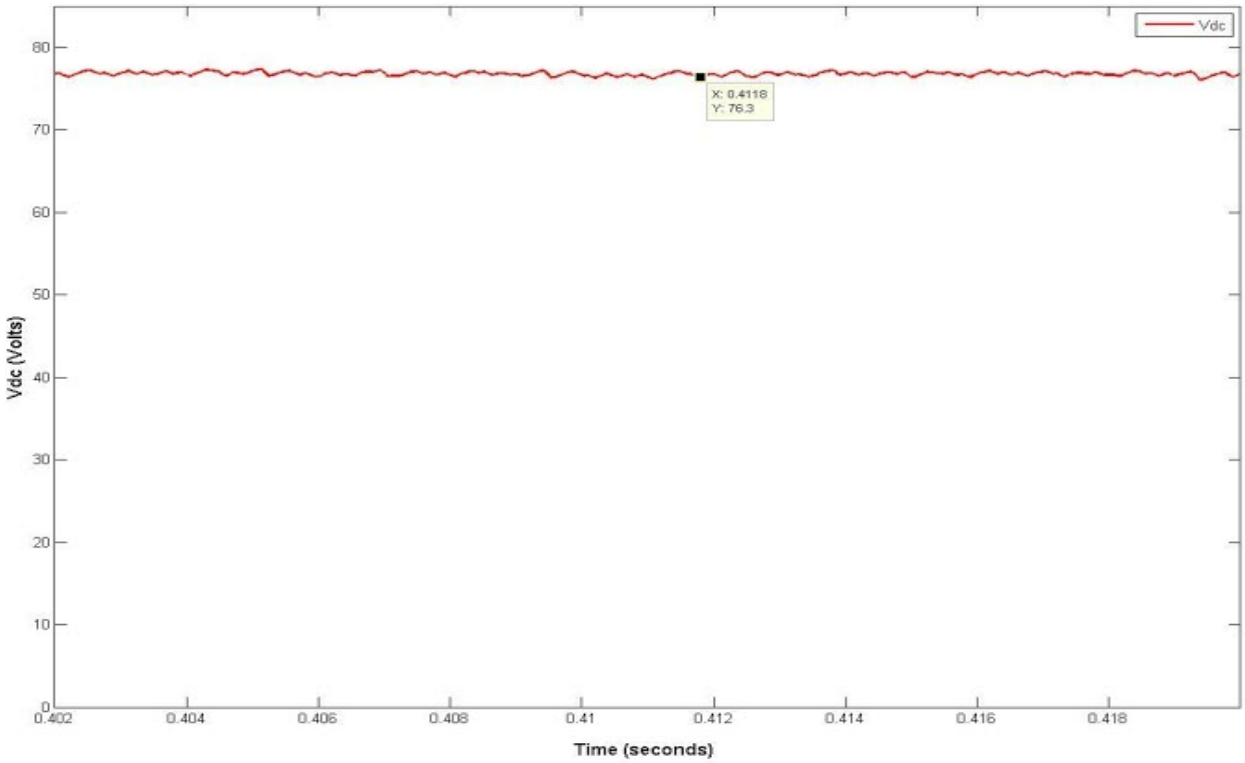
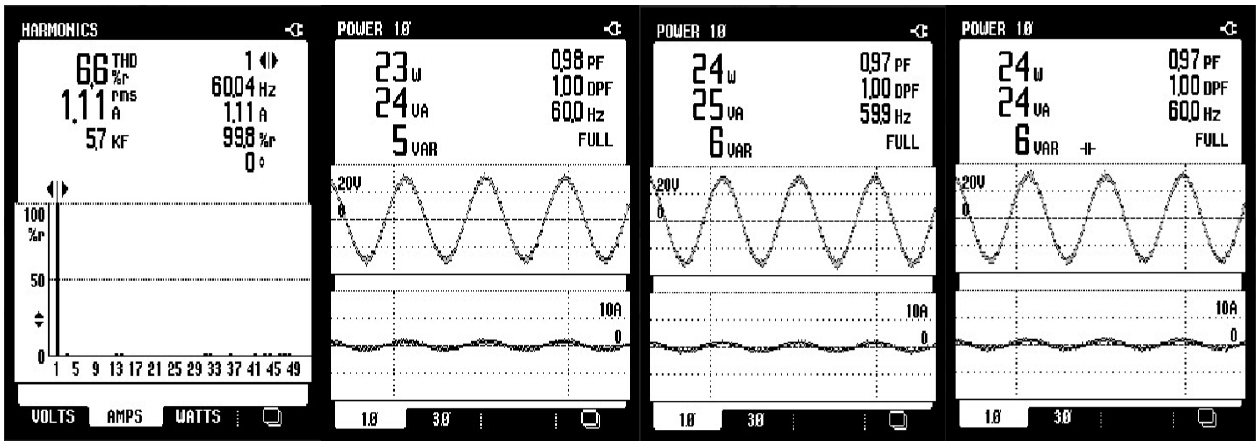


Figure 76.b: Simulation plot output DC voltage for case 1



(a) **(b)** **(c)** **(d)**

Figure 77: Experimental plot of THD of line current phase '**a**' (a), Input complex power of phase '**a**' (b), Input complex power of phase '**b**'(c) and Input complex power of phase '**c**'(d)

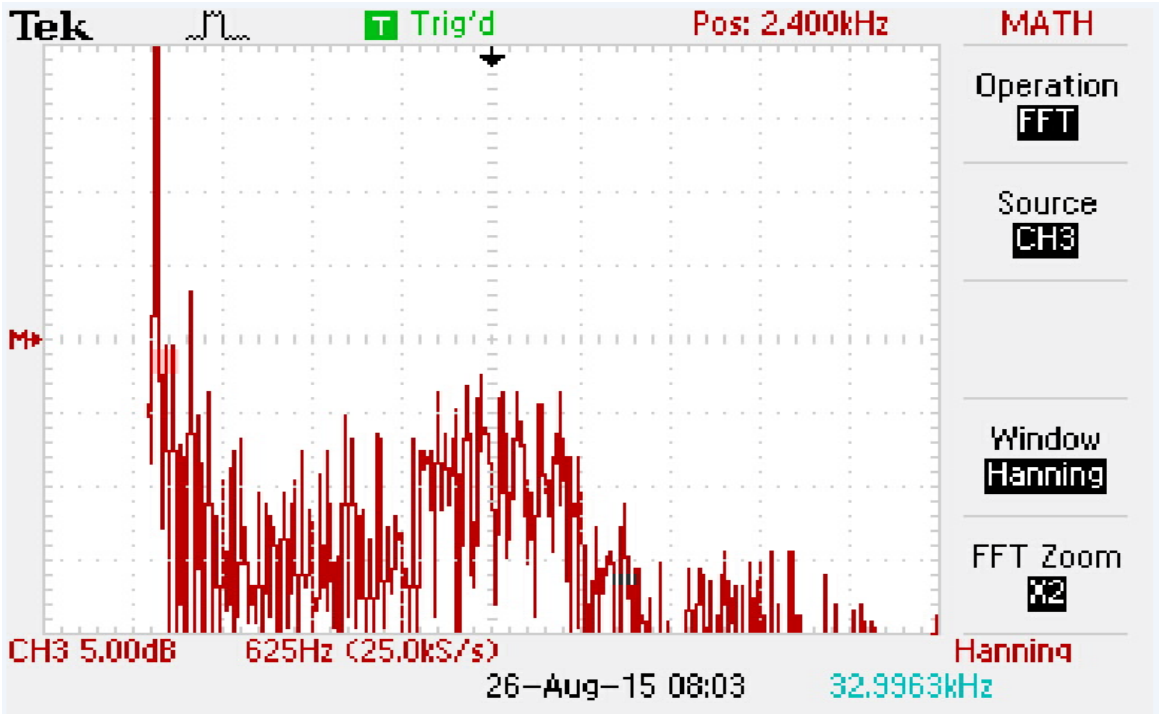


Figure 78.a: Experimental FFT plot of phase '**a**' current for case 1

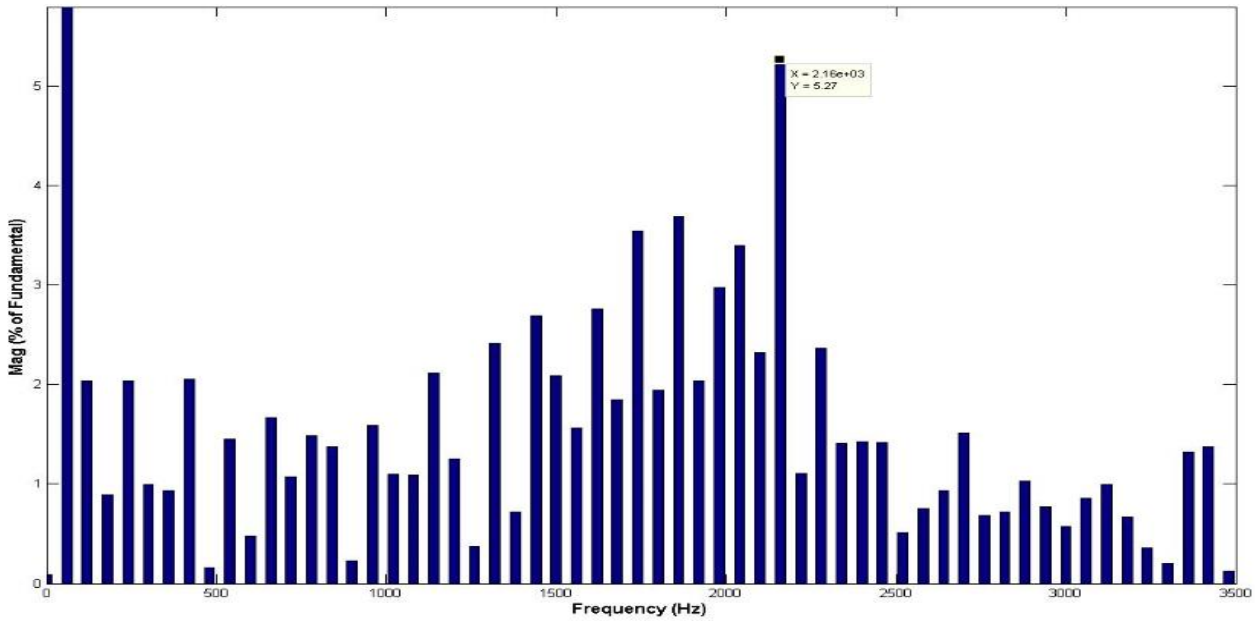
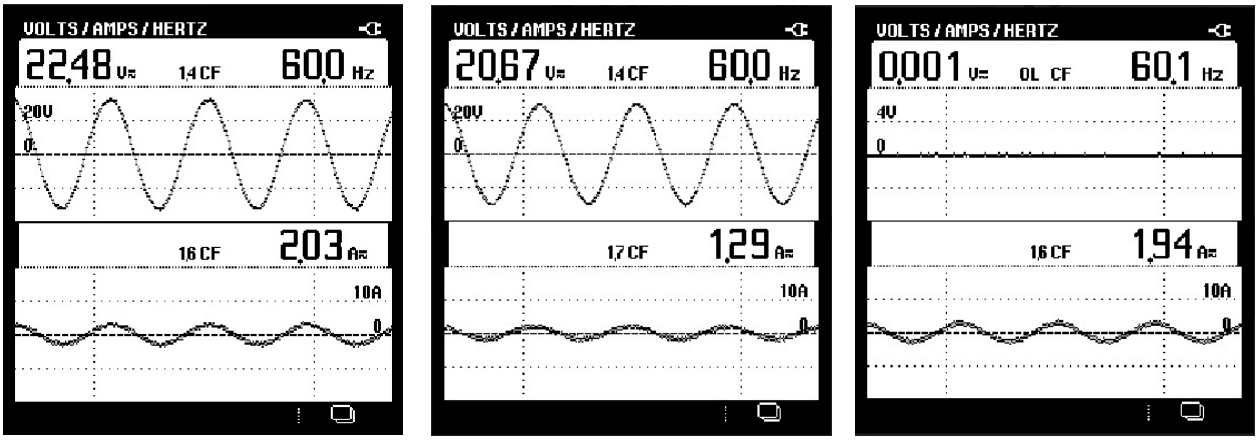


Figure 78.b: Simulation FFT plot of phase '**a**' current for case 1

The above plots for the balanced case show that the sampling frequency used in experimental set up is not suitable for implementing constant switching frequency at the pre-set value. The reading of Fig. 73 and Fig. 77 are taken from Power Quality Analyzer. The experimental plots from Fig 74 to Fig. 76 are taken from Control desk next generation GUI and all the values are instantaneous in nature. In Fig. 73.a and Fig. 73.b it is clearly seen the line current is not limited between the bandwidth set up. Hence, FFT plots of phase '**a**' is not at 9 kHz as shown in Fig. 78.a and Fig. 78.b. above. However, the switching frequency of the converter for both simulation and experimental are nearly of same value.

A similar analysis is done for an unbalanced condition (case 3). One of the voltage source is held at neutral voltage in experimental set up to make this unbalanced condition. Results of the experimental operation and simulation is provided from Fig. 79 to Fig 75.



(a) **(b)** **(c)**

Figure 79: Experimental plot of three phase voltage and current plot for experimental set-up (a) Phase '**a**' (b) Phase '**b**' (c) Phase '**c**' for case 3

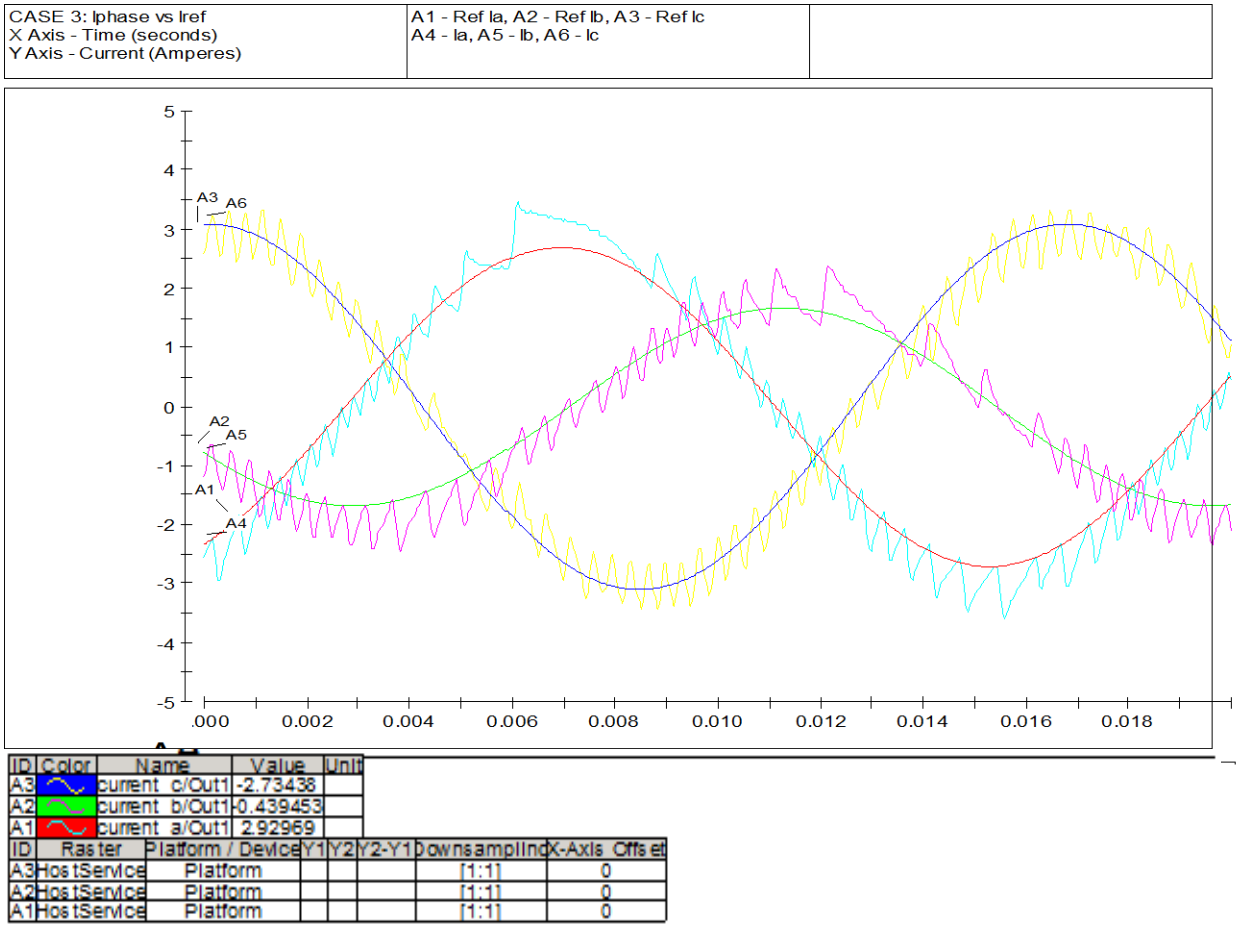


Figure 80.a: Experimental plot of three phase reference current versus line current for case 3

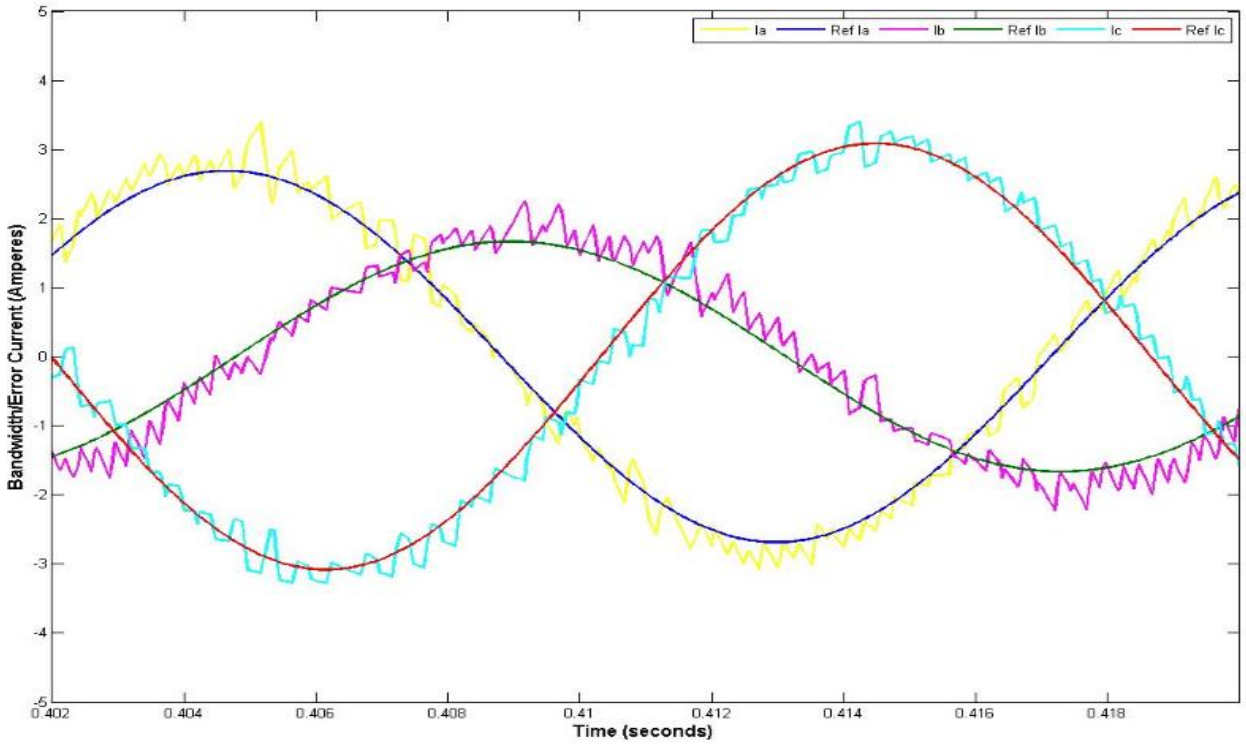
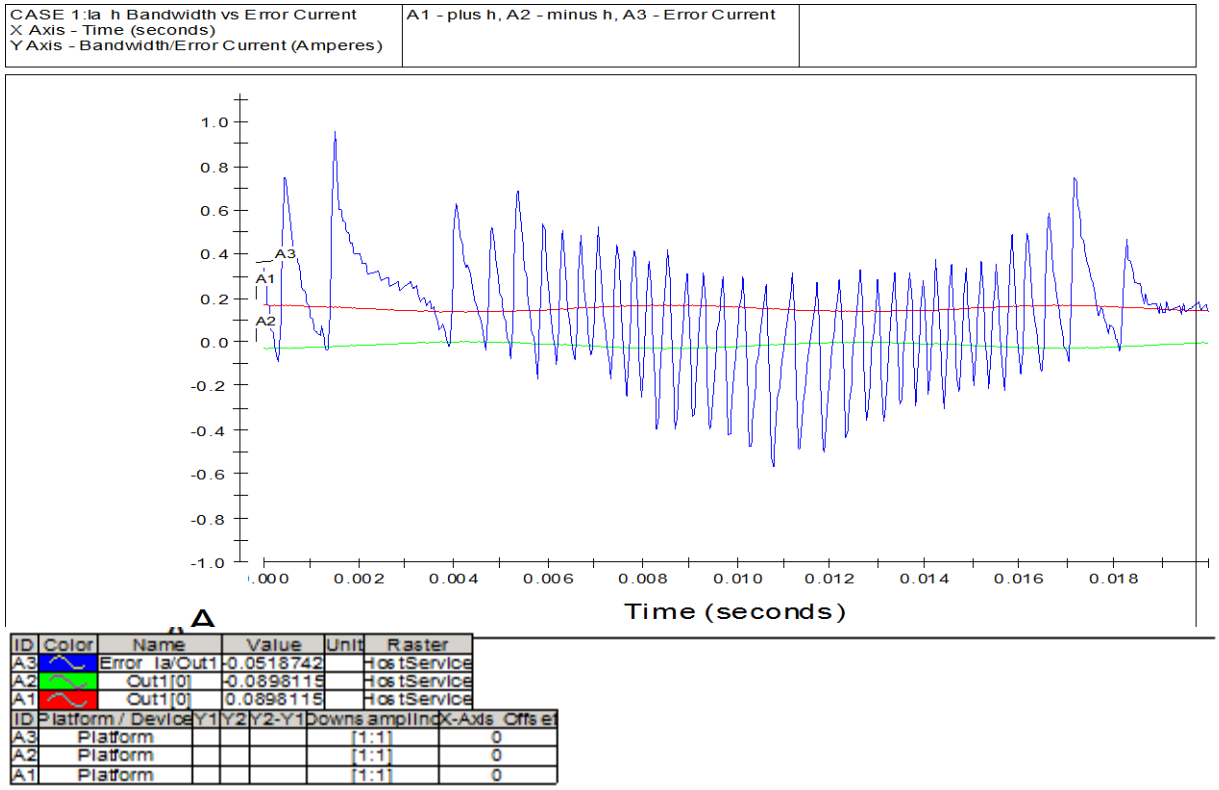


Figure 80.b: Simulation plot of three phase reference current versus line current for case 3



ID	Color	Name	Value	Unit	Raster
A3		Error Ia/Out1	-0.0518742		HostService
A2		Out1[0]	-0.0898115		HostService
A1		Out1[0]	0.0898115		HostService

ID	Platform / Device	Y1	Y2	Y2-Y1	Downsampling	X-Axis Offset
A3	Platform				[1:1]	0
A2	Platform				[1:1]	0
A1	Platform				[1:1]	0

Figure 81.a: Experimental plot of Bandwidth 'h' and error current for case 3

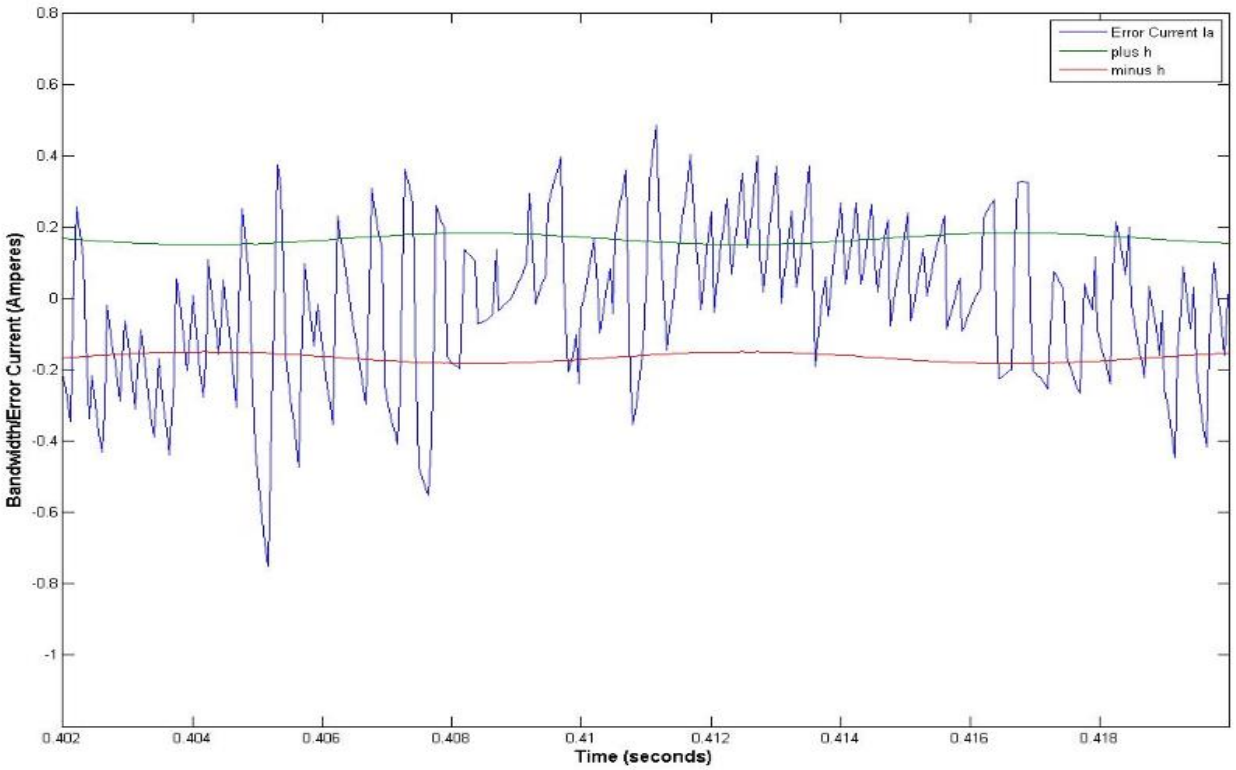


Figure 81.b: Simulation plot of Bandwidth 'h' and error current for case 1

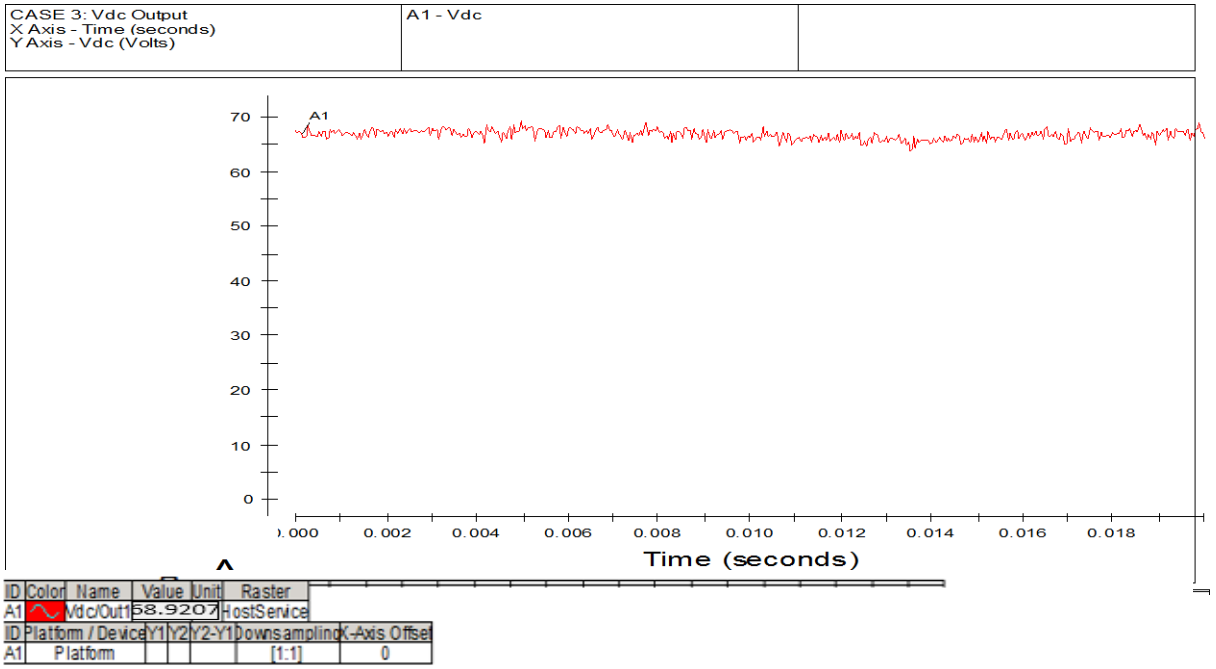


Figure 82.a: Experimental plot of output voltage V_{dc} for case 3

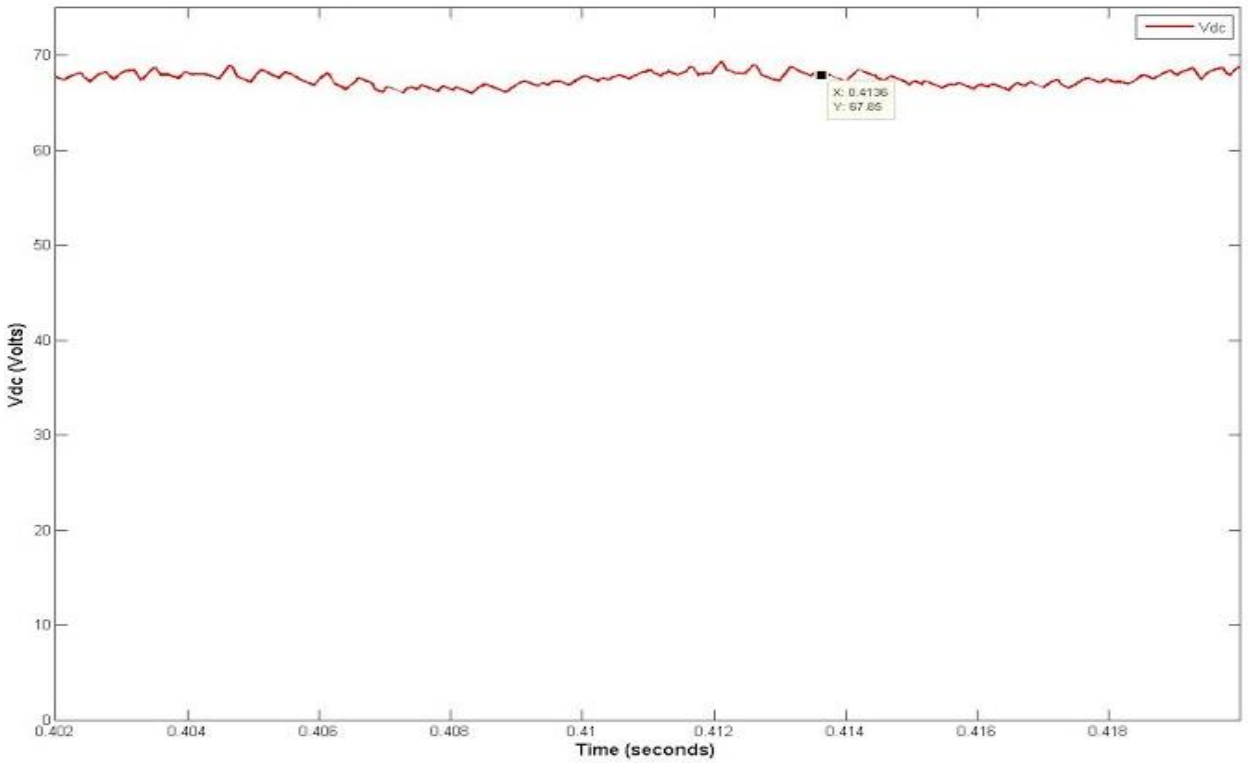
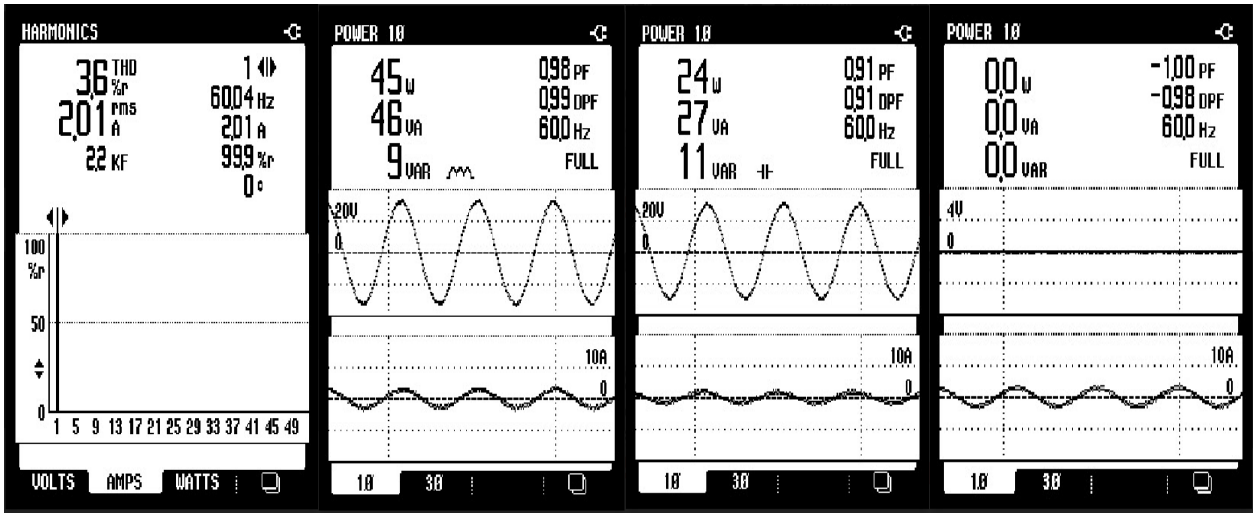


Figure 82.b: Simulation plot of output voltage V_{dc} for case 3



(a) **(b)** **(c)** **(d)**

Figure 83: Experimental plot of THD of line current phase '**a**' (a), Input complex power of phase '**a**' (b), Input complex power of phase '**b**'(c) and Input complex power of phase '**c**'(d)

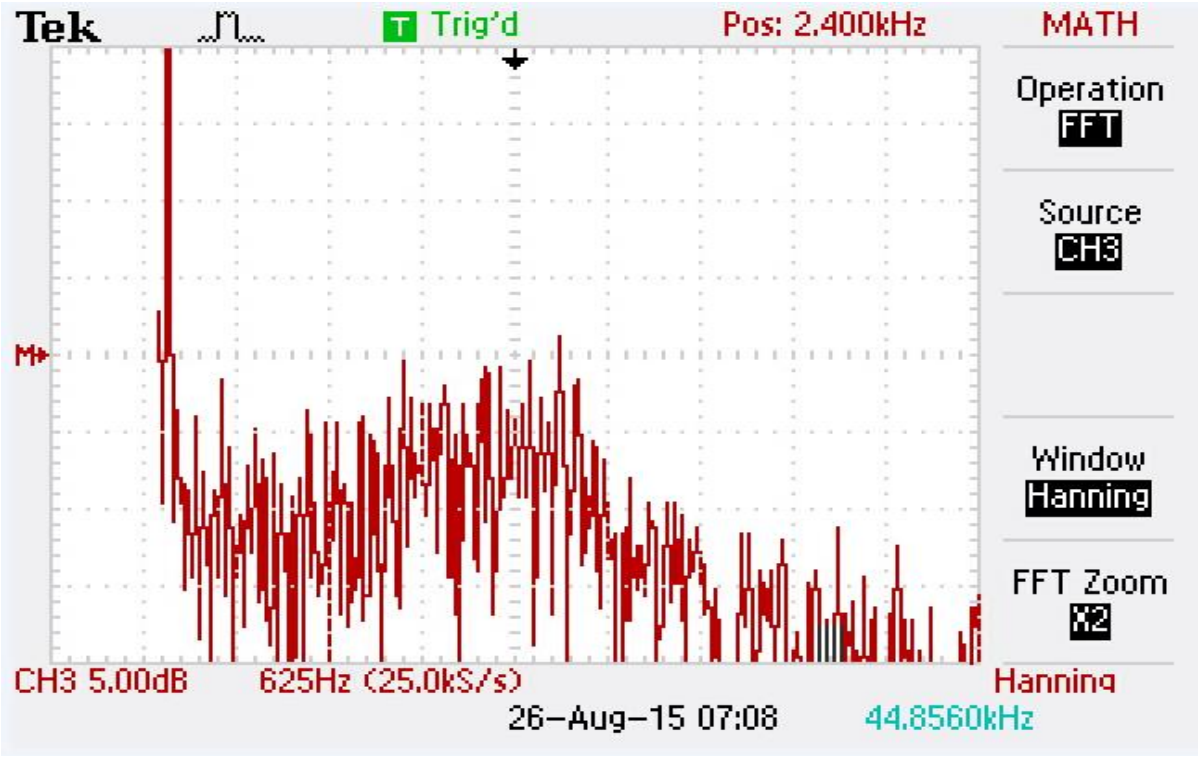


Figure 84.a: Experimental FFT plot of phase '**a**' current for case 3

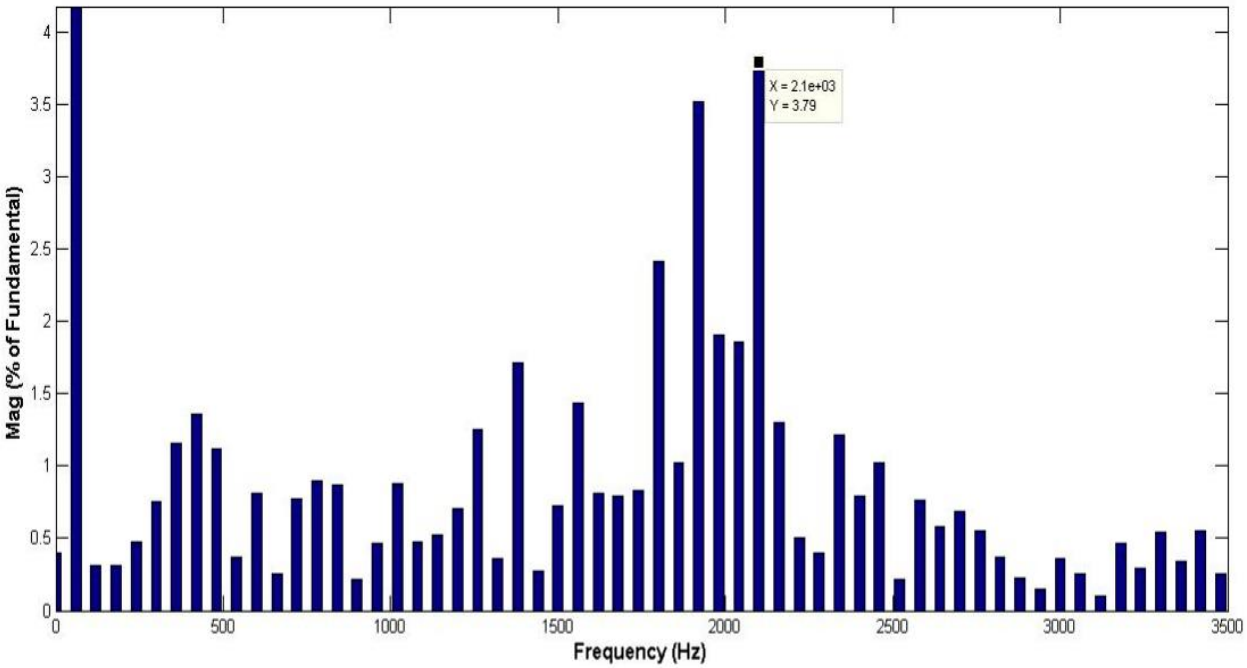


Figure 84.b: Simulation FFT plot of phase '**a**' current for case 3

The results obtained from unbalanced condition for experimental and simulation set up has similar results. Table XI compares the experimental results with equivalent simulation set up for three phase input currents, output DC voltage and total harmonic distortion (THD) of phase '**a**'. All the values of experimental set up and equivalent Simulink model are consistent.

TABLE XI: RESULT SUMMARY

Case #	Simulation Currents (RMS)			Experimental Currents(RMS)			Output		THD of Phase a (%)	
	Phase a (A)	Phase b (A)	Phase c (A)	Phase a (A)	Phase b (A)	Phase c (A)	Simulation DC output (V)	Experimental DC Output (V)	Simulation	Experimental
1	1.166	1.17	1.163	1.15	1.15	1.14	76.30	77.64	11.32	6.6
3	2.008	1.311	2.214	2.03	1.29	1.94	67.85	68.92	9.70	3.6

Also in Table XII comparison of three phase input power and output power is done. The Simulink model set up in this experiment uses MOSFETs as their switching device. The drop of efficiency in both experimental and simulation model is due to switching losses of MOSFETs. The drop of efficiency from case 1 to case 3 due to sudden increase in level of input currents. During extreme unbalance condition in voltage the efficiency of converter decreases.

TABLE XII: POWER AND EFFICIENCY SUMMARY

Case #	Experimental			Simulation			Experimental		Simulation		Experimental	Simulation
	Input						Output				Efficiency (%)	Efficiency (%)
	Active (W)	Reactive (VAR)	Power factor	Active (W)	Reactive (VAR)	Power factor	Power (W)	DC link Voltage (V)	Power (W)	DC link Voltage (V)		
1	71.00	5.00	1.00	64.79	1.6030	1.00	60.28	77.64	58.22	76.30	84.90	89.85
3	69.00	2.00	1.00	64.82	1.5800	1.00	47.50	68.92	46.04	67.85	68.84	71.02

The converter operates at unity power factor for both experimental and simulation model. The simulation model has higher current rms values than the experimental set-up, which results in higher THD values in simulation than that of experimental model.

4.2.2 Result Analysis

The experimental results from Lab-volt test bench along with DSPACE real time implementation when compared to equivalent Simulation set-up in MATLAB/Simulink explains the limitation of the experimental verification. The steady state Fourier analysis of both results are comparable. It is observed that with operating sampling frequency at 25 kHz the line current of the three phases cannot be limited within the boundaries of hysteresis controller bandwidth. The Fourier analysis for both the case suggests the operation of shifts from preset value of 9 kHz to around 2.16 kHz for simulation and 2.4 k Hz for experimental set-up which is not desirable.

Hence, it proves the requirement of higher frequency processor is required to achieve the desired constant switching frequency at 9 kHz. Since, all other parameter have consistent performance it can be inferred that a constant switching frequency shall be achieved if input line currents of three phase can be restricted between the calculated hysteresis bandwidth.

Chapter V

CONCLUSION AND FUTURE WORK

5.1. Conclusion

The thesis presents a generalized solution for achieving near constant switching frequency under extremely unbalanced condition. Three steps used for the proposed solution are listed as follows.

1. Reference current is calculated for input-output harmonic elimination under extremely unbalanced condition
2. Bandwidth of variable hysteresis is calculated by grounding the midpoint of the DC link capacitor
3. The bandwidth calculated for the grounded midpoint of the DC link capacitor is then extended to floating condition using neutral current addition in current controller

The previous work on unbalanced operation of the three phase boost type rectifiers has presented a generalized solution for elimination of harmonics under extremely unbalanced conditions without constant switching frequency operation. Whereas, solutions having constant switching frequency operation with power factor control is achieved only for balanced condition. Unlike previous works, this thesis presents a simple successful generalized solution for constant switching frequency under extremely unbalanced condition. The proposed solution is verified on all cases of extreme unbalance conditions in input voltages and input impedances successfully in simulation.

The relevant plots are presented for the new variable bandwidth hysteresis controller proposed in this thesis which results in near constant switching frequency and results are compared with the conventional hysteresis controller. The output results of simulation are presented for both closed loop and open loop and closed loop operation. This proves the feasibility of the proposed solution.

The experimental set-up for the solution is built successfully. The output of the experimental operation shows the relevance of high speed processor to be used for implementing the current controller. The simulation parameter set up according to experimental equivalent gives similar results. It is concluded that a calculation sampling frequency of DSPACE DS1104 processor which is around 38μs is not enough for precise implementation of digital hysteresis controller. It results in excursion of line current from the set calculated bandwidth required for achieving constant switching frequency. The value of output voltage, input line current, input power factor and total harmonic distortion for both experimental set-up and its equivalent simulation model are comparable.

The method developed has some constraints which are also discussed. The validity of the method is only when following requirements are fulfilled by the system:

1. The value of input impedance when in unbalanced condition never has zero value.
2. The switching function used is always less than or equal to one for practical operation of the boost rectifier.
3. The value of input voltage and input impedance for the same phase is never equal to zero at same instance.

The PWM boost type rectifier operating at near constant switching frequency is compared with the conventional hysteresis controller has the total harmonic distortion of the line current for each phases in the case of former is more than the latter. This is an expected behavior due to sinusoidal nature of hysteresis band. The value of the band accommodates higher values error current to maintain switching frequency constant and all these harmonics are present at a single preset value which is significant.

5.2. Future work

A successful experimental verification is eminent to prove the practical solution of the proposed method. As the inadequate calculation frequency of the DSP controller DS1104 is concluded in the above section, a high frequency comparator is required to eliminate excursion of line current from the set bandwidth. This is essential to achieve constant switching frequency. Hence, a complete practical implementation of this thesis can be done by using different high frequency controller for precise comparison reference current and star type line current as done in [26]

Recent progress done in model predictive hysteresis controller in [30] and [31] shows excellent results with lower frequency comparator than used in conventional live comparator which requires high frequency comparison. A model is developed to predict the hysteresis bandwidth of next switching state which is compared with the present state bandwidth using PLL loop to find the error in bandwidth in the present state. The error in bandwidth is then processed through PI controller to make the predictive model accurate. This not only reduces the requirement of high speed comparator but also increases the transient response of the current controller.

This method is a generalized way and should be tested on other various topologies of the three phase PWM boost converter system by using a variable hysteresis band controller to achieve constant switching frequency. In [32] a method to achieve constant switching frequency without a bandwidth control is shown.

As the present study is steady state analysis of the PWM boost rectifier under unbalanced operation to achieve constant switching frequency, it is desired to investigate the dynamic response of the system.

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APPENDIX

A. MATLAB programs

A.1. Program for Reference Current Calculation for Harmonic Elimination (Gives initial conditions)

```
clc
clear
%% Variable Initialization
Ts=0.00002;                              % Switching frequency (Hertz)

%Define the sytem voltages
V1=60;                                   % Phase a voltage (Volts)
V2=60*(cos(-2*pi/3)+j*sin(-2*pi/3));     % Phase b voltage (Volts)
%V2=0;                                   % Phase b Unbalanced voltage (Volts)
V3=60*(cos(2*pi/3)+j*sin(2*pi/3));       % Phase c voltage (Volts)
%V3=0;                                   % Phase c Unbalanced voltage (Volts)

% Define system frequency
f=60;                                    % Line frequency (Hertz)

%Define the system impedances
z1=2*pi*f*0.01j-0.000001j;               % Phase a impedance (Ohms)
%z1=0;                                   % Phase a Unbalanced Impedence (Ohms)
z2=2*pi*f*0.01j;                         % Phase b impedance (Ohms)
%z2=2*pi*f*0.001j;                        % Phase b Unbalanced Impedance (Ohms)
z3=2*pi*f*0.01j+0.000001j;               % Phase c impedance (Ohms)
%z3=0;                                   % Phase c Unbalanced Impedance (Ohms)

%Define the power
S=250;                                   % System Power (VA)

%Giving the initial condition
I=zeros(1,3);                            % Initial value of Current (Amperes)

%% Calculation of three phase reference current
Vc1=conj(V1);                            % Conjugate of V1 (Volts)
Vc2=conj(V2);                            % Conjugate of V2 (Volts)
Vc3=conj(V3);                            % Conjugate of V3 (Volts)
Sc=conj(S);                              % Conjugate of Power (VA)

% Coefficients of quadratic equation
a=((2*z1*(Vc3-Vc1)/(Vc2-Vc1))-((z1+z2)*(Vc3-Vc1)^2/(Vc2-Vc1)^2)-(z1+z3));
b=((V3-V1)-(Vc3-Vc1)*(V2-V1)/(Vc2-Vc1))-(2*z1*Sc/(Vc2-
Vc1))+(2*Sc*(z1+z2)*(Vc3-Vc1)/(Vc2-Vc1)^2);
c=(Sc*(V2-V1)/(Vc2-Vc1))-((z1+z2)*Sc^2/(Vc2-Vc1)^2);


I(3)=(-b-sqrt(b^2-4*a*c))/(2*a);         % reference current phase a (Amperes)
I(2)=(Sc-I(3)*(Vc3-Vc1))/(Vc2-Vc1);      % reference current phase b (Amperes)
I(1)=-I(2)-I(3);                         % reference current phase c (Amperes)

%% Check phase sequence of the reference currents
```

```
if angle(I(3))< angle(I(1))|| angle(I(2))> angle(I(1))
   I(3)=(-b+sqrt(b^2-4*a*c))/(2*a);
   I(2)=(Sc-I(3)*(Vc3-Vc1))/(Vc2-Vc1);
   I(1)=-I(2)-I(3);
end

%% Solve for the reference current for simulation circuit
%I
IM=abs(I)*sqrt(2);                    % Current Magnitude (Amperes)
IA=angle(I);                          % Current Angle (Radians)
```

A.2. Program for Online Hysteresis Bandwidth Calculation

```
function H = bandwidth(Vin,Iin,Vdc,L)
%% Calculating h in Matlab
% Initialization of the inputs required for calculation
% Vin, Iin, Vdc, L
%% calculating absolute value of Vin and Iin
AbsVin = abs(Vin);                % Absolute value of input voltages
AbsIin = abs(Iin);                % Absolute value of reference currents
dAbsIin = [diff(AbsIin);0];       % Differentiating reference currents
a = L.*dAbsIin;                   % Intermediate variable a
b = AbsVin-a;                     % Intermediate variable b
Num = Vdc/2.*Vdc/2 -b.*b;         % Numerator calculation
Den = 2*9e3*L*Vdc;                % Denominator with switching frequency fs =
9kHz
H = Num./Den;                     % Calculation of bandwidth
```

A.3. Program for Variable Hysteresis Current Controller for Block ‘myrelay’

```
%% Defining Input for the controller
% In_I= error current from comparator; h = hysteresis bandwidth
% delay_out = previous state
function Out_I = my_relay(In_I, h,delay_out)

if In_I >= h                  % when error current >or= h
    Out_I = 1;                % output of controller = ON

elseif In_I <= -h             % when error current <or= -h
    Out_I = 0;                % output of controller = OFF

else
    Out_I = delay_out;        % when error current between h and -h Output of
controller = previous state
end
```

A.4. Program for Online Reference Calculation for Block 'Online Reference Calculator'

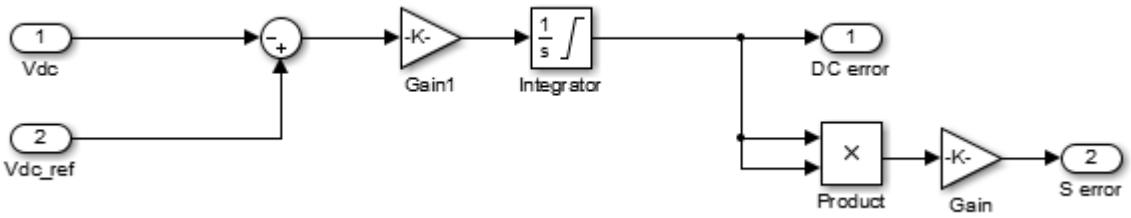
```
function [IM,IA]= fcn(S)
%#codegen
%% Variable Initialization
Ts=0.00002;                              % Switching frequency (Hertz)
%Define the sytem voltages
V1=60;                                   % Phase a voltage (Volts)
V2=60*(cos(-2*pi/3)+j*sin(-2*pi/3));     % Phase b voltage (Volts)
%V2=0;                                   % Phase b Unbalanced voltage (Volts)
V3=60*(cos(2*pi/3)+j*sin(2*pi/3));       % Phase c voltage (Volts)
%V3=0;                                   % Phase c Unbalanced voltage (Volts)

% Define system frequency
f=60;                                    % Line frequency (Hertz)

%Define the system impedances
z1=2*pi*f*0.01j-0.000001j;               % Phase a impedance (Ohms)
%z1=0;                                   % Phase a Unbalanced Impedence (Ohms)
z2=2*pi*f*0.001j;                        % Phase b impedance (Ohms)
%z2=0;                                   % Phase b Unbalanced Impedance (Ohms)
z3=2*pi*f*0.01j+0.000001j;               % Phase c impedance (Ohms)
%z3=0;                                   % Phase c Unbalanced Impedance (Ohms)

%Giving the initial condition
I=zeros(1,3)+ j*zeros(1,3);              % Initial value of Current (Amperes)

%% Calculation of three phase reference current
Vc1=conj(V1);                            % Conjugate of V1 (Volts)
Vc2=conj(V2);                            % Conjugate of V2 (Volts)
Vc3=conj(V3);                            % Conjugate of V3 (Volts)
Sc=conj(S);                              % Conjugate of Power (VA)

% Coefficients of quadratic equation
a=((2*z1*(Vc3-Vc1)/(Vc2-Vc1))-((z1+z2)*(Vc3-Vc1)^2/(Vc2-Vc1)^2)-(z1+z3));
b=((V3-V1)-(Vc3-Vc1)*(V2-V1)/(Vc2-Vc1))-(2*z1*Sc/(Vc2-
Vc1))+(2*Sc*(z1+z2)*(Vc3-Vc1)/(Vc2-Vc1)^2);
c=(Sc*(V2-V1)/(Vc2-Vc1))-((z1+z2)*Sc^2/(Vc2-Vc1)^2);

I(3)=(-b-sqrt(b^2-4*a*c))/(2*a);         % reference current phase a (Amperes)
I(2)=(Sc-I(3)*(Vc3-Vc1))/(Vc2-Vc1);      % reference current phase b (Amperes)
I(1)=-I(2)-I(3);                         % reference current phase c (Amperes)

%% Check phase sequence of the reference currents
if angle(I(3))< angle(I(1))|| angle(I(2))> angle(I(1))
   I(3)=(-b+sqrt(b^2-4*a*c))/(2*a);
   I(2)=(Sc-I(3)*(Vc3-Vc1))/(Vc2-Vc1);
   I(1)=-I(2)-I(3);
end

%% Solve for the reference current for simulation circuit
%I
IM=abs(I)*sqrt(2);                       % Current Magnitude (Amperes)
IA=angle(I);                             % Current Angle (Radians)
```

A.5. Program for Reference Current Calculation for Experimental Set-Up

```
clc
clear
% Defining Sampling frequency and initial value of phase angle for
% referrence current
Ts=0.00004;
ph=77.5353/180*pi;
%Defining the unbalanced voltage level for experiment
U1=20;
U2=20*(cos(-2*pi/3)+j*sin(-2*pi/3));
%U2=0;
%U3=20*(cos(2*pi/3)+j*sin(2*pi/3));
U3=0;

% Defining the unbalanced impedances and system frequency
f=60;
w=2*pi*f;                    % Calculating w
Z1=w*0.01j+0.0001j;
%Z1=0.001j;
Z2=w*0.01j;
%Z2=0.001j;
%Z3=0;
Z3=w*0.01j-0.0001j;
% Defining the complex power set for operation of converter
S=60;
% Giving the initial values for the reference currents
I=zeros(1,3);
% Calculation of conjugates for input voltages and complex power
Up1=conj(U1);
Up2=conj(U2);
Up3=conj(U3);
Sp=conj(S);
% Calculation of a for quadratic equation a*I3^2 + b*I3 + c = 0
a=((2*Z1*(Up3-Up1)/(Up2-Up1))-((Z1+Z2)*(Up3-Up1)^2/(Up2-Up1)^2)-(Z1+Z3));
% Intermediate variables
t1=((U3-U1)-(Up3-Up1)*(U2-U1)/(Up2-Up1));
t2=(2*Z1/(Up2-Up1))-(2*(Z1+Z2)*(Up3-Up1)/(Up2-Up1)^2);
t3=(U2-U1)/(Up2-Up1);
t4=((Z1+Z2)/(Up2-Up1)^2);
% Calculation of b and c for quadratic equation a*I3^2 + b*I3 + c = 0
b=((U3-U1)-(Up3-Up1)*(U2-U1)/(Up2-Up1))-(2*Z1*Sp/(Up2-
Up1))+(2*Sp*(Z1+Z2)*(Up3-Up1)/(Up2-Up1)^2);
c=(Sp*(U2-U1)/(Up2-Up1))-((Z1+Z2)*Sp^2/(Up2-Up1)^2);

% Calculation of reference currents
I(3)=(-b+sqrt(b^2-4*a*c))/(2*a);
I(2)=(Sp-I(3)*(Up3-Up1))/(Up2-Up1);
I(1)=-I(2)-I(3);

% Calculation for magnitude and phase angle for reference currents
IM=abs(I)*sqrt(2);
IA=angle(I);
IA1=IA;
IA=IA+ph;
```

B. SIMULINK Blocks

B.1. DC Voltage Sensor for Closed Loop Operation



B.2. Neutral Current Calculation Block