Preprint
UCRL-JC-151647

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This article was submitted to
2003 Pulsed Power Conference, Dallas, Texas, June 15-18, 2003

U.S. Department of Energy
Lawrence Livermore National Laboratory

June 3, 2003

This work was performed under the auspices of the U.S. Department of Energy by University of California, Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

INVESTIGATION of VACUUM INSULATOR SURFACE DIELECTRIC STRENGTH with NANOSECOND PULSES *

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Abstract

The maximum vacuum insulator surface dielectric strength determines the acceleration electric field gradient possible in a short pulse accelerator. Previous work has indicated that higher electric field strengths along the insulator-vacuum interface might be obtained as the pulse duration is decreased [1].. In this work, a 250 kV, single ns wide impulse source was applied to small diameter, segmented insulators samples in a vacuum to evaluate the multi-layer surface dielectric strength of the sample construction. Resonances in the low inductance test geometry were used to obtain unipolar, pulsed electric fields in excess of 100 MV/m on the insulator surface. The sample construction, experimental arrangement and experimental results are presented for the initial data in this work. Modeling of the multi-layer structure is discussed and methods of improving insulator surface dielectric strength in a vacuum are proposed.

I. INTRODUCTION

Supporting very high electric fields in a vacuum environment is essential for compact particle accelerators. In fact, the electric field gradient on the vacuum insulators determines the acceleration gradient of a compact accelerator.

High gradient insulators are commonly fabricated by stacking multiple layers of insulators with thin layers of interleaved conductors. The rationale for this structure is based on the canonical vacuum insulator, surface dielectric strength failure mechanism of surface electric field distortion due to local surface electron avalanches. In an insulator surface dielectric strength failure, electrons emitted from a metal-insulator-vacuum triple point impact the insulator surface after being accelerated by the electric field. The incident electrons generate additional electrons via secondary electron emission, which proceed to generate additional electrons along the insulator surface. The movement and impact of the surface electrons result in surface heating, which leads to gas emission and ionization, and surface electric field distortion which results in the insulator surface being breached by a conducting discharge. The interleaved conducting layers are inserted in the insulator structure to intercept and dissipate the surface electron avalanche as well as capacitivly grade the voltage across the insulator in a transient voltage applications. Furthermore, should one of the multi-layer sections be shorted by a surface discharge, the capacitive nature of the stack distributes the potential change over the remaining surface uniformly.

Previous work by Elizondo, et. al[2] indicates that the surface dielectric strength of the insulator surface increases as the inverse root of the thickness of the individual insulator layer. The object of this work is to evaluate the surface dielectric strength of a multi-layer insulator stack when exposed to a very short duration (few ns) high electrical field (1 MV/cm) impulse.

II. EXPERIMENTAL SETUP

Several, multilayer insulator samples were fabricated and inserted into a nanosecond insulator test circuit, described below.

A. Insulator Test Articles

The multi-layer insulators, illustrated in Fig. 1, were fabricated with 10 mil Rexolite™ insulators and 0.5 mil Stainless Steel conducting layers by Krogh at the Honeywell KCP, Kansas City, MO.

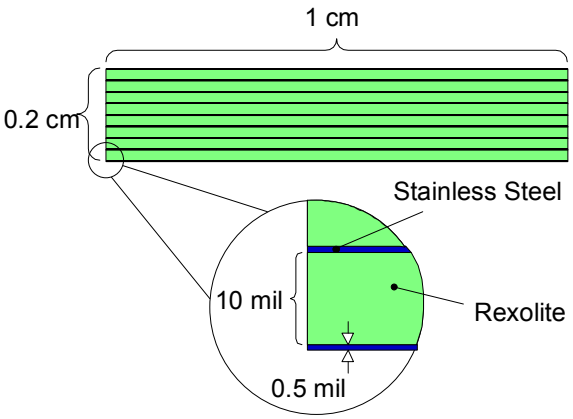

Figure 1. High Gradient Insulator Test Article

B. Nanosecond High Voltage Test System

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The above samples were exposed to a high voltage pulse that was generated by a fast Marx system, fabricated by Applied Physical Electronics, LC3 Austin, TX The Marx drives a 50 Ohm output cable that delivers a 250 kV impulse with a Full Width Half Max duration of approximately 1 ns to the insulator test chamber

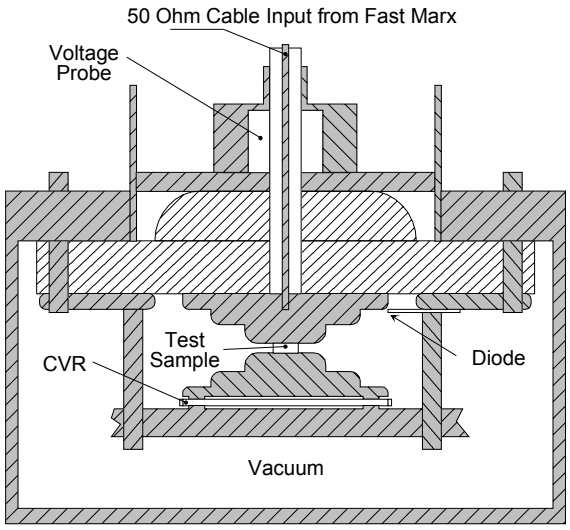

Figure 2. Nanosecond Insulator Test fixture

illustrated in Fig. 2. The test chamber was modified to minimize the inductance and stray capacitance of the sample holding electrodes. The fast Marx and the

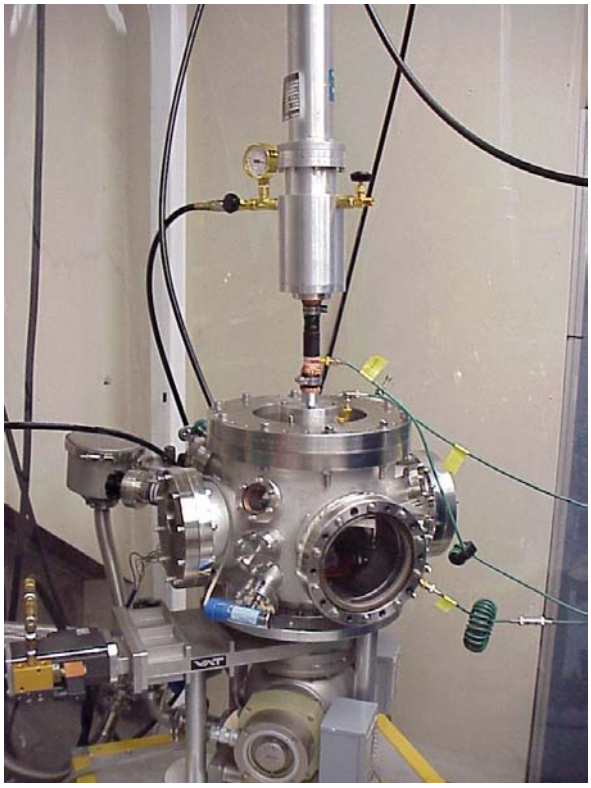

Figure 3. Marx and Sample Test Chamber

sample test chamber are shown in Fig. 3. A picture of the test sample mounted in the test fixture is shown in Fig. 4.

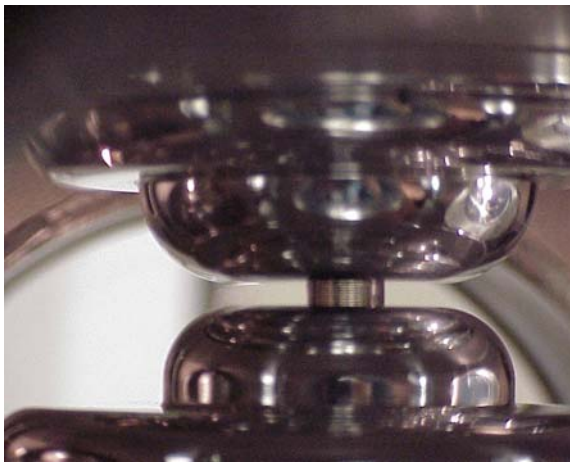

Figure 4. Multi-layer Sample in Test System

The voltage test chamber input voltage probe and the Current Viewing Resistor (CVR) illustrated in Fig. 2 were calibrated by replacing the 250 kV input from the 50 Ohm cable with a 1 kV, 1 ns impulse from a 50 Ohm cable reed pulse generator and the voltage across the sample directly measured with a Barth attenuator string. A 50 Ohm load was placed in parallel with the sample for a number of measurements to match the calibration setup. The distributed 50 Ohm load in parallel with the sample improved the voltage measured across the sample by reducing the after pulse ringing.

III. TEST CIRCUIT

The test circuit is a resonant circuit driven by an impulse from a 50 Ohm source as illustrated in Fig. 5.

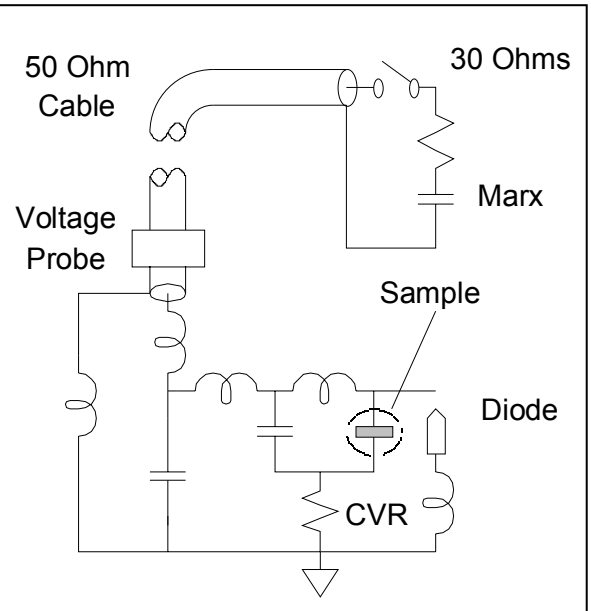

Figure 5. Insulator Test Circuit

The resonant nature of the circuit results in ringing current through the capacitor. The capacitance of the test circuit electrodes is dominated by the capacitance of the test

sample and the CVR measures the current through the test sample. The inductance of the current path is larger than desired such that the test sample voltage is isolated from the cable input and the test sample voltage is determined by the resonant circuit. The Marx generates a 350 kV, nanosecond pulse that is divided between the Marx output impedance and the 50-Ohm coaxial cable to deliver a 250 kV impulse to the test chamber.

The voltage input to the test chamber is shown in Fig. 6. Note that the additional voltage oscillations at late

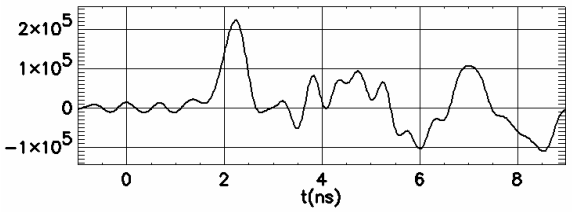

Figure 6. Chamber Input Voltage from Marx (V)

time in the voltage trace. The addition of a 50 resistor in parallel across the load reduces the amplitude of the late time oscillations. In addition, a vacuum gap was added in parallel with the sample to short the voltage at late times across the sample. The resulting current through the

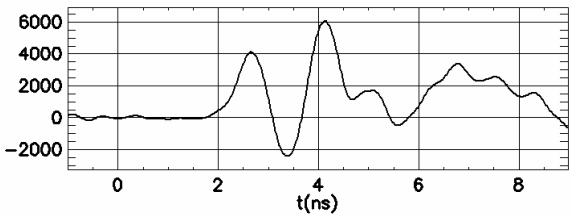

Figure 7. Capacitor Sample Current (A)

sample, measured with the CVR is shown in Fig. 7. Note that the current through the capacitor oscillates, but that the negative going portion of the current is smaller than the positive portion. Integrating the current through the insulator sample and the electrode capacitance in parallel yields the voltage across the sample, shown in Fig. 8.

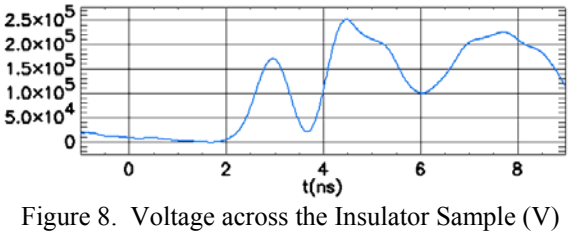

Figure 8. Voltage across the Insulator Sample (V)

The voltage across the capacitor is not the single impulse desired, but it does reach a gradient in excess of 1 MV/cm with an effective duration of 2-3 ns.

IV. INSULATOR DIAGNOSTICS

The insulator samples were conditioned by increasing the pulse voltage starting at 200 kV/cm and increased to maximum voltage out of the Marx. The 2mm high insulators experienced several surface failures as the voltage was increased. After each surface failure, the voltage was decreased by about ten percent and the voltage increased on subsequent voltage pulses. In this fashion, the voltage applied to the insulator samples was increased to that shown in Fig. 8. After 5-20 pulses at the maximum voltage, the samples would fail and recovery was not possible. Multiple samples demonstrated the same behavior in that it was possible to condition the samples to the maximum voltage, but the sample did not maintain the stress level over a large number of pulses.

The samples were examined under the microscope and observations of the surfaces and metal interfaces indicate several paths for improving the sample durability and possible performance. The sample surface shown in Fig. 9 indicates several tracks between individual layers in the

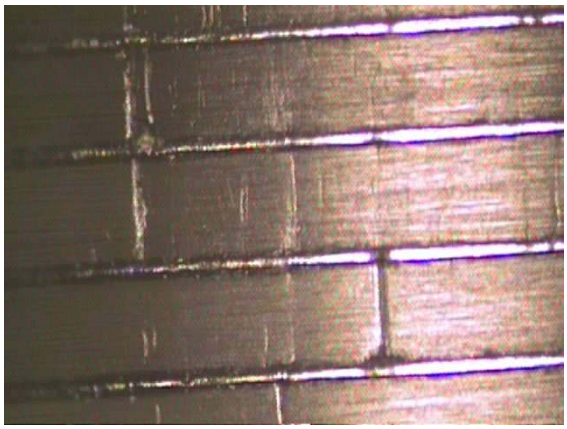
Figure 9. Insulator Interlayer Conduction Paths

insulator stack. Another close up of the insulator-metal layer interface in Fig. 10 illustrates several problems related to the geometry of the insulator stack. The

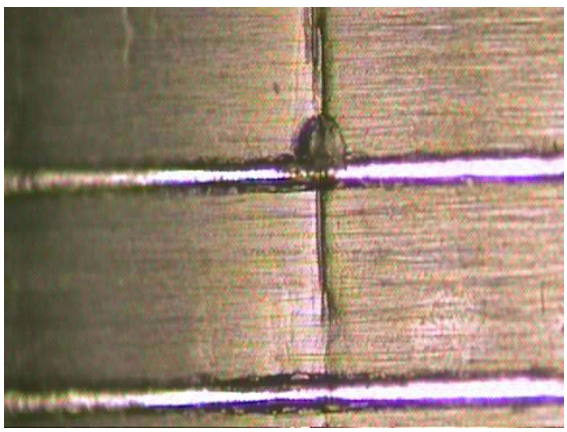
Figure 10. Metal-Insulator Interface Faults

interface between the metal-insulator is recessed such that the electric field at the metal-insulator-vacuum junction or triple-point is enhanced. The sharp edge of the metal layer, 0.5 mil thick, greatly enhances the electric field. In addition, the permittivity of the insulator material that is removed near the edge of the metal layer further enhances the electric field at the triple point. This situation

illustrates the difficulty of intimately mating the insulator and the metal layers and hiding or reducing the electric field at the triple point.

After a number of failures at the maximum voltage, the insulator could not be reconditioned, due to the excessive damage shown in Fig. 11.

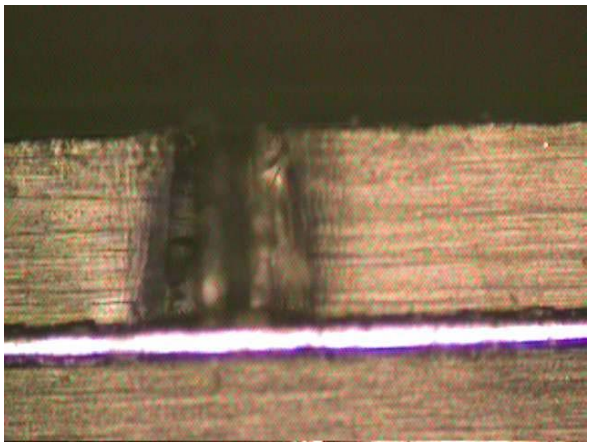

Figure 11. Terminal damage of insulator layer

A second observation is that the thin metal layer is easily vaporized in a inter-layer discharge due to its small cross section and the point nature or cathode spot dimensions of a discharge from the metal. The vaporized metal is easily deposited on the insulator surface as illustrated in Fig. 12. This result indicates the presence

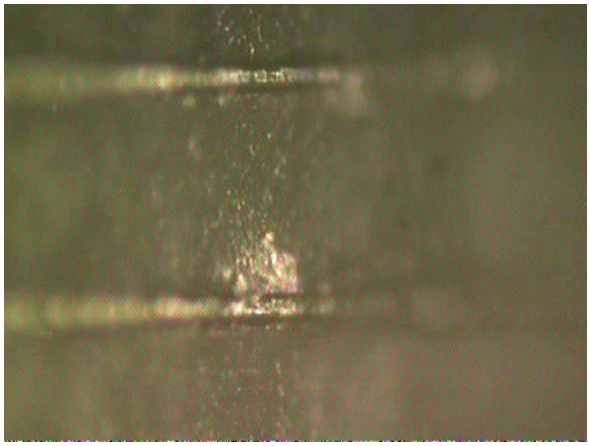

Figure 12. Metal Deposited on Insulator Surface

of the metal layers is not always beneficial, especially very thin layers.

V. SUMMARY AND CONCLUSIONS

These experiments with very short, very low energy, but very high electric field pulses applied to insulator surfaces have indicated several directions for development of multi-layer insulators. The low pulse energy employed allowed the effects on the insulators to be observed without massive destruction of the insulator surfaces. These preliminary results follow a trend that vacuum insulators can support much higher surface electric fields in short duration electrical pulses as

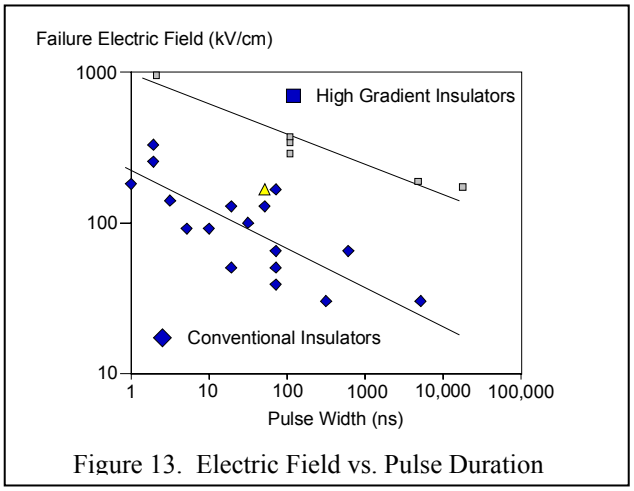

Figure 13. Electric Field vs. Pulse Duration

illustrated in Fig. 13. [4]

The two most important observations are that the presence of the thin metal layers is not necessarily beneficial. The very thin metal layers seem to be detrimental when the sharp metal edges enhance the electric field to provide many sources of free electrons and the recessed insulator geometry further serves to further enhance the triple point emission of electrons. The second detrimental aspect of the thin metal layers at the insulator surface do not have sufficient thermal mass to prevent vaporization of the metal and deposition of the metal on the insulator surfaces, prior to the formation of carbon conduction paths.

This work thus results in several recommendations for future multi-layer insulator fabrications: 1) the triple points for any conducting layers should be hidden as much as possible at the surface, and 2) the material used for the conducting layers should be very high temperature materials that force low current density conduction. One such material is Silicon Carbide, which is a high temperature material with a resistivity that can be tailored to optimize current spreading at discharge sites.

VI. REFERENCES

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