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Fault Discrimination Algorithm for Busbar Differential Protection Relaying Using Partial Operating Current Characteristics

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Abstract

Differential protection is the unit protection system which is applied to protect a particular unit of power systems. Unit is known as zone in protection terminology which is equivalent to simple electrical node. In recent time, low impedance current differential protection schemes based on percentage restrained characteristics are widely used in power systems to protect busbar systems. The main application issue of these schemes is mis-operation due to current transformer (CT) saturation during close-in external faults. Researchers have suggested various solution of this problem; however, individually they are not sufficient to puzzle out all mis-operational scenarios. This thesis presents a new bus differential algorithm by defining alternative partial operating current characteristics of a differential protection zone and investigating its performance for all practical bus faults. Mathematical model of partial operating current and operating principle of the proposed bus differential relay are described in details. A CT saturation detection algorithm which includes fast and late CT saturation detection techniques is incorporated in relay design to increase the sensitivity of partial operating current based internal-external fault discriminator for high impedance internal faults. Performance of the proposed relay is validated by an extensive test considering all possible fault scenarios.

Keywords: Differential Protection; CT Saturation; Internal Fault; External Fault; Fault Discrimination; Relay.

Chapter 1

1. Introduction

In Chapter 1 we provide a general idea about a power system and its protection, especially the bus protection. Various differential protection schemes are used in modern power systems. Particularly, for bus protection, low impedance differential protection is very popular and effective [1]. However, current transformer (CT) saturation has a severe impact on the performance of low impedance differential protection. The overview of current transformer (CT) saturation and historical review of low impedance bus differential protection as well as current transformer (CT) saturation are presented. After extensive historical review of existing methods, the outline of this thesis is provided in Section 1.8.

1.1 Overview of Power System

Modern power systems are the combination of various complex elements such as generators, transformers, transmission lines, loads and protection and control equipments. Generally, power systems are divided into three stages: generation, transmission and distribution. The most convenient method to generate electricity is to burn fossil fuels to convert water into steam which is used to rotate a turbine that is connected to the rotor shaft of an electric generator. Water is also used to turn generators in hydro-electric power plant. In the last few decades, various new sources of electricity has been introduced which is called renewable energy such as solar, wind, geothermal and biomass etc. In all cases, the electricity generated at these facilities flows across the transmission system. Voltage at the generating stage is normally low, and hence, the generated voltage is raised by using step-up transformers

to transmit power over long distance to reduce the higher voltage level transmission loss by reducing current. At the end of transmission system, voltage is stepped down by using step down transformer for power flow through distribution system and for supplying to residential and commercial customers.

The primary goal of any electric power utility is to provide uninterrupted power to the end consumer, and to achieve the goal, electric utilities depend on protection systems to provide protection to power systems equipment and elements such as generators, transformers, bus bars, overhead transmission lines operating in abnormal or fault conditions.

Most important criteria of power systems are the balance between generation and demand and to maintain the balance, utilities all over the world use various control systems such as supervisory control and data acquisition (SCADA) system and automatic generation control (AGC) system.

1.2 Overview of Power System Protection

The main purpose of a power system protection is to isolate a faulty section of the electrical power system from rest of the healthy systems so that the remaining live portion can function satisfactorily without any severe damage due to fault current [1]. Identification fault and isolating faulty part from the remaining healthy systems to secure the continuation of power supply are not straightforward.

The elementary power system protective device is the fuse. When the current through a fuse exceeds a certain threshold, the fuse element melts and produces an arc across the resulting gap that is then extinguished to interrupt the circuit [2]. Given that fuses can be built as the weak point of a system, fuses are ideal for protecting circuits from damage. Fuses

however have two problems: first, after they have functioned, fuses must be replaced as they cannot be reset. This can prove inconvenient if the fuse is at a remote site or a spare fuse is not on hand. And second, fuses are typically inadequate as the protective device in most power systems as they allow current flows well in excess of that that would prove lethal to a human or animal. In general, fuses are used to protect simple and low power equipments. They are not suitable to use as the sole safety device in modern day high voltage and complex power systems.

Modern day's power system protection schemes are very sophisticated. They are built by integrating various complex devices or components. Circuit breaker, relay and DC system are the three main components of any protection scheme of power systems. All of these three components of protection scheme work simultaneously to give effective security against faults. Circuit breaker isolates the faulty system from rest of the healthy system and this circuit breakers automatically open during fault condition due to its trip signal comes from protection relays [1].

Depending on arc quenching mechanisms, circuit breakers are classified as bulk oil circuit breaker, minimum oil circuit breaker, SF_6 circuit breaker, air blast circuit breaker and vacuum circuit breaker etc. They are also classified as solenoid circuit breaker, spring circuit breaker, pneumatic circuit breaker, hydraulic circuit breaker etc. depending on operating mechanisms.

Power system protection relays are classified as current relays, voltage relays, impedance relays, power relays, frequency relays, etc. based on operating parameter. As per

operating characteristics, they are categorized as definite time relays, inverse time relays, stepped relays etc. According to operating logic, they are categorized as over current relays, distance relay and differential relays etc.

All the circuit breakers of electrical power systems are DC (Direct Current) operated. Because DC power can be stored in battery and if situation comes when total failure of AC power occurs, still the circuit breakers can be operated for restoring the situation by the power of storage battery . Hence the battery is another essential item of the power system protection. Some time it is referred as the heart of the electrical substation. An electrical substation battery or simply a station battery containing a number of cells accumulate energy during the period of availability of AC supply and discharge at the time when relays operate so that relevant circuit breaker is tripped.

The main philosophy of protection is that no protection of power systems can prevent the flow of fault current through the system, it only can prevent the continuation of flowing of fault current by quickly disconnect the short circuit path from the system [1] [3]. Protection systems should have several important functional requirements to satisfy this quick disconnection.

Reliability is the most important requisite of power system protection. The protection relays should remain inoperative for a long time before a fault occurs; but if a fault occurs, they must respond instantly and correctly.

Selectivity is another important requisite of power system protection schemes. Relays should be operated in only those fault conditions for which schemes are commissioned in the

system. There may be some typical condition during fault for which some relays should not be operated or operated after some definite time delay and so protection relays must be proficient to select appropriate condition for which it would be operated.

The protective relays must be sufficiently sensitive so that it can be operated reliably when level of fault condition just crosses the predefined set limit.

Another important requisite of protection systems is the speed of operation. The protective schemes must operate within set time duration after detecting fault. There must be a correct coordination provided in various power system protection relays in such a way that for the fault at one portion of the system should not disturb other healthy portions [4] [5]. Fault current may flow through a part of healthy portion as they are electrically connected. However, relays associated with that healthy portion should not be operated faster than the relays of faulty portion otherwise undesired interruption of healthy systems may occur. If relay associated with faulty portion is not operated in proper time due to any defect in it, then only the next relay associated with the healthy portion of the system must be operated to isolate the fault [4] [5]. Therefore, it should neither be too slow which may result in damage to the equipment nor should it be too fast which may result in undesired operation.

1.3 Overview of Busbar Protection

The main objectives of all protection schemes, specifically to maintain continuity of supply and limit the material damage, are achieved by isolating the faulty element as quickly as possible. Delay increases not only the risk of damage of faulty element and it's adjacent elements, but also the risk of undue disturbance of the normal operation of the whole systems

by, for example, loss of stability and reduction of voltage. Hence, no part of power systems can safely be left unprotected, much less the busbars because of their especially vital position and function in the system. All means of protection, even those applied to the earliest and simplest system, have in some way or other contrived to satisfy the precept that all elements of the system must be protected, including busbars [6]. Busbar is the most critical element of a power system, as it is the point of convergence of many transmission lines, transformers, generators and loads. The effect of a single bus fault is equivalent to many simultaneous faults and usually, due to the concentration of supply circuits, involves high current magnitudes. Any incorrect operation would cause the loss of all of these elements. Therefore, protection of busbar demands high speed, reliability and stability. Failure-to-trip on an internal fault, as well as false tripping of a busbar during service, or in case of an external fault, can both have disastrous effect on the stability of the power system, and may even cause complete blackout of the system [7]. So, it is very essential to incorporate precision and reliability factors during designing a busbar protection scheme. It was a very old practice in small substations to provide over-current relays to work for the protection of the busbar and no separate relays were used for the purpose as this was not found to be cost effective. But, with the increase in substation equipments and feeder's complexity, it was felt necessary to go for reliable busbar protection schemes. The methods most commonly used to protect busbars are frame leakage protection, direction comparison protection and differential protection.

The frame leakage method involves insulating the bus-supporting structure and its switch gear from ground; and interconnecting all the framework, circuit-breaker tanks, etc. to provide a single ground connection through a current transformer (CT) [6]. The secondary side

of that CT is connected with an over current relay. The over current relay drives a multi-contact auxiliary relay that trips the breakers of all circuits connected to the bus. This method is most effective when the switchgear is of the isolated-phase construction. However, it is possible to design other types of switchgear with special provisions for making ground faults the most probable. If phase to phase faults not involving ground occur, the frame leakage method would probably not be justified. The frame leakage protection is quite popular in small indoor installations [8]. This method is most effective for the metal-clad type installation where provision can be made for effective insulation from ground. Certain existing installation may not be adaptable to fault-bus protection, owing to the possibility of other paths for short-circuit current to flow to ground. It is necessary to insulate cable sheaths from the switchgear enclosure and entrance bushing support from the rest of the structure otherwise cable ground-fault currents may find their way to ground through the fault-bus CT and improperly trip all the switchgear breakers. For sectionalized bus structure, separate frame leakage relaying must be employed for each section. The frame leakage method does not offer overlapping of protective zones; therefore complementary relaying is required to protect the regions between bus sections.

The directional comparison method is based on the comparison of relative directions of the fault currents flow in all the circuits connected to the busbar. For bus faults, currents through all circuits connected to the bus flow toward bus; however, fault current flows outward from the busbar in at least one circuit for external fault [6]. Typically, this principle has been used only with ground relays, on the basis that most bus faults start as ground faults, or at least that they very quickly involve ground. This greatly reduces the cost of the equipment.

Phase relays can also be used; however, it is more costly than other bus protection systems.

The chief disadvantage of this scheme is the greater maintenance required and the greater probability of failure to operate because of the large number of contacts in series in the trip circuit [3]. Another disadvantage is that connections from the current transformers in all the circuits must be run all the way to the relay panel if phase relays were used. Moreover, phase would depend on bus voltage for polarization, and, therefore, they might not operate for a metallic short circuit that reduced the voltage practically to zero.

Differential protection is widely used to protect busbar because of its versatility and cost effectiveness. Differential relays are very sensitive to the faults occurred within the protected zone but they are least sensitive to the faults that occur outside the protected zone. The operating principle of differential relay is somewhat different from other relay. The differential relay operates when there is a difference between two or more similar electrical quantities exceeds a set or threshold value. In differential relaying scheme, more than one current come from different parts of an electrical node or junction. Summation of these currents passes through the relay coil. According to Kirchhoff Law, the phasor sum of these currents is zero at normal operating condition [9]. Therefore, no current will be flowing through the relay coil at normal operating conditions. But due to any abnormality in the node or junction, the phasor sum of these currents no longer remains zero and this non-zero current will be flowing through the relay coil therefore relay being operated. In differential scheme, more than one set of current transformer are involved to protect equipment by differential relay. The ratio of the current transformer (CT) needs be chosen carefully. The polarity of CTs is another very important issue for differential protection. Differential scheme is only used for clearing the fault

inside the protected zone or equipment in other words differential relay should clear only internal fault of the zone or equipment [10]. Therefore, the protected zone or equipment should be isolated as soon as any fault occurred inside the equipment or zone. They need not be waiting or delaying for coordination with other relays in the system. There are mainly two types of differential protection system depending upon the principle of operation: voltage balanced differential protection and current balanced differential protection.

In voltage balanced differential protection scheme, the current transformers are connected in such a way that EMF induced in the secondary of current transformers (CTs) will oppose each other according to the original current direction at primary circuit. The differential relay coil is connected in the loop created by series connection of secondary of CTs. In normal operating conditions and also in through fault conditions, resultant EMF is zero and hence no current would be flowing through the relay coil. But as soon as any internal fault occurs in the protected zone, the resultant EMF is no longer balanced hence current starts flowing through the relay coil and finally trips circuit breakers [3]. Multi tap transformer construction is required to accurate balance between current transformers.

In current balanced differential scheme, current transformers (CTs) are connected in such a way that the secondary currents of CTs will oppose each other according to the original current direction at primary circuit. Summation of these currents which is called operating current which passes through the operating coil of the relay element. Ideally, under normal operating conditions or external through fault conditions, current summation is zero; hence no current will be flowing through the relay coil. However, if any ground fault occurs inside the

protected zone, summation of secondary currents will be no longer zero. In this situation the differential relay is being operated to isolate the faulty zone from the system [11] [12]. According to the type of relay used, there are two kinds of current balanced differential protection such as high impedance and low impedance differential protection.

In high impedance differential protection, relay is connected with a high impedance resistance. Here, voltage relay is used that means relay is operated by voltage [3]. Any operating current is forced through the high impedance causing voltage drop across the relay and relay gets trip.

In low impedance differential protection, a relay operated by current is used and it has low impedance current inputs. If any operating current resulting from an internal fault passes through the operating coil of the relay and relay gets trip.

1.4 Low Impedance Differential Protection: CT Saturation Issues

Recently, micro-processor based low impedance differential protection schemes have become popular to protect busbars. Low impedance differential protection schemes are operated based on operating current which is the summation of all CT secondary currents. Practically summation of the secondary current is not zero even for normal operating conditions as accurate matching of characteristics of current transformer cannot be achieved hence there may be spill current flowing through the relay in normal operating conditions. Moreover, there may be a probability of mismatching in cable impedance from CT secondary to the remote relay panel. These uneven pilot cables' capacitance causes high current through the relay operation coil when large external through fault occurs. This operating current is known

as false operating current and it becomes high during high loading conditions or high system congestion. To overcome these issues, the concept of restrained current has been adapted with low impedance differential scheme. This modified scheme is known as percentage restrained differential protection because the operating current required to trip can be expressed as a percentage of restrained current. There are several mathematical definitions of restrained current. In most of the cases, the restrained current is defined by half of the summation of secondary currents magnitude of all CTs involved with protected zone [13]. Under normal and through fault conditions, operating current is less than a percentage of restraining current therefore relay remains inactive. During internal fault, the operating current becomes greater than a percentage of restrained current and the relay is operated [14].

The main application issue with this modified differential protection is to make it secure from mal-operation in response to the CT saturation during close-in external faults. During close-in external faults, probability of CT saturation becomes high and this CT saturation creates high operating current in CT secondary circuit which causes the undesired operation of relay. The primary reason for such mal-operation is the fact that the traditional percentage differential principle relies exclusively on current magnitude rather than directionality for tripping decisions. Therefore, proper discrimination of external and internal fault becomes the main concern for the performance of bus bar differential protection.

1.5 Literature Review Low Impedance Differential Protection

To prevent the mal-operation of current balanced busbar differential protection due to current transformer saturation especially during external fault, several techniques were proposed by different scientists and researchers. This section reviews available fault

discrimination techniques to secure current balanced bus bar differential protection system from false operation.

Multi slope Percentage restrained differential protection is one of the oldest forms of adaptive protection algorithms. The slope characteristic can provide high sensitivity when low levels of current are flowing in the zone of protection but has less sensitivity when high levels of current are flowing [14]. This improves security because CTs are more prone to saturation when they have to reproduce high levels of current in the primary circuits. Although the above slope characteristic provides some security against CT errors, it is not adequate for all practical scenarios. Two common failures reported with conventional slope characteristics are due to CT saturation which occurs during close-in external faults and the subsidence currents present after clearing external faults.

Several techniques were proposed based on CT saturation detection supervision to prevent mal operation of bus differential relay during CT saturation in external fault. However, they are failed to provide complete solution as CT can also be saturated during internal fault. A harmonic-current-based restraining method was introduced by Kennedy and Hayward [15]. If the harmonics contained in the differential current are larger than the threshold, the relay is inhibited. The method ensures stability on an external fault, but delays the operating time of a relay for an internal fault until after the DC component decays to a low value. When a CT saturates, the operating time is significantly increased. An algorithm that detects the onset of CT saturation based on the first-difference function of the current was described by Phadke and Thorp [16]. It assumes the current immediately collapses to zero when the CT enters saturation.

Difficulties arise if the current does not collapse to a low value during saturation. A solid-state busbar protection relay was proposed by Royle and Hill [17]. The relay detects the onset of saturation by detecting when the current collapses to a low value. It then shunts the current away from the operating circuit by closing a switch adjacent to the saturated CT. Although this technique prevents an external fault, the relay causes an operating time delay when a CT saturates on an internal fault. A microprocessor-based busbar protection relay that included a countermeasure for CT saturation was reported by Andow et al. [18]. The waveform discriminating element (WDE) is based on the assumption that the differential current during an external fault is nearly zero between the periods that corresponds to CT saturation. The WDE detects the onset of saturation by comparing the change in the instantaneous differential current against the instantaneous restraining current. The relay is inhibited for a predetermined period if the former is significantly less than the latter. The WDE is unable to indicate which CT is saturated and the blocking scheme may delay the operation of the relay on an internal fault. In addition, for a power system with a large primary time constant, a larger blocking period is needed and consequently a longer operating time delay is inevitable.

An impedance-based CT saturation detection algorithm for busbar differential protection was described by Fernandez [19]. The detection algorithm relies on the assumption that the current is decreased during saturation and thus the impedance is increased. The impedance is calculated at the relaying point and compared with the source impedance. If the estimated impedance is larger than the source impedance, saturation is detected and a blocking signal is issued. The algorithm is only valid if, after fault occurrence, the change in the impedance is negligible until saturation starts. Thus, it is difficult to detect saturation when the

impedance increases significantly after fault occurrence. In addition, the algorithm uses a voltage signal to detect saturation and thus can cause an increase in the operating time. A microprocessor-based bus bar protection system that estimates the impedances of the positive- and negative sequence circuits for every feeder connected to the busbar was proposed by Gill et al. [20]. The basic idea of the algorithm is similar to phase angle comparison. It compares the direction of current flow for each feeder and consequently is less dependent on the effect of CT saturation than a magnitude comparison algorithm [21]. The technique detects an internal fault if all the impedances seen by every feeder are located in the third quadrant of the impedance plane. The performance of the technique is satisfactory for mild saturation. However, correct operation of the technique is not guaranteed for severe saturation caused by a high level of remnant flux. Moreover, the technique requires significant computational burden as compared with phase angle comparison, since it calculates the positive- and negative sequence components of the voltages and currents for every feeder. Yong-Cheol Kang et al., has proposed a bus differential relay which operates in conjunction with a saturation detection algorithm based on the third-difference function applied to the current signal [22]

A wavelet transform (WT) based busbar protection scheme that utilizes detail decomposition of differential current to detect internal faults [23]. The algorithm relies on the assumption of time shift in transients between differential current and source current as most of the connected elements are inductive. However, the transients associated with the source current and the fault current are independent of location of fault (internal or external) which leads to mal-operation of the protection scheme. A backup protection is proposed based on polarities of peak d-coefficients obtained from Multi Resolution Analysis to prevent this mal-

operation; even then, this technique is vulnerable at CT saturation and high impedance internal fault.

The preservation of current phase angle always takes place even if CT saturation or dc offset conditions occur to the input ac currents. As a result, if the phase angle of the current waveforms is compared with the phase angle of each of the input bus currents, a decision can be made whether a fault is external or internal to the differential protected zone irrespective of the waveform distortions due to the errors in CTs. Comparing phase currents in near real time, a comparison can be made between currents that are entering the bus and those currents that are leaving the bus. This is intuitively true since Kirchoff's law also applies to phase angles as well as to current magnitudes. However, the key challenge in this method is estimation of phase angles between all current phase angles rapidly in real time. A technique based on dot product was used in reference [13] [24] to determine the differences in phase angles. This technique is suitable for transformer differential protection where two input currents are involved. But it is critical to implement for bus bar differential protection as more than two input currents are involved. Moreover, during a high impedance internal bus fault, load flow may continue to flow on passive elements and may cause the phase angles function to block the relay from tripping for the internal fault.

A fault discrimination method was proposed based on differential rate of change of operating current and restrained current [24] [25]. The detection algorithm relies on the assumption that for an internal bus fault, the rate of change of operating current is greater than the rate of change of restrained current whereas for external faults, the rate of change of

restrained current is greater than the rate of change of operating current. This technique provides security for low CT saturation during external fault. However, it has limitation for severe CT saturation as change of operating current becomes high as soon as CT starts saturated.

A different technique has been proposed based on alienation concept in order to determine busbar fault type whether internal or external to make relay trip or no trip decision, respectively [26]. The variance between any two signals is defined as the alienation coefficient, which is obtained from correlation coefficient. For internal fault, alienation coefficient is greater than zero and for external fault it is less than zero. In case of CT saturation, this technique compares the alienation coefficients of unsaturated portion and saturated portion of current to discriminate the fault. It assumes current remains unsaturated in first quarter cycle. This technique provides security for slow CT saturation during external fault. However, it leads mal-operation for severe CT saturation as CT starts saturated in first quarter cycle.

1.6 Current Transformer (CT) Saturation

Protective relays are actuated by current and voltage supplied by current and voltage transformers. These transformers provide insulation against the high voltage of the power circuit and also supply the relays with quantities proportional to those of the power circuit, but sufficiently reduced in magnitude so that the relays can be made relatively small and cost effective. All types of current transformers are used for protective-relaying purposes. The bushing CT is almost invariably chosen for relaying in the higher-voltage circuits because it is less expensive than other types. It is not used in circuits below about 5 kV or in metal-clad

equipment [3]. All CT accuracy considerations require knowledge of the CT burden. The external load applied to the secondary of a current transformer is called the burden. The burden is expressed preferably in terms of the impedance of the load and its resistance and reactance components. The term burden is applied not only to the total external load connected to the terminals of a current transformer but also to elements of that load.

Protective relay accuracy and performance are directly related to the steady state and transient performance of the CTs. Protective relays are designed to operate in a shorter time than the time period of the transient disturbance during a system fault. Large errors of CT transient may delay or prevent relay operation. CT output is impacted drastically when the CT operates in the nonlinear region of its excitation characteristic [27]. Operation in this region is initiated by:

- Large asymmetrical primary fault currents with a decaying dc component.
- Residual magnetism left in the core from an earlier asymmetrical fault, or field testing, if the CT has not been demagnetized properly.
- Large connected burden combined with high magnitudes of primary fault currents.

The instantaneous CT secondary current is the sum of the instantaneous burden current and the magnetizing current. The CT steady-state magnetizing current is very negligible as long as the CT operates in its linear region; therefore the burden current is a replica of the primary current adjusted by the CT ratio. When the CT is forced to operate in its nonlinear region, the magnetizing current can be very large due to a significant reduction of the saturable

magnetizing inductance value. The magnetizing current which can be considered as an error current, subtracts from burden current and drastically affects the current seen by the connected burden on the CT secondary winding. When the CT saturates because of the dc component, it can do so in the first few cycles of the fault. Long dc time constant offset faults can cause CTs to saturate many cycles after a fault [28].

1.7 Literature Review of CT Saturation Detection

Low impedance differential protection is severely affected by the current transformer saturation during close-in external faults. This CT saturation creates high operating current in CT secondary circuit which causes the undesired operation of relay. Proper CT saturation detection is one of the major concerns to prevent mal-operation of bus bar differential protection.

A CT saturation algorithm has been proposed based on waveform model by A.G. Phadke and J. S. Throp [16]. It is based on the fact that secondary current is abruptly changed when CT saturation sets in. However, this algorithm fails when CT secondary current changes slowly. Another waveform method based on long data window has been proposed to detect CT saturation [29]. Computational time is comparatively high for this method because number of involved variables is more. Therefore, this method is slow to use together with any fast tripping algorithm. An algorithm based on the core flux calculating from a secondary current and then compensating the distorted secondary current was proposed [30]. The algorithm can successfully calculate the core flux and detect CT saturation in various conditions. However, this method is based on the assumption that the remanent (residual) flux at the beginning of calculation is zero.

Based on evaluating mean of error and the mean and variance of current amplitude, a CT saturation detection method was suggested [31]. The error is calculated on the assumption that the current is a perfect sinusoid. Hence the summation of the current and its second-order derivative should be zero. C. Fernandez has proposed an impedance-based CT saturation detection algorithm for bus-bar differential protection [19]. It is based on the first-order differential equation for the power system source impedance at the relay position and uses the busbar voltage as well as current signal to detect CT saturation.

An algorithm based on the third difference of a secondary current has been presented to CT saturation detection [32]. Third difference is more effective to detect CT saturation because it has large value than first and second difference. However, an anti-aliasing low-pass filter softens the current and, thus, reduces the values of the third difference at those instants. Selection of sampling rate is very important to overcome the effect of a remanent (a term used by IEEE) flux in the core and a low-pass filter on the proposed algorithm.

A method based on symmetrical component analysis has been suggested to detect current transformer (CT) saturation [33].The proposed algorithm computes the positive-sequence negative-sequence and zero-sequence components of the differential current and also monitors the rate of change of the sequence component currents. The sequence component domain of differential current allows the differential protection scheme to more sensitively detect the system changing from a symmetrical condition to an asymmetrical fault condition. This concept is applied to detect CT saturation which gives an early indication of a CT being driven into saturation.

An algorithm has been developed to detect CT saturation by comparing the angle difference between the second harmonics of the rate of change of operating current and the rate of change of restrained current [34]. In this algorithm, the phase between the second harmonic of the derivatives of the operating current and restrain current is estimated and compared against the threshold value.

1.8 Scope of Thesis

The purpose of this research is to develop a fault discrimination algorithm that is based on newly defined partial operating current characteristics of a differential protection zone to overcome the impact of CT saturation on low impedance current differential protection. Finally, a bus differential relay is designed by incorporating the proposed fault discrimination algorithm and its performance is validated by an extensive experimental study. The detail scope of work of the thesis is presented below:

- Mathematical development of the partial operating current characteristics.
- Development of the proposed fault discrimination algorithm.
- Designing of a bus differential relay by incorporating the proposed fault discrimination algorithm as well as a supervisory technique based on CT saturation detection algorithm to ensure high sensitivity for high impedance internal fault conditions.
- Modeling the proposed bus differential relay in Matlab platform.
- Modeling a three bus test system in EMTP which includes all possible elements of power systems such as transmission line, generator (active source) and load (inactive source).

- Simulating all possible bus faults (12 scenarios) and finding the responses of proposed relay.
- Comparing results with two latest existing methods, namely, delta phase angle method and rate of change method.

Chapter 2

2 Mathematical Modeling

In this chapter, mathematical modeling of differential protection principle and current transformer (CT) saturation are discussed in detail. Different existing methods to discriminate internal and external faults are explained.

2.1 Differential Protection Principle

Power systems can be divided into different blocks or units such as generator, transmission line, transformer, bus and motor etc. Protection systems are applied to the system can be classified into two categories such as unit protection or non-unit protection. Differential protection is the unit protection system which is applied to protect a particular unit. Unit is known as zone in protection terminology which is equivalent to simple electrical node. The unit or zone is bounded by CT locations.

2.1.1 Basics of Differential Protection

Kirchhoff's current law is the principle of conservation of electric charge which implies that: at any node (junction) in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node, or equivalently the algebraic sum of currents in a network of conductors meeting at a point is zero [35].

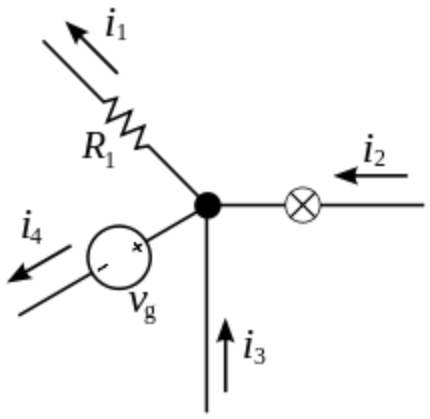

Figure 2.1: Electrical node or junction [35]

Recalling that current is a signed (positive or negative) quantity reflecting direction towards or away from a node; this principle can be stated as:

$$\sum_{k=1}^{n} I_k = 0 \tag{2.1}$$

Where n is the total number of branches with currents flowing towards or away from the node. This formula is valid for complex currents:

$$\sum_{k=1}^{n} \vec{I}_k = 0 \tag{2.2}$$

The law is based on the conservation of charge whereby the charge (measured in coulombs) is the product of the current (in amperes) and the time (in seconds). Differential protection works based on above mentioned Kirchhoff's current law. According to Kirchhoff's current law, under normal condition input current equals to output current for a power system

zone [35]. In power system, zone can be two terminals such as transformer, transmission line etc. or multi terminals such as busbar.

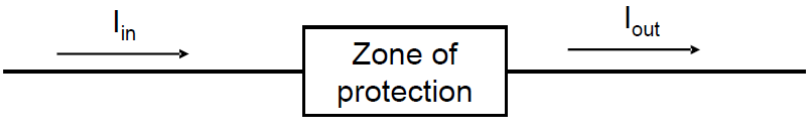

Figure 2.2: Two terminal zone under normal condition

In case of two terminal zone as shown in Figure 2.2, when system is normal

$$I_{in} = I_{out} \tag{2.3}$$

However, if there is any fault in the system as shown in Figure 2.3

$$I_{in} \neq I_{out} \tag{2.4}$$

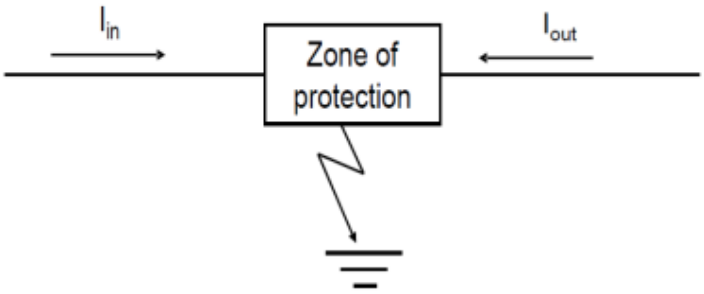

Figure 2.3: Two terminal zone under fault condition

With multi terminal zone as shown in Figure 2.4, when system is normal

$$I_{in} = I_{out}$$

$$I_2 + I_3 = I_1$$

$$I_1 - I_2 - I_3 = 0 \tag{2.5}$$

Considering phasor of the currents, Equation (2.5) can be rewrite as

$$I_1 + I_2 + I_3 = 0 \tag{2.6}$$

Eq. (2.6) shows in normal system condition, vector summation of all terminal currents must be equal to zero.

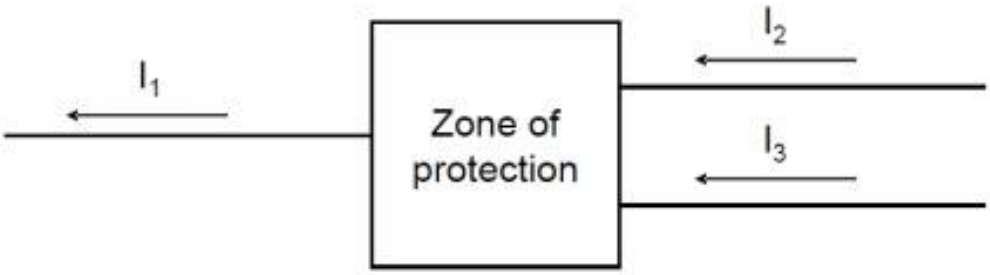

Figure 2.4: Multi terminal zone under normal condition

With multi terminal zone as shown in Figure 2.5, when system is faulty

$$I_{in} \neq I_{out}$$

$$I_2 + I_3 \neq I_1$$

$$I_1 - I_2 - I_3 \neq 0 \tag{2.7}$$

Considering phasor of the currents, Equation (2.7) can be rewrite as

$$I_1 + I_2 + I_3 \neq 0 \tag{2.8}$$

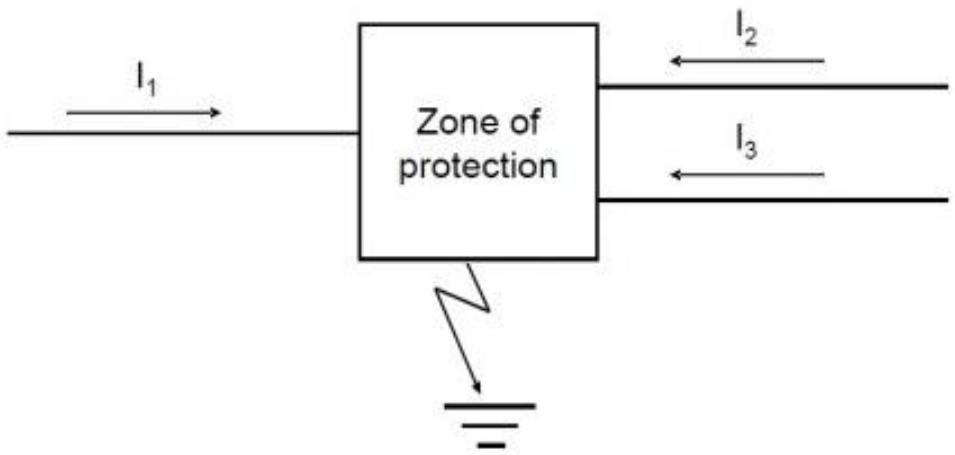

Figure 2.5: Multi terminal zone under fault condition

Eq. (2.8) shows in abnormal or faulty system condition, vector summation of all terminal currents is not equal to zero.

2.1.3 Restrained differential Protection

Practically, summation of CT secondary currents is not zero even for normal operating conditions due to the mismatch of CT ratio and burden. Hence there is some spill current flowing through the relay in normal operating conditions which is known as false operating current. It becomes high during high loading conditions or high system congestion. To overcome these issues, the concept of restrained current has been adapted with low impedance differential scheme. This modified scheme is also known as percentage restrained differential protection. In this scheme, the operating current is compared with the restrained current to detect fault or abnormal condition as shown in Figure 2.6.

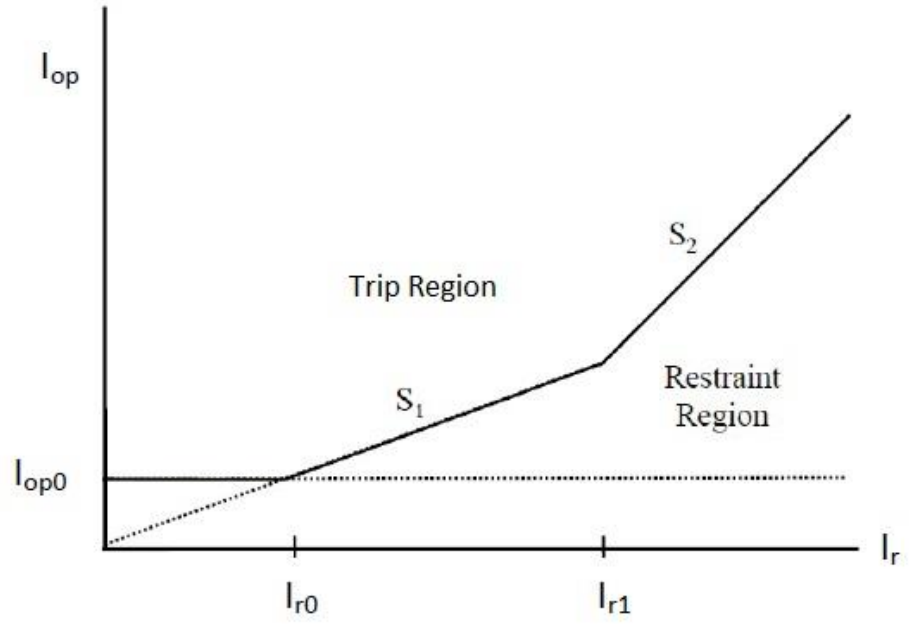

Figure 2.6: Characteristics curve of double slope restrained differential relay

The definition of operating current is

$$I_{op} = |I_1 + I_2 + \cdots + I_n| \tag{2.9}$$

n represents number of terminal of the zone to be protected.

There are several mathematical definitions of restrained current such as

$$I_r = 0.5(|I_1| + |I_2| + \cdots + |I_n|) \tag{2.10}$$

$$I_r = \max(|I_1|, |I_2|, \ldots |I_n|) \tag{2.11}$$

Usually, restrained current defined by Eq. (2.10) is most widely used. The characteristics of percentage restrained differential scheme can be expressed mathematically as follows:

$If\ I_r < I_{r0}$, then:

$$I_{op} > I_{op0} \rightarrow Trip$$

$$I_{op} < I_{op0} \rightarrow No\ Trip$$

$If\ I_{r0} \leq I_r \leq I_{r1}$, then:

$$I_{op} > S_1(I_r - I_{ro}) + I_{op0} \rightarrow Trip$$

$$I_{op} < S_1(I_r - I_{r0}) + I_{op0} \rightarrow No\ Trip$$

$If\ I_r > I_{r1}$, then:

$$I_{op} > S_1(I_{r1} - I_{ro}) + S_2(I_r - I_{r1}) + I_{op0} \rightarrow Trip$$

$$I_{op} < S_1(I_{r1} - I_{r0}) + S_2(I_r - I_{r1}) + I_{op0} \rightarrow No\ Trip$$

S_1 and S_2 are the slopes. The value of S_1 varies from 0.4 to 0.7 and value of S_2 varies from 0.5 to 0.75 [36]. I_{op0}, I_{ro} and I_{r1} are the relay settings and their values depend on system parameters.

2.2 Mathematical Modeling of CT Saturation

The circuit model of current transformer (CT) is shown in Figure 2.7.

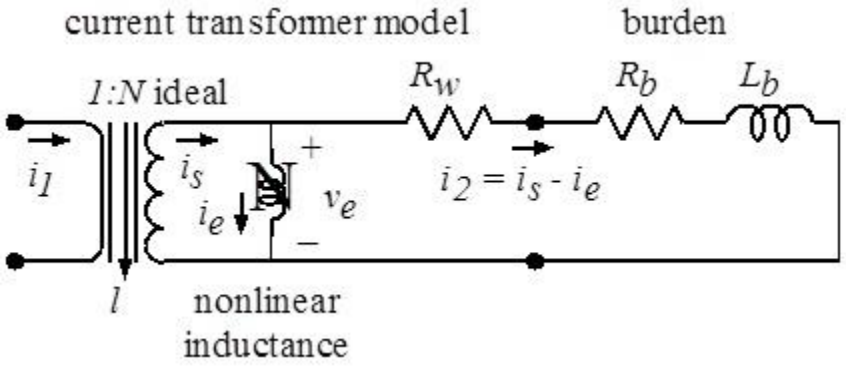

Figure 2.7: CT Circuit model [37]

The excitation characteristic of the CT is invariably a plot of secondary rms voltage versus secondary rms current, on log-log axes, as shown in Figure 2.8.

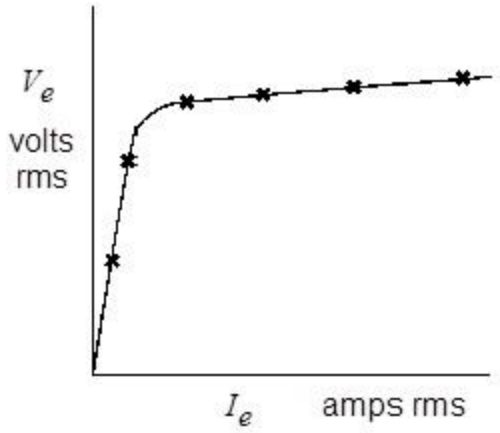

Figure 2.8: CT excitation curve [37]

Two parameters *S* and V_S can be extracted from the curve as shown in Figure 2.9.

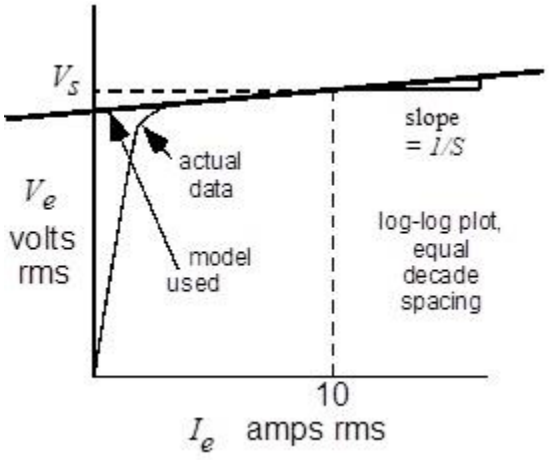

Figure 2.9: Method of determining the parameters V_s and *S* [37]

The reason for choosing the *saturation voltage,* V_s, at the point where the excitation current is ten amps, is that this is the definition used in the standard [37]. The straight line curve with slope 1/*S* shown in Figure 2.9 is not linear. It is a curve defined mathematically as

$$logV_e = \frac{1}{S} logI_e + logV_i \qquad (2.12)$$

where V_i is the value of V_e for I_e=1, that is for log I_e=0.

After removing the logs from both sides:

$$V_e = V_i I_e^{\frac{1}{S}} \tag{2.13}$$

In order to solve the circuit of Figure 2.7, the instantaneous λ (flux-leakage) versus i_e curve is required. It is postulated [37] that a curve defined as

$$i_e = A.\lambda^S \tag{2.14}$$

is suitable as long as the exponent S is an odd integer [37]. In order to allow S to be any positive number, and keep the function odd, the following expression can be used:

$$i_e = A.sgn(\lambda).|\lambda|^S \tag{2.15}$$

where sgn(λ) is the sign of λ as shown in See Figure 2.10 and A is a constant.

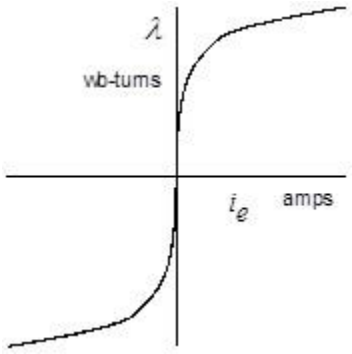

Figure 2.10: Postulated instantaneous values saturation curve [37]

The flux-linkages λ are related to the instantaneous excitation voltage v_e by Faraday's law [38] as

$$v_e = \frac{d\lambda}{dt} \tag{2.16}$$

The excitation curve is assumed as sinusoidal voltage, which implies that the flux-linkages are also sinusoidal

$$v_e = \sqrt{2}V_e \cos(\omega t) \tag{2.17}$$

$$\lambda = \int v_e dt = \int \sqrt{2}V_e \cos(\omega t)\, dt = \frac{1}{\omega}\sqrt{2}V_e \sin(\omega t) \tag{2.18}$$

The excitation current is non-sinusoidal, since it is a S^{th} order function of λ as

$$i_e = A\lambda^S = A\left[\frac{1}{\omega}\sqrt{2}V_e \sin(\omega t)\right]^S = A\left[\frac{1}{\omega}\sqrt{2}V_e\right]^S \sin^S(\omega t) \tag{2.19}$$

The rms value of this current is

$$I_e = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_e^2 dt} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} A^2\left[\frac{\sqrt{2}V_e}{\omega}\right]^{2S} \sin^{2S}(\omega t) dt}$$

$$= A\left[\frac{\sqrt{2}V_e}{\omega}\right]^S \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \sin^{2S}(\omega t) dt} \tag{2.20}$$

Now, the ratio of rms-value-to-peak-value of the excitation current can be defined as

$$RP = \frac{rms}{peak} \tag{2.21}$$

For a sinusoid RP=0.7071, and for i_e RP is given by

$$RP = \frac{\sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(\sqrt{2}I_e\right)^2 \sin^{2S}(\omega t)dt}}{\sqrt{2}I_e}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \sin^{2S}(\omega t)dt} \qquad (2.22)$$

The difference between *RP* for a sinusoid and *RP* the assumed excitation current waveform is illustrated in Figure 2.11. The factor *RP* gets smaller as the value of *S* increases.

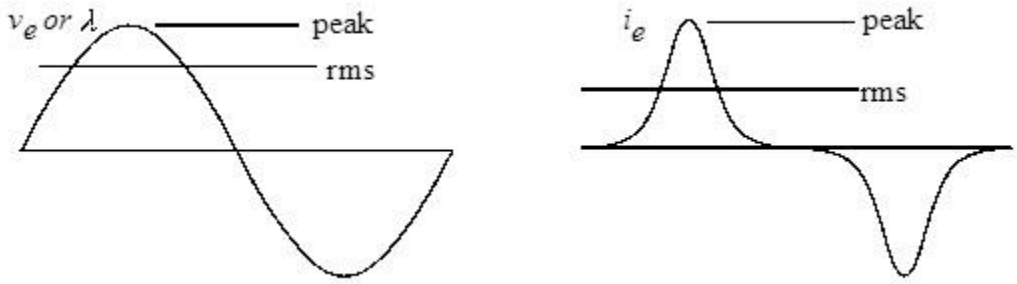

Figure 2.11: Comparison of the rms/peak relationship for two wave shapes [37]

Substituting the result Eq. (2.22) into Eq. (2.20), yields

$$I_e = A\left[\frac{\sqrt{2}V_e}{\omega}\right]^S RP \qquad (2.23)$$

As V_e=V_s when I_e=10 , substituting,

$$10 = A\left[\frac{\sqrt{2}V_s}{\omega}\right]^S RP$$

Solving for *A*:

$$A = \frac{10\omega^S}{\left(\sqrt{2}V_S\right)^S} \ \frac{1}{RP} \tag{2.24}$$

Substituting the value of A in Eq. (2.15), yields

$$i_e = sgn(\lambda)\frac{10\omega^S}{\left(\sqrt{2}V_S\right)^S} \ \frac{1}{RP} \ |\lambda|^S \tag{2.25}$$

Now, applying Kirchhoff's Voltage Law around the right-hand loop of the circuit in Figure 2.7, yields

$$v_e - (i_s - i_e)R_t - L_b\frac{d}{dt}[i_s - i_e] = 0 \tag{2.26}$$

The solution of i_s and its derivative are [36]:

$$i_s = \frac{i_1}{N} = \frac{\sqrt{2}I_p}{N}[Off.e^{-\frac{t}{\tau}} - \cos(\omega t - \cos^{-1} Off)]$$

$$\frac{di_s}{dt} = \frac{\sqrt{2}I_p}{N}[-\ \frac{Off}{\omega}.e^{-\frac{t}{\tau}} + \frac{1}{\omega}\cos(\omega t - \cos^{-1} Off)] \tag{2.27}$$

Where *Off* = per unit dc-offset magnitude and τ = system time constant.

Note that

$$\frac{di_e}{dt} = \frac{di_e}{d\lambda}.\frac{d\lambda}{dt} \tag{2.28}$$

$$\frac{di_e}{dt} = A.S.|\lambda|^{S-1} \tag{2.29}$$

Finally, with substitutions and manipulation, equation (2.26) can be re-written as

$$\frac{d\lambda}{dt}\left[1 + L_b A\, S\, |\lambda|^{S-1}\right] = -R_t i_e + R_t i_s + L_b \frac{di_s}{dt} \tag{2.30}$$

This first-order nonlinear differential equation is solved for *λ(t)* using standard numerical analysis techniques. Then the excitation current i_e is given by equation (2.14), and the actual secondary current is

$$i_2 = i_s - i_e \tag{2.31}$$

In case of the single-valued saturation curve, conventional remanence is not possible because non-zero λ cannot occur for zero i_e . However, remanence can be approximated very closely by simply assuming that the initial excitation current is non-zero. For convenience, λ_{rem} is expressed in per unit of V_s as shown in Figure 2.12.

$$\lambda_{rem} = \frac{x}{V_S} \tag{2.32}$$

In order to specify λ_{rem} accurately, x must be specified no greater than V_{knee} [37].

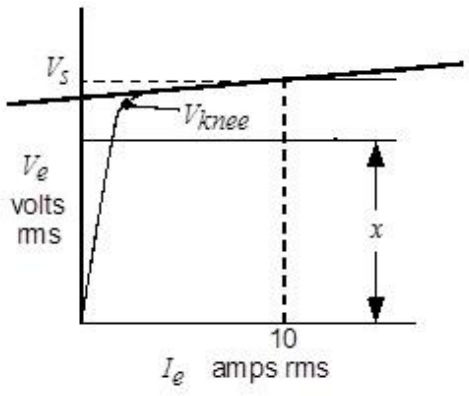

Figure 2.12: Definition of per unit remanence [37]

2.3 Existing Methods to Discriminate Internal and External Faults

Dual slope characteristic of percentage differential relay provides some protection against current transformer (CT) saturation; however, it is not enough for all practical external fault scenarios. Researchers have proposed various techniques and schemes to discriminate internal and external fault for providing more security for differential protection against CT saturation. Mathematical modeling of two latest methods is presented in this section.

2.3.1 Phase Angle Comparison Method

Phase Angle Comparison Method principle essentially monitors the phase angle relationships with the incoming and the outgoing currents of a protected zone. As implementing the phase angle in real time is a challenging task, the phase angles of the combination of various incoming and outgoing currents are executed in real-time using the dot-product method to compare whether the phase angle difference is within the threshold value to declare whether the fault is internal or external (Figure 2.13 & 2.14) to the zone of protection [13] [24] [39].

For two currents I_i & I_j, the dot product is

$$I_i . I_j = |I_i| \left|I_j\right| cos\theta_{ij}$$

$$cos\theta_{ij} = \frac{I_i \, . \, I_j}{|I_i| \, |I_j|} \tag{2.33}$$

Where, the term $cos\theta_{ij}$ directly indicates the phase difference between the two vectors. For n-terminals protected zone,

$$i \, , j = 1,2, \dots , n$$

If $cos\theta_{ij}$ is greater than a specific threshold value ($cos\theta_0$) for all combinations of *i* and *j,* then the metric of Equation 2.34 indicates existence of an internal fault.

$$cos\theta_{ij} > cos\theta_0$$

$$\frac{I_i \,.\, I_j}{|I_i|\,|I_j|} > cos\theta_0$$

$$I_i . I_j > |I_i|\,|I_j| cos\theta_0 \qquad (2.34)$$

Any phasor current with a magnitude less than a specific set value (I_0) is excluded from this algorithm.

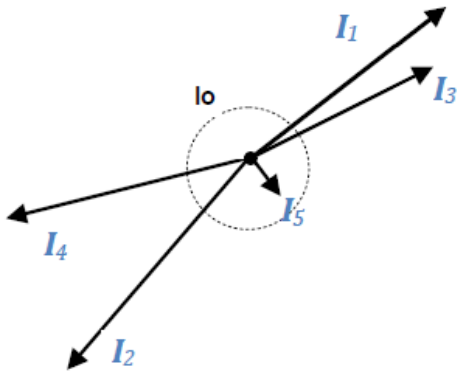

Figure 2.13: External Fault scenario

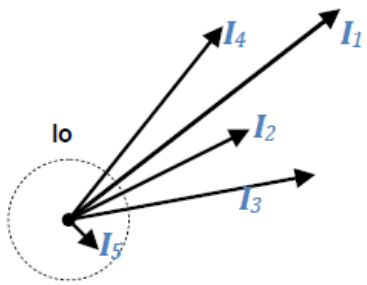

Figure 2.14: Internal Fault scenario

2.3.2 Differential Rate of Change Method (ROCOD)

During faults, operating current (I_{op}) and restrained current (I_r) change as Figure 2.15. From the trajectory of I_{op} and I_r during internal and external faults, it can be concluded that the rate of change of I_{op} is greater than the rate of change of I_r for an internal fault, whereas for external faults, the rate of change of I_{op} is less than the rate of change of I_r [24] [25] [39].

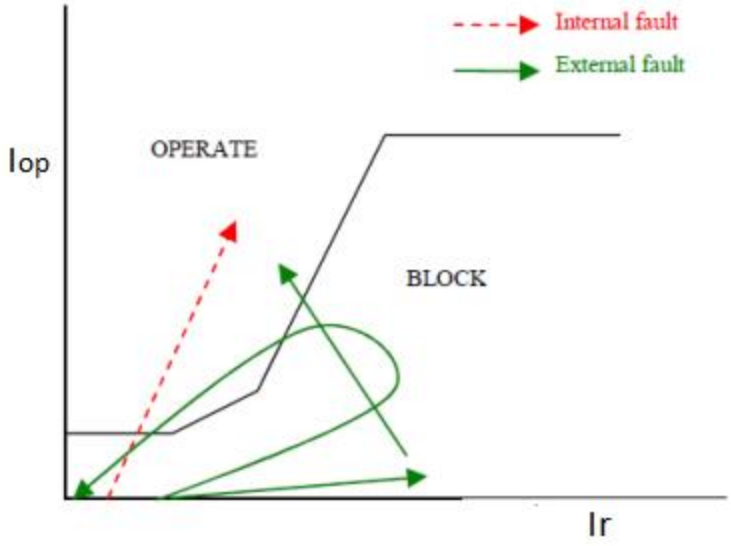

Figure 2.15: Trajectory of I_{op} and I_r [24]

Equation 2.35 indicates the condition for Internal Faults while External Faults satisfy Equation 2.36 when using ROCOD.

$$\frac{dI_{op}}{dt} > \frac{dI_r}{dt} \tag{2.35}$$

$$\frac{dI_{op}}{dt} < \frac{dI_r}{dt} \tag{2.36}$$

The detail logic of differential rate of change method is presented in Figure 2.16. To declare a fault as an internal fault, the fault needs to satisfy two conditions. First, the rate of change of operating current (I_{op}) as well as the rate of change of restraint current (I_r) must be the positive. To ensure this the rate of change of operating current (I_{op}) as well as the rate of change of restraint current (I_r) are compared with a small positive threshold value (I_{th}). Secondly, the rate of change of I_{op} must be greater than the rate of change of I_r .

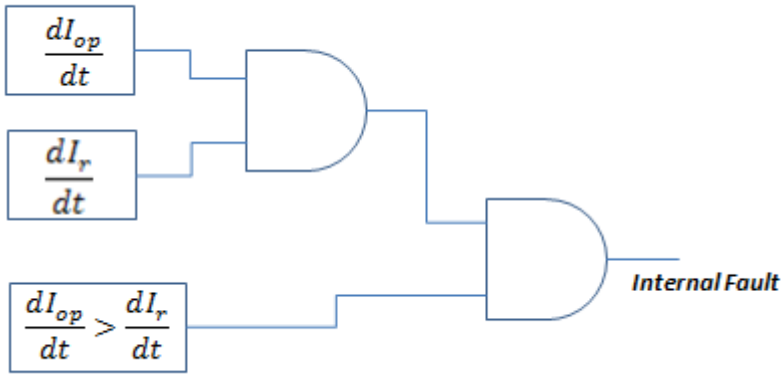

Figure 2.16: Logic Diagram of Differential Rate of Change Method

This chapter has covered the mathematical development of current differential protection which includes restraint characteristics. Mathematical modeling of CT saturation as well as two widely used fault discrimination methods has been described in details. The next chapter will cover the main contributions of this thesis which includes mathematical modeling of a proposed fault discrimination algorithm as well as the design details of a differential bus protection relay including proposed fault discrimination algorithm.

Chapter 3

3 Thesis Contributions

Chapter 2 has given the insight of differential protection principle, current transformer (CT) saturation, and existing techniques to discriminate internal and external faults. This chapter starts by describing the fault discrimination difficulties for low impedance current balanced differential protection schemes and explains a new methodology to address the issues. Finally, the design details of a differential bus protection relay are presented which includes proposed fault discrimination algorithm.

3.1 Problem Statement: Difficulties in Discrimination of Faults

The main concern with bus differential protection is to make it secure from mal-operation in response to the CT saturation during external faults. During external faults, when fault current becomes high, CT can get saturated. The CT saturation creates high operating current which causes the undesired operation of relay. The primary reason for such mal-operation is the fact that the traditional differential principle relies exclusively on current magnitude rather than directionality for tripping decisions.

There are several existing techniques to discriminate between internal fault and external fault for bus differential protection. CT saturation detection supervision is one of the earliest techniques, however, it fails to provide complete solution as CT can also be saturated during internal fault. Phase angle comparison is very widely used technique, although it has computational complexity when large numbers of input currents are involved. Moreover, during a high impedance internal bus fault, load flow may continue to flow on passive elements

which may cause the phase angles function to block the relay from tripping for the internal fault. The latest proposed method is based on rate of change of operating and restrained current which has limitation on fast CT saturation condition.

3.2 Objective

The main objective of this thesis is to come up with an effective algorithm to discriminate between internal and external faults. Based on this algorithm, a differential relay will be designed for bus protection which is capable of overcoming the impact of CT saturation. This thesis presents a new fault discrimination algorithm by defining partial operating current characteristics of a differential protection zone based on investigating its performance on busbar differential protection.

3.3 Mathematical Model of Partial Operating Current and Proposed Algorithm

In power system, differential protection zones are two types; two terminals such as transformer or transmission line and multi terminals such as busbar. Figure 3.1 shows a typical multi terminals protection zone which has three terminals. Terminal is a branch-circuit where transmission line or generator or load is connected. This is the single phase representation of a three phase system. Differential protection works on phase wise differential zone which means all elements of a zone must be in same phase. Although Figure 3.1 displays a zone with three terminal, physical zone may have more than three terminal which will be addressed in the later part of this section.

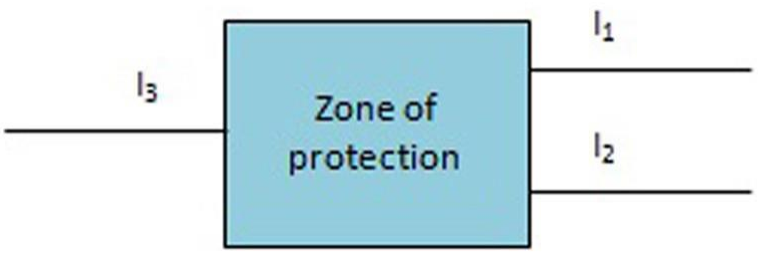

Figure 3.1: Single phase representation of a typical multi terminal protection zone

3.3.1 Mathematical Model of Partial Operating Current

The thesis includes introducing the concept of partial operating current from the terminal currents of a protection zone based on the definition of vector sum. The partial operating current phasors I_{op1} and I_{op2} for Figure 3.1 are defined as Equation (3.1) and Equation (3.2) respectively.

$$I_{op1} = I_1 + I_2 \tag{3.1}$$

$$I_{op2} = I_1 + I_2 + I_3 = I_{op1} + I_3 \tag{3.2}$$

In Equation (3.1) and Equation (3.2): I_1, I_2, and I_3 are the phasor currents of three terminals respectively. The magnitude and direction of any resultant partial operating current depends on the magnitude and direction of its two input currents. If both input currents leave the zone, then the resultant partial operating current will be greater than the larger one of its two input currents in magnitude and its direction will be out of zone. Similarly, if both input currents enter to the zone, then the resultant partial operating current will be greater than the larger one of its two input currents in magnitude and its direction will be towards the zone. However, if the input currents are in opposite direction which means one is toward zone and another one is out of zone, then the resultant partial operating current will be smaller than the

larger one of its two input currents in magnitude and its direction will be same as larger input current.

The operation of power systems are categorized as normal operation and fault conditions. Faults can be categorized further as internal fault to the protection zone and external fault to the protection zone. The characteristic metrics of newly defined partial operating current corresponding to the three operation categories are described next.

Metric 1: Normal operation: As stated in Kirchhoff Current Law, for normal operational condition the vector summation of the currents entering to a zone must be equal to vector summation of the currents leaving from the zone [35]. Figure 3.2 shows a protection zone in normal operating condition, where I_1 and I_2 are entering to the zone and I_3 is leaving from the zone. The partial operating currents $\mathrm{I}_{\mathrm{op1}}$ and $\mathrm{I}_{\mathrm{op2}}$ are presented as Equation (3.3) and Equation (3.4) respectively.

Figure 3.2: Normal operating condition

$$I_{op1} = I_1 + I_2 \tag{3.3}$$

$$I_{op2} = I_1 + I_2 + I_3 = I_{op1} + I_3 \tag{3.4}$$

Ideally, for normal operating condition, $\mathrm{I}_{\mathrm{op2}} = 0$. Figure 3.3 displays phasor representation of the terminal and partial operating currents. As displayed in the phasor

diagram of Figure 3.3, for normal operation, magnitude of I_{op1} is greater than the magnitude of I_1 as well as magnitude of I_2; however, magnitude of I_{op2} is less than the magnitude of I_{op1} as well as magnitude of I_3 which are mathematically described by Equation (3.5).

$$|I_{op1}| > \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max\left(\left|I_{op1}\right|, |I_3|\right) \tag{3.5}$$

Although Figure 3.2 displays a zone where I_1 and I_2 are entering to the zone and I_3 is leaving from the zone, current direction could be varied for a physical zone in normal operation. If we consider I_1 is entering the zone while I_2 and I_3 are leaving the zone, then the relation described in Equation (3.5) will appear as Equation (3.6)

$$|I_{op1}| < \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max\left(\left|I_{op1}\right|, |I_3|\right) \tag{3.6}$$

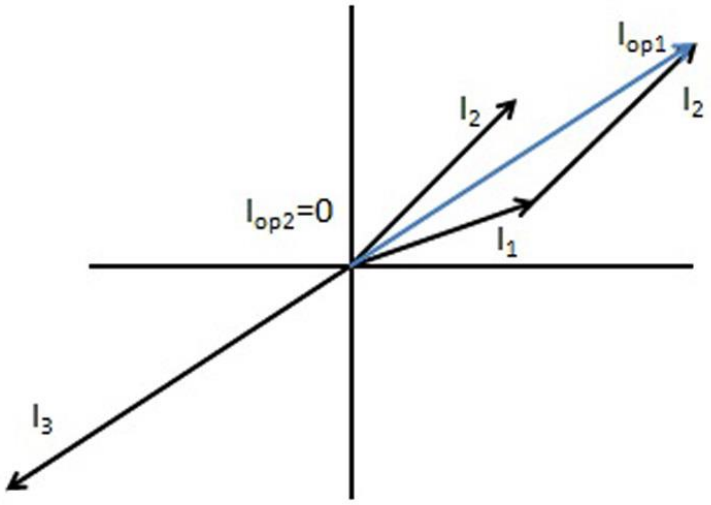

Figure 3.3: Phasor diagram in normal operational condition

Again, if we consider I_1 is leaving the zone while I_2 and I_3 are entering the zone, then the relation could be described by Equation (3.7).

$$|I_{op1}| < \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max\left(\left|I_{op1}\right|, |I_3|\right) \tag{3.7}$$

Similarly, it can be proved that at least one of the resultant partial operating currents I_{op1} or I_{op2} is smaller than the larger one of its two input currents for all possible combination of current direction in normal operation. Although the development is based on three terminal zone; the above statement is true for any number of input or output currents of a protection zone.

Metric 2: Internal Fault: If there is any fault within the zone which is called internal fault or in zone fault, currents through all terminals connected to the protection zone flow toward zone [6], [21]. As shown in Figure 3.4, all currents are following toward zone to feed the fault current which means currents measured by CTs are in same direction. According to the definition, two or more currents are in same direction when the maximum phase difference among them is less than 90 degree [13]. I_f is the phasor of fault current and for internal fault $I_{op2} = I_f$.

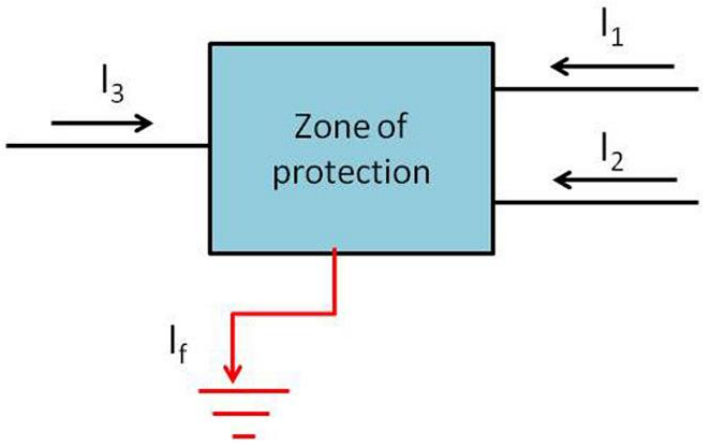

Figure 3.4: Internal fault condition

Figure 3.5 shows the phasor diagram of the currents during internal fault. According to the phasor diagram (Figure 3.5), magnitude of I_{op1} is greater than magnitude of I_1 as well as

magnitude of I_2 and magnitude of I_{op2} is greater than the magnitude of I_{op1} as well as magnitude of I_3 which are mathematically described by Equation (3.8).

$$|I_{op1}| > \max(|I_1|, |I_2|) \ and \ |I_{op2}| > \max(|I_{op1}|, |I_3|) \tag{3.8}$$

Equation (3.8) states that all of the resultant partial operating currents are simultaneously greater than the larger one of its two input currents for internal fault condition. This statement is true for any differential protection zone irrespective of terminal numbers.

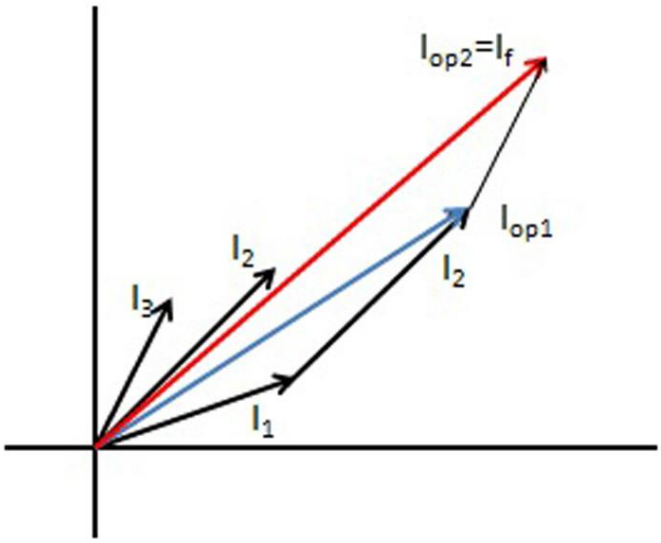

Figure 3.5: Phasor diagram during internal fault condition

Metric 3: External Fault: During external fault, current flows out-bound from the protection zone at least in one terminal [6], [21]. As shown in Figure 3.6, all currents except the current of faulted terminal are flowing toward zone to feed the fault current. Direction of the faulted terminal current is opposite to the other terminal currents. Normally $I_{op2} = 0$ for external fault condition, however, I_{op2} can be high due to CT saturation. When a CT saturates, the magnitude of the fundamental component of the secondary current decreases and its

phase angle advances [40]. Figure 3.7 and 3.8 show the phasor diagram of currents during external fault without CT saturation and with CT saturation respectively.

According to the phasor diagrams (Figure 3.7 and 3.8), magnitude of I_{op1} is greater than the magnitude of I_1 as well as magnitude of I_2 ; however, magnitude of I_{op2} is less than the magnitude of I_{op1} as well as magnitude of I_3 which are mathematically described by Equation (3.9).

$$|I_{op1|} > \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max(|I_{op1}|, |I_3|) \tag{3.9}$$

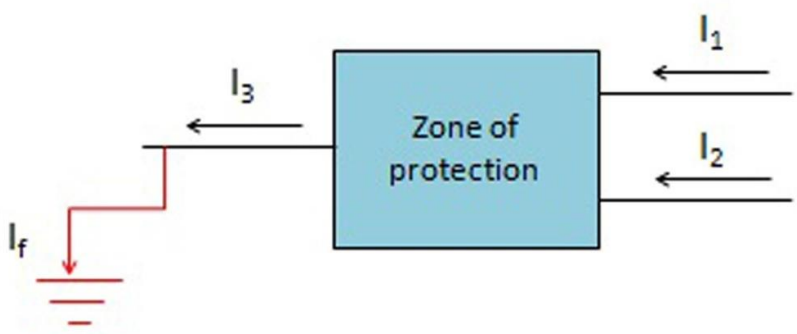

Figure 3.6: External fault condition

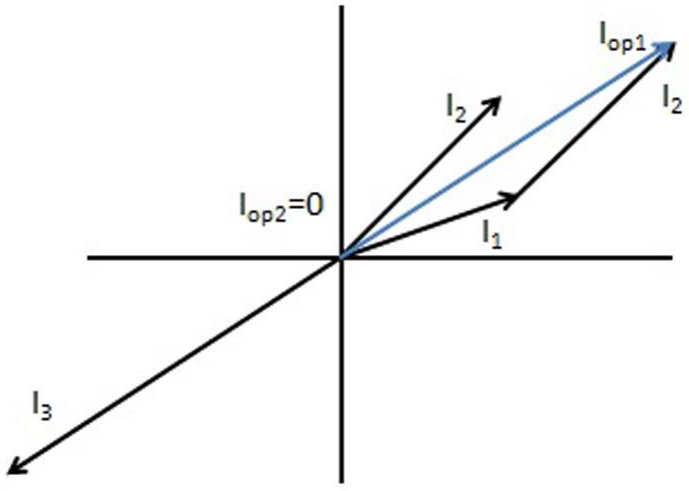

Figure 3.7: Phasor diagram during external fault condition without CT saturation

Although Figure 3.6 displays an external fault at terminal 3, faults could occur at any terminal of a physical protection zone. If we consider an external fault at terminal 1 of the zone shown in Figure 3.6, then the relation described in Equation (3.9) will change as Equation (3.10).

$$|I_{op1}| < \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max(|I_{op1}|, |I_3|) \tag{3.10}$$

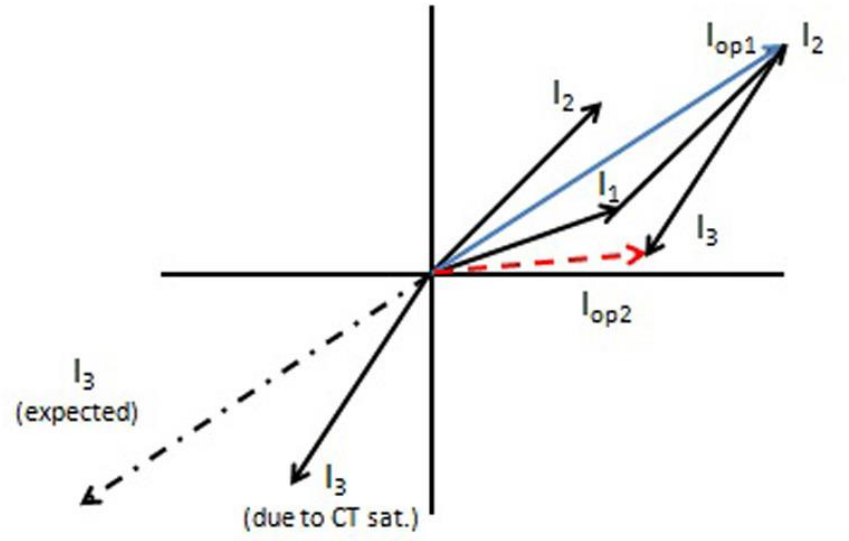

Figure 3.8: Phasor diagram during external fault condition with CT saturation

Similarly, for an external fault at terminal 2 of the zone shown in Figure 3.6, the relation could be described as Equation (3.11).

$$|I_{op1}| < \max(|I_1|, |I_2|) \ and \ |I_{op2}| < \max(|I_{op1}|, |I_3|) \tag{3.11}$$

From Equation (3.9), (3.10), and (3.11), it is obvious that at least one of the resultant partial operating current is smaller than the larger one of its two input currents for external fault condition. This statement is also true for any protection zone irrespective of terminal numbers.

3.3.2 Proposed Algorithm

The proposed fault discrimination algorithm is based on the characteristic metrics of the newly defined partial operating current of a protection zone. Above [Explain above] mathematical analysis shows that during internal fault, all of the resultant partial operating currents are simultaneously greater than the larger one of its two input currents as described in Equation (3.8). However, for normal operation and external fault condition statement of Equation (3.8) is violated. More generally, for n terminal zones, Equation (3.8) can be re-written as Equation (3.12).

$$
\begin{gathered}
|I_{op}1| > max(|I_1|, |I_2|), \\
and \\
|I_{op}2| > max(|I_{op}1|, |I_3|), \\
\ldots\ldots\ldots\ldots \\
\ldots\ldots\ldots\ldots \\
|I_{op}(n-2)| > max(|I_{op}(n-3)|, |I(n-1)|), \\
and \\
|I_{op}(n-1)| > max(|I_{op}(n-2)|, |In|).
\end{gathered}
\qquad (3.12)
$$

The characteristic described in Equation (3.12) will be known as ”internal fault condition” and could be applied to discriminate between external and internal faults of a differential protection zone effectively. Practically, all of the connected elements of a protection zone may not have active sources behind them or any line can be opened from far end. Load current or small charging current may continue to flow on these passive elements or opened line during fault. The current through the terminal less than a specific set value I_0 is considered as zero and excluded from partial operating current phasor calculation. The value of I_0 must be higher than the charging current of longest line connected to the zone. Flowchart of

the proposed fault discrimination algorithm is presented in Figure 3.9. The proposed algorithm is summarizes as follows:

- Take all connected terminal phasors as the input.
- Check the magnitude of each terminal phasor. If the magnitude of a terminal phasor is greater than I_0, tag the terminal as ”qualified terminal” and pass to partial operating current calculation; otherwise exclude it from partial operating current calculation.
- Check the number of total qualified terminal. If number of qualified terminal is zero, set output as ”no fault” and display. If the number of qualified terminal is one, set output as ”internal fault” and display. If the number of qualified terminal is more than one, check the ”internal fault condition”.
- If partial operating current characteristic obeys ”internal fault condition”, set output as ”internal fault” and display, otherwise set output as ”external fault” and display.

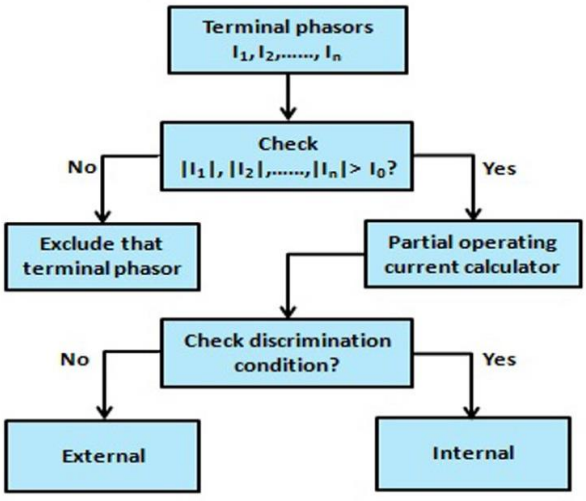

Figure 3.9: Flowchart of the proposed algorithm

3.4 Relay Design

As mentioned earlier, main objective of this thesis is to design fault discrimination scheme for bus differential protection which is capable of discriminating between internal and external faults to overcome the impact of CT saturation. In the previous section, a fault discrimination algorithm has been proposed based on the cumulative vector sum concept. In this section, a bus differential relay model has been presented by incorporating the proposed fault discrimination algorithm. The block diagram of the proposed relay is shown in Figure 3.10. The output of the CTs is instantaneous analog signal. A data processor is used to convert these analog signals to digital phasor form. Dual slope restrained characteristics is used to detect fault which is already described in section 2.1.3. Along with internal and external fault discrimination algorithm, a supervisory technique is included by using fast CT saturation detection algorithm to ensure high sensitivity for internal through fault (high impedance fault) condition. Detail working principle of data processor, CT saturation detection and trip logic unit will be presented in following sub-sections.

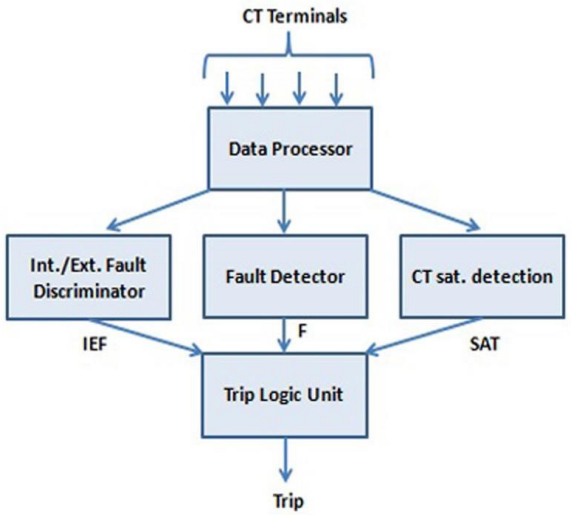

Figure 3.10: Block diagram of proposed relay

3.4.1 Data Processor

As the CT secondary currents are analog signals, they are sampled in a particular sampling rate to convert them into digital signals. In this model, the sampling frequency is 200 samples per cycle. From these digital signals, phasor values are extracted by using Discrete Fourier Transform (DFT) technique with a one cycle window. The DFT of a signal x is defined [41] by

$$X(\omega_k) \triangleq \sum_{n=0}^{N-1} x(t_n) e^{-j\omega_n t_n}, \qquad k = 0, 1, 2, \dots, N-1 \quad (3.5)$$

And its inverse is defined by

$$x(t_n) \triangleq \frac{1}{N} \sum_{n=0}^{N-1} X(\omega_n) e^{j\omega_n t_n}, \qquad n = 0, 1, 2, \dots, N-1 \quad (3.6)$$

3.4.2 CT Saturation Detection Algorithm

In this relay model, fast CT saturation detection algorithm and late CT saturation detection algorithm are considered [34] [42]. The outputs of the two algorithms are combined by OR logic to ensure the sensitivity of saturation detection logic for fast and late saturation conditions. Figure 3.11 shows the combined saturation detection algorithm.

Fast CT saturation algorithm has been developed based on the phase relationship of the second harmonic components of dI_{op}/dt and dI_r/dt. The estimated phase difference (O_d) between the second harmonic of dI_{op}/dt and dI_r/dt is compared with a threshold value(O_c).

$$O_d > O_c \rightarrow CT\ saturated$$

$$O_d \leq O_c \rightarrow CT\ not\ saturated$$

Fast CT saturation detection algorithm is shown in Figure 3.12.

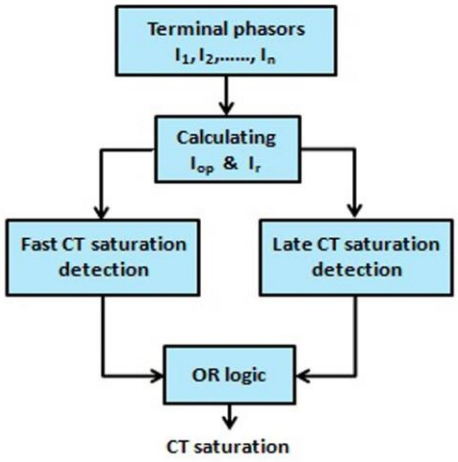

Figure 3.11: CT saturation detection algorithm

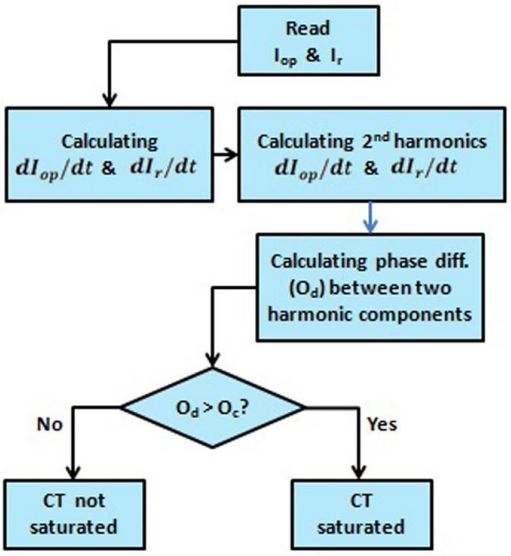

Figure 3.12: Fast CT saturation detection algorithm

The fast CT saturation detection algorithm is only effective when the CT saturation occurs in the first cycle after the fault inception. It cannot detect the late CT saturation. The late CT saturation is detected by using the Block Zone defined in Figure 3.13 (shaded region). This zone is bounded by $I_r = 2\ x\ I_{rs}$ and a line with 20% of slope which is passed through origin. The value of I_{rs} should be set a little bit greater than the maximum bus transfer load [34]. The fault level must be high enough to make the trajectory get into this zone for external fault with late CT saturation.

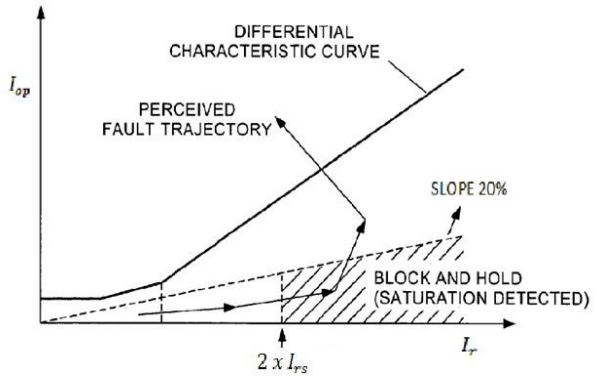

Figure 3.13: Trajectory of operating and restrained current [34]

3.4.3 Trip logic Unit

Trip logic unit is the final step of the relay modeling. It decides whether to trip or block based on the outputs of fault detector unit (F), internal-external fault discriminator unit (IEF) and CT saturation detection unit (SAT). The truth table for trip logic is shown on Table 3.1. The trip equation is defined as

$$Trip = \text{F AND NOT IEF AND NOT SAT OR F AND IEF}$$

Fault Type	Output of fault detector unit (F)	Output of internal-external fault discriminator unit (IEF)	Output of CT saturation detection unit (SAT)	Trip
No fault	0	0	0	0
No fault	0	0	1	0
No fault	0	1	0	0
No fault	0	1	1	0
High impedance internal fault	1	0	0	1
External fault	1	0	1	0
Internal fault	1	1	0	1
Internal fault	1	1	1	1

Table 3.1: The truth table for trip logic

The output of this logic is directly connected to the trip coils of all circuit breakers connected with the protected zone. The logic diagram is shown in Figure 3.14.

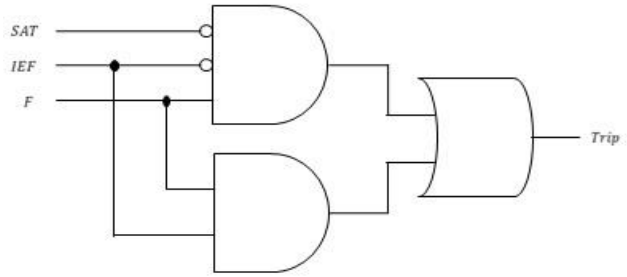

Figure 3.14: Trip logic diagram

This chapter has covered the mathematical modeling of a fault discrimination algorithm which has been proposed in this thesis. It has also described the design details of a differential bus protection relay including proposed fault discrimination algorithm. The next chapter will describe a test system where the proposed relay will be applied to check its performances.

Chapter 4

4.0 Test System

This chapter presents a three test system that is used to test the performance of the bus differential protection relay which is proposed in Chapter 3.

4.1 Description of the Test System

A three bus 230kV system is used to test the performance of the proposed bus differential protection scheme. The system has three generators, two transmission lines and three loads at three buses. The system is shown in Figure 4.1. The proposed relay is used at bus-1, where two transmission lines, one generator and one load are connected.

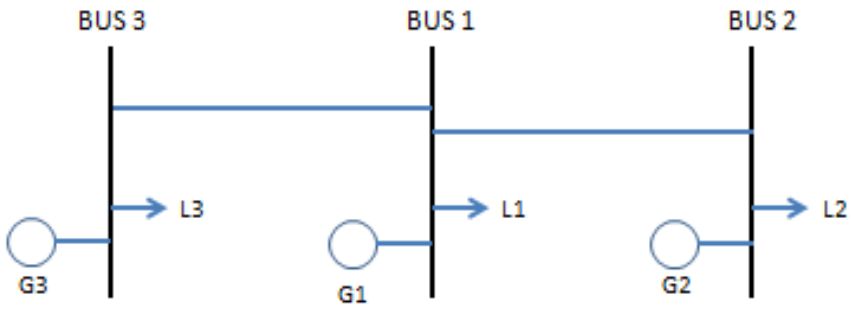

Figure 4.1: Three bus test system

4.2 Transmission Line Data

Transmission lines play a critical role in the generation of transients. The resistance, inductance and capacitance of overhead transmission lines are evenly distributed along the line length. Therefore, in general, they cannot be treated as lumped elements. Most electromagnetic transient programs contain two major categories of transmission line models:

- Constant parameter models
- Frequency-dependent parameter models

Constant-parameter distributed line model [43] is used in this test system. Detail data of the transmission lines are given in Table 4.1.

Line #	From Bus	To Bus	Length (Miles)	Diameter (Inches)	DC (Ω/Miles) resistance at 50˚C	Earth resistivity (Ω-m)
1	1	2	30	1.216	0.09222	50
2	1	3	75	1.216	0.09222	50

Table 4.1: Transmission line data [44]

Tower configuration of transmission lines are considered as same and described in Table 4.2.

Phase	Horizontal separation from reference (ft)	Height at tower (ft)	Height at mid span (ft)
A	0	100.00	73.00
B	0	83.50	56.50
C	0	67.00	40.00

Table 4.2: Transmission line tower configuration [44]

4.3 Generator Data

The following two generator models are the most commonly used in the protective relaying studies:

- Ideal sinusoidal sources behind sub-transient reactance or Thevenin impedances
- Detailed synchronous machine model

In this study, all three generators are modeled as ideal sinusoidal voltage sources behind Thevenin impedances. Detail data of the transmission lines are given in Table 4.3.

Generator #	Connected Bus	Line-line voltage (kV)	Positive sequence Impedance		Zero sequence Impedance	
			R (Ω)	X (Ω)	R (Ω)	X (Ω)
1	1	230	6.1	16.7	2.7	8.37
2	2	230	6.1	16.7	2.7	8.37
3	3	230	6.1	16.7	2.7	8.37

Table 4.3: Generator data [44]

4.4 Load Data

Detail data of the load are given in Table 4.4.

Load #	Connected Bus	Rated Voltage (kV)	Load (MW)	Load (MVAR)
1	1	230	45	21
2	2	230	45	21
3	3	230	45	21

Table 4.4: Load data

This chapter has covered a three bus test system including all system parameters such as generator data, transmission line data, and load data. The next chapter will describe the EMTP model of the test system, Matlab model of the proposed relay, simulation methodology, and finally the results with detail discussion.

Chapter 5

5.0 Simulation and Results

Chapter 5 includes the simulation methodology and the results found by using the Test System described in Chapter 4. The results found from proposed method are compared with two existing methods, namely, Phase Angle Comparison Method, and Rate of Change of Differential (ROCOD) Method. To perform simulation of the Test System, we need to build the system using Electromagnetic Transient Program (EMTP) and simulating by use of Matlab Program. Building the System Model and its simulation appear in Section 5.1 and 5.2.

5.1 EMTP Model

To test the proposed method, the three bus test system is built in EMTP as shown in Figure 5.1. Initially, power flow is solved to verify the validity of data. The power flow results are compared with Power System Analysis Framework (PSAF) model and POWER WORLD model. Differential bus protection works on phase wise differential zone which means all elements of a zone must be in same phase. EMTP model is built as three split phases where proposed relay is connected in phase A of bus 1. Four current transformers (CTs) are used in four branches connected with bus 1 to measure currents of those branches. Instantaneous ideal switches are used to create fault. For high impedance fault, 200Ω resistance is connected in series with the switch.

Modeling of current transformer is very important for testing the performance of any relaying system. Figure 5.2 shows the current transformer (CT) model that is used in this study to include the effect of CT saturation {45}. This model comprises of an equivalent circuit built

around an ideal transformer. CT parameters R_p, L_p, L_s, and inter-winding capacitance are very small which can be neglected [44]. In this study, inter-winding capacitance is neglected; however, R_p, L_p, and Ls are taken into consideration. R_b represents combined CT secondary winding resistance, lead resistance, and the CT burden. Values of CT parameters are given in table 5.1.

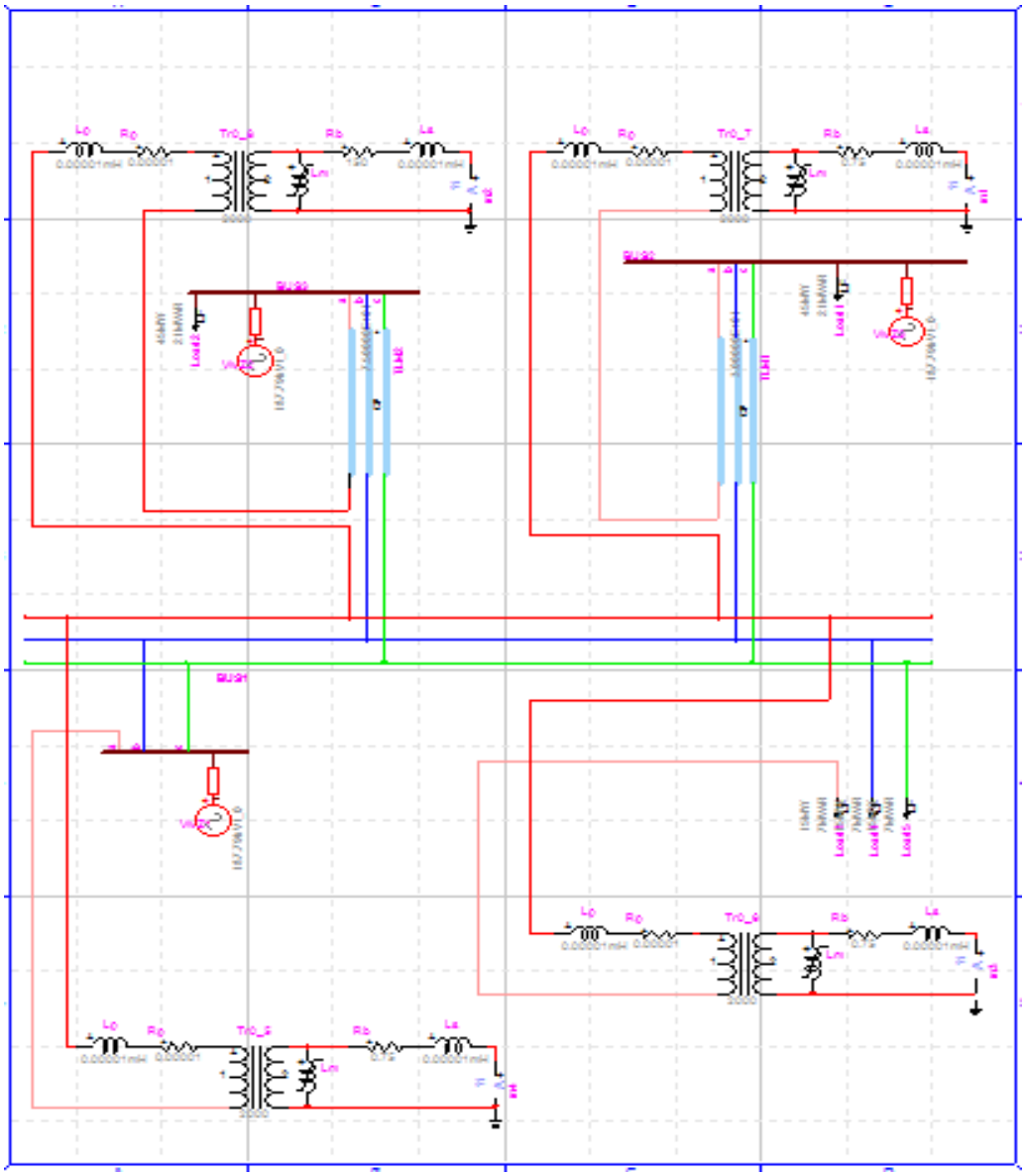

Figure 5.1: EMTP model of three bus test system

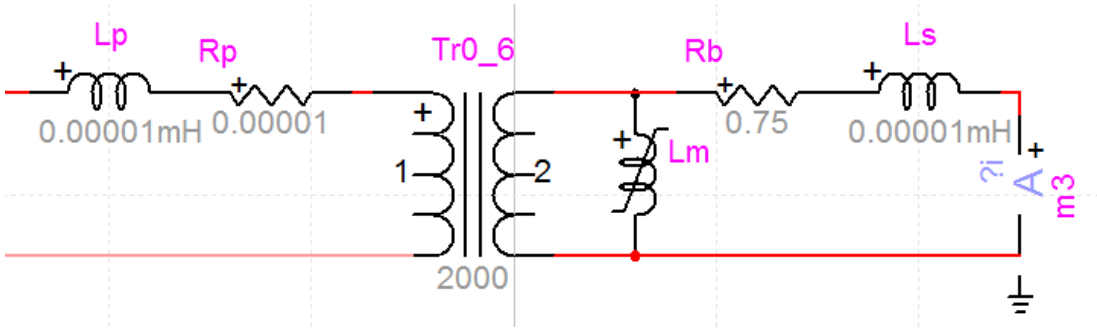

Figure 5.2: EMTP current transformer (CT) model

CT #	Measured Current	Connection point	Rp (Ω)	Lp (mH)	Rb (Ω)	Ls (mH)
1	i_1	At the branch between bus 1 and 2 (bus 1 side)	0.00001	0.00001	0.75	0.00001
2	I_2	At the branch between bus 1 and 2 (bus 1 side)	0.00001	0.00001	150	0.00001
3	i_3	At the branch between bus 1 and generator 1 (bus 1 side)	0.00001	0.00001	0.75	0.00001
4	i_4	At the branch between bus 1 and load 1 (bus 1 side)	0.00001	0.00001	0.75	0.00001

Table 5.1: CT parameters [43]

The burden of CT 2 is selected as high to capture the CT saturation. The CT ratio is 2000/1 for all current transformers.

The magnetizing branch can be located on the CT primary or secondary. Simulation results are identical in both cases. Location on the secondary is preferred because V-I curve measurements are regularly performed from the CT secondary. The magnetizing branch L_m is

represented by a nonlinear inductor element whose Ψ-I characteristic is specified in piecewise linear form Same Ψ-I characteristic is used for all four CTs as shown in Table 5.2.

Current	Flux
0.0198	0.2851
0.0281	0.6040
0.0438	1.1141
0.0565	1.5343
0.0694	1.8607
0.1025	2.2771
0.2167	2.6522
0.7002	3.0234
1.0631	3.1098
15.903	3.2261

Table 5.2: CT Ψ-I characteristic [44]

5.2 Matlab Model

The proposed relay in chapter 3 is modeled using Matlab. The proposed relay has three separate working blocks. Block 1 detects fault or abnormality in the system based on dual slope percentage restrained characteristics which has been described in section 2.1.3. Performance of this block depends on five setting values such as minimum pickup (I_{op0}), slope 1 (S_1), slope 2 (S_2), first transition point (I_{r0}) and second transition point (I_{r1}) . Table 5.3 shows the settings that are used in this study.

Block 2 is internal and external fault discriminator unit which has been described in detail in Section 3.3. A set value (I_0) is used to check the magnitude of each phasor current. If the magnitude of any phasor is less than I_0, it will be excluded from this algorithm. The value of I_0 is given in Table 5.3.

Block 3 is used to detect CT saturation. Detail of this block has been described in Section 3.4.2. This section has two sub-blocks. One of these sub-blocks is responsible for detecting fast CT saturation which depends on a threshold value O_c and the second sub-block is responsible for detecting late CT saturation. The late CT saturation is detected by using the Block Zone defined in Figure 3.12 (shaded region). This zone is bounded by $I_r = 2\ x\ I_{rs}$ and a line with 20% of slope which is passed through origin. The value of I_{rs} is given in Table 5.3.

I_{op0}	S_1	S_2	I_{r0}	I_{r1}	I_0	O_c	I_{rs}
0.5	50%	60%	0.2	1	0.2	12˚	1

Table 5.3: Settings for proposed relay [34] [46]

Another two relays are also modeled using Matlab based on exiting phase angle comparison method and ROCOD method. Same percentage restrained characteristic is used for three relays. The value of threshold current (I_0), threshold angle (θ_0) for phase angle comparison method are 0.2 and 80˚ respectively.

5.3 Bus Faults

Faults involved with power systems are mainly classified into two categories: symmetrical or balanced fault and asymmetrical or unbalanced fault. A fault which affects each of the three phases equally is called symmetrical fault. Symmetrical fault includes three phase fault (LLL) and three phase to ground fault (LLLG). An asymmetrical fault does not affect each of

the three phases equally. Asymmetrical fault includes phase to ground fault (LG), phase to phase fault (LL) and double phase to ground fault (LLG).

As a power system element, busbar can be affected by any one of the three mentioned faults. According to the location, faults can be classified as internal or in zone fault and external or out of zone fault. Faults listed in table 5.4 are considered in this study.

SL No.	Fault Name	Categories
1	Phase to ground (LG) internal fault	Asymmetrical
2	Phase to phase (LL) internal fault	Asymmetrical
3	Double phase to ground (LLG) internal fault	Asymmetrical
4	Three phase (LLL) internal fault	Symmetrical
5	Three phase to ground (LLLG) internal fault	Symmetrical
6	High impedance phase to ground (LG) internal fault	Asymmetrical
7	High impedance phase to phase (LL) internal fault	Asymmetrical
8	Phase to ground (LG) external fault	Asymmetrical
9	Phase to phase (LL) external fault	Asymmetrical
10	Double phase to ground (LLG) external fault	Asymmetrical
11	Three phase (LLL) external fault	Symmetrical
12	Three phase to ground (LLLG) external fault	Symmetrical

Table 5.4: List of bus faults

5.4 Results and Discussion

All twelve faults mentioned in Table 5.4 are simulated in EMTP model and measured currents were set as the input of Matlab relay models. Total simulation time is 250 milliseconds (ms) and fault is incepted at 50 ms. Measured currents for each fault and corresponding response of the proposed relay are presented graphically in this section. The comparative result found from three methods (proposed method and existing phase angle comparison and ROCOD methods) is also presented for each fault condition.

Phase to ground (LG) internal fault:

CT secondary currents (phase A only) for four branches during LG internal fault are shown in Figure 5.3. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are very low in comparison to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became zero as there was no active source at the other end of the load. However, currents through all other three branches were very high during fault due to having active sources behind them. The corresponding responses from the various components of proposed relay for LG internal fault are shown in Figure 5.4. The output of fault detector (F) became high (fault detected) within 1.5ms after fault inception. Also the output of internal-external fault detector (IEF) became high (internal fault detected) within 1.5ms after fault inception. However, the output of CT saturation detector remained low (no saturation) as there was no CT saturation during this LG internal fault. Finally, the trip output of the proposed relay (TRIP) became high (trip command issued) within 1.5ms as expected. The comparative results with other two existing methods are shown in Figure 5.5. The results show that the ROCOD

method as well as phase comparison method issued trip command at same time as the proposed method for this LG internal fault.

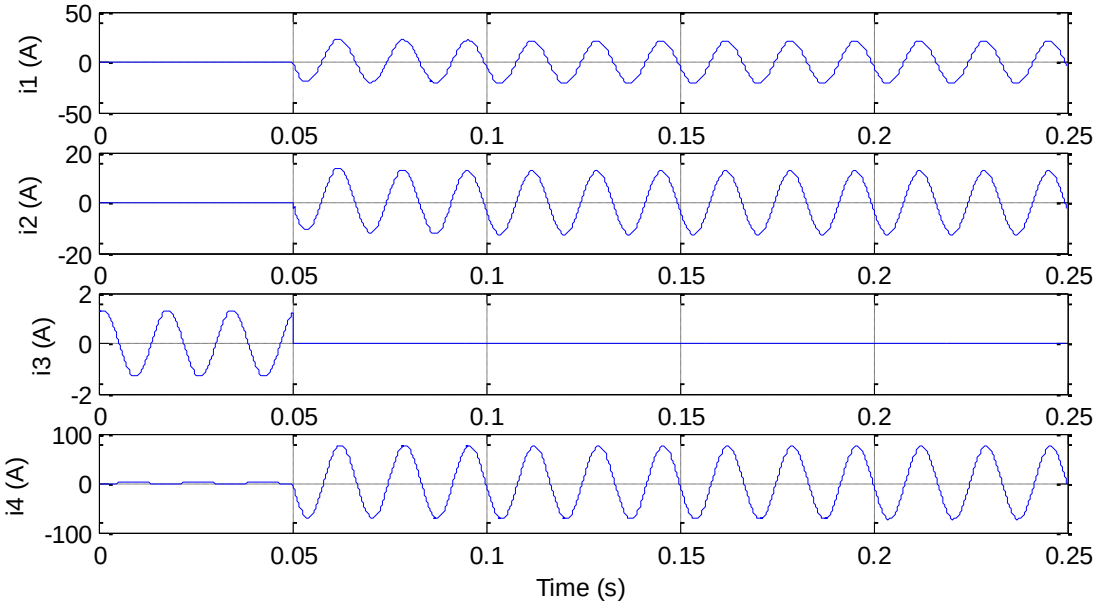

Figure 5.3: CT secondary currents for LG internal fault

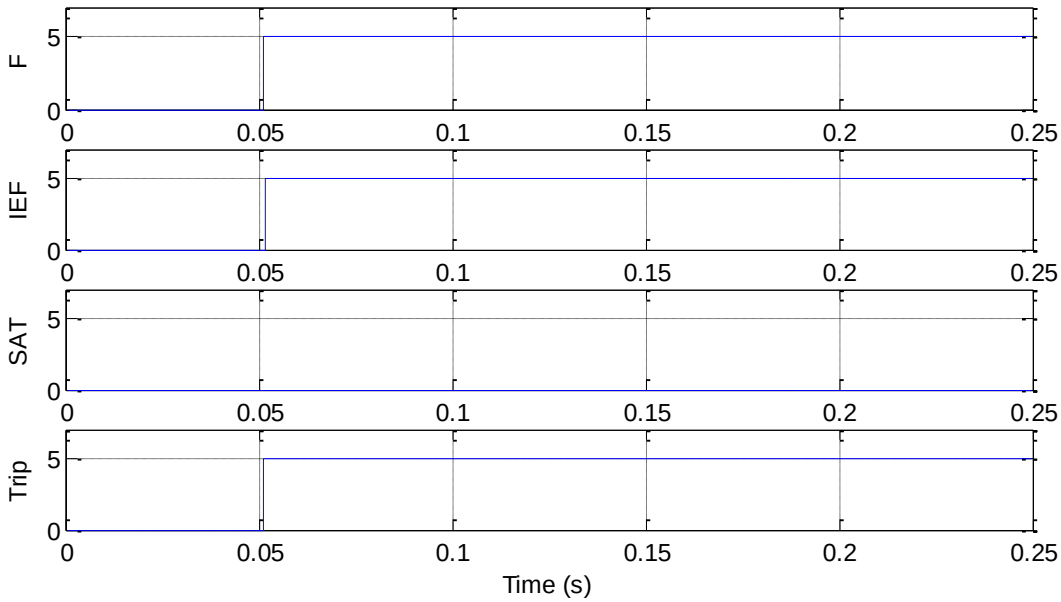

Figure 5.4: Responses from proposed method for LG internal fault

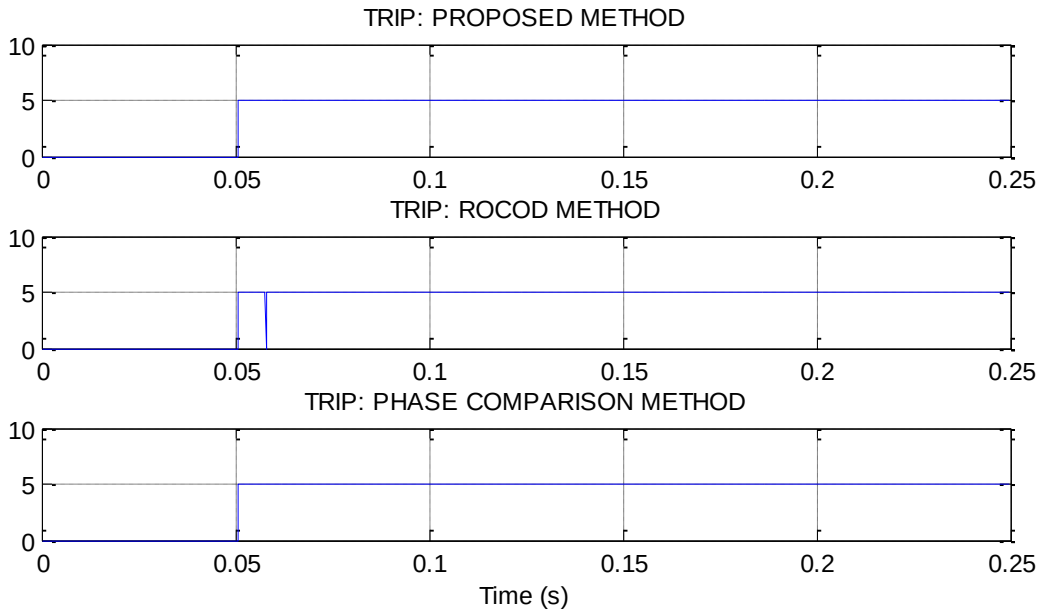

Figure 5.5: Comparative results for LG internal fault

Phase to phase (LL) internal fault:

CT secondary currents (phase A only) for four branches during LL internal fault are shown in Figure 5.6. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are very low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became low; however, not became zero even there was no active source at the other end of the load. This happened because there was no ground involvement during the LL fault. The currents through all other three branches were very high during fault due to having active sources behind them. The corresponding responses from the various components of proposed relay for LL internal fault are shown in Figure 5.7. The output of fault detector (F) became high (fault detected) within 1.5ms after fault inception; however, the output of internal-external fault detector (IEF) remained low (no internal fault) as the current through the load (i_3) was flowing out from bus and its magnitude was greater than I_0. The output of CT saturation detector remained low (no saturation) as there was no CT saturation during this LL

internal fault. However, the trip output of the proposed relay (TRIP) became high (trip command issued) within 1.5ms as expected. The comparative results with other two existing methods are shown in Figure 5.8. The results show that the ROCOD method issued trip command at same time as the proposed method for this LL internal fault; however, the phase angle comparison method did not issue trip command which is unexpected.

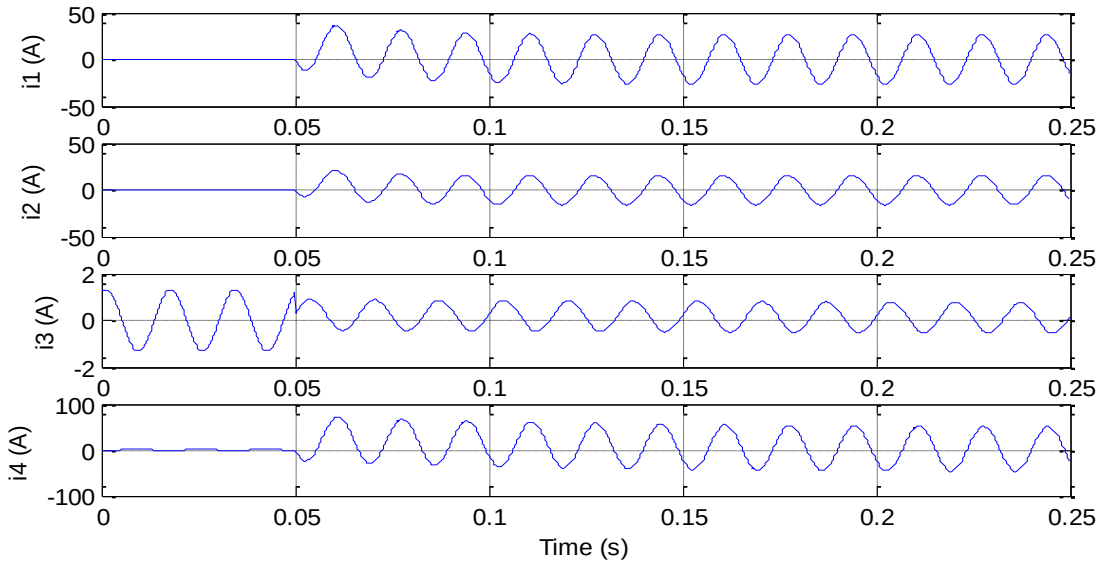

Figure 5.6: CT secondary currents for LL internal fault

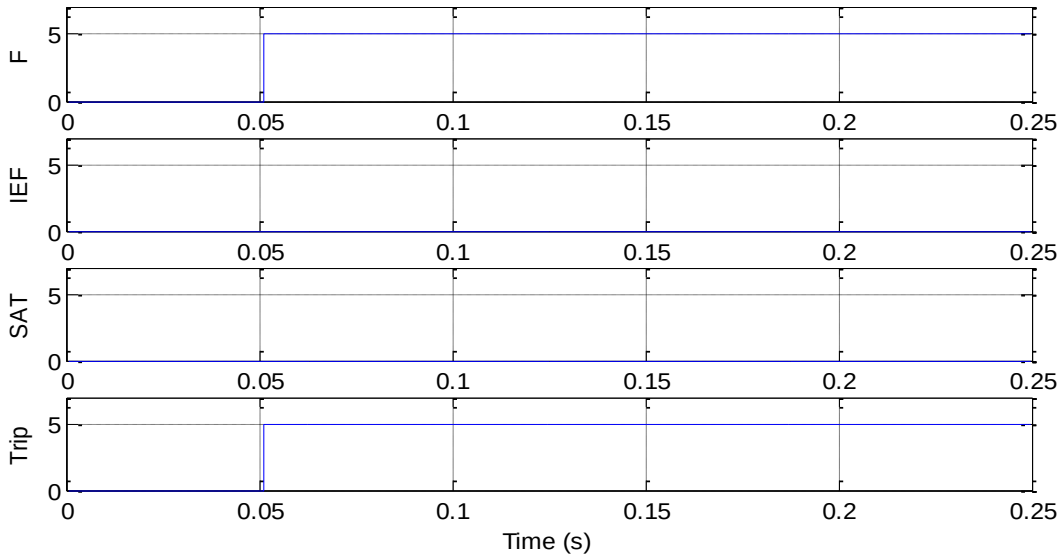

Figure 5.7: Responses from proposed method for LL internal fault

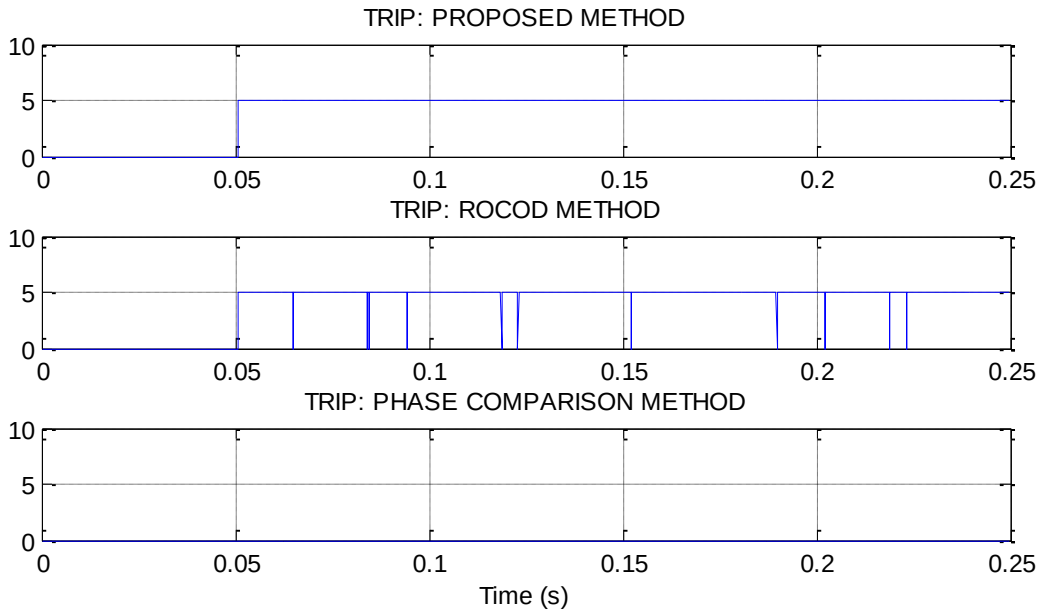

Figure 5.8: Comparative results for LL internal fault

Double phase to ground (LLG) internal fault:

CT secondary currents (phase A only) for four branches during LLG internal fault are shown in Figure 5.9. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are very low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became zero as there was no active source at the other end of the load. However, currents through all other three branches were very high during fault due to having active sources behind them. The corresponding responses from the various components of proposed relay for LLG internal fault are shown in Figure 5.10. The output of fault detector (F) became high (fault detected) within 1.5ms after fault inception. Also the output of internal-external fault detector (IEF) became high (internal fault detected) within 1.5ms after fault inception. However, the output of CT saturation detector remained low (no saturation) as there was no CT saturation during the above mentioned fault. Finally, the trip output of the proposed

relay (TRIP) became high (trip command issued) within 1.5ms as expected. The comparative results with other two existing methods are shown in Figure 5.11. The results show that the ROCOD method as well as phase comparison method issued trip command at same time as the proposed method for this LLG internal fault.

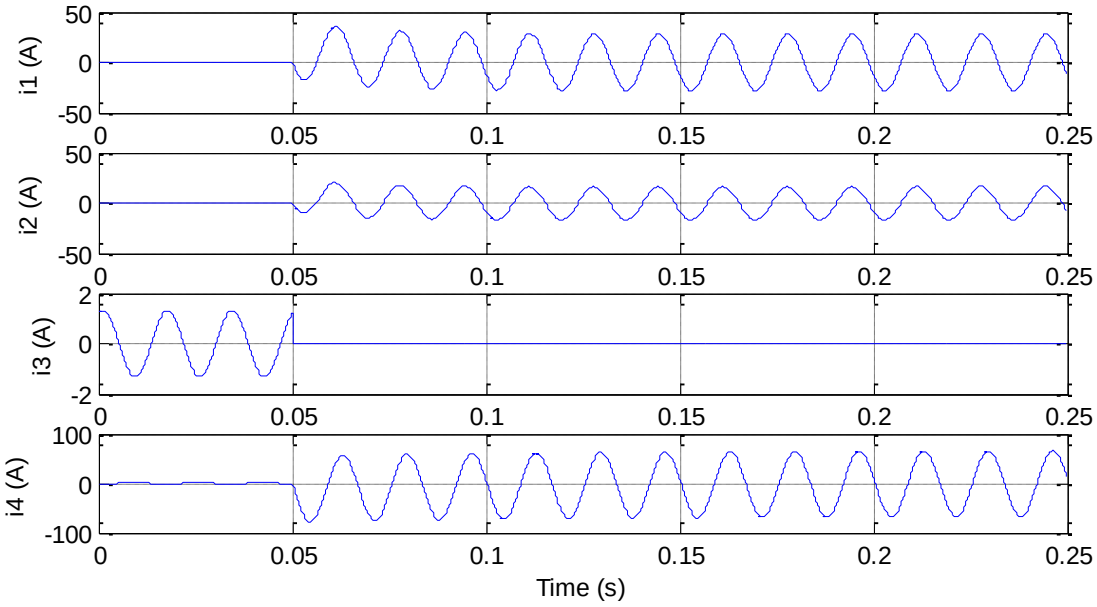

Figure 5.9: CT secondary currents for LLG internal fault

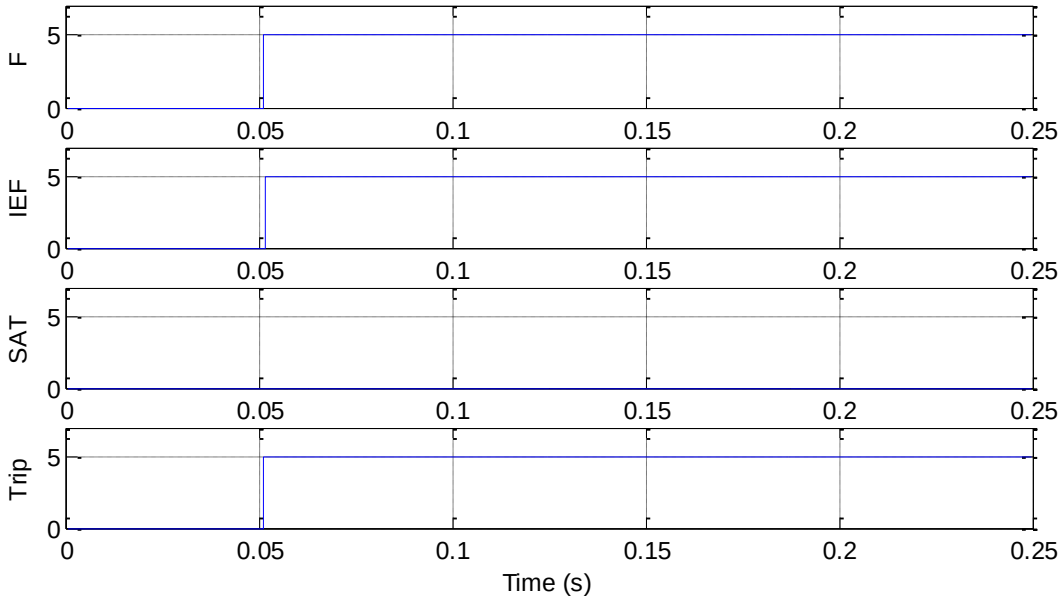

Figure 5.10: Responses from proposed method for LLG internal fault

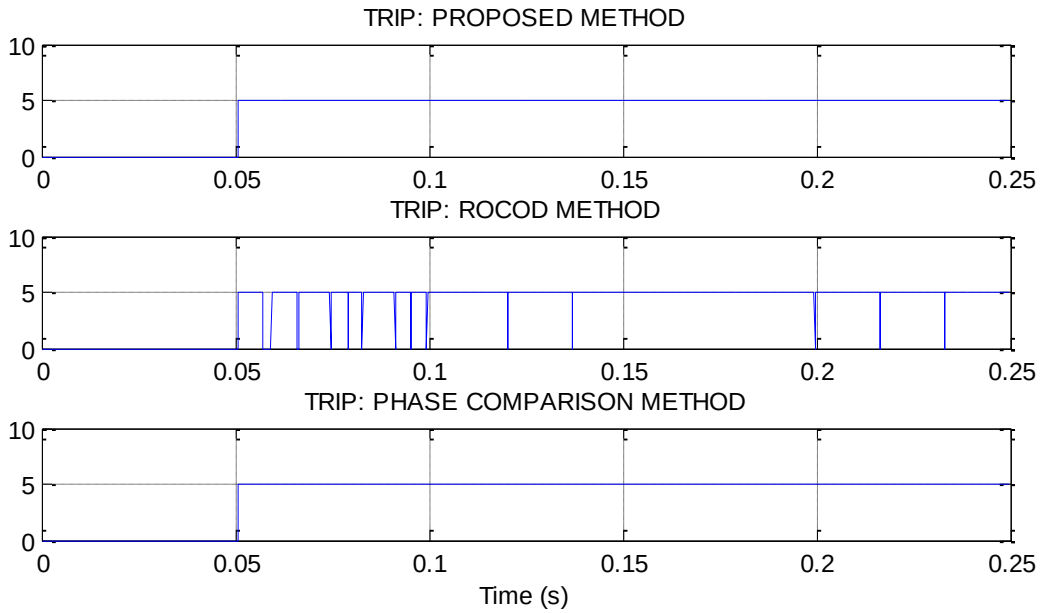

Figure 5.11: Comparative results for LLG internal fault

Three phase (LLL) internal fault:

CT secondary currents (phase A only) for four branches during LLL internal fault are shown in Figure 5.12. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are very low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became zero as there was no active source at the other end of the load. However, currents through all other three branches were very high during fault due to having active sources behind them. The corresponding responses from the various components of proposed relay for LLL internal fault are shown in Figure 5.13. The output of fault detector (F) became high (fault detected) within 1.5ms after fault inception. Also the output of internal-external fault detector (IEF) became high (internal fault) within 1.5ms after fault inception. However, the output of CT saturation detector remained low (no saturation) as there was no CT saturation during the above mentioned fault. Finally, the trip output of the proposed relay

(TRIP) became high (trip command issued) within 1.5ms as expected. The comparative results with other two existing methods are shown in Figure 5.14. The results show that the ROCOD method as well as the phase comparison method issued trip command at same time as the proposed method for this LLL internal fault.

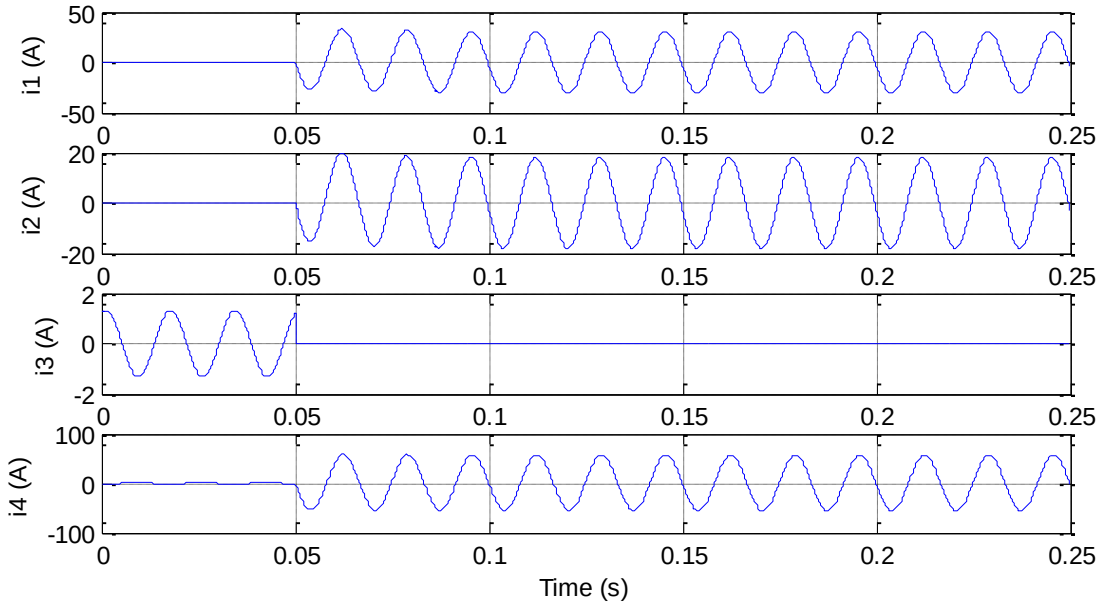

Figure 5.12: CT secondary currents for LLL internal fault

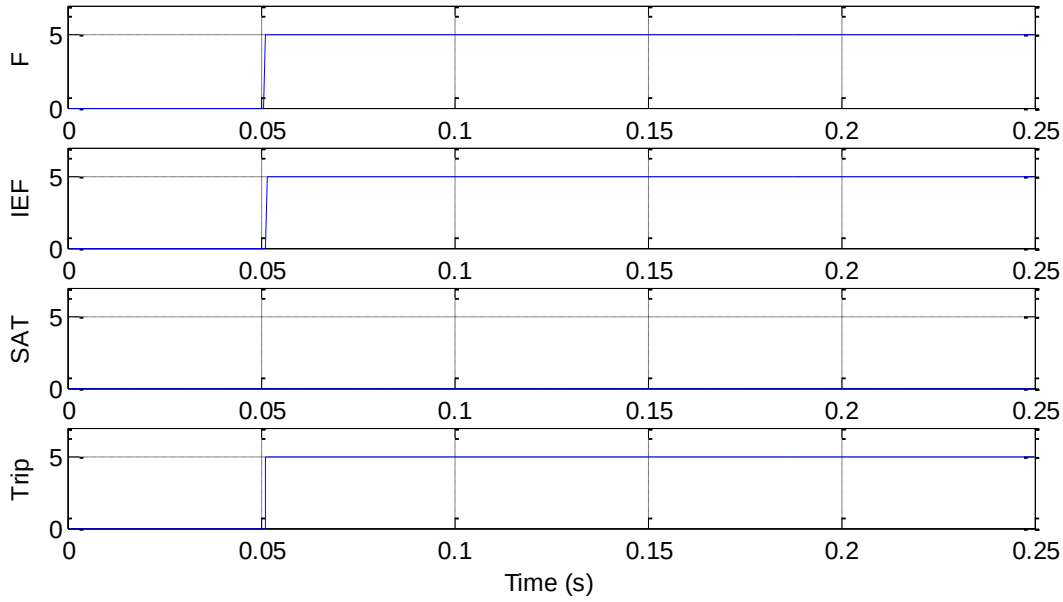

Figure 5.13: Responses from proposed method for LLL internal fault

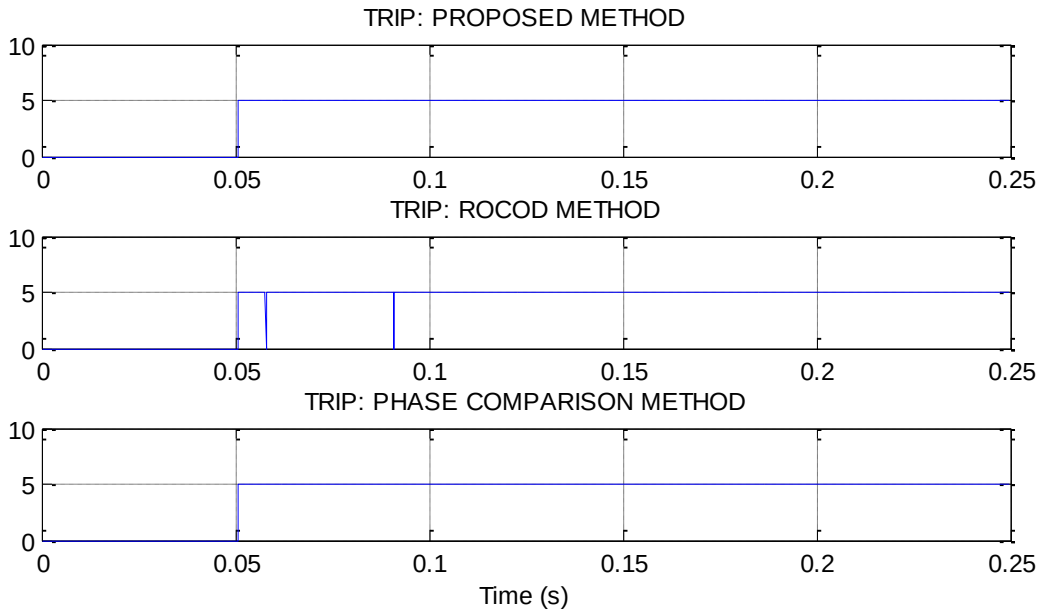

Figure 5.14: Comparative results for LLL internal fault

Three phase to ground (LLLG) internal fault:

CT secondary currents (phase A only) for four branches during LLLG internal fault are shown in Figure 5.15. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are very low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became zero as there was no active source at the other end of the load. However, currents through all other three branches were very high during fault due to having active sources behind them. The corresponding responses from the various components of proposed relay for LLLG internal fault are shown in Figure 5.16. The output of fault detector (F) became high (fault detected) within 1.5ms after fault inception. Also the output of internal-external fault detector (IEF) became high (internal fault detected) within 1.5ms after fault inception. However, the output of CT saturation detector remained low (no saturation) as there was no CT saturation during the above mentioned fault. Finally, the trip output of the proposed

relay (TRIP) became high (trip command issued) within 1.5ms as expected. The comparative results with other two existing methods are shown in Figure 5.17. The results show that the ROCOD method as well as the phase comparison method issued trip command at same time as the proposed method for this LLLG internal fault.

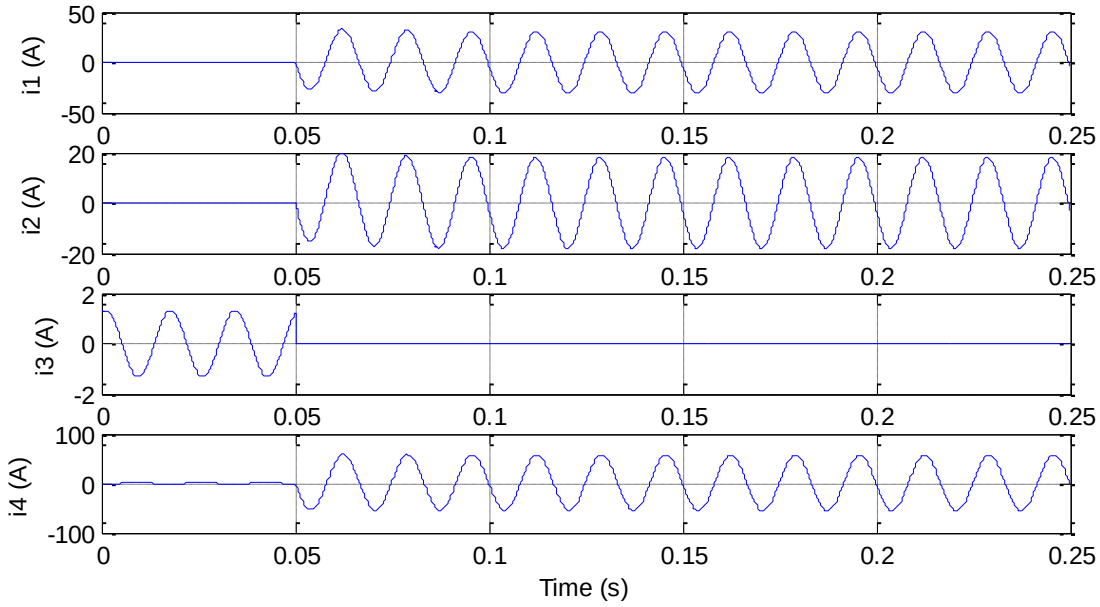

Figure 5.15: CT secondary currents for LLLG internal fault

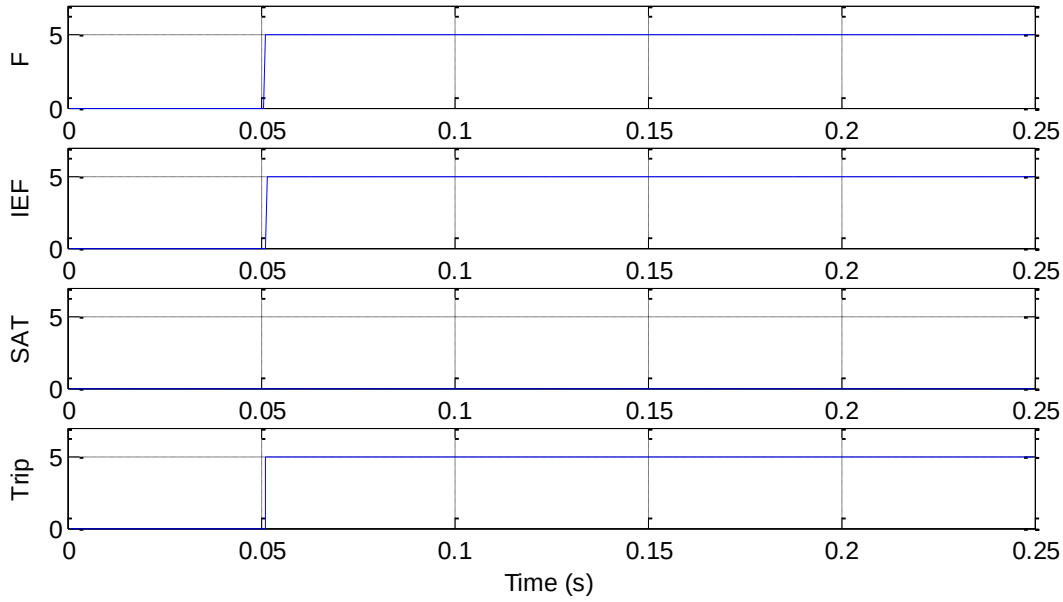

Figure 5.16: Responses from proposed method for LLLG internal fault

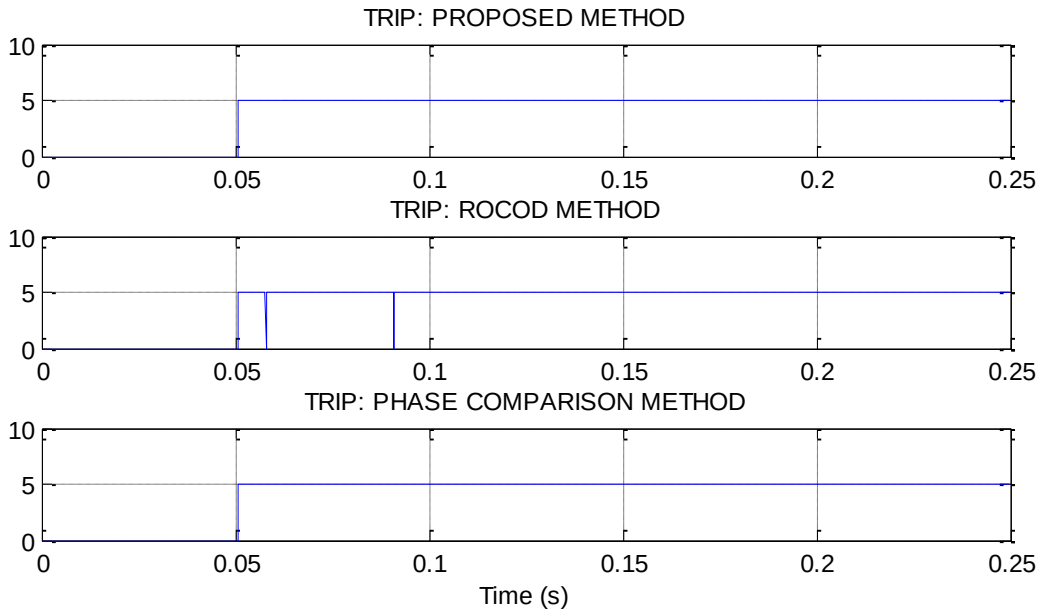

Figure 5.17: Comparative results for LLLG internal fault

Phase to ground (LG) high impedance internal fault:

CT secondary currents (phase A only) for four branches during LG high impedance internal fault are shown in Figure 5.18. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) was same as the current during normal operation even there was no active source at the other end of the load. This happened because the fault impedance was high as 200 Ohms. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LG high impedance internal fault are shown in Figure 5.19. The output of fault detector (F) became high (fault detected) within 4ms after fault inception. However, output of internal-external fault detector (IEF) remained low (no internal fault) as the current through the load (i_3) was flowing out from bus and its magnitude was greater than I_0. The

output of CT saturation detector also remained low (no saturation) as there was no CT saturation during the above mentioned fault. Even then the trip output of the proposed relay (TRIP) became high (trip command issued) within 4ms as expected. The comparative results with other two existing methods are shown in Figure 5.20. The results show that the ROCOD method issued trip command at same time as the proposed method for this LG high impedance internal fault; however, the phase angle comparison method did not issue trip command which is unexpected.

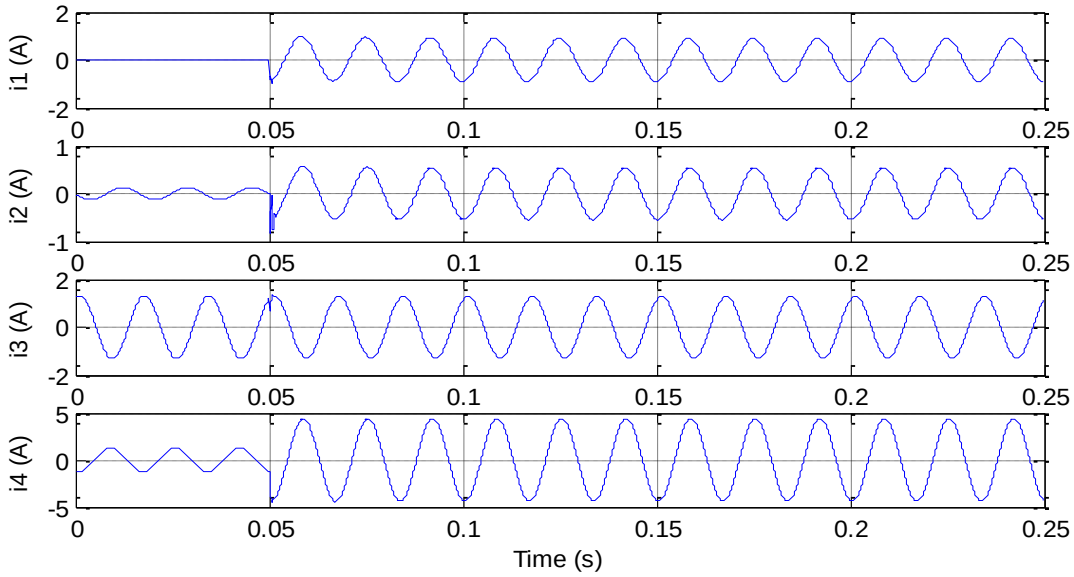

Figure 5.18: CT secondary currents for LG high impedance internal fault

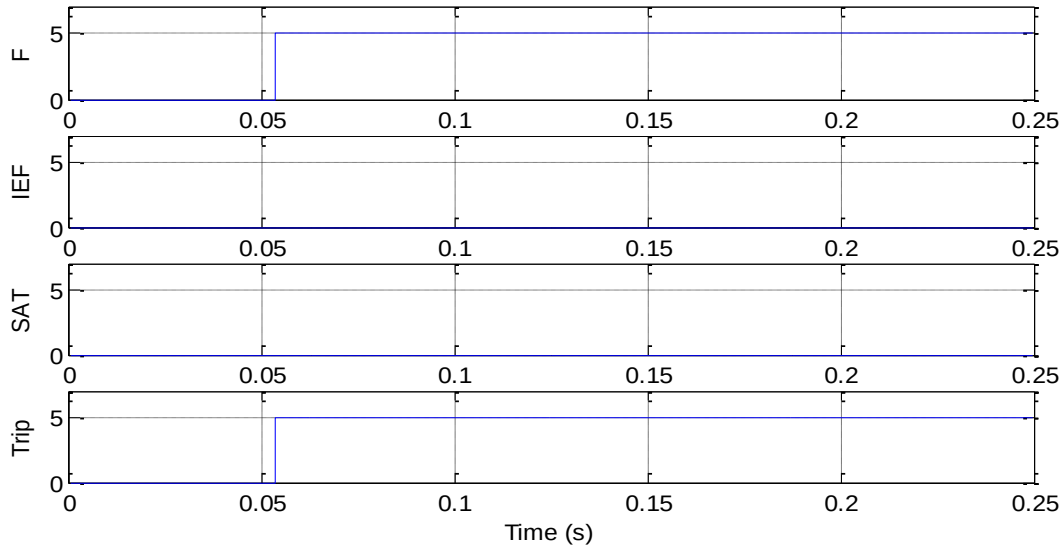

Figure 5.19: Responses from proposed method for LG high impedance internal fault

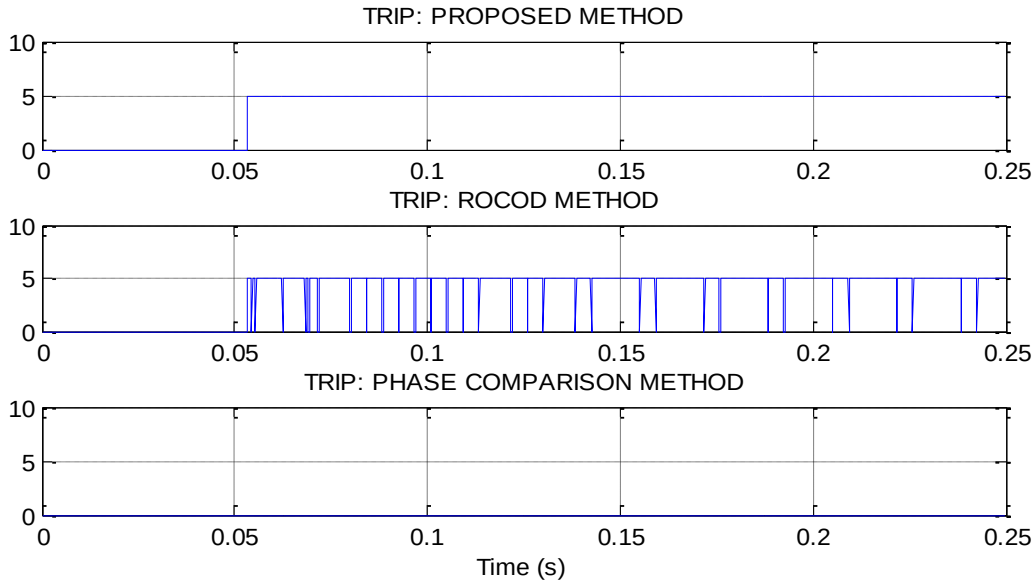

Figure 5.20: Comparative results for LG high impedance internal fault

Double phase to ground (LL) high impedance internal fault:

CT secondary currents (phase A only) for four branches during LL high impedance internal fault are shown in Figure 5.21. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) was same as the current during normal operation even there was

no active source at the other end of the load. This happened because the fault impedance was high as 200 Ohms. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LL high impedance internal fault are shown in Figure 5.22. The output of fault detector (F) became high (fault detected) within 2ms after fault inception. However, output of internal-external fault detector (IEF) remained low (no internal fault) as the current through the load (i_3) was flowing out from bus and its magnitude was greater than I_0. The output of CT saturation detector also remained low (no saturation) as there was no CT saturation during the above mentioned fault. Even then the trip output of the relay (TRIP) became high (trip command issued) within 2ms as expected. The comparative results with other two existing methods are shown in Figure 5.23. The results show that the ROCOD method issued trip command at same time as the proposed method for this LL high impedance internal fault; however, the phase angle comparison method did not issue trip command which is unexpected.

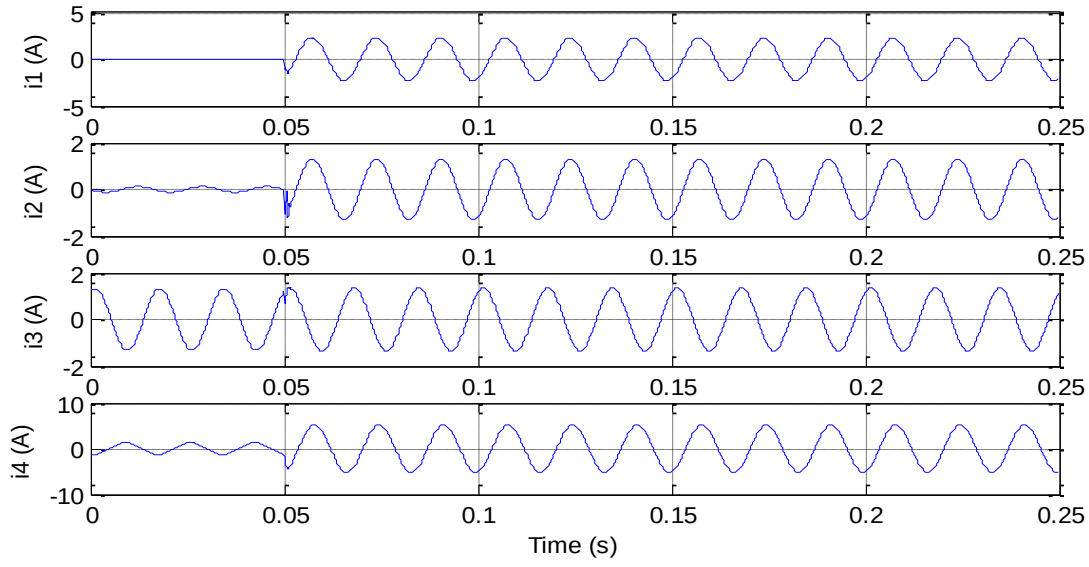

Figure 5.21: CT secondary currents for LL high impedance internal fault

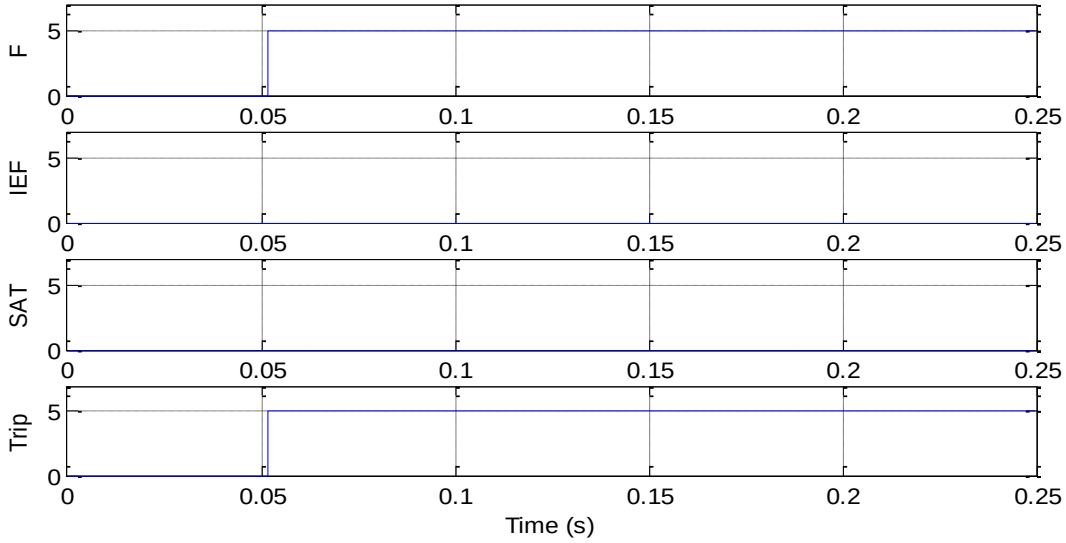

Figure 5.22: Responses from proposed method for LL high impedance internal fault

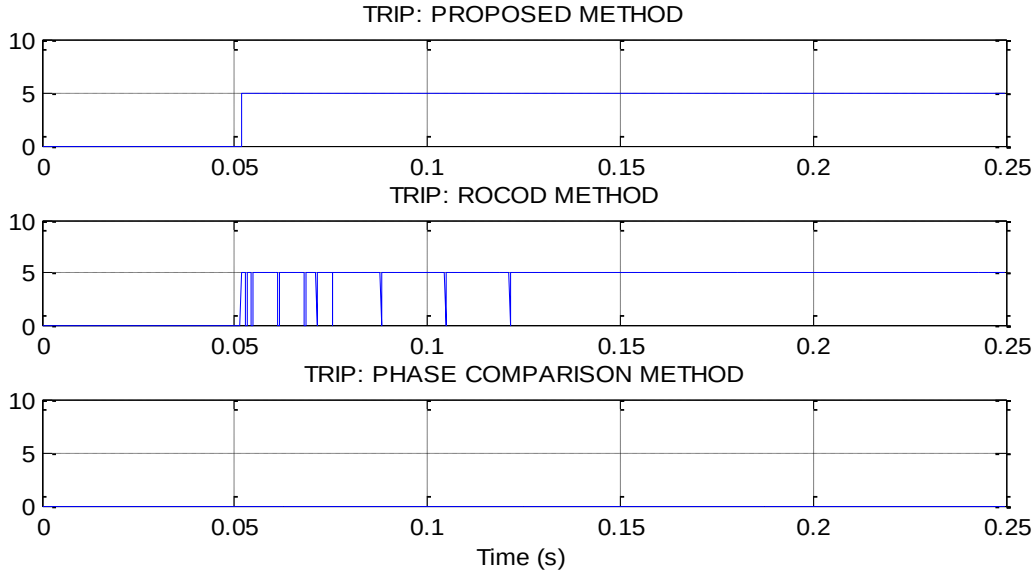

Figure 5.23: Comparative results for LL high impedance internal fault

Phase to ground (LG) external fault:

CT secondary currents (phase A only) for four branches during LG external fault are shown in Figure 5.24 where i_2 is distorted as the CT connected to that branch was saturated. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became close to zero as there was no active source at the other end of the load. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LG external fault are shown in Figure 5.25. The output of fault detector (F) became high (fault detected) within 6.5ms after fault inception even through the fault was incepted at out of zone (external fault). This was happened due to the resultant differential current from distorted i_2 because of CT saturation. However, output of internal-external fault detector (IEF) remained low (external fault) as i_2 was flowing out from bus. The output of CT saturation detector became high (saturated) as the CT connected to the branch 2 got saturated. Therefore, the trip output of the relay (TRIP) remained low (no trip command issued) as expected. The comparative results with other two existing methods are shown in Figure 5.26. The results show that the ROCOD method unexpectedly issued trip command after 6.5ms of fault inception for this LG external fault; however, the phase angle comparison method did not issued trip command which is harmonious with the proposed method.

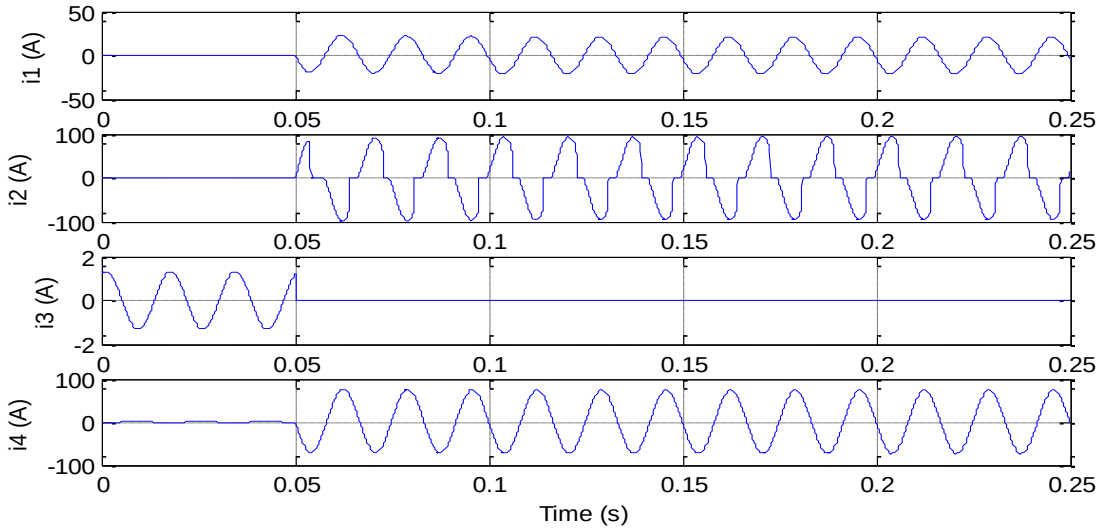

Figure 5.24: CT secondary currents for LG external fault

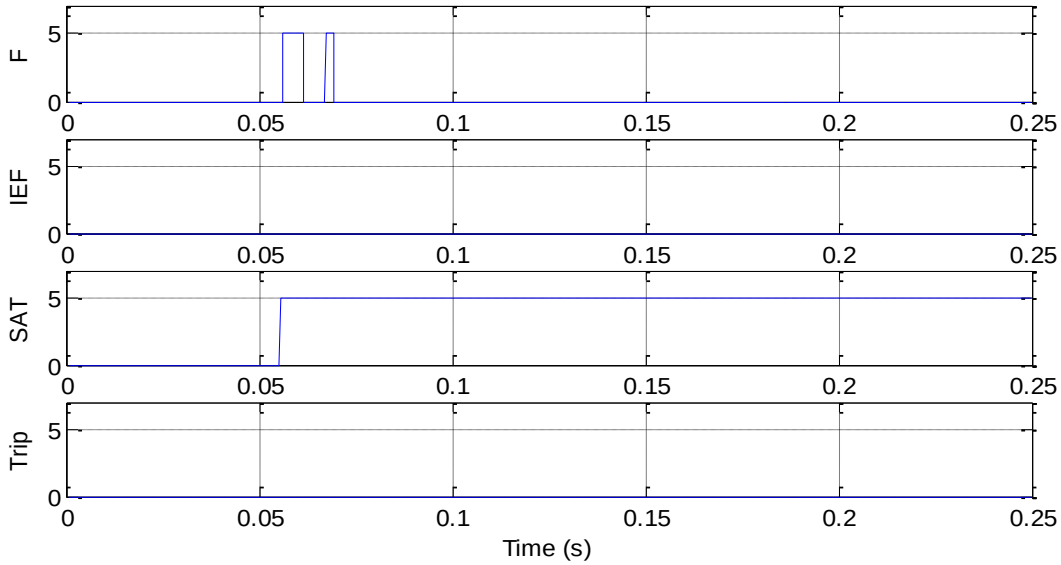

Figure 5.25: Responses from proposed method for LG external fault

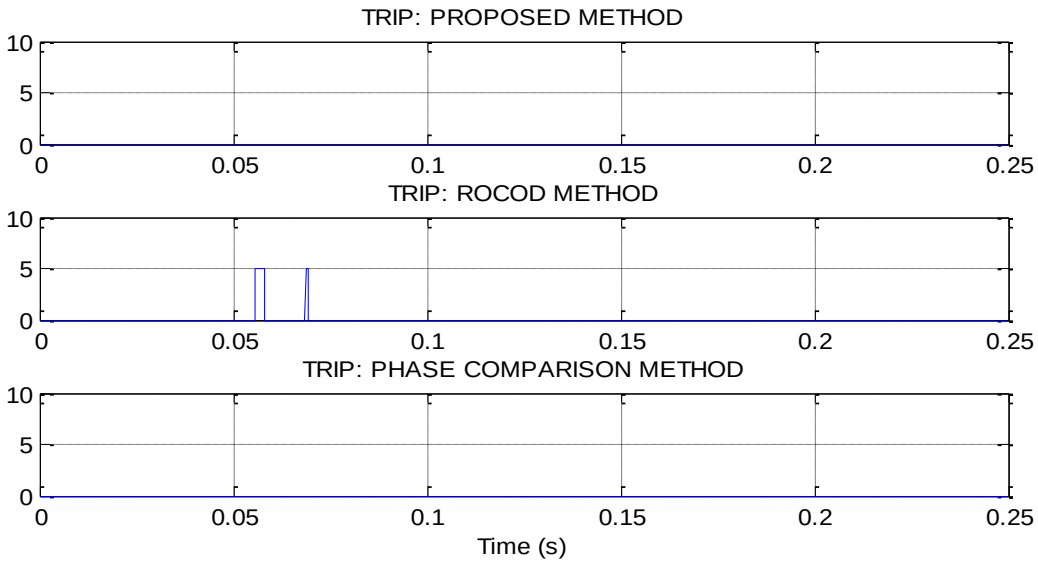

Figure 5.26: Comparative results for LG external fault

Phase to phase (LL) external fault:

CT secondary currents (phase A only) for four branches during LL external fault are shown in Figure 5.27 where i_2 is distorted as the CT connected to that branch was saturated. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, a small current through the load (i_3) was continuing to flow due to phase-to-phase (LL) fault. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LL external fault are shown in Figure 5.28. The output of fault detector (F) became high (fault detected) within 12ms after fault inception even through the fault was incepted at out of zone (external fault). This was happened due to the resultant differential current from distorted i_2 because of CT saturation. However, output of internal-external fault detector (IEF) remained low (external fault) as i_2 and i_3 were flowing out from bus. The output of CT saturation detector became high (saturated) as

the CT connected to the branch 2 got saturated. Therefore, the trip output of the relay (TRIP) remained low (no trip command issued) as expected. The comparative results with other two existing methods are shown in Figure 5.29. The results show that the ROCOD method unexpectedly issued trip command after 12ms of fault inception for this LL external fault; however, the phase angle comparison method did not issued trip command which is harmonious the proposed method.

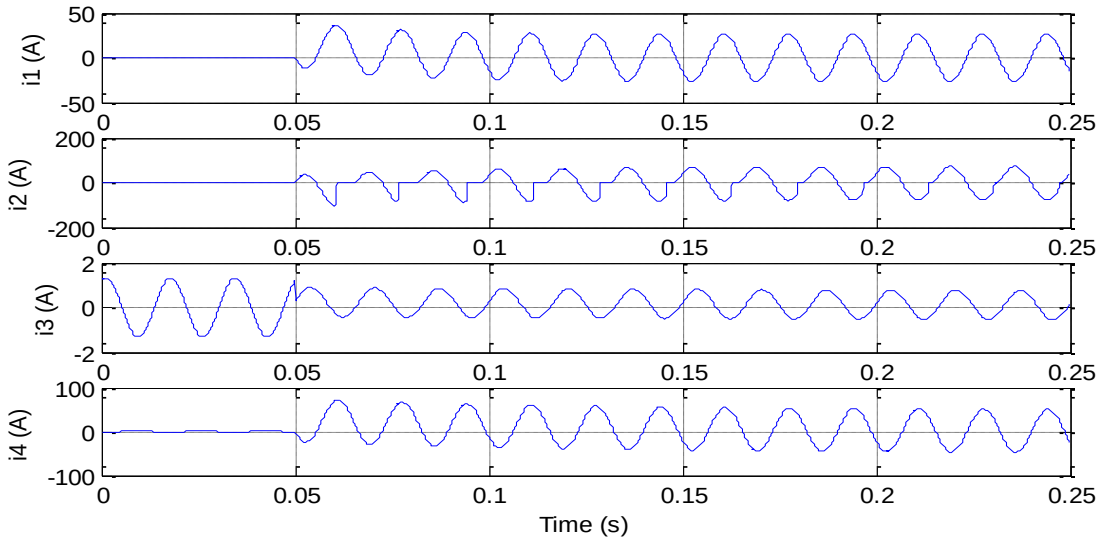

Figure 5.27: CT secondary currents for LL external fault

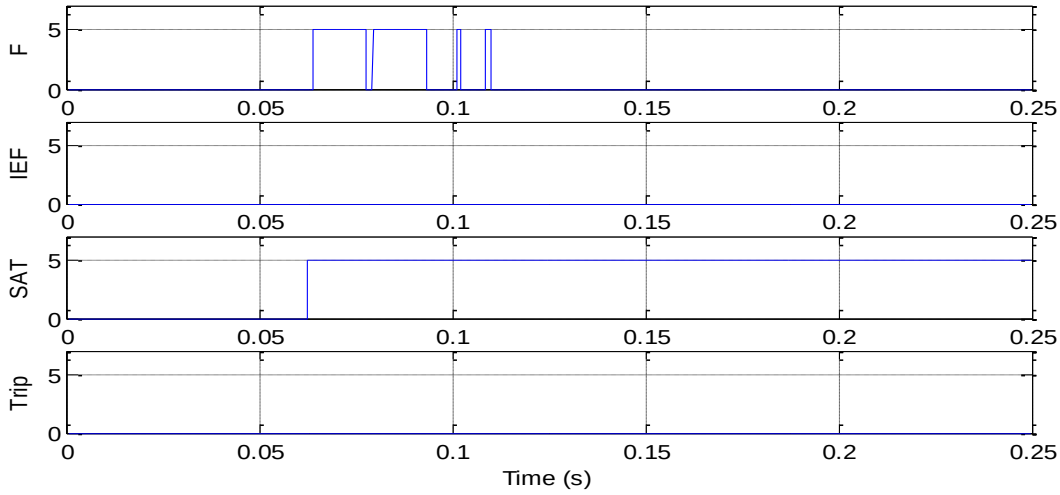

Figure 5.28: Responses from proposed method for LL external fault

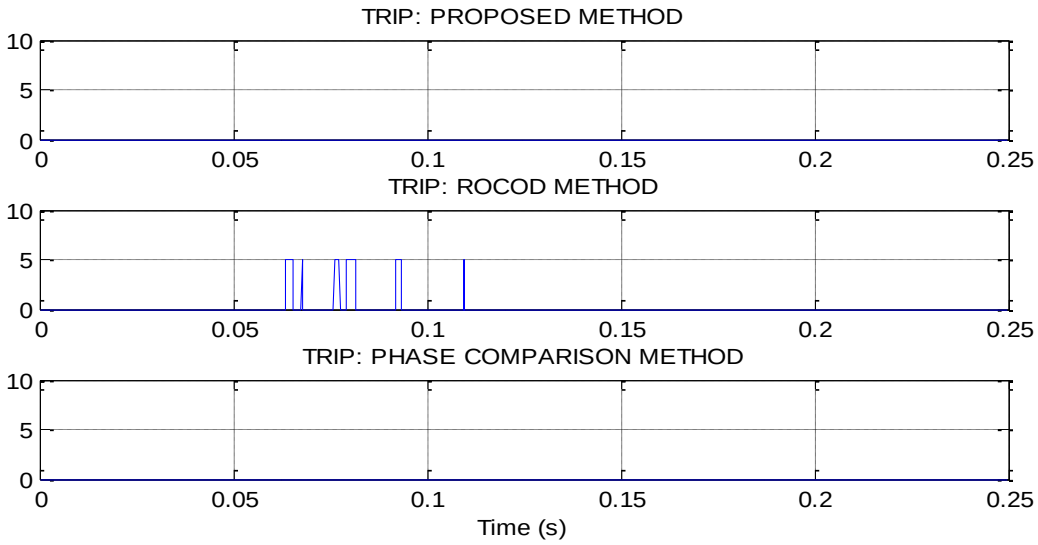

Figure 5.29: Comparative results for LL external fault

Double phase to ground (LLG) external fault:

CT secondary currents (phase A only) for four branches during LLG external fault are shown in Figure 5.30 where i_2 is distorted as the CT connected to that branch was saturated. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became close to zero as there was no active source at the other end of the load. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LLG external fault are shown in Figure 5.31. The output of fault detector (F) became high (fault detected) within 5.5ms after fault inception even through the fault was incepted at out of zone (external fault). This was happened due to the resultant differential current from distorted i_2 because of CT saturation. However, output of internal-external fault detector (IEF) remained low (external fault) as i_2 was flowing out from bus. The output of CT saturation detector became high (saturated) as the CT connected to the branch 2 got saturated. Therefore, the trip output of the

relay (TRIP) remained low (no trip command issued) as expected. The comparative results with other two existing methods are shown in Figure 5.32. The results show that the ROCOD method unexpectedly issued trip command after 5.5ms of fault inception for this LLG external fault; however, the phase angle comparison method did not issued trip command which is harmonious with the proposed method.

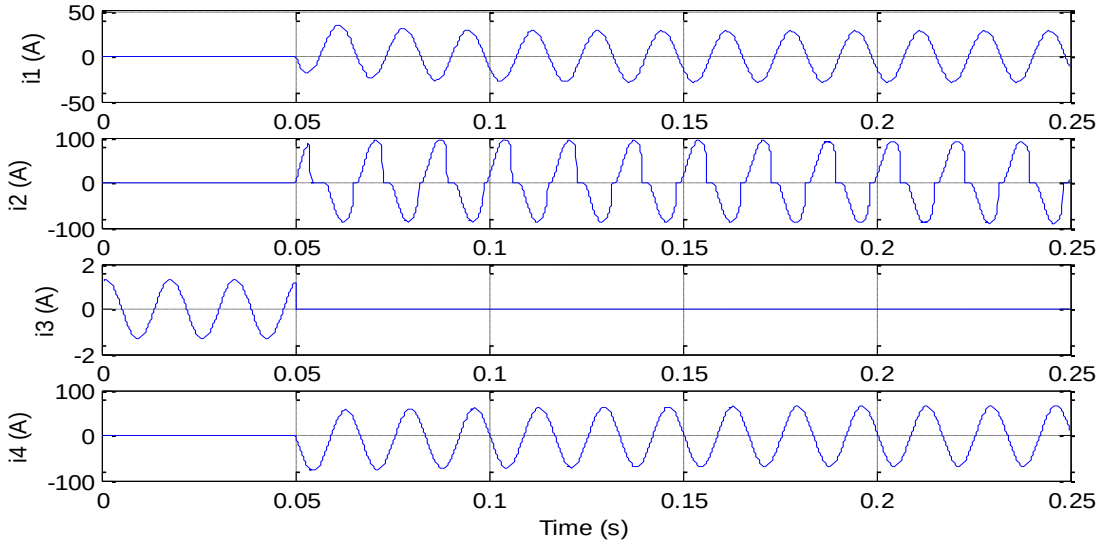

Figure 5.30: CT secondary currents for LLG external fault

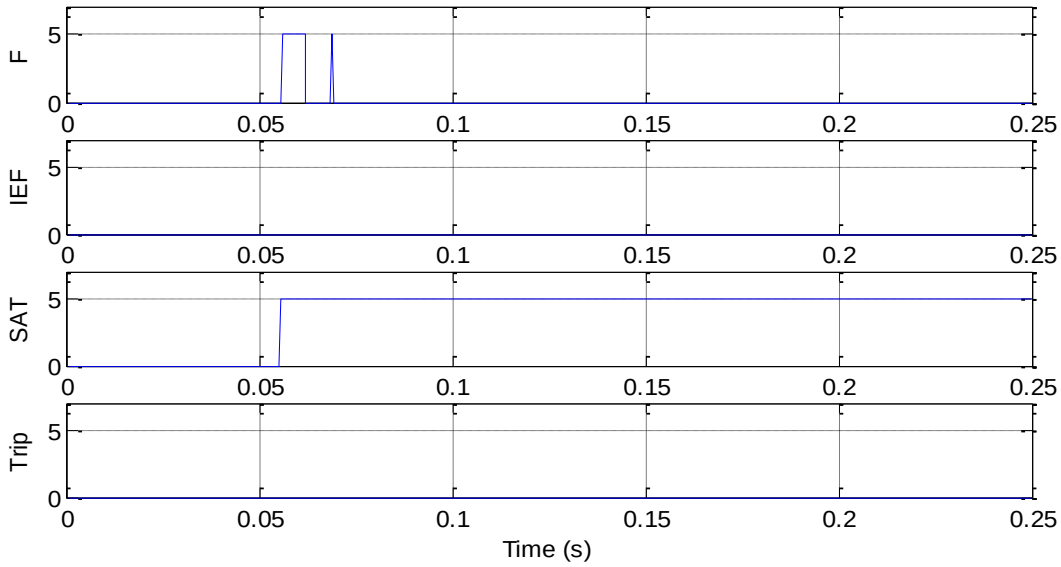

Figure 5.31: Responses from proposed method for LLG external fault

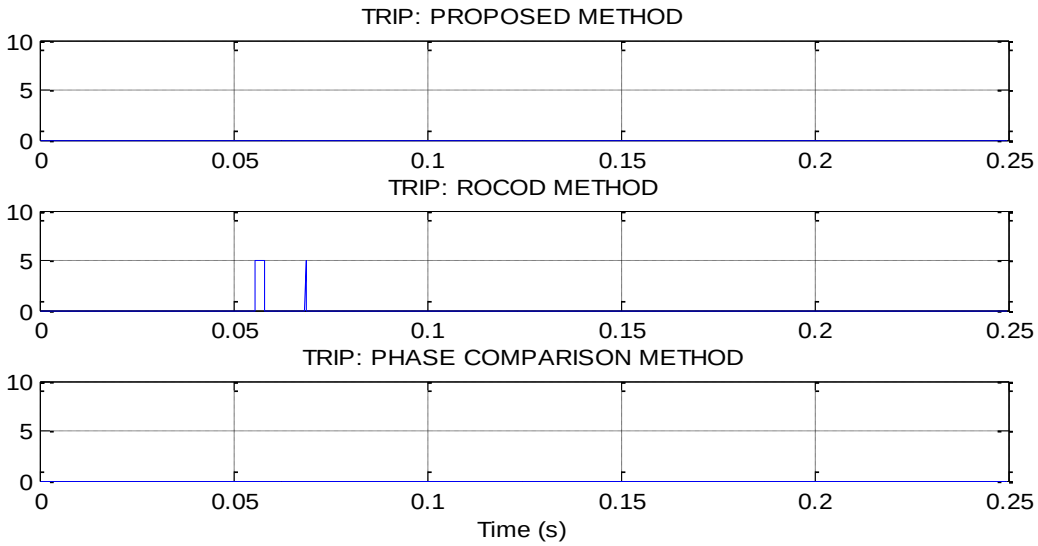

Figure 5.32: Comparative results for LLG external fault

Three phase (LLL) external fault:

CT secondary currents (phase A only) for four branches during LLL external fault are shown in Figure 5.33 where i_2 is distorted as the CT connected to that branch was saturated. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became close to zero as there was no active source at the other end of the load. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LLL external fault are shown in Figure 5.34. The output of fault detector (F) became high (fault detected) within 6ms after fault inception even through the fault was incepted at out of zone (external fault). This was happened due to the resultant differential current from distorted i_2 because of CT saturation. However, output of internal-external fault detector (IEF) remained low (external fault) as i_2 was flowing out from bus. The output of CT saturation detector became high (saturated) as the CT connected to the branch 2 got saturated. Therefore, the trip output of the

relay (TRIP) remained low (no trip command issued) as expected. The comparative results with other two existing methods are shown in Figure 5.35. The results show that the ROCOD method unexpectedly issued trip command after 6ms of fault inception for this LLL external fault; however, the phase angle comparison method did not issued trip command which is harmonious with the proposed method.

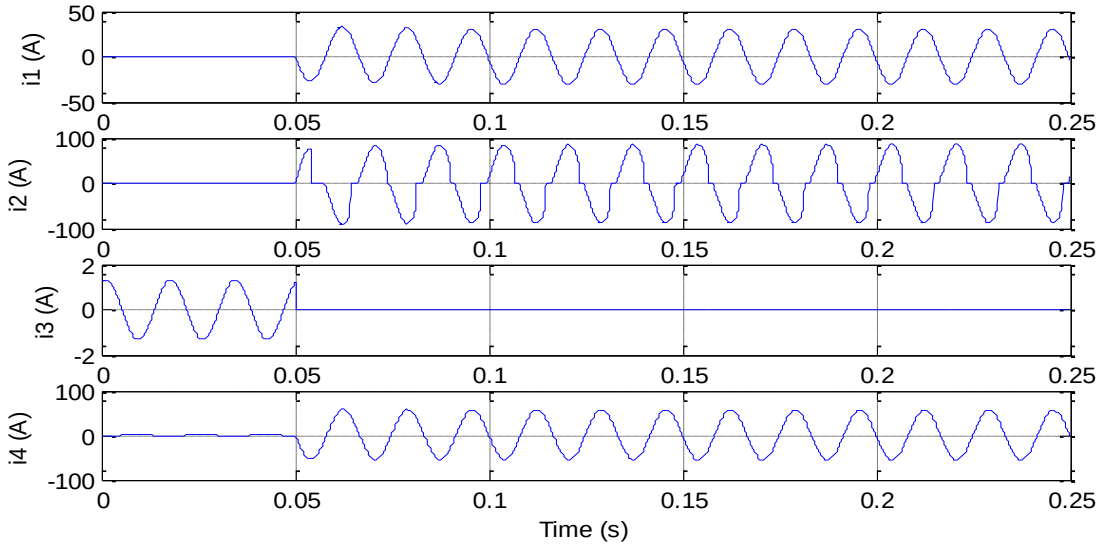

Figure 5.33: CT secondary currents for LLL external fault

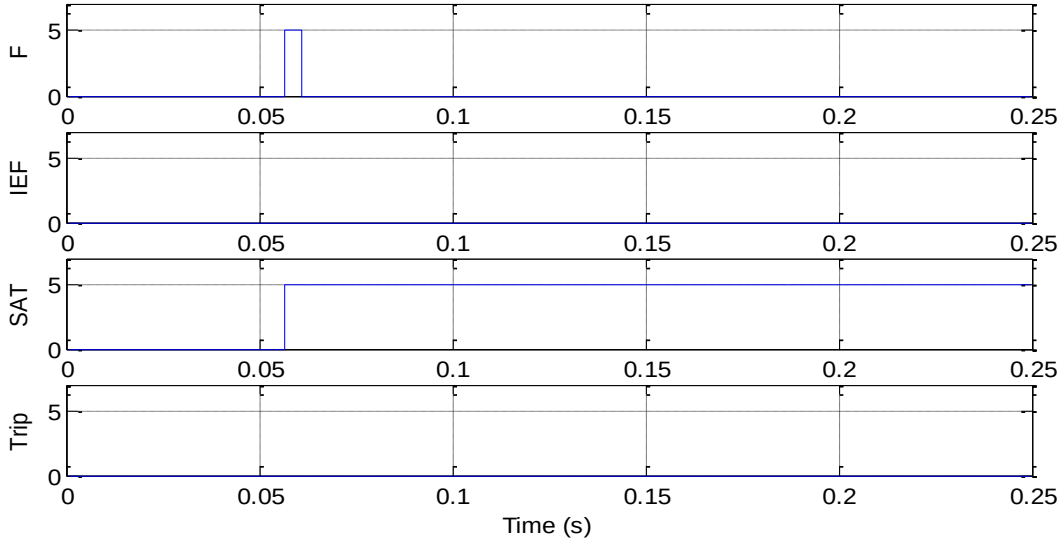

Figure 5.34: Responses from proposed method for LLL external fault

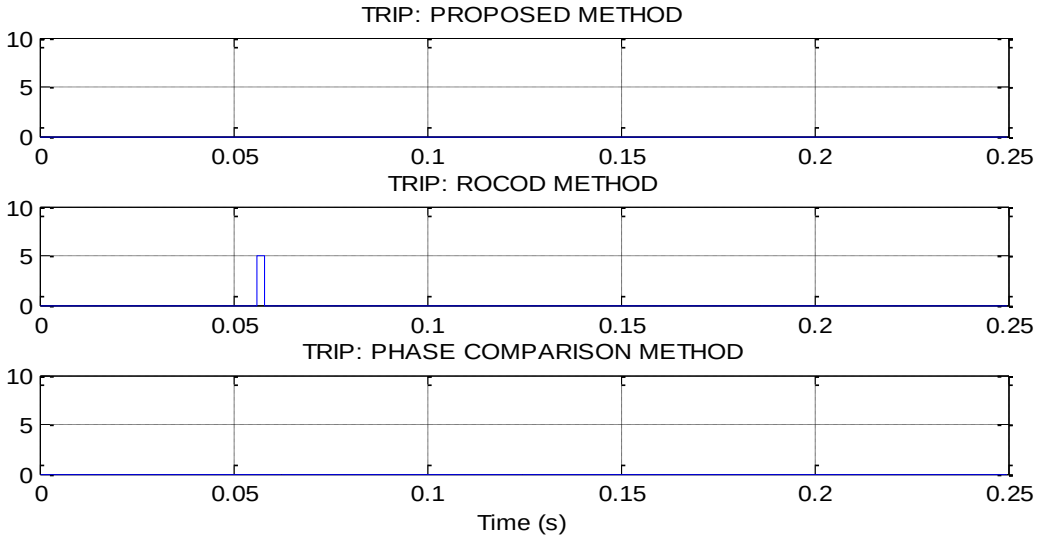

Figure 5.35: Comparative results for LLL external fault

Three phase to ground (LLLG) external fault:

CT secondary currents (phase A only) for four branches during LLLG external fault are shown in Figure 5.36 where i_2 is distorted as the CT connected to that branch was saturated. The branch currents (i_1, i_2, i_4) during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at 50ms, the current through the load (i_3) became close to zero as there was no active source at the other end of the load. The currents through all other three branches were high during fault due to the active sources behind them. The corresponding responses from the various components of proposed relay for LLLG external fault are shown in Figure 5.37. The output of fault detector (F) became high (fault detected) within 5.5ms after fault inception even through the fault was incepted at out of zone (external fault). This was happened due to the resultant differential current from distorted i_2 because of CT saturation. However, output of internal-external fault detector (IEF) remained low (external fault) as i_2 was flowing out from bus. The output of CT saturation detector became high (saturated) as the CT connected to the branch 2 got saturated. Therefore, the trip output of the

relay (TRIP) remained low (no trip command issued) as expected. The comparative results with other two existing methods are shown in Figure 5.38. The results show that the ROCOD method unexpectedly issued trip command after 5.5ms of fault inception for this LLLG external fault; however, the phase angle comparison method did not issued trip command which is harmonious with the proposed method.

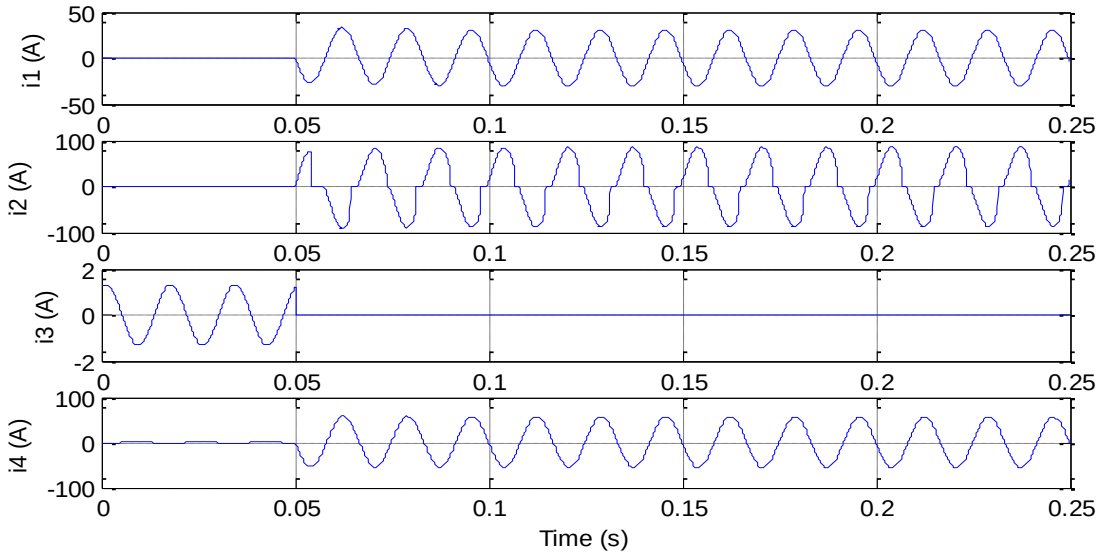

Figure 5.36: CT secondary currents for LLLG external fault

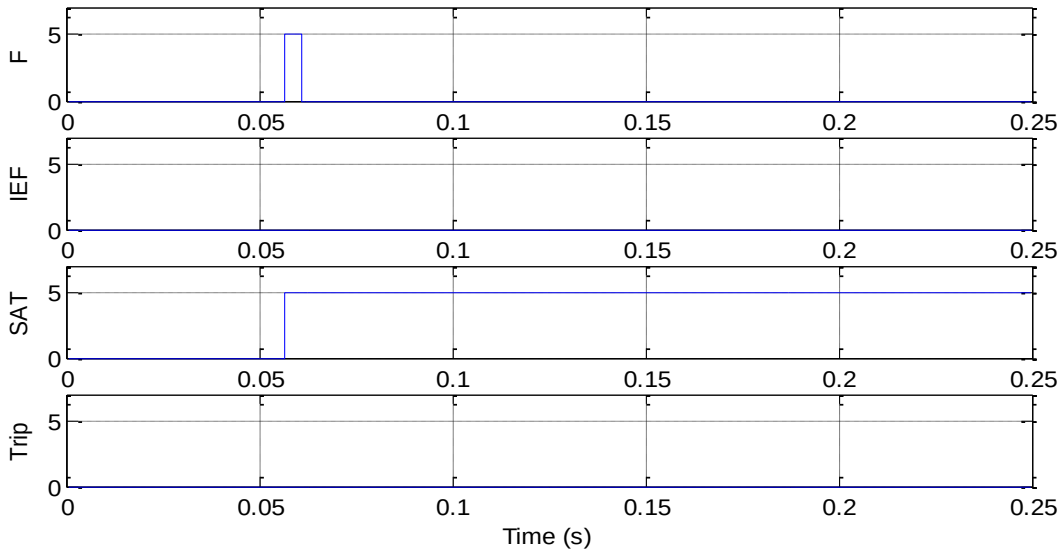

Figure 5.37: Responses from proposed method for LLLG external fault

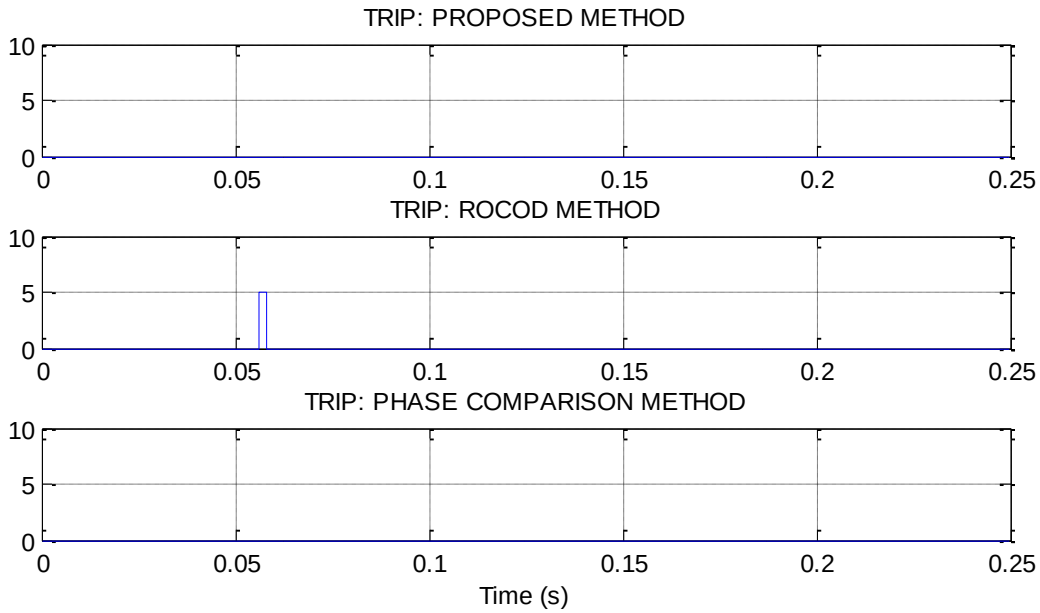

Figure 5.38: Comparative results for LLLG external fault

This chapter has covered the detail simulation methodology and discussions on found results. The results found from proposed method are also compared with two existing methods, namely, Phase Angle Comparison Method, and Rate of Change of Differential (ROCOD) Method. The next chapter will describe the conclusion remarks of this thesis and future research works.

Chapter 6

6 Conclusions Remarks and Future Research

In this thesis, a fault discrimination algorithm is presented based on newly defined partial operating current characteristics of a differential protection zone to overcome the impact of CT saturation on low impedance differential protection. Mathematical model of partial operating current characteristics is described. A bus differential relay is modeled in Matlab based on proposed algorithm which also includes percentage restrained characteristics to detect faulty conditions. To ensure high sensitivity for through internal fault (high impedance) condition, a supervisory technique is included by using CT saturation detection algorithm. The performance of proposed algorithm and relay are validated by a three bus test system. Proposed relay is applied in a bus which is connected with all possible elements of power system such as transmission line, generator (active source) and load (inactive source). The test system is built in EMTP. All possible bus fault scenarios are simulated in EMTP model and measured currents are set as the input of Matlab relay model to find the responses of proposed relay. Finally, results are compared with two latest existing methods, namely, delta phase angle method and rate of change method.

From the experimental results, it is found that proposed method has given correct responses for all faults scenarios including fast CT saturation, late CT saturation as well high impedance fault. The proposed relay gets trip for all types of internal faults irrespective of fault impedances and restraints trip during external faults even with CT saturation. It is also found that phase angle comparison method has given correct results for all external faults; however,

it fails to trip for phase to phase internal fault and all high impedance internal ground faults. The rate of change of differential method responds correctly only for internal faults but it is unable to restraint trip for external fault during CT saturation. Comparative summary of the results are shown in Table 5.5.

Fault Types	**Fault Name**	**Expected Response**	**Response from proposed method**	**Response from phase angle comparison method**	**Response from ROCOD method**
Internal	LG	TRIP	TRIP	TRIP	TRIP
	LL	TRIP	TRIP	NO TRIP	TRIP
	LLG	TRIP	TRIP	TRIP	TRIP
	LLL	TRIP	TRIP	TRIP	TRIP
	LLLG	TRIP	TRIP	TRIP	TRIP
High impedance internal	LG	TRIP	TRIP	NO TRIP	TRIP
	LLG	TRIP	TRIP	NO TRIP	TRIP
	LLLG	TRIP	TRIP	NO TRIP	TRIP
External (CT saturation)	LG	NO TRIP	NO TRIP	NO TRIP	TRIP
	LL	NO TRIP	NO TRIP	NO TRIP	TRIP
	LLG	NO TRIP	NO TRIP	NO TRIP	TRIP
	LLL	NO TRIP	NO TRIP	NO TRIP	TRIP
	LLLG	NO TRIP	NO TRIP	NO TRIP	TRIP

Table 6.1: Comparative summary of the results

Moreover, the proposed relay has satisfied all four functional requirements of power system protection schemes. Reliability is the most important requisite of power system protection. The proposed relay remained inoperative for normal operation before a fault occurs; but if a fault occurs, it responded quickly. Selectivity is another important requisite of power system protection schemes. Relays should be operated in only those fault conditions for which schemes are commissioned in the system. From the experimental results, we have seen that the proposed relay operated only for internal faults and remained inoperative during all external faults irrespective of CT saturation. The proposed relay is also sufficiently sensitive to operate reliably when level of fault condition just crosses the predefined set limit. Another important requisite of protection systems is the speed of operation. The results have shown that the proposed relay operated within sub-cycle time ranges after fault inception.

From the listed experimental results and above performance analysis, it is clear that the proposed relay including fault discrimination algorithm based on partial operating current characteristics is performing superiorly. Although, this thesis has only covered the applicability of the proposed fault discrimination algorithm in bus differential protection, it could be the promising options for line differential as well as transformer differential protections. A detail study is recommended to check the effectiveness of the proposed fault discrimination algorithm for line differential and transformer differential protections.

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Vita

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