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Development, Characterization, and Applications of High Temperature Superconductor Nanobridge Josephson Junctions

Joel R. Wendt, Chris P. Tigges, Vincent M. Hietala, Thomas A. Plut, Jon S. Martens, Kookrin Char, Marie E. Johansson

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DEVELOPMENT, CHARACTERIZATION, AND APPLICATIONS OF HIGH TEMPERATURE SUPERCONDUCTOR NANOBRIDGE JOSEPHSON JUNCTIONS

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Abstract

A well-controlled, high-yield Josephson junction process in high temperature superconductors (HTS) is necessary for the demonstration of ultra-high-speed devices and circuits which exceed the capabilities of conventional electronics. We developed nanobridge Josephson junctions in high quality thin-film YBaCuO with dimensions below 100 nm fabricated using electron-beam nanolithography. We characterized this Josephson junction technology for process yield, junction parameter uniformity, and overall applicability for use in high-performance circuits. To facilitate the determination of junction parameters, we developed a measurement technique based on spectral analysis in the range of 90-160 GHz of phase-locked, oscillating arrays of up to 2450 Josephson junctions. Because of the excellent yield and uniformity of the nanobridge junctions, we successfully applied the junction technology to a wide variety of circuits. These circuits included transmission-line pulse formers and 32 and 64-bit shift registers. The 32-bit shift register was shown to operate at clock speeds near 100 GHz and is believed to be one of the faster and more complex digital circuit demonstrated to date using high temperature superconductor technology.

Acknowledgment

The authors thank S. Y. Hou and J. M. Phillips of AT&T Bell Laboratories for providing the high-quality, thin-film YBaCuO material used in this work, and Ric Corless for electron beam lithography support. Work performed at Conductus was supported in part under AFOSR contract No. F19628-90-C-0149.

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DEVELOPMENT, CHARACTERIZATION, AND APPLICATIONS OF HIGH TEMPERATURE SUPERCONDUCTOR NANOBRIDGE JOSEPHSON JUNCTIONS

Introduction

Nanobridge Josephson junctions are a new junction technology made possible by high-quality thin-film high temperature superconducting (HTS) material, electron beam lithography, and improved aqueous etching. The yield and uniformity obtained with this junction technology makes it particularly suited to incorporation in high performance circuits.

This report describes the research into high temperature superconductor nanobridge Josephson junctions and their application to high performance circuits carried out under the Laboratory Directed Research Program (LDRD) *High Temperature Superconducting Nanobridges and Other Josephson Junctions* (Case 3539.020).

Background

Further improvements in the capabilities of superconducting electronics made from HTS materials will rely in large part on the ability to develop lithographic and patterning processes that are flexible, offer excellent dimensional control, and do not degrade the films. Furthermore, high-frequency operation will require submicron geometries for a wide variety of these devices. For example, bridge widths below 1 μm may be required for greater than 100 GHz operation of the superconducting flux-flow transistor.[1] To create Josephson nanobridges without relying on grain boundary formation, lithographic control of dimensions below 100 nm will be required.[2] A direct-write electron beam lithography system has been used, in conjunction with new wet etches, to fabricate nanobridges of these dimensions with reasonable performance parameters.

Several possible technologies for the fabrication of Josephson junctions from HTS films have been reported and most involve the engineered fabrication of grain boundaries. The earliest attempts exploited the Josephson coupling across grain boundaries which existed as imperfections in the deposited film. This technique is not amenable to circuit fabrication because of the difficulty in controlling both the number and placement of the grain boundaries, although some progress has been made towards this end. The first controlled grain boundary formation used custom $SrTiO_3$ substrates made with two crystallographic orientations present.[3] The YBCO film grows following these orientations and a high angle, Josephson-like grain boundary forms at the interface. This technique would be difficult to use in more complicated circuitry. A refinement of this process uses a seed layer, deposited on the substrate, to form the basis for the other axis of growth.[4] Another approach has been to form step-edge junctions by patterning the substrate prior to deposition of the superconducting thin film.[5] Film growth on these substrates quite reproducibly forms a grain boundary at the etched step. While this technique is more controllable than the use of bi-crystalline substrates, it introduces additional processing that may degrade the surface of the starting substrate prior to HTS film growth.

A more elaborate process technology is that of selective epitaxy on a substrate with a patterned silicon nitride overlayer.[6] In this work, electron beam lithography was used to pattern the silicon nitride film rather than the superconductor film directly. Using this technique, YBCO lines down to 0.13 μm have been formed but achieving finer resolution is limited by particulate formation during deposition. Additionally, there are concerns about stress in the grown films and silicon outdiffusion from the silicon nitride mask. Electron beam lithography has been used in combination with ion milling to pattern a YBCO film directly for the fabrication of grain boundary junction DC SQUIDs.[7] The minimum reported feature size obtained via this technique was 0.25 μm, limited in part by the use of a thick, negative electron beam resist. Additionally, the damage to the thin film induced by the ion milling process would increasingly and

unacceptably degrade the film characteristics as the linewidth were reduced to 0.1 μm and below. More recent work[8] describes the fabrication of microbridge junctions in YBCO having dimensions in the range of 0.1 to 0.5 μm using either of two techniques similar to those just described[6,7] and, hence, having the same limitations as those previously discussed.

We have combined direct-write electron beam lithography utilizing a thin, positive electron beam resist having an ultimate resolution smaller than 20 nm with an improved aqueous etchant[9] to fabricate nanometer-scale nanobridges on high-quality, epitaxial YBCO. To our knowledge, these are the smallest geometry devices yet reported on an HTS film. This technique allows the fabrication of Josephson junctions at arbitrary position, orientation, and density, resulting in minimal constraints on the design of superconducting circuits and without the requirement for grain boundary formation.

Development and Characterization of Nanobridge Josephson Junctions

Nanobridge Structure and Fabrication

The first step in applying a positive electron beam resist process to the direct patterning of YBCO films was to check that the associated process treatments did not degrade the characteristics of the film. The surface resistance of a virgin YBCO film on $LaAlO_3$ substrate was first measured at 77K, as a function of frequency, using the confocal resonator technique.[10] The same sample was then dehydration-baked for 15 minutes in air at 170°C, spin-coated with polymethylmethacrylate (PMMA) resist in solution with chlorobenzene, and baked for one hour at 170°C. Although not exposed to an electron beam, the sample was immersed in the methylisobutylketone(MIBK): isopropyl alcohol(IPA)-based developer for one minute after which the PMMA film was stripped in acetone. Finally, the sample was rinsed in IPA and blown dry with dry-N_2. The surface resistance of the sample was then re-measured and the degradation was found to be less than 5% which is consistent with that observed for other solvent exposure.

In making the YBaCuO films, Y and Cu metals are evaporated from separate electron gun sources and BaF_2 is resistively evaporated. The YBaCuO films are nominally 25 nm thick and are epitaxially oriented with the c-axis normal to the substrate. The samples are annealed ex-situ in a carefully optimized multi-stage process[11] to produce T_c s of about 90K and critical current densities at 77K (0 field) of about 1 MA/cm^2. Three optical lithographic process levels were performed on each of the samples prior to the electron beam lithographic step. These include mesa etching for delineation of the active YBCO area, deposition of Ag contacts (which also includes the deposition of the alignment marks used by the electron beam lithography system to align to the optical levels), and a second etch to thin the YBCO film in the areas where the weak links are to be formed. This central area was thinned to about 10 nm to control the effects of undercutting during the etch. Details of these processes have been published previously.[9,12]

For the electron beam lithography level, we used 100 nm thick PMMA baked for one hour at 170°C. The exposure was performed on a JEOL JBX-5FE field-emission electron beam lithography system with a beam current of 800 pA at a beam diameter of 6 nm. Prior to exposure, a thin gold layer (~10 nm) was thermally evaporated onto the insulating sample to provide a current path for the incident electrons. Prior to development, this thin gold film is removed in a standard potassium iodide/iodine (KI/I) etch. Note that the superconductor film is entirely protected by PMMA during the gold etch and does not come in contact with the KI/I solution. Development was performed for 60 seconds in 1:3::MIBK:IPA. The weak links were fabricated by notching in from both sides of a narrowed, thinned region of YBCO film. The geometry of a discrete nanobridge is shown in Fig. 1(a). The notches were patterned by exposing pairs of single-pass lines with doses between 2.3 and 4 nC/cm to obtain lithographically-defined bridge lengths of 20 to 80 nm. A scanning electron micrograph of a discrete nanobridge is shown in Fig. 1(b) and indicates the sub-100 nm dimensions achieved. The effective bridge length is smaller than the notch opening due to curvature of the etched bridge as shown in Fig. 1(b). The bridge width was varied in the computer-aided design (CAD) pattern from 0.2 to 0.1

μm, biased upwards to account for gap shrinkage from the proximity effect. The decarbonated disodium ethylenediaminetetraacetic acid (Na_2H_2EDTA) etch[9] was applied in sequential steps, measuring for junction behavior after etch step. Because the YBCO film is so thin (10 nm) and the etch rate of the aqueous etch is slow, we did not experience difficulty with uncontrolled undercut during the wet etch as evidenced by the superior yield on the smallest geometry devices.

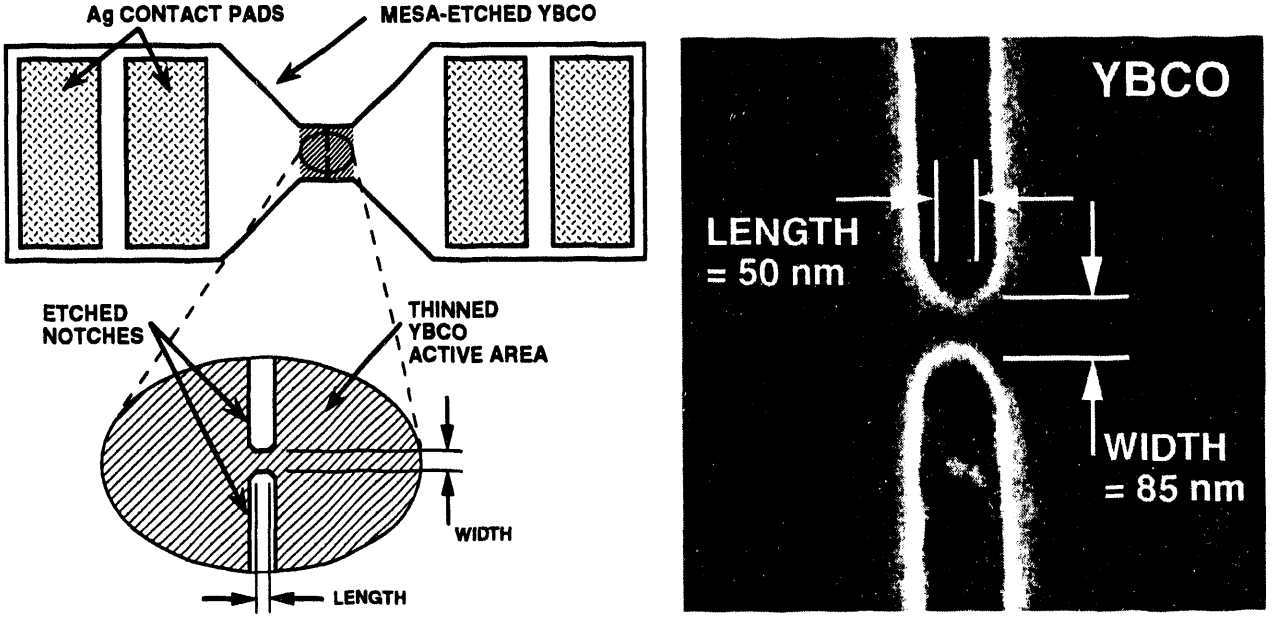

Fig. 1. (a) Schematic illustration of a discrete nanobridge showing the mesa-etched YBCO film and Ag contact pads with inset detail of the geometry of the bridge formed by notching the thinned YBCO active area. (b) Scanning electron micrograph of a discrete nanobridge with sub-100 nm dimensions.

Nanobridge Characteristics

Functional junctions exhibited critical currents, I_C, in the range of 20-40 μA with normal state resistances, R_n, in the range of 5-20 Ω, resulting in I_CR_n products of 100-400 μV at 77K. These numbers are comparable to results for other YBCO technologies. A typical current-voltage (*I-V*) curve measured at 77K for a Josephson nanobridge is shown in Fig. 2(a). The *I-V* curve is nearly ideal, following the standard resistively-shunted junction (RSJ) model.[13] The *I-V* curve of the same device upon application of an 11 GHz field is shown in Fig. 2(b). The dependence of current step magnitude on field amplitude was found to be consistent with that of the low capacitance RSJ model. A plot showing the dependence of the critical current with applied magnetic field is shown in Fig. 3. The magnetic field dependence is very close to the ideal $\sin(kI_C)/(kI_C)$, suggesting an extremely uniform junction.[13] Yield showed a very weak dependence on the length of the nanobridge, but the width dimension was very important. As would be expected, the narrower bridges (in terms of the gap defined in the CAD pattern) had much higher yields (~60%) and it is believed that the small widths achieved were aided by limited undercutting by the etch. Note that the yield does not decrease with decreasing lithographic dimensions, indicating excellent yield of the lithographic process in the nanometer regime. The need for precise control of the lithographic process is clear. If the etch-mask-defined gap is too small, then any appreciable undercutting of the mask by the aqueous etch would be expected to result in a zero-width bridge or open circuit. Conversely, if the etch-mask-

defined gap were too large, then one would be relying solely on undercut to achieve appropriate dimensions for Josephson junction formation which could not be expected to be a high yield process. Yield is ultimately limited by film inhomogeneities. Junction to junction spread on I_C was about ± 11% and on R_n, about ± 6%. These worst case numbers are based on measurements of 100 junctions over four typical wafers written in the same run (1 σ spreads are about ± 4% and ± 2% respectively). These variations are correlated in that a higher I_C goes with a lower R_n resulting in narrower spreads on $I_C R_n$.

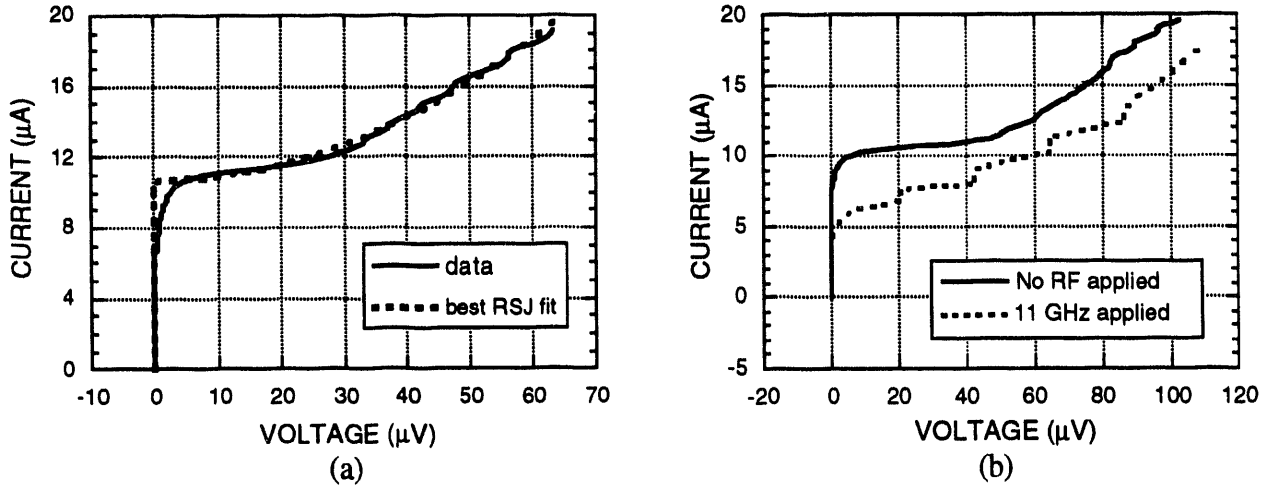

Fig. 2. (a) Current-voltage characteristics of a typical nanobridge junction at 77K shown with best-fit RSJ result. (b) Current-voltage characteristic upon application of an 11 GHz field showing clean Shapiro step formation confirming Josephson behavior.

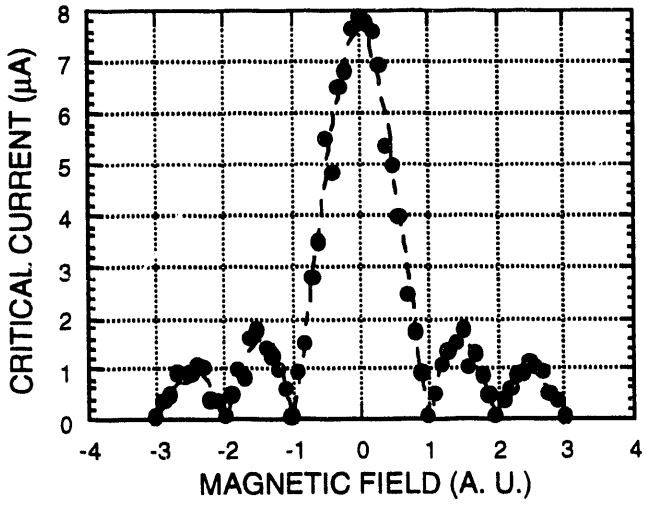

Fig. 3. The critical current of a nanobridge as a function of applied magnetic field. The dashed line is a best-fit curve to theory and the excellent agreement indicates a nearly ideal junction.

It is unlikely that geometric constrictions alone produce the observed junction behavior since the constriction is probably not small enough for true Josephson weak link behavior given the magnitude of the critical currents. A more likely explanation is that there is oxygen depletion in the constricted region forming a reasonably uniform barrier. To test this hypothesis, existing junctions were annealed at 400 °C for 15 minutes in oxygen. Critical currents increased, on

average, by a factor of 2.5 with some junctions demonstrating flux flow behavior. This suggests that an oxygen-depleted barrier in the bridges is critical. Long term reliability of these junctions would then depend directly on the stability of these depletion barriers. Standard junctions show less than a 5% variation in critical current over a nine month period while stored at room temperature in air and cycled at least ten times to 77K.

Determination of the Uniformity of Nanobridge Josephson Junctions Using 2-D Arrays

As HTS junction processes and circuits increase in density and complexity, statistical parameter data is of rapidly increasing importance. In particular, promising HTS digital circuits require quite careful control of junction parameters in order to be produced with reasonable yield. Thorough DC characterization is most commonly used but due to the large number of measurements required for adequate statistics, this can be extremely time-consuming and expensive. DC measurements of series arrays work as a good test for hysteretic junctions but fail for non-hysteretic junctions, which includes most HTS technologies, since there are no easy-to-see switching events. Arrays of HTS junctions have recently been demonstrated[14] and offer the ability to quickly extract statistics for hundreds or thousands of junctions in a single measurement. This is based on the dependence of the oscillation spectrum on the spreads in critical current, and to a lesser extent, normal state resistance. The relationship has been explored by several groups before[15-17] both theoretically and experimentally with Nb junctions at 4.2K. Here we have studied nanobridge junctions in YBaCuO at 77K.

We started by assuming that the junction parameters were normally distributed and independent which is a reasonable assumption for sufficiently large arrays. Then, for a given array topology and bias conditions, there were four unknowns in the system: mean critical current ($\langle I_C \rangle$), standard deviation of critical current (σI_C), mean normal state resistance ($\langle R_n \rangle$), and standard deviation of normal state resistance (σR_n). From the known bias data and array geometry, it was possible to extract reasonable estimates of $\langle I_C \rangle$ and $\langle R_n \rangle$. The fitting routines were then used to extract the remaining two parameters from the normalized spectrum. The spreads σI_C and σR_n both affect the shape of the spectrum but the effect of spreads in critical current are particularly dramatic.[15] The accuracy of the extraction of σI_C is therefore expected to be better than that for σR_n as will be discussed below.

The measured spectra were fit, using a Levenberg-Marquardt algorithm,[18] to that computed from a self-consistent simulation of the structure illustrated in Fig. 4. As discussed by several groups,[15] the two-dimensional structures are considerably more forgiving to defects and deviations because of the myriad of alternate current paths available. The analysis began by applying Kirchoff's law at each node of the array. The junctions were assumed to be resistively-shunted junction (RSJ)-like at least in the sense that the low-temperature *I-V* curve nearly fits the theory and the usual voltage-phase relation holds. Thermal noise was modeled by a modification of the analysis by Ambegaokar and Halperin,[19] although it is believed that this will overestimate the broadening for some of the junction technologies since the current-phase relationships are not perfectly sinusoidal. Each junction was assumed to be coupled to an external impedance (a ground plane was always assumed) which was composed of a radiation resistance and some near-field impedance. While the former is important for computing the loading and output power coupling, the latter represents an additional coupling mechanism between the junctions in the array. These contributions were estimated from finite element techniques but one can see they arise from surface-wave mode coupling, microstrip patch coupling and dielectric reflection.[20] Based on work with arrays of FETs and diodes[21,22] and due to the high dielectric constants involved, we assumed that the reactive part of this coupling impedance was predominantly capacitive. Loop inductance was neglected since for the array geometry analyzed here, each loop had less than about 1 pH of inductance. The individual loop LI_C product was always less than $0.05\Phi_0$ so flux quantization was neglected. Quantization in multiple loops is physically possible[15] and, in general, should be considered but it is less likely in the present geometry. The phase at each node ϕ_j is the state variable.[15-16] The equation for node j is then

$$\sum_{i=1}^{N_j}\left[I_{c,i,j}\sin(\phi_i-\phi_j)+\frac{\hbar}{2eR_{i,j}}\frac{\partial(\phi_i-\phi_j)}{\partial t}\right]$$
$$+\sum_{k=1}^{N}\frac{\hbar}{2e}\left[B_{k,j}\frac{\partial(\phi_k-\phi_j)}{\partial t}+C_{k,j}\frac{\partial^2(\phi_k-\phi_j)}{\partial t^2}\right]=I_{ext,j} \quad (1)$$

where $I_{c,i,j}$ and $R_{i,j}$ describe the junction connecting nodes i and j, N_j is the number of nearest neighbors to node j and N is the total number of nodes. The second summation represents the coupling impedances discussed above (first term resistive, second term capacitive). For interior nodes, N_j=4 for the standard 2D structure shown in Fig. 4. Variations on this present structure allow values up to N_j=16 (all data and further analysis refers only to the standard 2D structure). For junctions on the edge of the array in the standard structure, N_j is 3.

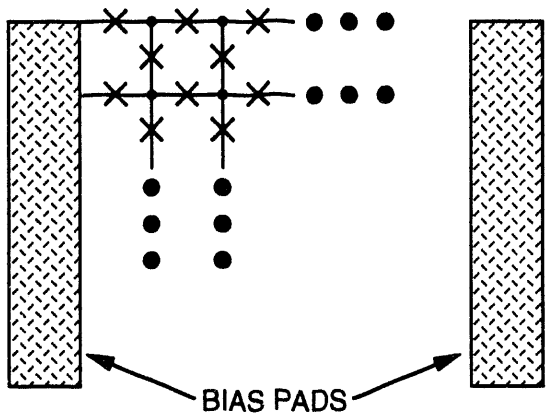

Fig. 4. The standard two-dimensional array structure used in the measurements and analysis. The array consisted of 2450 junctions with bias applied from the two ends through large contact pads.

The B_{kj} and C_{kj} terms describe the coupling between junctions (multi-junction interactions are not considered explicitly) through surface modes and the near fields (B_{kk} and C_{kk} =0). These values were *numerically* estimated through finite element simulations based on a pair of junctions in the environment of the circuit: on the $LaAlO_3$ or YSZ substrate with ground plane. The nearest neighbor B_{kj} values were always below 0.02 in absolute value and the nearest neighbor C_{kj} values were below 10^{-12}. The C_{kj} values fall off super-linearly with node separation but the B_{kj} interactions fall off sub linearly (representing the surface mode components). While it appears from the measurements and simulations that the nearest neighbor interactions dominate, the effect of the ground plane cannot be neglected because of the substantial effects on impedance, the addition of capacitance, and the promotion of surface modes. Normal metal ground planes were used experimentally but perfect conductors were assumed for the calculations. Clearly both B and C values will increase as the substrate gets thinner or as the dielectric constant increases. As the array packing increases or electrode width increases, the direct coupling parameters C increase but B values do not change much. If the metallization occupies a very large fraction of the surface the B parameters do increase and their spatial dependence flattens out (a parallel plate mode is more likely). These dependencies combine to create different B and C parameters for different arrays.

$I_{ext,j}$ is the external current applied to node j and is zero for all interior and top/bottom nodes. For nodes that are biased, $I_{ext,j}$ is equal to the bias current per row multiplied by ±1 depending on the exact bias arrangement used. For these experiments, the bias was applied uniformly from the side bias pads although many other possibilities are of interest.[23]

The usual approach is to formulate the phase derivatives as a function of the phase state variable Φ and solve the differential equation system conventionally in time. That is, we desire a system of the form

$$\begin{bmatrix} \frac{\partial \phi_1}{\partial t} \\ \bullet \\ \bullet \\ \bullet \\ \frac{\partial \phi_{2N}}{\partial t} \end{bmatrix} = \begin{bmatrix} f_1(\Phi) \\ \bullet \\ \bullet \\ \bullet \\ f_{2N}(\Phi) \end{bmatrix} \tag{2}$$

but as presently formatted, the system is described by

$$[A] \begin{bmatrix} \frac{\partial \phi_1}{\partial t} \\ \bullet \\ \bullet \\ \bullet \\ \frac{\partial \phi_{2N}}{\partial t} \end{bmatrix} = \begin{bmatrix} g_1(\Phi) \\ \bullet \\ \bullet \\ \bullet \\ g_{2N}(\Phi) \end{bmatrix} \tag{3}$$

where Φ represents all of the nodes phases $\phi_1, ..., \phi_{N;fi}$ and g_i are functions of the node phases, the junction parameters, the stimulus and the topology. The state variable $\phi_{N+1}, ..., \phi_{2N}$ are dummy variables for the first derivatives of the phases (following the standard approach of solving a second order system by converting it to a larger first order system). To understand the terms in this system, consider node p which initially we assume not to be on an edge. By looking at the first equation, the dominant elements of A in the p^{th} row are (Q=number of junctions per row of the array):

$$\begin{aligned} a_{p,p+1} &= \frac{1}{R_{p,p+1}} + B_{p,p+1} \\ a_{p,p-1} &= \frac{1}{R_{p,p-1}} + B_{p,p-1} \\ a_{p,p+Q} &= \frac{1}{R_{p,p+Q}} + B_{p,p+Q} \\ a_{p,p-Q} &= \frac{1}{R_{p,p-Q}} + B_{p,p-Q} \\ a_{p,p} &= -\frac{1}{R_{n,p,p-Q}} - \frac{1}{R_{n,p,p+Q}} - \frac{1}{R_{n,p,p-1}} - \frac{1}{R_{n,p,p+1}} \end{aligned} \tag{4}$$

$$-B_{p,p+1} - B_{p,p-1} - B_{p,p+Q} - B_{p,p-Q} - C_{p,p+N+1} - C_{p,p+N-1} - C_{p,p+N+Q} - C_{p,p+N-Q}.$$

The other terms in the row are straightforward to derive from Eq. (1). The corresponding $g_p(\Phi)$ is given by

$$g_p(\Phi) = -\frac{2e}{\hbar}\left[\begin{array}{l} I_{c,p,p+1}\sin(\phi_{p+1}-\phi_p)+I_{c,p,p-1}\sin(\phi_{p-1}-\phi_p) \\ +I_{c,p,p+Q}\sin(\phi_{p+Q}-\phi_p)+I_{c,p,p-Q}\sin(\phi_{p-Q}-\phi_p)\end{array}\right]. \quad (5)$$

For nodes on the right edge of the matrix, $a_{p,p-1}=0$ and the second term in g_p is replaced by $-I_{ext,p}$. For nodes on the left edge, $a_{p,p+1}=0$ and the first term in g_p is replaced by $-I_{ext,p}$. For nodes on the top edge, $a_{p,p-Q}=0$ and the fourth term in g_p is replaced by 0. For nodes on the bottom edge, $a_{p,p+Q}=0$ and the third term in g_p is replaced by 0. The terms for the corner nodes are obvious extensions of this reasoning. To clean up the details on the dummy variables, $g_{N+k}=\phi_k$ and $a_{N+k,l}=\delta_{kl}$ for k running from 1 to N.

Since the matrix A is dependent only on the array topology and the effective junction resistances, it can be pre-computed and inverted before the differential equation is solved. Depending on the coupling coefficients B_{jk} and C_{jk}, the matrix A is not particularly sparse and general routines must be used. If the ground plane is far away (not an advisable situation based on the resultant poor power coupling to the measurement apparatus), sparse matrix techniques can sometimes be employed.

During the differential equation solution period, the phase derivative vector can then be quickly computed based on present phase values. This is computationally more efficient and far more robust than relying on previous values of the phase derivative. The differential equation was solved using a Bulisch-Stoer method[18] with adaptive step-size control. Since the solution to this problem is relatively smooth , this is a computationally efficient approach. Because this is a time domain calculation, the result itself is not of prime interest but rather the power spectrum is. The computation was continued for approximately 1000 cycles after periodicity in the terminal waveform was established. The power spectrum of the resulting waveform was then computed using fast Fourier techniques and a Welch window.[18] The resulting spectrum was normalized and compared to the measured spectrum in an RMS sense over a frequency range of five times the linewidth of the measured signal. The measured spectrum was corrected for the frequency dependence of the receiving measurement system before this process. This routine was repeated 10-20 times in a Monte Carlo fashion. Because of the averaging nature of the array, many Monte Carlo iterations were not needed unless a particularly bizarre distribution was obtained (e.g., a statistical anomaly such as a cluster of dead junctions). The average of these error functions was fed back as the error for the fitting routine.

Arrays of up to 2500 junctions were simulated using this technique. On a computer based on a Motorola 68040 microprocessor operating at 33 MHz, a fit for a 400-junction array took approximately 2 hours while for the 2500-junction arrays, the fit took approximately 3 days. The precision requested for these benchmarks was about 10^{-4} on the parameter spreads and the accuracy is expected to be within 10% on σI_c. Because of the weaker dependence of spectral shape on σR_n, the accuracy is expected to be only about 20%. Changes in R_n most clearly affect the tails of the spectrum making the extraction of that parameter even more difficult if the coupled signal is weak. Also, it was assumed that $\sigma R_n \approx \sigma R$ since the junction resistance dominates the interaction between nearest neighbors. It must be emphasized that the above numbers are errors on the spreads and not spreads themselves.

The measured nanobridge arrays were composed of 35 rows and 35 columns with a total of 2450 junctions. There was no *a priori* knowledge of systematic variations of junction parameters as a function of position: all junctions within an array were lithographically the same and all were assumed to belong to the same distribution. All arrays were constructed with a ground plane of normal metal, either sputtered or press-fit using a conductive adhesive onto the back of the substrate of $LaAlO_3$ or YSZ. The relatively high dielectric constants of these substrates (>20) contributed to the importance of surface modes in array behavior. In all cases, two-dimensional arrays were fabricated and their spectra measured in the 90-160 GHz range. At least

three frequencies were used in the measurements to ensure that the fit spreads were in agreement and the average of these results are discussed below.

Preliminary measurements were performed to examine the validity of the C_{kj} and B_{kj} parameters used in the calculations. Two junctions, arranged similarly to those in the array, were connected with a large inductance (order of nH) so that a resonator could be formed using the coupling capacitance between the junctions and the ground plane. The resulting resonator, which operated at about 9 GHz, produced C_{kj} values within about 20% of that found from the finite element analysis. This was done at low frequencies since it was assumed the surface wave coupling effects would be weaker and it was hoped that the frequency dependence of the capacitive effects would be small. A higher frequency two-junction resonator was then attempted to extract B_{kj} estimates. Since presumably C_{kj} is now known and the direct electrical interaction is known, the surface wave effects can be isolated somewhat. This resonator, operating at 65 GHz, produced B_{kj} values within about 30% of those calculated for the array. While not conclusive, these two-junction experiments provide some indication that the analysis is plausible.

The arrays were measured at 77K and a representative spectrum, along with the fit spectrum, is shown in Fig. 5. The spectrum was measured using a horn antenna coupled to a heterodyne receiver operating over the range 90-160 GHz with a minimum noise floor of approximately -80 dBm. Power was coupled with 20 dB gain rectangular waveguide horns (W or D band) placed 4 to 10 cm above the array with the position adjusted for maximum power. The spectra were observed not to change shape with this adjustment. The angular orientation of the horn was adjusted in all cases for maximum power, generally obtained when the short wall was aligned with the bias current direction. The receiver, a spectrum analyzer harmonic mixer, was calibrated and the accuracy of the power levels was approximately ±2 dB. The orientations were adjusted for maximum power since the high dielectric constant of the substrate impeded coupling somewhat. This coupling was not estimated for these experiments. Absolute power entering the horn was measured directly since the spectral shape was of primary interest.

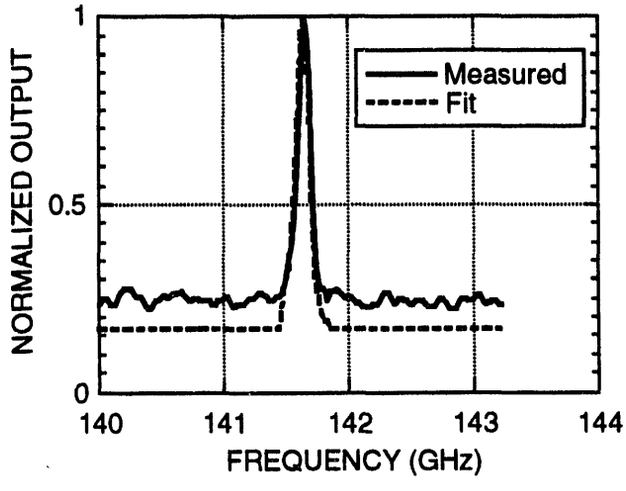

Fig. 5. Measured and fit spectra from the nanobridge array. The peak has been normalized to 1 and the frequency dependence of the receiving system has been removed. The noise level was not included in the fit hence the baseline does not match.

The vertical scale in Fig. 5 was normalized to a peak of 1 since it is the spectral shape more than the absolute power values that are of interest in these experiments. This spectrum was corrected prior to normalization for the frequency dependence of the receive antenna and down-conversion circuitry which were measured independently using a commercial broadband source. The absolute power levels of the arrays tended to be on the order of tens to hundreds of nW. These power levels are affected by the non-uniformities in the arrays as well as the coupling

structure used in the given measurement. The power levels are also consistent with DC power levels with conversion efficiencies of a few percent.

The fitting routines discussed above were applied to three arrays. The fit spectrum for one of the arrays is shown in Fig. 5 along with the corresponding measured results and indicate reasonable agreement. The baseline on the fit curve is arbitrary since the numerical noise floor could be chosen, the only criteria is that it was chosen to be at or below the measurement noise floor in each experiment. The results for the three arrays were averaged together and are shown in Table I. From array to array, variations in the parameters did not exceed 5% and from frequency to frequency within one array, they did not vary by more than 1%. DC results from a variety of junctions from different runs are also shown in the table and are corrected for varying junction widths. The DC data is based on approximately 200 nanobridge junctions. The HTS material deposition runs for the DC and array circuits were close together in time for the junctions so one would expect similar junction characteristics. This is indeed reflected in the statistics and gives us some confidence in the reliability of the array technique.

TABLE I. Tabulated mean and standard deviation values of critical current and normal state resistance for the nanobridge junction technology. Both DC-measured and array-derived results are shown.

Statistical Parameters	Values
$\langle I_c \rangle$ DC	13 μA
$\langle I_c \rangle$ arrays	14 μA
σI_c DC	0.3 μA
σI_c arrays	0.2 μA
$\langle R_n \rangle$ DC	11.5 Ω
$\langle R_n \rangle$ arrays	12.0 Ω
σR_n DC	0.2 Ω
σR_n arrays	0.2 Ω

In the classical junction models, one would expect the resistance and critical current variations to be similar in amplitude and correlated: something leading to reduced critical current would generally lead to increased R_n and vice versa. This does not characterize many HTS junction families but does seem to hold for the nanobridge junctions where the R_n and I_c spreads on a percentage basis are similar and they are, based on DC observations, quite correlated as discussed above. This suggests a more intrinsic junction. This is consistent with the absence of an inter-material barrier in the nanobridges and may point to a requirement for any uniform HTS junction technology.

Applications of Nanobridge Josephson Junctions

Josephson Transmission Lines for Pulse Formers

Narrow pulses and/or high speed step waveforms are needed for applications such as single flux quantum[24] and other high speed logic[25] and materials characterization. Shock wave transmission lines composed of non-linear devices embedded in a quasi-lumped structure can generate these signals. These transmission lines rely on the dependence of some reactive component of the transmission line (series inductance or shunt capacitance) on signal level to generate high slew signals. Passive networks can convert these rapid edges into a narrow pulse by, for example, taking a derivative. Significant work has been done using diodes as shunt

capacitance in artificial transmission lines fabricated on semiconductors. These devices rely on the voltage dependent capacitance of diodes to form the shock wave.[26] The use of Josephson elements in non-linear transmission lines has also been considered (e.g., Ref. 27) for a variety of applications. It is possible using Josephson junctions, to form the pulse sharpening transmission line from a single film of superconducting material resulting in simpler fabrication and greater process compatibility with superconducting digital electronics. It is also anticipated that the resulting pulses will be sharper.

All of the circuits studied were fabricated on $LaAlO_3$ substrates that were initially 300-500 μm thick. All circuits had annealed Ag contacts, were incorporated into coplanar waveguide structures, and were measured with either Cascade probes or a monolithic Josephson spectral technique described in the next section.

The reactive non-linearity used in these circuits is the Josephson inductance that increases with current level[9] up to the critical current. Hence, if an artificial transmission line were composed of many series junctions with some quasi-lumped shunt capacitance, the velocity of the shock wave would be less than the phase velocity resulting in a falling edge with increased slope.[28] The structure and equivalent circuit of such a line are shown in Fig. 6. Because of the very small junction capacitance of the nanobridge junctions, it was omitted from the equivalent circuit. Because the spacing between the junctions was small (on the order of 10 μm) and the line impedance was low, the transmission line inductance was neglected relative to that of the junctions. Assuming that the shock wave exists over a sufficiently large electrical length, an important conclusion is that the fall time is limited to something on the order of $6\tau_0$ where τ_0 is the fundamental junction time constant given by[28]

$$\tau_o = \frac{\Phi_o}{2\pi I_c R_n} \tag{6}$$

where Φ_0 is the flux quantum. The amplitude squared of the shock wave will behave as[28]

$$|V|^2 \propto A\left[1 - \tanh\left(\frac{(x-ut)B}{u\tau_0}\right)\right] \tag{7}$$

where x is the position along the line, u is the velocity of the shock wave, B is a parameter describing the non-linearity,[28] and τ_0 is given by Eq. (6). Most importantly, B is negative for inductance non-linearities (as in serial Josephson systems) and is positive for capacitive non-linearities. This causes the falling edge to be steepened for inductive systems and the rising edge to be steepened for capacitive systems. As I_cR_n increases, the pre-factor $B/(u\tau_0)$ in the *tanh* argument will increase making the transition steeper.

The serial system is a classical shock wave structure that has a number of advantages including being able to keep the junctions below their critical current and hence dissipating essentially no power. The output signal level is limited by the critical current since in this structure the current level in any junction is not intended to rise above the critical current. Hence, in a 50 Ω system, the output voltage is limited to about $50I_c$.

The serial Josephson lines (Fig. 6) were comprised of about 60 junctions which created some granularity problems, probably increasing the fall time and causing ripples in the output response. The average I_cR_n product was about 200 μV at 77K. For this experiment, a pulse with rise and fall times approximately equal to 20 ps and amplitude of 50 μA (just below critical currents) was applied to the line. One would expect a time constant on the order of 10 ps based on Eq. (6). Measured results are shown in Fig. 7 and the fall time was approximately 12 ps. This waveform was measured with a 50 GHz digitizing oscilloscope with rise time of approximately 7 ps hence the resolution on this measurement is on the margin but the measured result is qualitatively close to that expected. The degree of resolution obtained did require a careful, temperature-stabilized calibration of the entire signal path.

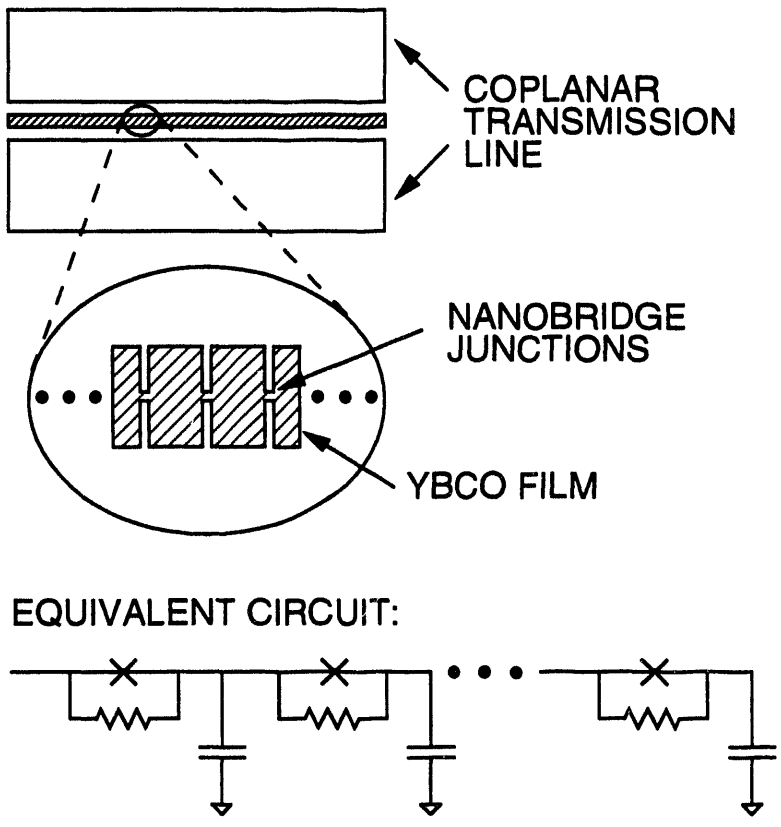

Fig. 6. Schematic illustration of the serial junction Josephson transmission line shock-wave pulse-former and its equivalent circuit.

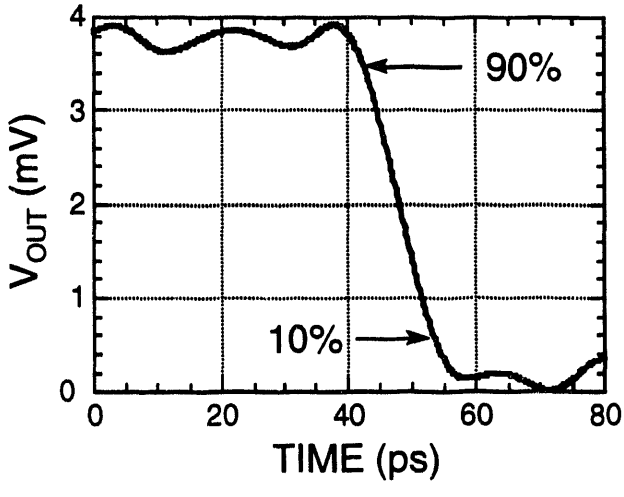

Fig. 7. Falling edge data for a nanobridge serial line measured with a sampling oscilloscope. The result is near the measurement bandwidth limit and the fall time of 12 ps agrees reasonably well with the theoretically expected 10 ps. The input pulse had a rise/fall time of 20 ps and of amplitude 50 μA. A buffer output amplifier was used to obtain the signal shown, the actual step height was approximately 500 μV.

The measured transition time of the falling edge pulses was consistent with theoretical analysis within the limits of granularity and coupling parasitics. This suggests that a significant fraction of the junctions were functioning in each line (estimated to be greater than 80%) and that

their uniformity is quite high. The Josephson inductance followed the expected bias dependencies determined from JSPICE to within about 10%.

32 and 64-bit Shift Registers

There has been considerable work done in rapid single flux quantum (RSFQ) logic in recent years[24,29-31] motivated by speed and power advantages over latching logic and the potential straightforward application to HTS materials. Few complex HTS RSFQ circuits had been demonstrated to date because of problems with the various HTS junction technologies, most notably in the areas of reproducibility and parameter spreads. But the nanobridge junction technology does have yield and uniformity appropriate for incorporation into circuits. A shift register based on the serial manipulation of individual fluxoids is a logical application[32-34] which has significant potential benefits in the areas of speed and power dissipation. Because of this circuit's relative tolerance of variations in circuit parameters, it is an ideal early demonstration of integrated HTS technology.

A block diagram for the general circuit is shown in Fig. 8 as has been discussed in the literature before.[35] It consists of the relevant input and output drivers, a clocking arbitration register, and the main data register. The block diagram was kept quite general since several variations have been used among the circuits tested. The cells of the arbitration and data register are stacked and two versions of the pairing are shown in Figs. 9(a) and 9(b). More details can be found in the literature discussing the LTS design.[35] Operation is quite simple; data are stored in the data registers in the form of the presence or absence of a single flux quantum with attendant circulating current. The inductance of a cell is chosen so that only one quantum is stored. When a clock pulse comes down the clock register, the upper Josephson transmission line, it sends each successive junction momentarily into the voltage state after sending a current pulse down to the data register, the lower Josephson transmission line. If a '1' is stored in the data register, its circulating current plus the clock current causes the junction to switch sending the data bit to the right. The clock pulse is injected from the left so that the junctions switch in the proper order with the help of the arbitration junctions. Timing glitches are possible in such an arrangement and bias margins are tighter than necessary. The second architecture, shown in Fig. 9(b), was used[35] to relieve some of these problems. The buffer stage in each of the cells provides more safety on the timing of the cell switching which enables broader bias margins.

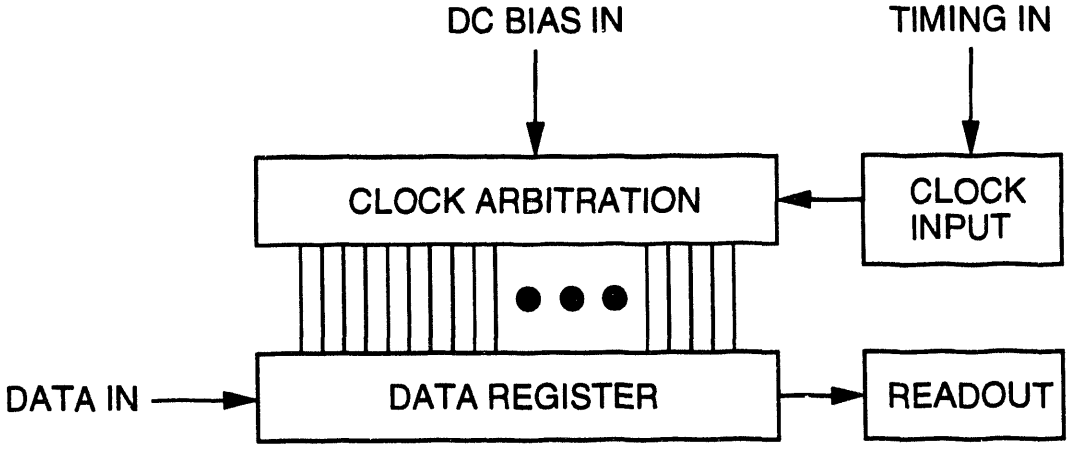

Fig. 8. Block diagram of the shift register. Each stage of the circuit includes a data cell and a clock arbitration cell. The clock input and readout are accomplished in several ways as described in the text.

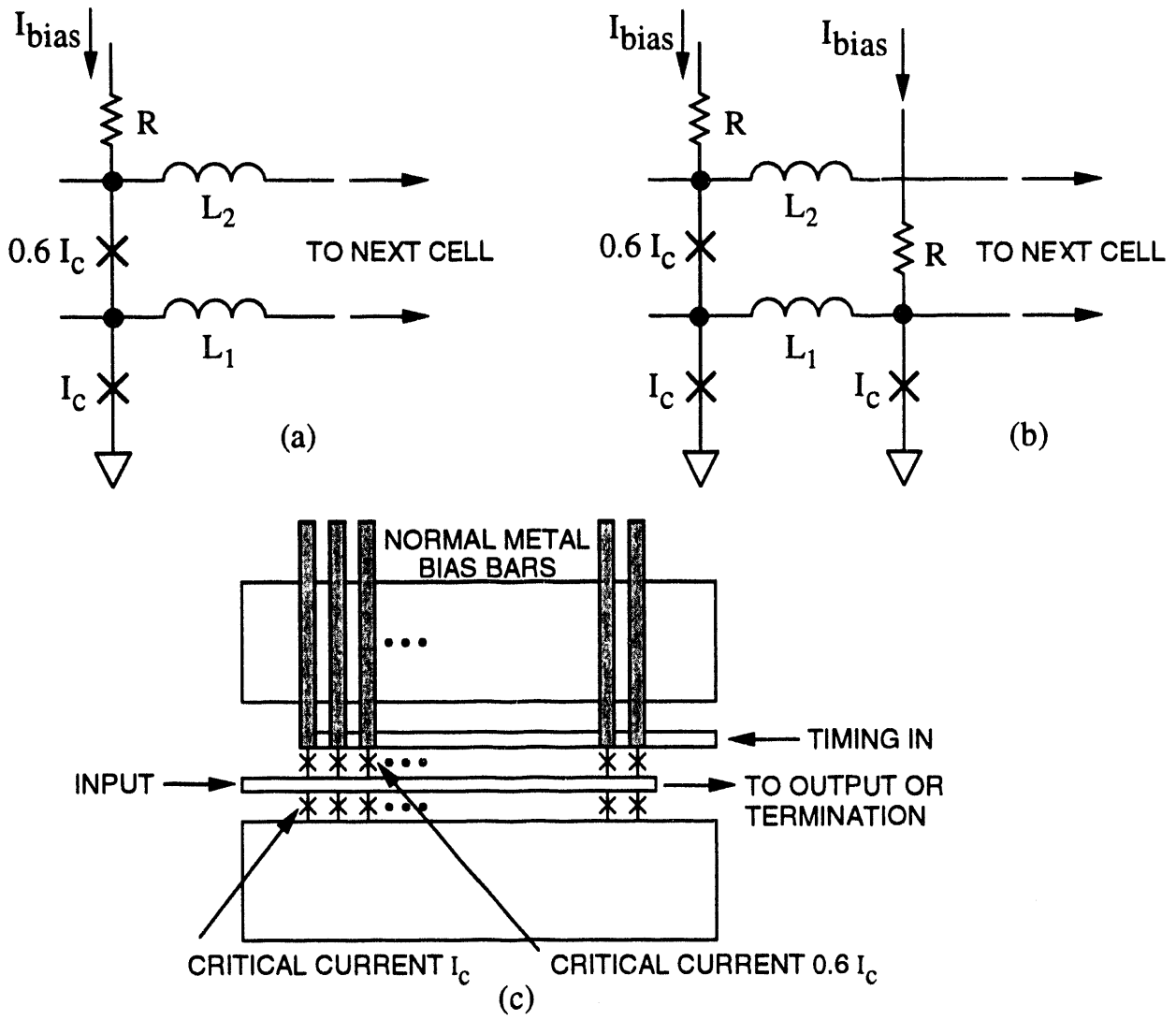

Fig. 9. Equivalent circuits for (a) an unbuffered and (b) a buffered stage of the register. Data is stored in the form of a circulating current between two junctions in the data register. (c) Schematic diagram of the unbuffered shift register design.

A sketch of the layout of a register corresponding to Fig. 9(a) is shown in Fig. 9(c). There is one superconducting layer, separated from the normal metal biasing and ground lines by a polyimide or an amorphous Al_2O_3 dielectric. The ratio of the critical currents between arbitrating and register junctions is basically as shown in Fig. 9(c). The inductance L_1 is nominally chosen such that $L_1 I_c \approx 3\text{-}4 \times 10^{-15}$ Wb and L_2 is chosen primarily to keep the line impedances reasonable but L_2 should be no larger than L_1. The resistance R is less than 0.5 Ω in the sense of wire resistance but there may be a contact resistance term contributing as well.

Clocking was done in two ways as shown in Fig. 10. The DC/SFQ converter is straightforward and generates a single pulse on an input signal of sufficient amplitude. For larger scale clock distribution, a larger pulse amplitude is desirable and Josephson transmission line pulse sharpeners were used as discussed in the previous section. An incoming sinusoid is sharpened and differentiated with a simple LC low pass circuit implemented in coplanar waveguide to form larger amplitude pulses. These pulses were then distributed through resistive dividers to the appropriate clock inputs.

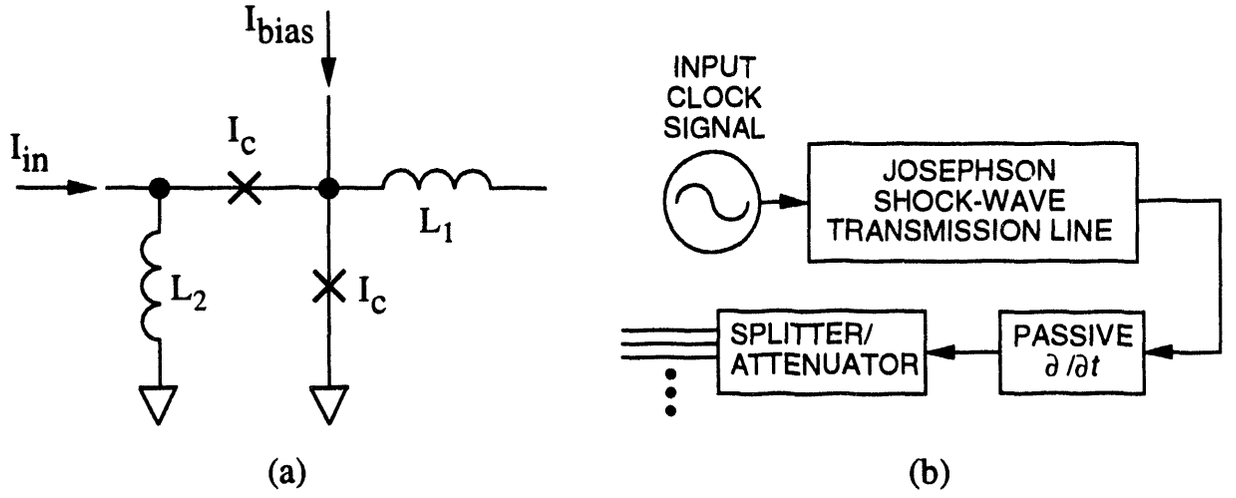

Fig. 10. (a) Equivalent circuit of the DC/SFQ clock input and (b) block diagram of the Josephson shock-wave transmission line approach to clocking. In the first approach, the lower junction produces a clock pulse when the input current rises above a threshold. The second approach produces large pulses suitable for distribution but is not amenable to larger scale integration.

Data readout was also done in several ways. Single SQUIDs were used to read the individual cells (only the last cell in the case of the larger registers) via magnetic coupling. Flip-chip SQUIDs were also used to readout selected cells within the register. These SQUIDs are nanobridge-based YBCO circuits fabricated previously and have a small coupling loop 50 μm in size included. The SQUID is placed physically on top of the register or its upper ground plane and biased separately.

The registers were extensively simulated on JSPICE to determine allowed parameter margins and to evaluate circuit behavior. The individual circuit parameters were varied in a Monte Carlo fashion on limited 4-bit test structures to determine the critical parameters. The critical design margins on the data register I_c and LI_c product were determined to be ±26-30% for the buffered design and ±22-26% for the unbuffered design. Based on the process spreads, it was expected that bias margins, defined as the allowed variation from the optimum bias current on any bias line before the circuit fails, would exceed 20% on the nanobridge circuits.

We present results for two configurations of shift registers, a 32-bit circuit with no buffering, I_c=40 μA, pulse-formed clocking, and SQUID readout; and a 64-bit circuit with buffering, I_c=120 μA (four bridges in parallel), DC/SFQ clocking, and SQUID readout. The shift registers were fabricated on both YSZ and $LaAlO_3$ substrates. When comparison was possible, no substrate dependence was noted. A normal metal ground plane was used on all circuits. An upper, flip-chip mounted, superconducting ground plane was used on most tests since it seemed to reduce noise and cross-talk problems as well as provide a better-controlled inductance. In cases where SQUID coupling to individual cells was needed, holes were introduced into the ground plane. Normal metal bias lines fed each cell in the structure and provided an additional small resistance. Coplanar waveguide feeds were used throughout for high speed data transfers.

The nominal HTS film thickness was 70 nm. Inductances were generally derived from experimental SQUID measurements (on other chips) with inductance levels ranging from 8-10 pH/square. The uniformity on the nanobridge junctions is sufficient to allow unilateral biasing of registers of up to 64 bits in length. The critical currents are low enough, however, that noise-induced false switching is a severe problem. This was partially addressed in the 64-bit register by using four bridges in parallel in a physically small structure to minimize resonances and SQUID effects. Additionally, the critical currents were adjusted, as necessary, using a variation

of the heat treatment discussed earlier. In an iterative process, the entire row of data register junctions was heated with a shielded quartz lamp in an approximately 80% O_2 atmosphere to increase their critical currents slightly so that register performance could be optimized. During this exposure, the other row of junctions was kept somewhat cooler with a radiation shield and liquid nitrogen backing. It was estimated that the average critical current could be increased by 35% in a controlled fashion with negligible increases in parameter spread.

Error rates are an important issue and an estimate can be obtained from a fairly standard analysis of the energy barriers involved.[36] As a coarse estimate, the error rate of a junction is

$$R = Be^{-U/kT} \tag{8}$$

where B is a model-dependent effective bandwidth (nominally between 10^{10} and 10^{12} sec^{-1}), U is the barrier height, and kT is the thermal energy. The barrier height, defined by the Josephson coupling energy is approximately

$$U = \frac{\hbar I_c}{e}\alpha \approx 4I_c \times 10^{-16} \tag{9}$$

where α is a constant between zero and one representing the effective bias point (0.4-0.6 I_c), α goes to 1 as the bias current goes to 0 and is model dependent.[37] At 77K, the exponent is about $-400{,}000I_c$ so for an error rate of 10^{-10} (considered by some to be adequate for communications applications), a critical current of about 120 μA is needed. Thus one would expect the 32-bit register probably not to work well in these applications while the 64-bit register might work acceptably well.

All tests were done at 77K with a cryogenic probe station. All signals were coupled in coaxially with either low speed probes (for bias), moderate speed probes (1-5 GHz bandwidth), high speed probes (40 GHz bandwidth coplanar waveguide), or mm-wave finline probes (50-75 GHz and 75-110 GHz versions). The first three varieties were also used for coupling signals off-chip to a sampling oscilloscope. DC power needs ranged from 20 μA/bit for the 32-bit register to 125 μA/bit for the 64-bit register. Under high speed operation, the DC voltage drop was always less than 5 mV.

A simple and direct low speed test is to load the register at low speed with some random word and then read it out at low speed. This was done with both configurations of shift register. It was not possible to get an error free read-out from the 32-bit register because of thermal noise and a higher than optimum inductance level (anomalous kinetic inductance is suspected). The 64-bit register did provide correct read-out with bias margins of about 15% with the data being clocked at a 100 MHz rate.

One high speed test relies on limited data sets and a very short period clock. A high frequency sinusoid of either 60 or 94 GHz from a Gunn oscillator was fed to the shock line and its differentiator which in turn drove the clock line of the shift register. The result was a pulse train with a period of approximately 16.7 or 10.6 ps, respectively. A step was applied to the input line and the delay to the output of the shift register was measured in a time domain transmission (TDT) measurement using 40 GHz CPW probes for data in and data out and a fin-line to CPW transition for the clock launch. The signal path was calibrated with a short through line on the test wafer to establish the zero on the time scales. The result, shown in Fig. 11 for the 64 bit register used serially, shows a delay corresponding to approximately 64 clock pulses. The full scale output, about 5 mV, was amplified by about 20 dB with a high speed, conventional amplifier off-chip (.005-20 GHz amplifiers are readily available and can be combined with low frequency amplifiers using a simple crossover to cover from DC to greater than 20 GHz). The deviation is probably due to some miscalibration and a crude accounting for pad parasitics on the actual register. Since this was only for one data type (1111...), the test result does not necessarily imply error-free operation at this speed but it does indicate shifting without a flow-through mode. This test was also successfully performed with the 32-bit registers with clock rates as high as

120 GHz. Since the data storage time was so short during this experiment and only a data set of (1111...) was used, many noise induced errors were hidden. It was not a test of complete functionality but provides an upper bound for operating speed.

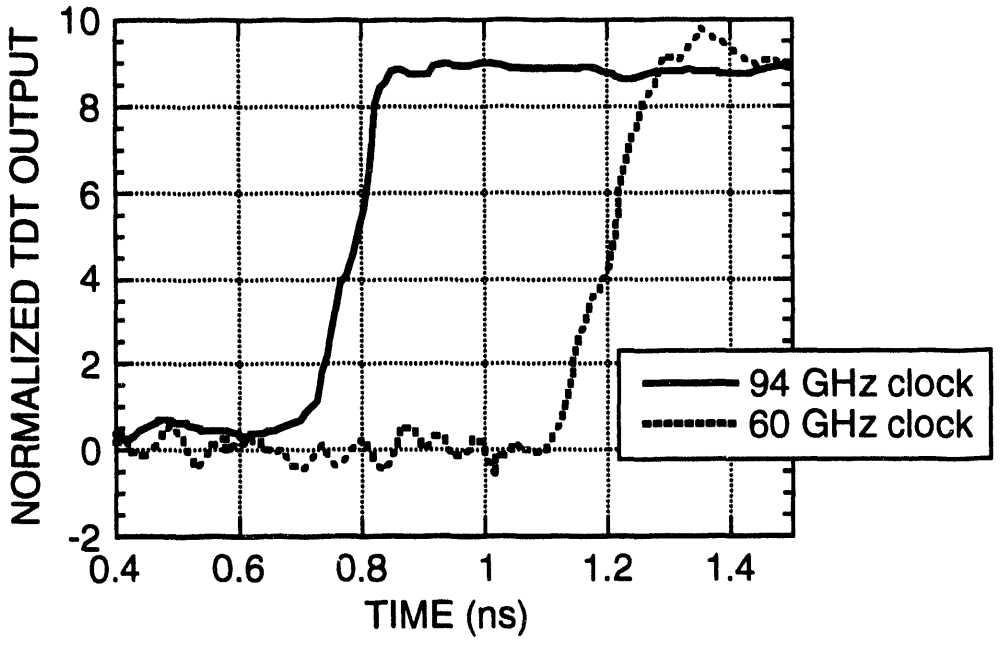

Fig. 11. Time domain transmission measurement of the 64 bit shift register when clocks of 60 GHz and 94 GHz were applied with input data of (1111...). The time delay corresponds almost exactly to 64 clock cycles suggesting that high speed operation is possible.

Although not as practically useful, another test can provide a lower bound on the cell transit time. If the trigger line bias is increased high enough, the register enters flow-through: any input will be shuttled from cell to cell without a trigger pulse because the $I_{data}+I_{bias}$ will exceed the shift threshold alone. A simple time domain transmission measurement was conducted where a step arrived at the data port and was observed at the end of the register. The (total delay)/32 (32-bit register) then gives a minimum intercell shift time. A total delay of about 155 ps was obtained which is consistent with a minimum shift time of slightly less than 5 ps. JSPICE simulations produced an intercell shift time of about 3.5 ps under flow-through conditions.

A more convincing test of high speed performance is a recirculation test. This test used two shift registers connected in a loop as suggested in Fig. 12. The data and clock out lines of register 1 drove the data and clock in lines of register 2. The data out line of register 2 was fed back as the data in line on register 1. The registers were loaded with some arbitrary data and then clocked at a high rate for some period of time, generally a few minutes. The clock was coupled in with fin-line transitions and the two shift registers were flip-chip mounted. This arrangement allowed the necessary high data rates (~100 GHz) while maintaining pulse fidelity. Since the data in and out rates were quite slow, the input/output design was not a major problem. The clock fidelity was not of major importance and its amplitude could be maintained quite easily. The clock signal was brought in with a finline and finline-to-coplanar transition while the data was handled by moderate speed probes. This experiment was performed with the 64-bit registers with a clock frequency of 60 GHz for a period of about 1 minute. Initial data consisting of the three 16 bit words (111111...), (101010...), and (100100...), were tried. The output streams, positioned arbitrarily in the lower register, were amplified off-chip by a conventional

amplifier and are shown in Fig. 13. No errors were detected on these simple tests which were performed at least 20 times for each starting word.

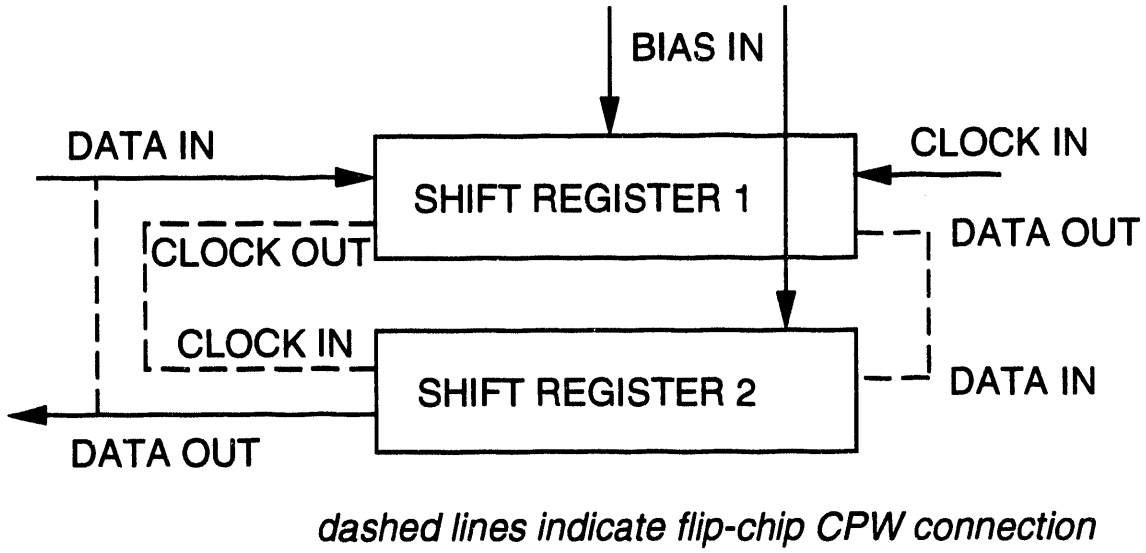

Fig. 12. Block diagram of the recirculation experiment. Data is slowly loaded into register 1 before the pair is clocked at a high rate for a period of time. The data is then slowly clocked out to check for integrity. The two registers are flip-chipped for speed reasons.

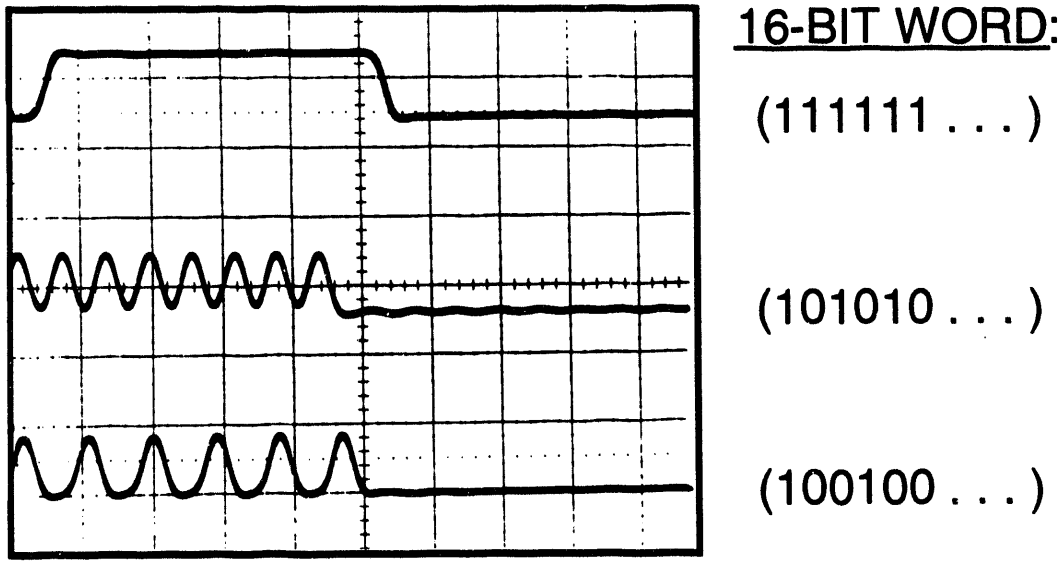

Fig. 13. Final outputs after circulation tests on three input data streams consisting of 16-bit words (111111...), (101010...), and (100100...). The data was clocked in the circulation path at 60 GHz for about one minute.

Summary

We have used electron beam nanolithography in combination with an improved aqueous etch to fabricate superconducting nanobridges in YBaCuO with dimensions of less than 100 nm. Neither the electron beam lithographic process nor the aqueous etch was seen to degrade the characteristics of the YBCO film more than a nominal 5%. Functional junctions exhibited critical currents, I_c, in the range of 20-40 μA with normal state resistances, R_n, in the range of 5-20 Ω, resulting in I_cR_n products of 100-400 μV at 77K. Typical junction to junction spread on I_c was about ± 11% and on R_n, about ± 6% as determined from DC measurements of 100 junctions. The excellent yield and uniformity of this junction technology makes the nanobridge junctions applicable to incorporation into circuits.

We have demonstrated the use of arrays of nanobridge junctions to evaluate statistics of the junctions in a more time efficient manner than individual DC testing. The radiation spectra of the arrays oscillating at 77K and 90-160 GHz allows the extraction of spreads on critical current and normal state resistance which agree very well with those determined from DC measurements. New annealing sequences for nanobridges have also been developed using the arrays as a characterization tool. The iterative adjustment of the process using array performance as feedback enabled a 4 point drop in 3σ critical current spread. It is expected that this technique can be used for further improvements in junction parameter control.

The serial Josephson shock-wave transmission lines clearly sharpened the falling edges of the input waveforms. With a simple passive network, the steep, falling step waveform can be converted into a narrow impulse. The signals generated by these circuits can be a powerful tool for the testing of ultrafast circuits. Because the fabrication technology is compatible with that for SFQ circuits, one may actually build on-chip pulse generators for SFQ circuits.

32 and 64-bit shift registers operating at 77K have been demonstrated to function at high speed. Static random word, TDT shifting, and continuous shift tests were performed and indicated functionality of most, if not all, of the individual shift register cells. Shift times as low as 10 ps were demonstrated for at least some data types and 60 GHz operation for nearly arbitrary data was shown. One minute operation of the 60 GHz clocked registers with no errors suggests error rates below 10^{-12}. Ongoing work includes the fabrication of such circuits as high-speed memories and 4 and 8-bit analog to digital converters (ADC).

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APPENDIX, LDRD Summary

Publications Resulting from this Work:

Wendt, J. R., et al. 1992. "$YBa_2Cu_3O_7$ nanobridges fabricated by direct-write electron beam lithography." *Appl. Phys. Lett.* **61**, 1597.

Martens, J. S., et al. 1992. "High temperature superconducting Josephson transmission lines for pulse and step sharpening." *J. Appl. Phys.* **72**, 5970.

Martens, J. S., et al. 1993. "A High Temperature Superconducting Shift Register Operating at Over 100 GHz." *IEEE J. Solid State Circuits* (accepted for publication).

Martens, J. S., et al. 1993. "The Use of 2-Dimensional Arrays to Determine the Uniformity of Josephson Junctions." *IEEE Trans. on Applied Superc.* **3**, 3095.

Presentations Resulting from this Work:

Martens, J. S., et al. 1992. "High Temperature Superconducting Step-Edge and Nanobridge Junctions: Performance Dependencies, Arrays and Circuits." Paper presented at the Fall Materials Research Society Meeting, Boston, 30 November-4 December.

Martens, J. S., et al. 1993. "HTS Circuits Based on SNS and Nanobridge Junctions." Paper presented at the International Superconductive Electronics Conference, Boulder, 9-13 August.

Martens, J. S., et al. 1993. "HTS Circuits." Paper presented at the Workshop on Superconducting Electronics, Ogunquit, 3-7 October.

Martens, J. S., et al. 1993. "High Temperature Superconducting Digital Circuits and Subsystems." Paper presented at the Government Microcircuit Applications Conference (GOMAC), New Orleans, 1-5 November.

Martens, J. S., et al. 1993. "Electron Beam Defined Nanobridge Junctions: Uniformity, Physics and Applications." Paper presented at the Fall Materials Research Society Meeting, Boston, 29 November-3 December.

Whiteley, S. R., et al. 1994. "HTS Digital Circuits." Paper presented at the SPIE International Symposium OE/LASE '94, Los Angeles, 22-29 January.

Invention Disclosures Resulting from this Work:

1. J. R. Wendt, J. S. Martens, and T. A. Plut, "High Temperature Superconducting Nanobridge Josephson Junctions," SD-5154, S-76,815.

Patents Applied for or Issued Resulting from this Work:

A patent application is currently being processed for the above disclosure.

Copyrights for Software Resulting from this Work:

None

Employee Recruitment Resulting from this Work:

None

Student Involvement in this Work:

None

Number of Awards Resulting from this Work:

None

Number of New non-LDRD Funded Projects Resulting from this Work:

None

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