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DESIGN OF A PIXEL CELL OPTIMIZED FOR A DATA PUSH ARCHITECTURE READOUT*

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A pixel cell has been designed which has been optimized for a data push architecture readout. It retains the features of preceding designs which allow time stamping, analog signal processing, XY address recording, ghost elimination and sparse data transmission. It eliminates a number of problems inherent in previous designs by use of sampled data techniques, destructive readout, and current mode output drivers. This document examines the motivation for this new pixel and covers the theory of operation of the various blocks. A discussion of the tradeoffs affecting speed, power, device size, and radiation stability is included as well.

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TABLE OF CONTENTS

Page

I. INTRODUCTION 2
II. MOTIVATION FOR THE NEW PIXEL 2
A. Architecture Differences 2
B. Chip 5 Pixel Redundancy 3
C. Chip 5 Existing Pixel Potential Problems 3
D. Data Push Pixel Solutions 4
III. THEORY OF OPERATION 4
A. Input Stage. 5
B. Analog Storage 6
C. Pixel Comparator. 6
D. DPA Pixel Multiple Hit Capability. 7
IV. RADIATION STABILITY 8
V. TRADEOFFS AND COMPONENT SELECTION 9
VI. CONCLUSIONS 11
VII. BIBLIOGRAPHY 12

I. INTRODUCTION

The introduction of the "Data Push" detector architecture (DPA) concept [1] has created an opportunity for an improved small area smart pixel based on the Hughes "Chip 5" pixel design. The objective of this document is to examine the motivations for a new pixel, briefly cover the theory of operation of the various blocks, and discuss the tradeoffs regarding speed, power, radiation stability, and component sizing.

II. MOTIVATION FOR THE NEW PIXEL

A. Architecture Differences

The pixel requirements imposed by the new DPA concept are a significant departure from those imposed by the Chip 5 architecture. From the pixel's perspective, the most important difference between the two is that unlike Chip 5, the DPA makes no selection of "interesting data" based on a Trigger Level 1 (TL1) decision, but pushes ALL data off chip for downstream electronics to make this selection. The need to make this selection on chip drove most of the requirements on the Chip 5 pixel, namely, the "time walk" specification and the non-destructive analog-data-read channels.

1. Time walk

The very tight time walk requirement was necessary to determine to which 16 ns interaction time window events of varying magnitude belonged. This selection was to be made by the chip based on a TL1 input signal. Since the pixel was always envisioned as low power (20 μW)

and of small area (50 μm x 150 μm), by necessity it could have circuits of only limited complexity. This constraint made the time walk specification of 16 ns unachievable. The new DPA virtually eliminates this requirement, since ALL data is sent off chip, and can be "back annotated" for time based on the analog signal magnitude.

2. Non-destructive analog read channel

The need to make the selection of "interesting data" on chip meant that the analog data stored in the pixel was to be accessed more than once. The first time, the data was to be used for "ghost elimination" in the periphery. Then it was to be accessed again once it was deemed "interesting" for readout to the system. This multiple access capability requires a non-destructive read process, involving source follower buffers and their inherent problems. These problems will be discussed in more detail in a later section.

The new DPA accesses the analog data only one time. During this access, "ghost elimination" is accomplished, and the data is simultaneously sent off chip to the system pipeline. This allows a destructive read process which eliminates many of the problems associated with the Chip 5 analog read channel.

B. Chip 5 Pixel Redundancy

The Chip 5 pixel is designed to send out an XY address when a hit occurs. Unfortunately, a "ghost" problem develops when more than one hit occurs on the chip, provided they are not in the same column or row. To solve this problem, Chip 5 is equipped with a "ghost discriminator" periphery. After the digital hit signals are received by the periphery, the chip systematically enables each hit column, records the status of the analog data in the pixel, and then compares this with the contents of the "hit row" register. Whenever a discrepancy occurs, the location is deemed a "ghost" and is eliminated from the "real event" category.

It can be shown that, for multiple hits, the "hit row" digital signal from the pixel is redundant, since the same operations are required whether that signal is present or not. The hit row signal uses ~3% of the pixel area, but, more importantly, requires a horizontal digital signal line. Eliminating this redundant signal would free up valuable pixel area, and reduce the risk that pixel-to-pixel crosstalk would trigger the entire array when only one pixel is hit.

C. Chip 5 Existing Pixel Potential Problems

1. Threshold non-uniformity effects

A common ailment of CMOS is the threshold non-uniformity of the MOSFETs. For a 1 cm^2 chip, a peak-to-peak threshold variation of > 200 mV can be expected across the chip. For a 10 fF integration capacitor, a 2000 e- threshold corresponds to 32 mV. It is obvious that a single source-follower buffer's threshold variation would swamp the minimum size signal which we are trying to detect at the ghost discriminator periphery. For this reason, the Chip 5 pixel used a differential source follower in the analog channel in order to capitalize on better localized device matching. Subsequent studies by M. Wright and F. Forti have measured an effective mismatch σ of ~44 mV-μm/$\sqrt{WL}$. For the 10 μm/1.6 μm source followers in the Orbit process, this mismatch works out to a σ of ~11 mV, corresponding to a peak-to-peak value (6 σ) of ~66 mV, which is still larger than the minimum signal. The problem is exacerbated by the fact that the ghost discriminator is also a differential circuit with a V_t mismatch of its own which adds to the error as the Root Sum Square.

To first order, to reduce the peak-to-peak errors to a desired value of 10% of the signal, or ~3 mV (200 e-), would require differential source followers with a gate area of 2 x 7700 μm^2, which would occupy slightly more than double the area of the whole 50 x 150 μm^2 pixel. To reduce the σ to 3 mV, a gate area of 2 x 215 μm^2 is needed, or a total area of 800 μm^2 (source and drains almost double the needed area). This will take up more than 10% of the total area of the cell just for the readout source followers, which is clearly unacceptable. Even if this 3 mV σ V_t mismatch reduction were accomplished, it would still have serious effects on the threshold of the ghost discriminator periphery. Radiation effects would only make matters worse.

2. Voltage mode Hit_Row, Hit_Col signals

The digital pixel outputs were originally designed for full 5 V voltage mode operation. The transistors were designed and fabricated with large W/L ratios for high speed charging and discharging of the output lines. When testing Chip 4, a false triggering of the entire column occurred when only one pixel was hit. This crosstalk was attributed to the high voltage swing of the Hit_Col lines, since only a stray capacitance of 7 x 10^{-17} F between the output and input is needed to generate a 2000 e- signal. It is practically impossible to eliminate 0.07 fF stray capacitors, since this is equivalent to a capacitance between two parallel 1 μm long metal lines.

Chip 5 was redesigned to function with 100 mV Hit_Row and Hit_Col voltage signals from the pixel. This reduces the false triggering risk by a factor of 50, since Q = CV, and V has decreased by 50. It is difficult to reduce the signal below 100 mV, since threshold non-uniformity effects begin to dominate. Also, additional level-shifting circuitry is required, which introduces more delay (~50 ns), though with negligible time-walk.

Lower delay and signal voltage swing are desirable, but cannot be accomplished with voltage mode outputs. A current mode output scheme can reduce the delay to 10 ns, and the voltage swing to 5-20 mV. The Chip 5 pixel outputs, however, are not suitable for current mode operation, and a redesign would be necessary.

D. Data Push Pixel Solutions

The new DPA pixel can address all of the deficiencies of the Chip 5 pixel. To eliminate the redundancy of the Hit_Row signal, the corresponding circuitry need only be removed. Since the DPA allows destructive read of analog data, virtually all of the threshold mismatch and non-uniformity issues can be removed through sampled data techniques (i.e. resetting). In addition, while the Chip 5 pixel uses 7 FETs, 2 capacitors and 6 lines to implement analog voltage storage, the destructive read with correlated double sampling (CDS) charge storage can be implemented with 1 FET, 1 capacitor and 2 lines.

The digital Hit_Col signal can simply be designed as a current mode signal. The expected voltage swing is around 10 mV and the current-to-voltage conversion time delay is expected to be about 10 ns.

III. THEORY OF OPERATION

The new DPA pixel is being designed to work with the existing LBL silicon PIN detectors, which collect holes. Figure 1 shows the proposed schematic and block diagram of the pixel. It consists of 14 FETs, 5 capacitors and 15 lines. This compares with 22 FETs, 7 capacitors and 20 lines for the Chip 5 pixel. It is hoped that the reduced component count will enable the layout of a more robust and smaller area pixel, with much of the area reduction being in the smaller 50 μm dimension.

For simplicity, and to keep from getting bogged down in a description of secondary effects, the following assumptions and simplifications have been made in the explanation of operation:

1. $V_{ds\ sat}$ of MOSFET = 0 V.
2. MOSFETS used as switches are ideal switches with 0 R_{ds} and no capacitive feedthroughs.
3. Source follower gain is assumed to be 1.0.
4. Inverter input switching voltage is 4.1 V.
5. Infinite inverter gain.
6. Clock rise and fall times of 0 ns.

A. Input Stage

The input stage consists of FETs M1 through M7 and capacitors CIN and CFB. The detector charge collection node is the gate of M1. Transistors M1, M2 and M3 form a single stage cascoded inverting amplifier. M4 is the reset switch, and CFB is the feedback integration capacitor for the detector charge. M6 and M7 form a source-follower buffer stage. M5 and CIN are used during testing for detector simulation, for active dynamic range control, and for leakage current compensation during chip operation.

To operate the front end, RST goes high and resets the input and output of the amplifier to $-V_{tn}$. After the reset is complete, RST goes low. All this time, the source of M7 is following the drain of M2, but 1 V_{tp} above. Assuming that the magnitudes of both V_{tp} and V_{tn} are 1 volt, then the drain of M2 is 1 volt, and the source of M7 is 2 volts at this point. Since the pixel is collecting positively charged holes, the dynamic range of the pixel at this point would be slightly less than 1 volt. (The drain of M2 would rail out, approaching ground.)

In order to extend the dynamic range, we use the conveniently present input test circuit of M5, VIN and CIN. During chip operation, all VIN nodes and IN_SEL nodes would be selected, such that the VIN signal would be a common signal to all pixels on the chip. Just after the RST goes low, VIN also steps low. Since the input is a gain stage with a gain of -1 from VIN to the drain of M2, the magnitude of the downward VIN step would be ~1 volt. This would change the drain of M2 from 1 volt to 2 volts, and the source of M7 from 2 volts to 3 volts. Thus, the new dynamic range would be ~2 volts.

The circuit can also be used to subtract the detector leakage current after radiation damage. The detector leakage would be in the form of holes, so a negative going ramp on VIN such that $CIN \times (dVIN/dt) = I_{lkg}$ would subtract the leakage carriers. In this case, VIN might start at 3 V, step to 2 V for dynamic range adjustment, and then ramp down toward ground to counter the effects of leakage carriers. Here then, IN_SEL would have to be > 4.5 VDC.

During testing, IN_SEL and VIN would be selectively addressed, such that only pixels of interest would be activated. Once the input stage has settled, VIN would ramp high by a specified amount (e.g. 32 mV to simulate a 2000 e- signal). Since the gate of M1 is a virtual ground, the voltage ramp on VIN would simulate a detector current through CIN ($I_{cap} = C(dV/dt)$).

B. Analog Storage

The analog storage block is made up of the capacitor Ccds and the read switch M8. The circuit is designed to operate with a charge sensitive amplifier (CSA) connected to the node A_OUT. During chip reset, M8 is on until the input stage settles. Once the voltage on the source of M7 is stable, RD goes high and turns M8 off. Thus, the voltage difference between the CSA input voltage and M7 source voltage (preamp output voltage) is stored across the capacitor Ccds. When a hit occurs in the pixel, both Ccds nodes move down. For a signal of 25,000 e-, a change of 0.4 V would occur.

To read the analog signal, RD is brought low and turns M8 on again. The CSA will now read out a signal proportional to the charge stored on Ccds, which is Ccds × dV. Notice, that the read operation simultaneously resets Ccds as the CSA "sucks" the charge out of the pixel. Once the read is completed, RD goes high and shuts M8 off. Notice that once again, the voltage difference between the CSA input voltage and M7 source voltage is stored across Ccds.

Normally, a complimentary read switch would be used to cancel clock feedthrough effects on Ccds, but an extra N-channel MOSFET would nearly double the line capacitance of A_OUT. The speed of the Charge Sensitive Amplifier (CSA) on the periphery is inversely proportional to the line capacitance, so we must use only a single switch. Since the clock feedthrough now introduces an almost constant pedestal to the signal, it can be calibrated and subtracted by the downstream electronics.

The read operation is destructive, since there is no way to read the previously stored charge a second time. However, there are no threshold non uniformity problems, since the same CSA is always used, and any threshold offset of the input stage is subtracted by the CDS. Until the dynamic range is exhausted, there is no need to reset the input stage of the pixel for subsequent hits, since the analog storage block only stores the latest voltage difference on Ccds.

The CDS also performs the important function of eliminating the $\sqrt{(kT/C)}$ reset noise of the 10 fF CFB which, unremoved, would add ~40e^- (650 μV). Though an unremoved 117 μV noise contribution will be present due to the reset of Ccds, it only corresponds to ~7 e^- and is negligible.

C. Pixel Comparator

The comparator consists of transistors M9 through M14 and capacitors CTH and CAC. M11 and M10 form an inverting gain stage. M12 and M13 form an inverter for additional gain. M14 converts the voltage at the drains of M12 and M13 into a current signal to the periphery. This comparator is designed to work with a low input impedance current to voltage converter on the chip periphery.

The operation of the comparator is similar to that of the analog storage in that the comparator is AC coupled and responds only to changes in voltage. During chip reset, both the input preamp and the comparator are reset. While RST is high, RST_COMP is low, forcing the gate of M11 and drain of M11 to the same voltage of 4 V. Assuming the switching point of the inverter to be 4.1 V, the drain of M13 will be at 5 V, and M14 will be off. The RST_COMP stays low until the source of M7 settles from the reset and the VIN dynamic range control pulse. Notice that again, the voltage difference between the source of M7 and gate of M11 is stored across CAC.

If CTH were not present, then RST_COMP going high and turning M9 off would leave the comparator precisely at threshold. Any voltage fluctuation of the source of M7 in the negative direction would bring the drain of M11 to 5V, drain of M13 to 3V, and turn on M14.

Table I. Proposed DPA Pixel Specifications

	Needed	Goal
Pixel size (μm)	50 × 150	40 × 120
Power budget (mW/cm^2)	< 500	< 300
Time walk [4 ke$^-$ - 25ke$^-$](ns)	< 100	< 50
25 ke$^-$ delay [Idet-Hit_col](ns)	< 100	<50
Total Noise [Pre rad](e$^-$)	< 200	< 100
Dynamic range (e$^-$)	50 k	> 100 k
Pixel comparator reset time (ns)	< 100	< 50
Chip reset time (ns)	< 1000	< 500
Radiation tolerance (MRad)	0.8	> 1
Analog data read time (ns)	50	< 40
Pileup [hits without preamp reset]	3	5

To create a threshold of 32 mV (2,000 e-), CTH is present. As RST_COMP goes high, CTH and CAC form a capacitive voltage divider. The voltage change on the gate of M11 will be -CTH/CAC times the magnitude of the RST_COMP pulse. For the values shown, a 3 volt RST_COMP pulse would create a threshold of 30 mV, the gate of M11 would then be at 4.030 V. In reality, the stray C_{gs} capacitance of M9 (~.5 fF) adds in parallel to CTH. Thus, a 37 mV threshold would be established with the true capacitive divider. In addition, the RST_COMP voltage pulse height can be controlled off chip, thus allowing precise control of the comparator threshold.

After the comparator fires, RST_COMP is brought low again to reset the comparator. Again, the difference between M7 source and M11 gate is stored across CAC. Thus, the comparator can be reset without the need to reset the input stage, and can again operate on the next change in voltage on M7 source.

D. DPA Pixel Multiple Hit Capability

The DPA pixel can process multiple hits without having its input stage reset. Since the output dynamic range has been shown to be ~2 V, and a typical particle will generate ~25 ke- (0.4 V), it is obvious that the pixel can process up to five events in a "staircase" pattern before needing to be reset. After each event, the pixel is read out, resetting the analog storage block and the comparator. Since both blocks operate with CDS, the difference between their nominal voltages and the new input stage output voltage is stored across Ccds and CAC. Thus, after a read and a comparator reset, the pixel is again ready. The timing waveforms for the complete pixel operation are shown in Figure 2. Table 1 shows the proposed design criteria for the pixel.

IV. RADIATION STABILITY

Although the radiation environment envisioned for the DPA pixel is less hostile than that for the SDC pixel [2], a total dose radiation tolerance of ~1 MRad is still desirable. The pixel presented so far is DC coupled to the PIN diode detector. This implies that any detector leakage current is integrated along with particle hit signals. Since the comparator can only be reset every 10 μs and still retain a >99% live time, the threshold being 2,000 e- and Q = It, a current of only 32 pA/pixel will trigger the comparator. With detector dimensions of 50 x 150 x 300 μm^3 this current will occur at a fluence of only 4.7×10^{11} particles/cm^2, corresponding to ~28 kRad. In addition, if the radiation effect is to be kept to no more than 30% of a minimum signal, or 600 e-, the radiation hardness drops to ~8 kRad. [3] Clearly, some kind of compensation scheme is necessary.

By applying a negative going voltage ramp on VIN and CIN, the CdV/dt current can be made to compensate for the radiation leakage current from the detector. For maximum radiation tolerance, CIN should be as large as possible for maximum current. However, for other reasons discussed below, CIN must be kept below 43 fF.

In the analysis, the following assumptions have been made:

1. Detector damage coefficient $A = 3 \times 10^{-17}$ Amps/cm
2. 1 μs chip reset time (max).
3. Maximum voltage ramp is 3 V
4. Detector dimensions are 50 x 150 x 300 μm^3 (2.25×10^{-6} cm^3)

Since the chip dead time should be kept to about 1% maximum, the minimum reset time for the front end is 100 μs. Then the maximum leakage current that can be compensated for is $I = CdV/dt = 40$ fF × 3 V / 100 μs = 1.2 nA per detector or 1.2×10^{-9} Amp/2.25×10^{-6} cm^3 = 533 μA/cm^3. Using I = F x A, where F is the fluence in particles/cm^2, A is the damage coefficient and solving for F, F ~1.78×10^{13} particles/cm^2. This fluence corresponds to ~1 MRad. Thus, the pixel can now tolerate 1 MRad, provided the actual devices are still functioning, and the radiation damage is uniform across the 1 cm^2 array of pixels.

Note that the voltage ramp on CIN cancels only the DC component of the leakage current. This means that the shot noise of the current is not taken out. For a current of 1.2 nA at 1 MRad, and a comparator reset period of 10 μs, the shot noise is $(1.2\ nA \times 10\ \mu s/q)^{1/2}$, or ~300 e-. Thus, the integrated leakage shot noise on the comparator will dominate the noise of the pixel at 1 MRad, provided the FET noise does not degrade significantly with radiation. This may force us to raise the comparator threshold from 2000 e- to 3000 e- or more.

Another aspect of this method, that is not obvious, has to do with CIN uniformity across the array. Since only one voltage ramp per chip is envisioned, capacitor uniformity is just as important as detector damage uniformity. For the numbers that have been considered (1.2 nA leakage at 1 MRad, 600 e- threshold variation, 10 μs comparator reset time), the capacitor uniformity must be 600 e-/(1.2 nA × 10 μs)=0.8%. However, as the radiation levels go beyond 1 MRad, this already tight tolerance must be surpassed.

It is important to note the behavior of the pixel as the 1 MRad threshold is surpassed. Again, assuming the rest of the circuit is functioning and the damage is very uniform, the ramp must become steeper than 3 V/100 μs. By allowing the reset period of the chip to go below 100 μs, it will still function. In other words, after 1 MRad, the chip dead time will begin to slowly increase from 1%. For 2 MRad total dose, the chip will exhibit a 2% dead time, and the noise will increase by 40%. In addition, to reduce the need for capacitor uniformity beyond 0.5% for radiation levels beyond 1 MRad, either the threshold of the comparator may be increased to 4 ke-, or the comparator reset interval can be reduced from 10 μs to 5 μs or both. By reducing the comparator reset interval, the chip will again exhibit a 2% dead time, but both the need for capacitor uniformity and the effective noise of the pixel will be reduced. For a 2 MRad total dose, a 3 ke- threshold, a reset interval of 5 μs, the CIN uniformity can be 1.2% and the noise due to the leakage current would remain at $(2.4\ nA \times 5\ \mu s/q)^{1/2}$, or about 300 e-, retaining a threshold-to-noise ratio of ~=10.

The effects of noise due to leakage current on the analog storage block are more pronounced. The analog block will be reset only when the column is read out, or every 64 μs on average. This implies that the noise due to leakage current will on average be $(1.2\ nA \times 64\ \mu s/q)^{1/2}$ or ~700 e- at 1 MRad. At 2 MRad it will increase to ~1000 e-. The spatial resolution determined by the use of charge sharing based on this analog information would gradually degrade with radiation at these total dose levels.

V. TRADEOFFS AND COMPONENT SELECTION

a. Driver M1

The driver W/L selection affects the noise and speed performance of the pixel front end. In this design, the noise of the front end is dominated by the noise of the driver M1. The major components of the MOS device noise are 1/f and thermal. 1/f noise is proportional to ~1/WL of the device, and the thermal noise goes as $gm^{-1/2}$. It can be shown that a noise minimum occurs when the driver gate capacitance is equal to the total input node capacitance [4], which in this design is ~100 fF. To obtain the optimum noise performance, WLCox = 100 fF. To minimize thermal noise, maximize gm, which is proportional to $(W/L)^{1/2}$. We choose L to be minimal at 1.2 μm, and W to be 54 μm. The gate oxide is assumed to be 225 Å thick, and $\varepsilon_{ox} = 3.9\ \varepsilon_0$. To optimize speed, we need the highest gm. This is consistent with optimum thermal noise.

b. Cascode M2

Two criteria drive the choice of the cascode W/L. The cascode must have a high enough gm to keep the Miller effect to less than 10% of the effective feedback (CFB × Gain), and must have the lowest drain capacitance possible to allow high speed.

To calculate the minimum W/L needed in strong inversion (worst case), we use a conservative gain of 200 for the preamp, and a conservative gate-drain capacitance of half of the gate capacitance, or 50 fF. The effective capacitance presented to the detector is CFB times the Gain of the preamp, or 10 fF × 200 = 2 pF. Thus, the Miller effect must be less than 200 fF. The gain at the drain of M1 is $\sim 2 \times (W1L2/L1W2)^{1/2}$ [5]. Thus, to keep the gain below (2 pF × 10%)/50 fF = 4, and assuming that L1 = L2 = 1.2 μm, the minimum W2 is 13.5 μm. Thus, the minimum W/L dimensions of the cascode are 13.5 μm/1.2 μm. The highest

gm/C_{drain} ratio is obtained with the smallest annular gate, which in the MOSIS 1.2 μm rules, is W/L = 19.2 μm/1.2 μm.

c. Current Source M3

M3 needs to provide enough resistance for proper functioning of the gain stage. An open loop DC gain of 1000 (60 dB) is desirable. Gain can be expressed as $gm_1 \times R_{ds3}$. Using channel length modulation, $\lambda = 0.01\ V^{-1}$ for a 10 μm gate length, and a current of 2 μA, $R_{ds3} \sim= 1/g_{ds3} = 1/\lambda I_d = 50\ M\Omega$. Since M1 is in sub-threshold, $gm_1 = I_d/[n(kT/q)]$. Using $I_d = 2\ \mu A$, n = 3 (worst case) and T = 300°K, $gm_1 \sim= 25$ μmho. Thus, a 10 μm long device provides an open loop DC gain of 25 μmho × 50 MΩ, or 1250 (62 dB).

d. CFB

The feedback capacitor should be the smallest that can be made with reliability and uniformity. The conservative value is about 10 fF. While values of 4 fF have been reported by Rockwell, and 1/2 fF by LBL, these would not be considered conservative values.

e. CIN

CIN must not significantly impact the noise of the pixel. Since noise is proportional to $CIN_{TOT}^{1/2}$, to keep the noise contribution of CIN to 10% of total, CIN must be less than 43 fF. A 40 fF CIN, chosen earlier, meets this requirement.

f. Source Follower Buffer M7

The source follower should be large enough to drive the load Ccds and settle to 8 bits in 30 ns or less. For Ccds of 0.3 pF, M7 must have a gm of at least 60 μmhos. Since $g_m \sim= (2C_{ox}\mu_o I_{ds} W/L)^{1/2}$, and choosing a current of 3 μA and L = 2 μm, W must be at least 24 μm. The carrier mobility at the surface μ_0 is~400 $cm^2/V\text{-}s$.

g. Current Source M6

M6 needs to provide enough resistance for proper functioning of the source follower. Its R_{ds} should be > 5 × R_{ds} of M7. Since R_{ds} goes as L_{eff}, and using Lateral Diffusion (LD) ~= 0.13 μm, $L_{eff6} = 5L_{eff7} \sim= 10$ μm.

h. Comparator Driver M11

The comparator reset time should be less than 25 ns for an overall column access time of 100 ns. The maximum signal the comparator is expected to see is 50 ke-, or 0.8 V. To settle to 10% of threshold, or 3 mV, we need ~6RC, where C = 0.25 pF, and $R = 1/gm_{11}$. Thus, the minimum g_m must be 6 × C/25 ns or 60 μmhos. Using a drain current of 2 μA and L = 1.2 μm, the minimum W is ~12 μm.

i. Current Source M10

M10 needs to provide enough resistance for proper functioning of the gain stage. It's R_{ds} should be $> 5 \times R_{ds}$ of M11. Since R_{ds} goes as L_{eff}, and using LD~= 0.13 μm, $L_{eff10} = 5L_{eff11}$ ~= 5 μm.

j. CTH and CAC

Capacitors CTH and CAC form a voltage divider that is used to set the threshold of the comparator. Assuming that they divide a 3 V clock pulse, and a ~30 mV threshold is desired, a 100:1 ratio is needed. To choose CTH, we must choose the smallest uniformly manufacturable capacitor. Based on experience with Chip 4, 2 fF is a reasonable choice. This forces CAC to be 200 fF.

k. Ccds

The Ccds capacitor must be large enough not to be dwarfed by the parasitic line capacitance of A_OUT, which is estimated to be 4 pF. Also, it needs to be large enough to be insensitive to the radiation leakage current of M8. Scaling the detector leakage current by the ratio of volumes, and assuming the volume of the source junction to be 0.5 μm x 4 μm x 4 μm = 8 μm^3. The detector volume is 50 x 150 x 300 μm^3 = 2.25 x 10^6 μm^3, so M8 leakage current is 1.2 nA $\times$ 8/(2.25 $\times$ 10^6) = 4.3 fA. To be conservative, assume readout silicon damage is 10 times worse than that of the detector, so leakage is ~50 fA. With a 100 μs reset period, and a max 3 mV change in voltage, C = Q/V = 50 fA $\times$ 100 μs/3 mV, or 1.7 fF. Thus, the first limit of not being swamped by the 4 pF line capacitance is the deciding factor. A choice of 0.3 pF seems reasonable.

VI. CONCLUSIONS

A new pixel cell concept has been presented which is consistent with a Data Push Architecture concept. It retains those aspects of preceding designs which allow time stamping, analog signal processing, XY address recording, ghost elimination and sparse data transmission. It eliminates a number of problems inherent in previous designs, such as threshold mismatch and nonuniformity issues, potential crosstalk due to large voltage swings, and dead time effects due to frequent front end resetting, by the use of sampled data techniques, destructive readout and current mode output drivers. A discussion of the trade-offs affecting speed, power and device size has been included in this document for clarity.

The simplification achieved by not having to re-read the analog data within the pixel, and the use of current mode output drivers has reduced the device count within the pixel dramatically. This design will be implemented in a pixel which is 50 μm x 150 μm at first, so that it can be bonded to already existing PIN detector arrays, however, the reduced device count will allow for a much smaller pixel area for the final device.

The Radiation hardness specification for this new pixel is set at 1 MRad. This specification is, however, not a hard one, in that the device lifetime can be extended beyond this total dose at the expense of either chip dead time and/or noise performance. The chip will be designed using the Hewlett-Packard 1.2 μm process design rules, so that the migration path to presently existing 1MRad hard processes is clear. The development at Texas Instruments of a new

1 MRad, 0.8 μm SOI process which will have the same noise characteristics as today's bulk CMOS processes is exciting, but is not exploited in this pixel design.

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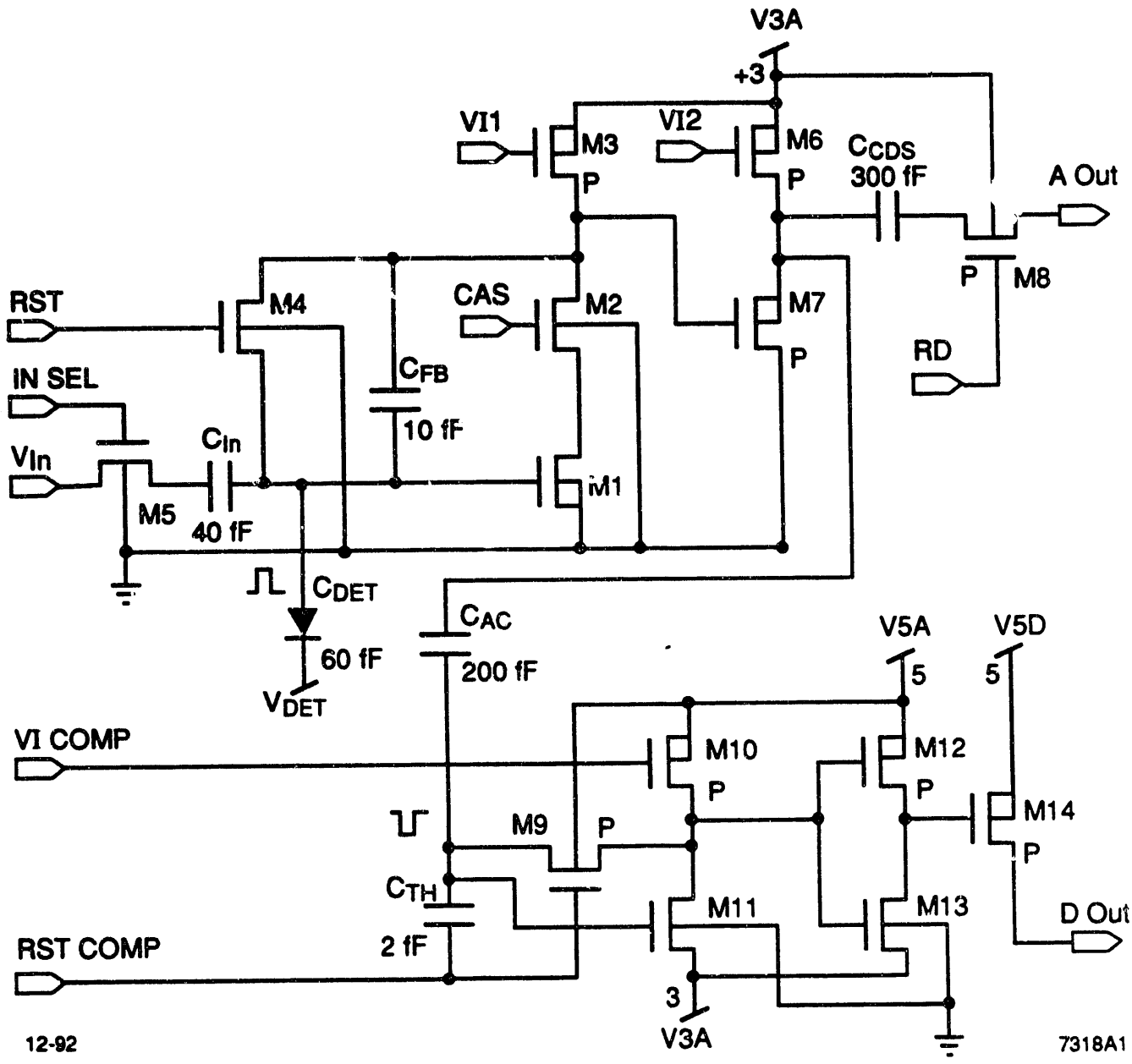
V3A
+3
VI1
M3
P
VI2
M6
P
CCDS
300 fF
A Out
P
M8
RD
RST
M4
CAS
M2
M7
P
IN SEL
CFB
10 fF
VIn
CIn
M5
40 fF
M1
CDET
60 fF
VDET
CAC
200 fF
V5A
5
V5D
5
VI COMP
M10
P
M12
P
M14
P
M9
P
CTH
2 fF
M11
M13
D Out
RST COMP
3
V3A
12-92
7318A1

Fig. 1

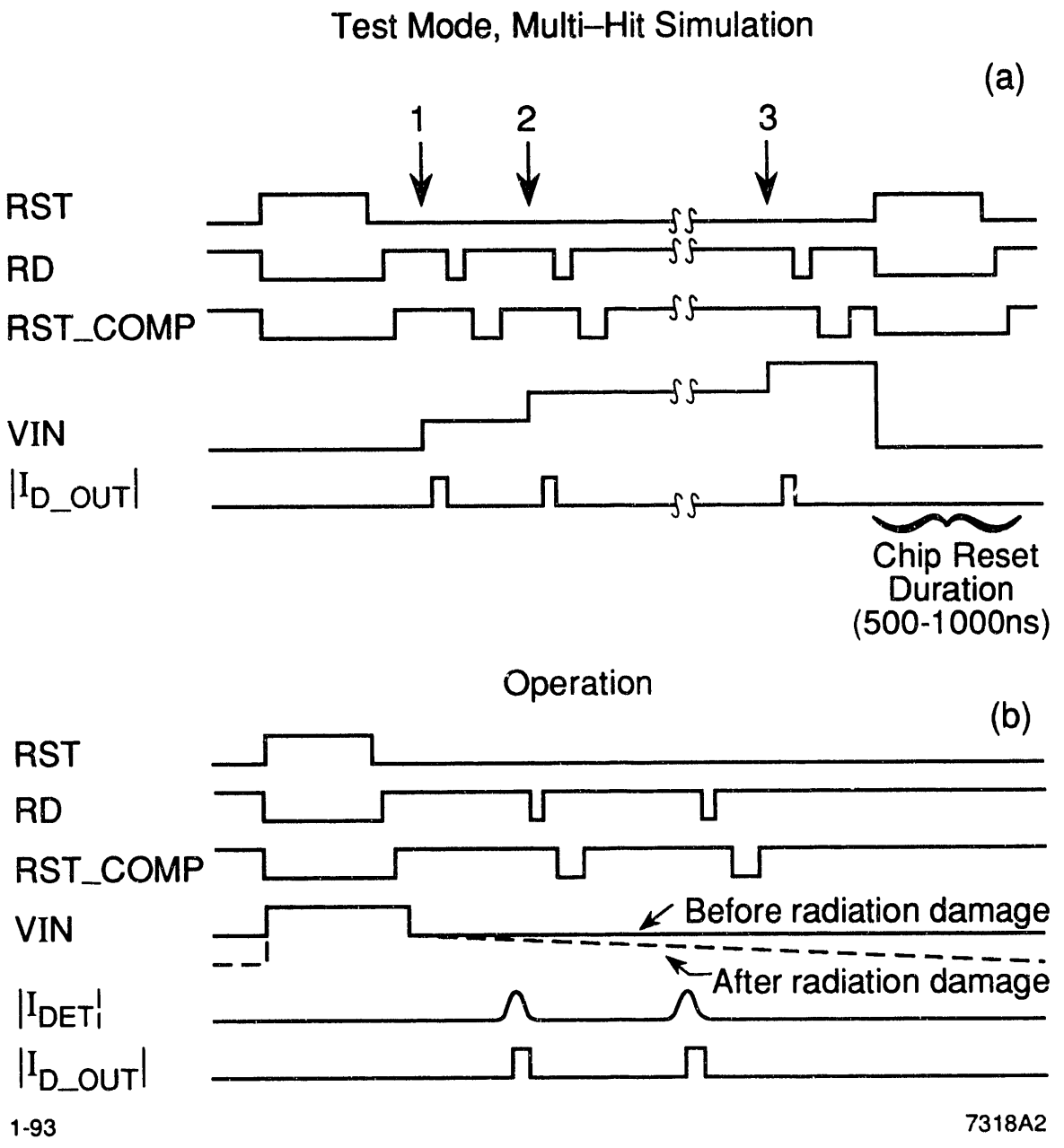
Test Mode, Multi–Hit Simulation
(a)
1
2
3
RST
RD
RST_COMP
VIN
|I_D_OUT|
Chip Reset
Duration
(500-1000ns)
Operation
(b)
RST
RD
RST_COMP
VIN
Before radiation damage
After radiation damage
|I_DET|
|I_D_OUT|
1-93
7318A2

Fig. 2

END

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