TEMPERATURE-HUMIDITY-BIAS AGING TECHNIQUE TO IDENTIFY DEFECTIVE SURFACE MOUNT CAPACITORS

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SUMMARY

Ceramic chip capacitors can potentially crack due to thermal stresses in a surface mount assembly process. The electrical performance of the cracked capacitors will degrade with time, and they will prematurely short. In high reliability applications, the cracked capacitors must be identified and eliminated.

We have developed and demonstrated the temperature-humidity-bias (THB) aging technique to identify cracked capacitors. The initial phase of the study involved setting up automated test equipment to monitor 100 surface mounted capacitors at 85% relative humidity, 85°C with 50 volts dc bias. The capacitors subjected to severe thermal shock were aged along with control samples. Failure mode analysis was done on the failed capacitors. The capacitors with surface cracks short-out within the first 8 hours of aging, whereas the capacitors that failed after a longer aging time (8 to 1000 hours) had a shorting path in an internal void. Internal voids are typical defects introduced during manufacturing of multilayer ceramic (MLC) capacitors. In the second phase of the study, we used the THB aging technique to study the effect of surface mount processes on capacitor cracking and, thus the reliability. The surface mount processes studied were vapor phase, infra-red (IR) and convection belt reflow soldering. The results showed that 6.3 % of vapor phase soldered capacitors, and 1.25% of the IR and convection belt soldered capacitors had cracks. In all capacitors, regardless of the solder process used, an additional 3 to 4% of the capacitors failed due to a shorting path in the internal void. The results of this study confirm that this technique can be used to screen cracked capacitors and compare different solder and manufacturing processes.

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INTRODUCTION

Many surface mount studies have focused on the solder joint reliability concerns caused by cyclical thermal loading, but relatively little attention has been given to the component damage that occurs during an actual surface mount process. A typical MLC is made up of barium titanate based dielectric ceramics with interleaved layers of palladium-silver electrodes and a termination which also consist of Pd/Ag alloys, a nickel barrier layer and a solder coating. All these constituent materials have a wide spectrum of thermal expansivity, thermal conductivity and heat capacity. As a result, when a MLC capacitor is subjected to a rapid change in temperature as in a typical surface mount process, thermal stresses are generated within the component. After the component is attached to the substrate, there could be additional stresses created due to thermal expansion mismatch between the component and the substrate during cool down. It has been reported that thermal shock treatments cause micro cracks in the MLC capacitors[1-5]. The cracks frequently occur near the end terminations and extend from one electrode layer to another, providing a shorting path for electrode metal migration. Over a period of time either in use or in storage, the cracked capacitors will slowly degrade and prematurely short. In high reliability applications, specifically where the surface mount assembly is stored for a long time, it is critical that the cracked capacitors be identified and eliminated from the assembled boards.

In the past, several investigators have reported different techniques to identify cracks in discrete capacitors. The more common techniques are visual inspection and monitoring electrical behavior in ambient conditions, and less common techniques are acoustic microscopy[6] and brine solution soak[2]. All these techniques are either unreliable, impractical or destructive methods. A few investigators have reported[2,3] that under high temperature, humidity and bias (THB), the shorting mechanisms in a cracked capacitor are accelerated. Although these past studies have inferred higher failure rates to increased thermal shock treatment, they have not established a direct correlation between THB failure rates to cracks induced by surface mount processes. In this study, we have investigated THB aging technique and showed that it is a reliable method to identify the cracks in a surface mount capacitor. The THB conditions used were 85°C, 85% relative humidity with 50 volts dc bias. In the second part of the study, we have used THB aging technique to compare the effect of vapor phase, infra-red and convection belt solder processes on capacitor cracking and thus its reliability.

EXPERIMENTAL

Test Circuit Board

1. Design

The capacitor test boards were designed and fabricated to simulate circuit boards made for high reliability applications. Twenty capacitors were asymmetrically located on a polyimide/quartz board of size 4" x 4" x .062" as shown in Figure 1. The capacitor used were 1 microfarad, 2225 size, 50v and X7R dielectric type. Since we wanted to measure very small leakage current through the capacitors, the test board was designed with features to minimize the noise contributed by the leakage currents on the board. High and low potential wires were routed with maximum possible separation, and a guard ring surrounding the low potential pad of the capacitor was provided to intercept board leakage currents.

Thermal expansivities of the capacitors and polyimide were measured as a function of temperature[7] and reported in Figure 2.

2. Fabrication

The boards were fabricated at Sandia National Laboratories, Albuquerque, NM and assembled at Allied Signal, Kansas City, MO using the standard manufacturing procedures. Before assembly, all boards and capacitors were visually and electrically inspected and only good parts were used. The boards for Phase I and Phase II were assembled a year apart using the standard production line process being used at the time. For Phase I of the study, the boards were assembled using vapor phase solder process and reflowed twice to simulate an additional rework step. Three assembled boards were treated with several additional cycles of thermal shock by quenching from the reflow zone to a room temperature solvent bath. The purpose of the thermal shock treatment was to obtain cracked capacitors to verify the sensitivity of the THB aging technique. For Phase II of the study, we assembled an equal number of boards by vapor phase, infra-red and convection belt solder processes. All boards in this phase were reflowed three times to simulate two rework cycles. The temperature profiles used for the three solder processes are shown in Figure 3.

Temperature-Humidity-Bias Test Set

A test set was custom designed and built at AT&T Bell Laboratories, Allentown, PA to automatically monitor the leakage currents in batches of 100 capacitors while being aged at 85°C, 85% relative humidity with 50 volts dc bias. The simplified block diagram of the THB test set is shown in Figure 4, and the detailed description of the test set is given in reference 8. The assembled boards were aged in a Blue-M THB Chamber that maintained a given temperature and relative humidity. The boards were connected to an external bias panel using Teflon sockets and cables. The bias panel provided the interface of high voltage to the positive terminals of the capacitors and grounding to the negative terminals. The data acquisition system consisted of a Keithley 707 switching matrix, and a PC. An individual capacitor under 50 volt bias was addressed by the Keithley 707 switching matrix and the data were acquired using a CEC IEEE-488 bus card that interfaced the PC to the Keithley switching matrix. The test set measured the leakage current through all 100 capacitors at programmed interval times. In the automatic mode, the initial measurement was made at a desired delay time. This delay time was programmed to increase by 5% for every subsequent reading. Thus, initially the readings were taken with almost no delay between readings, but as aging time progressed, the delay

time increased, e. g. after 900 hours, the delay time was in days. The test was designed to measure low current values of 10^{-9} amps with 50:1 signal to noise ratio. The leakage current through a "good" capacitor measured about 10^{-9} to 10^{-8} amps, whereas the current through a "short" capacitor was two to three orders of magnitude higher. This allowed us to clearly identify a short capacitor.

Aging Procedure

During the experimental set-up stage, we observed that the as-received bare boards (without capacitors), when THB aged gave high initial leakage currents of 10^{-7} amps due to the presence of water-soluble ionic contaminants on the board surface. After rinsing the boards with DI water for 30 minutes, the leakage current on the bare board as a function of aging time reduced to less than 10^{-9} amps for first 600 hours of aging, and later it steadily increase to 10^{-8} amps after 1500 hours. This board leakage current was sufficiently low to identify a shorted capacitor. Thus before a run, the assembled boards were rinsed in DI water for 30 minutes, and the THB chamber was wiped with alcohol and DI water. Each run was made with a maximum of 5 boards, each with 20 capacitors, at 85°C, 85% relative humidity with 50 volts dc bias for 1000 hours minimum. The capacitance and dissipation factors were measured, and the solder joints visually inspected before and after each run.

The first set of reading was taken as soon as the oven was stabilized at 85°C, 85% relative humidity. The total time taken to measure leakage currents through all 100 capacitors was 1 hour. Thus, all readings, although reported as time = t hour, were actually taken in t to t+1 hours.

Failure Mode Analysis

The capacitors identified as shorts according to the leakage current data obtained during THB aging experiments were sent for destructive physical analysis to investigate the failure mechanisms. Some additional "good" capacitors were also sent as control samples. All capacitors were cross-sectioned with electrical wires attached to the end termination to monitor the leakage current through the capacitor. The capacitors were ground and examined every few mils for defects, while monitoring the leakage current. When a short causing defect like a crack or an internal void was ground away, the capacitor's leakage current would significantly reduce. The nature of this defect was noted, and a best attempt was made to capture this defect on a micrograph for the record.

RESULTS AND DISCUSSION

The study was done in two phases. In Phase I, the THB aging technique to detect cracked capacitors in a surface mount assembly was developed and confirmed. In Phase II, this technique was used to investigate the effect of different solder processes on capacitor cracking.

Phase I - Development of THB Aging Technique

The assembled board identified as 001 is a control sample that was processed in a normal way, whereas the boards identified as 008, 011 and 019 were thermal shocked to obtain cracked capacitors.

1. Visual & Electrical Inspection before THB Aging

We detected only one visual crack (site 10 on board 019) because it is very difficult to visually inspect a capacitor assembled on a board. The measured capacitance and dissipation factor at room temperature were found to be in the range of .97 x 10^{-6} to 1.08 x 10^{-6} farad and .0164 to .0207, respectively. No abnormalities were observed.

2. THB Aging Data

The assembled boards were aged at 85°C, 85% relative humidity with 50 volt bias for 1500 hours. The examples of the outputs of the THB test set, plotted on log-log scale as leakage current versus time, are shown in Figure 5 for board 011. Board 011, which was thermal shocked, had several shorted capacitors. The capacitor on site 12 started short, capacitor at sites 2 and 15 shorted after 10 hours, and capacitor at site 4 shorted after 600 hours. The summary of the data from all four assembled boards is shown in Table 1.

The untreated board 001 did not have any short capacitor, whereas thermal shock treated boards, 008, 011, and 019 had several shorted capacitors. The failure mode analysis shows that capacitors that failed within the first 8 hours of aging had a shorting path through a surface crack. When a crack cut

across two adjacent electrodes, it provides a migration path for electrode ions, which eventually will short the capacitor. The capacitors that failed after 10 hours or more had a large internal void that also provided a shorting path between adjacent electrodes. The internal voids are either actual voids left by a contaminant included during processing of the green ceramics or voids created by localized melting of electrodes during a current surge[9]. In either case, the number of capacitors with such an internal void is an indication of the manufacturing defect level.

TABLE 1
PHASE I - LIST OF FAILED CAPACITORS AFTER THB AGING

Board #	Failed Cap. site #	Time to Failure (hours)	Short-Causing Defect	Reference
No Pretreatment				
001	None	---	---	---
Thermal Shocked				
008	9	0	Surface Crack	Fig. 6a
	13	3	Surface Crack	Fig. 6b
	16	0	Surface Crack	
	17	0	Surface Crack	
	18	0	Surface Crack	
	19	3	Surface Crack	
	8	8	Surface crack	
	5	108	---	
	14	157	---	
	15	413	Internal Void	
	11	517	---	
011	12	0	Surface Crack	Fig.6c
	2	12	---	
	15	12	Internal Void	Fig. 7a
	4	600	Internal Void	Fig. 7b
019	16	0	Surface Crack	
	14	0	Surface Crack	
	10	0	Surface Crack	
	13	10	Internal Void	Fig. 7c

The data confirm that the THB aging technique is a viable method to detect defects, which cannot be reliably detected by visual or dry electrical inspection. If the requirement is to identify capacitors with surface cracks only, then 8 hours of aging is sufficient. This could become a non-destructive technique depending on the damage 8 hours of THB aging does to the capacitors and other components on the assembled board. If the requirement is to identify the MLC manufacturing defects, then at least 1000 hours of aging is recommended. In this case, THB aging technique would be a destructive technique.

The electrodes in MLC capacitors are composed of thick film 70% silver-30% palladium. Both palladium and silver electromigration has long been known as a reliability concern in the electronics industry[10-12]. Palladium electromigration is accountable for low voltage failures only. Under normal voltage conditions, as used in this study, silver from the electrode migrates along the shorting path and forms a dendrite filament extending from the anode to cathode. This mechanism is highly accelerated in the presence of high humidity. Since the electrodes in a MLC capacitor are enclosed in ceramic, the time to failure is dependent on the accessibility of the moisture to the electrodes. In the presence of a surface crack, the shorting path is readily available for moisture to enter and speed-up silver migration. Thus the capacitors, which have a surface crack intersecting adjacent electrodes, will short within the first few hours of THB aging. In the absence of a surface crack, the moisture will penetrate along the electrode-ceramic interface because of its higher porosity. Ultimately after a longer aging time, the moisture will reach a large internal void, if there is any, and speed-up the ion migration, which will ultimately short the electrodes of opposite polarity. The time to failure in this case will depend on the diffusion rate of moisture along electrode-ceramic interface and the location of the void.

Some additional observations made are as follows.

1) After THB aging when the capacitors were dried, none of the short capacitors recovered. This confirms that shorting was caused not by ionic solution but by dendrite filament bridging between electrodes of opposite polarity.

2) A few capacitors during aging tend to short and heal. This cycle of shorting and healing can repeat itself several times. The mechanisms for this phenomenon are not clearly known. Probably the capacitor initially shorts by formation of a filament bridge, followed by high current surges that can burn-out the filament causing the capacitor to heal. It appears that the 10 Mohm current limiting resistors used in the test set circuit did not prevent the current surges. In this regard, a higher resistance value, 50 to 100 Mohm, would have been more appropriate. But by using higher current limiting resistors, the sensitivity of the technique to detect shorted capacitors would proportionately reduce.

Phase II - Effect of Different Solder Processes

In this phase we compared the effect of different solder processes on capacitor cracking. The solder processes we investigated were vapor phase, infra-red and convection belt soldering.

After assembling the boards, a group of samples from each solder process lot was temperature cycled, 100 cycles from -65^{0}C to +125^{0}C with half hour dwell times at each extreme. The solder joints were intact after thermal cycles. Both groups (with and without temperature cycling) were THB aged for 1000 hours minimum, and the short capacitors were identified. The summary of the data is shown in Table 2.

TABLE 2
PHASE II - THB DATA
COMPARISON OF SOLDER PROCESSES
WITH AND WITHOUT TEMP CYCLES

	Temp. Cycled	Without Temp Cycled	Total
Vapor Phase			
# of Caps. Tested	120	180	300
% of Caps. Short	10	10.6	10.3
Infra-red			
# of Caps. Tested	80	160	240
% of Caps. Short	5	5	5
Conv. Belt			
# of Caps. Tested	80	160	240
% of Caps. Short	5	3.75	4.2

For each solder process, there is no significant effect of 100 thermal cycles on the capacitor failure rate. Thermal expansivity of polyimide/quartz board is about 5 ppm/^{0}K higher than that of the capacitor dielectric as shown in Figure 2. The result indicates that thermal expansion mismatch is not large enough to cause fatigue cracking, either in the capacitor or in the solder joint.

There are significant differences in failure rates of vapor phase and of IR or belt solder processes. The failure mode analysis was done on 50% of the failed capacitors and the results were consistent with Phase I results. The capacitors that failed within the first 8 hours had a shorting path in a surface crack, whereas those that failed after longer aging times had a short in the internal void. In Table 3, the percent capacitors that failed in less than 8 hours and those that failed after 8 hours are reported for each solder process group.

TABLE 3
PHASE II - THB DATA
COMPARISON OF SOLDER PROCESSES

Solder Process	% Failed in <8 hrs.	% Failed in >8 hrs.	Total
Vapor Phase	6.3	4	10.3
Infra-Red	1.25	3.75	5
Conv. Belt	1.25	2.9	4..2

Vapor phase solder processes yielded 6.3% cracked capacitors compared to only 1.25% obtained with infra-red and belt processes. Higher failure rates with vapor phase soldered batch can be explained by comparing the temperature profiles of all three solder processes shown in Figure 3. The cool down rate is the least steep in vapor phase soldering, and thus it cannot account for the higher failure rate of vapor phase soldered parts. This also implies that thermal stress due to thermal expansivity mismatch is not a major contributing factor in causing the capacitor failure because capacitor to substrate attachment occurs only at the on-set of cool down. Surface cracks are probably caused by thermal shocks that a capacitor undergoes during the solder process. Vapor phase has the steepest heating rate. Majority of the cracks were seen near the bottom half of the end terminations of the capacitors (refer to Figure 6). During a rapid heating in vapor phase oven, the solder material because of its higher heat capacity will heat up before either the ceramic or the organic board. Thus, the bottom half of end terminations of the capacitors will see higher thermal gradients and more cracking. Although majority of the cracks were seen as described above, a few were seen on the top surface and a few that run through the center of capacitor. Probably these cracks could have been initiated at a weak site caused by a defect already present in the capacitor before the assembly.

For all solder processes, the percent capacitors that failed due to a short in an internal void does not differ significantly . This observation is expected because the capacitors from the same lot were assembled on all boards, thus the manufacturing

defects, like internal voids, will be the same, regardless of the solder process used.

In our study, we have demonstrated the use of the THB aging technique to compare the effect of different surface mount process on the component reliability. Based on the results, the process engineers may take appropriate actions such as altering the temperature profile of the vapor phase process, switching to IR or convection belt soldering, or for a longer term solution developing dielectric and electrode materials that are more tolerant to thermal shocks[4].

CONCLUSIONS

We have developed and demonstrated a THB aging technique to identify capacitors with cracks. In the initial phase of the study we designed and built a temperature-humidity-bias test set to automatically monitor the leakage current through 100 surface mount capacitors while being aged in a chamber at 85^{0}C, 85% relative humidity with 50 volt bias. The results showed that the capacitors with a surface crack intersecting two adjacent electrodes, would short within first 8 hours. The capacitors that failed after longer aging times, 8 to 1000 hours, had short-inducing internal voids. The surface cracks are frequently created during assembly processes, and the internal voids are defects introduced during manufacturing of capacitors.

Since surface cracks in MLC capacitors are frequently developed due to thermal shock from the surface mount processes, in the second phase of the study we have investigated the effect of different solder processes on the capacitor cracking. The surface mount processes used were vapor phase, infra-red and convection belt soldering. The vapor phase soldered board had 6.3% capacitors with surface cracks compared to 1.25% cracked capacitors for IR and belt soldered boards. This study demonstrates that THB aging technique can be effectively used in optimizing surface mount processes and materials.

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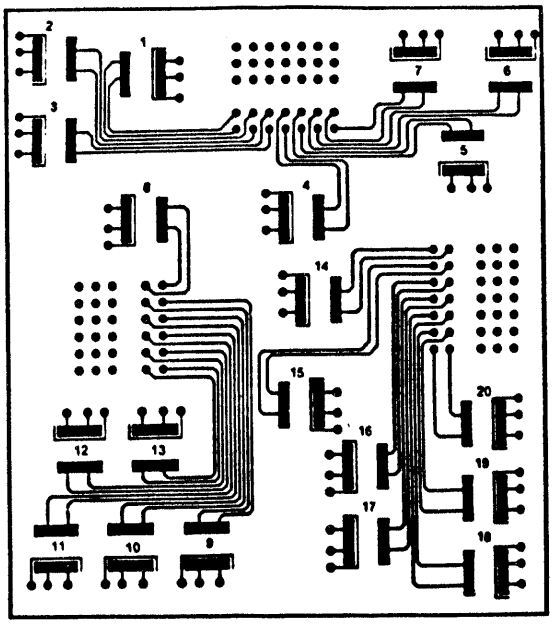


Figure 1 Capacitor pad layout on the test board.

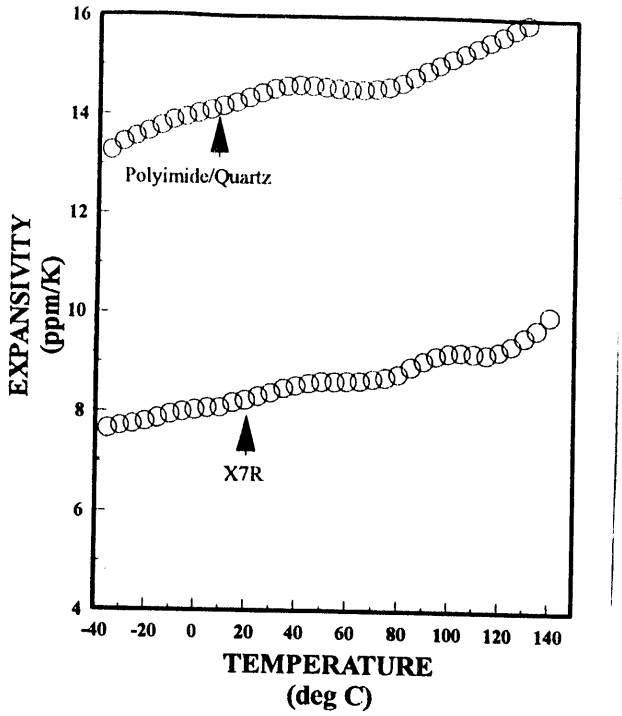


Figure 2 Thermal expansivity of the board and capacitor dielectric.

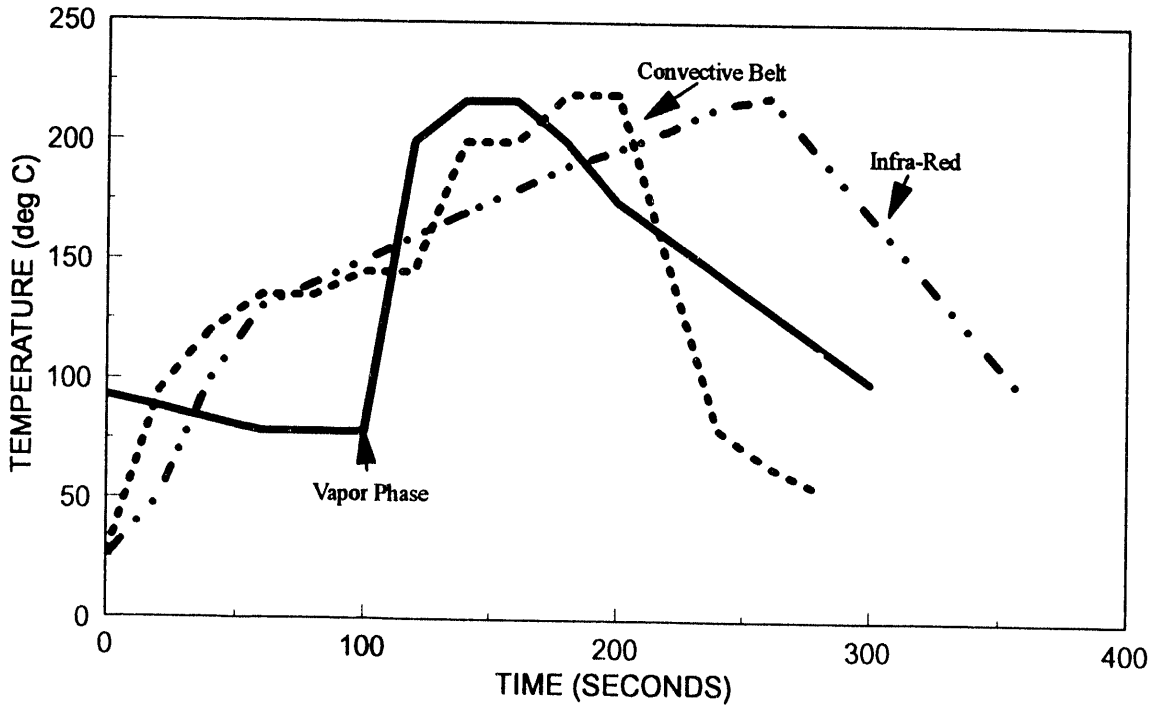


Figure 3 Temperature profiles of different solder processes.

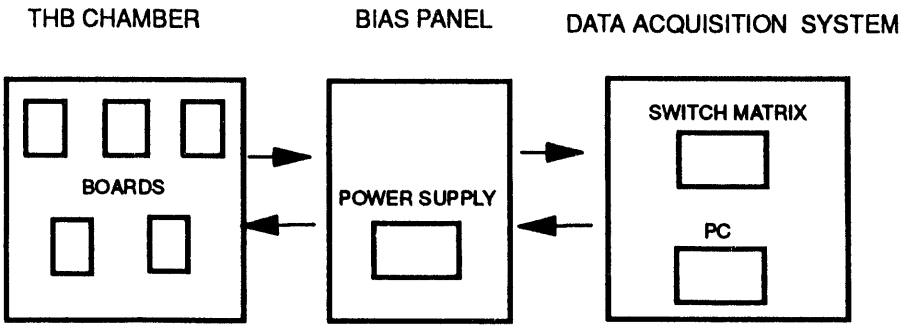


Figure 4 Block diagram of Temperature-Humidity-Bias test set.

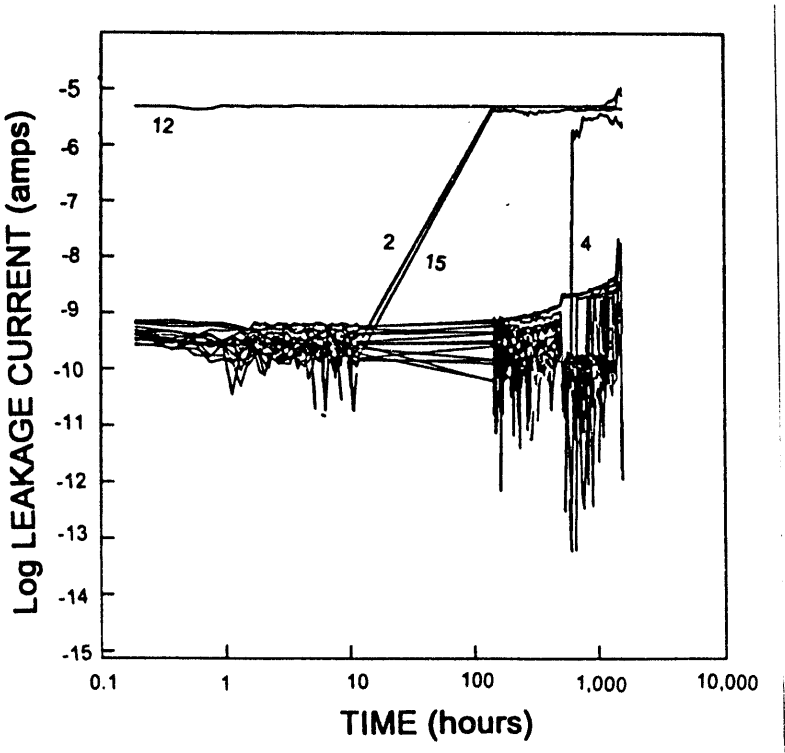
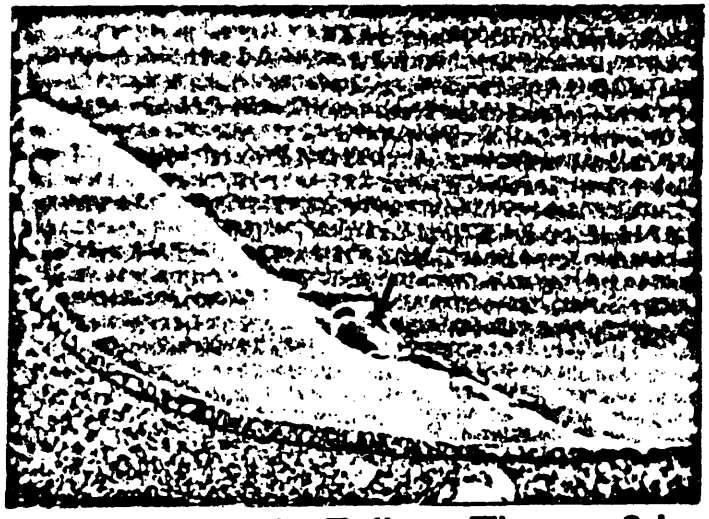
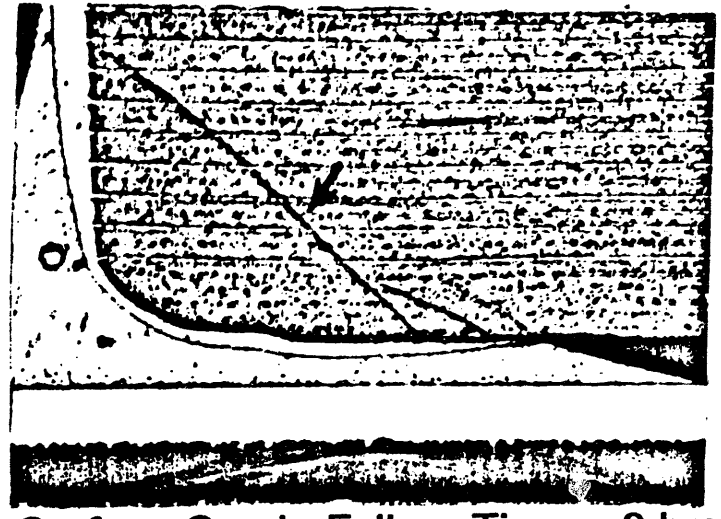


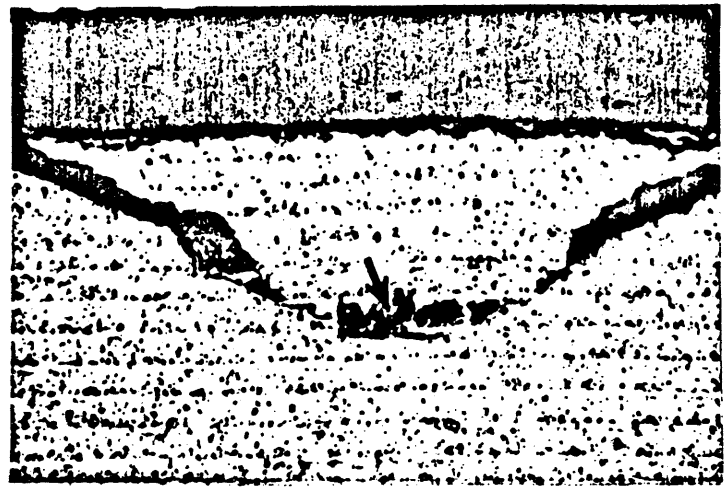
Figure 5 Plot of THB data for board 011.



(a) Surface Crack, Failure Time = 0 hrs.



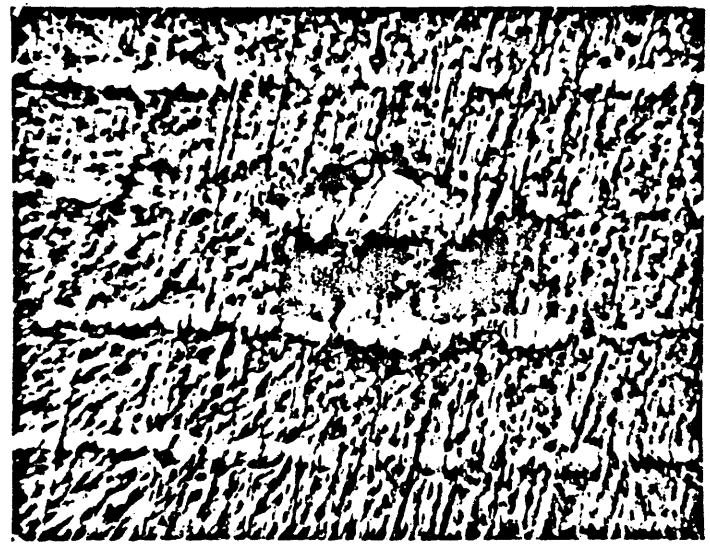
(b) Surface Crack, Failure Time = 3 hrs.



(c) Surface Crack, Failure Time = 0 hrs.

Figure 6 Micrograghs showing surface cracks.

(a) Internal Void, Failure Time = 12 hrs.



(b) Internal Void, Failure Time =600 hrs.

(c) Internal Void, Failure Time =10 hrs.

Figure 7 Micrographs showing internal voids.

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