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Abstract

This paper presents the design and characterization of an 8-channel preamplifier-shaper intended for use with silicon strip detectors ranging in capacitance from 1 to 20pF. The nominal peaking time of the circuit is 200ns with an adjustment range of ±50ns. The circuit has a pitch (width) of 84μm/channel with a power dissipation of 1.2mW/channel and has been fabricated in 2μm p-well CMOS. The 0pF noise is 330e with a noise slope of 64e/pF. The design approach is presented as well as both test bench and strip detector measurements.

I. INTRODUCTION

The original application for this preamplifier-shaper, called the BVX for Bottom Vertex, was for use in the Bottom Collider Detector (BCD) at Fermilab, but the circuit is presently being used for silicon strip detector evaluation for the PHENIX detector at RHIC. The nominal peaking time is 200ns with an adjustment range of at least ±50ns for compatibility with the proposed Tevatron upgrade (400ns interaction rate) and a circuit pitch of 84μm for compatibility with 100μm pitch silicon strip detectors. An 8-channel device was fabricated to study channel uniformity and crosstalk, but the design is easily expanded to 64 or 128 channels as required. The power dissipation is 1.2mW per channel.

One requirement of this circuit was a conversion gain of greater than 50mV/fC. This was to minimize the effect of offset nonlinearities in a subsequent analog memory array. The circuit as fabricated has a conversion gain of approximately 75mV/fC for a 0pF detector capacitance. The shaping is approximately CR-RC^3 which allows a return to baseline within 2 beam crossings (800ns). The chosen topology for the preamplifier is that of the folded cascode with a long NMOS feedback resistor to allow compensation of detector leakage current[1]. Because of the high conversion gain and multi-pole shaping, a topology comprised of two differential amplifiers was chosen. All poles are real and the time response is unipolar without the resultant undershoot often exhibited by filters employing complex poles.

A description of the circuitry will be presented with comparisons between simulated and fabricated circuits. Noise, gain and offset measurements of the actual circuits and description of present use will also be presented.

II. CIRCUIT DESCRIPTION

The preamplifier, shown in Fig. 1, is a folded cascode topology utilizing a long channel NMOS transistor for the feedback resistor[1]. The input transistor is a PMOS device with a width/length (W/L) value of 1080μm/2μm. A common problem with folded cascode designs is the noise generated by second-stage biasing circuits. To reduce this noise, two circuit techniques are employed in this design. The first is the use of a filter capacitor on the gates of the current sources. HSPICE simulations indicate that the presence of M15 improves the noise by approximately 23% for a 10pF detector capacitance. A transistor is used as the capacitor which provides more than a 60% increase in capacitance

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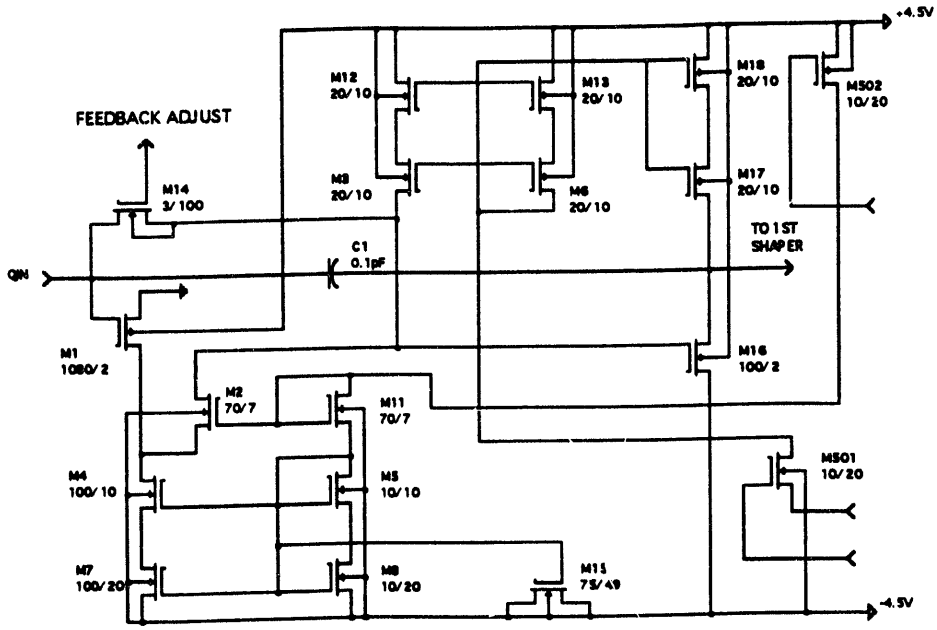

Fig. 1 Preamplifier schematic

compared to a double poly capacitor of the same approximate area. The second technique used to lower the noise is the use of source degenerated current mirrors for biasing. The use of transistors M7 (W/L=100μm/20μm) and M8 (W/L=10μm/20μm) biased in the deep ohmic region as resistors at the sources of the driver M5 (W/L=10μm/10μm) and mirror M4 (W/L=100μm/10μm) improves the noise approximately 5% over sizing M4 and M5 with the same width, but with a length of 30μm. This increase in length would make the overall area of the mirror pair approximately the same as with the degeneration. Source degeneration was also applied to the mirror set of M3 and M6.

The first and second shapers are differential amplifier stages with bandwidth control to implement the shaping. A long channel NMOS transistor is used to adjust the peaking time by setting the location of the pole. The third stage shaper is primarily a gain-filter stage that is also buffered for off-chip drive. The third stage feedback resistors were implemented as strips of p-well.

III. NOISE MEASUREMENTS

The noise measurements, presented in Table I, were made on bare die mounted on a circuit board.

Table I
Noise vs. Input Capacitance

Cin (pF)	Simulated ENC	Measured ENC
0	180	330
1	-	400
5	-	700
10	810	970
20	-	1620

We believe that there are two reasons for the differences between the simulated and measured noise. First, transconductance has been found to be overestimated by the vendors models, particularly since the input device of this preamplifier is operating between weak and strong inversion, a difficult region to model. Second, the series noise in large geometry devices has been found to be higher than predicted by SPICE[2]. The simulation includes the additional bonding pad and input wiring capacitance which is approximately 0.5pF. A photograph of the integrated circuit is shown in Fig. 2.

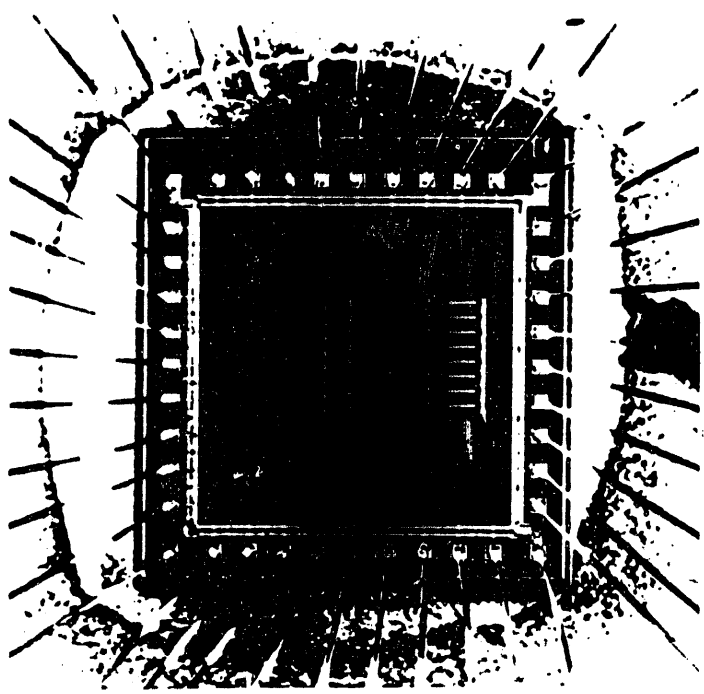

Fig. 2 Die photo of the BVX

IV. ON-CHIP AND CHIP-TO-CHIP PERFORMANCE SUMMARY

A summary of all eight channels on one chip is given in Table II. The measurement parameters are Cin = 10pF, Qin = 5fC. Peaking time is controlled by a voltage on the peaking time adjust input pin which was equal to +2.25V for this test. The mean value of the output offset is 63.6mV and σ (standard deviation) is 51.2mV. The high value of σ is partly due to the layout. The differential input devices of the first and second stage shapers have both small gate areas[3] and, due to tight space requirements, a layout that is not common centroid geometry[4]. Although the magnitude is not surprising, the variation is disappointing since the reason for the differential designs is to allow both the amplifier pedestal and the subsequent analog memory pedestal to be much less than 1fC. Given the high conversion gain, this would allow the electronic pedestal to be virtually ignored. Since the output of the second shaper is not designed for off-chip drive, a 47K resistor from the output to the negative supply was added to enhance drive in the presence of excess capacitance for the following measurements.

Table II
8-channel performance summary (chip#2)

Channel	Peaking time(ns)	Gain (mV/fC)	ENC(e)	Vout DC(mV)
1	240	79.3	900	+43
2	244	79.0	920	+126
3	248	79.8	910	+35
4	244	78.6	900	+109
5	244	77.6	880	+68
6	236	76.4	900	-42
7	240	78.4	910	+114
8	244	81.0	930	+56

The matching between two chips is shown in Table III.

Table III
Chip #1 - chip #2 comparison (Peaking-time adjust = 2.25V, Cin=10pF, channel 6 of chip#1 non-operational)

Chip #	Peaking time(ns)	Gain (mV/fC)	ENC(e)	Vout DC(mV)
1	x=215, σ=4	x=74, σ=0.94	x=947, σ=27.1	x=93, σ=123
2	x=243, σ=3.4	x=78.8, σ=1.3	x=906, σ=14	x=63.6, σ=51.2

The chip-to-chip matching is obviously not as good as the channel-to-channel matching on a given chip. For example, the worst case spread for peaking time varies from 212ns on chip #1 to 248ns on chip #2, a difference of 17%. Within some range, however, the spread may be completely acceptable for a given application. The dynamic range of the amplifier is from 0 to +28fC and 0 to -10fC with a 4% integral linearity error between +5fC and +20fC. The adjacent channel crosstalk is approximately 1%.

V. CURRENT USE OF THE BVX AND PLANS FOR PHENIX

The BVX is presently being used at Los Alamos National Laboratory as a strip preamplifier to test the OPAL FOXFET silicon strip detectors[5]. The detector is a 6cm ac-coupled detector biased with a tunable dynamic resistance. Such detectors are being considered for use in the PHENIX silicon vertex detector. LANL is presently building a laser diode pulser setup for careful characterization of detectors. Quantitative results of this work will be reported at a later date.

The BVX must be modified for PHENIX because of the 112ns beam crossing time of the RHIC collider. A new silicon strip/pad system is being developed by ORNL/LANL/UC Riverside for PHENIX. The front end will consist of (for each channel) a 30ns peaking time preamplifier-shaper-summer, analog memory with approximately 13μs depth, and a 6-bit ADC.

VI. SUMMARY

The results of measurements of the BVX silicon strip preamplifier-shaper have been presented. Noise, gain, and offset measurements have been performed and match well with predictions from simulations. The noise and gain results are as desired, but the variation of the DC offset voltage (σ of approximately 0.6fC) would require pedestal subtraction. For off-chip drive, some enhancement of the output drive capability would be needed.

VII. ACKNOWLEDGMENTS

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