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Status of the Silicon Strip High-Rate FASTBUS Readout System

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Fermilab Experiment E771

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I. INTRODUCTION

Increasingly, experiments at Fermilab are being designed to perform high statistics studies of rare phenomena. These studies are becoming possible at the Tevatron collider as its luminosity is increased and are becoming the main focus of the fixed target program. Fermilab's extracted beams can be made intense enough so that the event rate in fixed target experiments is usually limited by the capabilities of the detector and associated electronics, rather than by the rate of interactions that can be produced. Engineers from the Fermilab Research[1] and Computing Divisions have just finished developing front end and readout electronics for silicon microstrip detectors (SSD's) that operate much faster than anything previously built. SSD's provide very precise position measurements of passing charged particles and allow the measurement of the decay of short lived species such as charm and bottom mesons and baryons.

Our new readout system [1,2] was developed in collaboration with, and largely to the specification of, the E771 experimenters. E771 is a fixed target experiment designed to study the production of B hadrons by an 800 GeV/c proton beam. The experiment will operate at rates of up to 200 million beam protons per second and 10 million interactions per second. The experimental apparatus will consist of an open geometry magnetic spectrometer featuring good muon and electron identification (much of which was used in E705), and a compact 16000 channel Silicon Strip Detector. In order to satisfy the experimenter's desire to instrument 16000 SSD elements in a package only 5 cm wide, 5 cm high, and 21 cm deep, and in order to meet the performance specifications, we have made extensive use of "Application Specific Integrated Circuits" (ASIC's) [3, 4].

Extracted beams at Fermilab retain the 53 MHz RF structure of the Tevatron accelerator. This means that events in the fixed target experiments occur in well defined "buckets" of time that are approximately 1.5 nanoseconds long and occur every 18.9 nanoseconds. Our new SSD readout system operates synchronously with the 53 MHz RF. It has single bucket resolution, which means that all of the SSD information from an event is unambiguously identified with one particular RF bucket. Data and trigger requests are pipelined in such a way that the system can be readout without incurring any front end deadtime. If a high speed data destination is provided, the system is capable of zero deadtime operation at average trigger rates in excess of 1 MHz.

The SSD readout system is also being used for the E771's Resistive Plate Chamber (RPC) and the Proportional Wire Chamber (PWC) systems.

II. SYSTEM DESCRIPTION

A system to collect and process data at high rate, 53MHz, from a silicon microstrip detector has been developed. A parallel, synchronously clocked technique is used to strobe analog signals from the detector into and through the system. The signals are amplified, amplitude discriminated, logically combined and address encoded before transmission to a processor farm. The system is implemented using the FASTBUS standard and modularized at the board level in 128 channel increments. The system has been in development for over two years and includes the following features:

[1] This work was performed under the auspice of the United States Deparment of Energy.

- Zero dead time readout for average trigger rate as high as 1MHz.
- Pipelined triggers and event readout.
- Programmable data delay of up to 4.8usec(Level 1 decision time delay).
- FASTBUS system readout.
- Histogram readout option.
- Multiple high-speed bipolar process ASICS.

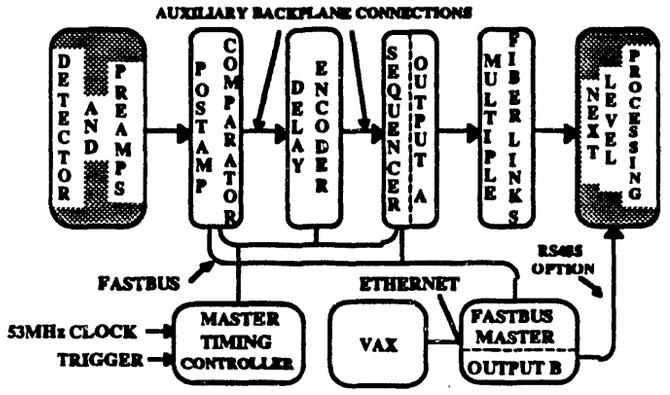

Figure 1: System Data Flow

A general block diagam of data flow for the SSD readout is provided in Figure 1. All the detector signals are received and operated on in parallel. Each FASTBUS crate contains the modules required to condition and encode two silicon strip planes, consisting of 768 channels each. The PostAmp/Comparator module (P/C) and Delay/Encoder (D/E) module handle the detector signals in 128 channel increments. This requires 12 module pairs to implement a 1536 channel crate subsystem. The subsystem crate is shown in Figure 2. Each D/E receives 128 channels of discriminated data at 53MHz from the associated P/C and stores it in memories used as circular buffers. Data is stored for 4.8 μsec pending a trigger signal.

A. SSD Backplane, Control and Timing Signals

The SSD reaadout system was designed to minimize the number of timing signals distributed at the sytem level. To satisfy the timing and data rate requirements a backplane was designed and tested. The backplane implements the FASTBUS protocol and uses the auxiliary section for SSD control and readout, providing connections between P/C, D/E and Sequencer (SEQ). The FASTBUS and auxiliary backplane were designed as an integral unit. The driving requirements and impedance for each signal on the auxiliary section were specified for a fully loaded subsystem crate. Special care was taken when distributing the clocks and control signals because of the implications on system timing and synchronization.

At the subsystem crate level the SEQ connections provide all the data acquisition control. Note that all the signals distributed on the backplane by the SEQ are originated at the Mater Timing Controller (MTC) or derived from MTC signals. The SEQ retimes some of the signals and provides the appropriate timing to operate the subsystem crate.

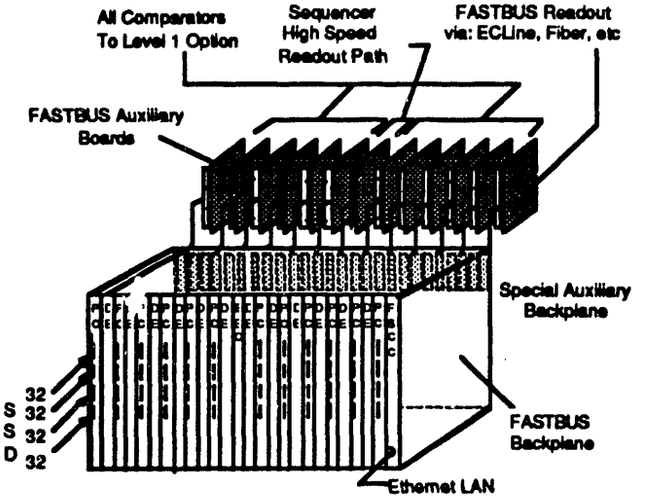

Figure 2: SSD Subsystem Crate

The D/E and P/C are driven with 53MHZ clocks, CLK1 and CLK2, respectively. The phase relation between CLK1 and CLK2 is controlled by the SEQ and is set to establish synchronization between the P/C latching the hits and the D/E writing the hit data to memory. Normally the phase relation between CLK1 and CLK2 is equal for all subsystem crates. The phase relation of CLK1 with respect to the accelerator clock is FASTBUS programmable at the SEQ, allowing each subsytem crate to be tuned to the data processed by the crate. This approach requires that the detector data skew be minimized at the P/C input and the smaller the skew the more efficient the subsystem crate.

To establish system synchronization three signals are used: WRITE ENABLE, SYNC and RESET. RESET is used to bring the system to a

known state. The WRITE ENABLE is used to enable the D/Es to write data into memory and the SYNC signal initiates the write process. The SYNC is a periodic signal that is used for system wide synchronization checks.

For event readout the backplane implements an ADDRESS BUS and ADDRESS VALID signal connecting to all D/Es. For data transfer, independent DATA busses (byte wide) and DATA VALID signals are used between each D/E and the SEQ. Data transfers are synchronous to CLK3 (26.5MHz, driven by the SEQ) and D/Es driving data assert the corresponding DATA VALID signal with the data.

The P/C-D/E connection consist of 128 point-to-point connections between two adjacent slots. For the subsystem crate twelve of these connections are provided.

B. System Control and Readout

The SSD readout integration into an overall system is simplified by the implementation of the MTC. At the system level the MTC controls the D/E, the P/C and the SEQ. The MTC generates system clocks, controls system synchronization and generates delay memory addresses upon the receipt of triggers from the experiment's trigger system. The MTC recieves the 53MHz Tevatron RF clock and distributes it to each SEQ and eventually to all D/Es and P/Cs. The previously mentioned SYNC signal is generated by the MTC every 256 cycles and distributed to all subsystem crates D/Es to perform system wide synchronization tests. Each D/E checks the SYNC pulse against it's internal reference and in case of disparity it asserts a sync error signal. This signal is provided at the sytem level to the MTC. In this way all subsystem crates controlled by an MTC are checked for synchronization to the same source. The event acquisition by D/Es is initiated by the SYNC pulse when the WRITE ENABLE signal is asserted.

The MTC generates a read or "hit" address when a trigger is received. The hit address generated is offset from the current write address based upon a calibration of the trigger decision time. A write address counter is implemented in the MTC to keep track of the write counter at the D/Es. Hit addresses are placed into a high speed FIFO capable of queuing up to eigth trigger requests that can be accepted on succesive RF buckets. The read addresses from the FIFO are broadcast to all D/Es at a rate determined by ENCODER READY signals summed from all D/Es. At the time that the address is being output the MTC determines D/E memory overwrite errors; however to prevent such a condition the system can be throttled using the WAIT signal which the MTC sends to the trigger system when the trigger FIFO fills past a programmable depth.

The trigger addresses received by the SEQ are broadcast to the D/Es which respond by reading, encoding and transmitting the encoded event to the SEQ synchronous to CLK3. The SEQ stores the event fragments from each D/E in separate FIFOs and supports queueing of events. The flow of trigger addresses from the MTC to the SEQ is controlled by the SEQ, which negates the ENCODER READY signal when a readout from the D/Es is taking place. A logical OR of the ENCODER READY of all subsystem crates is sent to the MTC. In addition when the queues on the SEQ exceed a limit the SEQ READY signal to the MTC is negated to stop the flow of triggers.

For the initial implementation the events are readout by the FASTBUS Smart Crate Controller (FSCC) through FASTBUS. Each crate subsystem FSCC in the system transmits the hit address data out the FASTBUS auxiliary port to a processing farm or storage system. This is implemented with a single readout bus and access to the bus is controlled by a token passing mechanism. The FSSCs can also use independent links to the processing farm or storage system for higher throughput. An alternate readout path is provided by the SEQ which implements an auxiliary port similar to the FSCC. The SEQ output is intended to be used to feed a fiber optical link. In the fiberoptic link case, each crate transmits data to an independent receiving buffer at 40MBytes/sec.

III. HARDWARE TESTS

All the modules used for the SSD readout where tested individually to satisfy single board test requirements. Test modules where designed to assist in the debugging process. In particular, a D/E Test Stand Module (TSM) was developed which can generate data patterns at 53MHz. In addition, a board driven by the TSM was designed, the Level Shifter Module (LSM), to test the analog section of the P/C. The LSM converts the signals from the TSM to differential signals with amplitudes in the operating range of the P/C.

Another test module for the SEQ was designed to test simultaneously each of the 12 D/Es data channels.

To test the functionality of the readout system a subsystem crate as shown in Figure 2 was used. The test setup uses an additional crate containing the MTC and an FSCC. For this test the system readout diagnostic capability designed into the P/C is used. This was provided by including digital pattern injection logic at the analog/digital internal interface of the module. This logic is implemented using a FASTBUS setable counter that injects static or dynamically changing patterns into the digital section of the P/C. In this test one FSCC is used to generate and force triggers through the MTC using FASTBUS. The subsystem crate FSCC is used to read and check the encoded event. To synchronize the processes running on each FSCC, communication was establised using the front panel port of the module. This test is used to check a set of 12 P/C, 12 D/E and a SEQ before the set is delivered to the experiment. A set of boards for the subsystem crate was defined as working if the test ran for two million events.

IV. SOFTWARE DEVELOPMENT

A. Test and Diagnostics

The software development was based on the following environment, which is supported by the Fermilab Computing Division Online Support Department:

-Low Level Monitor and Debugger : pROBE
-Multitasking Kernel : pSOS
-Cross Compiler System (C,680x0 Assembler)
-FASTBUS Standard Routines
-Interface Drivers for RS232 and ETHERNET

The Software was developed on VAX/VMS using the native source code management tools. The software can be divided up into three main packages, which share low level functions:

A) Single Board Test
B) System Test
C) Readout and Control

The first two packages were developed in collaboration with the hardware developers, the Online Support Department and the experimenters [6,7]. This effort allowed the experiment to gain valuable experience with the SSD system before installation in the experiment. The software is menu driven and allows the setting of most of the parameters for diagnostic purposes.

The Single Board Test tests the D/E, P/C, SEQ and MTC. Low level functions were grouped into packages for each of the boards including test boards and reused in B and C. There are two modes in all tests, a default test which only gives a FAIL or PASS and a user test with user settable parameters and extensive error reporting for diagnostics. Only the D/E can be tested fully using the TSM with this package. This test includes the generation of random hit patterns and user selected patterns. The other boards receive their final test using the System Test.

The System Test package not only includes the full test of the readout chain and control logic starting from the P/C and ending at the FSCC, but also the test of the analog part of the P/C using the TSM and LSM pair. This test allows the determination of hot channels, dead channels and cross talk. The test software is able, by varying delay and threshold, to trace the shape of an input signal. The hardware and software is flexible enough to fully test two other front end boards which replace the P/C in the Restistive Plate Chamber and Proportional Wire Chamber detector systems.

B. Readout and Control for E771

The Readout and Control program used in the experimnet was designed to control three detector systems consisting of up to 25 FASTBUS crates, which are read out in one chain via RS485. To accomplish this the software support for the FSCC was extended as follows:

- Download of software to the FSCC via ETHERNET
- Basic ETHERNET driver
- Reliable Datagram Communications
- Remote Procedure Execution via ETHERNET

The software for a single FSCC is loaded from the VAX via ETHERNET in less than 5 sec compared to 15 minutes over RS232. Using Remote Procedure Execution, the program on the VAX calls subroutines which are executed on the FSCC. The software on the VAX is

written in VAXC. The part which resides in the FSCC is written in C and Assembler. The readout code is totally written in Assembler and it is interrupt driven. It interfaces with the high level software via function calls and communication blocks, that give the current status of the FASTBUS crate including trigger numbers, FASTBUS module CSR0 contents, error numbers etc...

The readout code can be configured in different ways, which allows filling of histograms and/or an event ring buffer. The minimum readout time for a typical event is 60 usec. With histogramming and buffer filling this time is around 200 usec. By removing all overhead it was measured to be 15 usec. With the online histogramming in real time one or two spills are sufficient to check the basic performance of the detector.

The higher level software uses the FASTBUS standard routines to access modules in the crates. All procedures are implemented on the FSCCs, which are necessary to run the above described Hardware System Test on the VAX, using Remote Procedure Execution, without modifications.

The software for the SSD, RPC and PWC detector systems is identical. It is controlled by configuration and parameter files, which define the crate and readout configurations and keep the parameter values. Delay and noise rate curves can be generated under program control. Histograms, event buffers and status information is sent to the controlling VAX during data taking on request.

V. SSD Readout Hardware for E771

SSD amplifiers and prototype P/C's were used during the 1990 fixed target run to debug the prototypes and to examine the performance of the system. The modules were found to be oscillation free and the system was shown to have a stable operating point above the background noise. Figure 3 shows a beam profile taken by the silicon microstrip. Figure 4 shows top and side views of the silicon microstrip data used for track reconstruction.

During the current fixed target run, the electronics developed for the E771 SSD readout are being used on all the new detector systems that were installed since the last run of the E771 experiment predecessor, E 705. In addition to approximately 10,000 channels for the Silicon Strip Detector, 3000 channels of similar electronics for the RPC and 8000 channels for the PWC are being installed. The last two systems replace the P/C with modules designed for these systems. The PWC use an ASIC amplifier [5] that is a modified version of the SSD amplifier designed for use in E665 [8].

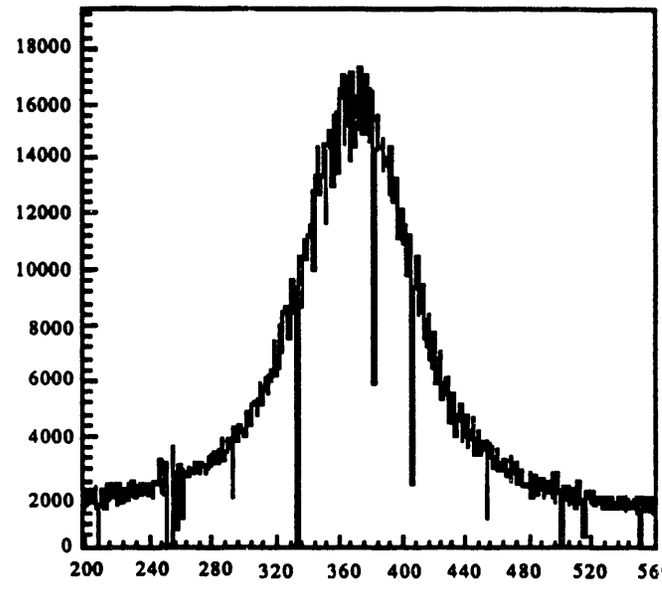

Figure 3: Beam Profile Taken with one Silicon Plane

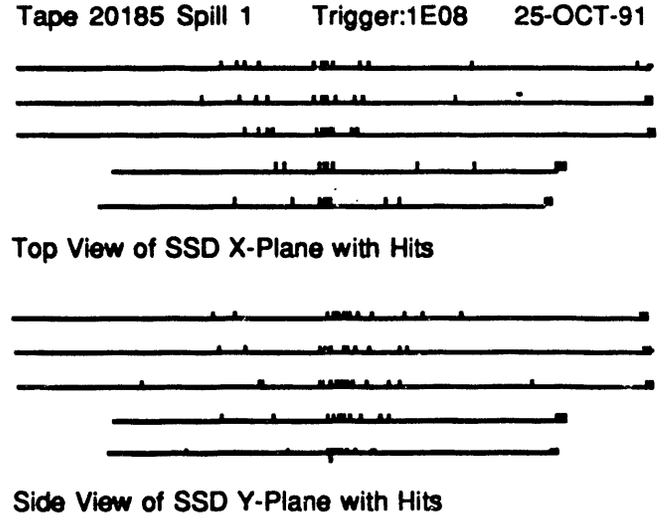

Figure 4: Views of X and Y SSD Planes

VI. Acknowledgements

A project of this size is never designed, fabricated, tested, and installed by one person. At least 25 man-years of effort has been expended by people from the Computing

Division, Research Division, and the E771 collaboration, in particular Duke University, University of Virginia and University of Athens. Each individual contributed to the completion of the development phase and the initial experimental installation. This project would have been impossible without the the excellent cooperation and support of all the people and organizations involved.

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[8] This work specified and completed in collaboration with John Oliver at Harvard University.

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