# Novel Failure Analysis Techniques Using
# Photon Probing With a Scanning Optical Microscope

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*Abstract*: Three new failure analysis techniques for integrated circuits (ICs) have been developed using localized photon probing with a scanning optical microscope (SOM). The first two are light-induced voltage alteration (LIVA) imaging techniques that (1) localize open-circuited and damaged junctions and (2) image transistor logic states. The third technique uses the SOM to control logic states optically from the IC backside. LIVA images are produced by monitoring the voltage fluctuations of a constant current power supply as a laser beam is scanned over the IC. High selectivity for localizing defects has been demonstrated using the LIVA approach. Logic state mapping results, similar to previous work using biased optical beam induced current (OBIC) and laser probing approaches [1,2], have also been produced using LIVA. Application of the two LIVA based techniques to backside failure analysis has been demonstrated using an infrared laser source. Optical logic state control is based upon earlier work examining transistor response to photon injection [3,4]. The physics of each method and their applications for failure analysis are described.

## INTRODUCTION

It is critical to develop new failure analysis techniques to keep pace with the continued development of increasingly complex ICs. Ideally, these new, improved analysis techniques should be easier to use, less damaging, more sensitive, and provide better spatial resolution. This challenge is being met with advanced techniques, including those that can be broadly categorized as either "passive" or "active". Passive techniques are noninvasive, in the sense that the normal operation of the IC provides the information or energy being measured. Examples include voltage contrast [5], light emission analysis [6], quiescent power supply current ($I_{DDQ}$) testing [7], fluorescent microthermal imaging [8], and magnetic force microscopy/current contrast imaging [9]. Active techniques use the response of the IC to special stimulus, such as electron, photon, or ion beams. Examples include electron beam induced current (EBIC) [5], optical beam induced current [10,11], and biased

resistive contrast imaging [12]. (A thorough review of failure analysis techniques is provided in [13].)

An ideal failure analysis technique would not only be simple, fast, and benign but would also use existing or readily available equipment and software. The scanning electron microscope (SEM) is a necessary part of every failure analysis laboratory, commonly used for high resolution images with a large depth of field. The SEM has become a powerful failure analysis tool because of the electron beam's ability to interact with an IC and precisely localize the effects of this interaction. Numerous SEM techniques that take advantage of electron beam effects on powered ICs have been developed, from voltage contrast for identifying electrical bias conditions to charge-induced voltage alteration (CIVA) for localizing open conductors [14].

Another instrument becoming more common in failure analysis laboratories is the SOM. The SOM's confocal mode provides improved image resolution and depth of focus compared to conventional optical microscopy. Like the SEM, the SOM can be a very useful analysis tool because of the laser beam's interaction with the IC. The effects of light on the electrical properties of active ICs have been well documented. The SOM enables localization of photocurrents to produce OBIC images that show junction regions and transistor logic states [10]. In addition to OBIC, photocurrent effects on $I_{DDQ}$ [2], transistor switching speed [15], and latch-up initiation [1] have been well described. The major advantages of SOM-based methods compared to SEM analysis techniques are the ease of IC electrical connection, no requirement for a vacuum system, and the absence of ionizing radiation effects.

We have applied localized photon probing with the SOM to develop three new, active failure analysis techniques for nondestructive IC analysis and failure site localization. Each of these techniques takes advantage of photon-induced interactions on electrically biased ICs.

Two techniques are based on light-induced voltage alteration (LIVA). Open circuits involving junctions can be imaged using LIVA with selectivity and signal strength large enough to examine the entire die in one image. LIVA can also be used for logic state mapping with results similar to

biased OBIC images, but with greatly improved signal to noise ratio and a much more flexible test system. In addition to "normal" front side examination, LIVA has been successfully applied to backside failure analysis of flip-chip packaged ICs and multilevel metal ICs in conventional packages using an infrared laser.

Optical control of logic states is based upon earlier experiments that examined the response of individual transistors to photon injection [3,4]. Optical logic state control permits control of the binary state of a sequential circuit element at power-up, at reset, or during operation at reduced $V_{DD}$, thus reducing the circuit stimulus requirements. We have expanded on the previous work by using an infrared laser source, permitting IC backside logic state control.

The optical beam interactions with the IC that generate the LIVA images are described in detail. The data acquisition system and protocols for image collection are also described. Examples of photon probing techniques applied to CMOS ICs demonstrate their utility as failure analysis tools.

## LIVA IMAGING TECHNIQUES

LIVA is analogous to CIVA, EBIC, and OBIC in that the biased IC is the detector. LIVA images are produced by monitoring the voltage change of a constant current source used to bias the IC as a focused laser beam is scanned across the sample.

*LIVA System*

A block diagram of the LIVA system is shown in Fig. 1. The SOM is a Zeiss Laser Scan Microscope. In our system,

four lasers were available: (1) the internal 633 nm, 5 mW HeNe laser; (2) an external 1152 nm, 5 mW HeNe laser; (3) an external 1320 nm, 320 mW Nd:YAG (neodymium doped yttrium aluminum garnet) laser; and (4) an external 1064 nm, 1.2 W Nd:YAG laser. Both YAG lasers were made by CVI Laser Corporation. Three filters could be introduced into the beam path to attenuate the beam intensity to 10%, 1%, or 0.1% of the incident intensity. A pair of galvanometer-driven mirrors move the laser spot across the field of view in a 512 x 512 pixel raster. The beam can be scanned in a single line or placed onto a single spot. The minimum spot size is diffraction limited. A photomultiplier (PMT) detector is used for the 633 nm laser and a germanium diode detector is used for the infrared lasers.

Electrical stimulus for the IC is provided by a Keithley 236 source measurement unit. This supply is used initially as a constant voltage supply at an appropriate voltage (typically within the IC's rated $V_{DD}$ range) to determine that the IC is powered-up properly and to measure the current needed for LIVA analysis. The supply is then switched to the constant current mode for LIVA analysis. Electrical stimulus for the inputs is selected using a simple switch box or can be provided through a computer-controlled matrix or digital tester.

With constant power supply current supplied to the IC, $V_{DD}$ varies as the laser beam scans across the IC active circuit region. The variation of $V_{DD}$ is amplified by an Ithaco 1201 voltage amplifier operating in the ac coupled mode. The amplifier gain and bandpass filters (both high and low pass) are adjusted to optimize the specific LIVA image. The output of the amplifier is connected directly into the SOM's OBIC port.
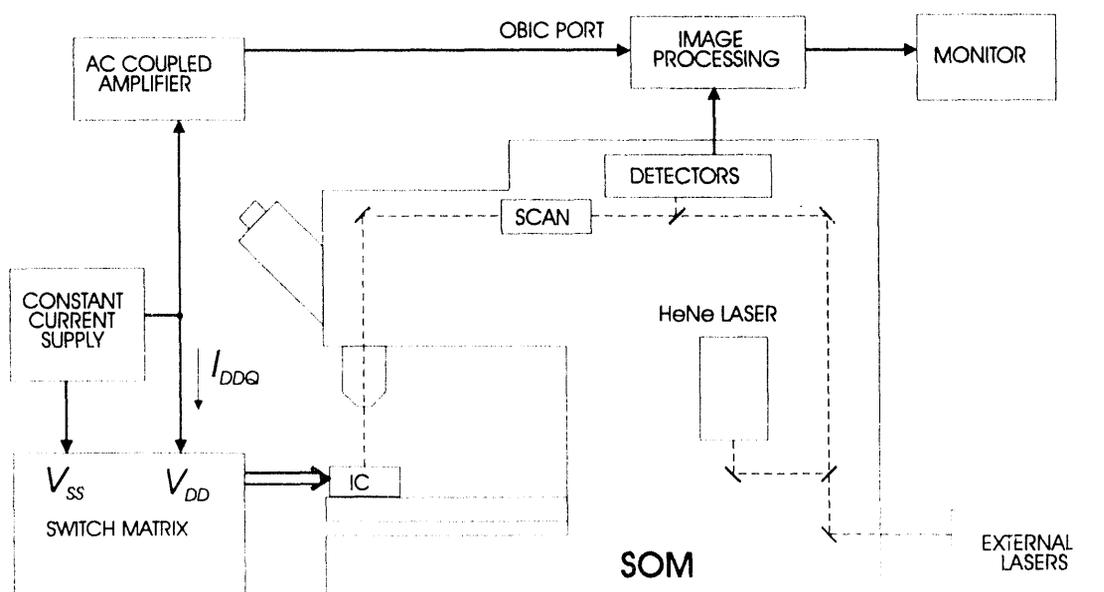


Fig. 1. LIVA system.

LIVA, like OBIC, takes advantage of photon generated electron-hole pairs to yield information about IC defects and functionality. When electron-hole pairs are generated near the interface between differently doped regions in an unbiased IC, the charge carriers are separated by the built-in potential between areas with different Fermi levels. Biasing an IC can increase or decrease the Fermi level difference between regions, thereby altering the magnitude of electron-hole pair separation. LIVA images are produced by monitoring the voltage changes of the constant current power supply as the optical beam from the SOM is scanned across an IC. Voltage changes occur when the electron-hole pair recombination current increases or decreases the power demands of the IC.

The LIVA measurement and imaging of voltage shifts has two advantages beyond directly observing the photocurrents or $I_{DDQ}$. First, the IC will act as its own current-to-voltage amplifier, producing a much larger LIVA voltage signal than photocurrent signal. This is in part due to the difference in "scale" for IC voltage and current. Figs. 2 and 3 illustrate this difference in "scale". Fig. 2 shows the *I-V* characteristics of a CMOS IC made with a *p*-well technology. The curves in Fig. 2 were generated by sweeping $V_{DD}$ from 10 to 0 V while the IC was biased in the static burn-in configuration. Individual transistor channels were illuminated by operating the SOM in spot mode and positioning the 633 nm laser in the middle of the polysilicon gate. The intensity of the 5 mW laser was reduced to 10% using one the neutral density filters. As expected, there is an increase in IC current when transistors are exposed to illumination.

Note that the increase in $I_{DDQ}$ with illumination is greater for "off" transistors than for "on" transistors. When a transistor is "off", there is a greater voltage between its source and drain that when the transistor is "on". This change in potential produces a difference in recombination current and in $I_{DDQ}$. (This $I_{DDQ}$ difference is used to identify logic states with photon exposure [2].)

Fig. 2 also shows that the $I_{DDQ}$ difference between the "off" and "on" states is greater for *p*-channel transistors than for *n*-channel transistors. This effect is explained by considering the recombination current for *p*-wells in *n*-substrates. Electron-hole pairs produced in the *n*-channel transistors will have recombination current across the *p*-well to *n*-substrate junction as well as source to drain current. The *p*-well to *n*-substrate current is independent of the IC logic state. Therefore illuminating the *n*-channel transistors in different logic states has a smaller relative effect than illuminating the *p*-channel transistors in different logic states.

Fig. 3 is a *V-I* curve produced by sweeping the supply current from 250 to 0 nA. Fig. 3 data were generated by configuring and illuminating transistors in the same manner as in Fig. 2. While the curves in Figs. 2 and 3 have similar shape, the change in "scale" can be observed by examining the differences at a given bias point. For example, in Fig. 2 at 5 V the "off" *p*-channel transistor had a photocurrent increase of 80 nA (from 90 to 170 nA) when exposed to the SOM beam.

The same transistor when supplied with 90 nA of current had a voltage decrease of 2.4 V (from 5 to 2.6 V) when exposed to the SOM beam. This large difference in signal, 2.4 V versus 80 nA, illustrates how the IC acts as its own current to voltage amplifier during LIVA analysis. Amplification would be required to make use of the 80 nA signal for imaging.
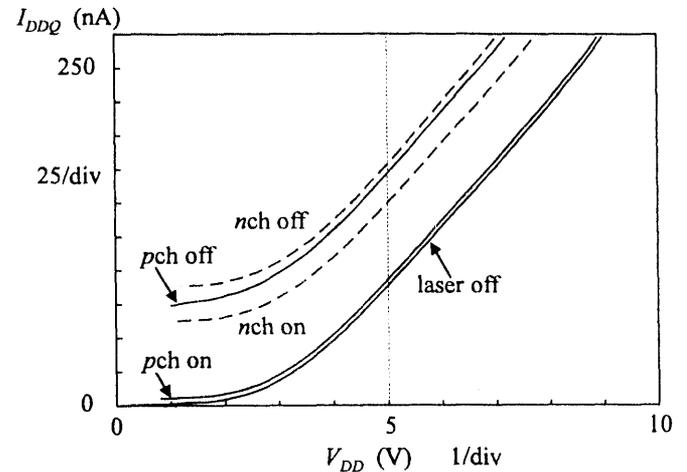


Fig. 2. *I-V* curves of an IC with laser illumination of individual transistors (a curve with no laser illumination is included). *p*-channel and *n*-channel transistors were illuminated in both the "off" and "on" logic state.
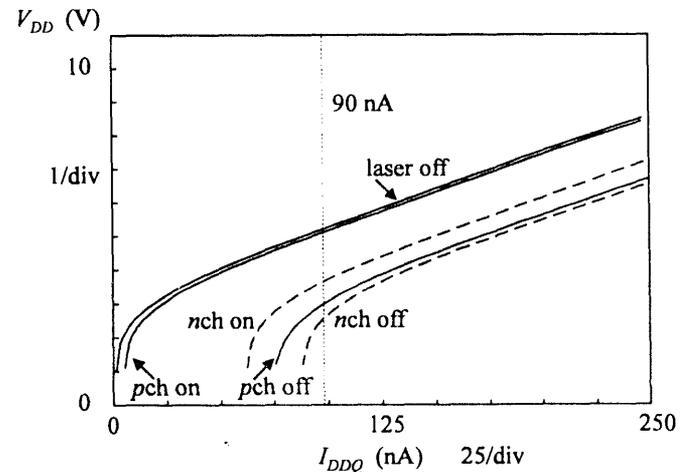


Fig. 3. Similar to Fig. 2, except $V_{DD}$ is measured as $I_{DDQ}$ is swept from 250 to 0 nA.

The second advantage of the LIVA approach versus direct photocurrent observation is that IC voltages are simpler to use than IC currents. While this may not appear to be too great an advantage at first, there are several important ramifications. Direct photocurrent measurement is done in series. Most current amplification systems will have maximum current capability (typically 250 µA) that restricts the operational range without modifications. There is also the added complication of sometimes needing to measure a relatively small photocurrent against a large dc background current. Voltage measurements, on the other hand, are made in

parallel, with none of the power limitations of current measurement. Small changes in voltage are easily measured using an ac coupled amplifier much less affected by background dc voltages.

The simpler equipment setup and relatively large signal make LIVA more attractive than conventional photocurrent methods.

*LIVA Signals From IC Defects*

The LIVA signal generation described in the previous section considers photon interactions on nondefective ICs. Under identical illumination conditions, localized defects on ICs can generate LIVA signals 3 to 4 orders of magnitude greater than other LIVA signals from nondefective ICs. This difference in LIVA signal depends upon the defect type, but two basic mechanisms are responsible for the increase. First, the defect, because of its location in the IC amplifies the effects of normal photocurrents by altering the power demand of circuit elements connected to the defect region. Second, the defect region itself is a site of enhanced recombination compared to nondefective areas. Two types of defects illustrating the differences between these mechanisms are described below.
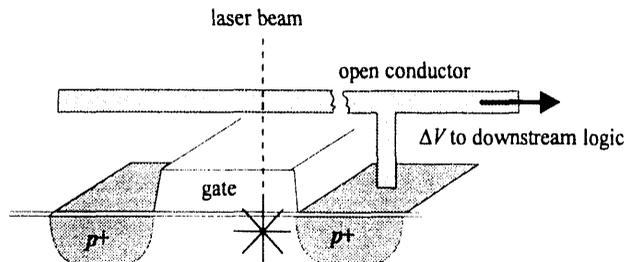


Fig. 4. Outline diagram showing how localized photon injection can affect open-circuited junctions and downstream logic.

For example, junctions connected to open conductors amplify normal photocurrent effects to produce a larger LIVA signal (Fig. 4). Photon injection and subsequent electron-hole pair production will initially produce a normal LIVA signal at the defective junction. The recombination current generated will reduce the voltage across the junction. Normally the transistor supplying the potential difference across the junction will quickly attempt to compensate for the recombination current and try to reestablish the initial bias conditions. If the interconnection path that supplies this "compensation charge" is open, then no compensation occurs and potential difference across the junction continues to decrease with photon injection. This can put the transistor directly associated with the open-circuited junction into saturation, increasing the IC's power demands. For constant current conditions, this results in a greater $V_{DD}$ decrease and a larger LIVA signal. Note also that the voltage of the open-circuited conductor connected to the junction will be the same as the voltage of the $p^+$ diffusion. Therefore any other transistors connected to the open conductor may also go into saturation, further amplifying

the LIVA signal. When photon injection ceases, the junction voltage will slowly recover to its initial equilibrium voltage which is determined by weak coupling of the open conductor to neighboring conductors, transistor bias, and parasitic leakage conditions [14].

If the open conductor has a significant amount of quantum mechanical tunneling (typical of stress voided open conductors), the recovery to initial conditions will be much faster (on the order of milliseconds) [14]. However, large LIVA signals can still be generated because the electron-hole pair recombination current at the junction can be greater than the tunneling current.

Of course, if the IC logic state is such that there is no potential difference across the open-circuited junction, there will be no LIVA signal.

Electrostatic discharge (ESD) damage of an input protection diode is an example of a defect that can cause a direct increase in recombination current. The changes in local Fermi levels caused by dopant redistribution and newly formed charge leakage paths will normally produce elevated $I_{DDQ}$ with no illumination. Electron-hole pair generation and recombination due to illumination in the area of the defect will produce even greater amounts of "leakage current". When the supply current is held constant, the result will be a decrease in supply voltage and therefore an increased LIVA signal.

In both of the cases described above, the large increase in LIVA signals from defects facilitates rapid localization of the defective regions while scanning the entire IC die.

*LIVA Signal Acquisition Using the AC Coupled Mode*

One final note about LIVA acquisition concerns the use of the ac coupled amplification system. As alluded to previously, one advantage of using ac coupled amplification is the mitigation of any dc offset signals that can complicate data acquisition. Another advantage is the use of an "over-supply" approach which increases the effective bandwidth of the LIVA system for strong LIVA signals. Increased system bandwidth permits faster image acquisition without a loss in spatial resolution.

The "over-supply" method involves increasing the supply current of the constant current source well above the maximum current needed to maintain the compliance voltage of the power supply. The compliance voltage (5 V for the examples in this paper) prevents damage to the IC from overvoltage. If the constant current supply had infinite bandwidth, no LIVA signal would be produced under "over-supply" conditions. Because the current source does have bandwidth (response time) limitations, there will be a momentary reduction in supply voltage as the current source attempts to "keep up" with power demands. The LIVA signal can be produced by amplifying the momentary voltage reductions with the resultant system bandwidth being determined by the constant current source. We have used this "over-supply" LIVA approach for CIVA, enabling image acquisition of an entire IC die while the electron beam is scanned at TV rates.

*Examples of LIVA Imaging*

The LIVA imaging approach described above can be used in two basic modes: defect localization and logic state determination. Examples of each are given below.

*Localization of Open-Circuited Junctions:* Fig. 5 is a LIVA image of a passivated CMOS ASIC. It is the same type of IC used to produce the curves in Figs. 2 and 3. The 633 nm, 5 mW HeNe laser was used to acquire the LIVA images. The two small areas highlighted by arrows show the increased signal from two open-circuited junctions on the IC. The open-circuited junctions resulted from metallization stress voiding. The absence of any other signal in Fig. 5 demonstrates the selectivity of LIVA for localizing defects. Fig. 6 is a combination of the LIVA image (white) and a reflected light image showing the same field of view as Fig. 5. Fig. 7 is a combined LIVA and reflected light image showing the two defects at increased magnification.

To confirm that the junctions seen in the LIVA image were indeed connected to open conductors, CIVA analysis was performed on the same IC. Fig. 8 is a combined CIVA and secondary electron image with about the same field of view as Fig. 7. Fig. 8 clearly shows the junctions are directly associated with the open conductors shown in Fig. 7.

*Logic State Mapping Using LIVA:* Fig. 9a is a LIVA image illustrating how the logic states of transistors can be identified. This image was acquired using the 633 nm HeNe laser used in Figs. 5-7. The IC is a CMOS microprocessor. The dark and bright areas indicate decreases and increases in the supply voltage, respectively. Bright contrast regions are produced as the SOM beam is masked from an "off" transistor by an opaque metal conductor, producing a return of the supply voltage to the nonilluminated condition. Note that the image is very similar in appearance to logic mapping with biased OBIC [1], but with the larger signal and ease of acquisition advantages of LIVA.

Fig. 9b displays a LIVA difference image made from two images of the microprocessor in two different logic states. The field of view is the same as Fig. 9a. The difference image was produced by a simple subtraction of two LIVA images, with the resultant image showing only those transistors that changed logic state. The metal interconnect between rows of logic cells does not produce a LIVA signal. The interconnect can be seen in Fig. 9c, a reflected light image at the same field of view as Figs. 9a and 9b.

*Backside LIVA Imaging Using IR Illumination*

The LIVA defect localization and logic state detection demonstrated in the previous sections work well assuming photons can reach the junctions of interest. However, LIVA is not possible if an optically opaque layer is present that prevents photon transmission. Flip-chip packaged IC's and IC's with multilevel metal interconnection would be very difficult or impossible to examine with LIVA using a visible light source. The use of infrared (IR) illumination for LIVA from a polished IC backside circumvents these problems. Backside examination of IC's has been well established in the

advantage of silicon's transparency to photons with energies less than the indirect silicon bandgap energy. Fig. 10 displays the percent transmission of photons through 625 $\mu$m of (a) $p^-$ silicon and (b) $p^+$ silicon as a function of wavelength [16]. The wavelengths corresponding to the indirect bandgap energy in silicon as well as the wavelengths of several lasers are indicated in Fig. 10. Generation of LIVA signals from backside IR illumination is somewhat more difficult than reflected light IR microscopy, because the photon wavelength must be long enough to penetrate through the silicon substrate but short enough (have enough energy) to produce electron-hole pairs in the junction regions.
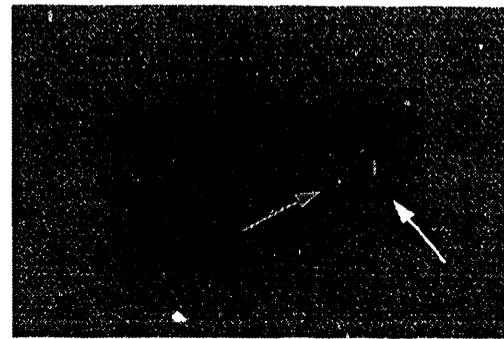


Fig. 5. LIVA image of an entire die taken with a 633 nm, 5 mW HeNe laser. The LIVA signals from open-circuited junctions are highlighted by arrows.
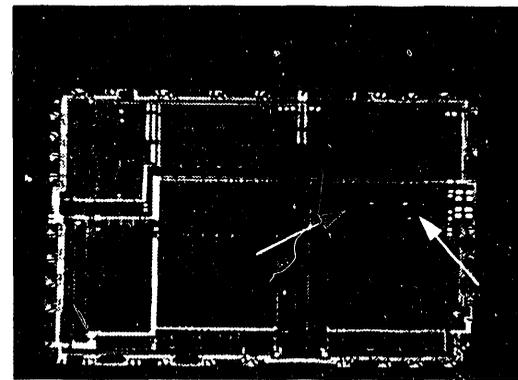


Fig. 6. Combined LIVA and reflected light image showing the field of view in Fig. 5.
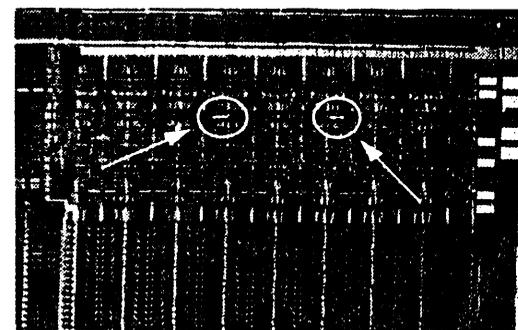


Combined LIVA and reflected light image showing the field of view in Fig. 5 at higher magnification.
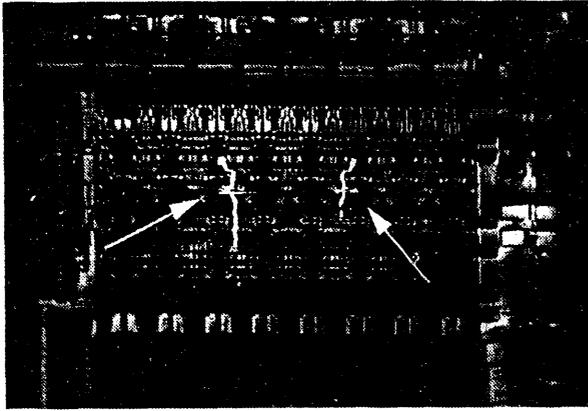
Fig. 8.   Combined CIVA and secondary electron image at
about the same field of view as Fig. 7 confirming that
the LIVA signal is associated with open conductors.

*Backside IR Localization of Defects:* Initial backside LIVA
experiments were performed with the 1152 nm, 5 mW, HeNe
laser. Fig. 11a is a polished backside LIVA image of a 64K
CMOS SRAM fabricated with a 2 micron, 2 level metal
technology. The LIVA signal indicated by the arrow results
from a floating input. The LIVA signal is much weaker than
those shown in Fig. 5, as evidenced by the 60 Hz noise in Fig
11a. The photon energy of the 1152 nm laser is just below the
indirect silicon bandgap energy, but close enough for some
electron-hole pair production (due to the energy level
distribution). Fig. 11b is a reflected IR micrograph of the
same field of view as Fig. 11a. The large depth of field of the
low magnification objective used in Fig. 11b generates an
image that has both the die frontside and backside in focus.
This prevents IC frontside structures from being observed at
low magnification. Figs. 12a and 12b are higher
magnification IR LIVA and reflected IR images of the open
SRAM input.

A stronger backside IR LIVA signal was produced from an
SRAM input with ESD damage. Figs. 13a and 13b are IR
LIVA and reflected IR images of an input with ESD damage.
The LIVA signal is generated at the $V_{DD}$ input protection
diode.

A radiation-hardened version of the Intel 80C51 fabricated
at Sandia was also examined using IR LIVA. The
microcontroller was made with a 1.25 micron, 2 level metal, 2
level polysilicon technology. Earlier failure analysis using
CIVA had identified open metal-1 to silicon contacts resulting
from a pellicle scratch [17]. The contacts were completely
obscured from surface optical examination by a metal-2 power
bus.

The microcontroller was packaged in a 40 pin ceramic dual
in-line package (DIP). To gain access to the die backside, the
package was delidded and extensions (approximately 3") to
the DIP's I/O pins were mounted on the top of the package.
The entire assembly was then potted in Epon 815 epoxy. This
was required to hold the die in place as the backside is
polished. Epon epoxy was chosen because of its low curing
temperature (27 °C) and negligible expansion. The
backside of the ceramic package was then polished

die back was exposed. Fig. 14 shows the package after
polishing.
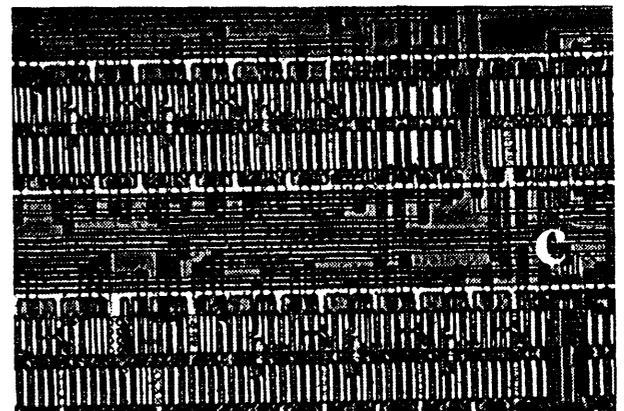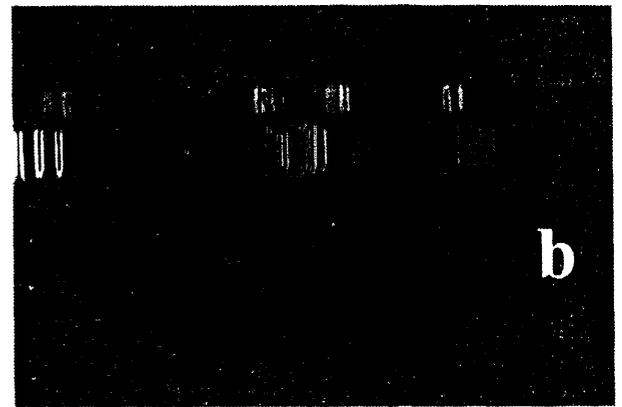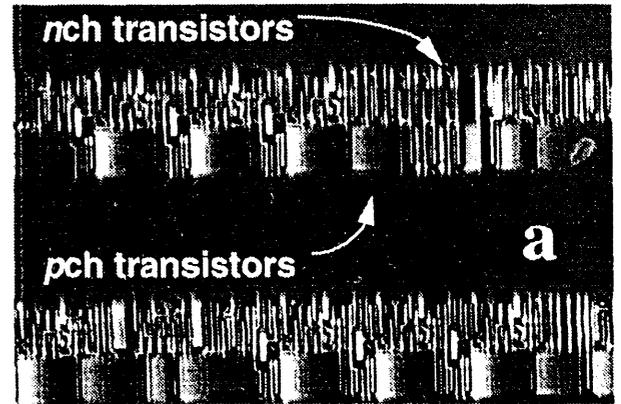






Fig. 9.   Three images showing (a) a LIVA logic map of cell
rows, (b) a LIVA difference image between two
different states, and (c) a reflected light image for
registration. The wavelength was 5 mW HeNe laser at
1152 nm for photocurrent images.
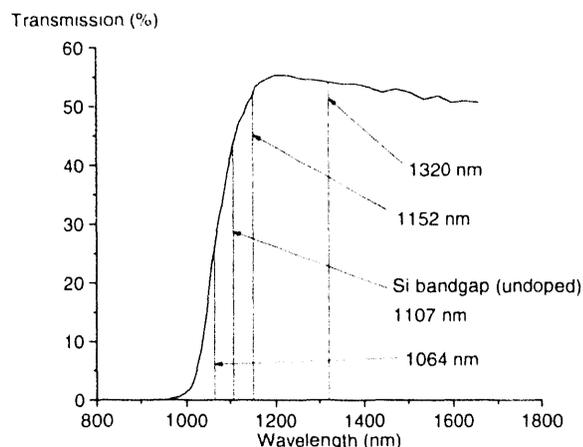
(a)
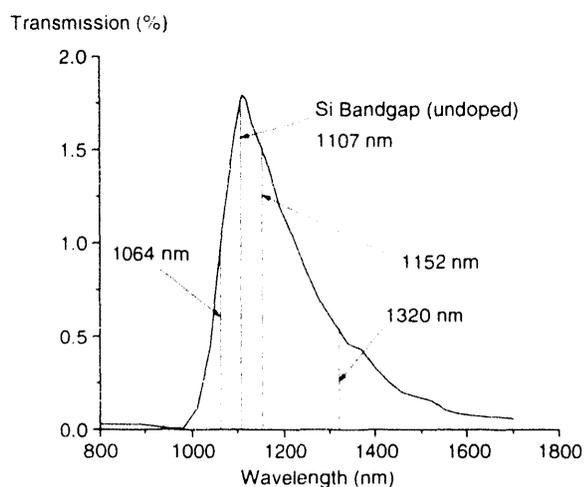


(b)

Fig. 10. Percent transmission of light through 625 μm of (a) $p^-$ and (b) $p^+$ silicon. The wavelengths corresponding to the indirect bandgap energy of silicon as well as several lasers are indicated.

Fig. 15a is a backside IR LIVA image of the entire microcontroller. The small LIVA signal indicated by the arrow is produced by the open metal-1 to silicon contact region. Fig. 15b is a reflected IR image showing the same field of view as 15a. Figs. 16a and 16b are backside IR LIVA and reflected IR images of the same defect site at higher magnification. The wide metal-2 bus obscuring front side observation of the contacts can be seen in Fig. 16b. Biased OBIC using $10^{10}$ gain and backside light emission were both attempted at the failure site identified with LIVA in Fig. 16. No anomalies were detected using either technique.

*Backside IR Logic State Mapping:* Even with the signal gain possible with LIVA imaging, logic states could not be observed with the 1152 nm, 5 mW HeNe laser. The wavelengths of the two additional lasers used to attempt backside IR logic state mapping with LIVA are indicated in Fig. 10. Both are relatively inexpensive water-cooled

Nd:YAG lasers. The 1320 nm, 320 mW laser was used first. Very high contrast reflected IR images were produced with the laser, but the photon energy was too low to produce electron-hole pairs. The defects observed earlier at 1152 nm were not visible in LIVA images using the 1320 nm laser.
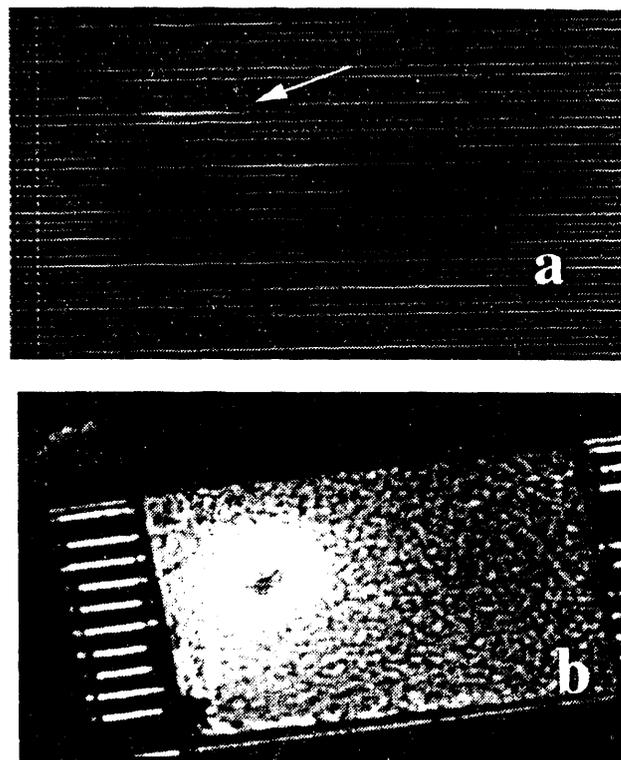


Fig. 11. (a) Backside IR LIVA and (b) reflected IR images of a SRAM with an open input. The 1152 nm, 5 mW, HeNe laser was used for these images.

As shown in Fig. 10, the 1064 nm laser intensity is attenuated significantly more than the other two IR lasers, but this wavelength was recently shown to be successful in backside OBIC imaging of thinned, heavily doped silicon [16]. It was hoped that the added power of the 1.2 W laser would compensate for the increase in silicon absorption.

Fig. 17 demonstrates that the 1064 nm, 1.2 W laser was indeed successful in producing backside IR logic state maps using LIVA. In fact, the signal strength was sufficient to view logic states with the laser power reduced by a factor of 10 with a neutral density filter. Fig. 17a shows an I/O structure from the microcontroller in a logical "1" state. The "off" transistors produce the dark contrast in Fig. 17a. Note that no bright signals from metal obscure the LIVA signal from the transistor junctions as in surface LIVA imaging. Fig. 17b is a LIVA difference image showing the transistors that change state when the output of the I/O structure goes from a logical "1" to a logical "0". Fig. 17c is a reflected IR image showing the same field of view as Figs. 17a and 17b. The one transistor highlighted by the arrow is described in the IR Optical Logic State Comparison section that follows.

A second example of backside IR logic mapping using the 1064 nm, 1.2 W laser is shown. Fig. 18a is a LIVA image showing
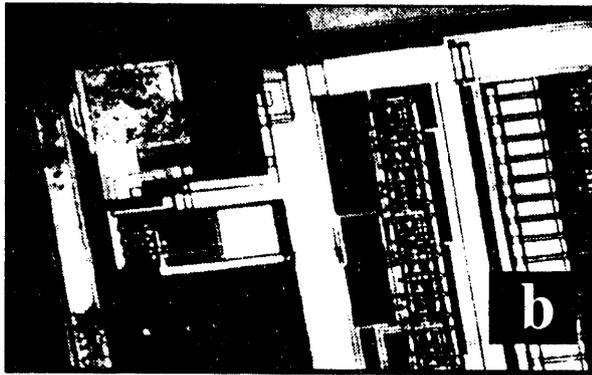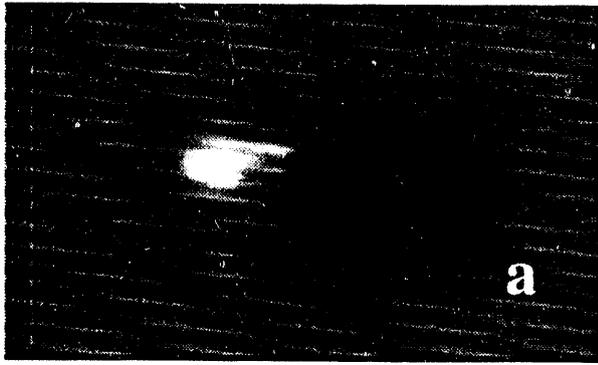
Fig. 12. Same as Fig. 11 but at higher magnification.





Fig. 14. Exposed die backside in an epoxy encapsulated DIP. The lead extensions enable LIVA analysis.
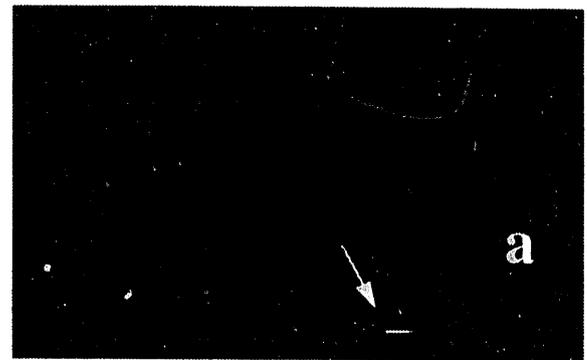
Fig. 15. (a) Backside IR LIVA and (b) reflected IR images of a microcontroller with open contacts. The 1152 nm, 5 mW HeNe laser was used for these images.

a portion of the SRAM on the microcontroller. No filters were used to attenuate the laser intensity. Each CMOS memory cell is composed of 6 transistors (4 transistors in the cross-coupled inverters and 2 n-channel access transistors). The dark areas are p-channel transistors in the "off" state. From this map one can easily determine the logic state of the SRAM memory cell. Fig. 18b is a reflected IR image for registration.

IR OPTICAL LOGIC STATE CONTROL

Fig. 13. (a) Backside IR LIVA and (b) reflected IR image of a SRAM with ESD damage in an input device. The 1152 nm, 5 mW HeNe laser was used to acquire the image.

been observed by several researchers [3,4]. Of course, if the transistor is internally driven by a transistor that can override the photon-induced preferred state, the logic state will be determined by that transistor. Optical logic state control can still be performed, but the choice of which transistors to illuminate becomes more complicated. Our success with backside IR LIVA indicated that we should be able to extend frontside logic state control using visible illumination into a tool for backside selection of logic states using IR illumination.
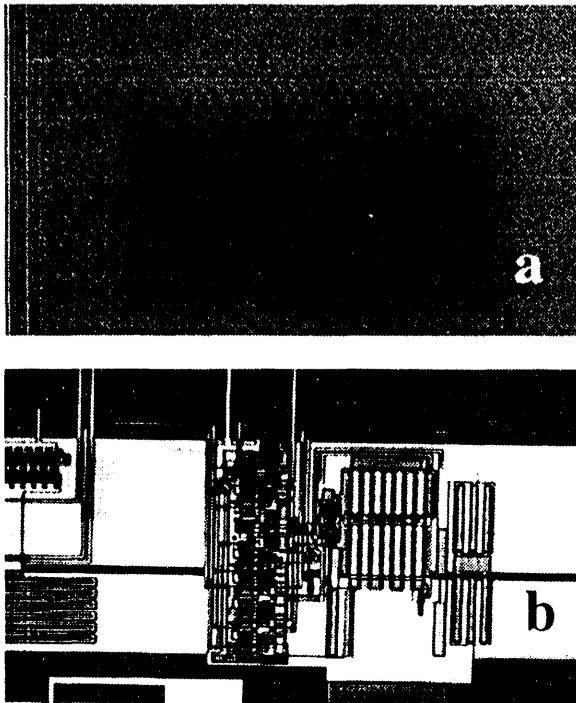


Fig. 16. Same as Fig. 15 but at higher magnification.

As a demonstration vehicle, optical logic state control using IR illumination was applied to the microcontroller SRAM shown in Fig. 18. A higher magnification image showing a portion of an SRAM cell is shown in Fig. 19. The memory cell's two *p*-channel transistor gates are highlighted in Fig. 19. Precise control of areas to be illuminated in the SOM is achieved by operating the SOM in spot mode and positioning the laser spot to the desired location. By illuminating only one *p*-channel transistor gate region in a SRAM cell, that transistor could repeatedly be turned "on" at IC power-up, effectively setting that particular SRAM bit in the microcontroller.

A second example of backside IR optical logic state control is demonstrated in Fig. 17. The arrow in Fig. 17c indicates the location of a *p*-channel transistor in a half latch circuit that holds the logic state of the I/O pin when tristated. By illuminating the active gate region of this transistor during power-up, the I/O structure was forced to a logical "1" state. Absence of illumination during the power-up state produced either a logical "1" or "0", with a preference for the "0" state.

Clearly these two examples indicate that optical logic state control can be used during backside analysis of IC
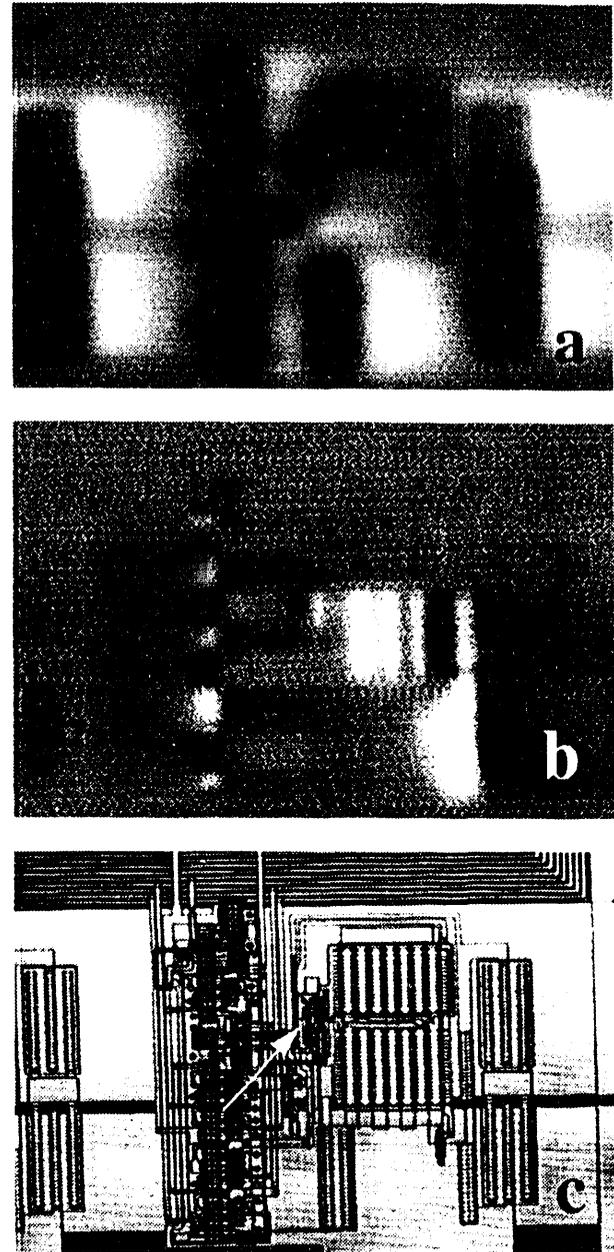


Fig. 17. Three backside IR images showing (a) a LIVA logic map of a microcontroller I/O structure at a logical "1", (b) a LIVA difference image between a "1" and "0" state, and (c) a reflected light image for registration. The 1064 nm, Nd:YAG laser attenuated to 120 mW was used for all three images. The arrow indicates the *p*-channel transistor used for IR optical logic state control as described in the text.

CONCLUSIONS

The three photon probing failure analysis methods described in this paper provide nondestructive enhanced IC evaluation and failure localization capabilities for both frontside and backside IC examination. All three techniques are easily implemented with existing SOM equipment. They are complimentary additions to the art of IC analysis tools.
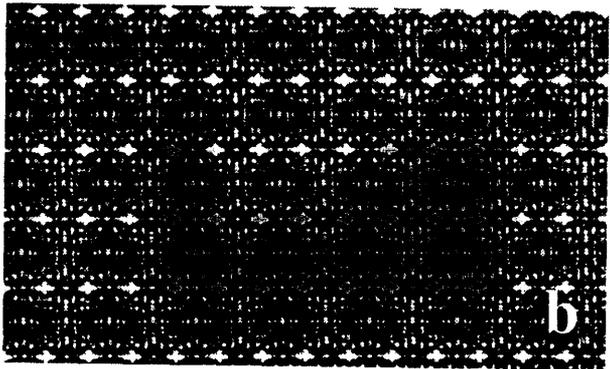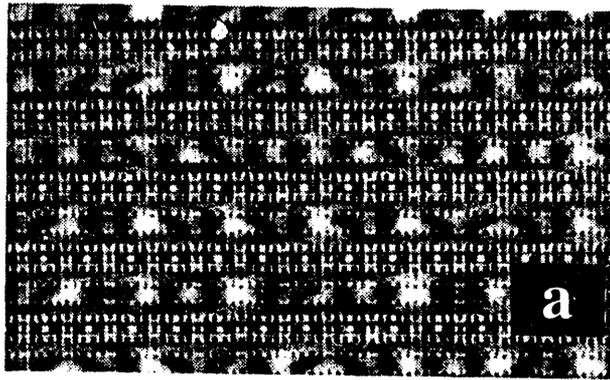
Fig. 18. (a) Backside IR LIVA and (b) reflected IR images of an SRAM in a microcontroller. The 1064 nm, 1.2 W laser was used to acquire the images.
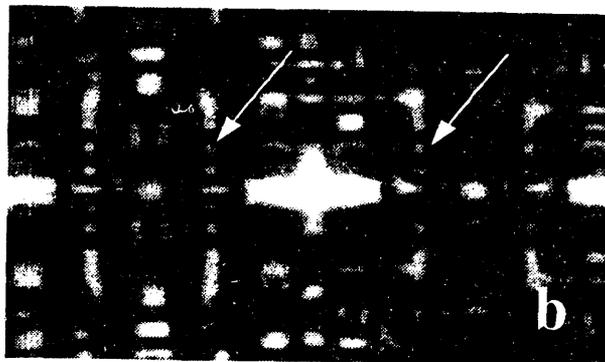


Fig. 19. (a) IR LIVA and (b) reflected IR images displaying a portion of an SRAM cell with the *p*-channel transistor gates highlighted. These gates are illuminated during power-up to control the logic state of the memory cell.

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