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HI-SPEED VERSATILE SERIAL CRATE CONTROLLER FOR CAMAC*

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ABSTRACT

A serial crate controller, primarily for use in the SLC CAMAC control system, has been designed, and has been in use for about 2 years. The design supports a party line approach, with up to 16 crates on a single twisted pair for data transfers, plus another pair for prompt *L* response. The bit rate is 5 megabits/*s*, and complete transaction times of about 10 μs are achieved for 16-bit data transfers over cables up to 1000 feet long. One of the primary objects of the design was simplicity – there are approximately 60 chips in the two-board unit.

1. INTRODUCTION

A serial crate controller (SCC) has been developed for use in the SLC control system, and has been in use for some time now. Due to its versatility it has also been used in several smaller CAMAC automation systems at SLAC. The basic idea of this design was to develop a high speed party-line system simpler to implement and support than the standard CAMAC serial system.

The ground rules of the design were as follows: 1) use of "standard" RS-422A drivers and receivers in a baseband system; 2) common party line approach for reliability and optimum response; 3) self-clocking line signals with unique leading synchronization avoiding the use of phase locked loops; 4)~ 10 μs overall data transfer time for 16 bit data; 5) single master line control, all crate controllers are slaves; 6) versatility to handle all CAMAC operations; 7) minimum capability to handle asynchronous *L* signals; 8) response after every command (system handshake); 9) no parity, for simplicity of application in limited distance, known environments. These principles are summarized in Table 1.

This paper discusses only the crate controller itself, and does not deal with other elements of the SLC control system, or other devices that support this SCC.

2. TYPICAL APPLICATIONS

A photograph of the unit is shown in Fig. 1, and a diagram of the typical SLC application is shown in Fig. 2. The party line twisted pair in each "sector" is normally Belden 9730 terminated at both ends in its characteristic impedance of 100 Ω. The total length of this line is about 500 feet but the maximum distance useable signals actually travel is one-half of that (250 feet). All bi-directional data transfers run 5 megabits/*s* and utilise this single twisted pair. Another pair is used for prompt *L* response, although *L* signals can be polled within the normal data handling structure as well.

Although some errors do occur in the overall SLC control system, the origin is as yet unknown, and measured error rates are not available. Overall error performance is well within the tolerable range. In another application at SLAC, the SCC is used in an experimental beam line magnet control system, with a total line length of about 1000 feet, running at 5 megabits/*s*. In this case, Belden 9851 with an impedance of 200 Ω is used, terminated at both ends.

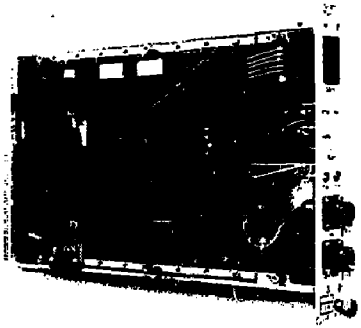

Figure 1. Photograph of the Unit.

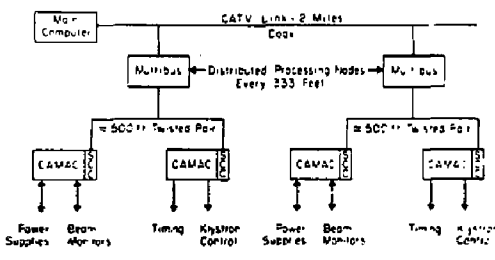

Figure 2. Typical Application at SLC.

3. LINE PROTOCOL

As in any serial system, the key to understanding lies in the logical system structure, or line protocol, shown in Fig. 3. Note in particular that each message is preceded by a unique double width sync pulse which initialises all units and assures that they interpret the 3 line control bits properly on every transaction, avoiding troublesome sync search procedures. An interesting feature of this simple line control protocol is the capability of single address block transfers for read, write, and control, achieving an increased transfer rate due to the lower overhead.

Another method to increase throughput is to optimize 16-bit read and write transfers, which are quite common in the SLC control system, thus saving the line overhead of 6 unused bits. At 5 megabits/*s* the transaction time is about 10 μs for a 16-bit transfer.

On every response *Q*, *X* and *L* status are returned to the driver, thereby giving a polled *L* capability. A second twisted

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pair, if desired, is used for a prompt *L* response where necessary. Once the crate is identified, all 23 *L*'s in the affected crate are read by a single special command. (See the next Section).

A response after every command (except write) gives continuous confirmation of system operation.

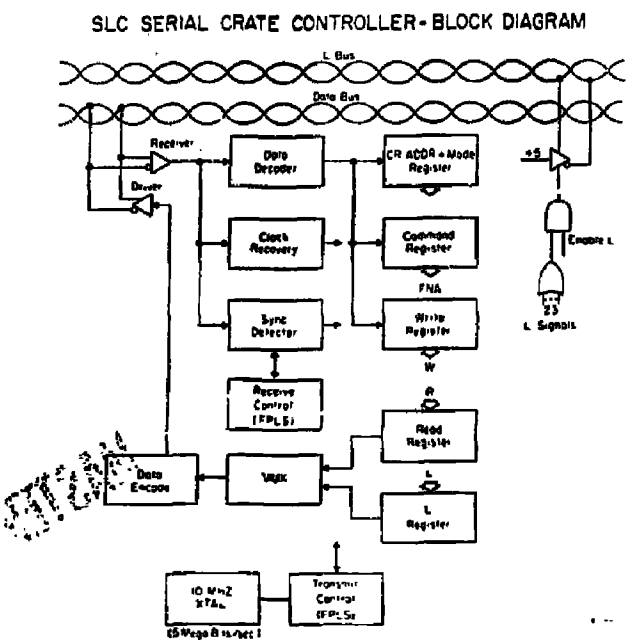

Figure 3. Line Protocol

4. SPECIAL COMMANDS

A set of special commands perform operations directed to the addressed SCC. These are shown in Table 2 and are designed to be compatible with the type *A* and *L* – 1 crate controllers for uniformity.

5. DESCRIPTION OF THE SCC

Design of the SCC to implement this protocol is quite straightforward. A block diagram is shown in Fig. 4. The essential data handling elements are shift registers which convert from serial to parallel and vice versa. During reception the clock is derived from the data stream, during transmission the internal 10 MHz crystal clock is used. All special commands are decoded in an 82S100 FPLA for versatility. The key elements in the control sections are two 82S105 FPLS which direct actions depending on the bit count state contained in a common 64 bit counter. This same philosophy is employed to generate the CAMAC cycle using the Receive FPLS, instead of using discrete logic.

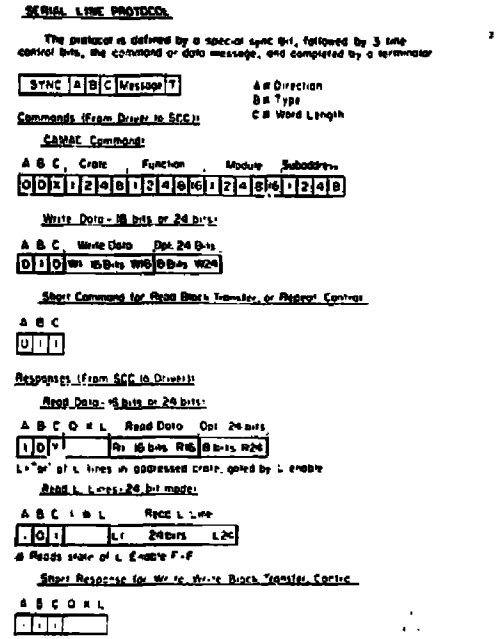

Figure 4. Serial Crate Controller-Block Diagram.

6. LINE SIGNALS

Differential line signals are used. A typical encoded data stream is illustrated in Fig. 5. Note that a transition occurs at each 200 *ns* bit boundary for clock recovery in the decoder. A transition in the center denotes a "one". This type of encoding is efficient in terms of line bandwidth for a self-clocked system. The sync pulse, not shown, is a double width 400 *ns* positive pulse preceding the message.

At the end of the line, signals are distorted by line dispersion, and a "jitter" is introduced at the zero, or slicing level, where an ideal receiver circuit switches. This jitter is primarily what limits line length.

Some manufacturers specify line related jitter. For example, a cable such as Belden 9730 has a typical length versus bit rate for a given percentage jitter, usually 5% as shown in Fig. 5. The system described in this paper tolerates considerably more than 5%.

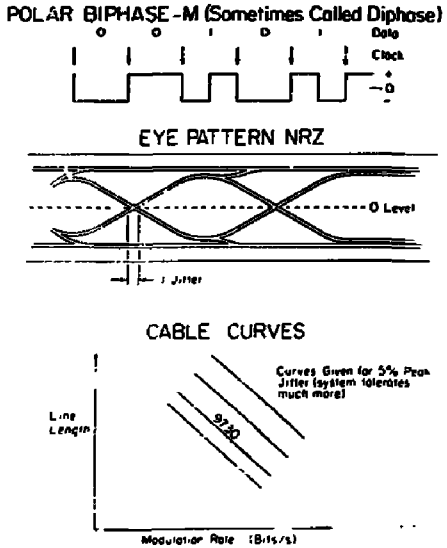

Figure 5. Line Signals.

7. ENCODER/DECODER

The encoder (transmitter) and decoder (receiver) circuits are shown in Fig. 6. The $J-K$ flip-flop assures a transition at each bit boundary as well as a transition at the center for a "one". Sync and termination generation are not shown.

The decoder is one-shot based, and derives clock pulses and sync from the data as well as NR2 data. A considerable amount of line distortion can be tolerated by this circuit.

8. ADDITIONAL SYSTEM COMPONENTS

Other devices and programs at SLAC are important to this development. The include the MBCD, Multibus CAMAC Driver designed by M. Browne; the SBD, Serial Branch Driver, designed by L. Paffrath, a CAMAC based driver; test equipment designed by W. Montalvo, and a new synchronous repeater, designed by I. Smith.

ACKNOWLEDGEMENTS

The author wishes to acknowledge the support of the *I* and *C* group at SLAC, under R. Melen, and the contributions of M. Browne, S. Mackenzie and L. Paffrath. H. Wals first suggested the use of the FPLS to implement the control logic of this SCC.

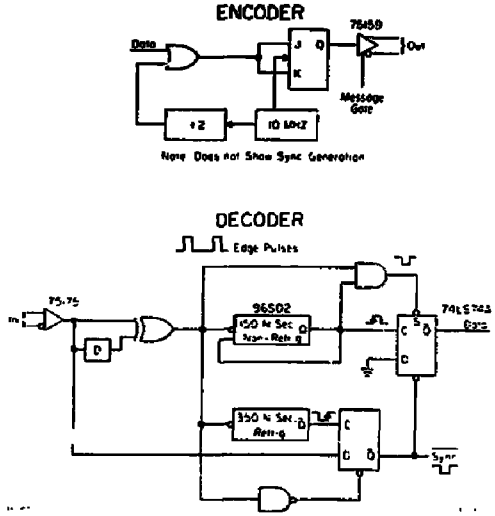

Figure 6. Encoder/Decoder Circuits.

Table 1. Design Principles

- 16 Crates on Bus
- TTL Differential Line Signals (RS-422A)
- Commercial Twisted Pair Cable, 500 ft. (min)
- 5 Megabits/s, 10 μs Transactions
- Bi-Phase Modulation
- Self-Clocking
- Unique Leading Sync
- Block Transfer Capability, Single Address
- *L* Signal Readout
- Transparent, No Processing
- No Parity Check

Table 2. Special Commands Of The SCC

- **N(31)** Addresses All Modules
- **N(30) F(10) A(0-7)** Read L Signals, I Line, L Enable
- **N(30) F(24) A(9)** Set $I = 0$
- **N(30) F(26) A(9)** Set $I = 1$
- **N(30) F(24) A(10)** Disable L
- **N(30) F(26) A(10)** Enable L
- **N(28) F(26) A(9)** Run Cycle with $C = 1$
- **N(28) F(26) A(8)** Run Cycle with $Z = 1$, Set $I = 0$, Disable L
- Power On: Same as Z

FIGURE CAPTIONS

1. Photograph of the Unit.
2. Typical Application at SLC.
3. Line Protocol.
4. Serial Crate Controller-Block Diagram.
5. Line Signals.
6. Encoder/Decoder Circuits.

TABLE CAPTIONS

1. Table 1 Design Principles.
2. Table 2 Special Commands of The SCC.