WAVEFORM DIGITIZING AT 500 MHz

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ABSTRACT

Experiment E787 at Brookhaven National Laboratory is designed to study the decay $K^+ \to \pi^+\nu\bar{\nu}$ to a sensitivity of 2×10^{-10}. To achieve acceptable muon rejection it is necessary to couple traditional methods (range/energy/momentum correlation) with observation of the $\pi^+ \to \mu^+\nu$, $\hookrightarrow e^+\nu\bar{\nu}$ decay sequence in scintillator.

We report on the design and construction of over 200 channels of relatively low cost solid state waveform digitizers. The distinguishing features are:

8 bits dynamic range, 500 MHz sampling, zero suppression on the fly, deep memory (up to .5 msec), and fast readout time (100 μsec for the entire system). We report on data obtained during the February-May 1988 run showing performance of the system for the observation of the above decay.

INTRODUCTION

The digitization of analog signals from standard high energy physics detector elements has often enriched our understanding of the devices generating the signals and frequently improved the performance of these systems through more thorough software analysis of the data. In a small class of experiments (ours included) such digitization is vital for extracting physics information unavailable through other readout means. In future high rate experiments at colliders such digitization will play a central role in pipelined systems necessary for high speed data acquisition. In this note we describe a system of 200 channels of 500 Msample/sec 8-bits of dynamic range digitizers used in Brookhaven National Laboratory (BNL) experiment E787 to observe the decay sequence $\pi \to \mu\nu$, $\hookrightarrow e^+\nu\bar{\nu}$ in scintillator. The system is extendable to even larger number of channels and has several features judged vital to high rate experiments such as zero-suppression prior to write, deep memory, fast readout in a standard format (FastBus) and on-line triggering capability.

PHYSICS REQUIREMENTS

BNL experiment E787 is designed to study the decay $K \to \pi\nu\bar{\nu}$ to the level of 2×10^{-10} in branching ratio. Figure 1 shows an outline of the detector. Low energy kaons (750 to 800 MeV/c) from a separated secondary beam are degraded by a Be degrader and stopped in a 2000 element (of 2 mm each) fiber target. The charged decay products are momentum analyzed in a cylindrical drift chamber ($\Delta p/p = 2\%$) and stopped in a 15 layer, 24 azimuthal sector, scintillator range stack.

A high rejection photon veto (lead-scintillator) surrounds the detector in both the barrel and endcap regions. A 10 kGauss solenoidal coil

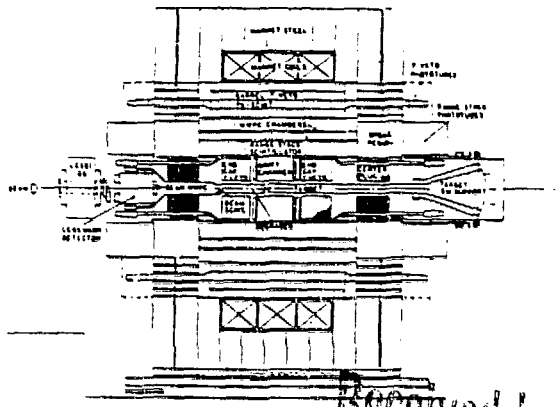

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Fig. 1. E787 Detector

surrounds the entire detector and a thick iron yoke and endcaps provide excellent flux return.

While it is not the purpose of this note to provide a detailed description of the detector, it is useful to give a brief outline of background rejection mechanisms. Roughly speaking the major backgrounds are $K^+ \to \pi^+\pi^0$ and $K^+ \to \mu^+\nu$ and $K^+ \to \mu^+\nu\gamma$. The first is rejected by a combination of the π^0 rejection from the photon veto ($\approx 5 \times 10^{-6}$) and by working with charged pions above the $K \to \pi^+\pi^0$ charge pion momentum of 205 MeV/c. The other two background's rejection depends on a combination of range/momentum/energy analysis and the observation of the decay sequence of the stopped charged track in the range stack. The pion will decay into a mono-energetic muon which in turn will decay into an electron and two neutrinos, while the muon will decay directly into an electron and two neutrinos. In order to observe the decay sequence in the scintillator one needs a device capable of digitizing the photomultiplier signals with sufficient performance. There are roughly 800 channels and the summing of more than 4 PMT channels into one digitizer is undesirable from the point of view of background rate and signal degradation. The parameters of the decay sequence set the performance scale of the digitizers:

(1) Since the typical signal is 40 nsec wide at the base and the pion lifetime is 26 nsec one needs sampling rate of upward of 300 Msamples to be able to detect early decays (less than 10 nsec). The detection of those decays is vital to having an overall large acceptance for pio

(2) Since the muon lifetime is 2.2 microseconds one needs a memory depth of at least 10 microseconds to insure high efficiency for the detection of the muon decay.

(3) The energy of the stopping pion ranges from 1 to 30 MeV while the decay muon is always 4 MeV in energy. In order to observe the muon with sufficient resolution and still have a small number of pion overflows it is necessary to have a dynamic range of at least 7 bits.

(4) The experiment is designed as a high rate, high statistics experiment. In order not to compromise the basic design of the data acquisition system, one needs a suppression of the large number of zero points prior to writing. This insures fast readout of the overall system.

We will show that our final design of the 500 Msample 8 bit system achieves all the above goals. Figure 2 shows a block diagram of the basic digitizing channel. It consists of four parts: the flash A/D converter, the custom data handling chip, fast ECL 256 x 4 memories and data acquisition readout protocol electronics.

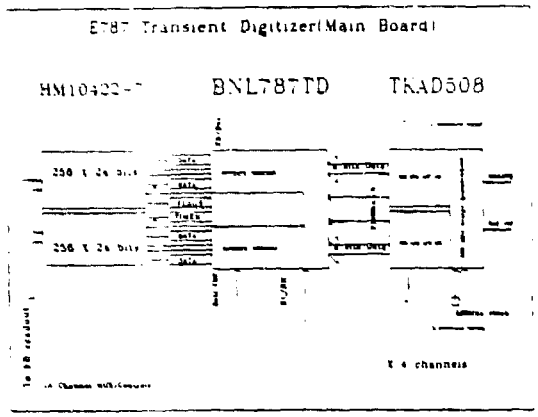

Fig. 2. Basic Digitizer Channel

THE FLASH A/D

In choosing the basic digitizing technique flash A/D's offer a somewhat lower dynamic range than charge coupled devices (CCD) or analog memory devices. However, they offer the distinct advantages of having the ability to subtract zeros prior to writing and of generally faster access to the data, as well as of having large depth of memory (or pipe). Our choice for the task was a Tektronix A/D converter hybrid TKAD508 consisting of a 500 Msample/sec Sample-and-Hold circuit and two interleaved 250 Msample/sec A/D converters. The hybrid with all 3 IC's comes in a standard 84 pin flat pack with 7 watt power consumption. Two differential input ports are provided, both with 50 ohm internal termination. Two separate sets of reference voltages (positive and negative) must also be provided to the hybrid. The driving clock is a pair of differential 500 MHz square waves. The output of the hybrid is a pair of interleaved bytes of data at a rate of 250 MHz. One byte is output on the rising edge of the clock, while the other is output on the falling edge of the clock. The device is capable of 7 effective bits performance at 90 MHz input frequency.

We use the two analog inputs in a non-standard fashion. Since our signals are all of one polarity (negative) we input the analog signal on one side and a DC level generated by the 12 bit DAC on the other. This allows to have a software settable threshold of .25 mV sensitivity while the digital threshold cut is at a fixed count of 7. This flexibility is necessary since standard PMT signals are transported on RG8X and RG58 cables and can acquire small DC shifts. Those small shifts can be disastrous in the sense that they push all signals above the zero suppression cut and cause a huge increase in the amount of data generated by the device. DAC level correction to those DC shifts effectively eliminated this problem as well as provide an efficient means of online testing and calibration.

The output rate of the flash A/D of two bytes at 250 MHz renders it difficult to deal with since no standard memory runs at such a fast rate. Also, as mentioned earlier, it is desirable to do zero suppression prior to writing in memory. We opted to design a custom IC to handle both the speed of the data and zero suppression, as well as the various housekeeping and digital readout duties required in such a device. The IC (BNL787TD) is commonly called the Macro-Cell and is described in the next section.

THE DATA HANDLER (MACRO-CELL)

The custom-designed IC BNL787TD is a time demultiplexer capable of handling input data rates of up to 400 MHz (it normally runs at 250 MHz) with power consumption of 12 watts. It is implemented in Signetics ACE2200 current mode logic technology and has roughly 2150 gate equivalent. Figure 3 shows a block diagram of the IC. In operation it has as input 2 bytes of data and a synchronizing clock (pair differential). The output is 4 bytes of data at half the input frequency. In addition the IC generates two identical sets of 8 bits of memory address for controlling the external ECL RAM. The

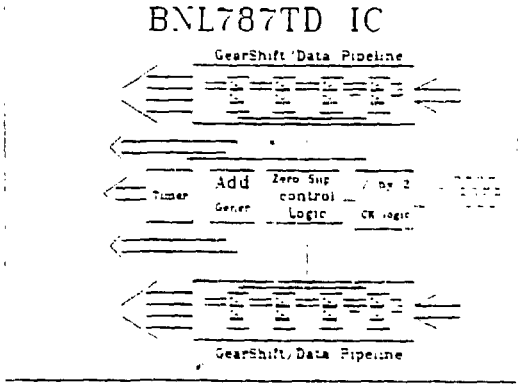

Fig. 3. Data handler custom IC block diagram

zero suppression is achieved by incrementing the memory address AFTER at least one of the input bytes has a value greater than 7. In effect values below 7 are overwritten by the subsequent data word. In addition a single input line (Enable Suppression) can, if held in ECL high state, force memory address incrementing regardless of the data value. This is a useful feature for debugging and testing. Since data is often overwritten, a timer word is necessary to identify the sequence of data in time. There is, internal to the IC, an 8 bit timer running at half input clock frequency, and when its value is written to the external RAM, can be used to reconstruct the data in time. The timer is then capable of registering times of up to 2 microseconds. In order to extend the depth of memory beyond 2 μsec a boundary word is forced into the memory every time the timer overflows. In a complete no-data event the memory is filled with boundary words (256 of them). The maximum memory depth with this scheme is .5 millisecond. In addition the IC accepts an input control line (Read/Write) that identifies the state of data taking: write (ECL low) during analog digitization and read (ECL high) after triggering and during readout by the data acquisition system. A word of data is forced into the memory every time this line changes state from write to read. This identifies the trigger time and synchronizes all channels in different boards or crates. Since the external RAM is used as a last-in-first-out (LIFO), a single input (decrement) is used to decrement the memory address during readout.

THE EXTERNAL MEMORY

The external RAM must be fast enough (125 MHz or 8 nsec) to handle the Macro-Cell output data. We chose the Hitachi HM10422-7 256 x 4 ECL memory with access time of 4 nsec. The data word width is 48 bits (32 bits of data, 8 bits of time and 8 bits of flags to disentangle the 4-PMT-to-one-channel sum) and one needs 12 such memories per channel (total power consumption of 12 watts). We operated the memory in a fashion where we do not strobe the write enable line, rather rely on the fact that the data and address lines arrive at exactly the same phase in order not to corrupt the memory by writing to the wrong location. That meant that the address lines from the Macro-Cell must be generated with less than 200 psec skew and the PC board layout has to insure similar performance. To reduce the load on the address line we organized the memories into two banks of 6 memories each (hence the two identical address line sets generated by the Macro-Cell). The entire memory system is placed on a separate PC board which is plugged into the mother board via a set of connectors. This makes for easier construction and debugging.

OVERALL ORGANIZATION

The system is organized into six FastBus crates each supporting up to 32 channels (see Figure 4). Each basic board is a double-width FastBus module with 4 channels. Each FastBus crate also contains a single board (TDMASTER) which houses the 32 DAC level generators and is used to readout the data. Because of the bandwidth limitation and expense of FastBus, the data is readout by the TDMASTER from the 32 channels over a special bus on the auxilliary backplane and transferred to the crate controller on

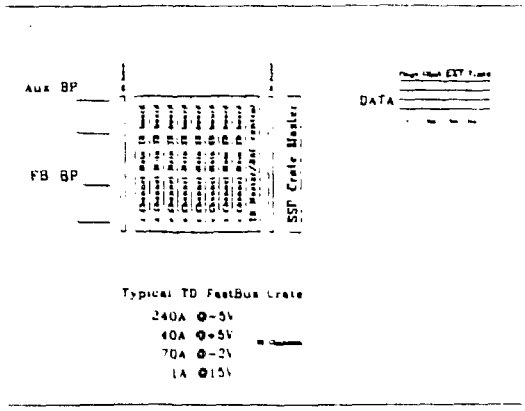

Fig. 4. Single crate organization

the main FastBus backplane. The crate of 8 TD boards and the TDMASTER then looks logically to any crate master as a single board at the geographical location of TDMASTER and containing 32 channels of secondary addresses. In addition each crate houses a SLAC Scanner Processor (SSP) as a crate master and two 500 MHz clock fanout boards. Total power consumption on the crate is 240 A on the -5 V, 70 A on the -2 V, and 40 A on the +5 Volt and 1 A each on the +15 and -15 Volt lines. Cooling is achieved by forced air through water-cooled heat exchangers. The typical local temperature is 25 °C near any of the devices. The overall readout time for the crate is 100 microsecond (with no software analysis).

ON-LINE TRIGGER AND OVERALL PERFORMANCE

100 channels of the system were operated between February and May of 1988. Roughly 3 million selected decays were recorded on tape. It is perhaps useful to show the obligatory typical event display. Figure 5 shows a muon pulse with the subsequent decay muon pulse.

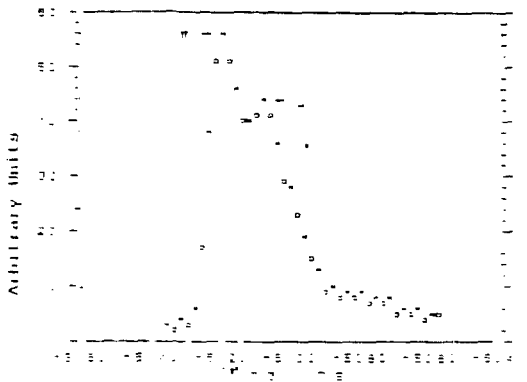

Fig. 5. Typical $\pi^- - \mu^-\nu$ decay pulse

There are essentially two parameters that characterize the performance of the system: the pion detection efficiency and the muon rejection efficiency. Both numbers are function of the exact software procedures used to analyze the data. Since in on-line analysis (done in the SSP) one is forced into cruder procedures, one might expect that on-line trigger methodology and efficiencies to be different from final off-line counterparts.

In the on-line analysis muon rejection was achieved by comparing the total pulse area (or sum of all the digitized voltages) to the maximum digitized voltage. These ratios can be converted to pion or muon detection efficiency as a function of the cut on the ratio. Figure 6 shows both efficiencies. In on-line rejection we obtained a factor of 7.2 rejection of muons for only a 28% loss of pions.

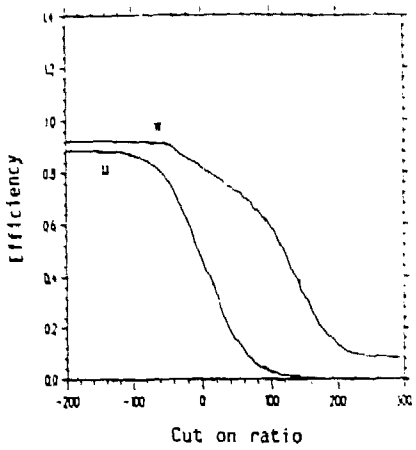

Fig. 6. Efficiency of the algorithm for pions and muons as a function of the cut on the extra area

OFF-LINE ANALYSIS

The off-line analysis naturally aims at a higher pion detection efficiency and higher muon rejection, albeit at the cost of extensive computing and reliance on highly complex algorithms. The best algorithm designed attempts to fit pulses in the

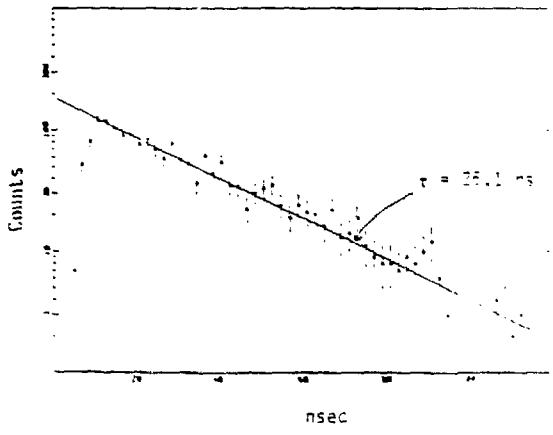

Fig. 7. Pion decay time distribution

stopping counter to two different hypotheses: the first is that of a signle pulse, and the second is that of two pulses of arbitrary size and time. Based on the χ^2 fit value one selection or the other is made. If the selection is that of two pulses the second pulse time and size are determined. The pulse time distribution is shown in Fig. 7, and corresponds accurately to the pion proper lifetime. The reader will note that the algorithm efficiency drops for times less than 8 nsec. This is due to the combination of rise-time and relative pulse sizes conspiring to blurr the two pulse distinction. Figure 8 shows the second pulse size which is consistent with a monoenergetic muon of roughly 4 MeV of kinetic energy. Figure 9 shows an example of

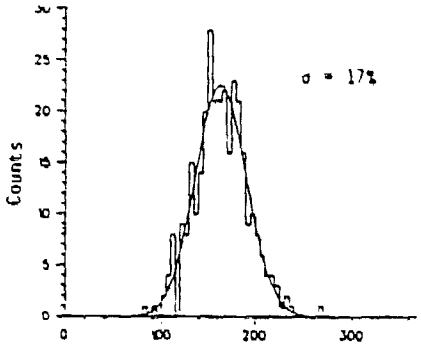

Fig. 8. Second pulse (u) area distribution

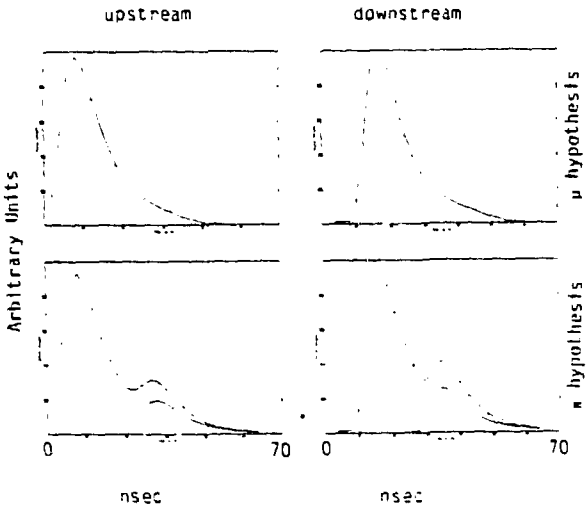

Fig. 9. Typical pulses from two ends of stopping counter fitted for both μ and π hypotheses

a real pulse and the two hypotheses fits for PMT pulses on both ends of the counter. In the final off-line analysis we achieved an overall muon rejection of better than 10^{-4}, with roughly 75% pion acceptance.

CONCLUSION

We have constructed and operated a system of transient digitizers capable of detecting the decay $\pi^+ \to \mu\nu_{e\nu\bar{\nu}}$ with 75% efficiency and of rejecting $\mu_{e\nu\bar{\nu}}$ decays to a level of 10^{-4}. The features of the system make it of interest to future high rate collider-type experiments.

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