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A DATA ACQUISITION AND EXPERIMENT CONTROL SYSTEM FOR A LARGE AREA NEUTRON DETECTOR*

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arrays, a main program and up to 62 program overlays. For the reasons outlined below, the main program and overlays are coded in FORTRAN. The common node can also accept data from the individual experiment control nodes for spooling on a shared peripheral device (e.g., magnetic tape) for subsequent analysis at the Central Scientific Computing Facility at BNL.

Functions of the experiment control and data acquisition node, such as spectrometer control, are accessible via FORTRAN level subroutine calls to system level routines within the experiment control node. Thus, the experimenter, who has intimate knowledge of the logical flow and data structure of his experiment, generates an experiment procedure by using these subroutines in a FORTRAN program. No other language is necessary since all special experiment functions are provided in these subroutine calls. The use of the experiment control nodes for any data reduction except that required for validation of data quality is discouraged since the typical node lacks the computational power necessary to reduce data from a complex experiment.

Generation of FORTRAN experiment control code takes place on the program development node, which is also part of the network. Code production is made as automated as possible through the use of batch streams on the program development node. Editing, compiling, linking and source library management all are done on this node.

The data-acquisition and experiment-control system for the small-angle neutron scattering facility is one of the complex nodes within the network. It has a data rate capacity, data array size and functional complexity beyond that required for most of the other nodes in the network. Yet, due to the generality of the network approach, the experiment is not hindered by the architecture of the system.

The data acquisition and experiment control node for the small-angle neutron scattering facility may be divided logically into a set of modular subsystems, each with its complement of hardware and software. (As noted previously, all experiment control operations within a particular subsystem are executed by an appropriate series of FORTRAN subroutine calls.) The modularity is implemented by the library management and automated linking routines within the program development node. Thus it becomes possible to transfer conveniently subsystems from one experiment to another. This technique allows complex systems to be assembled in a relatively short time.

Implementation

The data-acquisition and experiment-control node for the small-angle neutron scattering facility contains two digital processors, one general and one special purpose. The general purpose processor which executes all the experiment control code as described above, is a DEC PDP11/34* with 24 kwords of core memory and a console device. The hardware portions of most of the various subsystems are connected to this processor via the UNIBUS. These include a nine track magnetic tape drive and controller, a storage display terminal for graphical display of data, the neutron spectrometer control electronics package, a paper tape reader, and either a communications link to the common node of the Reactor Experiment Control Facility or a disk. Either one of these devices may be selected. This arrangement is shown in Fig. 1.

*DEC and PDP and UNIBUS are registered trademarks of the Digital Equipment Corporation.

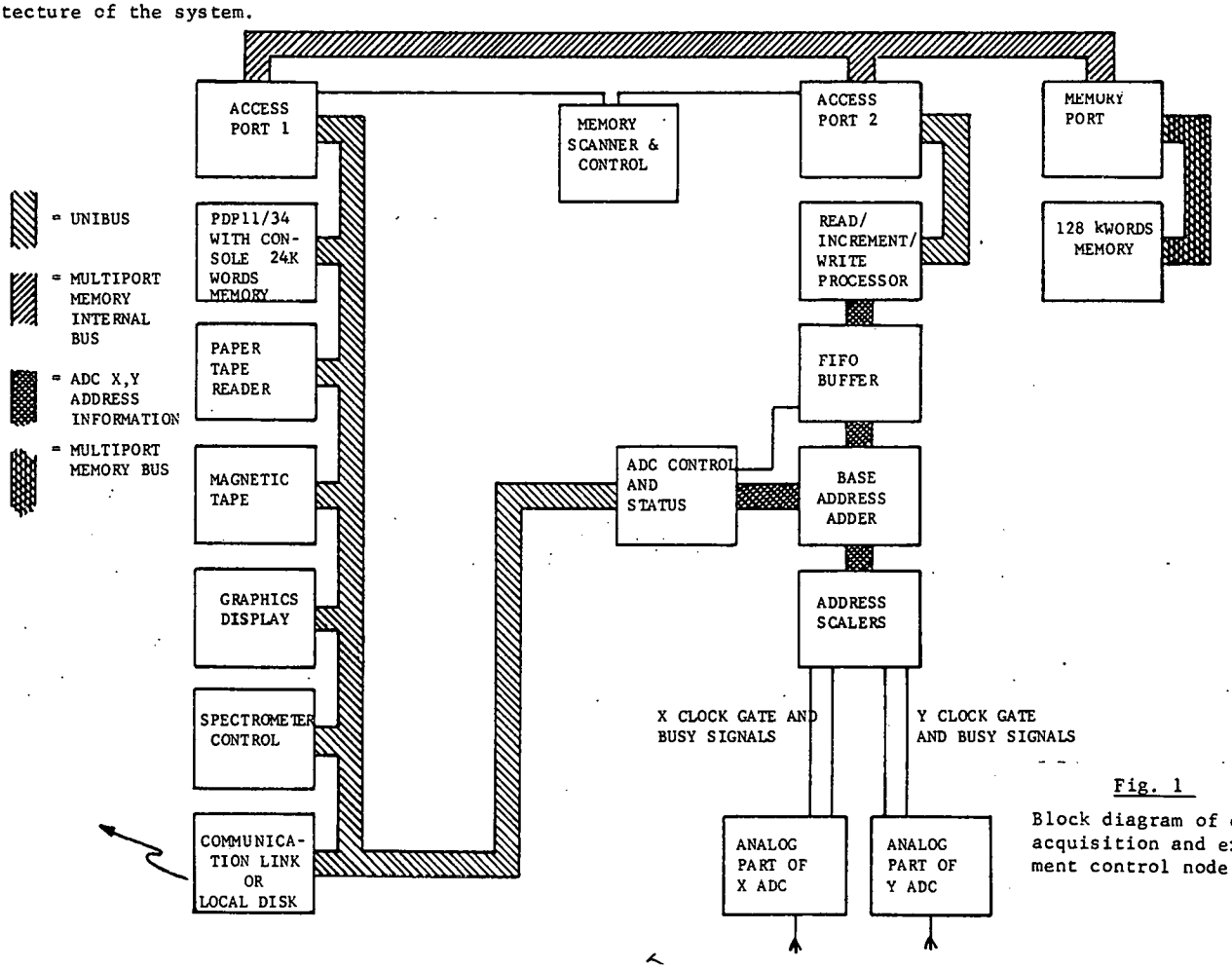

Fig. 1

Block diagram of data acquisition and experiment control node.

There are two additional devices connected to the processor UNIBUS, the first of which is the multiport memory. This is a device whereby several processors may communicate to common data arrays contained in a 30 bit address space distinct from the local processor address space (Dimmler and Hardy, 1977). Each processor reads or writes in the memory through an access port. Access to the multiport memory is through a 4096 word window between addresses $14\emptyset\emptyset\emptyset\emptyset_8$ and $16\emptyset\emptyset\emptyset\emptyset_8$ in the PDP11/34 address space. A 16 bit map register in the processor I/O page provides the high order physical address bits necessary to read or write to a location in the multiport memory. A scanner sequentially interrogates each access port in the node for a read or write request in multiport memory. If a request is pending, the scanner halts for the duration of the request and then continues. Thus each processor in the node has equal priority for reading or writing in the multiport memory. The access port for the PDP11/34 shown at the top of Fig. 1 is connected to both the UNIBUS and the multiport memory internal bus.

The second of these two devices is the dual-parameter analog-to-digital converter. The control and status register, and base address register are connected to the PDP11/34 UNIBUS. The read/increment/write processor contained in the analog-to-digital converter forms the special purpose second processor of this two processor experiment control node.

The general configuration of the analog-to-digital converter is shown in Fig. 1. Data from the two dimensional position-sensitive neutron detector accumulates in the multiport memory where the PDP11/34 can access it through its memory port. Although the PDP11/34 controls the starting and stopping of data collection, and the section of memory into which the data is collected, it does not process individual events in any way. Therefore no interrupts, direct memory transfers, etc., are necessary in the PDP11/34 to collect data.

The detailed configuration of the dual parameter analog-to-digital converter is shown in Fig. 2. Analog data from the x- and y-coordinate position readouts along with start signals arrive at the analog portions of the x- and y-digitizers. These units, which are housed in standard NIM modules, may be remote from the remainder of the experiment control system. They are generally kept close to the position-sensitive detector readout to avoid transmitting sensitive analog signals over long cables. The outputs of these units, the x- and y-clock gates and busy logic signals, are transmitted to 100 MHz address scalers over controlled impedance, shielded, twinaxial cables with good noise immunity. The address scalers have a capacity of 12 bits in each coordinate with address overflow latchup and are implemented in emitter coupled logic. The digitized x- and y-coordinate information then transfers to a fast address latch, which provides one level

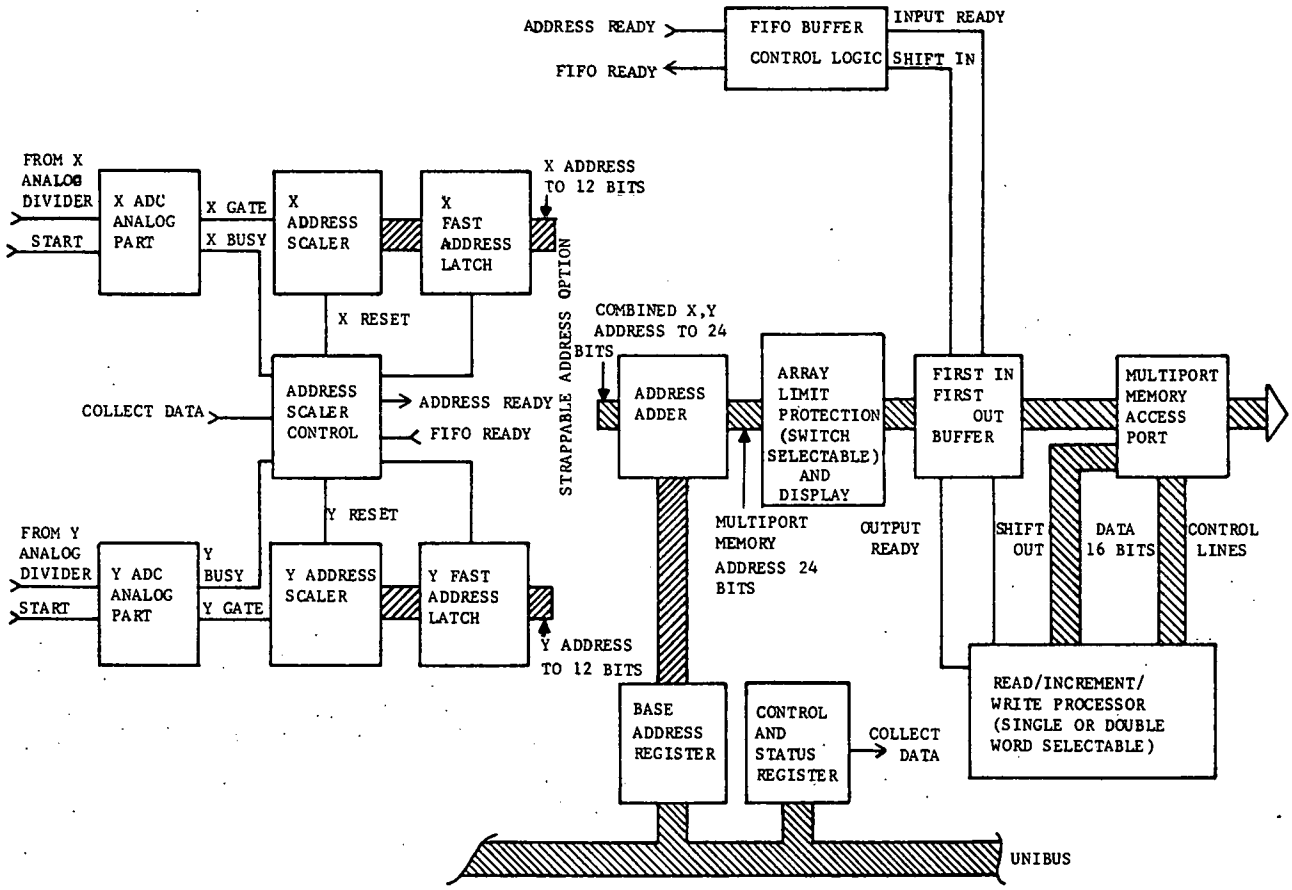

Fig. 2

Detailed block diagram of analog-to-digital converter. This is expanded from the righthand side of Fig. 1.

of time derandomization. A new event may be digitized after this transfer. The x-and y-addresses are concatenated in a hardware wireable jumper block. The analog-to-digital converter is currently configured for 7 bits each of x- and y- addresses formed into a 14 bit combined address. A 30 bit base address with the top 16 bits settable by the PDP11/34 is added to the combined x- and y-address to form the physical address to be incremented in multiport memory. This address must fall within the limits selected by the array limit switches otherwise the data is not transferred to multiport memory but ignored. Incoming data is displayed on binary LED's as a visible indication of proper operation. If the data falls outside the array limits, the LED's latch the erroneous data and an error is indicated. After passing this test a 64 level first-in-first-out buffer accepts the 30 bit physical address. Data from the output of this buffer is then presented to the address lines of the multiport-memory access port, and the read/increment/processor starts its memory cycle. The read/increment/write processor increments either a single (16 bit) or double (32 bit) memory location selected by wireable jumper on the circuit module. The node is currently configured for single word operation since data rates in small-angle neutron scattering are such that overflow is unlikely in a memory cell. If an overflow occurs, the content of the cell is set to all ones to indicate this condition. The memory cycle time of the read/increment/write processor is ~ 2.5 μsec including the multiport memory overhead.

A timing diagram for an event is shown in Fig. 3 up to the point where data enters the first-in-first-out buffer.

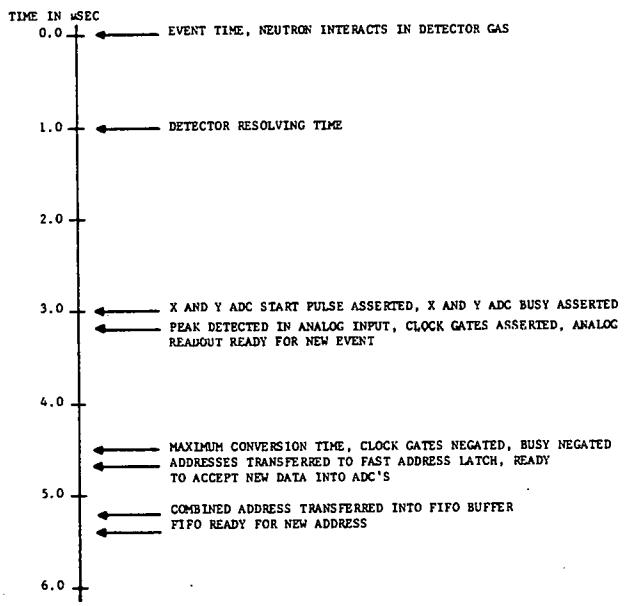

Fig. 3

Analog-to-digital conversion timing chart for a neutron interaction.

The event takes place in the ^3He of the detector gas at t = 0.0 μsec. At t = 1.0 μsec, the detector electronics is no longer sensitive to event pileup. Two microseconds later, x and y analog position signals are ready for digitization. A new event may start to be digitized at t = 4.7 μsec, and the first-in-first-out buffer is ready for a new address at t = 5.3 μsec. The limiting time in the front part of the analog to digital converter is the 3 μsec taken for analog processing of the event since the digital portion of the system is ready for a new event ~ 2.5 μsec after the start of digitization.

Dead time is an important consideration in any such analog-to-digital converter, and, in particular, variations in converter dead time can lead to significant loss of data accuracy. The multiport memory with its attendent lack of priority structure can cause variation in access port deadtime when the PDP11/34 is transferring data at high rates. The way in which a graphic display of neutron-detector data works demonstrates how this variation in access port deadtime can occur.

The PDP11/34 periodically reads the incoming data buffer in multiport memory and displays the data on the graphics terminal attached to its UNIBUS. In the worst possible case, where data is transferred from multiport memory to a buffer in internal PDP11/34 memory, the transfer loop consists of a dual-address autoincrement move instruction, an address compare instruction and a conditional branch instruction. The single pass time through this loop is ~ 9 μsec for this processor and the multiport memory read time is ~ 1 μsec with overhead time added. Thus the analog-to-digital converter access port would be dead 11% of the time during this transfer, thereby increasing the average read/increment/write processor deadtime and causing a variation in data deadtime loss. A simplistic solution to this problem would be to forbid access to the multiport memory by other processors during data collection. This, however, would defeat the purpose of this device.

The proper solution is to insert a first-in-first-out buffer for the digitized position data ahead of the analog-to-digital-converter read/increment/write processor. This device converts time-random data at its input to nearly time-periodic data at the output. Thus only the periodic data rate capacity of the read/increment/write processor is reduced by 11%. If the time-averaged data rate from the position-sensitive detector is less than the synchronous data rate capacity of the read/increment/write processor (in the limit of an infinitely deep first-in-first-out buffer), then no data is lost due to read/increment/write processor deadtime. The first-in-first-out buffer used in this node is 64 levels deep so that this relationship is valid. The maximum usable time-averaged data rate from the position-sensitive detector is ~ 10^5 events/sec. Thus the read/increment/write processor must update the data in less than ~ 9 μsec including multiport memory overhead time if memory accesses from the PDP11/34 are to have negligible effect. This time was demonstrated above to be 2.5 μsec. Hence the limiting deadtime in the system is the analog event processing time.

Subsystems

Each device described above requires control code to develop it into one of the set of modular subsystems described previously. Only when these are taken together are the subsystem functions accessible to the user through FORTRAN subroutine calls. Table 1 summarizes the subsystem names and functions. Each tabulated function corresponds to a FORTRAN subroutine call except where noted. An array in multiport memory is always allocated by a subroutine in the extended FORTRAN array subsystem before use by any other subsystem. The PDP11/34 is understood to be a device used by all subsystems to execute the appropriate code.

Remarks

At the beginning of this paper a set of objectives was laid out, some of them rather subjective, for an

Table 1. Major Subsystems Within the Data Acquisition and Experiment Control Node for the Small-angle Neutron Scattering Facility.

SUBSYSTEM NAME	MAJOR FUNCTION	HARDWARE USED BY SUBSYSTEM
Analog-to-digital Conversion	1. Set or read base address register 2. Start data collection to an array in multiport memory 3. Stop data collection 4. Test for data collection running 5. Collect for preset time 6. Collect for preset number of incident beam neutrons.	1. Analog-to-digital converter 2. Multiport memory
Extended FORTRAN Data Arrays	1. Allocate a FORTRAN array in multiport memory in up to 3 dimensions 2. Test if an array exists 3. Read FORTRAN integer, real, double integer or byte data from an array† 4. Write FORTRAN integer, real, double integer or byte data to an array† 5. Move data from one array to another.	1. Multiport memory
Magnetic Tape	1. Read data in fixed format from 9 track magnetic tape to an array in multiport memory by specifying file name. 2. Write data to 9 track magnetic tape from an array in multiport memory and name resulting file. 3. List files present on tape. 4. Find a file present on tape.	1. Nine track magnetic tape unit and controller 2. Multiport memory
Spectrometer Control	1. Set a particular axis in the spectrometer to the specified angle (up to 8 axes). 2. Halt an axis in process of moving 3. Set an angle encoder. 4. Read an axis. 5. Set an axis to zero angle position 6. Position an axis manually to desired angle	1. Neutron spectrometer and controller
Graphic Display	1. Consists of a package of commercially available subroutines for graphical display of data on the particular model of display terminal used.†	1. Storage tube graphics display terminal and interface.
Overlay	1. Load a FORTRAN overlay segment from the specified device to the overlay region of PDP11/34 2. Return to main program from current overlay segment.	1. Overlay storage device

†several FORTRAN subroutines.

experiment control facility for small angle neutron scattering. The following list summarizes some objective performance specifications for the system.

a) 30 bit address space available for position-sensitive detector data;

b) the ability to map incoming detector data into a series of arrays to facilitate time sequential studies;

c) simultaneous graphical display and acquisition of data;

d) data losses limited by 3 μsec detector analog position readout; and

e) either 16 bit or 32 bit data at each position location in the two dimensional array.

Analysis of the more subjective goals is left to the reader.

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