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LATCH-UP AND RADIATION INTEGRATED CIRCUIT -- LURIC: A Test Chip for CMOS Latch-Up Investigation

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Abstract

A CMOS integrated circuit test chip (Latch-Up and Radiation Integrated Circuit -- LURIC) designed for CMOS latch-up and radiation effects research is described in this report. The purpose of LURIC is (a) to provide information on the physics of CMOS latch-up, (b) to study the layout dependence of CMOS latch-up, and (c) to provide special latch-up test structures for the development and verification of a latch-up model. Many devices and test patterns on LURIC are also well suited for radiation effects studies. LURIC contains 86 devices and related test structures. A 12-layer mask set allows both metal gate CMOS and silicon gate ELA (Extended Linear Array) CMOS to be fabricated. Six categories of test devices and related test structures are included. These are (a) the CD4007 metal gate CMOS IC with auxiliary test structures, (b) ELA CMOS cells, (c) field-aided lateral pnp transistors, (d) p-well and substrate spreading resistance test structures, (e) latch-up test structures (simplified symmetrical latch-up paths), and (f) support test patterns (e.g., MOS capacitors, p^+n diodes, MOS test transistors, van der Pauw and Kelvin contact resistance test patterns, etc.). A standard probe pattern array has been used on all twenty-four subchips for testing convenience.

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SECTION I - INTRODUCTION

Latch-up (four-layer pnpn turn-on) has been known to present a potential problem in many integrated circuits. Junction-isolated CMOS integrated circuits are especially susceptible to latch-up. In order to develop and evaluate methods and processes for the control of latch-up, it is necessary to understand the physics of latch-up and to have models for the latch-up phenomena.

This report describes an integrated circuit test chip (Latch-Up and Radiation Integrated Circuit - LURIC) designed for CMOS latch-up and radiation effects research. This research was begun at Stanford University in 1977 with the overall goal of developing a general algorithm which can be applied to the prediction of the latch-up threshold for a specified CMOS layout and process. In addition, this algorithm can be used to evaluate methods for latch-up prevention.

The development of latch-up path models, and a threshold prediction algorithm, requires a considerable amount of empirical data for isolating the principal parameters involved in latch-up. For example, test structures are needed to obtain data on the influence of layout and impurity profiles upon latch-up. Also, special latch-up test vehicles are required to verify the model. The test chip described in this report was designed to fulfill this need.

Section II discusses the need for special test structures for latch-up research and presents the general philosophy used in designing the test chip. The test devices and related structures are described in Section III of this report. Table II may be considered the principal listing and description of the test devices. Finally, Section IV is a summary.

SECTION II - LATCH-UP TEST STRUCTURES

Figure 1 is a cross-sectional view of a typical CMOS integrated circuit. The electrical connections shown are for the standard CMOS inverter. Both a parasitic vertical npn transistor and a parasitic lateral pnp transistor are shown in Figure 1. The presence of these two parasitic transistors allows a latch-up, or regenerative, state to occur. Arrows indicate the lateral current paths which establish the voltage drops required to forward-bias the emitter-base junctions of these parasitic transistors. The physics of the latch-up process have been considered elsewhere [1, 2, 3].

Latch-up in CMOS integrated circuits is strongly dependent upon the substrate and p-well resistivities and geometrical layout [3]. It is convenient to consider these process and geometrical dependencies in terms of (a) the lateral resistances presented to both the substrate and p-well current paths, and (b) the current gains of the parasitic bipolar transistors.

The lateral resistances depend upon the substrate impurity concentration and the p-well impurity profile. Furthermore, the geometrical shape of the p-well and ohmic contact locations, along with the position of any diffused channel stops (i.e., guardbands), also play a role in determining these two resistance components. The magnitudes of the lateral substrate and p-well resistances essentially set the latch-up holding current necessary to sustain latch-up and influence the required current gain ($\beta_n \cdot \beta_p$) product to initiate latch-up [4]. Determination of the substrate and p-well resistances can be quite difficult. A straightforward analysis is complicated because (a) the guard-bands and source/drain diffused regions often are neither parallel or perpendicular to the latch-up path current flow, (b) the latch-up current flow is generally not laminar, and (c) the contact resistance can enter into the total path resistance.

In CMOS structures both a vertical npn and lateral pnp transistor form the pnpn latch-up path. The current gains of these transistors not only depend upon geometrical layout, and the base and emitter impurity profiles [5], but also on operating current density and minority carrier lifetime. In addition, the current gain of the lateral pnp transistor can be enhanced by two current-induced effects arising from the CMOS layout [6]. First, lateral current flow in the substrate, causing the lateral pnp to turn-on, forward biases the pnp emitter-base junction in such a way that the minority carrier injection occurs principally at the edge nearest the collector (in this case the p-well). This reduces the downward vertical injection of the pnp, which increases the emitter efficiency of the lateral pnp transistor. Second, an electric field is induced by the current flow across the base region which aids the transit of the minority carriers from emitter-to-collector. Computations show the current gain enhancement in wide base, field-aided, lateral transistors to typically be in the range of two to twenty [6].

Latch-up is especially difficult to analyze in commercially available CMOS integrated circuits because

(a) many parallel latch-up paths may simultaneously exist within any given CMOS integrated circuit, often leading to problems in latch-up path identification,

(b) adequate data is generally not available regarding impurity levels and diffusion profiles, nor are adequate "on-chip" test patterns included for obtaining such data, and

(c) severe restrictions usually exist which prevent accurate parameter information from being obtained from any given CMOS integrated circuit layout, hence, allowing only an incomplete analysis to be made.

These restrictions clearly limit the applicability of using commercial CMOS integrated circuits in a research program to correlate geometrical and process parameters to latch-up events.

In order to investigate the latch-up process in CMOS (or other latch-up prone integrated circuit families) and to develop adequate models for latch-up threshold prediction, special test structures are required. The objectives of the special latch-up test structures are

(a) to provide simple test structures for controlled latch-up, where layout is uncompromised by guardbands and other diffused regions, thus, allowing computer analysis for comparison and model testing,

(b) to provide simple test structures for isolating and quantitatively studying the influence of geometrical parameters upon latch-up,

(c) to allow variations in processing (e.g., diffusion depth of the p-well, substrate resistivity, and net doping at the surface of the p-well, etc.) for topologically identical structures, so that the influence of impurity levels and impurity profiles can be investigated,

(d) to provide field-aided lateral pnp test transistors, with controlled electric field in the base region, for studying and relating the enhanced current gain to the change in latch-up threshold,

(e) to provide spreading resistance test structures as an aid in the developing methods to calculate the lateral spreading resistance components, and

(f) to provide specially designed support test structures, located adjacent to the special purpose latch-up test structures, for collecting accurate resistivity and

and diffused layer sheet resistances for the analysis and modeling of latch-up.

The design and fabrication of the latch-up test structures and related support test structures represent an essential step in the program to quantify and understand the relevant parameters governing latch-up and to the successful modeling of the latch-up in CMOS and related integrated circuits.

SECTION III - DESCRIPTION OF LURIC TEST CHIP

This section describes the layout of the Latch-Up and Radiation Integrated Circuit (LURIC) test chip. The LURIC chip is 265 mils by 184 mils. It consists of 86 separate devices and test patterns arranged in 24 subchips (4 by 6 subchip array). Each subchip measures approximately 38.3 mils by 40.2 mils, and uses the RCA CD4007 bonding pad pattern, consisting of 14 bonding pads per subchip.

The same probe card can be used for testing each of the 24 subchips because of duplication in the bonding pad pattern. Furthermore, streets have been included so that any of the 24 subchips may be separately scribed and bonded in a 14-pin dual in-line package or other integrated circuit packages.

LURIC consists of 12 mask levels as summarized in Table I. Both metal gate and silicon gate processes are possible with the mask set--the corresponding mask levels for each process are listed in Table I.

Table II is a listing of all devices and test patterns on LURIC. Table II is formatted as follows: Each device or test pattern is assigned a "device number" (column 1), description and key dimensional information (column 2), chip location (column 5), pin or bonding pad positions (column 6), and defining process (column 3 for metal gate process or

column 4 for silicon gate process). In some cases, column 6 contains identifying remarks.

Figure 2 shows the bonding pad arrangement for each subchip and defines the pad number for correlation to the data in Table II. Figure 3 shows the locations of each of the 24 subchips. The 4 subchips in the upper left-hand corner of Figure 3 were previously used in another CMOS test chip (SDL TC-1 through SDL TC-4). The remaining 20 subchips are unique to LURIC (A1 through A20). Each group of devices or test patterns are briefly discussed below with regard to functional purpose and parameters to be determined for latch-up.

In addition, all drawings showing subchips and their layouts include the device numbers listed in column 1 of Table II.

A. SDL CMOS Test Array (Device Nos. 1-13)

The SDL CMOS test devices have been described in a Sandia Laboratories Technical Report (SAND78-1390) entitled, "CMOS Test Chip," by John D. McBrayer.

Subchip SDL TC-1 (Fig. 4) contains substrate and p-well MOS capacitors, both p-channel and n-channel gate and field oxide MOS test transistors, and an SCR test structure.

Subchips SDL TC-2 (Fig. 5) and SDL TC-3 (Fig. 6) are both patterned after the RCA CD4007 dual complementary pair plus inverter integrated circuit. Subchip SDL TC-3 is the complete CD4007 integrated circuit (RCA). However, subchip SDL TC-2 is unique to LURIC; the metalization layer (#11) has been modified. These modifications included disconnecting the n^+p gate protection diodes; however, the p^+n gate protection diodes may be biased to participate in latch-up or may be grounded (or may float). All source and drain regions are accessible

via the bonding pads, but no gate connections are possible. SDL TC-2 may be used in combination with the full CD4007 (SDL TC-3) to isolate selected latch-up paths. SDL TC-4 (Fig. 7) contains both n-channel and p-channel MOS transistors similar to those used in the CD4007. The bonding pad patterns used on SDL TC-2 and TC-3 are mirror images of the pin assignments usod on the RCA configuration. This should be accounted for when probing these two subchips and when packaging them (see SAND78-1390).

B. Field-Aided Lateral PNP Transistors (Device Nos. 14-23)

It has been shown that field-aiding can significantly enhance the current gain of the parasitic lateral pnp transistor in junction-isolated CMOS integrated circuits [6]. Ten field-aided lateral pnp transistor (FALT) structures have been included on LURIC. The purpose of the FALT structures is to study the field-aided current gain of the pnp transistors and to verify the wide-base, field-aided, lateral transistor theory [7]. Using the entire array of FALT structures, information can be obtained for the current gain dependence from base electric field strength, base width, ratio of emitter-to-collector lengths, and collector diffusion (p-well) depth. One FALT structure includes a field-plate over the base region between emitter and collector. Another FALT structure has an n^+ diffused bar between emitter and collector. Figures 8, 9, and 10 show the subchips containing the 10 FALT structures.

The connection for current gain measurements on the FALT structures is shown in Figure 11. The electric field in the base is established by passing a current between the two n^+ bar contacts. These n^+ diffused contacts also function as base contacts for the pnp transistors. By computing the ratio of the collector current, I_C, to the emitter current, I_E, the common base current gain, α, is obtained. The electric

field strength, E, is approximated by the bias voltage, V_{bias}, divided by the n^+ rail spacing (nominally 150 μm).

Subchips A1 and A2 (Fig. 8 and 9) contain 4 n^+ diffused rails for applying the dc bias to establish the base region electric field. Typically, the range of practical field strength ranges from approximately zero to about 100 volts/cm. The standard n^+ diffused rail spacing is 150 μm. Table III summarizes the pin connections for the bias rails on subchips A1, A2, and A3.

Table II lists the key dimensions of the FALT structures. Parameter W_b is the emitter-to-collector spacing, and parameter W_e is the emitter length (distance parallel to the collector). The corresponding collector length, denoted by W_c, is 150 μm, except on structure numbers 19, 22, and 23 (see Table II). Table IV relates the structure numbers of the FALT devices with the parameter variation to be studied.

C. Gated Diodes (N^+P and P^+N) (Device Nos. 26-27)

Gated diodes can be used to study leakage currents and surface recombination parameters [8-9]. Figure 12 shows the subchip containing two large gated diodes. Both a n^+p and p^+n gated diode have been included. The diffused and gate areas are approximately 3 $mils^2$ (~1950 μm^2), and 106.1 $mils^2$ (~68,500 μm^2), respectively. Additional data are given in Table II.

Leakage current in a reverse-biased pn junction can be separated into three components:

(a) generation within the depletion region,

(b) generation in the neutral bulk material within a diffusion length of the depletion region, and

(c) generation at the $Si\text{-}SiO_2$ interface where the depletion region meets the interface.

The silicon beneath the gate may be in three states; accumulation, depletion, and inversion. In the accumulated state, the leakage current will essentially consist of current components (a) and (b) for the diffused region (negligible contribution from gated region). Going to the depleted state from the accumulated state results in a sharp increase in leakage current. This is due to both an increase in current components (a) and (b), since the depletion region volume increases, and the initiation of current component (c) which now adds to the leakage current. Changing the gate potential so that the inversion state is attained will result in a decrease in total leakage current because current component (c) is reduced (only the contribution around the edge of the gate region remains). The interface generation velocity may be computed upon measuring the decrease in the leakage current when making the transition from the depletion state to the inverted state. Let ΔI represent the current decrease, then

$$\Delta I = \frac{1}{2} q n_i s_v A_{gate} \quad , \qquad (1)$$

where q is the magnitude of the electronic charge, n_i is the intrinsic carrier concentration, s_v is the $Si\text{-}SiO_2$ interface generation velocity, and A_{gate} is the gate area [8]. Actually, the area used in equation (1) should be the area where the depletion region meets the $Si\text{-}SiO_2$ interface. If the gate area is large, then A_{gate} will be a good approximation for the correct area. This condition holds for devices 26 and 27. It is worth noting that parameter s_v is often taken as a relative measure of the quality of the $Si\text{-}SiO_2$ interface. In addition, knowledge of the parameter s_v for the substrate region is necessary for estimating (and modeling) the base transport loss of the lateral pnp transistors due to surface recombination

(assuming the surface recombination velocity is equal to the surface generation velocity). This transport current loss is proportional to parameter s_v and the minority carrier density.

Additional parameters may be deduced from the leakage current measurements. The current due to generation within the depletion region (component (a)) is

$$I_{dep} = \frac{qn_i}{2\tau_o} X_d A_j \quad , \qquad (2)$$

where τ_o is the depletion layer generation time, X_d is the depletion layer width, and A_j is the area of the junction. The activation energy associated with I_{dep} is approximately 0.6 eV (approximately equal to $E_G/2$ because $I_{dep} \propto n_i$). The current due to generation in the neutral bulk (component (b)) is

$$I_{diff} = \frac{qn_i^2}{N\tau} LA_{eff} \quad , \qquad (3)$$

where N is the (average) impurity concentration of the bulk within one diffusion length of the junction, τ is the minority carrier generation (recombination) time, L is the minority carrier diffusion length, and A_{eff} is the effective junction area. The important quantity to know is the effective generation volume, represented by LA_{eff}. The activation energy associated with I_{diff} is typically 1.0 to 1.1 eV (approximately equal to E_G becuase $I_{diff} \propto n_i^2$). Usually $I_{dep} >> I_{diff}$ in silicon at $T \leq 300$ K. This can be verified for any particular structure by measuring the activation energy at the temperature of interest. The activation energy measurement should be carried out for gated diodes in the accumulated or inversion states so that current component (c) is minimized. When

$I_{dep} >> I_{diff}$ and the gate is biased for accumulation, then τ_o may be calculated from the measured leakage current and using the approximation $X_d A_j \cong 3000\ \mu m^3$. In general, volume $X_d A_j$ is bias dependent; more exact treatments should account for this fact.

D. Latch-up Structures (Device Nos. 29-44)

Sixteen latch-up structures (LATUS) have been included on LURIC. One of the goals of this research program is to develop a model for simulation of the latch-up phenomena. The LATUS test devices have been designed to provide a simple (single path) structure which will latch-up. All dimensions are carefully controlled; hence, the parameter input is simplified for computer simulation. In addition, key dimensions are varied to further confirm the computer model. The LATUS test structures can also serve as latch-up monitor test patterns for integrated circuit production lots.

Figures 13 through 16 show the 4 subchips containing the LATUS test devices. Figure 17 defines the principal dimensions associated with the LATUS test devices. Parameter W_b represents the lateral pnp transistor's base width. The spacing from the substrate's n^+ contact to the farthest edge of the p^+ region is denoted by L_{RS}, while the distance from the p^+ contact of the p-well to the farthest edge of the n^+ region is L_{RP}. Both L_{RS} and L_{RP} are key parameters which relate to the lateral resistance components (refer to the discussion in Section II).

Table V lists the bonding pad assignments for the 16 LATUS test devices. Table VI summarizes the parameter variation by structure number. Structure number 30 is the reference LATUS test device. The "wide" n^+ region in the p-well is 200 µm wide, whereas, the "narrow" n^+ region is 24 µm wide. The "tight guardband" completely surrounds and contacts the p-well only

on the edge nearest the substrate contact, and completely surround the p-well.

E. ELA CMOS Structures (Device Nos. 45-56)

Silicon gate extended linear array (ELA) CMOS [10] has been included on LURIC. Two categories of structures have been included: (a) functional blocks, and (b) p-well lateral resistance structures.

Subchips A9 and A10 (see Fig. 18 and 19) contain test structures designed to measure the lateral p-well resistance as a function of gate potential, V_{SS} contact location, and guardband position. All test structures on A9 and A10 have 6 μm wide gates. Subchip A9 contains dual V_{SS} contacts and subchip A10 has single V_{SS} contact structures. All lateral resistance test structures are formed in pairs, where one structure has a polysilicon gate, while its companion has the gate omitted. The guardband has been included in two forms: (a) the guardband meets the p-well on all four sides, and (b) the guardband meets the p-well on one side only (opposite the V_{SS} contacts), but still surrounds the p-well. In all cases, the p-well measures 124 μm by 56 μm (excluding lateral diffusion). V_{SS} contact sizes are 6 μm by 14 μm. The guard-band p^+ diffusion is 11 μm wide. Gate-to-gate spacing is 14 μm, and the n^+ diffusion within the p-well (pinched region) is 106 μm by 38 μm. Table II contains a description of each ELA lateral resistance structure and bonding pad locations.

Subchip A11 (Fig. 20) contains an asynchronous 1470 RST, while subchip A12 (Fig. 21) contains two 1720 two-input OR gates. One of the 1720's has V_{SS} bias straps across the p-well, whereas, the other does not (only V_{SS} contacts to p-well at outer edge of p-well). Both 1720's are embedded within dummy ELA sections. Table VII lists the bonding pad locations for these logic blocks.

In addition, a 4 μm gate ELA lateral resistance structure has been included (subchip A11). Device structures 52 and 53 are to be directly compared.

F. CMOS Inverters - Metal Gate and Silicon Gate (Device Nos. 57-60)

Subchip A13 (Fig. 22) contains two silicon gate CMOS inverters, and subchip A14 (Fig. 23) contains two metal gate CMOS inverters. *These pairs of inverters differ only by the* p^+ drain (of the p-channel MOS transistor) to p-well spacing (15 μm versus 25 μm). This spacing provides two different lateral pnp transistors base widths for investigating latch-up. All diffused regions are accessible via bonding pads (however, the gates for each inverter are connected together). This allows both the parasitic npn and lateral pnp transistors to be separately characterized via the terminals. Also, the n-channel and p-channel MOS transistors can be individually characterized.

The mask designed Z/L ratio of the silicon gate CMOS inverters is 15.7; however, with lateral diffusion accounted for, the Z/L ratio will be approximately 22. This compares with the mask designed Z/L ratio of 22 on the metal gate CMOS inverters, but with lateral diffusion the Z/L ratio is closer to 35. For both the silicon gate and metal gate CMOS inverters, the p^+ guardbands contact only the edge of the p-well nearest the p-channel MOS transistors.

The current gain of the npn transistors is largely determined by the p-well impurity profile. However, the spacing between the p-well and p^+ source (or drain) controls the lateral pnp current gain when the field-aiding factor is absent. Note that individual biasing of the lateral pnp does not provide for the current-induced electric field which would be present in latch-up situations. The FALT structures described in

Section B must be used to study the characteristics of the field-aiding.

G. Substrate Spreading Resistance Test Patterns (Device Structure 71)

An important parameter in characterizing latch-up is the V_{DD} contact-to-p-well resistance. Normally this is a spreading resistance which may be computed by various computer programs. Subchip A16 (Fig. 24) contains an array of 14 n^+ diffused regions measuring the substrate spreading resistance. Table VIII lists the dimensions for each of the 14 n^+ regions and the spacings between adjacent regions. This array of substrate spreading resistance structures can be used to test methods for computing the resistances between contacts. Table VIII summarizes the n^+ region spacings and contact sizes.

H. Square Array Collector Resistor (Device Structure 72)

A square array collector resistance structure (or four-probe bulk resistor) can be used to measure the substrate resistivity. Buehler and Thurber [11] have described the use of this structure and given equations for the computation of bulk resistivity. The square array collector resistor is located on subchip A15 (Fig. 25).

The bulk resistivity is determine from measurements on the square array collector resistor by forcing current between two adjacent contacts (e.g, pins 7 and 8) and measuring the voltage between the remaining adjacent contacts (e.g., pins 9 and 10). For the thick sample case, which is usually satisfied with non-epitaxial wafers, the resistivity is given by [11]

$$\rho = \frac{2\pi tV}{(2-\sqrt{2})I} = 10.73(t)\ \frac{V}{I} \quad , \qquad (4)$$

where t is the contact spacing ($t = 10^{-2}$ cm for device structure 72), V is the measured voltage difference, and I is the forced current. Therefore, for $t = 10^{-2}$ cm,

$$\rho = 0.1073\ \frac{V}{I}\ (\Omega - \text{cm}) \quad . \qquad (5)$$

For wafer thicknesses greater than 225 microns, equation (5) is accurate to within 10%. Buehler and Thurber should be consulted for the correction equation if greater accuracy is sought.

I. Gated Lateral PNP Transistors (Device Nos. 73-74)

Two gated lateral pnp transistors have been included on subchip A17 (see Fig. 26) to study surface effects on the lateral pnp transistors. Also, by applying lateral transistor theory [12-13], an approximate estimate to the substrate diffusion length may be obtained [14]. Both devices have 100 μm by 100 μm square emitters. The lateral base widths are 10 μm (device number 73) and 25 μm (device number 74). These are mask design base widths; with lateral diffusion included, the effective base widths are closer to being 5-6 μm (device number 73) and 20-21 μm (device number 74).

If the gates are biased for inversion, then these devices become p-channel MOS transistors. The effective Z/L ratios are approximately 85 (device number 73) and 22.5 (device number 74). Of course, the Z/L ratio is highly sensitive to drain voltage for these structures. Table IX gives the bonding pad assignment for these devices.

J. Kelvin Contact Resistors and van der Pauw Structures (Device Nos. 61-65 and 66-70)

These structures can be used to obtain information on the p-well sheet resistance, pinched p-well sheet resistance, n^+ and p^+ source/drain diffused sheet resistances, and p^+ guardband (silicon gate process) sheet resistance. Table II identifies the location and description of each of the Kelvin contact resistors and companion van der Pauw structures. The use of these structures have been described in the literature [15-18].

The Kelvin contact resistors are six square structures. The sheet resistance is measured by passing a current between the outer contacts and measuring the voltage developed between the inner contacts. If I represents the current flowing between the outer contacts, and V is the potential difference measured between the inner contacts, the sheet resistance is calculated by

$$R_{\Box} = 0.1667 \frac{V}{I} \quad . \tag{6}$$

Of course, the voltage should be measured with a voltmeter with input resistance much greater than the resistance between the inner contacts. Small currents should be used to avoid nonlinear effects.

The van der Pauw test structures (offset quadrate crosses) are used to compute sheet resistance in an analogous manner. These structures possess four-fold rotational symmetry, therefore, a simplified measurement scheme may be used. Current I is forced between two adjacent contacts, while the potential difference V is measured between the remaining two adjacent contacts. The sheet resistance is given by

$$R_{\Box} = \frac{\pi}{\ell n(2)} \cdot \frac{V}{I} = 4.532 \frac{V}{I} \quad . \tag{7}$$

The Kelvin contact resistors and van der Pauw structures have been paired to give dual readings for each of the five sheet resistances.

The test structures for the p-well sheet resistance appear on subchips A9 (Fig. 18) and A10 (Fig. 19), pinched p-well sheet resistance on A11 (Fig. 20) and A12 (Fig. 21), p^+ and n^+ source/drain sheet resistances on A18 (Fig. 27), and p^+ guardband sheet resistance on A20 (Fig. 29).

K. MOS Capacitors (Device Nos. 76-80)

MOS capacitors for the n-type substrate (both thin and thick oxide), n^+ diffused layer, and p-well are included on subchips A9 (thin oxide substrate), A15 (thick field substrate and large p-well), and A20 (n^+ and thick field substrate). Table II summarizes additional pertinent information for these five MOS capacitors. In addition, subchip SDL TC-1 includes two large MOS capacitors (p-well and thin oxide substrate).

C-V measurements are commonly made on MOS capacitors to obtain information on average surface concentration, surface state density (N_{ss}), and generation lifetime (τ).

(a) High frequency C-V plotting procedures are well known [19-20]. Let C_{ox} be the measured MOS capacitance in accumulation, and C_{min} be the measured high frequency (1 MHz) minimum capacitance in strong inversion. In strong inversion, the depletion width in the silicon is [19]

$$X_{dmax} = \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \left(\frac{C_{ox}}{C_{min}} - 1 \right) , \qquad (8)$$

where t_{ox} is the oxide thickness, ε_{si} is the silicon dielectric constant, and ε_{ox} is the oxide dielectric constant. The average doping density, denoted by N, is related to X_{dmax} by

$$X_{dmax} = \sqrt{\frac{4\varepsilon_{si} kT \ell n(N/n_i)}{q^2 N}} , \qquad (9)$$

where n_i is the intrinsic carrier concentration, k is Boltzmann's constant (1.38×10^{-23} joule/K), T is the temperature in degrees Kelvin, and q is the electronic charge (1.602×10^{-19} coulomb). Equations (8) and (9) may be solved by iteration for impurity concentration N. Curves are available for graphical solution, such as those presented by Goetzberger [21].

(b) A commonly used method to obtain the surface state density, denoted by N_{ss}, is the quasi-static C-V technique by Kuhn [22]. The quasi-static technique requires the measurement of the MOS displacement current in response to a linear voltage ramp. The interface surface state density is computed by

$$N_{ss} = \frac{C_{ox}}{q}\left[\frac{\dfrac{C_{LFm}}{C_{ox}}}{1 - \dfrac{C_{LFm}}{C_{ox}}} - \frac{C_{si}}{C_{ox}}\right] , \qquad (10)$$

where C_{ox} was defined above, C_{LFm} is the low-frequency capacitance minimum on the quasi-static C-V plot, and C_{si} is the theoretical minimum capacitance associated with the maximum depletion layer formed in strong inversion. The quantity (C_{si}/C_{ox}) is given by

$$\frac{C_{si}}{C_{ox}} = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{\frac{q^2 \varepsilon_{si} N}{4kT\ell n(N/n_i)}} , \qquad (11)$$

where all symbols have been defined above. In addition, C_{ox} is computed by

$$C_{ox} = \frac{\varepsilon_{si}}{t_{ox}} , \qquad (12)$$

and

$$n_i = 3.93 \times 10^{16}(T)^{1.5}\exp(-7010.43/T) \quad , \qquad (13)$$

where T is in units of degrees Kelvin. The correct units for N_{ss} are number per square centimeter per electron volt. A graphical solution for N_{ss} can be obtained upon knowing N, t_{ox}, and the ratio (C_{LFm}/C_{ox}) at T = 300 K. The required curves, along with detailed explanation, appear in Van Overstraeten, et. al. [23].

(c) The generation lifetime may be estimated from measurement of the relaxation time of the inversion layer in an MOS capacitor. This is accomplished by pulsing an MOS capacitor from the accumulated state into the deep depleted state, while the high-frequency capacitance is monitored. The fast pulse establishes a depletion region of a depth greater than the equilibrium value (X_{dmax}). As time proceeds, the inversion layer forms and the depletion depth progressively decreases to its equilibrium value. The initial condition, immediately following the application of the pulse, is termed deep depletion. The inversion layer formation is due to the generation of electron-hole pairs in the depletion region, one carrier type being swept to the surface (interface) and the other to the bulk. From Shockley-Read-Hall theory, the generation rate is [20]

$$G = \frac{n_i}{2\tau} \quad , \qquad (14)$$

where τ is the minority carrier lifetime. Given that

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{si}} \quad , \qquad (15)$$

it can be shown that

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \left[\frac{C_{min}}{C} - 1\right]\frac{2n_i C_{ox}}{C_{min}\tau N} \quad , \qquad (16)$$

where all symbols have been previously defined. Plotting $d((C_{ox}/C)^2)/dt$ versus $((C_{min}/C) - 1)$ yields a straight line whose slope is related to lifetime.

Examining C-time curves by the above method requires considerable data reduction. Often the C-time relaxation curve can be fitted reasonably well by a straight line over most of the decay. Let t_F represent the total time of the C-time relaxation, then

$$C(t) \cong C_{initial} + (C_{min} - C_{initial})\frac{t}{t_F} \quad , \qquad (17)$$

where t is time and $C_{initial}$ is the initial capacitance of the pulsed MOS capacitor. The lifetime, denoted by τ, may then be obtained from [24]

$$\tau = \frac{n_i}{8N}\frac{C_{min}}{C_{ox}} t_F \left(1 + \frac{C_{initial}}{C_{min}}\right)^2 \quad . \qquad (18)$$

This expression neglects surface generation (τ is due to bulk generation) and, of course, light must not be allowed to fall on the sample during the measurement.

L. P^+N Junction Diodes (Device Nos. 81-85)

P^+N junction diodes are contained on subchips A19 (Fig. 28) and A20 (Fig. 29) for measuring junction leakage currents. The primary reason for the inclusion of p^+n diodes is to study leakage current of gold doped junctions (relate to the use of gold doping to control latch-up in CMOS [25]). Subchip A19 contains three p^+n diodes of varying area and perimeter. This allows an analysis of the leakage current in terms of areal and peripheral leakage components. Two small, identical p^+n diodes are placed near the n^+ contact of the MOS capacitor (device number 79) on subchip A20.

The three major components of leakage current were discussed in section C (gated diodes). Equations (1) through (3) are the relevant equations. However, from practical considerations, it is often more convenient for prediction purposes to express the leakage current in terms of areal and peripheral components. These components may be resolved by comparing diode leakage currents for diodes of different area and perimeter. For example, taking devices #81 (area = 45 $mils^2$, and perimeter = 49 mils) and #82 (area = 45 $mils^2$, and perimeter = 28 mils), a plot of the measured leakage currents versus perimeter provides an estimate of the areal and peripheral leakage components. The slope gives the peripheral component, whereas, the intercept at perimeter = 0 gives the areal component. Other diode combinations may be used, with appropriate scaling, to provide additional data for the resolution of areal and peripheral components. Table II summarizes all necessary data on the p^+n junction diodes.

M. Contact Resistance Test Pattern (Device No. 28)

A p^+ region-to-metal (Aℓ) contact resistance test pattern is located on subchip A4 (Fig. 12). This is a Kelvin contact

structure in which current I is passed between two adjacent bonding pads (e.g., pins 8 and 9, or 10 and 11), while the potential difference V is measured between the remaining two adjacent bonding pads (e.g., pins 10 and 11, or 8 and 9). The contact resistance per unit area is computed by

$$R_c = 0.01 \frac{V}{I} \ (\text{ohms}/\mu\text{m}^2) \quad . \tag{19}$$

This equation is derived from the fact that the contact is 10 μm by 10 μm.

N. Thick Field MOS Transistors (Device Nos. 24 and 25)

Subchip A3 (Fig. 10) contains two thick field oxide MOS test transistors. Both are p-channel devices. During the silicon gate processing, both silicon gate (device No. 25) and metal gate (device No. 24) MOS transistors result. The effective Z/L ratio of the metal gate MOS transistor is 12, whereas, the effective Z/L ratio of the silicon gate MOS transistor is 6.5 (lateral diffusion effects are accounted for).

O. Vertical NPN Transistor (Device No. 75)

A separate p-well base npn vertical bipolar transistor is available on subchip A17 (Fig. 26). This transistor corresponds to the parasitic npn transistor in LATUS structure No. 38, however, no guardband diffusion is included. The emitter is 78 μm by 206 μm. Pin locations are given in Table II.

F. Miscellaneous Structures

A resolution pattern appears on subchip A4 (device No. 86) for all 12 levels (see Fig. 12). It consists of a series of rectangles and squares (dimensions detailed in Table II).

Finally, crosses have been included for alignment patterns. Metal gate process alignment patterns appear on subchips SDL TC-2 and TC-3, A4, A15, and A19. Silicon gate process alignment patterns appear on subchips A3 and A12.

SECTION IV - SUMMARY

This report has described a test chip for CMOS latch-up and radiation effects research. In addition, numerous test structures on the LURIC test chip can function as process monitoring and control devices. Both metal gate and silicon gate (ELA) processes are possible using the twelve layer mask set.

Six basic categories of test devices and related test structures have been described.

(1) CD4007 metal gate CMOS integrated circuit
(2) ELA silicon gate CMOS cells
(3) Field-aided lateral transistors (FALT structures)
(4) Substrate spreading resistance test structures
(5) Latch-up structures (LATUS devices)
(6) Support test structures (e.g., MOS capacitors, gated diodes, $p^{+}n$ diodes, van der Pauw and Kelvin contact resistors, MOS test transistors, etc.)

The use of each category of test structures has been discussed, with equations given where pertinent.

SECTION V - ACKNOWLEDGMENTS

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REFERENCES

[1] C. E. Barnes, et. al., "Latch-up Prevention in CMOS," Sandia Laboratories Technical Report SAND76-0048, Albuquerque, New Mexico, March, 1976.

[2] B. L. Gregory and B. D. Shafer, "Latch-up in CMOS Integrated Circuits," IEEE Trans. Nuclear Science, NS-20, pp. 293-299, December, 1973.

[3] B. D. Shafer, "CMOS Latch-up Analysis and Prevention," Sandia Laboratories Technical Report SAND75-0371, Albuquerque, New Mexico, June, 1975.

[4] D. B. Estreich, unpublished notes.

[5] S. K. Ghandhi, The Theory and Practice of Microelectronics, J. Wiley & Sons, Inc., New York, 1968.

[6] D. B. Estreich, "Latch-up in CMOS Integrated Circuits," contributed to Computer-Aided Engineering of Semiconductor Integrated Circuits, prepared by J. D. Meindl, et al., Stanford Electronics Laboratories Report SEL78-011 (TR 4969-3), Stanford University, pp. 218-239, February, 1978.

[7] D. B. Estreich (to be published).

[8] A. S. Grove, Physics and Technology of Semiconductor Devices, J. Wiley & Sons, Inc., New York, 1967, pp. 264-271, pp. 290-305.

[9] D. J. Fitzgerald and A. S. Grove, "Surface Recombination in Semiconductors, " Surface Science, Vol. 9, pp. 347-369, 1968.

[10] R. S. Flores, "Preliminary Analysis of the ELA Silicon Gate Cell Family," Sandia Laboratories Report SAND77-4011, Albuquerque, New Mexico, November 29, 1977.

[11] M. G. Buehler and W. R. Thurber, "A Planar Four-Probe Test Structure for Measuring Bulk Resistivity," IEEE Trans. Elec. Dev., ED-23, pp. 968-974, August, 1976.

[12] J. Lindmayer and W. Schneider, "Theory of Lateral Transistors," Solid-State Electronics, 10, pp. 225-234, 1967.

[13] S. Chou, "An Investigation of Lateral Transistors - D. C. Characteristics," Solid-State Electronics, 14, pp. 811-826, 1971.

[14] D. B. Estreich (to be published).

[15] M. G. Buehler and D. E. Sawyer, "Microelectric Test Patterns Aid Production of Custom IC's," Circuit Manufacturing, pp. 46-56, February, 1977.

[16] L. J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," Philips Res. Rpt., 13, pp. 1-9, 1958.

[17] M. G. Buehler, Semiconductor Measurement Technology: Microelectronic Test Patterns (An Overview), NBS Spec. Publ. 400-6, August, 1974.

[18] H. A. Schafft (ed.), Semiconductor Measurement Technology ARPA/NBS Workshop Test Patterns for Integrated Circuits, NBS Spec. Publ. 400-15, 1976.

[19] S. M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, New York, 1969; see Chapter 9.

[20] A. S. Grove, Physics and Technology of Semiconductor Devices, J. Wiley and Sons, Inc., New York, 1967.

[21] A. Goetzberger, "Ideal MOS Curves for Silicon," Bell System Technical Journal, 45, 1097, 1966.

[22] M. Kuhn, "A Quasi-Static Technique for MOS C-V and Surface State Measurements," Solid-State Electronics, 13, pp. 873-885, 1970.

[23] R. Van Overstraeten, G. Declerck, and G. Broux, "Graphical Technique to Determine the Density of Surface States at the Si-SiO_2 Interface of MOS Devices Using the Quasi-static C-V Method," J. Electrochem. Soc., 120, pp. 1785-1787, December, 1973.

[24] D. K. Schroder, and J. Guldberg, "Interpretation of Surface and Bulk Effects Using the Pulsed MIS Capacitor," Solid-State Electron, 14, pp. 1285-1297, 1971.

[25] W. R. Dawes, Jr. and G. F. Derbenwick, "Prevention of CMOS Latch-up by Gold Doping," IEEE Trans. Nuclear Science, NS-23, pp. 2027-2030, December, 1976.

TABLE I

DEFINITION OF MASK LEVELS FOR LURIC TEST CHIP

Mask Level	Description	Metal Gate	Si Gate
1	P-well Implant	X	X
2	P^+ Guardband Implant		X
3	Thin Oxide Definition		X
4	Polysilicon Definition*		X
5	N^+ S/D Implant		X
6	P^+ S/D Implant		X
7	P^+ S/D Diffusion	X	
8	N^+ S/D Diffusion	X	
9	Thin Oxide Definition	X	
10	Contact Definition	X	X
11	Metalization Definition*	X	X
12	Protection Layer Definition	X	X

*Mask levels 4 and 11 are dark field; all others are clear field.

TABLE II

LIST OF ALL DEVICES AND TEST PATTERNS

No.	Description	Metal Gate	Si Gate	Location	Comments
1	4007 CMOS Dual Complementary Pair plus Inverter IC	X		TC-3 (Fig. 6)	Replica of RCA CD4007 Layout (pins 1 - 14)
2	Individual P-channel MOS transistor (Z = 20.4 mils, L = 0.3 mils)	X		TC-4 (Fig. 7)	Identical to MOS transistor on CD4007 IC (pins 11, 12, 13, & 14)
3	Individual P-channel MOS transistor with shorted source-to-substrate (Z = 20.4 mils, L = 0.3 mils)	X		TC-4 (Fig. 7)	Matches structure No. 2 above except for shorted source-to-substrate (pins 1, 2, 3, & 14)
4	Individual N-channel MOS transistor (Z = 9.31 mils, L = 0.3 mils)	X		TC-4 (Fig. 7)	Identical to MOS transistor on CD4007 IC (pins 7, 8, 9, & 10)
5	Individual N-channel MOS transistor with shorted source-to-p-well (Z = 9.31 mils, L = 0.3 mils)	X		TC-4 (Fig. 7)	Matches structure No. 4 above except for shorted source-to-p-well (pins 4, 5, & 6)
6	SCR	X		TC-1 (Fig. 4)	(pins 7, 8, 9, & 10)
7	P-well MOS Capacitor (A = 106.1 $mils^2$)	X		TC-1 (Fig. 4)	(pins 4 & 5)
8	N-substrate MOS capacitor (A = 106.1 $mils^2$)	X		TC-1 (Fig. 4)	(pins 6 & 7)
9	N-channel gate oxide MOS transistor (Z = 2.0 mils, L = 0.3 mils)	X		TC-1 (Fig. 4)	Standard test MOS transistor (pins 1, 2, 3, & 14)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
10	N-channel field oxide MOS transistor (Z = 2.0 mils, L = 0.3 mils)	X		TC-1 (Fig. 4)	Standard test MOS transistor (pins internal)
11	P-channel gate oxide MOS transistor (Z = 2.0 mils, L = 0.3 mils)	X		TC-1 (Fig. 4)	Standard test MOS transistor (pins 7, 11, 12, & 13)
12	P-channel field oxide MOS transistor (Z = 2.0 mils, L = 0.3 mils)	X		TC-1 (Fig. 4)	Standard test MOS transistors (pins internal)
13	4007 CMOS IC with modified metalization (No gate connections and can disconnect gate protection diodes)	X		TC-2 (Fig. 5)	Compare with structure No. 1 listed above (pins 1 - 14)
14	Field-aided lateral PNP transistor I (W_b = 10 μm, W_e = 150 μm, W_c = 150 μm)	X	X	A1 (Fig. 8)	Standard FALT structure (pins 4, 5, 7, & 10; optional 3)
15	Field-aided lateral PNP transistor II (W_b = 20 μm, W_e = 150 μm, W_c = 150 μm)	X	X	A1 (Fig. 8)	(pins 7, 8, 9, & 10; optional 3)
16	Field-aided lateral PNP transistor III (W_b = 40 μm, W_e = 150 μm, W_c = 150 μm)	X	X	A1 (Fig. 8)	(pins 1, 2, 3, & 13; optional 10)
17	Field-aided lateral PNP transistor IV (W_b = 10 μm, W_e = 30 μm, W_c = 150 μm)	X	X	A1 (Fig. 8)	Emitter width is 0.20 of collector width (pins 3, 11, 12, 13; optional 10)
18	Field-aided lateral PNP transistor V (W_b = 10 μm, W_e = 30 μm and 150 μm, W_c = 150 μm)	X	X	A2 (Fig. 9)	T-shaped emitter (pins 1, 2, 3, & 13; optional 10)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
19	Field-aided lateral PNP transistor VI (W_b = 10 μm, W_e = 30 μm on all three P^+ regions, $W_c = W_e$)	X	X	A2 (Fig. 9)	Triple P^+ regions for three combinations of emitter and collector (pins 4, 5, 6, 7, & 10; optional 3)
20	Field-aided lateral PNP transistors VII (W_b = 40 μm, W_e = 150 μm, W_c = 150 μm)	X	X	A2 (Fig. 9)	P-well diffusion for collector and P^+ diffusion for emitter (pins 7, 8, 9, & 10; optional 3)
21	Field-aided lateral PNP transistor VIII (W_b = 20 μm, W_e = 150 μm, W_c = 150 μm)	X	X	A2 (Fig. 9)	P-well diffusion for collector and P^+ diffusion for emitter (pins 3, 11, 12, & 13; optional 10)
22	Field-aided lateral PNP transistor IX (W_b = 20 μm, W_e = 100 μm, W_c = 100 μm)	X	X	A3 (Fig. 10)	N^+ diffused rail between emitter and collector of 10 μm width (pins 3, 4, 5 & 7)
23	Field-aided lateral PNP transistor X (W_b = 20 μm, W_e = 100 μm, W_c = 100 μm)	X	X	A3 (Fig. 10)	Gate over lateral base region (pins 3, 7, 8, 9, & 10)
24	Metal-gate P-channel MOS transistor (Z = 70 μm, L = 10 μm)	X	X	A3 (Fig. 10)	(pins 1, 2, 3, & 14)
25	Silicon-gate P-channel MOS transistor (Z = 70 μm, L = 15 μm)		X	A3 (Fig. 10)	(pins 3, 11, 12, & 13)
26	P^+N gated diode (diode area ≈3.0 mils², and gate area = 106.1 mils²)	X	X	A4 (Fig. 12)	(pins 1, 2, & 14)
27	N^+P gated diode (diode area ≈3.0 mils², and gate area = 106.1 mils²)	X	X	A4 (Fig. 12)	(pins 3, 4, & 5)
28	P^+-to-metal contact resistor (10 μm by 10 μm contact)	X	X	A4 (Fig. 12)	(pins 8, 9 or 10, & 11)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
29	Latch-up structure I (W_b = 20 µm, L_{RS} = 39 µm, and L_{RP} = 48 µm)	X	X	A5 (Fig. 13)	(pins 1, 2, 3, & 14)
30	Latch-up structure II (W_b = 10 µm, L_{RS} = 39 µm, and L_{RP} = 48 µm)	X	X	A5 (Fig. 13)	Reference cell (pins 3, 4, 5, & 6)
31	Latch-up structure III (W_b = 10 µm, L_{RS} = 39 µm, and L_{RP} = 35 µm)	X	X	A5 (Fig. 13)	(pins 7, 8, 9, & 10)
32	Latch-up structure IV (W_b = 10 µm, L_{RS} = 39 µm, and L_{RP} = 61 µm)	X	X	A5 (Fig. 13)	(pins 10, 11, 12, & 13)
33	Latch-up structure V (W_b = 10 µm, L_{RS} = 39 µm, and L_{RP} = 22 µm)	X	X	A6 (Fig. 14)	(pins 1, 2, 3, & 14)
34	Latch-up structure VI (W_b = 60 µm, L_{RS} = 39 µm, and L_{RP} = 22 µm)	X	X	A6 (Fig. 14)	(pins 3, 4, 5, & 6)
35	Latch-up structure VII (W_b = 30 µm, L_{RS} = 39 µm, and L_{RP} = 48 µm)	X	X	A6 (Fig. 14)	(pins 7, 8, 9, & 10)
36	Latch-up structure VIII (W_b = 40 µm, L_{RS} = 39 µm, and L_{RP} = 48 µm)	X	X	A6 (Fig. 14)	(pins 10, 11, 12, & 13)
37	Latch-up structure IX (W_b = 10 µm, L_{RS} = 39 µm, and L_{RP} = 48 µm)	X	X	A7 (Fig. 15)	Full guardband (pins 1, 2, 3, & 14) (Note: Compare to structure No. 30)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
38	Latch-up structure X (W_b = 10 μm, L_{RS} = 39 μm, and L_{RP} = 87 μm)	X	X	A7 (Fig. 15)	(pins 3, 4, 5, & 6)
39	Latch-up structure XI (W_b = 10 μm, L_{RS} = 22 μm, and L_{RP} = 48 μm)	X	X	A7 (Fig. 15)	(pins 7, 8, 9, & 10)
40	Latch-up structure XII (W_b = 10 μm, L_{RS} = 89 μm, and L_{RP} = 48 μm)	X	X	A7 (Fig. 15)	(pins 10, 11, 12, & 13)
41	Latch-up structure XIII (W_b = 40 μm, L_{RS} = 39 μm, and L_{RP} = 87 μm)	X	X	A8 (Fig. 16)	Narrow N^+ region (pins 1, 2, 3, & 14)
42	Latch-up structure IXV (W_b = 20 μm, L_{RS} = 39 μm, and L_{RP} = 87 μm)	X	X	A8 (Fig. 16)	Narrow N^+ region (pins 3, 4, 5, & 6)
43	Latch-up structure XV (W_b = 10 μm, L_{RS} = 39 μm, and L_{RP} = 87 μm)	X	X	A8 (Fig. 16)	Narrow N^+ region (pins 7, 8, 9, & 10)
44	Latch-up structure XVI (W_b = 10 μm, L_{RS} = 39 μm, and L_{RP} = 87 μm)	X	X	A8 (Fig. 16)	Full guardband (pins 10, 11, 12, & 13) (Note: Compare structure No. 38)
45	ELA P-well resistance structure (double V_{SS} contact - 6 μm gates)		X	A9 (Fig. 18)	Without polysilicon gates and with extended guardband (pins 4 and 5)
46	ELA P-well resistance structure (double V_{SS} contact - 6 μm gates)		X	A9 (Fig. 18)	Without polysilicon gates and with tight guardband (pins 6 and 7)
47	ELA P-well resistance structure (double V_{SS} contact - 6 μm gates)		X	A9 (Fig. 18)	With polysilicon gates and with extended guardband (pins 8, 9, & 10)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
48	ELA P-well resistance structure (double V_{SS} contact - 6 µm gates)		X	A9 (Fig. 18)	With polysilicon gates and with tight guardband (pins 11, 12, & 13)
49	ELA P-well resistance structure (single V_{SS} contact - 6 µm gates)		X	A10 Fig. 19)	Without polysilicon gates and with extended guardband (pins 4 and 5)
50	ELA P-well resistance structure (single V_{SS} contact - 6 µm gates)		X	A10 (Fig. 19)	Without polysilicon gates and with tight guardband (pins 6 and 7)
51	ELA P-well resistance structure (single V_{SS} contact - 6 µm gates)		X	A10 (Fig. 19)	With polysilicon gates and with extended guardband (pins 8, 9, & 10)
52	ELA P-well resistance structure (single V_{SS} contact - 6 µm gates)		X	A10 (Fig. 19)	With polysilicon gates and with tight guardband (pins 11, 12, & 13)
53	ELA P-well resistance structure (single V_{SS} contact - 4 µm gates)		X	A11 (Fig. 20)	With polysilicon gates and with tight guardband (pins 3, 4, & 5)
54	ELA Asynchronous 1470/ Reset		X	A11 (Fig. 20)	(pins 6 to 13)
55	ELA 2-input OR gate		X	A12 (Fig. 21)	With V_{SS} strap across P-well (pins 2, 7, 8, 9, 12 & 13)
56	ELA 2-input OR gate		X	A12 (Fig. 21)	Without V_{SS} strap across P-well (pins 1, 10, 11, 12, 13, and 14)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
57	Polysilicon gate CMOS inverter I (Z = 220 μm, L = 14 μm)		X	A13 (Fig. 22)	15 μm separation between transistors (pins 4 to 10)
58	Polysilicon gate CMOS inverter II (Z = 220 μm, L = 14 μm)		X	A13 (Fig. 22)	25 μm separation between transistors (pins 1, 2, 3, 11, 12, 13, and 14)
59	Metal-gate CMOS inverter I (Z = 220 μm, L = 10 μm)	X		A14 (Fig. 23)	15 μm separation between transistors (pins 1, 2, 3, 11, 12, 13, and 14)
60	Metal-gate CMOS inverter II (Z = 220 μm, L = 10 μm)	X		A14 (Fig. 23)	25 μm separation between transistors (pins 4 to 10)
61	Kelvin contact resistor (6 square resistor)	X	X	A9 (Fig. 18)	P-well sheet resistance (pins 1, 2, 3, & 14)
62	Kelvin contact resistor (6 square resistor)	X	X	A11 (Fig. 20)	Pinched P-well sheet resistance (pins 1, 2, 3, & 14)
63	Kelvin contact resistor (6 square resistor)	X	X	A18 (Fig. 27)	P^+ S/D sheet resistance (pins 7, 8, 9, & 10)
64	Kelvin contact resistor (6 square resistor)	X	X	A18 (Fig. 27)	N^+ S/D sheet resistance (pins 1, 2, 3, & 14)
65	Kelvin contact resistor (6 square resistor)	X	X	A20 (Fig. 29)	P^+ guardband sheet resistance (pins 7, 8, 9, & 10)
66	Van der Pauw structure	X	X	A10 (Fig. 19)	P-well sheet resistance (pins 1, 2, 3, & 14)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
67	Van der Pauw structure	X	X	A12 (Fig. 21)	Pinched P-well sheet resistance (pins 3, 4, 5, & 6)
68	Van der Pauw structure	X	X	A18 (Fig. 27)	P^+ S/D sheet resistance (pins 10, 11, 12, & 13)
69	Van der Pauw structure	X	X	A18 (Fig. 27)	N^+ S/D sheet resistance (pins 3, 4, 5, & 6)
70	Van der Pauw structure	X	X	A20 (Fig. 29)	P^+ guardband sheet resistance (pins 11, 12, 13, & 14)
71	Substrate resistance pattern (see text)	X	X	A16 (Fig. 24)	Twelve resistance paths included (pins 1 to 14)
72	Square array collector resistor (100 μm square layout)	X	X	A15 (Fig. 25)	(pins 7, 8, 9, & 10)
73	Gated lateral PNP (or MOS) transistor I (W_b = 10 μm)	X	X	A17 (Fig. 26)	(pins 1, 2, 3, & 14)
74	Gated lateral PNP (or MOS) transistor II (W_b = 25 μm)	X	X	A17 (Fig. 26)	(pins 7, 8, 9, & 10)
75	P-well NPN transistor	X	X	A17 (Fig. 26)	(pins 12, 13, 14)
76	Thin oxide substrate MOS capacitor (area = 62 mils^2)	X	X	A9 (Fig. 18)	(pins: internal)
77	Thick field oxide MOS substrate capacitor I (area = 133 mils^2)	X	X	A15 (Fig. 25)	(pins: internal)

TABLE II
(Continued)

No.	Description	Metal Gate	Si Gate	Location	Comments
78	P-well MOS capacitor (area = 210 mils^2)	X	X	A15 (Fig. 25)	(pins 3 and 14)
79	N^+ MOS capacitor (area = 56 mils^2)	X	X	A20 (Fig. 29)	(pins 4 and 6)
80	Thick field oxide MOS substrate capacitor II (area = 66 mils^2)	X	X	A20 (Fig. 29)	(pins 4 and internal)
81	P^+N diode I (area = 45 mils^2, and perimeter = 49 mils)	X	X	A19 (Fig. 28)	(pins 6 or 7, and 14)
82	P^+N diode II (area = 45 mils^2, and perimeter = 28 mils)	X	X	A19 (Fig. 28)	(pins 3 and 14)
83	P^+N diode III (area = 120 mils^2, and perimeter = 104 mils)	X	X	A19 (Fig. 28)	(pins 11 and 14)
84	P^+N diode IV (area = 2.25 mils^2, and perimeter = 6 mils)	X	X	A20 (Fig. 29)	(pins 2 and 4)
85	P^+N diode V (area = 2.25 mils^2, and perimeter = 6 mils)	X	X	A20 (Fig. 29)	(pins 3 and 4)
86	Resolution pattern (all levels included)	X	X	A4 (Fig. 12)	8 µm x 8 µm, 6 µm x 6 µm, 4 µm x 4 µm with 10 µm x 30 µm to 2 µm x 30 µm patterns (pins: none)

TABLE III

BONDING PAD CONNECTIONS BY REGION

(FALT Structures)

Contacted Region	Subchip A1	Subchip A2	Subchip A3
Bias Rails (base)	3 7 10 13	3 7 10 13	3 7
Emitters	2 4 9 11	2 4 9 11 (6)	4 10
Collectors	1 5 8 12	1 5 8 12 (6)	5 8
Gate			9

TABLE IV

PARAMETERS TO BE STUDIED BY FALT STRUCTURES

Structure Number	Parameter Varied	Parameters Constant
14,15, 16	Study W_b Variation	W_e, W_c
14,17	Study W_e Variation	W_b, W_c
17,19	Study W_c Variation	W_e, W_b
20,21	Study collector depth (p-well diffusion) Compare to 16 - 15, respectively	W_e, W_c
18	Study emitter shape (T-shaped emitter--compare to 14, 17, and 19)	
22	N^+ diffused region between emitter and collector	
23	Gate over base region; study surface recombination effects	

NOTE: Subchips A1 (Fig. 8), A2 (Fig. 9), and A3 (Fig. 10).

TABLE V

BONDING PAD CONNECTIONS BY REGION
(LATUS Test Patterns)

Structure Number	P-well Contact	N^+ Region in P-well	P^+ Region in Substrate	Substrate Contact
29	14	1	2	3
30	6	5	4	3
31	7	8	9	10
32	13	12	11	10
33	14	1	2	3
34	6	5	4	3
35	7	8	9	10
36	13	12	11	10
37	14	1	2	3
38	6	5	4	3
39	7	8	9	10
40	13	12	11	10
41	14	1	2	3
42	6	5	4	3
43	7	8	9	10
44	13	12	11	10

NOTE: Subchips A5 (Fig [illegible]), A6 (Fig. 14), A7 (Fig. 15), and A8 (Fig. 16).

TABLE VI

PARAMETER VARIATION OF LATUS STRUCTURES

Structure Number	Parameter Varied	Parameters Constant
29,30,35, 36	Study W_b variation for wide N^+ region and L_{RP} = 48 μm	L_{RS},L_{RP}
41,42,43	Study W_b variation for narrow N^+ region and L_{RP} = 87 μm	L_{RS},L_{RP}
33,34	Study W_b variation for wide N^+ region and L_{RP} = 22 μm	L_{RS},L_{RP}
30,31,32, 33	Study L_{RP} Variation	W_b,L_{RS}
37,38,40	Study L_{RS} Variation	W_b,L_{RP}
38 & 44, 30 & 37	Study tight guardband versus loose guardband	W_b, L_{RS},L_{RP}

NOTE: Subchips A5 (Fig. 13), A6 (Fig. 14), A7 (Fig. 15), and A8 (Fig. 16).

TABLE VII

ELA BONDING PAD CONFIGURATIONS

Block	Bonding Pad Configuration
1720 (with V_{SS} strap) (Subchip A12)	12 - V_{DD} and 13 - V_{SS} 2 - Y output ($\overline{X}$) 9 - X output 8 - B input 7 - A input
1720 (without V_{SS} strap) (Subchip A12)	12 - V_{DD} and 13 - V_{SS} 14 - Y output ($\overline{X}$) 11 - X output 1 - A input 10 - B input
1470 (Subchip A11)	8 - V_{DD} and 7 - V_{SS} 10 - $\overline{\text{Clock}}$ 6 - Clock 9 - data in 13 - reset 11 - Q output 12 - $\overline{Q}$ output

TABLE VIII

N^+ REGION SPACINGS FOR SUBSTRATE RESISTANCE TEST PATTERNS

Pad Number	Region Size	Spacing
1	18 x 18 µm	60 µm
2	90 x 18 µm	30 µm
3	90 x 18 µm	60 µm
4	90 x 18 µm	120 µm
5	90 x 18 µm	60 µm
6	78 x 18 µm	246 µm
7	90 x 18 µm	90 µm
8	270 x 18 µm	120 µm
9	270 x 18 µm	60 µm
10	270 x 18 µm	30 µm
11	270 x 18 µm	60 µm
12	18 x 18 µm	60 µm
13	18 x 18 µm	—
14	18 x 18 µm	

NOTE: Subchip A16 (Fig. 24).

TABLE IX

GATED LATERAL pnp TRANSISTOR CONFIGURATIONS

Device No.	Lateral pnp				p-chan MOS			
	E	C	G	B	S	D	G	Sub
75	2	1	3	14	1	2	3	14
76	8	10	9	7	10	8	9	7

NOTE: Subchip A17 (Fig. 26).

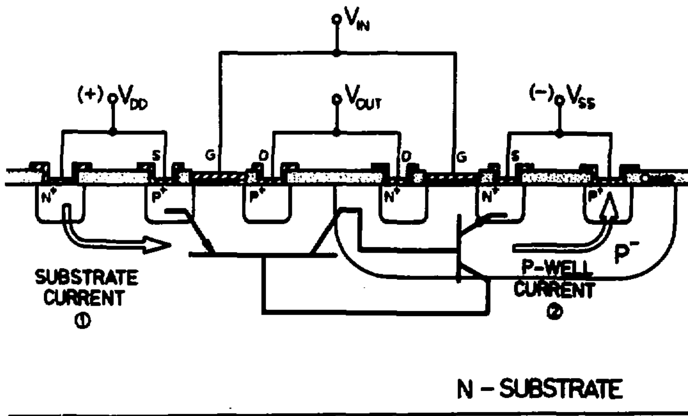
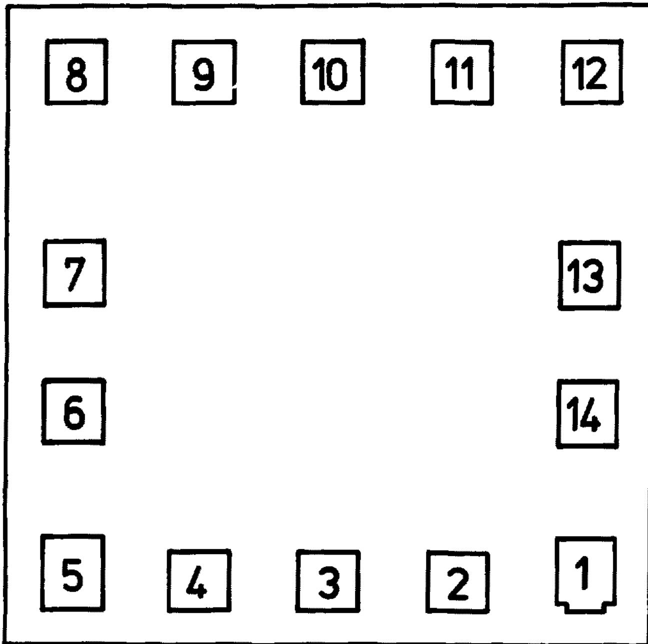


FIG. 1

Fig. 1 Cross-section of CMOS integrated circuit inverter along latch-up path.



BONDING PAD LOCATIONS

Fig. 2 Bonding pad configuration (14 pads) with pad numbering scheme as used in this report. Note: Numbers used in Table II.

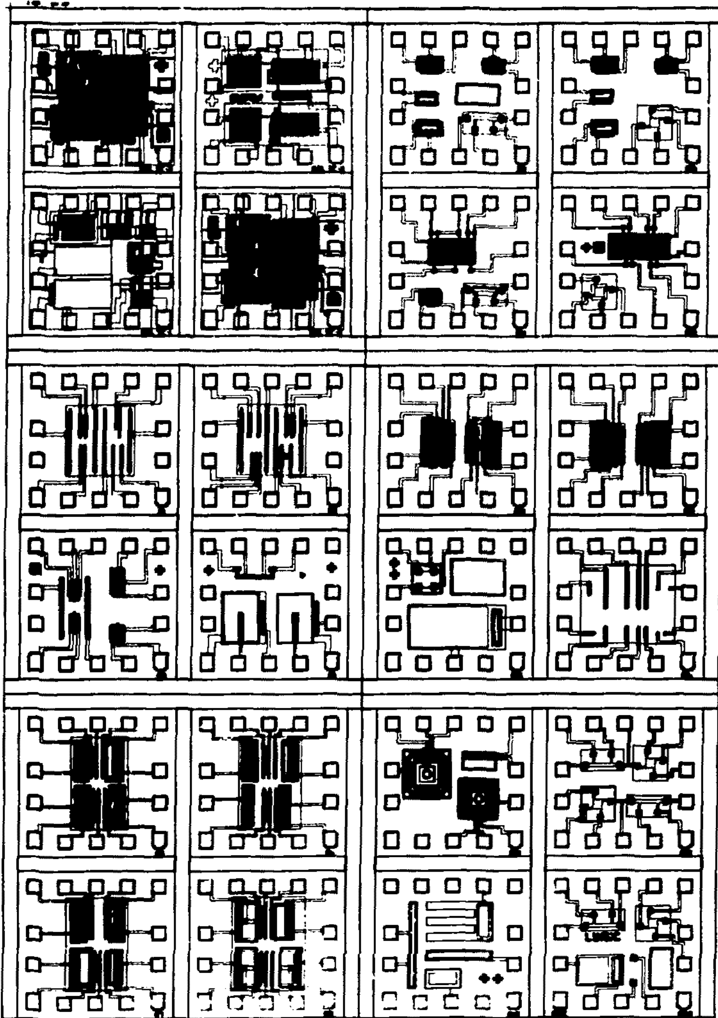


Fig. 3 Complete LURIC test chip showing relative locations of all 24 subchips.

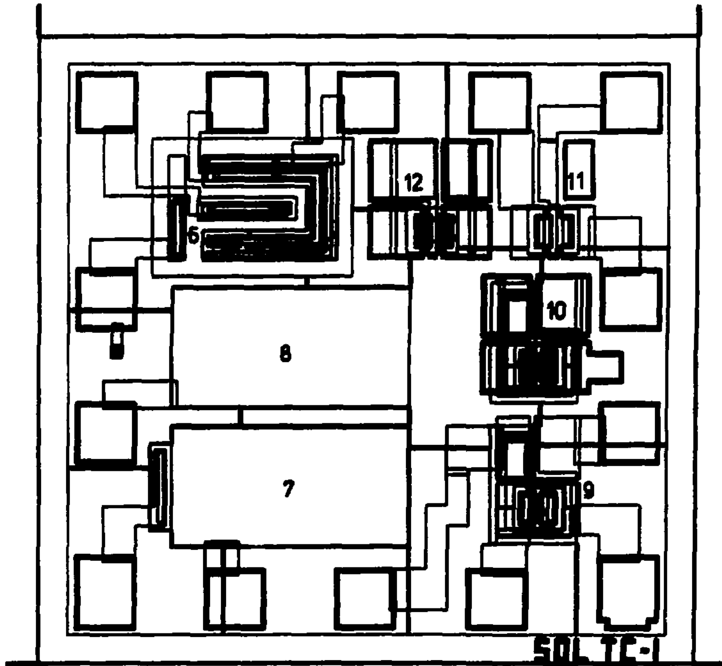


Fig. 4 SDL TC-1 - Subchip containing SCR, MOS test transistors, and MOS capacitors.

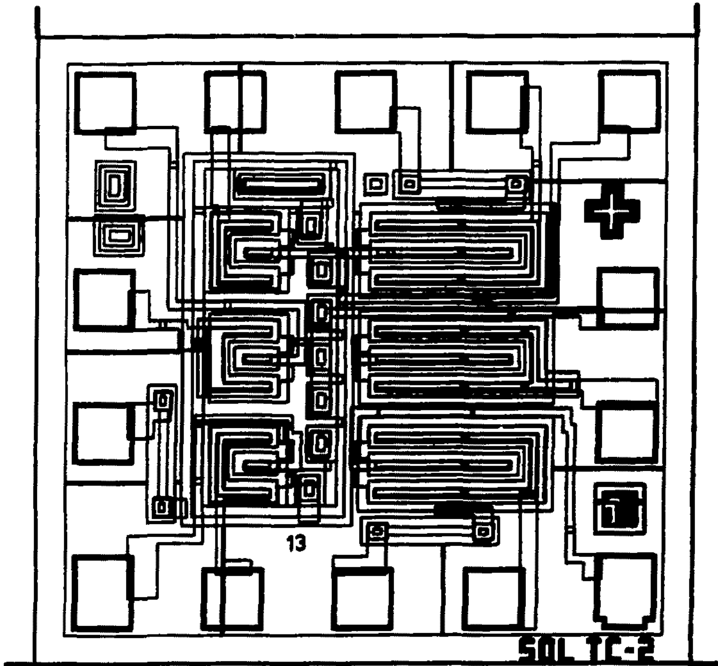


Fig. 5 SDL TC-2 - Subchip containing CD4007 CMOS IC with modified metalization (see text).

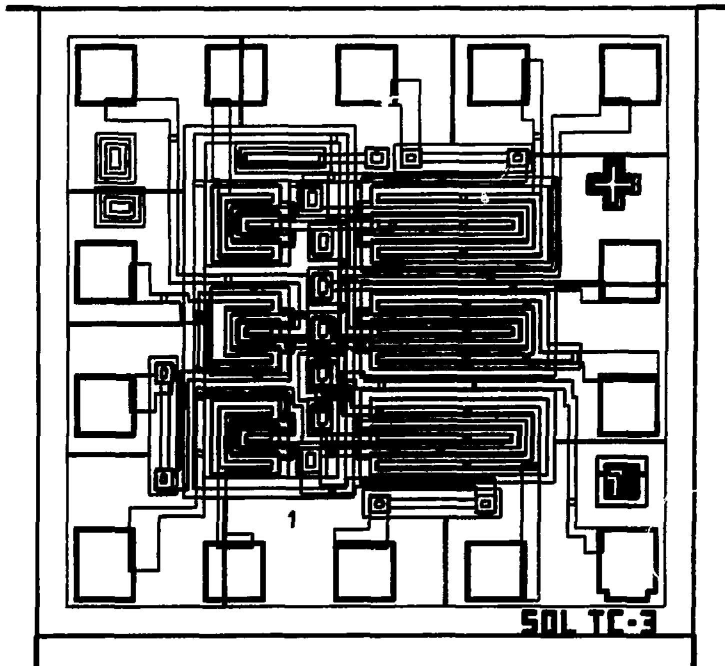


Fig. 6 SDL TC-3 - Subchip containing CD4007 CMOS dual complementary pair plus inverter.

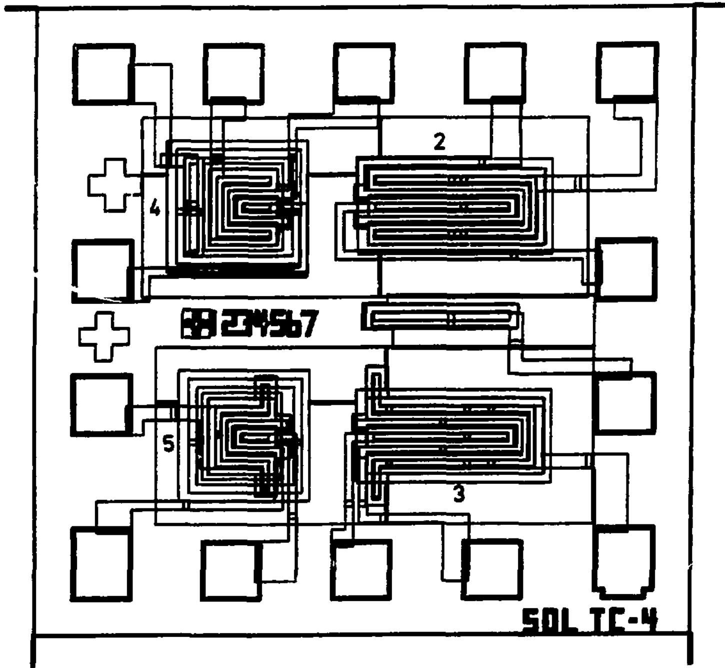


Fig. 7 SDL TC-4 - Subchip containing n-channel and p-channel MOS transistors (compare to MOS transistors on CD4007 CMOS IC's).

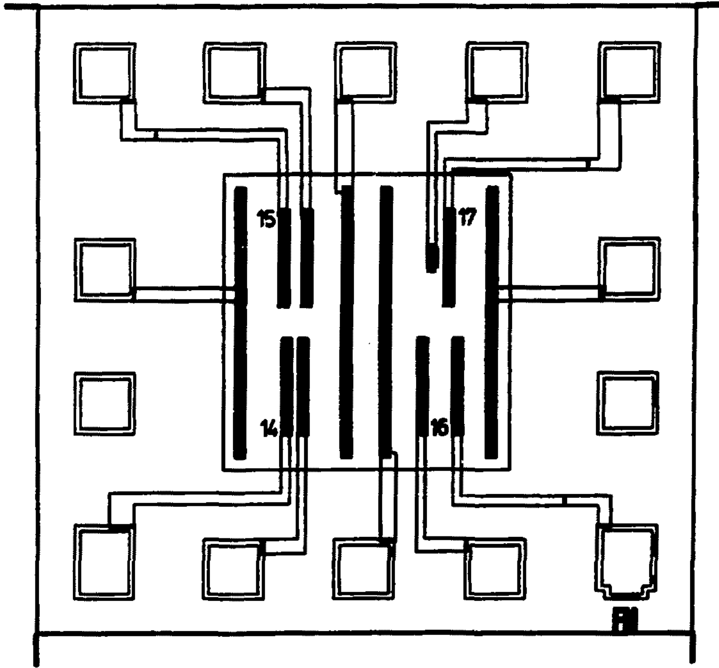


Fig. 8 Subchip A1 - Field-aided lateral transistors (FALT).

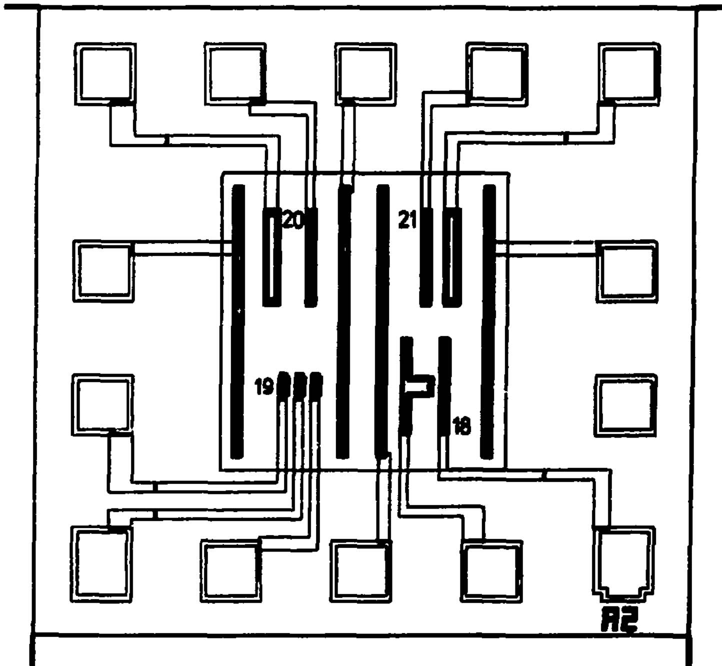


Fig. 9 Subchip A2 - Field-aided lateral transistors (FALT).

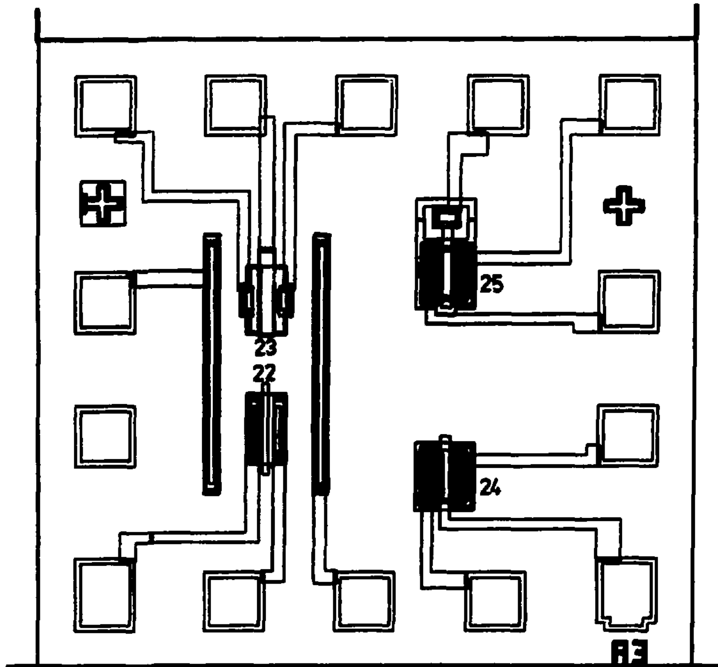


Fig. 10 Subchip A3 - Field-aided lateral transistors with n^+ bar and gate over base, and field oxide MOS transistors (both metal gate and silicon gate).

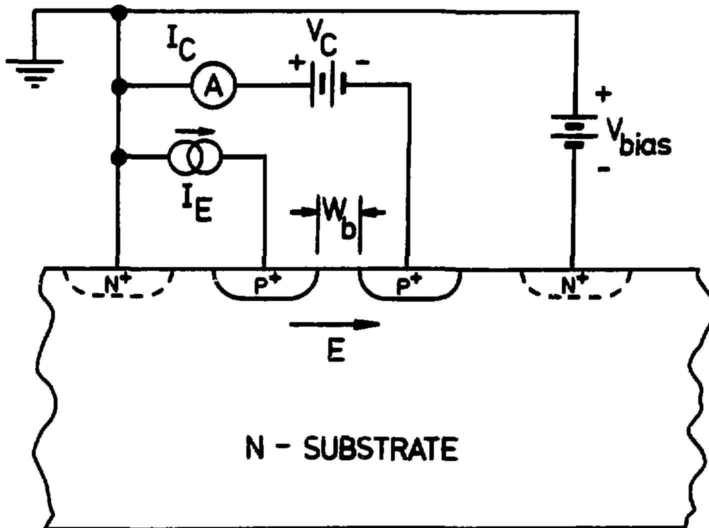


Fig. 11 Bias configuration for field-aided lateral transistor (FALT) structures.

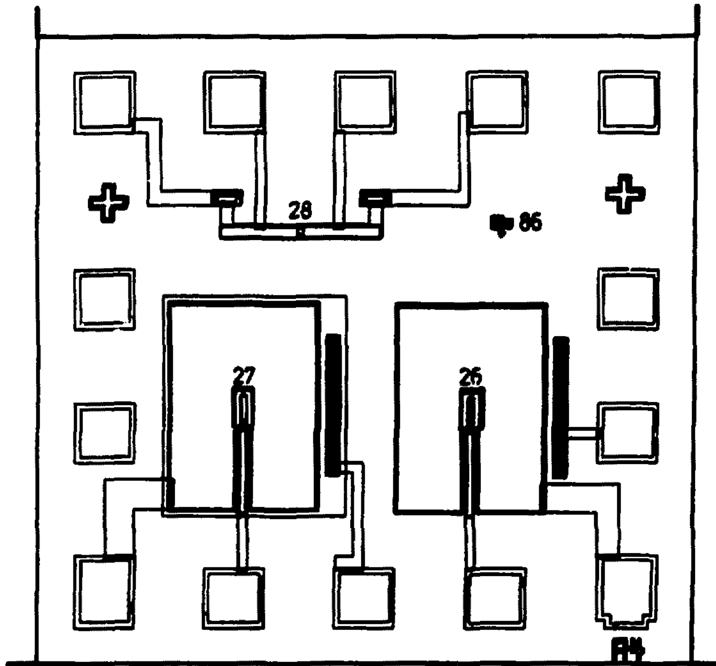


Fig. 12 Subchip A4 - Large gated diodes (p^+n and n^+p) with resolution pattern, and p^+-to-metal contact resistance structure.

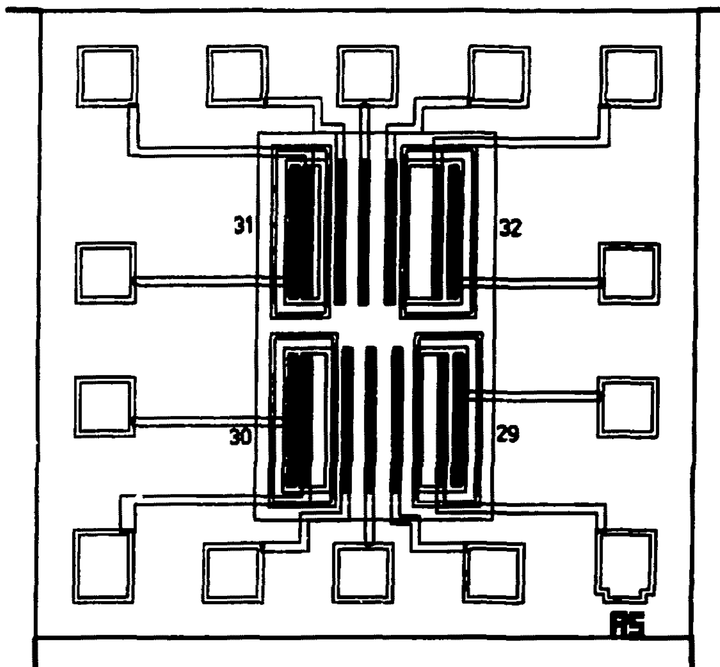


Fig. 13 Subchip A5 - Four latch-up structures (LATUS).

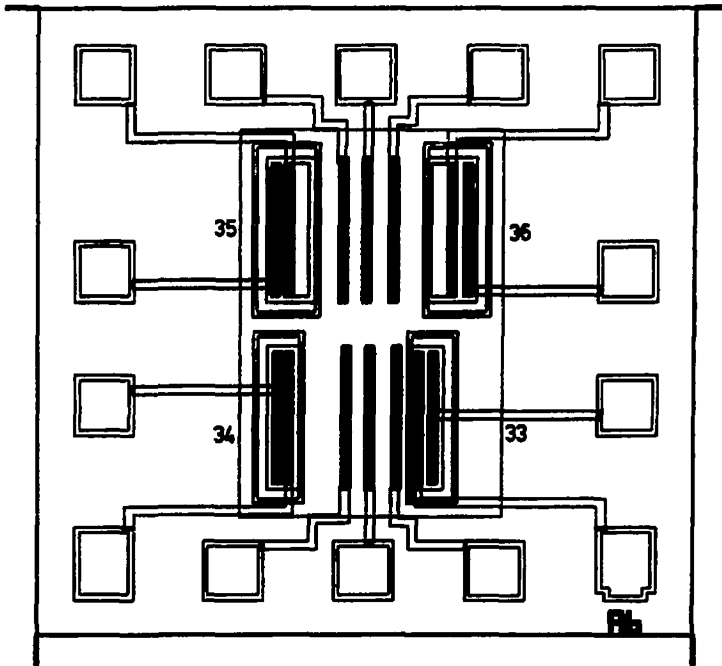


Fig. 14 Subchip A6 - Four latch-up structures (LATUS).

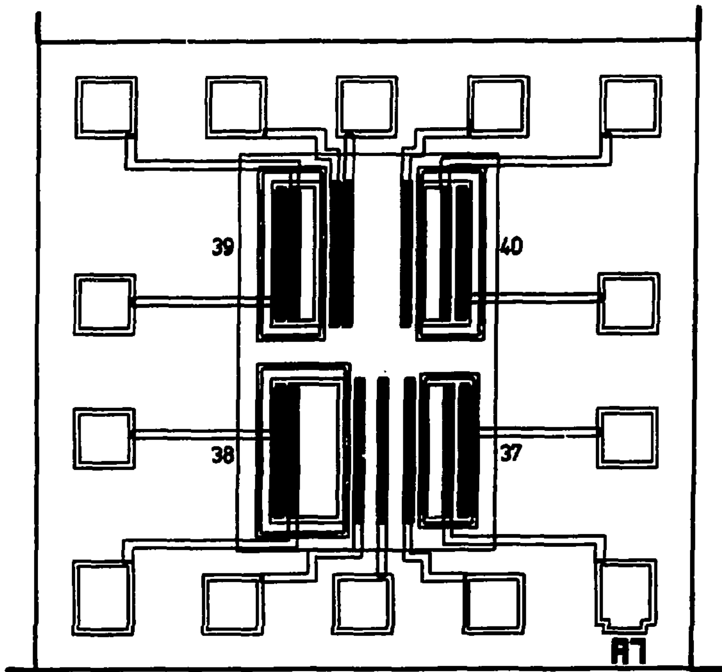


Fig. 15 Subchip A7 - Four latch-up structures (LATUS).

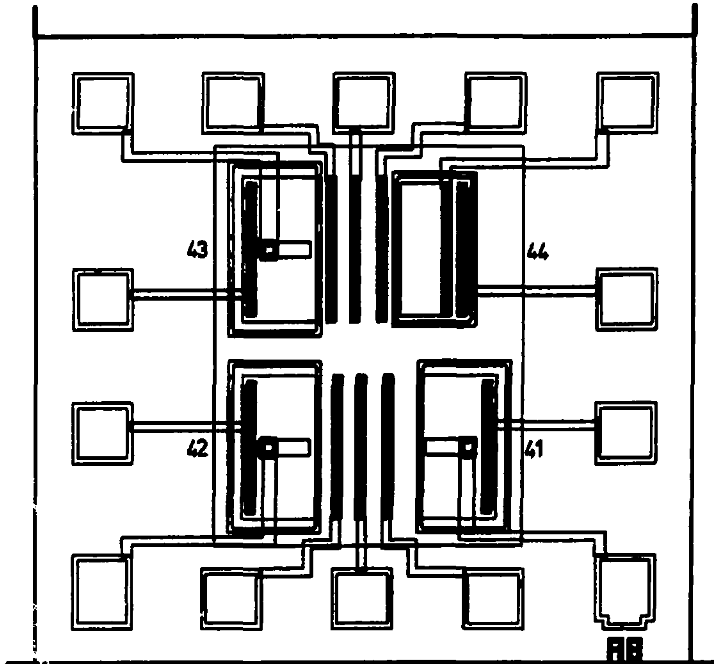


Fig. 16 Subchip A8 - Four latch-up structures (LATUS).

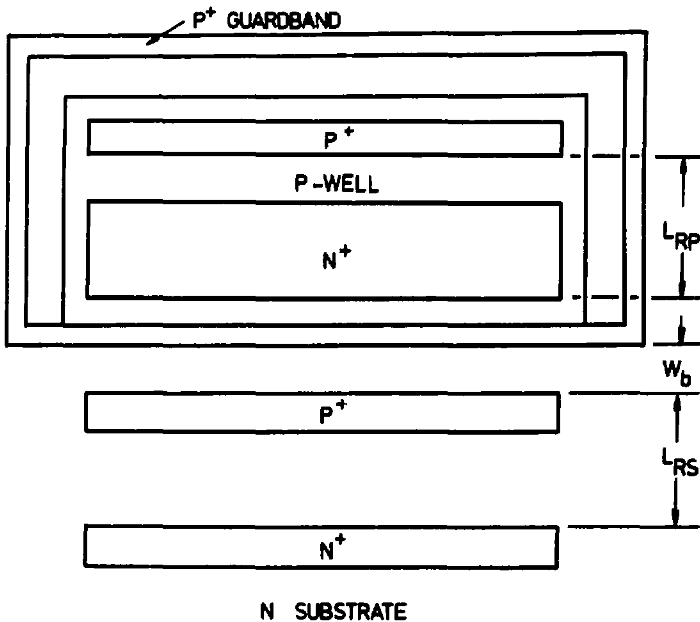


Fig. 17 Dimensional definitions for the latch-up structures (LATUS).

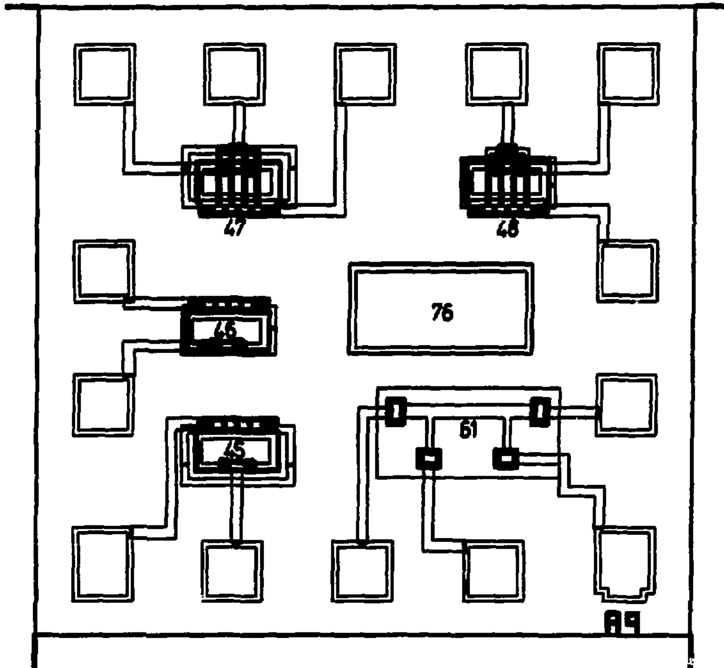


Fig. 18 Subchip A9 - ELA p-well resistance structures with dual contacts, field MOS capacitor, and p-well Kelvin contact resistor.

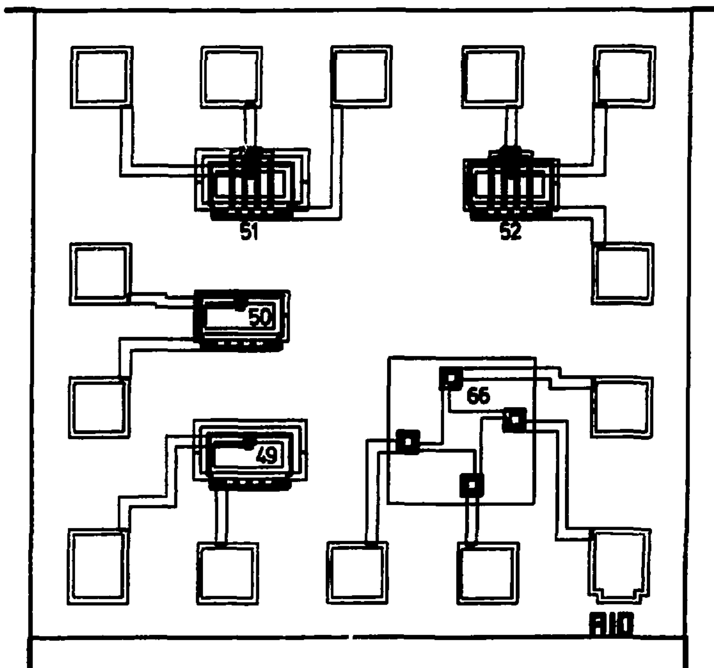


Fig. 19 Subchip A10 - ELA p-well resistance structures with single contacts, and p-well van der Pauw resistance structure.

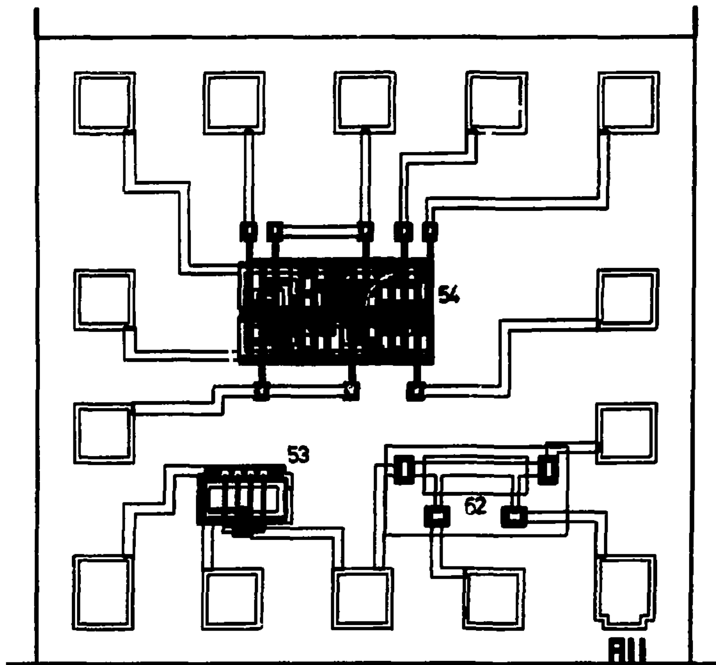


Fig. 20 Subchip A11 - ELA 1470 RST cell, single 4 μm gate p-well resistance structure, and pinched p-well Kelvin contact resistor.

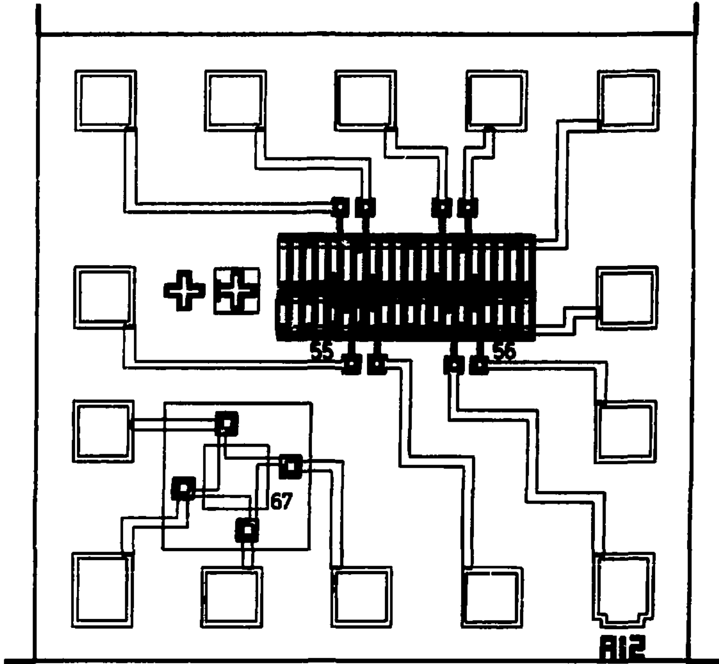


Fig. 21 Subchip A12 - Two ELA 1720 2-input OR gates (one with V_{SS} straps and the other without V_{SS} straps), and pinched p-well van der Pauw resistance structure.

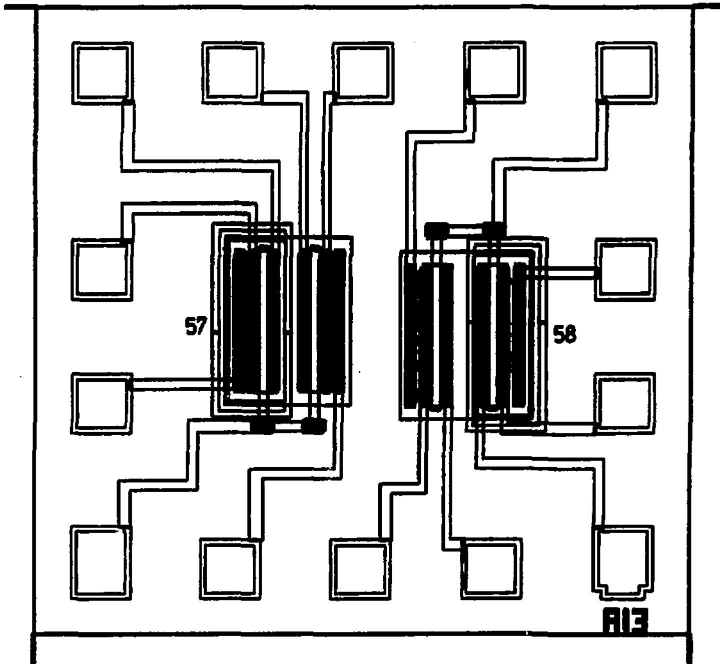


Fig. 22 Subchip A13 - Two silicon gate CMOS inverters for latch-up studies.

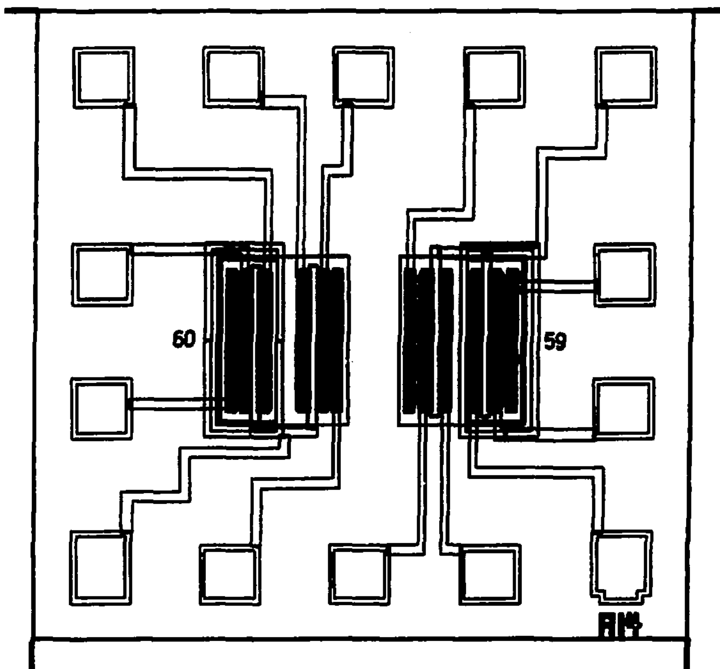


Fig. 23 Subchip A14 - Two metal gate CMOS inverters for latch-up studies.

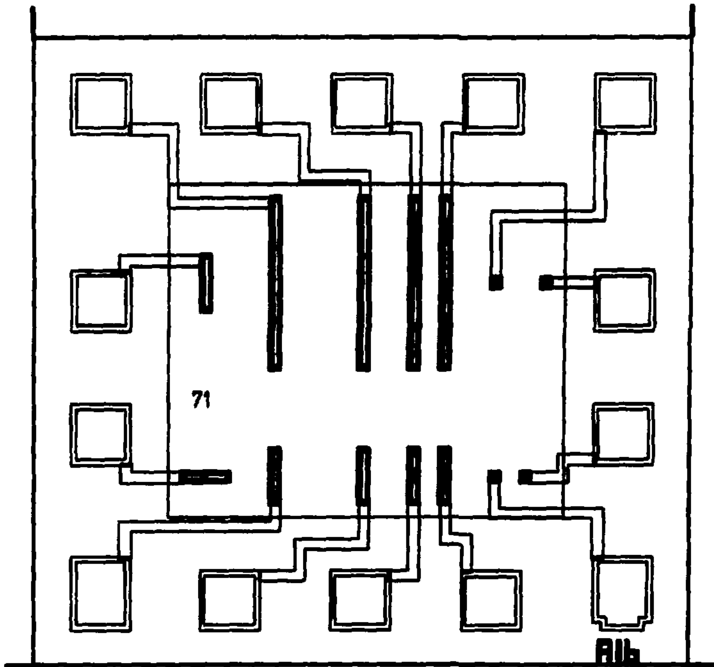


Fig. 24 Subchip A16 - Substrate spreading resistance test structures (14 contacts).

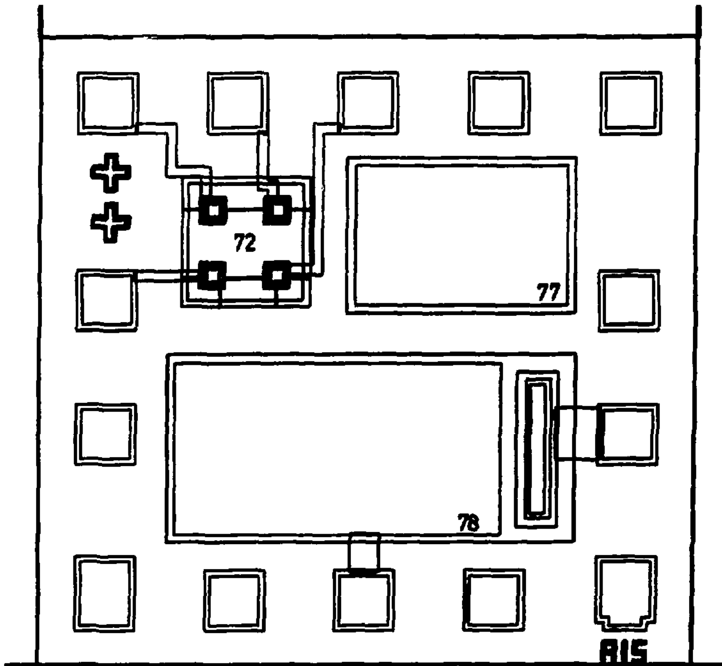


Fig. 25 Subchip A15 - Collector (substrate) resistance 4-probe square array structure, field MOS capacitor, and p-well MOS capacitor.

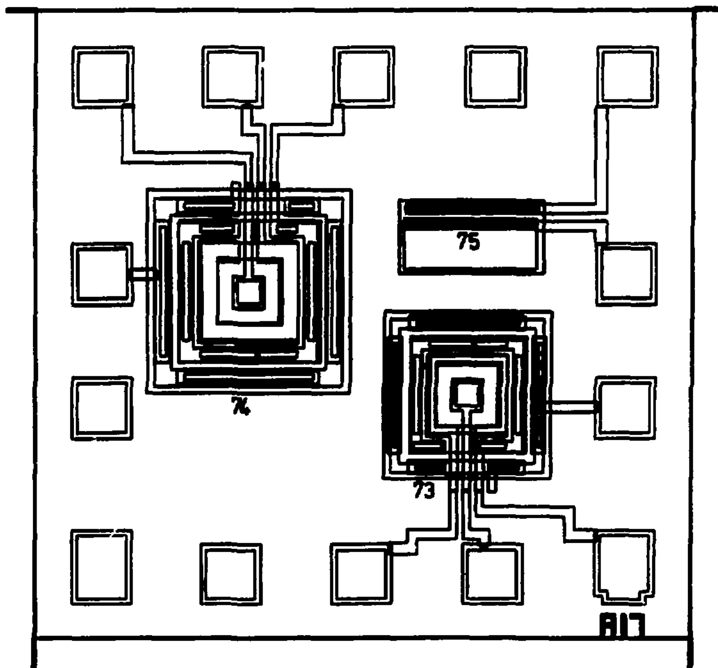


Fig. 26 Subchip A17 - Two square lateral pnp transistors with gates, and vertical p-well npn transistor.

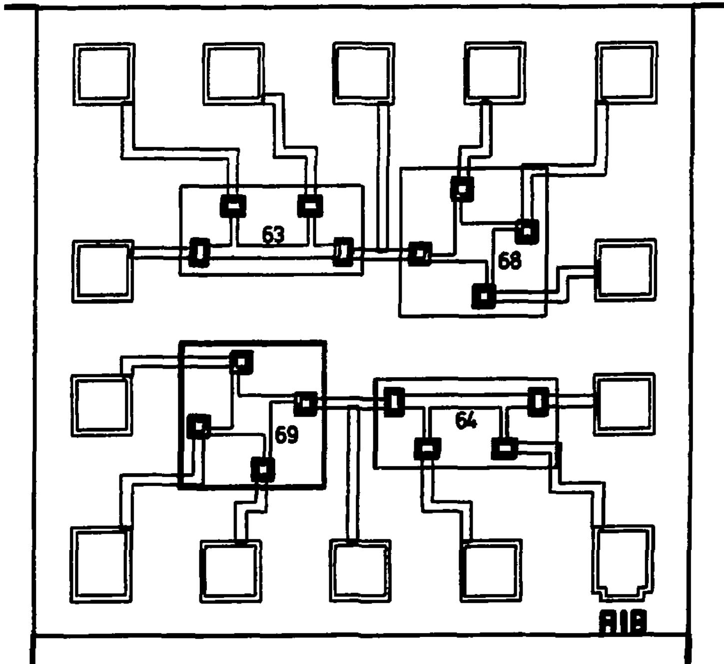


Fig. 27 Subchip A18 - Source/drain n^+ and p^+ van der Pauw resistance structures and Kelvin contact resistors.

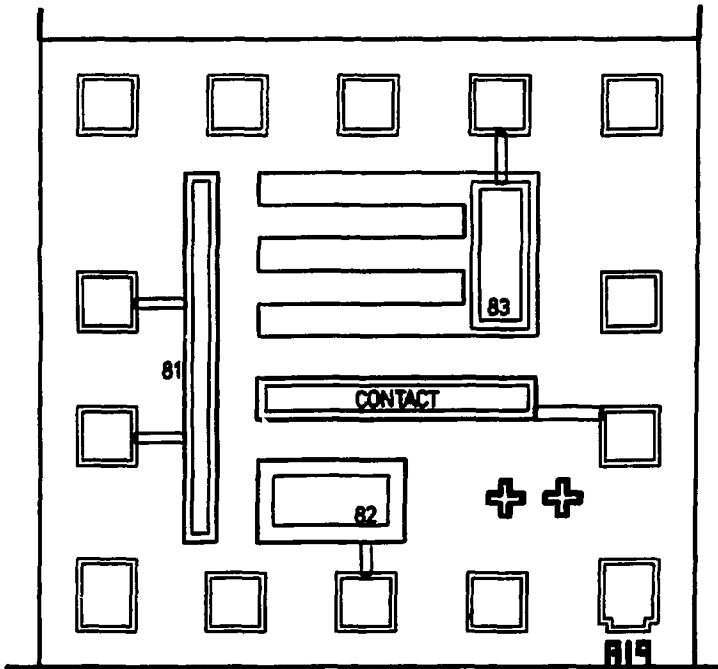


Fig. 28 Subchip A19 - Three $p^{+}n$ diodes for leakage current studies.

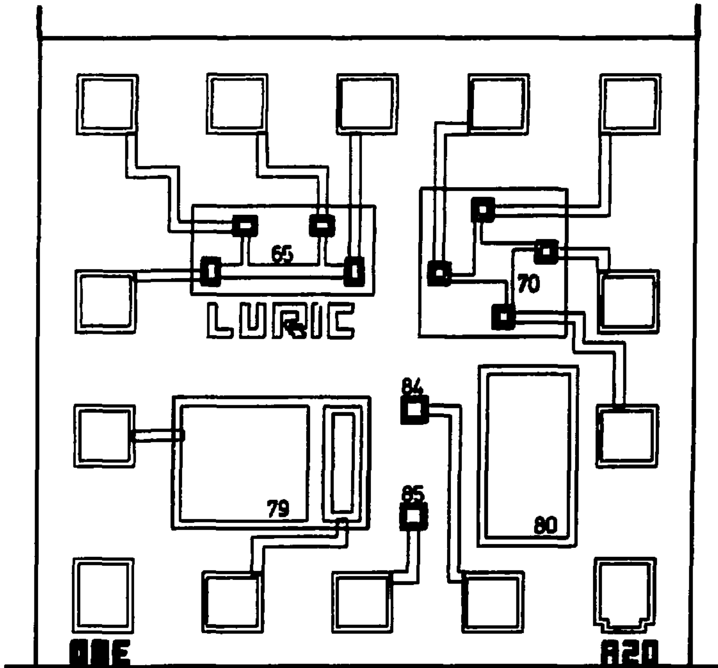


Fig. 29 Subchip A20 - Guardband (silicon gate process) p^+ resistance structures, gate oxide MOS capacitor, field oxide MOS capacitor, and two square p^+n diodes.

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