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Design of Readout Electronics for a Scintillating Plate Calorimeter

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Abstract

We describe the progress made on the design of readout electronics for a compensating scintillator plate calorimeter.

INTRODUCTION

A scintillator calorimeter produces unique problems for the designer of readout electronics. On the one hand the narrow time structure of scintillator pulses, ~10 nsec, is well matched to the rf structure of the SSC and gives hope of isolating information from individual beam crossings. On the other hand, the compensation mechanism and the need to broaden the pulse shape for use with analog signal sampling devices gives a somewhat wider time structure, ~50-100 nsec. Furthermore the granularity of such a device implies that the full energy of an electromagnetic shower may be totally contained within one readout channel. If the resolution of the electronics is not to compromise the intrinsic resolution of the calorimeter, assumed to be $\sigma/E \approx 15\%/\sqrt{E} + 1\%$ (E in Gev), coverage of the full dynamic range (40,000:1) requires at least two 12-bit devices with 7 bits of overlap for a linear front-end electronics chain.

The positioning of the electronics also is a critical issue. At luminosities of 10^{33} $cm^{-2}sec^{-1}$, electronics placed on the calorimeter must withstand doses of at least 10^{10} neutrons/cm^2 and 2000 Rad per year at 90°.

In the past year, the scintillating calorimeter collaboration has begun studying these and related issues. Among the work reported below is: a study related to remote location of the calorimeter electronics, a comprehensive program to evaluate the properties of FADCs capable of operation at 60-80 MHz, design of a analog memory unit and development of a "benchmark system" to help evaluate components under development both within and outside our collaboration.

REMOTING OF ELECTRONICS

The advantages of locating a substantial fraction of the front-end electronics away from the calorimeter include: accessibility and hence ease of maintenance and future upgrades, significantly reduced exposure to radiation and more space for cooling. The systems evaluated involve either using fiber optics for transmitting signals from phototransducers on the calorimeter to remote electronics, or bringing the scintillator light signals along fiber optic paths to remote phototransducers and electronics.

An investigation was made of the performance and cost of fiber optic links for sending analog data signals (and a possibly digitized trigger signal) from and digital control and clock signals to a multiplexed set of phototransducers. Analog bandwidths above 200 MHz and digital rates of up to 2 Gigabits/sec exist for such systems. The dominant cost is in the fiber optic links, ≥$300/channel.

The dominant cost in the alternative scheme of bringing the scintillator light away from the surface of the calorimeter is in the fiber itself. Long, low attenuation fibers are required and the total fiber length is in excess of 10,000 km. Low loss glass fibers are available, but the cost is prohibitive ($3000/km). There also may be difficulty in bonding glass fibers to the wavelength shifter fibers of the calorimeter. Clear acrylic fibers are currently being evaluated as an alternative approach.

FADC EVALUATION

A systematic study of commercially available Flash A/D converters capable of 100 Megasample per second operation has begun [1]. Such FADCs could be used to digitize the phototransducer output for trigger purposes or could be used with a non-linear preamplifier as part of the data collection stream. (Development of such an ASIC preamplifier is part of a Fermilab effort.)

We have built a CAMAC based test bench controlled by a VAXstation 3100 for the testing of FADCs. Communication with the test bench components is via both SCSI and GPIB buses. Two special purpose programmable CAMAC boards have been built: one provides clock and trigger signals, the other interfaces to various evaluation boards. The clock/trigger board allows ten discrete frequencies in the range 20-140 MHz to be supplied to the FADC under test. The FADC board contains 1 kbyte of 12-bit memory to store the digitized data. FADCs with dynamic ranges up to 12-bits can be tested. (Minor modification of the clock/trigger board can extend the range of available clock frequencies to lower values.) The test procedures follow the guidelines given in IEEE Std-1057, "IEEE Trial-use Standard for Digitizing Waveform Recorders." Among the properties measured are gain, offset, differential and integral non-linearity, maximum static error, monotonicity, hysteresis, effective number of digitizing bits, signal-to-noise ratio, peak error, aperture uncertainty, settling times, etc. Table 1 gives preliminary results of some of these studies for three of the FADCs currently under test.

Flash ADC	AD9002	CXA1176	CX20116
Manufacturer	Analog Devices	Sony	Sony
Advertised Maximum Rate (MSPS)	125	300	110
Clock Rate for Measurements(MHz)	30.0	80.0	20.0
Gain			
Static	0.995	0.994	0.996
Dynamic	0.983	0.989	0.995
Differential Non-Linearity			
Sine Wave	0.300	1.000	0.800
Triangle Wave	0.297	not measured	0.559
Integral Non-Linearity	0.576	0.638	0.333
Signal-to-Noise Ratio	168.1	156.0	202.5
Effective Number of Bits	7.271	6.988	7.405

Table 1 -- Preliminary Results from FADC Testing

ANALOG MEMORY

One possible scheme for collecting data from a scintillating calorimeter is given in Figure 1. In this scheme A/D conversion is done after two levels of triggering. This reduces the speed at which the conversion must be accomplished, but requires the data be stored in analog form for periods of up to 50 μsec. In addition if the storage is to be done on the outer surface of the calorimeter the analog memory units must be radiation hard. A VLSI chip to store analog signals from the calorimeter has been designed and is scheduled for submission to the MOSIS foundry in early November, 1990. The analog phototransducer output signals are

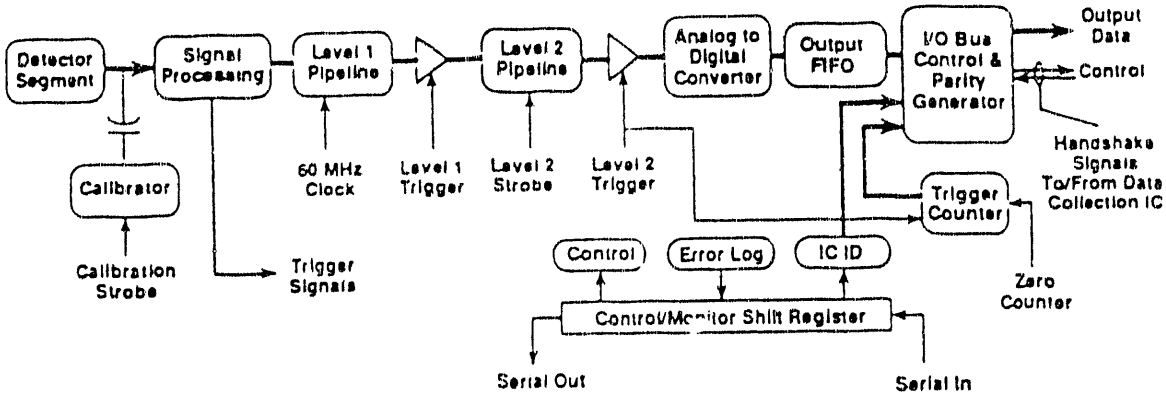

Figure 1 -- Possible Readout Architecture

integrated for 16 nsec and stored on capacitors. Integration, storage and digitization are performed on a single chip upon receipt of a second level trigger signal. The architecture stresses the simplicity of the logic and has the potential for deadtimeless operation. Figure 2 is a schematic diagram of one of the eight [illegible] be located on a single chip. Figure 3 shows the output circuit comparator for digitization.

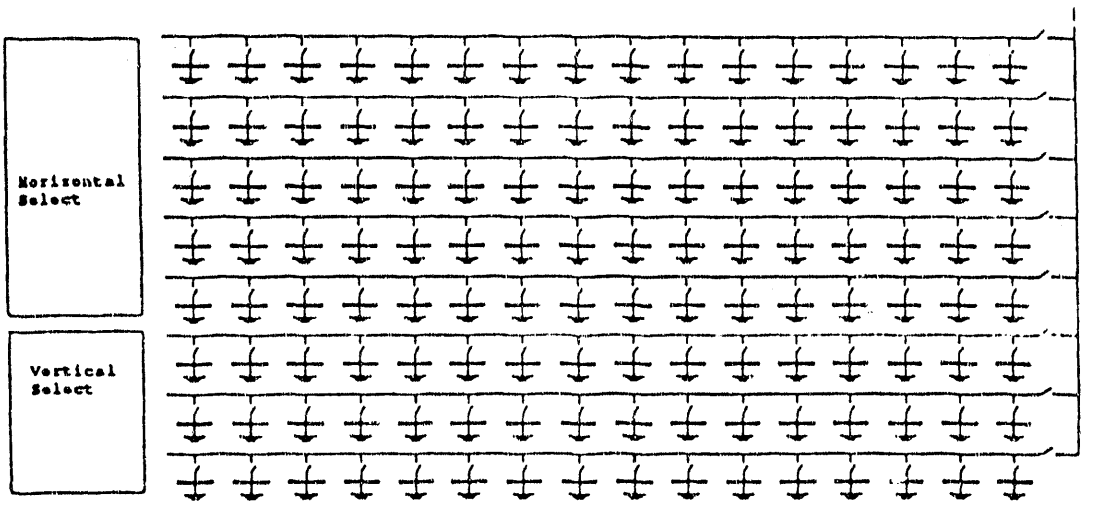

Figure 2 -- 8x16 Capacitor Array with Shift Registers Shown

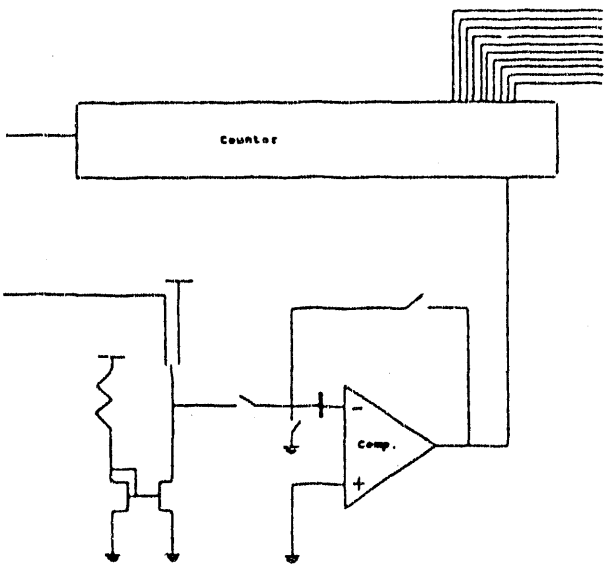

Figure 3 -- Output Stage of VLSI Chip

Discussions have begun with industry on creating a radiation hardened version of this chip.

BENCHMARK SYSTEM

We also are developing a "benchmark system" to use in a Fermilab test beam with calorimeter prototype modules which will allow the testing of new components as they become available.

Notes and References

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[1] H. B. Crawley et al, "Performance of Flash ADCs in the 100 MHz Range I. Test Bench and Preliminary Results," submitted to this symposium and to the 1990 Nuclear Science Symposium of the IEEE.

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