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LATCH-UP IN CMOS INTEGRATED CIRCUITS

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Abstract

An analysis is presented of latch-up in CMOS integrated circuits. A latch-up prediction algorithm has been developed and used to evaluate methods to control latch-up. Experimental verification of the algorithm is demonstrated.

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LATCH-UP IN CMOS INTEGRATED CIRCUITS

D. B. Estreich and R. W. Dutton

Junction isolated Complementary MOS (CMOS) integrated circuits often exhibit latch-up effects in either an ionizing radiation environment or terminal overvoltage stress condition. The latch-up state has been shown to arise from regenerative switching, identical to the turn-on mechanism in four-layer pnpn diodes.[1,2] In a typical bulk silicon CMOS integrated circuit numerous pnpn paths exist; it is important to be able to analyze the latch-up susceptibility of such pnpn paths in order to characterize and implement corrective design or process changes as needed to control latch-up.

A study has been made of the dominant physical mechanisms and electrical properties required for a CMOS pnpn path to sustain latch-up. From the results of this study an algorithm has been developed which gives a formal procedure to predict if conditions allowing latch-up can be achieved along a given pnpn path. The salient features of this algorithm are summarized:

(1) Identify potential pnpn latch-up path,
(2) compute p-well resistance and substrate spreading resistance along pnpn path,
(3) identify minority carrier injecting regions within the pnpn path,
(4) compute parasitic npn transistor current gain,
(5) compute parasitic lateral pnp transistor current gain (include field-aided gain enhancement if present),

(6) compute holding current of the pnpn path necessary to give current gain product required to sustain latch-up, and

(7) test to see if computed current gain product requirement exceeds the gain product from the holding current requirement.

The algorithm requires only the pnpn path geometry, the p-well sheet resistance, and substrate resistivity for input data.

New results have been obtained relating the lateral pnp transistor's field-aided current gain enhancement to the initiation of CMOS latch-up. A theory has been developed to describe the field-enhanced current gain and experimental data has confirmed the importance of such gain enhancement in latch-up. For this reason, the inclusion of the field-aiding mechanism is often essential in latch-up threshold prediction and can impose special restrictions on the testing of CMOS integrated circuits for latch-up screening.

Methods to prevent and control latch-up have been studied. Using the latch-up prediction algorithm, it is possible to analyze the effectiveness and establish the minimum requirements for latch-up control techniques. The most common methods discussed to date for latch-up prevention include:

(1) The establishment of layout rules (minimum spacings) to reduce the parasitic transistor current gains,

(2) minority carrier lifetime reduction,[3] and

(3) the use of p-type buried layers under the p-well and epitaxial substrates.

Special test structures have been used to study latch-up prevention techniques and can be used to monitor latch-up susceptibility on a CMOS process development line.

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