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ELECTRONIC TECHNOLOGY AND THE SLD DETECTOR*

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The SLD detector consists of five major subsystems, each with associated front-end electronics and an integrated FASTBUS control and data acquisition system. This paper highlights the choices among electronic technologies that have been developed for the SLD detector electronics. The common control, calibration, and data acquisition architectures are described. The functions of selected SLD integrated circuits, standard cells, gate arrays, and hybrids are summarized, and the integration of these functions into the common data acquisition path is described. Particular attention is directed to four areas of electronic technology developed for the SLD detector: (1) the preamplifier hybrid designs are compared and their performance and implementation examined; (2) the application of full custom CMOS digital circuits in SLD is compared to gate array and EPLD (electrically programmable logic device) implementations; (3) the fiberoptic signal transmission techniques in SLD are examined and the data rates and link topology are presented; and (4) finally, the packaging, power consumption, and cooling requirements for system functions resident inside the detector structure are explored. The rationale for the implementation choices in the SLD electronics is presented so that others might benefit from our experience.

1. SLD ARCHITECTURE AND OVERVIEW

The SLD detector is designed to study e^+e^- interactions at the Z^0 energy. The SLD is completing final assembly at the Stanford Linear Accelerator Center. Commissioning and a cosmic ray data run are planned to beginAugust 1990, with the detector scheduled to move onto the beamline of the Stanford Linear Collider in the fall of 1990. The SLD detector has been designed by an international collaboration of physicists and engineers.[1,2] SLD is unusual among contemporary detectors in that the bulk of the signal amplification, detection, and digitization is performed in custom hybrid or

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TABLE 1
SLD Detector Electronic System Summary: Detector Elements and Channel Count.

Subdetector	Function	Type	Channel Count	Data Volume (Mbyte/event)
Vertex	Precision tracking	CCD pixel	110×10^6 pixels	110
Drift	Tracking	Proportional wire	14K at 512 samples/channel	14
CRID	Particle ID	Čerenkov radiator/ proportional wire	15K at 512 samples/channel	15
LAC	Calorimetry	Lead/liquid argon	43K at 4 samples/channel	.35
WIC pads	Muon calorimetry	Streamer tube	10K at 2 samples/channel	.04
WIC strips	Muon tracking	Streamer tube	80K (digital discriminators)	.01
			Total data acquisition:	140 Mbyte/event

monolithic electronic circuits physically located within the detector structure. The system includes nearly 100,000 analog channels and another 80,000 digital channels. A digital fiberoptic network distributes control and timing signals to all detector subsystems, with associated digital fiberoptic links for output data paths from the detector elements to the external FASTBUS processing system. Each of the five subsystems has specialized electronic processing channels designed using a mix of analog and digital techniques. The analog functions have been implemented using custom analog integrated circuits, standard cells, hybrids, conventional components, and printed circuit board techniques. The digital functions have been implemented in a mix of custom CMOS VLSI, CMOS gate arrays, EPLD devices, and standard components. In each system a technology was chosen to implement the necessary functions in a manner consistent with the overall performance, space, and power constraints.

The SLD detector is composed of five subdetectors, which are the Vertex detector, the Drift Chamber, the Cherenkov Ring Imaging detector (CRID), the Liquid Argon Calorimeter (LAC), and the Warm Iron Calorimeter (WIC). Table 1 provides a summary of the features of each of the subdetectors.

Figure 1 presents a block-level diagram of the required data acquisition functions of the five SLD subdetectors. This diagram is directly applicable to the electronic functions used to instrument the Drift Chamber, the CRID, the LAC, and the WIC Pads (Muon Calorimeter) systems. The Vertex and the WIC Strip (muon tracking) systems use similar processing functions [including the Timing and Control Module (TCM)] with slightly different FASTBUS modules and data processing.[3,4,5,6]

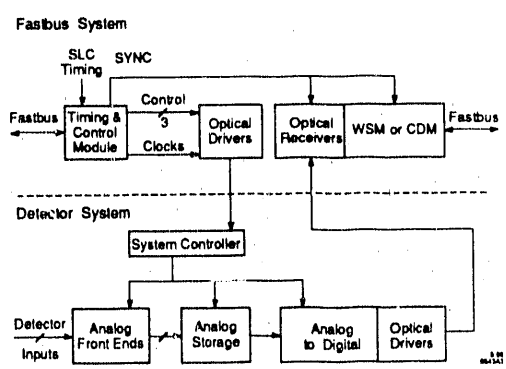

FIGURE 1
Block diagram of the "generic" SLD data acquisition system showing components in the FASTBUS system and on the detector.

All of the systems use a FASTBUS TCM module to send data, commands, and timing information to system controller modules physically located within the detector structure. These system controller modules decode the command and data messages, and use the timing signals to operate and synchronize the specific analog front-end circuitry, the analog sampling hybrids and the local digitizing system. The output signals from the detector to the external FASTBUS system (with the exception of the Vertex system) are all digital signals which are transmitted via a fiberoptic path.

This architecture places the analog and calibration functions directly inside the detector, and many electronic functions have been implemented in hybrid or IC forms to conserve space and power. The system hybrid preamplifiers typically contain linear amplification and shaping functions, precision input calibration sources, digital calibration control circuits and power switching and control elements. All of the SLD detector linear systems utilize some sort of analog storage elements to sample the detector signal, hold it in an analog buffer for later processing, and present the sampled values for digitization.

The SLD electronic systems take advantage of the 120 Hz beam crossing rate of the Stanford Linear Collider facility. This low crossing rate (with a 2 Hz average trigger rate at the design luminosity) allows 8 mS between beam crossings for signal digitization and trigger decisions. This relatively low repetition rate allows the SLD processing systems to use a multiplexed digitization scheme, with a concomitant simplification of the output data path. When a trigger is detected, the readout of the entire detector system is completed in a 66 mS interval.

2. CONTROL AND TIMING SYSTEM

The data acquisition system is controlled via a FASTBUS control path through the Timing and Control Modules. The TCM modules are programmable sequence generators that are driven from the Linac master oscillator. One TCM per subsystem is used to send command, data, and timing information via fiberoptic links to the device controllers. Each of the five detector TCMs executes a system specific command and timing sequence. The common master oscillator insures synchronization of the individual sub detectors to each other and to the electron-positron collisions within the detector.[7]

The message protocol used to send commands, data, and timing information to the device controllers is an SLD developed protocol common to all SLD device controllers. It is a bit serial message structure which includes an eight bit controller address field (including a broadcast address), a five bit command field and a variable length data field used to send data (such as channel calibration patterns) associated with the type of command. Commands which are part of a data acquisition sequence distribute timing information as part of the message.

3. FASTBUS SIGNAL PROCESSING ORGANIZATION

The SLD detector FASTBUS system has been designed using 11 types of standardized FASTBUS modules. All systems receive the serial data stream from the detector and convert this stream to a parallel data structure in an auxiliary card using timing information from the TCM. The LAC and WIC Pads share a similar structure based on a Calorimeter Data Module (CDM) processing system which contains 4 68020 microprocessors. The CRID and Drift systems use a Waveform Sampling Module (WSM) which is a variant of the CDM module.[4] The WIC Strip system uses a WICDRM module containing a 68020 microprocessor to process the serial digital data generated by the preamlifier/discriminator hybrids from the streamer tubes.[8] The Vertex system has the most complicated FASTBUS processing comprising VDP (CCD clock driver), VAB (amplification and bias generation) and VDA (digital cluster processing) modules. All systems use the Aleph Event Builder (AEB) module for online processing, with an additional AEB used for trigger processing.[9]

With the digitization functions inside the detector, the density of processing functions in FASTBUS is very high. As an example, each CDM module used in the

LAC system processes data from 1440 calorimeter channels. The entire FASTBUS plant for the full complement of 100,000 analog channels and 80,000 digital strip signals consists of only 18 crates. Of this number, six are required for the Vertex detector processing. The high density of the FASTBUS system reflects the complexity of functions that are integrated inside the detector and the processing power that is contained in the CDM/WSM modules.

4. SLD PREAMPLIFIER TECHNOLOGY

The front-end signal processing functions in the SLD detector have been implemented as hybrid circuits using discrete bipolar and FET transistor circuits, CMOS gate arrays and standard logic, and an analog standard cell custom component.[10,11,12] Figure 2 presents a block diagram of a "generic" preamplifier designed for SLD. All of the preamplifiers are multistage voltage or transimpedance amplifiers with pulse shaping networks and an input calibration source. Several of the preamplifiers additionally contain input protection circuits, digital calibration logic used to select internal channels for calibration or special test modes, power switching elements controlled by external digital signals, and high current output buffers. Table 2 compares the organization, technology, bandwidths, and internal features of these preamplifier building blocks.

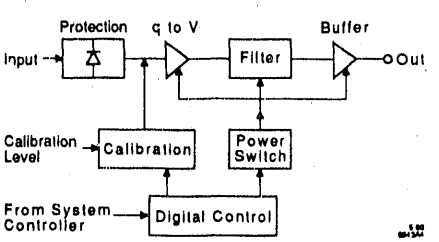

FIGURE 2
Generic pre..nplifier block diagram.

It is interesting to contrast the implementation of the CRID and Drift preamplifier and front-end circuits. Both systems are waveform recording digitizers that capture signals from proportional wire chambers, yet the technologies and partitioning of the system functions are quite different.

The Drift system is organized around a two-substrate custom hybrid circuit.[13] It is a highly integrated eight-channel front-end hybrid that allows all eight sense wires of a single drift cell to be processed in a single package. The amplifier substrate contains eight transimpedance amplifiers which are constructed of discrete bipolar transistors, surface mounted capacitors, and printed resistors. Each amplifier is composed of a three gain stages requiring six NPN and PNP devices bonded to the amplifier substrate. The preamplifiers provide 60 dB of voltage gain with a unity gain frequency of 110 MHz. Careful design attention is needed to avoid channel-to-channel crosstalk, as well as crosstalk from the fast comparators used in the hit trigger system. Each amplifier has a laser trimmed gain resistor adjusted for uniformity of channel gain.

The calibration substrate provides a precision calibration source, bipolar power supplies and power switching circuitry, CMOS logic to control the calibration system and select channels, and a digital trigger system that uses eight fast comparators and a CMOS gate array. This hit trigger system produces a serial bit stream that indicates if any of the eight channels produced a pulse over an externally programmed threshold. The analog functions are provided by discrete bipolar transistors or commercial analog circuits in chip form.The logic functions are constructed of a single custom CMOS gate array and commercial logic in die form.

The Drift preamp represents the densest and most integrated of all the SLD preamplifiers. The assembled hybrid provides a complete digitally controlled eight-channel subsystem in an 11 cm^2 package area. The development time—as well as integration and fabrication difficulties with cross-talk, grounding scheme, yield, etc.—of this system suggest to us that greater densities or functional integration will require different approaches.

The CRID preamplifier is organized as a single channel hybrid such that each end of a sense wire in the CRID

TABLE 2
SLD Preamplifier Summary: Properties and Performance.

System	Function	Implementation	Channels/ Package	Frequency Response (Rise Time)	Power/ Channel	Features
Vertex	CCD pixel charge amplifier	Hybrid	1	35 MHz	560 mW	External test input
Drift Chamber	Waveform digitizer with charge division	2-Substrate hybrid	8	20 MHz 15 ns	20 mW	Calibration source, Power switching, Trigger discriminator
CRID	Waveform digitizer with charge division	Monolithic macro cell + JFET, Hybrid carrier	1	67 ns	100 mW	Calibration source, Power switching
LAC	Charge integrator amplifier	2-Substrate hybrid	8	4 μs shaping time	30 mW	Calibration source, Power switching
WIC pads	Charge integrator amplifier	Monolithic amplifiers	2	5 μs shaping time	135 mW	Calibration source, Tower capacitance test
WIC strips	Streamer tube amplifier/ discriminator	Hybrid amplifier, Monolithic discriminators/ shift registers	4			Digital shift register output

detector has a single-channel preamplifier. The preamplifier functions are implemented using a single discrete low noise JFET, combined with an analog macrocell circuit that includes all of the remaining bipolar circuitry for the amplifier and pulse shaping. This approach allows the use of a low noise JFET, and the combined hybrid circuit provides high sensitivity (2.7 $\mu V/e^-$ gain) with a low noise floor of 1600 e^- rms. The CRID system additionally requires large dynamic range of 60 dB due to the avalanche gain of single photoelectron signals; the preamplifier is designed to recover from large overload signals with a rapid return to baseline. The macrocell is a patterned wafer that contains a selection of predesigned bipolar transistors, resistors, and capacitors which are not interconnected.[14] The part selected for the CRID preamplifier contains four macrocell arrays which provide 66 PNP and NPN devices plus diffused resistors, an interconnect bus, and several capacitors. The custom portion of the design is provided via a two-level metallization pattern which is user specified. This approach is much more economical than a full custom analog circuit approach, especially for the relatively low volume of circuits required ($\sim 3,000$). The final hybrid is a very simple substrate which uses the standard cell part in a surface mount package, active trimmed offset and gain components, and the external JFET for the transimpedance stage. Figure 3 shows the structure of the preamplifier and the partitioning of functions. The calibration control and logic functions are provided on a conventional PC motherboard which carries the preamplifiers.

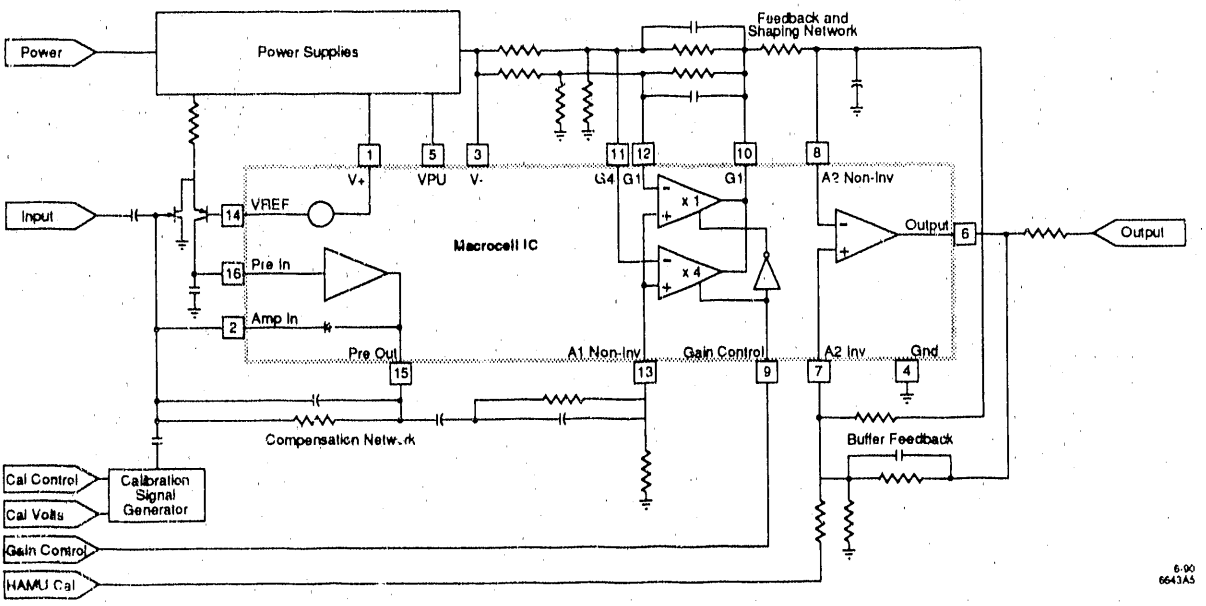

FIGURE 3.
CRID preamplifier composed of macrocell amplifier and external JFET and surface mount components.

This macrocell approach proved to be very successful in the CRID implementation, and the CRID hybrid is much simpler and easier to manufacture than the LAC and Drift preamplifiers constructed using discrete transistors. The manufactured cost of the packaged macrocell amplifier for the SLD production run was $3.30 per chip, with approximately $10K NRE cost to develop the design.

5. CUSTOM VLSI vs GATE ARRAY vs EPLD TECHNOLOGIES

The SLD architects have chosen an interesting technology mix in the implementation of functions in full custom IC form, gate array (and standard cell) technologies, and commercial EPLD (Electrically Programmable Logic Device) devices. We have used all of these techniques and tried to balance volume of implementation, required density of functions, development time and system cost.

The Calorimeter Data Unit (CDU) and Analog Memory Unit (AMU) chips are custom analog NMOS chips designed by a SLAC–Stanford University[15,16] collaboration. These circuits are the heart of the SLD processing system; they allow the ADC functions to be implemented in the detector and the serial multiplexing of the 100,000 analog channels during the data acquisition cycle. These key components provide the analog buffering of the detector signals, and without them the FASTBUS signal processing would have been an order of magnitude larger. These devices required a three-year development cycle and the investment of six man-years of engineering time.

The LAC and WIC Pads systems use the CDU as a multichannel simultaneous sample and hold system with sequential read.[15] These applications use the parallel write/serial read structure of the CDU circuit to share a single digitizer for many input channels.

The Drift and CRID systems in the detector use the AMU as a high-speed analog waveform memory.[16] Each AMU chip writes 256 successive samples of an input waveform into an analog memory, using a high-speed sampling clock. After sampling, the waveform samples

are then read out at a much slower digitizing rate. Again a single ADC is shared between many input channels, sequentially digitizing signals which are written in parallel. The HAMU hybrid packages 16 AMU die into a single hybrid circuit package, which samples eight parallel input channels using a 119 MHz write clock. The analog memory for each signal is 512 samples deep which allows a 4.3 μS sample record using the 119 MHz write clock. A read cycle of an eight-cell drift chamber motherboard takes 66 msec, which is 4096 data samples processed at the 2 μs/conversion effective ADC rate.

SLD development has produced two custom digital CMOS devices. The Digital Correction Unit (DCU) circuit has been designed for digital signal processing in the WSM/CDM FASTBUS modules, and a Cluster Arithmetic Processor (CAP) circuit has been designed for data reduction in the SLD Vertex System. These circuits provide algorithmic processing of raw digital data from the detector.

The SLAC designed DCU is a processing block used to linearize the sampled data from the AMU and CDU sampling chips.[17] The DCU operates with calibration data to provide a sixteen or an eight segment piecewise linearization of the calorimeter or sampled waveform data. The DCU linearization and calibration corrects for all signal elements in the analog processing chain, from the preamplifier through the analog buffering and slow A/D converters. This calibration compensates for gain errors, nonlinearities, offsets, and temperature effects. The DCU design contains approximately 42,000 transistors fabricated using a 2 μ CMOS process and was designed using a silicon compiler and hand optimization of the circuit layout. The DCU functions would occupy a significant portion of a FASTBUS module if implemented as standard logic. Each WSM or CDM module uses four of these devices.

The Vertex Cluster Arithmetic Processor (CAP) chip is a semicustom standard cell CMOS device developed by the Rutherford Appleton Laboratory.[18,19] It is used to sparsify the data from 110 million CCD pixels produced during a read of the Vertex Detector. Operating "on the fly" to minimize system deadtime, the CAP performs 1x1, 3x3, or 5x5 kernel convolutions on the 2D CCD data to search for clusters of hit pixels. Two independent digital filters are included to improve noise suppression. This chip is of approximately 5,000 gate complexity. The cluster processing algorithm compresses the 110 Megabytes of digitized CCD pixel data into a 40 Kbyte pixel value and cluster coordinate data record for offline processing.

A relatively simple CMOS gate array has been designed as a portion of the SLD drift chamber trigger processing system. This CMOS circuit is of approximately 300 gate complexity and one of these chips is included in each of the drift preamplifier hybrids. The straightforward structure of this design allowed very rapid design and fabrication of these parts.

SLD has made extensive use of EPLD devices for our digital functions. All of the device controller circuits have been implemented in UV erasable gate array circuits. These commercial parts utilize a macrocell structure with user programmable interconnects.[20] They are available with densities up to 128 macrocells (approximately 5600 equivalent gates) and the regular structure of these devices makes them very efficient for the implementation of state machines. As an example, each drift chamber motherboard (which processes data from 64 sense wires) is controlled and sequenced from a single 48 macrocell EPLD. While it would have been possible to design a CMOS gate array to provide the same functionality, it would not have been significantly denser, as the required functions are I/O or pin count constrained rather than constrained in functional complexity. Additionally, the flexibility and rapid prototyping available with the EPLD approach allowed new unanticipated functions to be added to the controllers, and several logic functions moved from one circuit board to another late in the design and integration phase of the project. This flexibility is a tremendous asset. Another feature we had to consider is the low production volume of these controller functions. It would have been uneconomical to produce gate arrays in production volumes of 100 parts, even if the designs had been finalized before the integration phase.

6. FIBEROPTIC DATA PATHS AND SIGNAL REDUNDANCY

The SLD processing architecture puts all analog digitization electronics within the detector (with the exception of the Vertex Detector) so that all control and signal paths in the acquisition system are digital. The early SLD system design used analog fiberoptic links from the AMU/CDU circuits inside the detector to external FASTBUS packaged A/D converters. This design proved difficult to implement for better than eight bit accuracy, and the system design chosen includes low power CMOS A/D components as part of each subsystem. A simple digital data protocol was developed for the transmission of 12 bit data with four additional framing and parity bits for error detection.

SLD has utilized commercial 820 nM fiberoptic driver, receiver, and cable components.[21] The majority of these links run at a 32 Mbit data rate, with the high-speed clock distribution system running at a 119 MHz clock rate. These data rates do not utilize more than a fraction of the optical fiber bandwidth. However, the data sources are distributed throughout the detector, and combining several 32 Mbit signal sources together into fewer optical channels would require additional electrical multiplexing within the detector and complicate the internal cable plant. We have organized the signals between the TCM modules and the device controllers as redundant fiber pairs, and redundancy is provided for critical output data links. With this topology a single point failure does not isolate any controller from the control path or remove tracking information in any solid angle. In this design we have tried to balance efficient use of the optical bandwidth, minimize the cable plant within the detector, and structure the loss of information should a link fail. Figure 4 shows the fiber distribution and data network used for the LAC Barrel.

We have achieved a tremendous reduction of cable plant volume compared to traditional detectors with external FASTBUS or CAMAC based digitization. As an example, all 35,000 barrel calorimeter signals are carried on 48 output fibers. The total fiber cable cross section

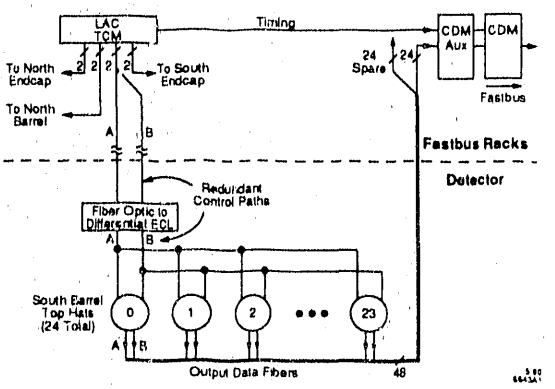

FIGURE 4

Redundant control and data paths as implemented on the LAC barrel.

for these 35,000 signals is less than 10 cm^2 including protective cable jacketing.

7. PACKAGING, POWER DISSIPATION, AND CIRCUIT PARTITIONING

The SLD Detector signal processing architecture has placed many functions inside the detector, so that much of the electronics is not packaged in a well-defined standard (such as FASTBUS) with power management and cooling systems. Some of the most difficult engineering design in the SLD electronics system results from these packaging, cooling and access constraints.

Electronic systems within the detector face an additional unusual requirement: they must operate exposed to the 0.6 Tesla magnetic field of the detector solenoid. This magetic field does not directly affect the majority of circuits, but conductors with time-varing currents experience magnetic forces. The hybrid power switching circuits and associated wire bonds required encapsulation to prevent Lorentz forces from producing bond failures.

The WIC Pads system is the most conventional system in its construction and partitioning. The system is mounted on the periphery of the detector steel structure in sixteen VME standard crates. Multilayer PC boards contain the preamplifiers and analog sampling functions, organized as 144 channels per 9U size VME module. A single controller module per crate communicates with the

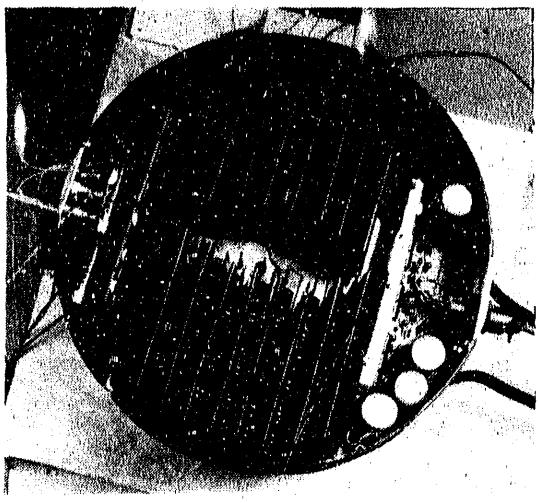

FIGURE 5

Photograph of a LAC "Top Hat" assembly. The cylindrical can is 13 cm high by 41 cm diameter.

FASTBUS system via the fiberoptic protocol; the controller includes the sequencing logic and the ADC functions. This system is cooled using conventional forced air, and has no special power dissipation limits.

The LAC system is packaged in 720 channel modules (referred to as "top hats") which are directly mounted on the signal feedthrough flanges of the calorimeter dewar. The system uses three types of multilayer PC boards to provide signal functions, with a single passive motherboard providing interconnections between the sixteen boards in each top hat. The amplification and sampling functions are partitioned with 48 channels per daughterboard and 15 daughterboards per feedthrough flange. A single system controller board, an A/D card, a microprocessor based cryogenic monitor, and a local power supply regulation card complete the electronic system. These systems are water cooled and the power is switched off (using a 15% duty cycle) between beam crossings to reduce power consumption. Each top hat enclosure processes data from 720 channels and dissipates 96 milliwatts/channel at the 120Hz crossing rate. Figure 5 is a photo of one of the enclosures with the system PC boards.[22,23]

The Drift system has provided the most difficult packaging task of any of the SLD subsystems. The system electronics are mounted directly to the chamber sense wires. This approach eliminates a cable plant with fast low-level signals, but it requires that the electronic motherboards must mount mechanically on the cylindrical geometry of the drift chamber. This detector comprises ten tracking superlayers, and each superlayer requires a unique physical board layout to match to the radius of curvature of each layer. As most electronic components and the SLD hybrid packages are designed in an orthogonal and rectangular coordinate form, matching the components to the cylindrical coordinates of the board layout proved to be a very difficult layout task.

Each drift motherboard is a self-contained waveform digitizer processing signals from 56 or 64 detector sense wires. The PC boards are constructed using 12 internal signal layers, with components surface mounted to both sides of a motherboard. Figure 6 is a photograph of one of these drift motherboards and figure 7 is a sketch showing the cross section of the motherboard assembly. Notice that two layers of components are attached on each side of the motherboard. Small outline IC (SOIC) circuits are surface mounted to the main board, and a second layer of

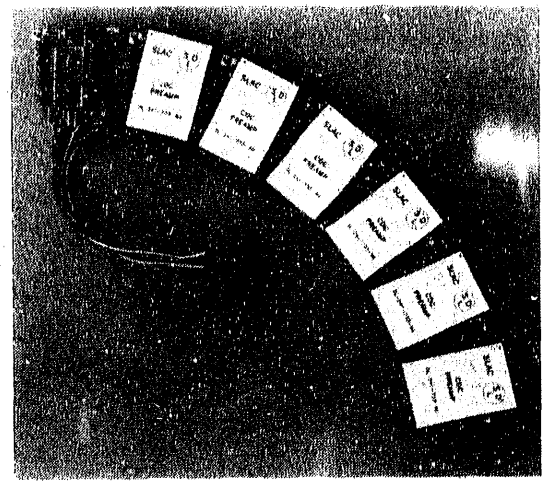

FIGURE 6

Photograph of a Drift system motherboard. This seven-cell board processes signals from 64 sense wires and is 7 by 40 by 1.4 cm.

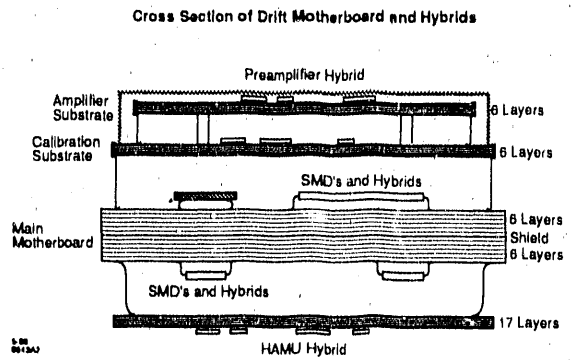

FIGURE 7

Cross section of a drift motherboard showing the main PC board with components and hybrids on both sides.

surface mounted hybrid packages are mounted over the SOIC circuits.

The Drift system is cooled via convected air to a water cooled chamber endplate. The system is extensively power switched during various parts of the acquisition cycle. Power management for the drift electronics motherboard is controlled by the system TCM. During beam crossings the system performs a write cycle and the preamplifiers, HAMU circuits, and high-speed clock logic is turned on to write waveform data into the analog memories. The front-end and HAMU circuits are then turned off during the trigger decision period, with the sampled waveforms stored as charge on the sampling capacitors of the powered off HAMUs. If a trigger is detected, the TCM issues a read command, which powers up the HAMU output buffer and ADC circuits. The HAMU circuits are then sequentially powered up to present their stored analog data and then powered down as their neighbor HAMU is being read. All of the power switching and sequencing is controlled by the device controller and power supply circuitry on each motherboard. Power dissipation for the system is 180 mW/channel running at the 120 Hz beam crossing and 2 Hz trigger rate.

The CRID system is similar to the Drift in its conformance to the mechanical structure of the CRID physical detector. The CRID electronics is partitioned into a motherboard, which holds 186 preamplifier hybrids for 93 wire channels. This partitioning places an amplifier on each end of a sense wire and charge division allows the measurement of a z-coordinate of the detected photoelectron. The motherboard provides active circuits for calibration and sequencing of the preamplifier hybrids. Three smaller circuit boards are then connected via multipin connectors to produce the assembly shown in figure 8. The outermost boards contain the HAMU sampling hybrids, while the innermost small PC board contains the digitizing functions. A external power supply regulator board interconnects all three levels of the assembly. This system is water cooled via an aluminum finned heat exchanger mounted around the preamplifiers. The power is switched in a manner similar to the Drift system. The CRID electronics package consumes 220 milliwatts/channel at the 120 Hz data acquisition rate.

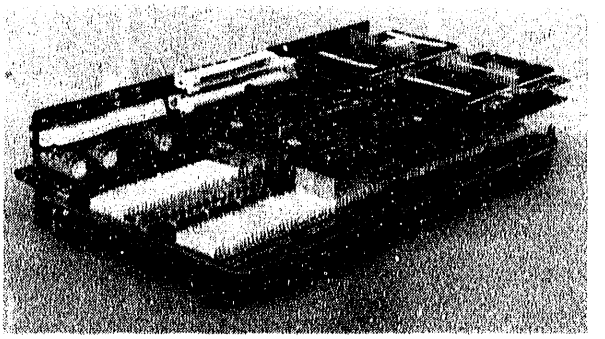

FIGURE 8

Photograph of a partially assembled CRID motherboard. Two hybrid preamplifiers are shown on the motherboard, with the HAMU, service, and power-regulation daughterboards.

8. SUMMARY AND OBSERVATIONS

The detectors of the next decade will certainly be more complex than the SLD as event rates and beam crossing frequencies are expected to be orders of magnitude larger. The SLD electronic system design experience can be extended to suggest areas of development that will be helpful for future detector designers.

The SLD preamplifier designs are largely chip and wire hybrids on multilayer printed substrates. The

rapidly developing analog ASIC technology should allow the development of highly integrated monolithic preamps for detectors. Work in this area is now underway.[24,25,26,27] Our experience with the CRID preamp (which combines the analog macrocell with the external discrete low noise JFET) suggest that the semicustom approach deserves to be considered in addition to full custom analog designs.

The use of EPLD devices in SLD helped in the system integration phase, as well as simplifying the digital system designs. Commercial development of these components continues. It is clear that for designs of moderate production volume, the EPLD approach makes more sense than the full custom design. Specialized signal processing functions, such as the DCU and Vertex CAP chip, make good economic sense for systems with clearly defined algorithms. The development of standard processing building blocks (such as the CDU/AMU) that could be shared across systems or across detectors deserves further research and development.[28,29]

The SLD design has achieved electrical noise immunity and reductions in cable plant volume through the use of fiberoptics. This advantage is coupled to the multiplexing possible with the CDU/AMU devices. Still the fiberoptic network in SLD utilized a fraction of the optical bandwidth and commercial fiberoptic technology is rapidly developing. Optical networks with greater than 1 GBit/sec capacity seem easily feasible for the next detectors.[30,31]

The packaging and power dissipation problems encountered in the SLD design will only become worse in future detectors. SLD benefits from the 120 Hz repetition rate of the Stanford Linear Collider, and uses power switching techniques to control power consumption. SLD also benefits from the benign radiation environment of the e^+e^- machine, which allows packaging electronic systems inside the detector. If the SSC and proposed B-Factory machines are typical of future detector environments, power consumption and packaging research and development will clearly be needed. The SLD design experience with dense multilayer circuit boards in curved geometries also clearly recommends development of better, more flexible routing and layout tools than are commercially available today.

The final observation from the SLD experience is the importance of a uniform system design, with standardized communications protocols and repeated use of standard component building blocks. The SLD design, with the common data acquisition structure across all the detector subsystems, shows the compactness and efficiency possible with this approach. Future efforts will certainly benefit from a similar common architecture.

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REFERENCES

1. SLD Design Report, SLAC-273, UC-34D (1988).
2. M. Breidenbach "Overview of the SLD," IEEE Trans. Nucl. Sci. NS-33, No. 1 (1986) 46.
3. M. Breidenbach and the SLD Collaboration, "A Status Report on the SLD Data Acquisition System," IEEE Trans. Nucl. Sci. NS-36 No. 1 (1989) 23.
4. D. J. Sherden, "The Data Acquisition System for SLD," IEEE Trans. Nucl. Sci. NS-3 (1987) 142.
5. R. S. Larsen, "Overview of the Data Acquisition Electronics System Design for the SLAC Linear Collider Detector (SLD)," IEEE Trans. Nucl. Sci. NS-33, No. 1 (1986) 65.
6. A. Benvenuti et al., "The Digital Data Acquisition Chain and the Cosmic Ray Trigger System for the SLD Warm Iron Calorimeter," SLAC-PUB-5066 (1989).
7. J. Hoeflich, "TCM Specification," SLD Internal document.
8. G. M. Bilei and R. Castaldi, "A FASTBUS Digital Readout Module for Streamer Tubes," IEEE Trans. Nucl. Sci. NS-35 (1988) 282.

9. A. Marchioro et al., "The Aleph Event Builder," IEEE Trans. Nucl. Sci. NS-34 (1987) 133; K. Einsweiler et al., "The Aleph Event Builder—A Multiuser FASTBUS Master," IEEE Trans. Nucl. Sci. NS-35 (1988) 316.

10. G. M. Haller, J. Moss, D. R. Freytag, D. Nelson, A. Yim, and C. Lo, "Design and Fabrication of Advanced Hybrid Circuits for High Energy Physics," IEEE Trans. Nucl. Sci. NS-35 (1988) 217.

11. E. Spencer et al., "Development of a Low Noise Preamplifier for the Detection and Position Determination of Single Electrons in a Cherenkov Ring Imaging Detector by Charge Division," IEEE Trans. Nucl. Sci. NS-35 (1988) 231.

12. F. Beconcini et al., "The Front End Electronics and the FASTBUS Readout Module for the SLD Limited Streamer Tubes," Nucl. Instrum. Methods A277 (1989) 222.

13. C. C. Lo et al., "The Hybridized Front End Electronics of the Central Drift Chamber in the Stanford Linear Collider Detector," IEEE Trans. Nucl. Sci. NS-35 (1988) 142.

14. Plessey Microelectronics, Inc., Scotts Valley, California.

15. G. M. Haller, D. R. Freytag, J. T. Walker and S. I Chae, "Performance Report for Stanford/SLAC Multichannel Sample and Hold Device," IEEE Trans. Nucl. Sci. NS-33 (1986) 221.

16. J. T. Walker et al., "Microstore—The Stanford Analog Memory Unit," IEEE Trans. Nucl. Sci. NS-32 (1985) 616.

17. S. Mackenzie, B. Nielsen, L. Paffrath, J. Russell and D. Sherden, "The Digital Correction Unit: A Data Correction/Compaction Chip," IEEE Trans. Nucl. Sci. NS-34 (1987) 250.

18. D. Phillips and A. R. Gillman, "The Cluster Arithmetic Processor—A Gate Array Design Summary," Rutherford Appleton Laboratory Report RAL-89-064 (1989).

19. C. J. S. Damerell, A. R. Gillman, and D. A. Phillips, "Real Time Data Sparsification for the SLD Vertex Detector," Proc. 1989 IEEE NSS Symposium (in print).

20. Altera Corporation, Santa Clara, California; Xilinx Corporation, San Jose, California.

21. Hewlett-Packard Corporation, Palo Alto, California.

22. G. M. Haller, D. Nelson, and D. R. Freytag, "The Analog Processing System for the Liquid Argon Calorimeter for SLD at SLAC," IEEE Trans. Nucl. Sci. NS-34, No. 1 (1986) 170.

23. G. M. Haller, J. D. Fox and S. R. Smith, "The Liquid Argon Calorimeter System for the SLC Large Detector," IEEE Trans. Nucl. Sci. NS-36, No. 1 (1989) 675.

24. H. W. Williams, "High Energy Physics Applications of Custom ICs," Proc. 1989 IEEE NSS Symposium (in print).

25. F. M. Newcomer et al., "A Fast Monolithic Preamp and Shaper for High Rate Gas Tracking Detectors," Proc. 1989 IEEE NSS Symposium (in print).

26. M. Campbell et al., "A 10 MHz Low Power CMOS Front End for Direct Readout of Pixel Detectors," Proc. 1989 IEEE NSS Symposium (in print).

27. T. Zimmerman, "A High Speed, Low Noise ASIC Preamplifier for Silicon Strip Detectors," Proc. 1989 IEEE NSS Symposium (in print).

28. S. A. Kleinfelder, "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit," Proc. 1989 IEEE NSS Symposium (in print).

29. S. A. Kleinfelder and R. P. Ely, Jr., "The SVX 128 Channel Parallel Analog Signal Acquisition Integrated Circuit," Proc. 1989 IEEE NSS Symposium (in print).

30. AMD Corporation, Sunnyvale, California; Gazelle Microelectronics, San Jose, California.

31. M. Wong, "Use of Fiber-Optics to Read Out the Silicon Microstrip Vertex Detector for the Collider Detector at Fermilab," Proc. 1989 IEEE NSS Symposium (in print).

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