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SILICON PIN DIODE ARRAY HYBRIDS FOR CHARGED PARTICLE DETECTION*

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ABSTRACT

We report on the design of silicon PIN diode array hybrids for use as charged particle detectors. A brief summary of the need for vertex detectors is presented. Circuitry, block diagrams and device specifications are included.

Presented at the Pixel Detector Workshop, Leuven, Belgium on June 1, 1988
by Stephen Shapiro

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

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1. INTRODUCTION

Hybrid silicon PIN diode arrays are promising devices for vertex and tracking detectors. Hybrid arrays having separate detector and readout structures have been developed for infrared radiation detection over the last 12 years. The technology can be easily extended to charged particle detection. The existing technology and the needs of detectors for use in high energy physics will be discussed

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2. THE SSC ENVIRONMENT

High resolution vertex and tracking devices at the SSC will be very important for revealing the detailed structure of complex events and, in particular, for the reconstruction of secondary vertices close to the primary interaction point. The expected combination of high luminosity and large particle multiplicity will present a number of problems for these devices and their associated electronics because of the high radiation environment which will prevail in the vicinity of the collision point. Therefore, it is necessary to develop vertex and tracking devices which are radiation hard, have fast response times, and have both fine spatial and multiple particle resolution.

The SSC beam crossing will occur approximately every 15 ns, and interesting events will occur every 1,000 to 10,000 crossings. The time of the hit will have to be recorded to an accuracy of one crossing time and the readout time of these detectors should be less than the mean interval between interesting events.

For a proton-proton total cross section of approximately 100 mbarn [1] the SSC will yield approximately 10^8 interactions per second when operating at its design luminosity of $10^{33}/cm^2/sec$. At a distance of 5 cm from the beam, the resulting absorbed radiation dose will be approximately 1 MRad per year.

3. DEVICE CANDIDATES

Candidates for vertex and tracking devices at the SSC include wire chambers, scintillating fiber detectors, silicon microstrip detectors, double sided microstrip detectors, silicon drift chambers, and pixel devices in the form of CCD arrays, monolithic silicon arrays, and hybrid microdiode arrays. Silicon devices offer substantially higher space, momentum, and multiple track resolution than wire chambers. It is also generally acknowledged that pixel devices are preferable to strip devices or drift devices for two track resolution.

Pixel devices, in particular silicon diode arrays, are a natural choice for vertex detectors. These devices provide three dimensional coordinate information with spatial resolution of a few microns. As the distance from the collision point to the tracking detector increases, other devices mentioned above become attractive candidates for a variety of reasons.

A vertex detector based on the use of a pixel device would provide efficient trackfinding with a minimum number of layers in the high multiplicity environment of the SSC due to the three-dimensional nature of the coordinate information provided. The absence of ambiguities in coordinate matching which are present for non-pixel devices allows the number of detector layers to be minimized, thereby reducing the size and cost of the vertex detector.

The only pixel devices presently in use in high energy physics experiments are CCDs [2]. These devices are inappropriate to the SSC environment for a variety of reasons. They have a small signal size of about 1,000 electrons which necessitates their being cooled, renders them extremely susceptible to degradation caused by radiation, and requires low noise readout electronics. CCDs have varying efficiency across their face, no off gate during readout resulting in a time/space ambiguity, and a serial readout resulting in a readout time of about 10 msec for a device with 10^5 pixels.

A number of researchers are presently working on the problem of fully integrated pixel detectors in monolithic arrays [3]. These arrays have their read out

electronics fabricated on the same high resistivity silicon as the detector diodes. Success in these efforts will result in detectors having the minimum thickness possible. However, there will be loss of flexibility. Each change in either the detector specification or the readout specification will result in not only a circuit change, but also a re-analysis of the production process as they are now intimately coupled. Monolithic arrays must be fabricated in high resistivity facilities that can handle both high resistivity silicon and also standard VLSI processing. There are far fewer of these facilities worldwide than those which can produce more conventional circuits.

4. MICRODIODES: SILICON PIN DIODE ARRAY HYBRIDS

An architecture which is appropriate for charged particle detection at the SSC is that of a hybrid [4]. The charged particle detector, a silicon PIN diode array, and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips, indium bump bonded together are the basic building blocks of a detector array.

The indium bump bonding process is one in which each diode of the detector array is bonded to an independent amplifier readout circuit on a mating VLSI chip via an array of aligned indium metal bumps that cold weld under pressure to form ohmic contact. This process allows flexibility in the selection of detector and readout electronics specifications [5]. For instance, a change in the leakage current specification of the detector array will not affect the readout electronics, nor will a change in the VLSI chip oxide thickness to accommodate a radiation hardness specification affect the detector array. Figure 1 is a schematic representation of a Microdiode hybrid.

The present readout chip allows random access to any pixel, which operates as an independent detector. By virtue of its geometry alone, each pixel detector (PIN diode) provides about 3000 times the radiation hardness of a microstrip detector. To compliment this increase in the radiation hardness of the detector diodes, one

of the present readout chips (the 10 x 64 array) has been fabricated in a technology which is radiation hard to 1 MRad of Cobalt 60 gamma rays.

The hybrid operates at room temperature, eliminating the need for a cryostat and easing the problems of installation, alignment, and accessibility for power and control cabling.

The detector thickness itself can be optimized. The PIN diode array can be fabricated to give the requisite signal (80 electrons per micron of silicon traversed). while the VLSI chip can be thinned to less than 100 microns if necessary. This feature is important for minimizing multiple-scattering effects and also for limiting the number of adjacent pixels turned on by tracks incident at large angles upon the active silicon volume.

It should be noted, that the diode anodes are indium bump bonded to the silicon readout chip, leaving the cathode available to be etched into a pattern of pads or strips. Signals picked up on the cathode pads would be available for fast triggering or for reducing the readout time by using the random access nature of the readout electronics. System considerations will determine if the cathode signals are useful.

In the present generation of readout chips, it should be noted that the power use during the write cycle is essentially zero. Power is used only when reading and cooling needs are, thus, lessened.

HARDWARE DESCRIPTION

There are two chip geometries currently being built into PIN detector arrays; a 10×64 array with 120 micron square pixels, and a 256×256 array with 30 micron square pixels. 512×512 readout arrays have, however, recently been fabricated by Hughes Aircraft Co. The diode arrays are identical as to process and differ only in that they must mate with their respective readout chips. The readout chips are similar in function, but differences between them exist. For instance, the 10×64 array has been fabricated and optimized to be radiation hard to 1 MRad at 10°K. It has a random access architecture in that a unique setting of its address

lines will select one and only one row. The 256 × 256 array, on the other hand, is random access in that the pixels are addressed via row and column shift registers. This feature makes addressing a given pixel more complicated but allows an easy implementation of a sparse scan algorithm. This particular readout chip has been optimized to collect electrons but is bipolar at the signal levels we expect.

Figure 2 is a schematic diagram of the MOSFET circuit of the 10 × 64 readout array. The diagram has been divided into its several functional portions. The section replicated for each pixel contains four MOSFETs. Signal charge is generated by the detector diode, and is fed to the gate of the signal MOSFET where it stays until a readout is made. The pixel selection circuit indicates how a sequence of address lines can select an individual pixel by turning on the gates of the V_{DD} bias MOSFET and the enable gate of the reset MOSFET. The U_{reset} signal allows the gate of the signal MOSFET to be reset to the V_{reset} level for any pixel that is enabled by the reset MOSFET. All of the signal MOSFETs are connected to a readout MOSFET (one per column) in a source follower configuration which provides power for driving an external circuit.

Figure 3 is a simple schematic of the readout addressing architecture of the 256 × 256 array. This array contains only two output nodes for the entire chip. It can be seen that by turning on all pixels on a row or column, an OR circuit is created and one will observe a signal from that pixel which has the most charge.

Figure 4 indicates schematically the coordinated sequencing of the reset line and the switches S1 and S2 in the external circuit necessary for the double correlated sampling technique used for measuring the charge collected on the gate of the signal MOSFET. The voltage difference across the correlated double sampling capacitor C_{CDS} is determined by the difference in the output prior to the reset (time 1) and after the reset (time 5). S1 is held open during the reset, insulating C_{CDS} from the large reset pulse. The analysis time per pixel is 1 microsecond.

Figure 5 is a block diagram of the high energy physics data acquisition system. A Sun Microsystems Sun-3/110LC-4 workstation controls a VME system crate

housing a Sun 3/E CPU, a Motorola 68020 bus converter board, amplifiers, ADCs, digital signal processors, and a clock generator. The digital signal processor is a Motorola DSP56001. This device acquires data at a rate of 10 MIPS, processes it, and passes it to the Sun 3/E. The bus converter board, a Parity systems AV20 dual port processor, interfaces the local analog bus (PECKBUS) to the VME standard.

The noise performance of the 10 × 64 readout chip at 10°K has been measured to be 45 electrons rms referred back to the input. This is within a factor of two of the 1/f noise of the input signal MOSFET. At room temperature, the noise will probably be somewhat higher. However, with a moderate effort to maintain low system noise, a noise level of about 200 electrons is achievable. If the noise performance is as expected, detectors thinner than the traditional 300 micron thick PIN devices currently being fabricated for high energy physics would still offer more than adequate signal-to-noise performance.

5. RESEARCH PROGRESS

Dr. Arens, Dr. Jernigan, and their collaborators have designed and built 10 micron infrared cameras. The details of one camera have been published in Applied Optics [6]. The camera, based on a 10 × 64 array of 120 micron square pixels, has been used at the University of Arizona 61" and 90" telescopes, the University of Wyoming 90" telescope, and the NASA Infrared Telescope Facility on Mauna Kea, Hawaii. Two detector chips were used: an arsenic doped and a gallium doped silicon array, each bump bonded to a 10× 64 Hughes readout chip. The camera consisted of the detector, the Dewar, the readout electronics and computers, and the control computer. The computers were Sun Microsystems workstations with additional multibus cards for input and output.

In 1987, the infrared camera was reconfigured to include a germanium PIN diode array as the detector element. This detector was used at the National Laser Users Facility of the Laboratory for Laser Energetics at the University of Rochester

to obtain x-ray images of laser targets [7]. Figure 6 is a photograph of one of the germanium detectors bump bonded to a 10 × 64 array.

Using Detector Development Funds from the Department of Energy, a contract was made with Micron Semiconductor to design and fabricate two silicon PIN diode arrays. The design and the masks necessary to fabricate the silicon chips have been completed. The PIN diodes are presently in production, with the first articles due this calendar year (1988). The array specifications were chosen to allow the detector chips to mate with the corresponding Hughes Aircraft Co. readout chips. The arrays being fabricated are a 10 × 64 array with 120 micron square pixels and a 256 × 256 array with 30 micron square pixels.

Additional Detector Development funds were used to begin the fabrication of the dedicated high energy physics data acquisition system described above. The amplifier/ADC/DSP56001 boards and the clock generator in the present system, however, are circuits remaining from the infrared data acquisition system. These need to be redesigned to high energy physics criteria.

A data acquisition and display software package based on the infrared system is being written. The operating system is UNIX, the DSP has been programmed in assembler language, and various control functions are written in Magic/L, an interactive language derived from Forth. The Parity AV20 dual port processor has been programmed in C, and the DSP will be reprogrammed in C.

At the present time, a system exists which can read either of our two detector geometries, 10 × 64 and 256 × 256. When the new detectors arrive, we will be ready to begin our program of testing and characterizing these devices. Table I is a current summary of device characteristics. Figure 7 is a photograph of a 256 × 256 Hughes readout chip.

6. FUTURE DIRECTION

Our efforts during the coming years will include testing and characterizing the new devices, designing and fabricating the remaining electronics to reflect the needs of these detectors, and exposing the new detectors to cosmic ray tests and beam tests.

To respond to data which may accumulate during the readout cycle, gating circuitry can be designed to inhibit the flow of charge between the detector and the readout chip after an event is tagged. Alternatively, an input buffer can be added to the design which leaves the detector alive but which does not allow alterations of the data being read out.

To avoid the confusion caused by data being recorded from various beam crossings, a design must be adopted which allows the data and the time of arrival to be correlated. The chips being built have been designed to provide a fast indication that a particle has been recorded, however, we have not yet explicitly studied this feature in the laboratory. This ability, interesting in its own right if confirmed, can be used in later design iterations to strobe shift registers which do, in fact, make use of the time information while retaining the small pixel size of our present chips.

We also intend to propose a redesign of the Hughes readout chip to include some of these requirements. These include radiation hardness, increased readout speed, and data recording with time tagging.

We will address various data acquisition problems particular to the SSC. It is our intention to design a prototypical barrel vertex detector, including the specification of the global architecture. We hope to address questions relating to the usefulness of having signal processing local to the detectors, the degree of parallelism required of the readout structure, mounting and cooling schemes, and the design of the optimum host computer.

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TABLE I

SUMMARY OF DEVICE PARAMETERS

Array Dimension	10 × 64	256 × 256
Pixel Size	120 microns	30 microns
Detector Material	Germanium Silicon	Germanium Silicon
Number of Output Channels	10	2
Power During "Write" Cycle	0 mW	0 mW
Power During Read Cycle	10 mW	2 mW
Present Clock Speed	1 MHz	1 MHz
Theoretical Clock Speed	10 MHz	10 MHz
Readout Mode	Random Access	Random Access
Processing Power	10 MIPS/channel	10 MIPS/channel
Radiation Hardness	1 MRad	?
Noise at 10°K	45 electrons rms	?
System Noise at Room Temperature	200 electrons rms	?
Operating Temperature	Ge - Cool Si - Room Temp.	Ge - Cool Si - Room Temp.
Sparse Scan	No	Yes
Fast Signal	No	?
Input Gating	No	No
Smart Pixel	No	No

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FIGURE CAPTIONS

1. Schematic representation of a hybrid detector.
2. Schematic drawing of the readout electronics of the 10 × 64 readout array.
3. Schematic representation of the readout architecture of the 256 × 256 readout array.
4. Schematic drawing of the off-chip readout electronics highlighting the double correlated sampling technique, with a timing diagram included.
5. A block diagram of the readout and display electronics
6. A photograph of a 10 × 64 readout chip bump bonded to a Germanium PIN diode array.
7. A photograph of a 256 × 256 readout chip.

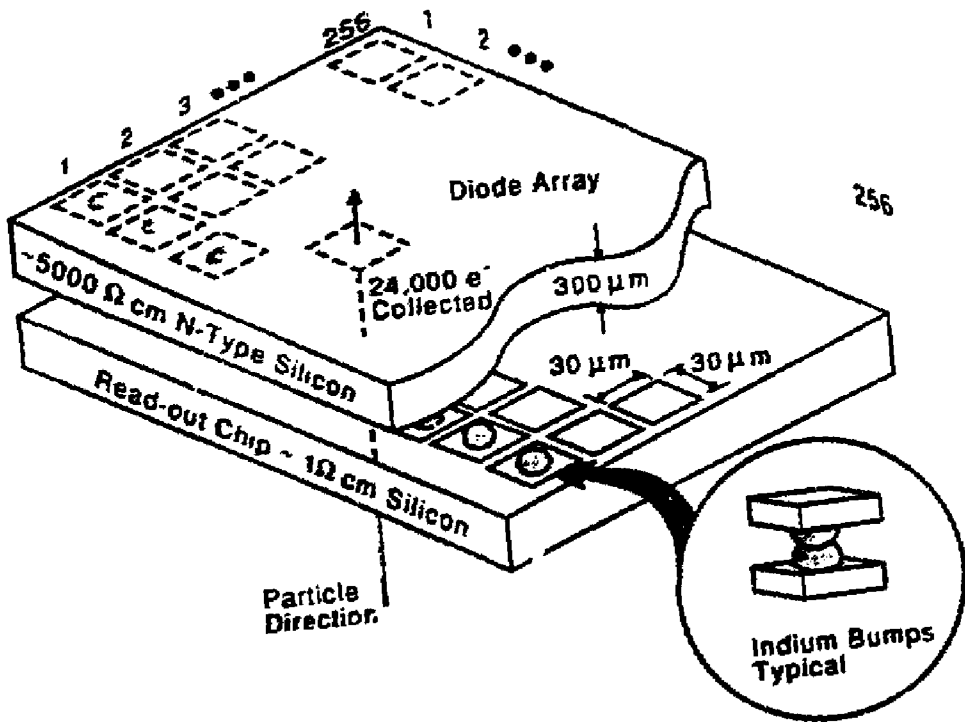


Fig. 1

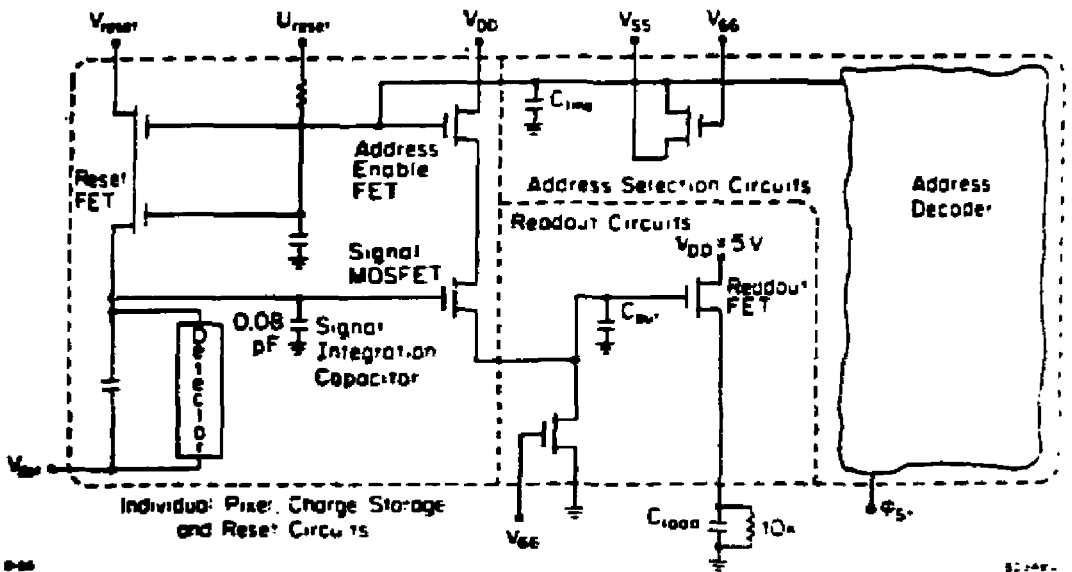


Fig. 2

256 x 256 SCHEMATIC

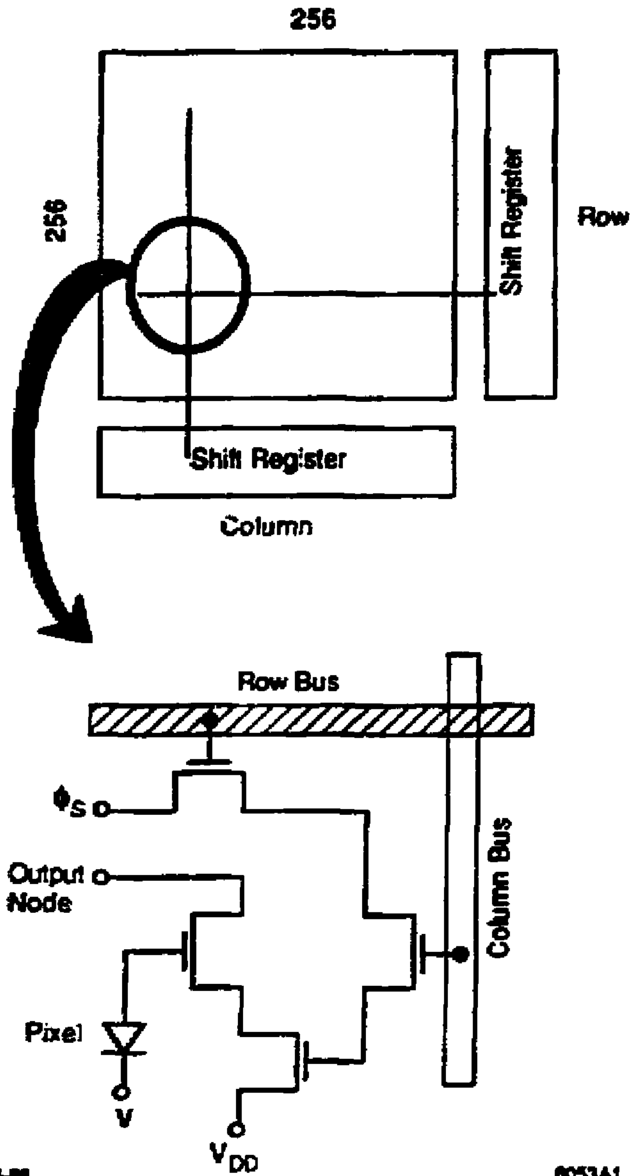
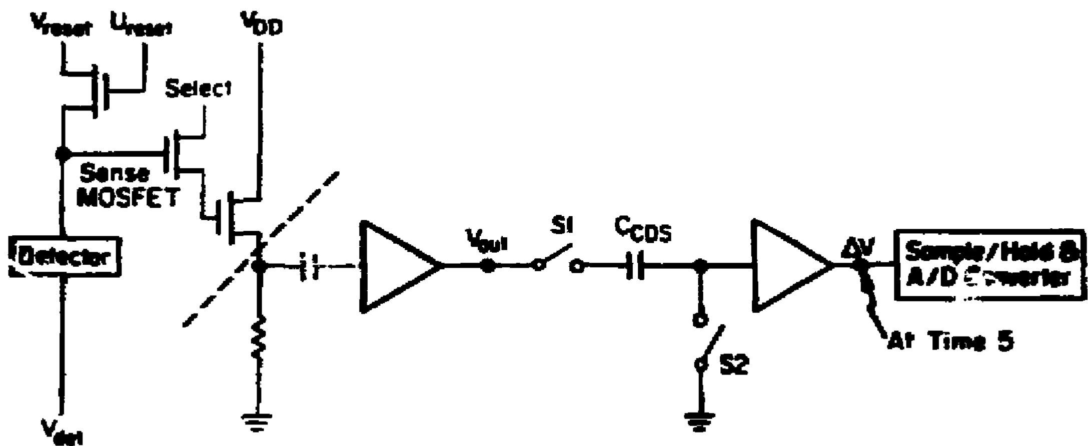


Fig. 3



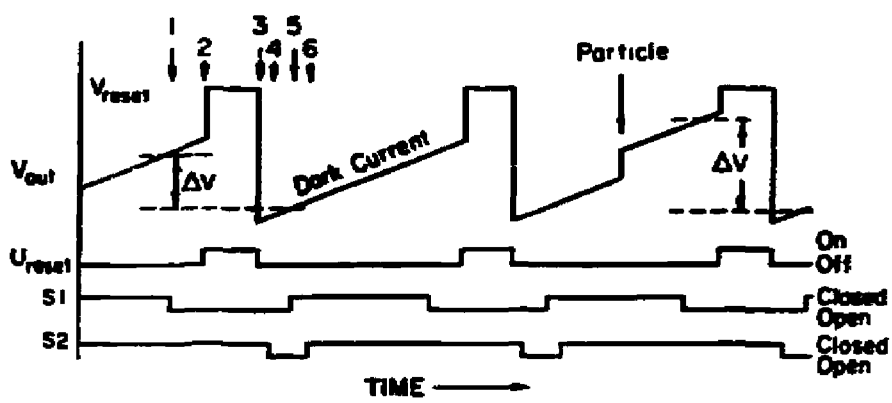


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Fig. 4

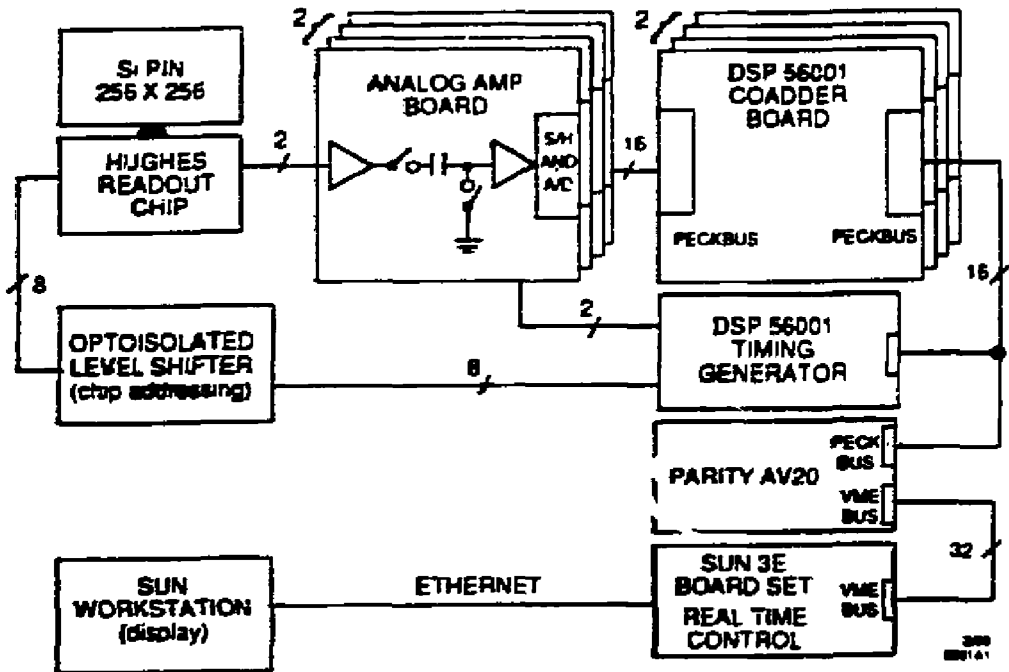


Fig. 5

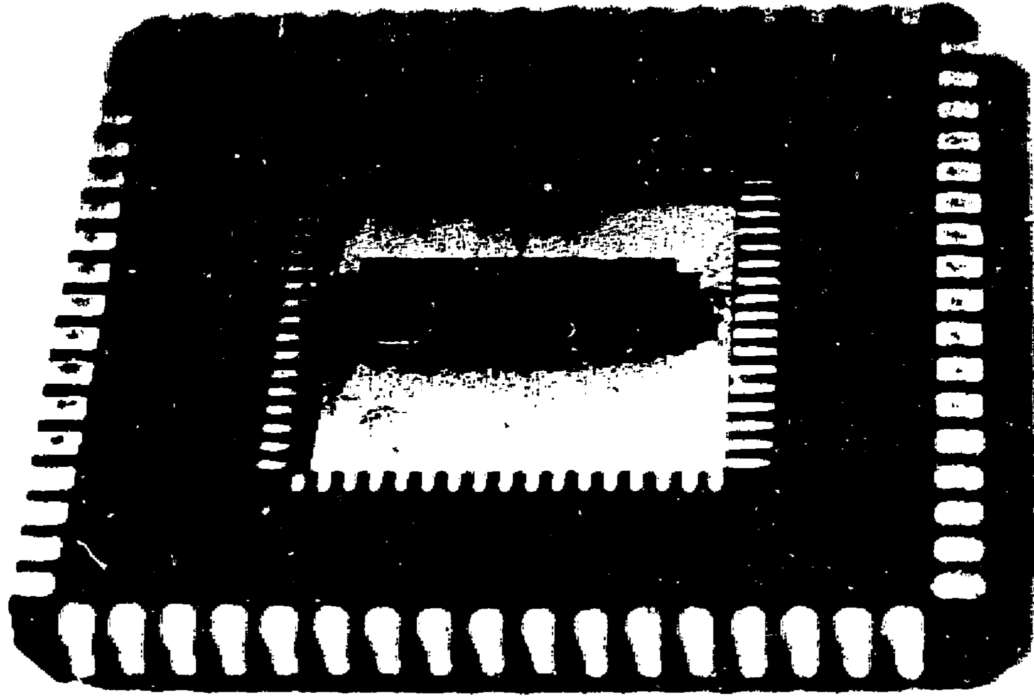
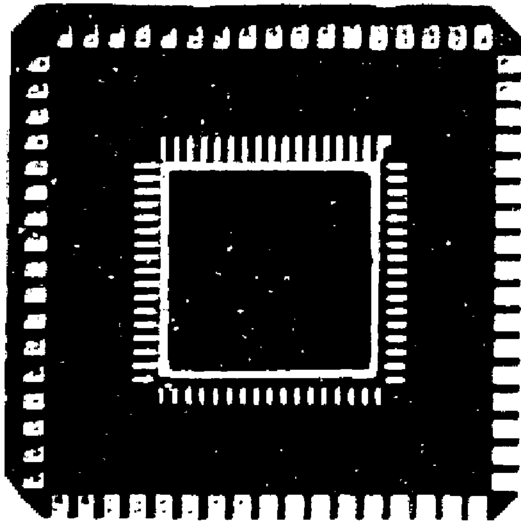


Fig. 6



9-88 Fig. 7

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5. RESEARCH PROGRESS

Dr. Arens, Dr. Jernigan, and their collaborators have designed and built cameras for 10 μm infrared wavelength. The details of one camera have been published in Applied Optics [7]. The camera, based on a 10×64 array of 120 μm square pixels, has been used at the University of Arizona 61″ and 90″ telescopes, the University of Wyoming 90″ telescope, and the NASA Infrared Telescope Facility on Mauna Kea, Hawaii. Two detector chips were used; an arsenic doped and a gallium doped silicon array, each bump bonded to a 10×64 Hughes readout chip. The camera consisted of the detector, the Dewar, the readout electronics and computers, and the control computer. The computers were Sun Microsystems workstations with additional multibus cards for input and output.

In 1987, the infrared camera was reconfigured to include a germanium PIN diode array as the detector element. This detector was used at the National Laser Users Facility of the Laboratory for Laser Energetics at the University of Rochester to obtain x-ray images of laser targets [8]. Figure 6 is a photograph of one of the germanium detectors bump bonded to a 10×64 array.

Using Detector Development Funds from the Department of Energy, a contract was made with Micron Semiconductor to design and fabricate two silicon PIN diode arrays. The design and the masks necessary to fabricate the silicon chips have been completed. The PIN diodes are presently in production, with the first articles due this calendar year (1988). The array specifications were chosen to allow the detector chips to mate with the corresponding Hughes Aircraft Co. readout chips. The arrays being fabricated are a 10×64 array with 120 μm square pixels and a 256×256 array with 30 μm square pixels.

Additional Detector Development funds were used to begin the fabrication of the dedicated high energy physics data acquisition system described above. The amplifier/ADC/DSP56001 boards and the clock generator in the present system, however, are circuits remaining from the infrared data acquisition system. These need to be redesigned to high energy physics criteria.

A data acquisition and display software package based on the infrared system is being written. The operating system is UNIX, the DSP has been programmed in assembler language, and various control functions are written in Magic/L, an interactive language derived from Forth. The Parity AV20 dual port processor has been programmed in C, and the DSP will be reprogrammed in C.

At the present time, a system exists which can read either of our two detector geometries: 10×64 and 256×256. When the new detectors arrive, we will be ready to begin our program of testing and characterizing these devices. Table I is a current summary of device characteristics. Figure 7 is a photograph of a 256×256 Hughes readout chip.

6. FUTURE DIRECTION

Our efforts during the coming years will include testing and characterizing the new devices, designing and fabricating the remaining electronics to reflect the needs of these detectors, and exposing the new detectors to cosmic ray tests and beam tests.

To respond to data which may accumulate during the readout cycle, gating circuitry can be designed to inhibit the flow of charge between the detector and the readout chip after an event is tagged. Alternatively, an input buffer can be added to the design which leaves the detector alive but which does not allow alterations of the data being read out.

To avoid the confusion caused by data being recorded from various beam crossings, a design must be adopted which allows the data and the time of arrival to be correlated. The chips being built have been designed to provide a fast indication that a particle has been recorded, however, we have not yet explicitly studied this feature in the laboratory. This ability, interesting in its own right if confirmed, can be used in later design iterations to strobe shift registers which do, in fact, make use of the time information while retaining the small pixel size of our present chips.

We also intend to propose a redesign of the Hughes readout chip to include some of these requirements. These include radiation hardness, increased readout speed, and data recording with time tagging.

We will address various data acquisition problems particular to the SSC. It is our intention to design a prototypical barrel vertex detector, including the specification of the global architecture. We hope to address questions relating to the usefulness of having signal processing local to the detectors, the degree of parallelism required of the readout structure, mounting and cooling schemes, and the design of the optimum host computer.

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TABLE I

SUMMARY OF DEVICE PARAMETERS

Array Dimension	10 × 64	256 × 256
Pixel Size	120 μm	30 μm
Detector Material	Germanium	Germanium
	Silicon	Silicon
Number of Output Channels	10	2
Power During "Write" Cycle	0 mW	0 mW
Power During Read Cycle	10 mW	2 mW
Present Clock Speed	1 MHz	1 MHz
Theoretical Clock Speed	10 MHz	10 MHz
Readout Mode	Random Access	Random Access
Processing Power	10 MIPS/channel	10 MIPS/channel
Radiation Hardness	1 Mrad	?
Noise at 10K	45 electrons rms	?
System Noise at Room Temperature	200 electrons rms	?
Operating Temperature	Ge - Cool	Ge - Cool
	Si - Room Temp.	Si - Room Temp.
Sparse Scan	No	Yes
Fast Signal	No	?
Input Gating	No	No
Smart Pixel	No	No

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FIGURE CAPTIONS

1. Schematic representation of a hybrid detector.
2. Schematic drawing of the readout electronics of the 10 × 64 readout array.
3. Schematic representation of the readout architecture of the 256 × 256 readout array.
4. Schematic drawing of the off-chip readout electronics highlighting the double correlated sampling techniqne, with a timing diagram included.
5. A block diagram of the readout and display electronics.
6. A photograph of a 10×64 readout chip bump bonded to a Germanium PIN diode array.
7. A photograph of a 256 × 256 readout chip.

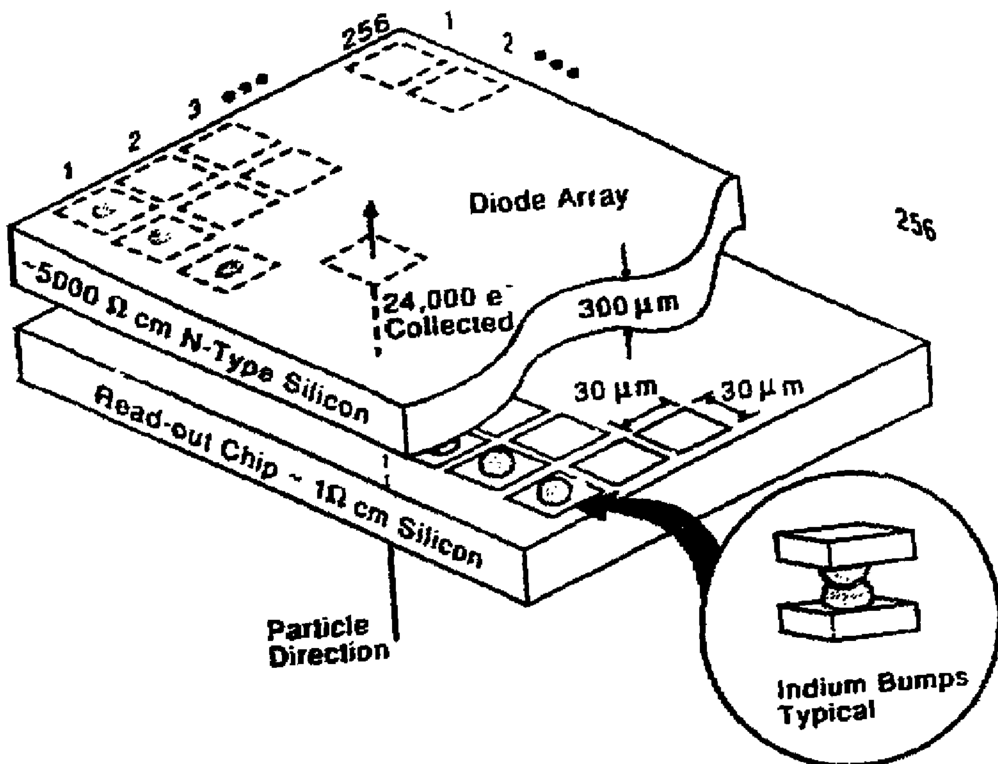


Fig. 1

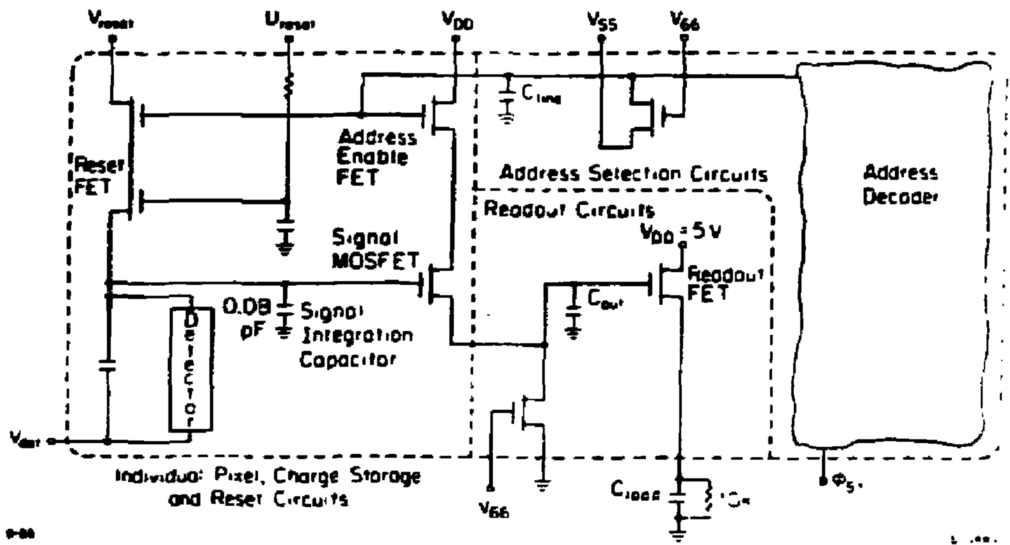


Fig. 2

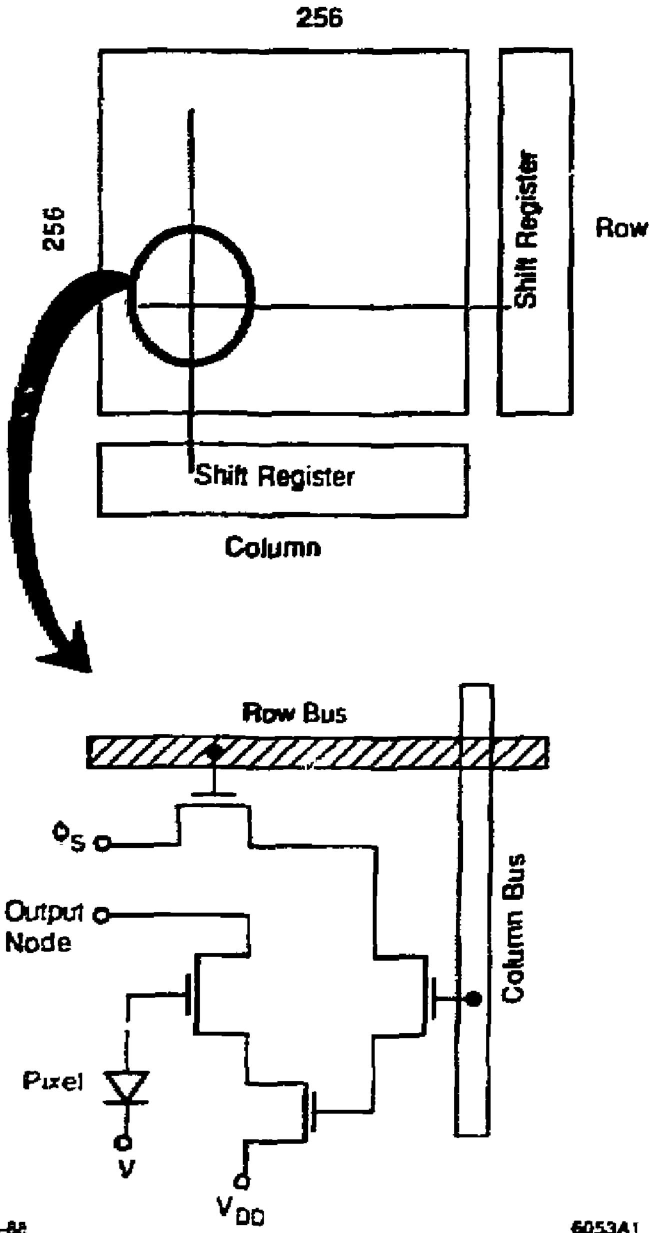
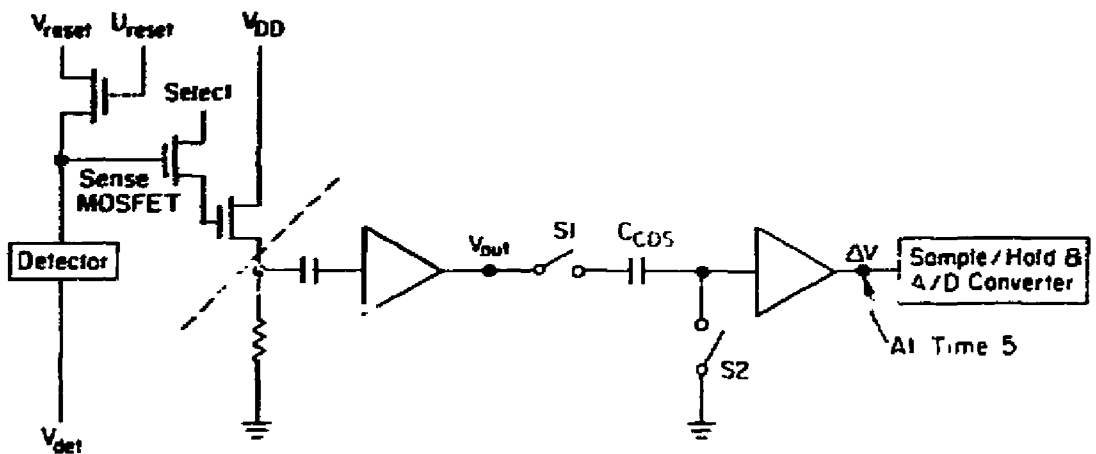


Fig. 3



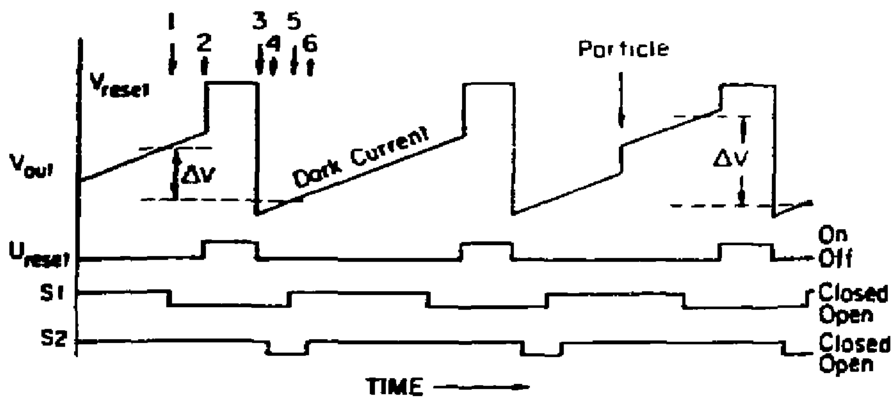


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Fig. 4

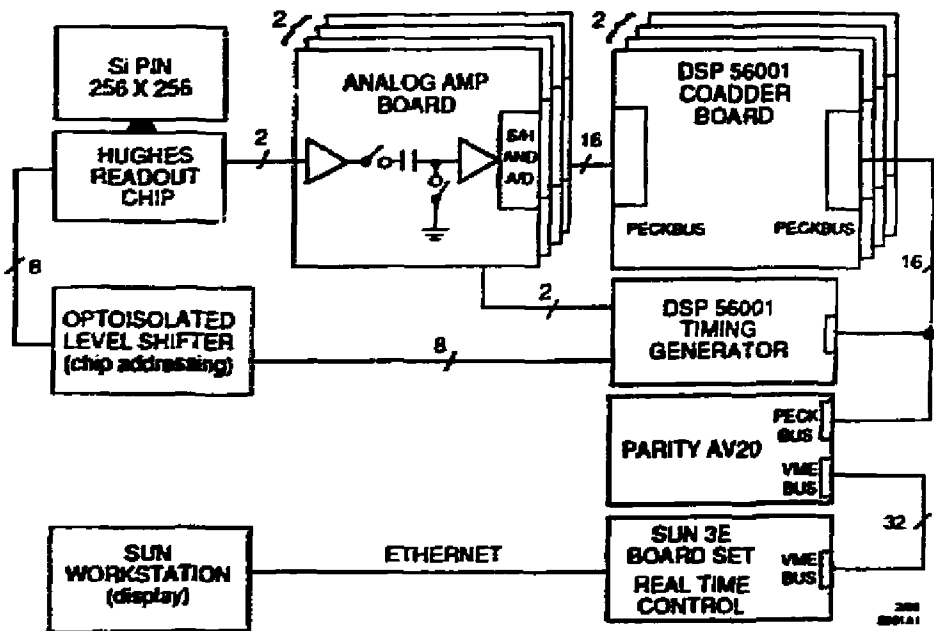
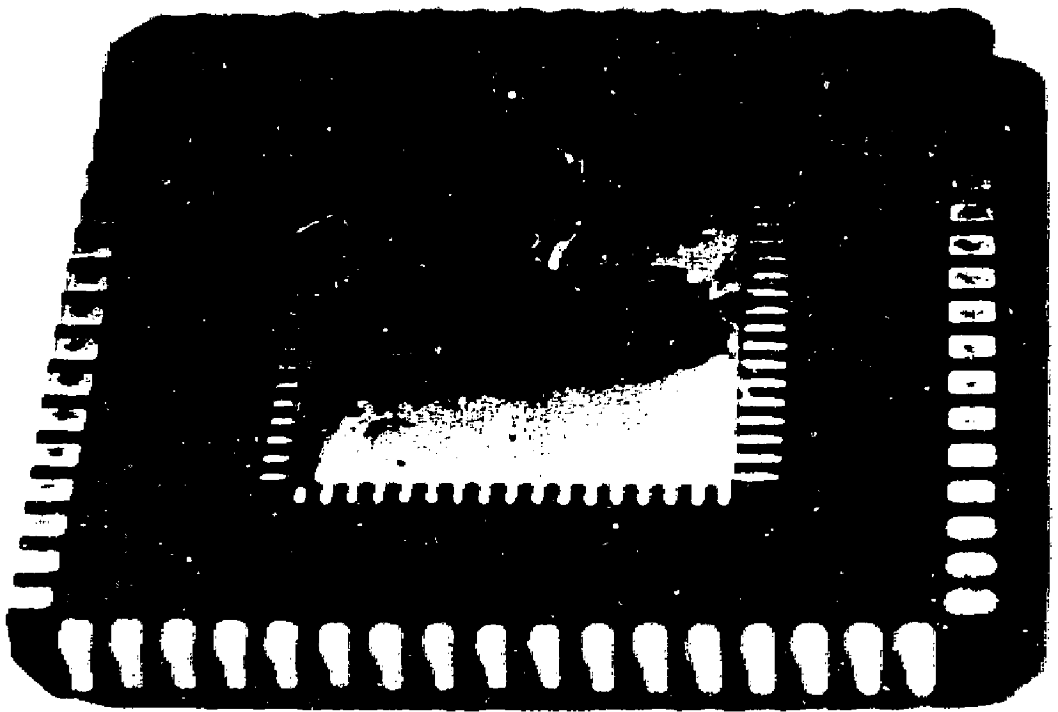


Fig. 5



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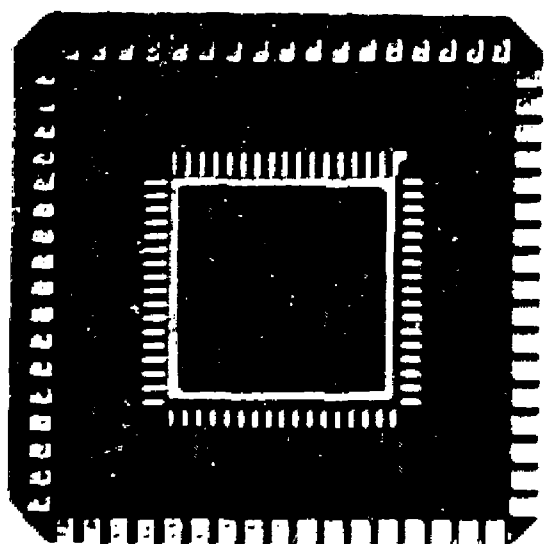

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